MSP430G2x44 混合信号微控制器

1 器件概述

1.1 特性

- 低电源电压范围：1.8V 至 3.6V
- 超低功耗
  - 激活模式：270μA（在 1MHz 频率和 2.2V 电压条件下）
  - 待机模式：1μA
  - 关闭模式（RAM 保持）：0.1μA
- 可在不到 1μs 的时间里超快速地从待机模式唤醒
- 16 位精简指令集 (RISC) 架构，62.5ns 指令周期时间
- 基本时钟模块配置
  - 带有四个已校准频率的高达 16MHz 的内部频率
  - 内部超低功率低频 (LF) 振荡器
  - 32kHz 晶振
  - 高达 16MHz 的高频 (HF) 晶振
  - 谐振器
  - 外部数字时钟源
  - 外部电阻器
- 具有 3 个捕获/比较寄存器的 16 位 Timer_A
- 具有 3 个捕获/比较寄存器的 16 位 Timer_B
- 通用串行通信接口(USCI)
  - 增强型通用异步收发器 (UART) 支持自动波特率侦测 (LIN)
  - IrDA 编码器和解码器
  - 同步串行外设接口 (SPI)
  - I^2C
- 具有内部基准、采样和保持、自动扫描和数据传输控制器的 10 位 200ksps 模数转换器 (ADC)
- 欠压检测器
- 串行板上编程、无需外部编程电压、由安全熔丝实现的可编程代码保护
- 引导加载程序 (BSL)
- 片上仿真模块
- 系列产品
  - MSP430G2444
    - 8KB + 256B 闪存存储器
    - 512B RAM
  - MSP430G2544
    - 16KB + 256B 闪存存储器
    - 512B RAM
  - MSP430G2744
    - 32KB + 256B 闪存存储器
    - 1KB RAM
- Section 3 汇总了可用的系列产品成员
- 封装选项
  - 薄型小外形尺寸封装 (TSSOP)：38 引脚 (DA)
  - 四方扁平无引线封装 (QFN)：40 引脚 (RHA)
  - 芯片级球状引脚栅格阵列封装 (DSBGA)：49 引脚 (YFF)
  - 塑料双列直插式封装 (PDIP)：40 引脚 (N) 可用于和 PMS430G2744IN40 相同的采样数量
- 要获得完整的模块说明，请参见《*MSP430x2xx 系列产品用户指南*》（文献编号：SLAU144）

1.2 应用范围

- 传感器系统
- 射频传感器前端

1.3 说明

德州仪器 (TI) 的 MSP430™ 超低功耗微控制器系列由几个器件组成，这些器件针对不同应用特有不同的外设集。 这种架构与 5 种低功耗模式相组合，专为在便携式测量应用中延长电池使用寿命而优化。 该器件具有一个强大的 16 位 RISC CPU，16 位寄存器和有助于获得最大编码效率的常数发生器。 此数控振荡器 (DCO) 可使器件在不到 1μs 的时间内实现从低功率模式唤醒至激活模式。

MSP430G2x44 系列是一款超低功耗混合信号微控制器，此微控制器具有 2 个内置 16 位定时器，1 个通用串行通信接口 (USCI)，具有集成基准和数据传输控制器 (DTC) 的 10 位模数转换器 (ADC)，以及 32 个输入输出 (I/O) 引脚。

典型应用包括传感器系统，此类系统负责捕获模拟信号，将之转换为数字值，随后对数据进行处理以进行显示或传送至一个主机系统。 独立射频 (RF) 传感器前端是另外一个应用领域。

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

器件信息(1)

部件号	封装	封装尺寸(2)
MSP430G2744DA	薄型小外形尺寸封装 (TSSOP) (38)	12.5mm x 6.2mm
MSP430G2744RHA	VQFN (40)	6mm x 6mm
MSP430G2744YFF	DSBGA (49)	3.1mm x 3.1mm
PMS430G2744N	PDIP (40)	52.46mm x 13.71mm

(1) 要获得所有可用器件的最新部件、封装和订购信息，请参见节 8中的*封装选项附录*或浏览 TI 网站 www.ti.com。
(2) 这里显示的尺寸为近似值。 要获得包含误差值的封装尺寸，请参见节 8中的*机械数据*。

1.4 功能方框图

图 1-1 显示了 MSP430G2x44 器件的功能框图。

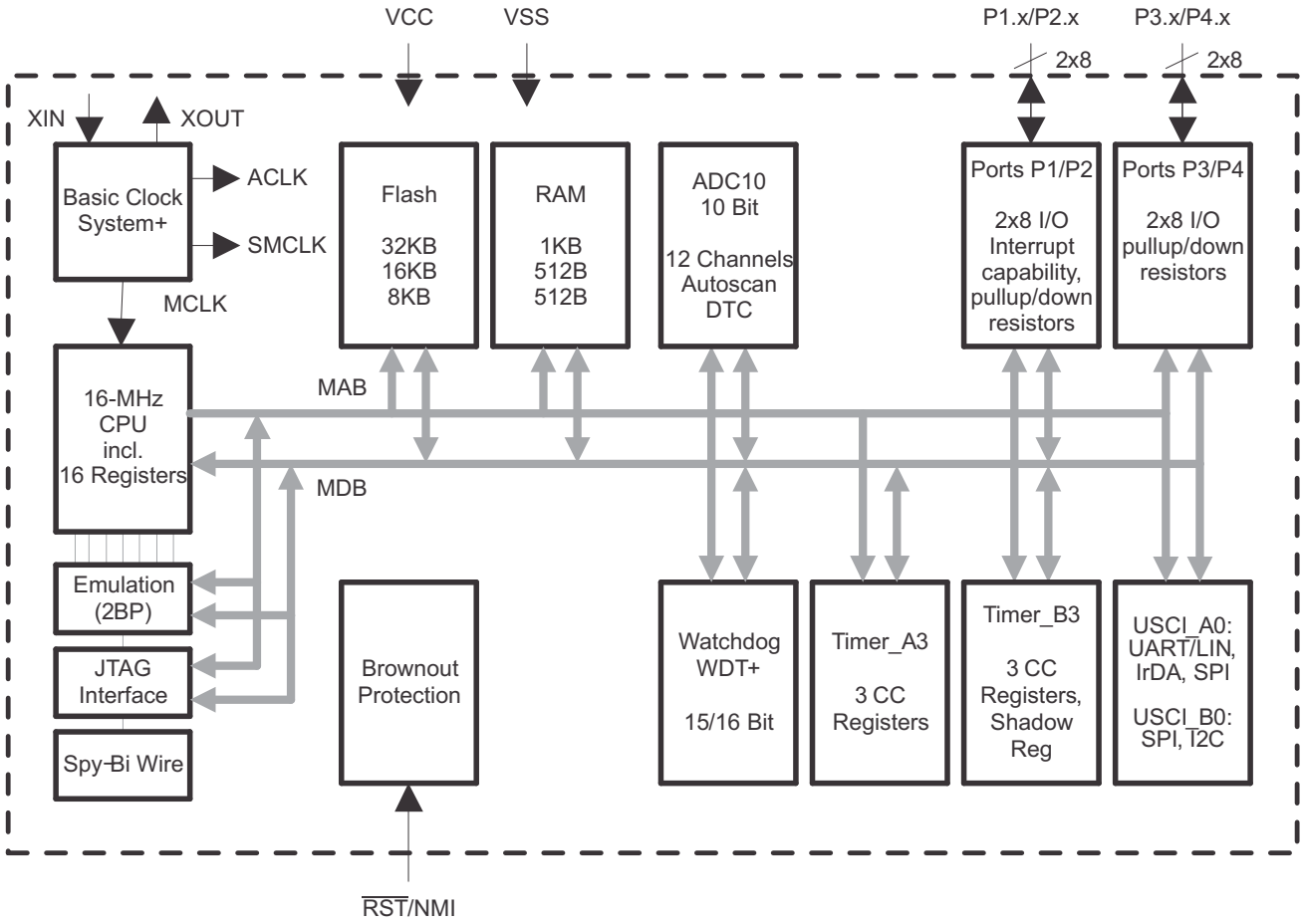

图 **1-1.** 功能方框图

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2 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C **Page**

- 通篇更改文档格式，其中包括添加章节编号 1
- 已添加器件信息表 2
- Added Section 3; moved and renamed Table 3-1 5
- Corrected size of RAM for MSP430G2744 in Table 3-1 5
- Added Section 5 and moved all electrical specifications to it 13
- Added Section 5.2 and moved T_{stg} to it 13
- 添加了节 7并将工具支持、器件命名规则、ESD 注意事项、商标部分移至其中 69
- 增加了节 8 73

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3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison(1)(2)

Device	BSL	EEM	Flash (KB)	RAM (B)	Timer_A	Timer_B	ADC10 Channel	USCI_A0, USCI_B0	Clock	I/O	Package Type
MSP430G2744IRHA40	1	1	32	1K	TA3	TB3	12	1	HF, LF, DCO, VLO	32	40-QFN
MSP430G2744IDA38										32	38-TSSOP
MSP430G2744IYFF										32	49-DSBGA
MSP430G2544IRHA40	1	1	16	512	TA3	TB3	12	1	HF, LF, DCO, VLO	32	40-QFN
MSP430G2544IDA38										32	38-TSSOP
MSP430G2544IYFF										32	49-DSBGA
MSP430G2444IRHA40	1	1	8	512	TA3	TB3	12	1	HF, LF, DCO, VLO	32	40-QFN
MSP430G2444IDA38										32	38-TSSOP
MSP430G2444IYFF										32	49-DSBGA

(1) For the most current package and ordering information, see the *Package Option Addendum* in 节 8, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pin diagram for the 38-pin DA package.

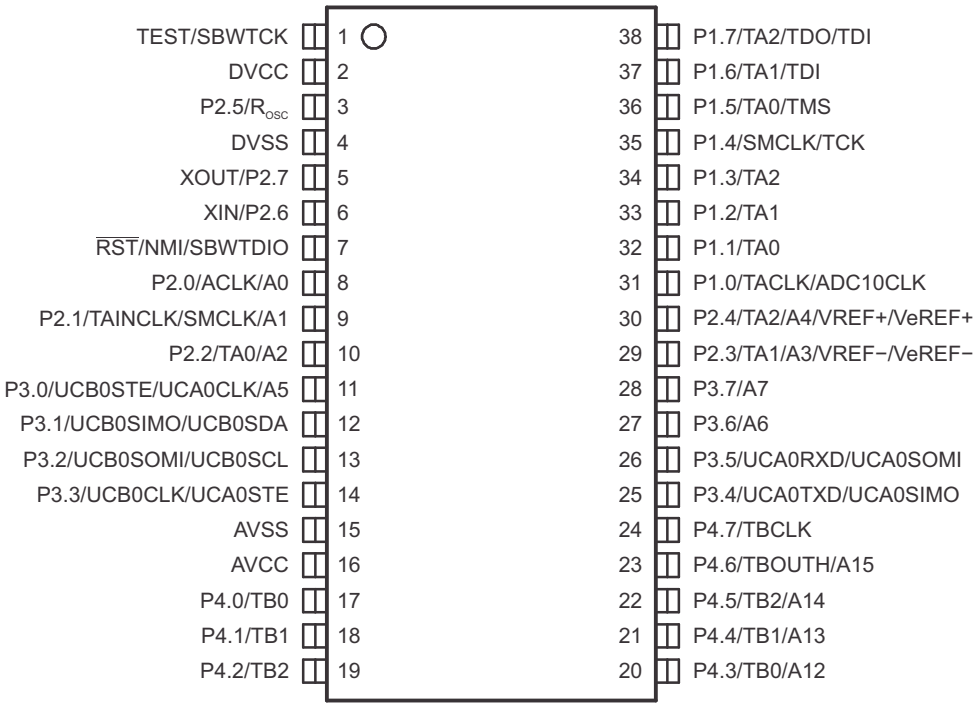

Figure 4-1. 38-Pin TSSOP (DA Package) (Top View)

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Figure 4-2 shows the pin diagram for the 40-pin N package.

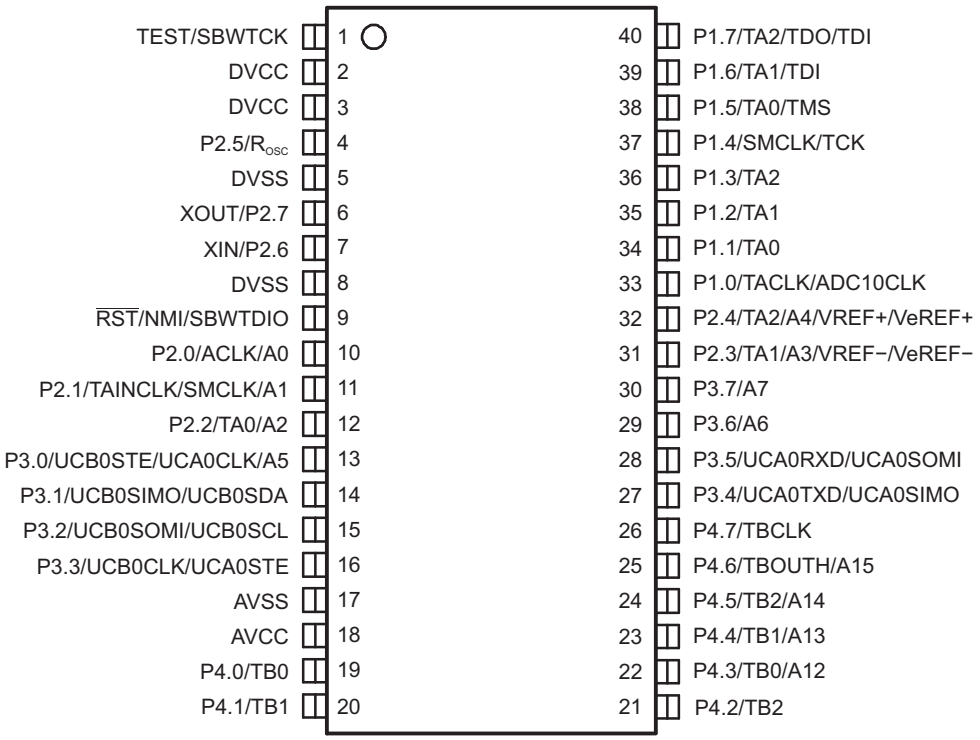

Figure 4-2. 40-Pin PDIP (N Package) (Top View)

Figure 4-3 shows the pin diagram for the 40-pin RHA package.

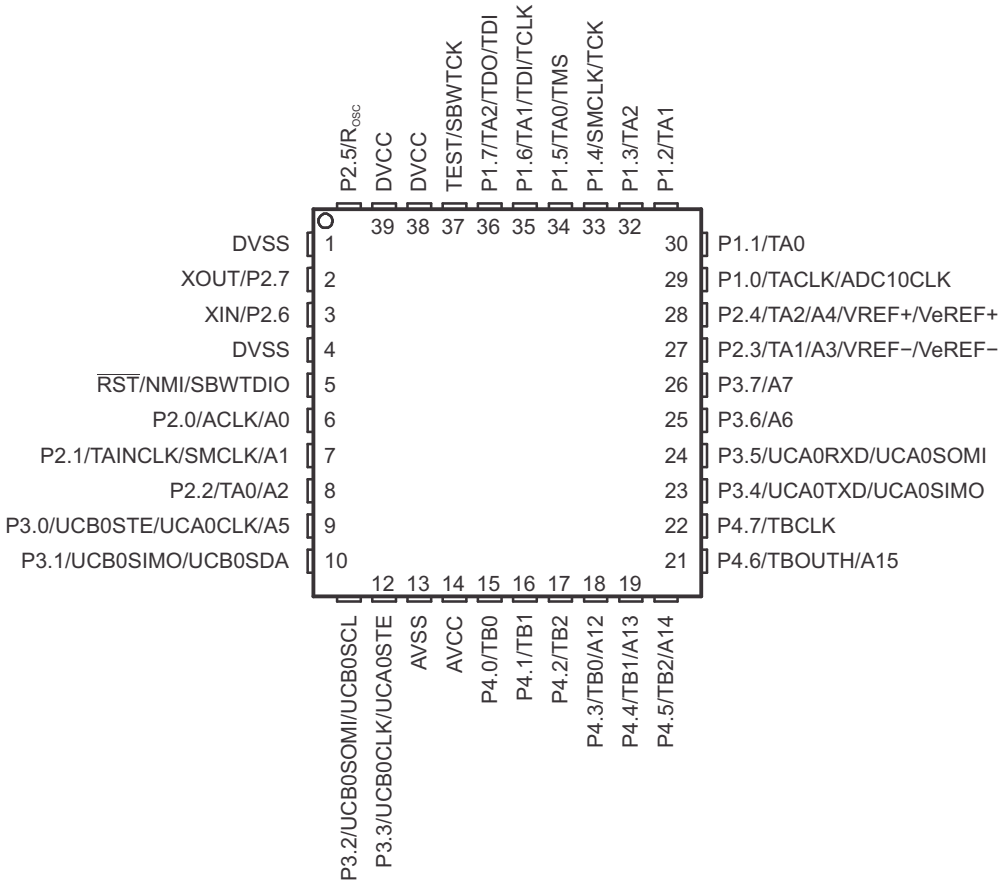

Figure 4-3. 40-Pin QFN (RHA Package) (Top View)

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Figure 4-4 shows the pin diagram for the 49-pin YFF package.

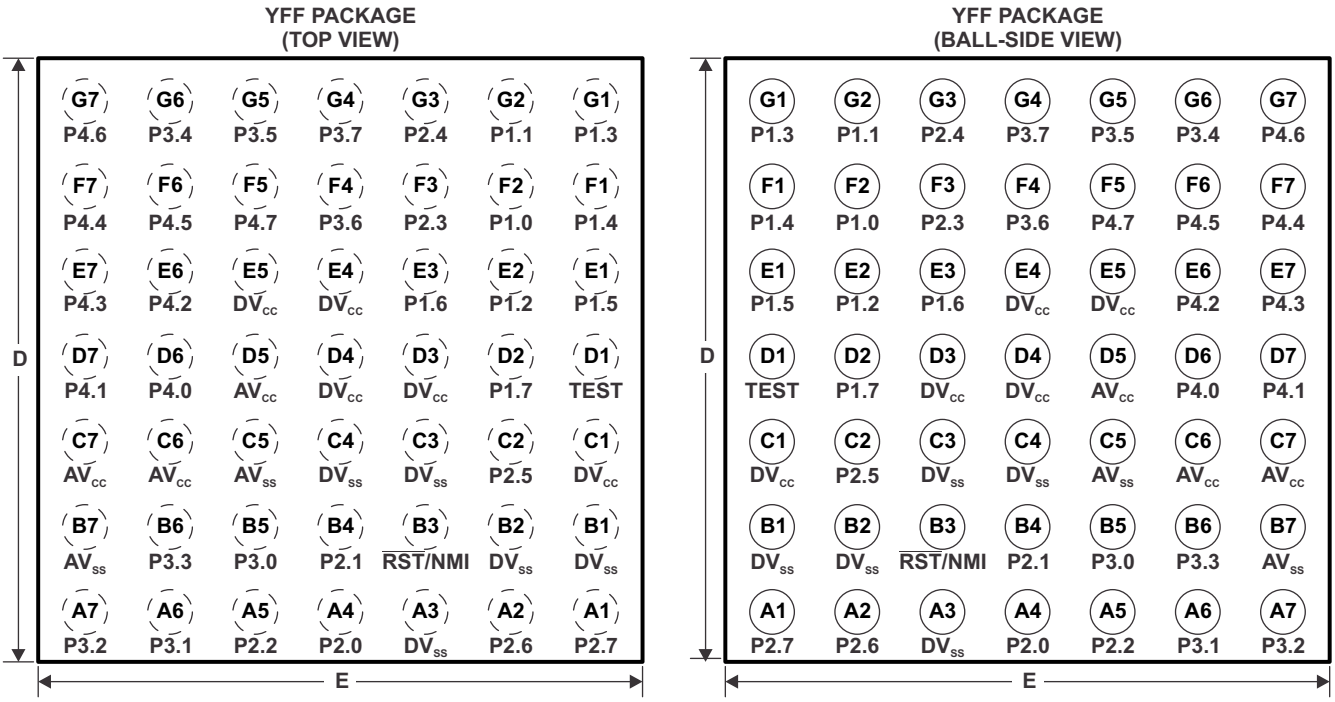

Figure 4-4. 49-Pin DSBGA (YFF Package)

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Terminal Functions

TERMINAL					I/O	DESCRIPTION
NAME	NO.					
	YFF	DA	N	RHA		
P1.0/TACLK/ADC10CLK	F2	31	33	29	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ADC10, conversion clock
P1.1/TA0	G2	32	34	30	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: OUT0 output; BSL transmit
P1.2/TA1	E2	33	35	31	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: OUT1 output
P1.3/TA2	G1	34	36	32	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: OUT2 output
P1.4/SMCLK/TCK	F1	35	37	33	I/O	General-purpose digital I/O pin SMCLK signal output Test Clock input for device programming and test
P1.5/TA0/TMS	E1	36	38	34	I/O	General-purpose digital I/O pin Timer_A, compare: OUT0 output Test Mode Select input for device programming and test
P1.6/TA1/TDI/TCLK	E3	37	39	35	I/O	General-purpose digital I/O pin Timer_A, compare: OUT1 output Test Data Input or Test Clock Input for programming and test
P1.7/TA2/TDO/TDI(1)	D2	38	40	36	I/O	General-purpose digital I/O pin Timer_A, compare: OUT2 output Test Data Output or Test Data Input for programming and test
P2.0/ACLK/A0	A4	8	10	6	I/O	General-purpose digital I/O pin ACLK output ADC10, analog input A0
P2.1/TAINCLK/ SMCLK/A1	B4	9	11	7	I/O	General-purpose digital I/O pin Timer_A, clock signal at INCLK, SMCLK signal output ADC10, analog input A1
P2.2/TA0/A2	A5	10	12	8	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input; BSL receive, compare: OUT0 output ADC10, analog input A2
P2.3/TA1/A3/ V_{REF-}/V_{eREF-}	F3	29	31	27	I/O	General-purpose digital I/O pin Timer_A, capture CCI1B input, compare: OUT1 output ADC10, analog input A3 Negative reference voltage output/input
P2.4/TA2/A4/ V_{REF+}/V_{eREF+}	G3	30	32	28	I/O	General-purpose digital I/O pin Timer_A, compare: OUT2 output ADC10, analog input A4 Positive reference voltage output/input
P2.5/R_{OSC}	C2	3	4	40	I/O	General-purpose digital I/O pin Input for external DCO resistor to define DCO frequency

(1) TDO or TDI is selected via JTAG instruction.

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Table 4-1. Terminal Functions (continued)

TERMINAL					I/O	DESCRIPTION
NAME	NO.					
	YFF	DA	N	RHA		
XIN/P2.6	A2	6	7	3	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin
XOUT/P2.7	A1	5	6	2	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin(2)
P3.0/UCB0STE/ UCA0CLK/A5	B5	11	13	9	I/O	General-purpose digital I/O pin USCI_B0 slave transmit enable USCI_A0 clock input/output ADC10, analog input A5
P3.1/UCB0SIMO/ UCB0SDA	A6	12	14	10	I/O	General-purpose digital I/O pin USCI_B0 slave in, master out in SPI mode USCI_B0 SDA I2C data in I2C mode
P3.2/UCB0SOMI/ UCB0SCL	A7	13	15	11	I/O	General-purpose digital I/O pin USCI_B0 slave out, master in SPI mode USCI_B0 SCL I2C clock in I2C mode
P3.3/UCB0CLK/ UCA0STE	B6	14	16	12	I/O	General-purpose digital I/O pin USCI_B0 clock input/output USCI_A0 slave transmit enable
P3.4/UCA0TXD/ UCA0SIMO	G6	25	27	23	I/O	General-purpose digital I/O pin USCI_A0 transmit data output in UART mode USCI_A0 slave in, master out in SPI mode
P3.5/UCA0RXD/ UCA0SOMI	G5	26	28	24	I/O	General-purpose digital I/O pin USCI_A0 receive data input in UART mode USCI_A0 slave out, master in SPI mode
P3.6/A6	F4	27	29	25	I/O	General-purpose digital I/O pin ADC10 analog input A6
P3.7/A7	G4	28	30	26	I/O	General-purpose digital I/O pin ADC10 analog input A7
P4.0/TB0	D6	17	19	15	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A input, compare: OUT0 output
P4.1/TB1	D7	18	20	16	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A input, compare: OUT1 output
P4.2/TB2	E6	19	21	17	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A input, compare: OUT2 output
P4.3/TB0/A12	E7	20	22	18	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0B input, compare: OUT0 output ADC10 analog input A12
P4.4/TB1/A13	F7	21	23	19	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1B input, compare: OUT1 output ADC10 analog input A13
P4.5/TB2/A14	F6	22	24	20	I/O	General-purpose digital I/O pin Timer_B, compare: OUT2 output ADC10 analog input A14

(2) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

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Table 4-1. Terminal Functions (continued)

TERMINAL					I/O	DESCRIPTION
NAME	NO.					
	YFF	DA	N	RHA		
P4.6/TBOUTH/A15	G7	23	25	21	I/O	General-purpose digital I/O pin Timer_B, switch all TB0 to TB3 outputs to high impedance ADC10 analog input A15
P4.7/TBCLK	F5	24	26	22	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
$\overline{\text{RST}}$/NMI/SBWTDIO	B3	7	9	5	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	D1	1	1	37	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DV_{CC}	C1, D3, D4, E4, E5	2	2, 3	38, 39		Digital supply voltage
AV_{CC}	C6, C7, D5	16	18	14		Analog supply voltage
DV_{SS}	A3, B1, B2, C3, C4	4	5, 8	1, 4		Digital ground reference
AV_{SS}	B7, C5	15	17	13		Analog ground reference
QFN Pad	NA	NA	NA	Pad	NA	QFN package pad; connection to DV_{SS} recommended.

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5 Specifications

5.1 Absolute Maximum Ratings(1)(2)

	MIN	MAX	UNIT
Voltage applied at V_{CC}	-0.3	4.1	V
Voltage applied to any pin(3)	-0.3	V_{CC} + 0.3	V
Diode current at any device terminal		±2	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.
(3) The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

5.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature (programmed or unprogrammed device)(1)	-55	150	°C

(1) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.3 Recommended Operating Conditions(1)(2)

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	$AV_{CC} = DV_{CC} = V_{CC}$	During program execution	1.8		3.6	V
			During program and erase of flash memory	2.2		3.6	V
V_{SS}	Supply voltage	$AV_{SS} = DV_{SS} = V_{SS}$			0		V
T_A	Operating free-air temperature			-40		85	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(1)(2) (see Figure 5-1)	V_{CC} = 1.8 V, Duty cycle = 50% ±10%		dc		4.15	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ±10%		dc		12	
		V_{CC} ≥ 3.3 V, Duty cycle = 50% ±10%		dc		16	

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.

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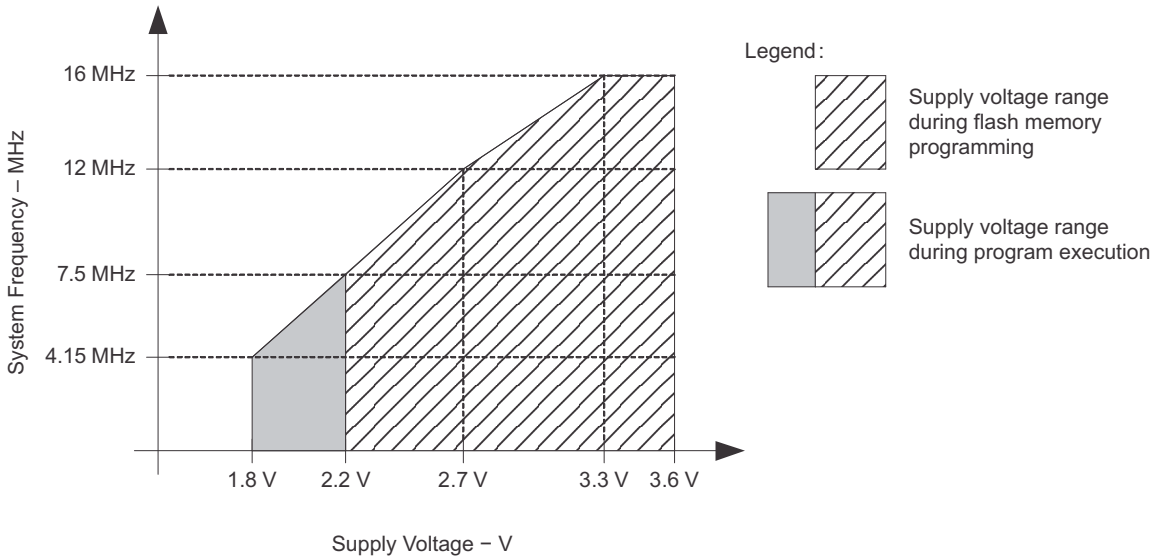

NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 5-1. Operating Area

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5.4 Active Mode Supply Current (Into DV_{CC} + AV_{CC}) Excluding External Current[1][2]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		270		µA
				3 V		390	550	

(1) All inputs are tied to 0 V or V_{CC} . Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

5.5 Typical Characteristics - Active-Mode Supply Current (Into DV_{CC} + AV_{CC})

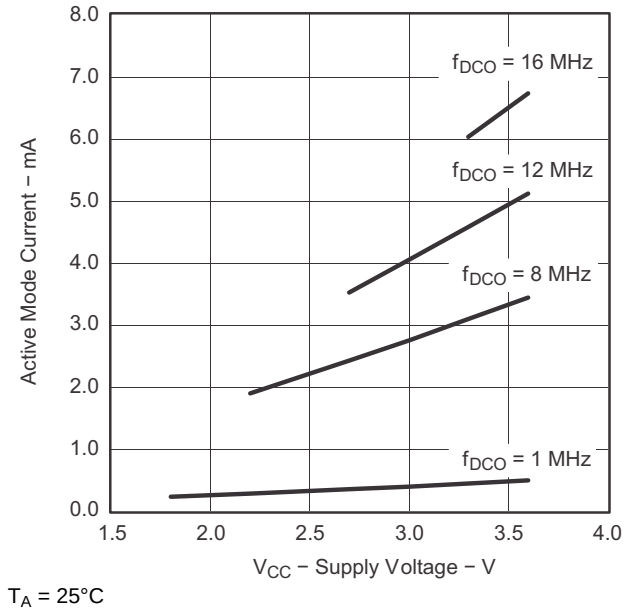

Figure 5-2. Active-mode Current vs Supply Voltage

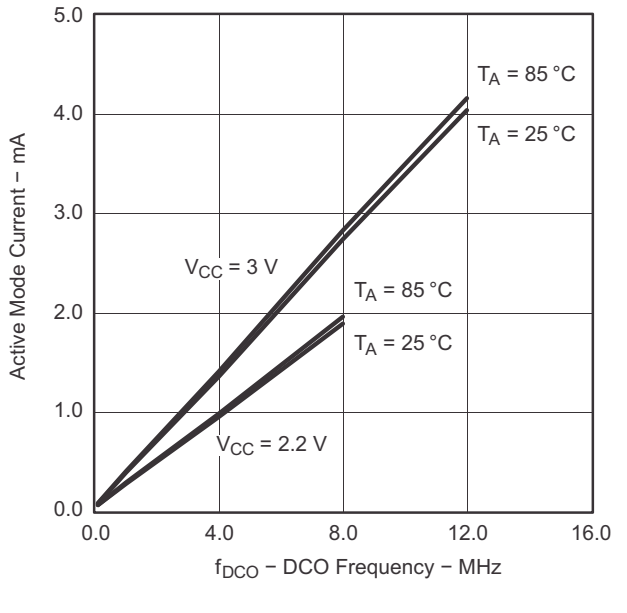

Figure 5-3. Active-Mode Current vs DCO Frequency

5.6 Low-Power-Mode Supply Currents (Into V_{CC}) Excluding External Current[1][2]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current[3]	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	25°C	2.2 V		75	90	µA
I_{LPM2}	Low-power mode 2 (LPM2) current[4]	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		22		µA
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current[4]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		1	2	µA
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3)[4]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.5	1	µA
I_{LPM4}	Low-power mode 4 (LPM4) current[5]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	2.2 V		0.1	0.5	µA
			85°C			1.5	3	

(1) All inputs are tied to 0 V or V_{CC} . Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

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5.7 Schmitt-Trigger Inputs (Ports P1, P2, P3, P4, and $\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} - V_{IT-})		3 V	0.3		1	V
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$	3 V	20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

5.8 Leakage Current, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	(1) (2)	3 V			±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

5.9 Outputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = -6 mA (1)	3 V		V_{CC} - 0.3		V
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 6 mA (1)	3 V		V_{SS} + 0.3		V

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

5.10 Output Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	Px.y, C_L = 20 pF, R_L = 1 kΩ against $V_{CC}/2$ (1) (2)	3 V		12		MHz
f_{Port_CLK}	Clock output frequency	Px.y, C_L = 20 pF (2)	3 V		16		MHz

(1) Alternatively, a resistive divider with two 2-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

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5.11 Typical Characteristics - Outputs

One output loaded at a time.

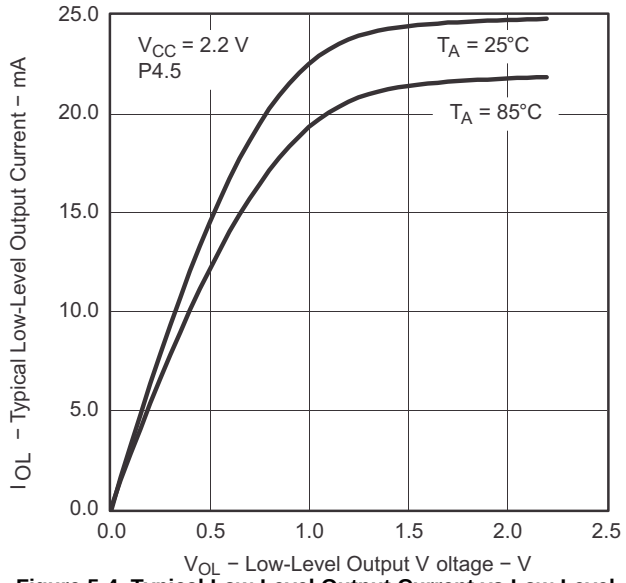

Figure 5-4. Typical Low-Level Output Current vs Low-Level Output Voltage

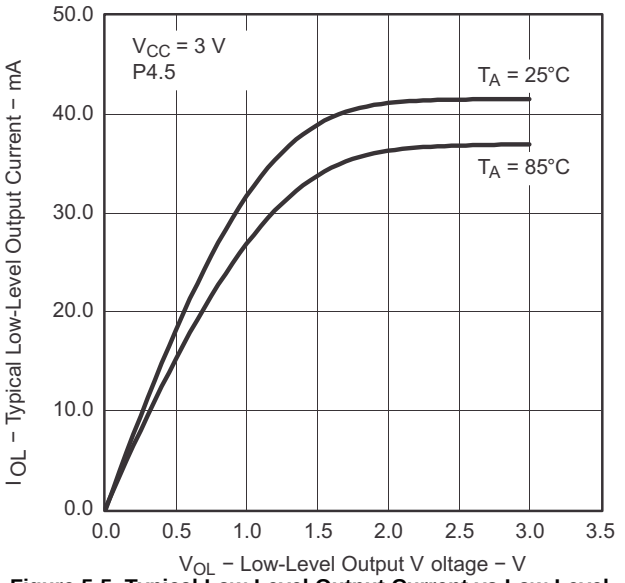

Figure 5-5. Typical Low-Level Output Current vs Low-Level Output Voltage

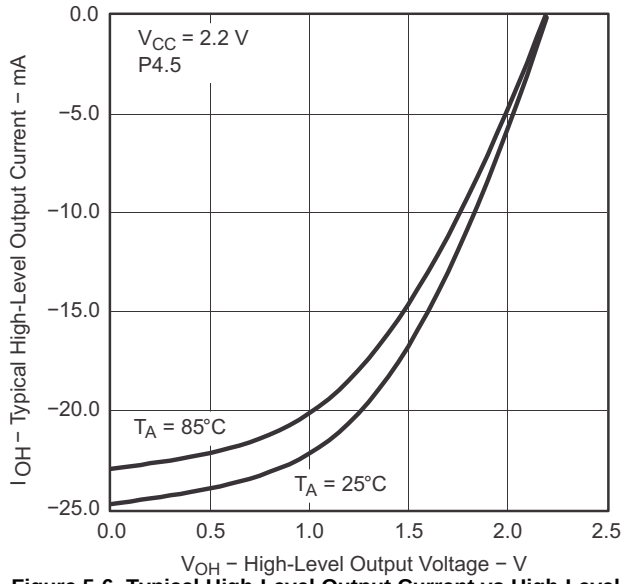

Figure 5-6. Typical High-Level Output Current vs High-Level Output Voltage

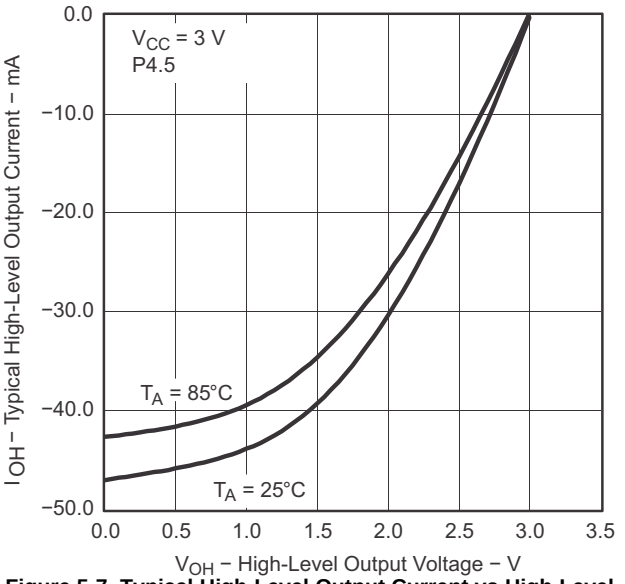

Figure 5-7. Typical High-Level Output Current vs High-Level Output Voltage

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5.12 POR and BOR(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 5-8	dV_{CC} /dt ≤ 3 V/s			0.7 × $V_{(B_IT-)}$		V
$V_{(B_IT-)}$	See Figure 5-8 through Figure 5-10	dV_{CC} /dt ≤ 3 V/s			1.35		V
$V_{hys(B_IT-)}$	See Figure 5-8	dV_{CC} /dt ≤ 3 V/s			140		mV
$t_{d(BOR)}$	See Figure 5-8				2000		µs
$t_{(reset)}$	Pulse duration needed at $\overline{RST}$/NMI pin to accept reset internally		2.2 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B_IT-)}$ + $V_{hys(B_IT-)}$ is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after V_{CC} = $V_{(B_IT-)}$ + $V_{hys(B_IT-)}$. The default DCO settings must not be changed until V_{CC} ≥ $V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

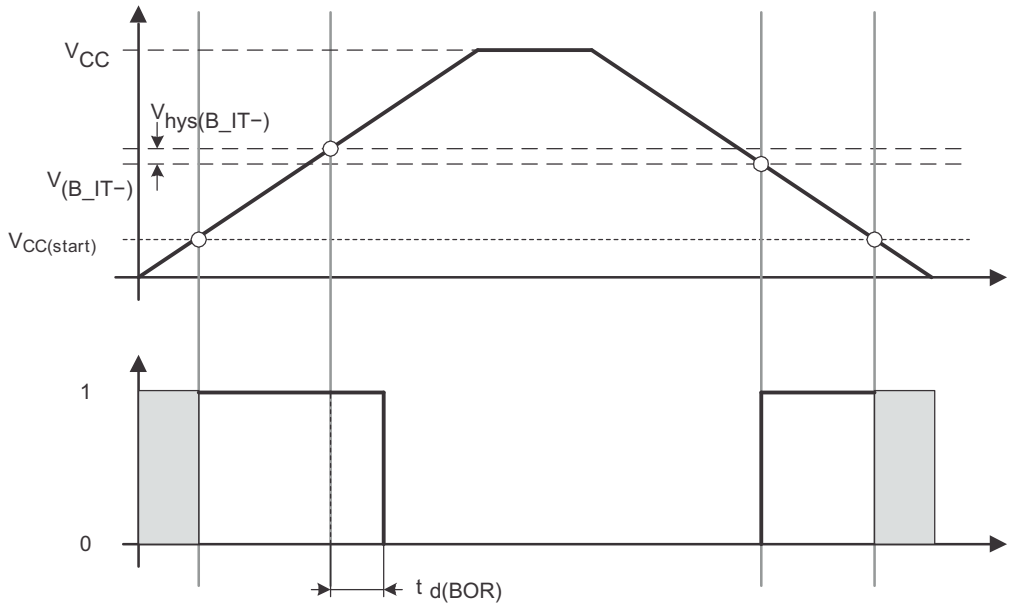

Figure 5-8. POR and BOR vs Supply Voltage

5.13 Typical Characteristics - POR and BOR

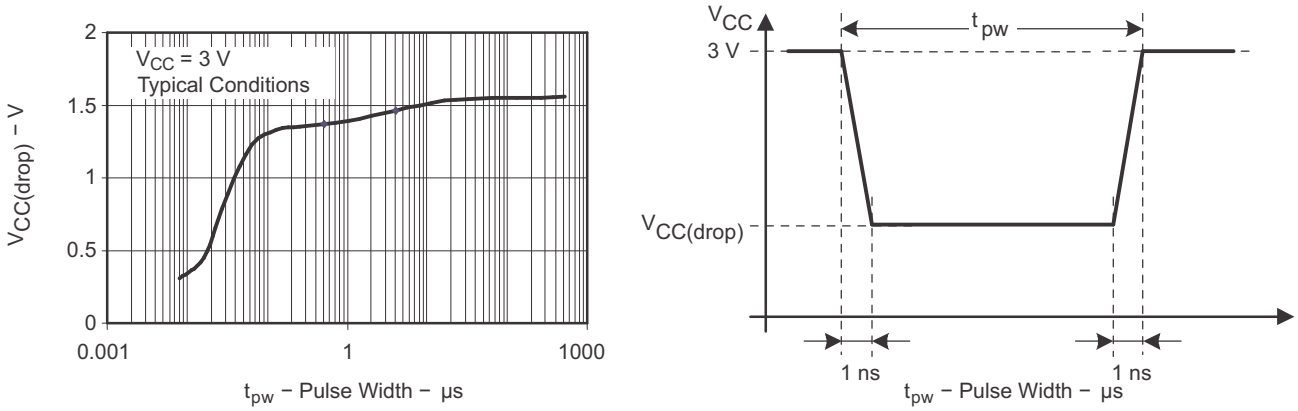

Figure 5-9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR or BOR Signal

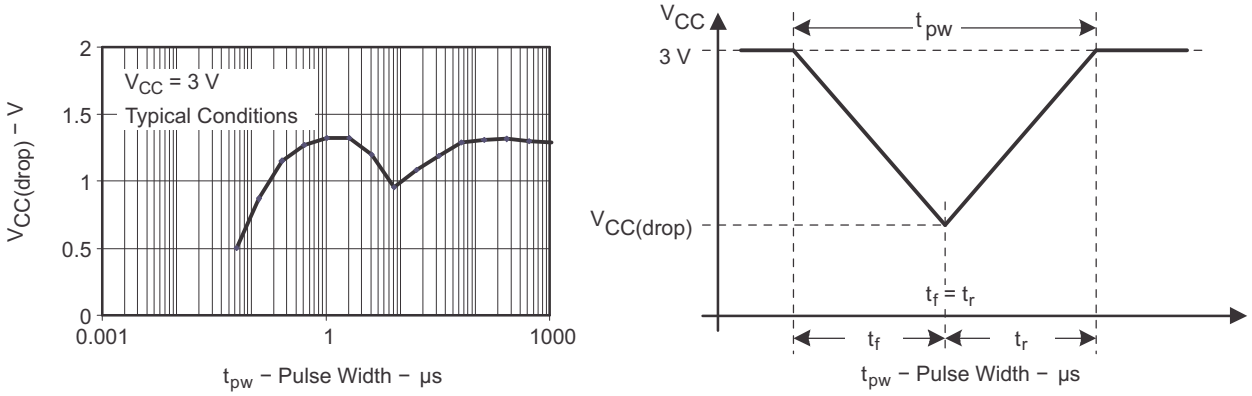

Figure 5-10. $V_{CC(drop)}$ Level With a Triangular Voltage Drop to Generate a POR or BOR Signal

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5.14 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	3 V				MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	3 V				MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	3 V				MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	3 V				MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	3 V				MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	3 V		1.6		MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	3 V		2.3		MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	3 V		3.4		MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	3 V		4.25		MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)} / f_{DCO(RSEL,DCO)}$	3 V		1.35		ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)} / f_{DCO(RSEL,DCO)}$	3 V		1.08		ratio
	Duty cycle	Measured at SMCLK	3 V		50%		

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5.15 Calibrated DCO Frequencies, Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3%	±0.5%	+3%	
1-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	30°C	1.8 V to 3.6 V	-3%	±2%	+3%	
1-MHz tolerance overall	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	1.8 V to 3.6 V	-6%	±3%	+6%	
8-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3%	±0.5%	+3%	
8-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	30°C	2.2 V to 3.6 V	-3%	±2%	+3%	
8-MHz tolerance overall	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	2.2 V to 3.6 V	-6%	±3%	+6%	
12-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3%	±0.5%	+3%	
12-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	30°C	2.7 V to 3.6 V	-3%	±2%	+3%	
12-MHz tolerance overall	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	2.7 V to 3.6 V	-6%	±3%	+6%	
16-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3%	±0.5%	+3%	
16-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	30°C	3.3 V to 3.6 V	-3%	±2%	+3%	
16-MHz tolerance overall	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	3.3 V to 3.6 V	-6%	±3%	+6%	

(1) This is the frequency change from the measured frequency at 30°C over temperature.

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5.16 Wake-Up From Lower-Power Modes (LPM3, LPM4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3 or LPM4 (1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	3 V		1.5		µs
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3 or LPM4 (2)				$1 / f_{MCLK} + t_{Clock,LPM3/4}$		

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

5.17 Typical Characteristics - DCO Clock Wake-Up Time From LPM3 or LPM4

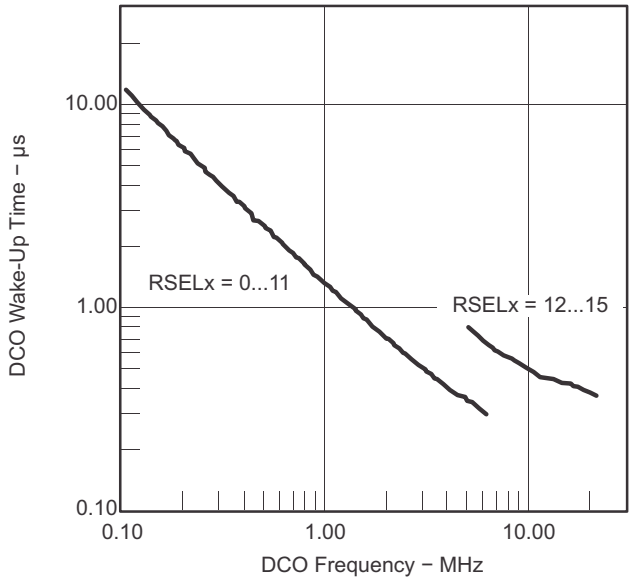

Figure 5-11. Clock Wake-Up Time From LPM3 vs DCO Frequency

5.18 DCO With External Resistor R_{OSC} (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO,ROSC}$	DCO output frequency with R_{OSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	2.2 V		1.8		MHz
			3 V		1.95		
D_T	Temperature drift	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V		±0.1		%/°C
D_V	Drift with V_{CC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V		10		%/V

(1) R_{OSC} = 100 kΩ. Metal film resistor, type 0257, 0.6 W with 1% tolerance and T_K = ±50 ppm/°C.

5.19 Typical Characteristics - DCO With External Resistor R_{OSC}

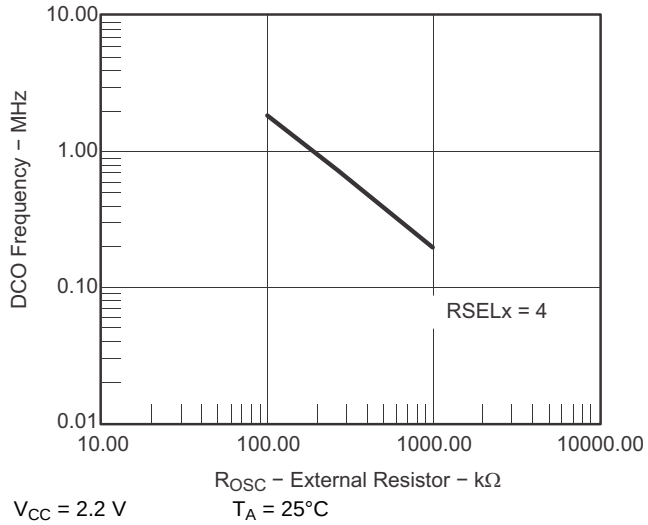

Figure 5-12. DCO Frequency vs R_{OSC}

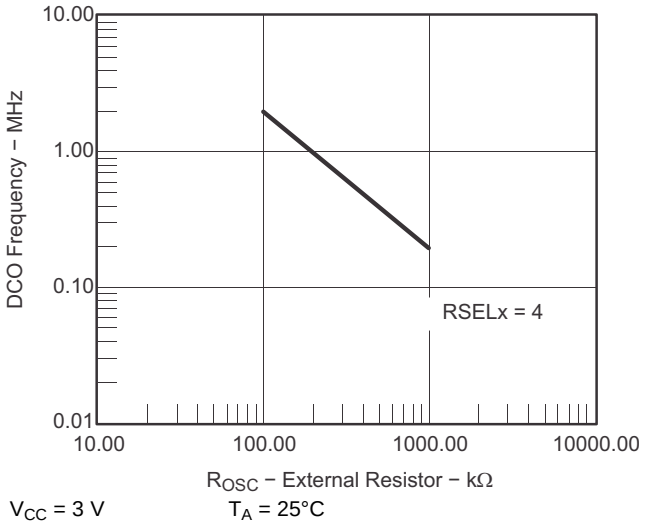

Figure 5-13. DCO Frequency vs R_{OSC}

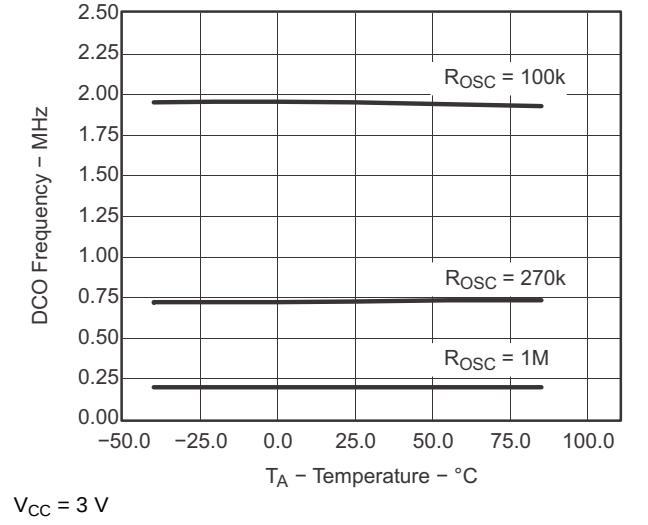

Figure 5-14. DCO Frequency vs Temperature

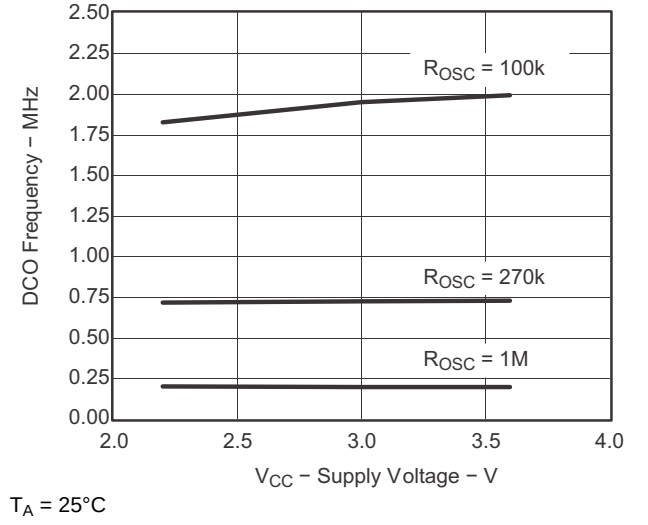

Figure 5-15. DCO Frequency vs Supply Voltage

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5.20 Crystal Oscillator LFXT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(2)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V	30%	50%	70%	
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(3)	XTS = 0, XCAPx = 0, LFXT1Sx = 3(4)	2.2 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the crystal that is used.

(3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(4) Measured with logic-level input frequency but also applies to operation with crystals.

5.21 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	-40°C to 85°C	3 V	4	12	20	kHz
df_{VLO}/dT	VLO frequency temperature drift (1)	-40°C to 85°C	3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift (2)	25°C	1.8 V to 3.6 V		4		%/V

(1) Calculated using the box method:
I version: [MAX(-40...85°C) - MIN(-40...85°C)]/MIN(-40...85°C)/[85°C - (-40°C)]

(2) Calculated using the box method: [MAX(1.8...3.6 V) - MIN(1.8...3.6 V)]/MIN(1.8...3.6 V)/(3.6 V - 1.8 V)

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5.22 Crystal Oscillator LFXT1, High-Frequency Mode(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1	1.8 V to 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2	1.8 V to 3.6 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3	1.8 V to 3.6 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 5-16 and Figure 5-17)	XTS = 1, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 1, LFXT1Sx = 1, $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 1, LFXT1Sx = 2, $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(2)	XTS = 1(3)			1		pF
	Duty cycle, HF mode	XTS = 1, Measured at P2.0/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V	40%	50%	60%	
		XTS = 1, Measured at P2.0/ACLK, $f_{LFXT1,HF}$ = 16 MHz		40%	50%	60%	
$f_{Fault,HF}$	Oscillator fault frequency(4)	XTS = 1, LFXT1Sx = 3(5)	2.2 V	30		300	kHz

(1) To improve EMI on the XT1 oscillator the following guidelines should be observed:
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(4) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals.

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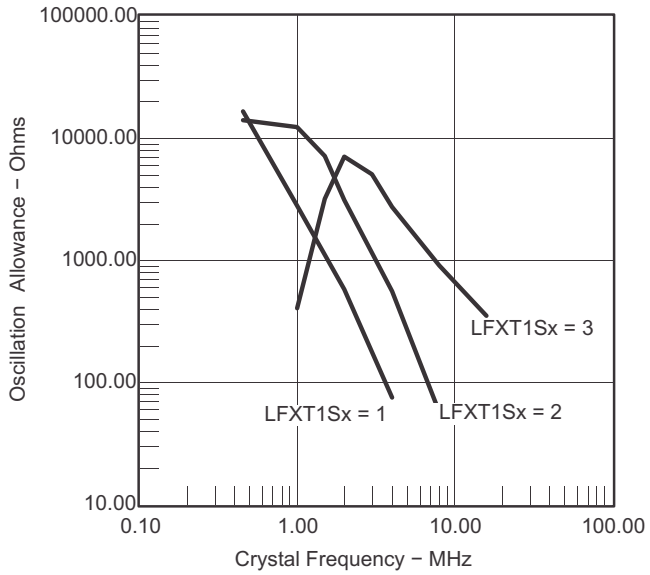
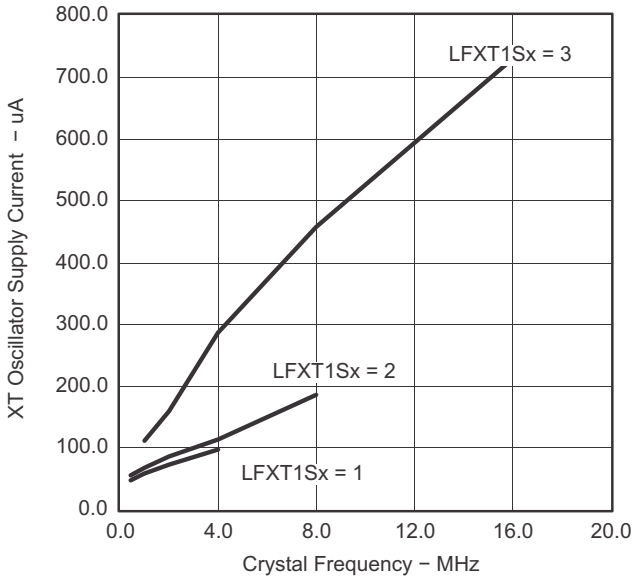
5.23 Typical Characteristics - LFXT1 Oscillator in HF Mode (XTS = 1)



$C_{L,eff}$ = 15 pF T_A = 25°C

Figure 5-16. Oscillation Allowance vs Crystal Frequency



$C_{L,eff}$ = 15 pF T_A = 25°C

Figure 5-17. Oscillator Supply Current vs Crystal Frequency

5.24 Timer_A, Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	SMCLK, Duty cycle = 50% ± 10%			f_{SYSTEM}		MHz
$t_{TA,cap}$	Timer_A capture timing	TAx, TBx	3 V	20			ns

5.25 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$f_{max,BITCLK}$	Maximum BITCLK clock frequency (equals baud rate in MBaud)		3 V	2			MHz
t_{τ}	UART receive deglitch time(1)		3 V	50	100	600	ns

(1) The DCO wake-up time must be considered in LPM3/4 for baud rates above 1 MHz.

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5.26 USCI (SPI Master Mode)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 5-18 and Figure 5-19)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		3 V	75			ns
$t_{HD,MI}$	SOMI input data hold time		3 V	0			ns
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	3 V			20	ns

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

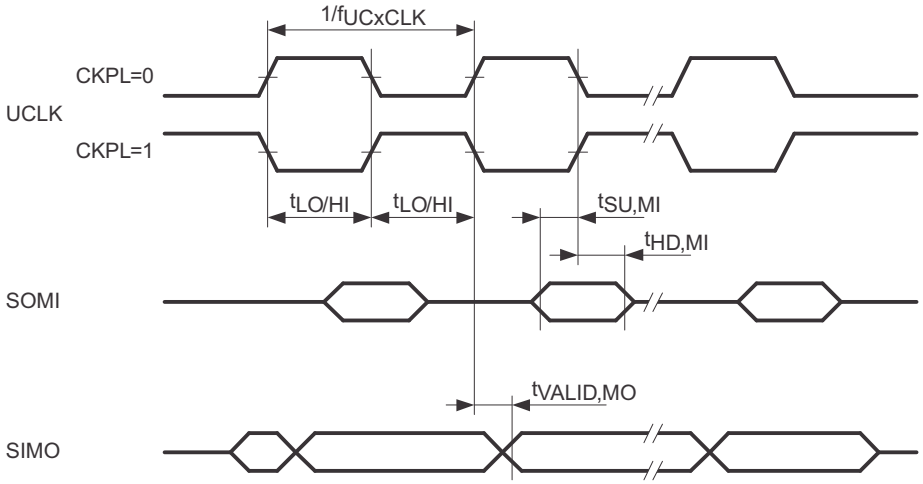

Figure 5-18. SPI Master Mode, CKPH = 0

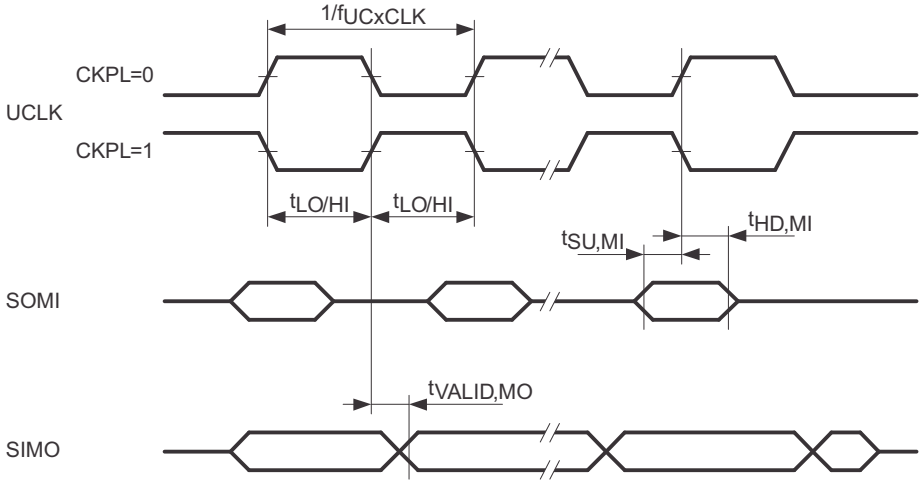

Figure 5-19. SPI Master Mode, CKPH = 1

5.27 USCI (SPI Slave Mode)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 5-20 and Figure 5-21)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock		3 V		50		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE high		3 V	10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out		3 V		50		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance		3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		3 V	15			ns
$t_{HD,SI}$	SIMO input data hold time		3 V	10			ns
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	3 V		50	75	ns

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached slave.

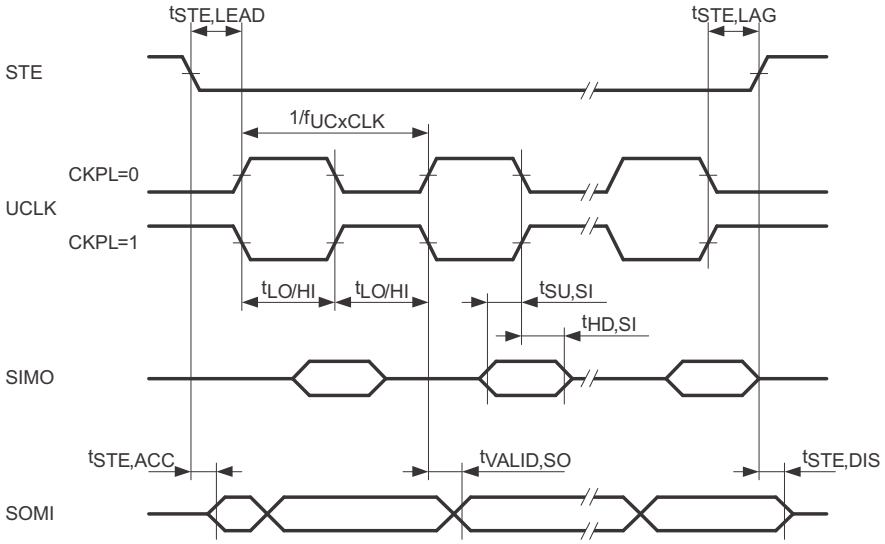

Figure 5-20. SPI Slave Mode, CKPH = 0

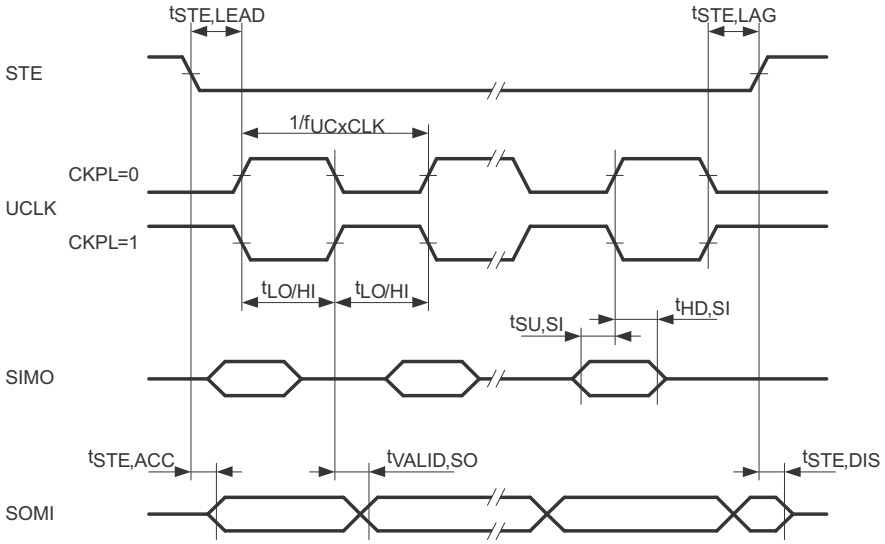

Figure 5-21. SPI Slave Mode, CKPH = 1

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5.28 USCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-22)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	3 V	4			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		3 V	0			ns
$t_{SU,DAT}$	Data setup time		3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		3 V	4			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		3 V	50	100	600	ns

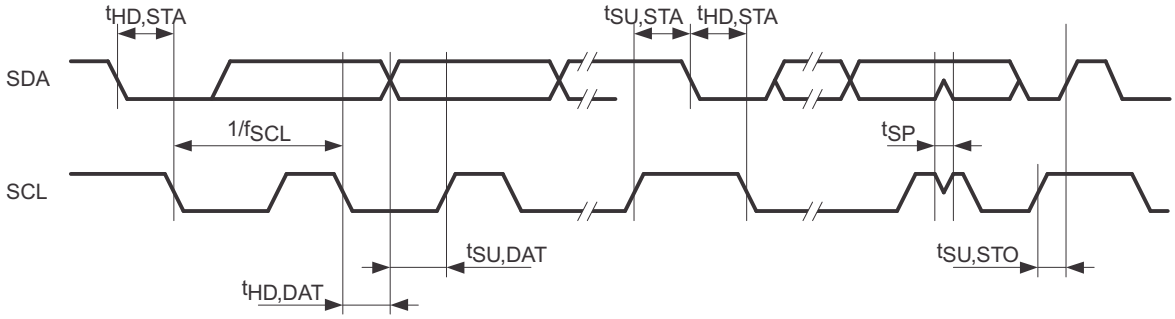

Figure 5-22. I^2C Mode Timing

5.29 10-Bit ADC, Power Supply and Input Range Conditions[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage range	V_{SS} = 0 V			2.2		3.6	V
V_{Ax}	Analog input voltage range[2]	All Ax terminals, Analog inputs selected in ADC10AE register		3 V	0		V_{CC}	V
I_{ADC10}	ADC10 supply current[3]	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	25°C	3 V		0.6		mA
I_{REF+}	Reference supply current, reference buffer disabled[4]	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	25°C	3 V		0.25		mA
		$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0				0.25		
$I_{REFB,0}$	Reference buffer supply current with ADC10SR = 0[4]	$f_{ADC10CLK}$ = 5 MHz ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	25°C	3 V		1.1		mA
$I_{REFB,1}$	Reference buffer supply current with ADC10SR = 1[4]	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1	25°C	3 V		0.5		mA
C_I	Input capacitance	Only one terminal Ax selected at a time	25°C	3 V			27	pF
R_I	Input MUX ON resistance	0 V ≤ V_{Ax} ≤ V_{CC}	25°C	3 V		1000		Ω

(1) The leakage current is defined in the leakage current table with Px.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
(4) The internal reference current is supplied from terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

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5.30 10-Bit ADC, Built-In Voltage Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	$I_{VREF+} \le 1$ mA, REF2_5V = 0		2.2			V
		$I_{VREF+} \le 1$ mA, REF2_5V = 1		2.9			
V_{REF+}	Positive built-in reference voltage	$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 0	3 V	1.41	1.5	1.59	V
		$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 1	3 V	2.35	2.5	2.65	
$I_{LD,VREF+}$	Maximum VREF+ load current		3 V			±1	mA
	VREF+ load regulation	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage $V_{Ax} \approx 0.75$ V, REF2_5V = 0	3 V			±2	LSB
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage $V_{Ax} \approx 1.25$ V, REF2_5V = 1	3 V			±2	
	VREF+ load regulation response time	I_{VREF+} = 100 µA to 900 µA, $V_{Ax} \approx 0.5 \times V_{REF+}$, Error of conversion result ≤1 LSB, ADC10SR = 0	3 V			400	ns
C_{VREF+}	Maximum capacitance at pin VREF+	$I_{VREF+} \le \pm 1$ mA, REFON = 1, REFOUT = 1	3 V			100	pF
TC_{REF+}	Temperature coefficient(1)	I_{VREF+} = constant with 0 mA ≤ I_{VREF+} ≤ 1 mA	3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 to 1	3.6 V			30	µs
$t_{REFBURST}$	Settling time of reference buffer to 99.9% VREF	I_{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1, ADC10SR = 0	3 V			2	µs

(1) Calculated using the box method:
I temperature: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))

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5.31 10-Bit ADC, External Reference(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference input voltage range(2)	$V_{eREF+} > V_{eREF-}$, SREF1 = 1, SREF0 = 0		1.4		V_{CC}	V
		$V_{eREF-} \le V_{eREF+} \le V_{CC}$ - 0.15 V, SREF1 = 1, SREF0 = 1(3)		1.4		3	
V_{eREF-}	Negative external reference input voltage range(4)	$V_{eREF+} > V_{eREF-}$		0		1.2	V
ΔV_{eREF}	Differential external reference input voltage range ΔVeREF = VeREF+ - VeREF-	$V_{eREF+} > V_{eREF-}$(5)		1.4		V_{CC}	V
I_{VeREF+}	Static input current into VeREF+	0 V ≤ V_{eREF+} ≤ V_{CC}, SREF1 = 1, SREF0 = 0	3 V		±1		µA
		0 V ≤ V_{eREF+} ≤ V_{CC} - 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1(3)	3 V		0		
I_{VeREF-}	Static input current into VeREF-	0 V ≤ V_{eREF-} ≤ V_{CC}	3 V		±1		µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, CI, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) Under this condition, the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
(4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

5.32 10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	2.2 V, 3 V	0.45		6.3	MHz
			ADC10SR = 1		0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V, 3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V, 3 V	2.06		3.51	µs
		$f_{ADC10CLK}$ from ACLK, MCLK or SMCLK, ADC10SSELx ≠ 0			13 × ADC10DIVx × 1 / $f_{ADC10CLK}$			
$t_{ADC10ON}$	Turn on settling time of the ADC(1)						100	ns

(1) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

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5.33 10-Bit ADC, Linearity Parameters(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	SREFx = 010	3 V			±1	LSB
E_D	Differential linearity error	SREFx = 010	3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω, SREFx = 010	3 V			±1	LSB
E_G	Gain error	SREFx = 010	3 V		±1.1	±2	LSB
E_T	Total unadjusted error	SREFx = 010	3 V		±2	±6	LSB

(1) Using the integrated reference buffer (SREFx = 010) increases the gain, and offset and total unadjusted error.

5.34 10-Bit ADC, Temperature Sensor and Built-In V_{MID} (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current(1)	REFON = 0, INCHx = 0Ah, T_A = 25°C	3 V		60		µA
TC_{SENSOR}		ADC10ON = 1, INCHx = 0Ah(2)	3 V		3.55		mV/°C
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected(3)	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	3 V	30			µs
I_{VMID}	Current into divider at channel 11	ADC10ON = 1, INCHx = 0Bh	3 V			(3)	µA
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, $V_{MID} \approx 0.5 \times V_{CC}$	3 V		1.5		V
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(4)	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	3 V	1220			ns

(1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1), or (ADC10ON = 1 and INCH = 0Ah and sample signal is high).When REFON = 1, I_{SENSOR} is included in I_{REF+}.When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
(2) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]
(3) No additional current is needed. The V_{MID} is used during sampling.
(4) The on time, $t_{VMID(on)}$, is included in the sampling time, $t_{VMID(sample)}$; no additional on time is needed.

5.35 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC\ (PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V, 3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V, 3.6 V		1	7	mA
t_{CPT}	Cumulative program time (1)		2.2 V, 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V, 3.6 V	20			ms
	Program and erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(2)			30		t_{FTG}
$t_{Block,\ 0}$	Block program time for first byte or word	(2)			25		t_{FTG}
$t_{Block,\ 1-63}$	Block program time for each additional byte or word	(2)			18		t_{FTG}
$t_{Block,\ End}$	Block program end-sequence wait time	(2)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	(2)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	(2)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word write, individual byte write, and block write modes.
(2) These values are hardwired into the state machine of the flash controller ($t_{FTG} = 1/f_{FTG}$).

5.36 RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

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5.37 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V	0.025		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge(1))	2.2 V			1	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time	2.2 V	15		100	µs
f_{TCK}	TCK input frequency(2)	2.2 V	0		5	MHz
$R_{Internal}$	Internal pulldown resistance on TEST	2.2 V	25	60	90	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

5.38 JTAG Fuse(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) After the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, or emulation feature is possible, and JTAG is switched to bypass mode.

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6 Detailed Description

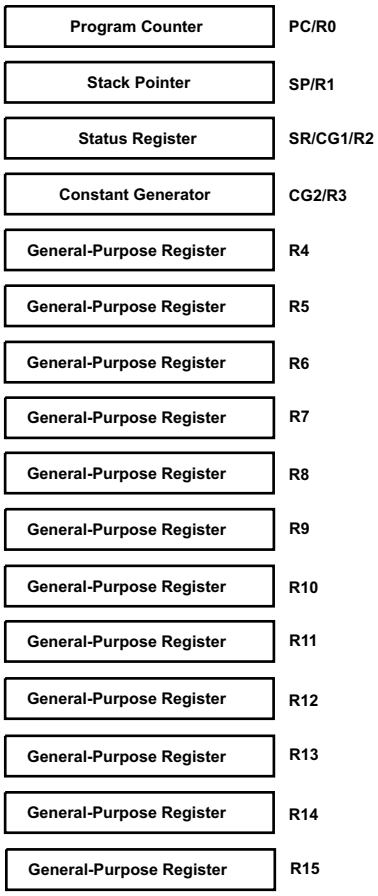
6.1 CPU

The MSP430™ CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.



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6.2 Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 6-1 shows examples of the three types of instruction formats; Table 6-2 shows the address modes.

Table 6-1. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional/conditional	JNE	Jump-on-equal bit = 0

Table 6-2. Address Mode Descriptions

ADDRESS MODE	S(1)	D(2)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source
(2) D = destination

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6.3 Operating Modes

The MSP430 microcontrollers have one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active.
  - MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled.
  - ACLK and SMCLK remain active.
  - MCLK is disabled.
  - DCO dc-generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - ACLK remains active.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator remains enabled.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - ACLK remains active.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK, MCLK, and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - Crystal oscillator is stopped.

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6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, if flash is not programmed), the CPU goes into LPM4 immediately after power up.

Table 6-3. Interrupt Vector Addresses

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	30
Timer_B3	TBCCR0 CCIFG(4)	maskable	0FFFAh	29
Timer_B3	TBCCR1 and TBCCR2 CCIFGs, TBIFG(2)(4)	maskable	0FFF8h	28
			0FFF6h	27
Watchdog Timer	WDTIFG	maskable	0FFF4h	26
Timer_A3	TACCR0 CCIFG(3)	maskable	0FFF2h	25
Timer_A3	TACCR1 CCIFG TACCR2 CCIFG TAIFG(2)(4)	maskable	0FFF0h	24
USCI_A0 or USCI_B0 Receive	UCA0RXIFG, UCB0RXIFG(2)	maskable	0FFEEh	23
USCI_A0 or USCI_B0 Transmit	UCA0TXIFG, UCB0TXIFG(2)	maskable	0FFECh	22
ADC10	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
(5)			0FFDEh	15
(6)			0FFDCh to 0FFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address range.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.
(4) Interrupt flags are located in the module.
(5) This location is used as bootstrap loader security key (BSLSKEY).
A 0AA55h at this location disables the BSL completely.
A zero (0h) disables the erasure of the flash if an invalid password is supplied.
(6) The interrupt vectors at addresses 0FFDCh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

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6.5 Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend

rw	Bit can be read and written.
rw-0, 1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), (1)	Bit can be read and written. It is Reset or Set by POR.
	SFR bit is not present in device.

Table 6-4. Interrupt Enable 1

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE	Oscillator fault interrupt enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Table 6-5. Interrupt Enable 2

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE	USCI_A0 receive-interrupt enable
UCA0TXIE	USCI_A0 transmit-interrupt enable
UCB0RXIE	USCI_B0 receive-interrupt enable
UCB0TXIE	USCI_B0 transmit-interrupt enable

Table 6-6. Interrupt Flag Register 1

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG	Flag set on oscillator fault
RSTIFG	External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power up.
PORIFG	Power-on reset interrupt flag. Set on V_{CC} power up.
NMIIFG	Set via $\overline{RST}$/NMI pin

Table 6-7. Interrupt Flag Register 2

Address	7	6	5	4	3	2	1	0
03h					UCB0TXIFG	UCB0RXIFG	UCA0TXIFG	UCA0RXIFG
					rw-1	rw-0	rw-1	rw-0

UCA0RXIFG	USCI_A0 receive interrupt flag
UCA0TXIFG	USCI_A0 transmit interrupt flag
UCB0RXIFG	USCI_B0 receive interrupt flag
UCB0TXIFG	USCI_B0 transmit interrupt flag

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6.6 Memory Organization

Table 6-8. Memory Organization

		MSP430G2444	MSP430G2544	MSP430G2744
Memory Main: interrupt vector Main: code memory	Size Flash Flash	8KB Flash 0FFFFh-0FFC0h 0FFFFh-0E000h	16KB Flash 0FFFFh-0FFC0h 0FFFFh-0C000h	32KB Flash 0FFFFh-0FFC0h 0FFFFh-08000h
Information memory	Size Flash	256 Byte 010FFh-01000h	256 Byte 010FFh-01000h	256 Byte 010FFh-01000h
Boot memory	Size ROM	1KB 0FFFh-0C00h	1KB 0FFFh-0C00h	1KB 0FFFh-0C00h
RAM	Size	512 Byte 03FFh-0200h	512 Byte 03FFh-0200h	1KB 05FFh-0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh-0100h 0FFh-010h 0Fh-00h	01FFh-0100h 0FFh-010h 0Fh-00h	01FFh-0100h 0FFh-010h 0Fh-00h

6.7 Bootstrap Loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 6-9. BSL Function Pins

BSL FUNCTION	DA PACKAGE PINS	RHA PACKAGE PINS	YFF PACKAGE PINS
Data transmit	32 - P1.1	30 - P1.1	G3 - P1.1
Data receive	10 - P2.2	8 - P2.2	A5 - P2.2

6.8 Flash Memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming and erasing. It can be unlocked, but care should be taken not to erase this segment if the device-specific calibration data is required.

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6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

6.10 Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, or the internal very-low-power LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

Table 6-10. DCO Calibration Data (Provided From Factory in Flash Information Memory Segment A)

DCO FREQUENCY	CALIBRATION REGISTER	SIZE	ADDRESS
1 MHz	CALBC1_1MHZ	byte	010FFh
	CALDCO_1MHZ	byte	010FEh
8 MHz	CALBC1_8MHZ	byte	010FDh
	CALDCO_8MHZ	byte	010FCh
12 MHz	CALBC1_12MHZ	byte	010FBh
	CALDCO_12MHZ	byte	010FAh
16 MHz	CALBC1_16MHZ	byte	010F9h
	CALDCO_16MHZ	byte	010F8h

6.11 Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

6.12 Digital I/O

There are four 8-bit I/O ports implemented—ports P1, P2, P3, and P4:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all eight bits of port P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup or pulldown resistor.

6.13 Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

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6.14 Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-11. Timer_A3 Signal Connections

INPUT PIN NUMBER				DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER			
DA	N	RHA	YFF					DA	N	RHA	YFF
31 - P1.0	33 - P1.0	29 - P1.0	F2 - P1.0	TACLK	TACLK	Timer	NA				
				ACLK	ACLK						
				SMCLK	SMCLK						
9 - P2.1	11 - P2.1	7 - P2.1	B4 - P2.1	TAINCLK	INCLK						
32 - P1.1	34 - P1.1	30 - P1.1	G2 - P1.1	TA0	CCI0A	CCR0	TA0	32 - P1.1	34 - P1.1	30 - P1.1	G2 - P1.1
10 - P2.2	12 - P2.2	8 - P2.2	A5 - P2.2	TA0	CCI0B			10 - P2.2	12 - P2.2	8 - P2.2	A5 - P2.2
				V_{SS}	GND			36 - P1.5	38 - P1.5	34 - P1.5	E1 - P1.5
				V_{CC}	V_{CC}						
33 - P1.2	35 - P1.2	31 - P1.2	E2 - P1.2	TA1	CCI1A	CCR1	TA1	33 - P1.2	35 - P1.2	31 - P1.2	E2 - P1.2
29 - P2.3	31 - P2.3	27 - P2.3	F3 - P2.3	TA1	CCI1B			29 - P2.3	31 - P2.3	27 - P2.3	F3 - P2.3
				V_{SS}	GND			37 - P1.6	39 - P1.6	35 - P1.6	E3 - P1.6
				V_{CC}	V_{CC}						
34 - P1.3	36 - P1.3	32 - P1.3	G1 - P1.3	TA2	CCI2A	CCR2	TA2	34 - P1.3	36 - P1.3	32 - P1.3	G1 - P1.3
				ACLK (internal)	CCI2B			30 - P2.4	32 - P2.4	28 - P2.4	G3 - P2.4
				V_{SS}	GND			38 - P1.7	40 - P1.7	36 - P1.7	D2 - P1.7
				V_{CC}	V_{CC}						

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6.15 Timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. Timer_B3 Signal Connections

INPUT PIN NUMBER				DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER			
DA	N	RHA	YFF					DA	N	RHA	YFF
24 - P4.7	26 - P4.7	22 - P4.7	F5 - P4.7	TBCLK	TBCLK	Timer	NA				
				ACLK	ACLK						
				SMCLK	SMCLK						
24 - P4.7	26 - P4.7	22 - P4.7	F5 - P4.7	TBCLK	INCLK						
17 - P4.0	19 - P4.0	15 - P4.0	D6 - P4.0	TB0	CCI0A	CCR0	TB0	17 - P4.0	19 - P4.0	15 - P4.0	D6 - P4.0
20 - P4.3	22 - P4.3	18 - P4.3	E7 - P4.3	TB0	CCI0B			20 - P4.3	22 - P4.3	18 - P4.3	E7 - P4.3
				V_{SS}	GND						
				V_{CC}	V_{CC}						
18 - P4.1	21 - P4.1	16 - P4.1	D7 - P4.1	TB1	CCI1A	CCR1	TB1	18 - P4.1	20 - P4.1	16 - P4.1	D7 - P4.1
21 - P4.4	23 - P4.4	19 - P4.4	F7 - P4.4	TB1	CCI1B			21 - P4.4	23 - P4.4	19 - P4.4	F7 - P4.4
				V_{SS}	GND						
				V_{CC}	V_{CC}						
19 - P4.2	21 - P4.2	17 - P4.2	E6 - P4.2	TB2	CCI2A	CCR2	TB2	19 - P4.2	21 - P4.2	17 - P4.2	E6 - P4.2
				ACLK (internal)	CCI2B			22 - P4.5	24 - P4.5	20 - P4.5	F6 - P4.5
				V_{SS}	GND						
				V_{CC}	V_{CC}						

6.16 Universal Serial Communications Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I2C.

6.17 ADC10

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling allowing ADC samples to be converted and stored without any CPU intervention.

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6.18 Peripheral File Map

Table 6-13 lists the peripheral registers that have word access, and Table 6-14 lists the peripheral registers that have byte access.

Table 6-13. Peripherals With Word Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS OFFSET
ADC10	ADC data transfer start address	ADC10SA	1BCh
	ADC memory	ADC10MEM	1B4h
	ADC control register 1	ADC10CTL1	1B2h
	ADC control register 0	ADC10CTL0	1B0h
	ADC analog enable 0	ADC10AE0	04Ah
	ADC analog enable 1	ADC10AE1	04Bh
	ADC data transfer control register 1	ADC10DTC1	049h
	ADC data transfer control register 0	ADC10DTC0	048h
Timer_B	Capture/compare register	TBCCR2	0196h
	Capture/compare register	TBCCR1	0194h
	Capture/compare register	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control	TBCCTL2	0186h
	Capture/compare control	TBCCTL1	0184h
	Capture/compare control	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A	Capture/compare register	TACCR2	0176h
	Capture/compare register	TACCR1	0174h
	Capture/compare register	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control	TACCTL2	0166h
	Capture/compare control	TACCTL1	0164h
	Capture/compare control	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

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Table 6-14. Peripherals With Byte Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS OFFSET
USCI_B0	USCI_B0 transmit buffer	UCB0TXBUF	06Fh
	USCI_B0 receive buffer	UCB0RXBUF	06Eh
	USCI_B0 status	UCB0STAT	06Dh
	USCI_B0 bit rate control 1	UCB0BR1	06Bh
	USCI_B0 bit rate control 0	UCB0BR0	06Ah
	USCI_B0 control 1	UCB0CTL1	069h
	USCI_B0 control 0	UCB0CTL0	068h
	USCI_B0 I2C slave address	UCB0SA	011Ah
	USCI_B0 I2C own address	UCB0OA	0118h
USCI_A0	USCI_A0 transmit buffer	UCA0TXBUF	067h
	USCI_A0 receive buffer	UCA0RXBUF	066h
	USCI_A0 status	UCA0STAT	065h
	USCI_A0 modulation control	UCA0MCTL	064h
	USCI_A0 baud rate control 1	UCA0BR1	063h
	USCI_A0 baud rate control 0	UCA0BR0	062h
	USCI_A0 control 1	UCA0CTL1	061h
	USCI_A0 control 0	UCA0CTL0	060h
	USCI_A0 IrDA receive control	UCA0IRRCTL	05Fh
	USCI_A0 IrDA transmit control	UCA0IRTCTL	05Eh
	USCI_A0 auto baud rate control	UCA0ABCTL	05Dh
Basic Clock System+	Basic clock system control 3	BCSCTL3	053h
	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P4	Port P4 resistor enable	P4REN	011h
	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 resistor enable	P3REN	010h
	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 resistor enable	P2REN	02Fh
	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

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Table 6-14. Peripherals With Byte Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS OFFSET
Port P1	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

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6.19 Port Schematics

6.19.1 Port P1 Pin Schematic: P1.0 to P1.3, Input/Output With Schmitt Trigger

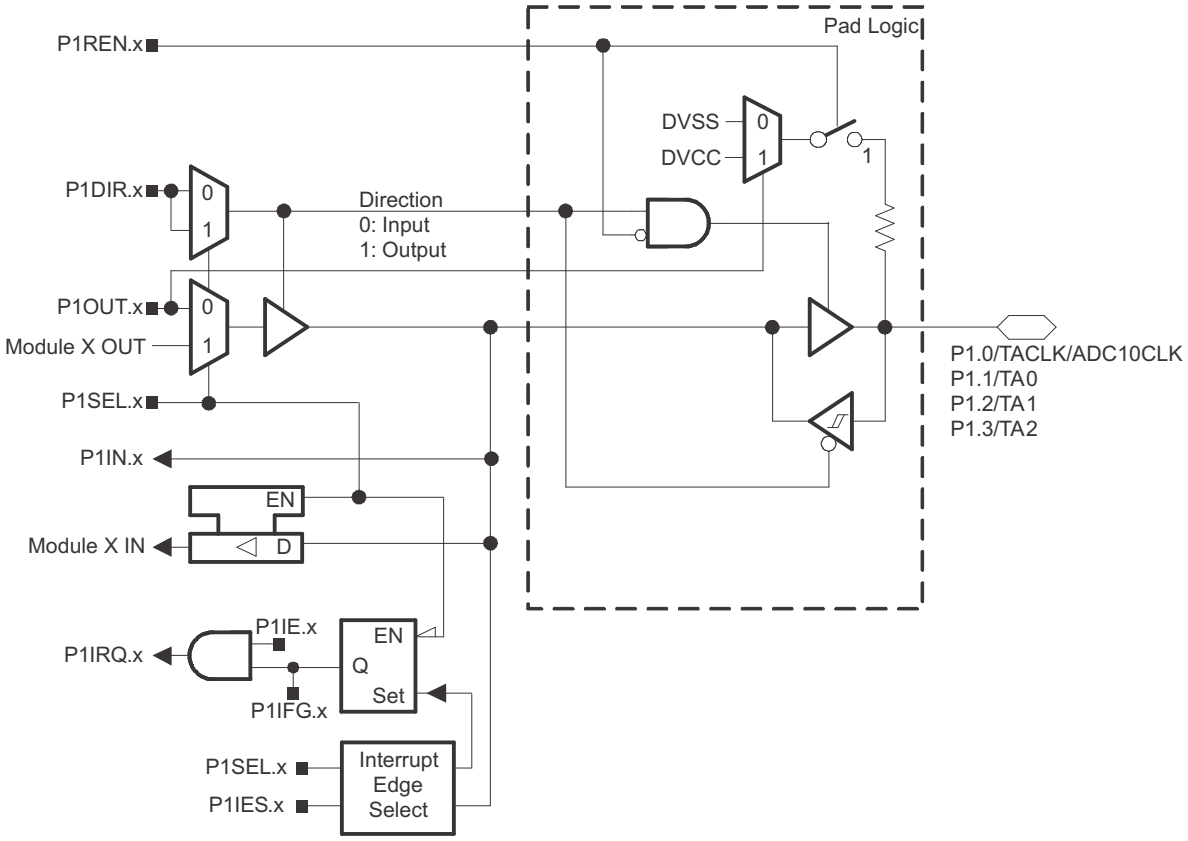

Table 6-15. Port P1 (P1.0 to P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK/ADC10CLK	0	P1.0(1)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		ADC10CLK	1	1
P1.1/TA0	1	P1.1(1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2(1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TA2	3	P1.3(1) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1

(1) Default after reset (PUC, POR)

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6.19.2 Port P1 Pin Schematic: P1.4 to P1.6, Input/Output With Schmitt Trigger and In-System Access Features

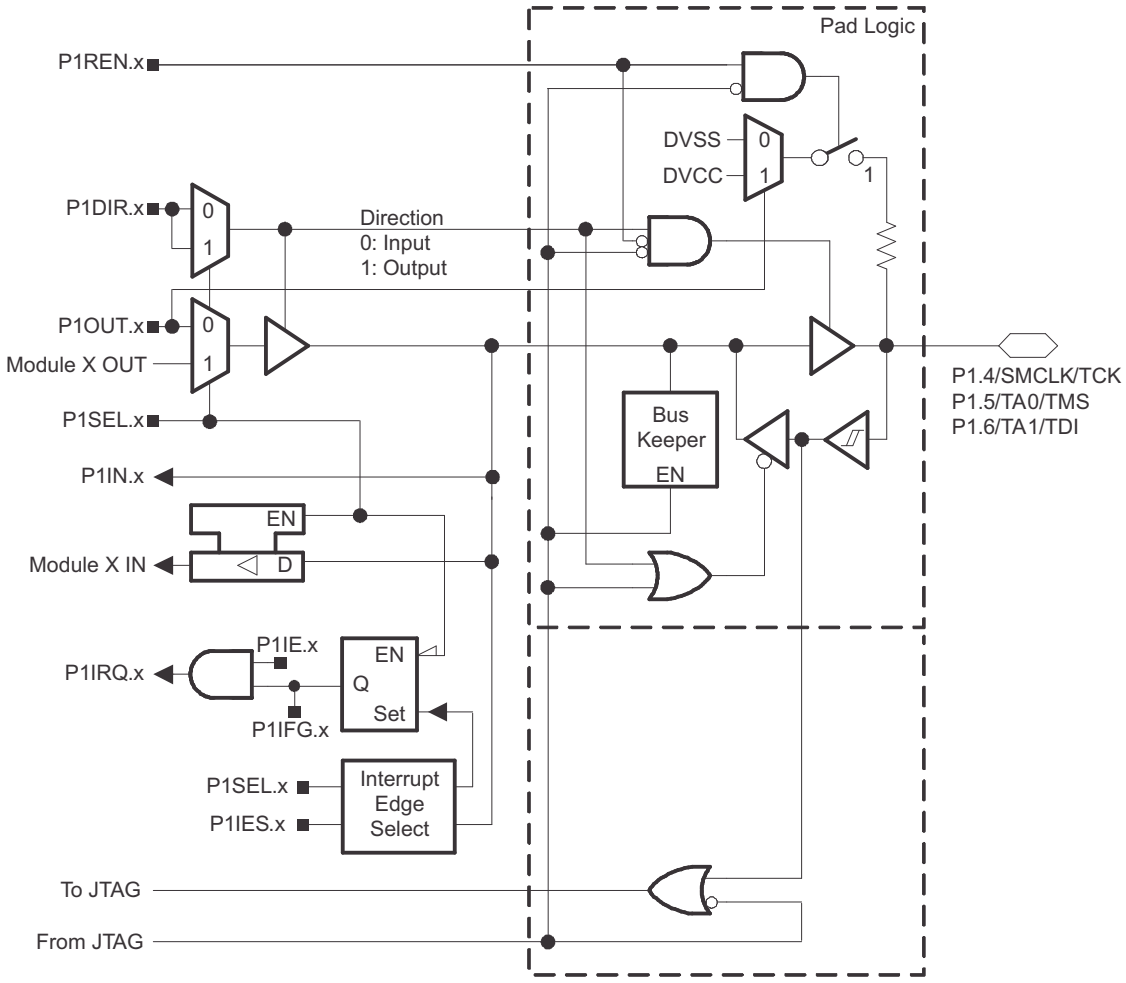

Table 6-16. Port P1 (P1.4 to P1.6) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.4/SMCLK/TCK	4	P1.4(2) (I/O)	I: 0; O: 1	0	0
		SMCLK	1	1	0
		TCK	X	X	1
P1.5/TA0/TMS	5	P1.5(2) (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA0	1	1	0
		TMS	X	X	1
P1.6/TA1/TDI/TCLK	6	P1.6(2) (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA1	1	1	0
		TDI/TCLK(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) Function controlled by JTAG

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6.19.3 Port P1 Pin Schematic: P1.7, Input/Output With Schmitt Trigger and In-System Access Features

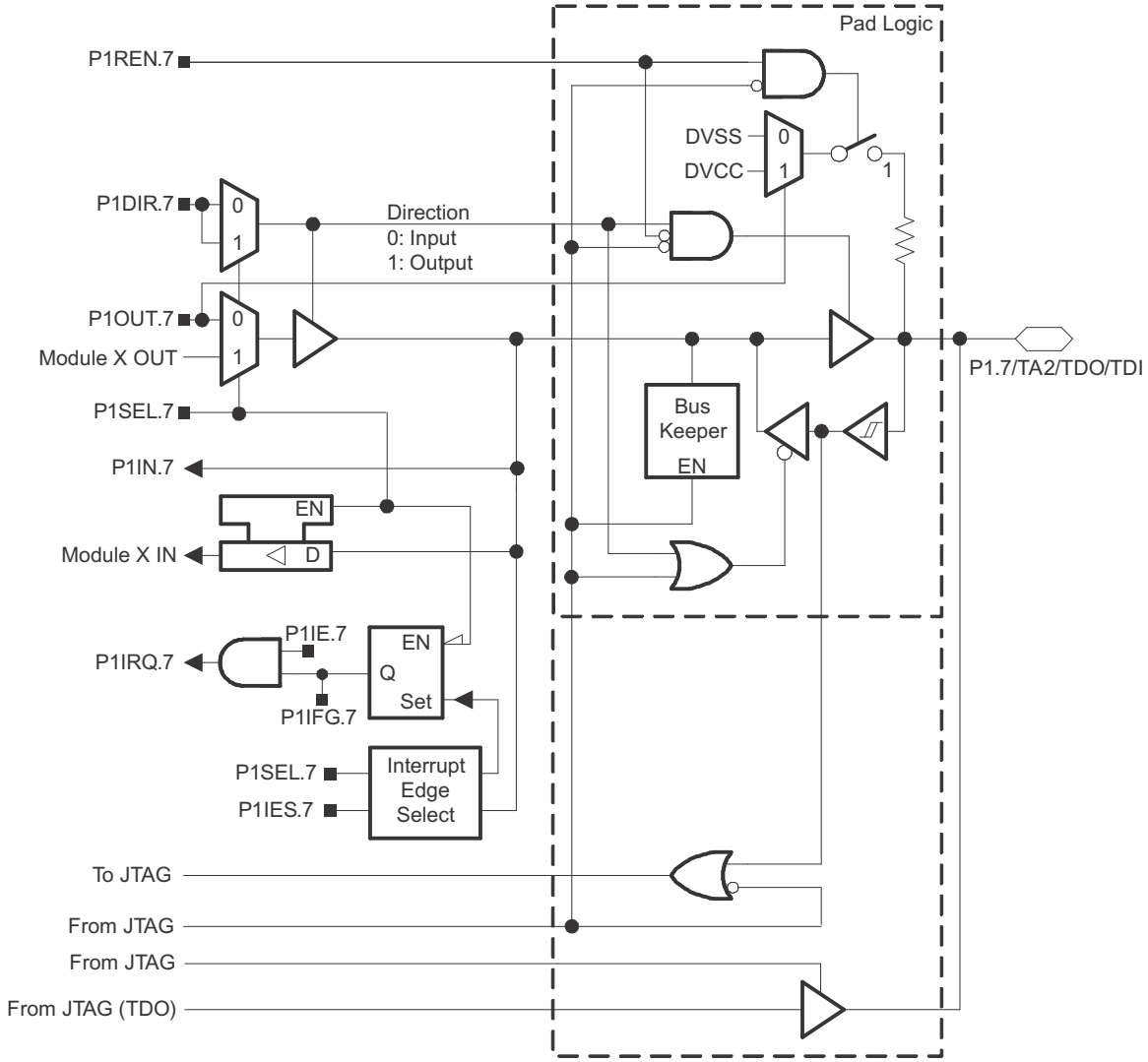

Table 6-17. Port P1 (P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.7/TA2/TDO/TDI	7	P1.7(2) (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA2	1	1	0
		TDO/TDI(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) Function controlled by JTAG

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6.19.4 Port P2 Pin Schematic: P2.0, P2.2, Input/Output With Schmitt Trigger

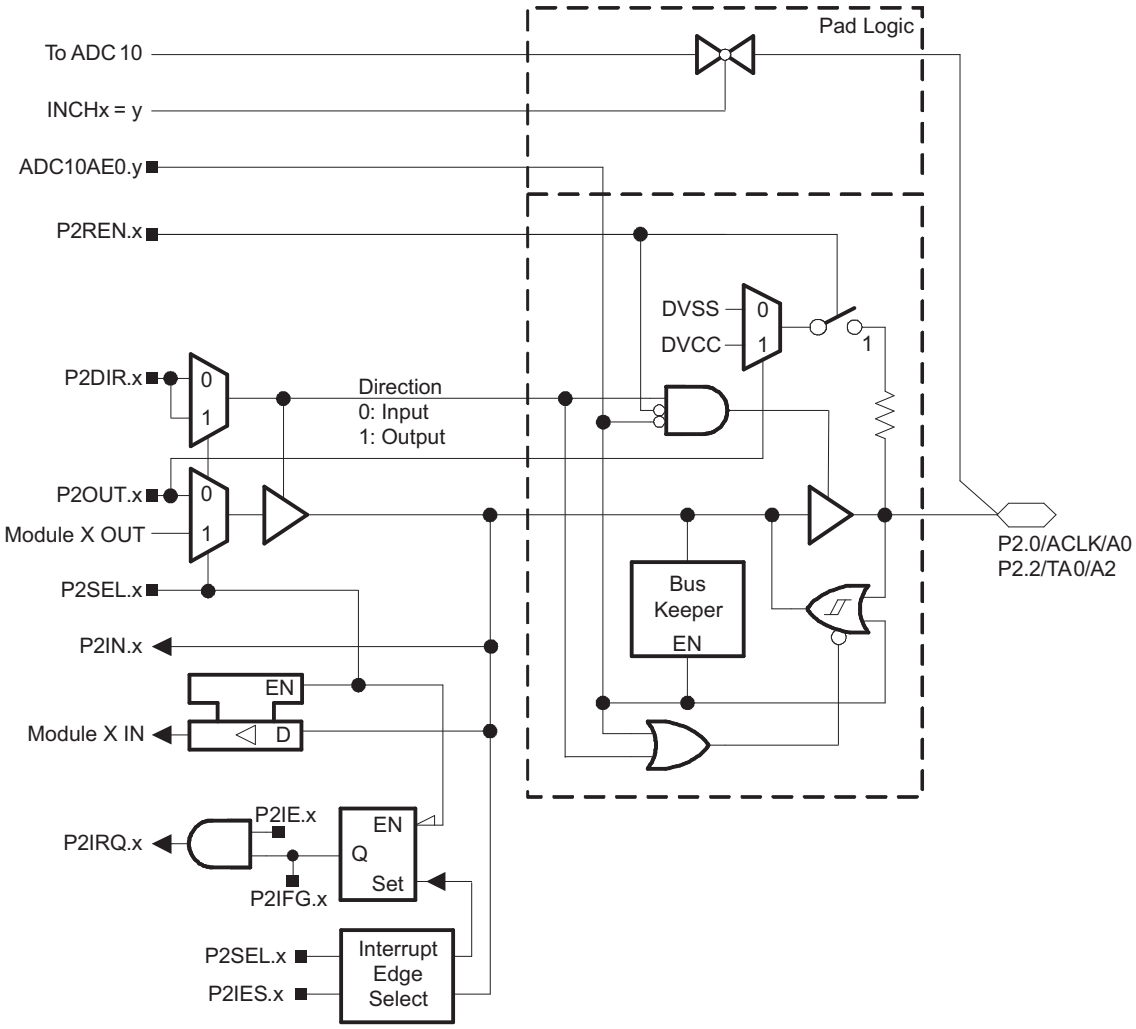

Table 6-18. Port P2 (P2.0, P2.2) Pin Functions

Pin Name (P2.x)	x	y	FUNCTION	CONTROL BITS OR SIGNALS(1)		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.0/ACLK/A0	0	0	P2.0(2) (I/O)	I: 0; O: 1	0	0
			ACLK	1	1	0
			A0(3)	X	X	1
P2.2/TA0/A2	2	2	P2.2(2) (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI0B	0	1	0
			Timer_A3.TA0	1	1	0
			A2(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) Setting the ADC10AE0.y bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.19.5 Port P2 Pin Schematic: P2.1, Input/Output With Schmitt Trigger

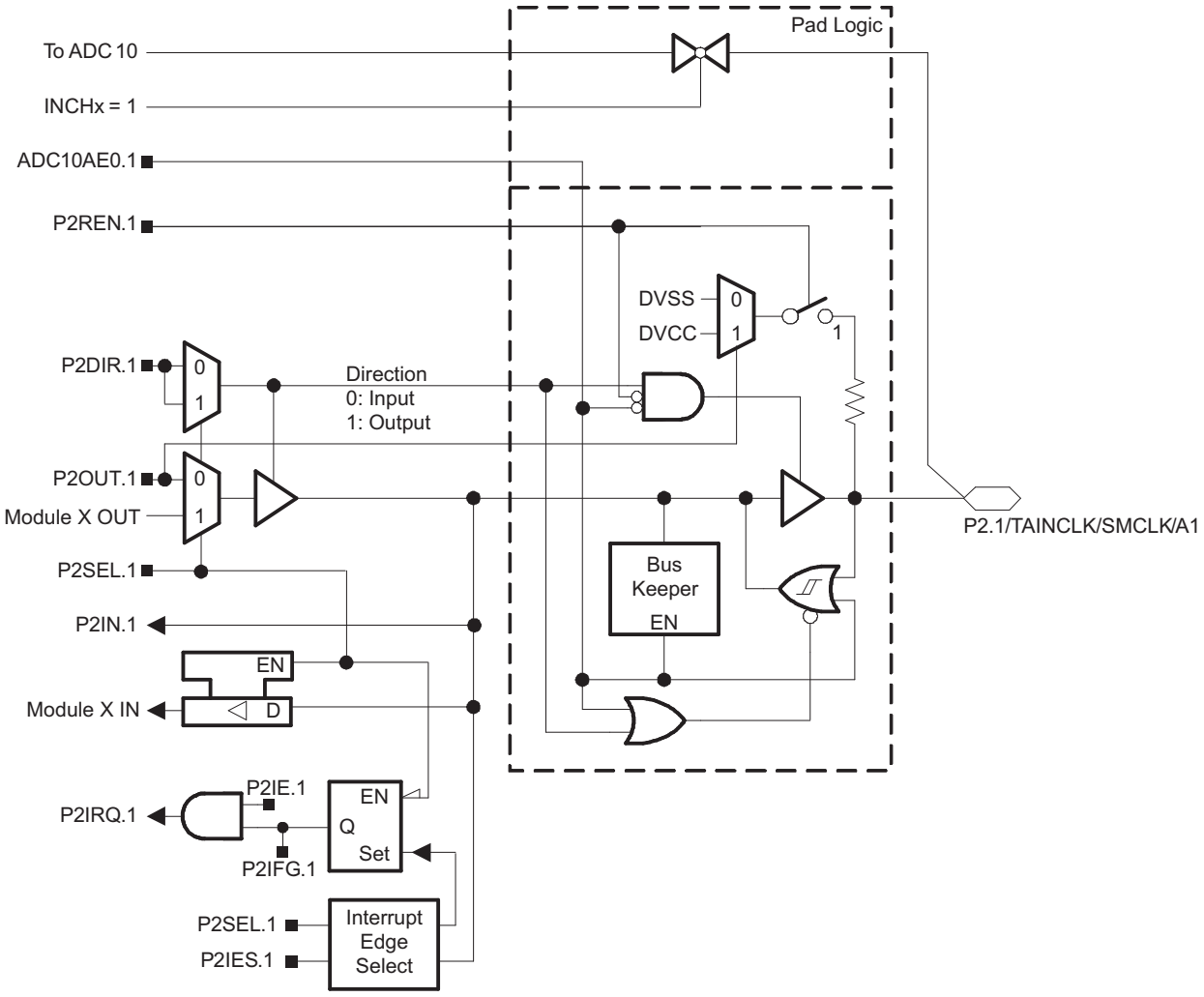

Table 6-19. Port P2 (P2.1) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS OR SIGNALS(1)		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.1/TAINCLK/ SMCLK/A1	1	1	P2.1(2) (I/O)	I: 0; O: 1	0	0
			Timer_A3.INCLK	0	1	0
			SMCLK	1	1	0
			A1(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) Setting the ADC10AE0.y bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.19.6 Port P2 Pin Schematic: P2.3, Input/Output With Schmitt Trigger

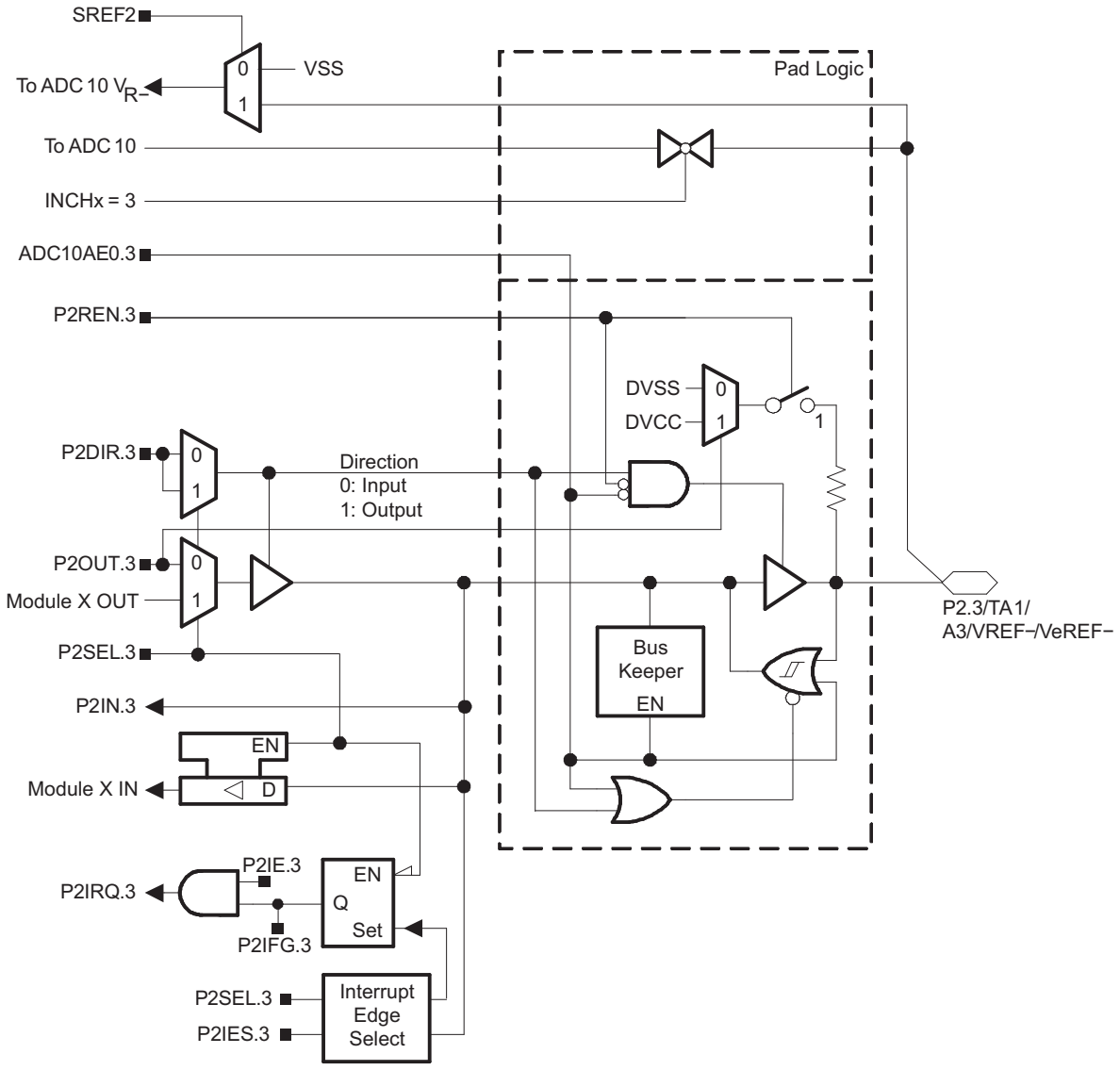

Table 6-20. Port P2 (P2.3) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS OR SIGNALS(1)		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.3/TA1/A3/ VREF-/VeREF-	3	3	P2.3(2) (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI1B	0	1	0
			Timer_A3.TA1	1	1	0
			$A3/V_{REF-}/V_{eREF-}$ (3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) Setting the ADC10AE0.y bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.19.7 Port P2 Pin Schematic: P2.4, Input/Output With Schmitt Trigger

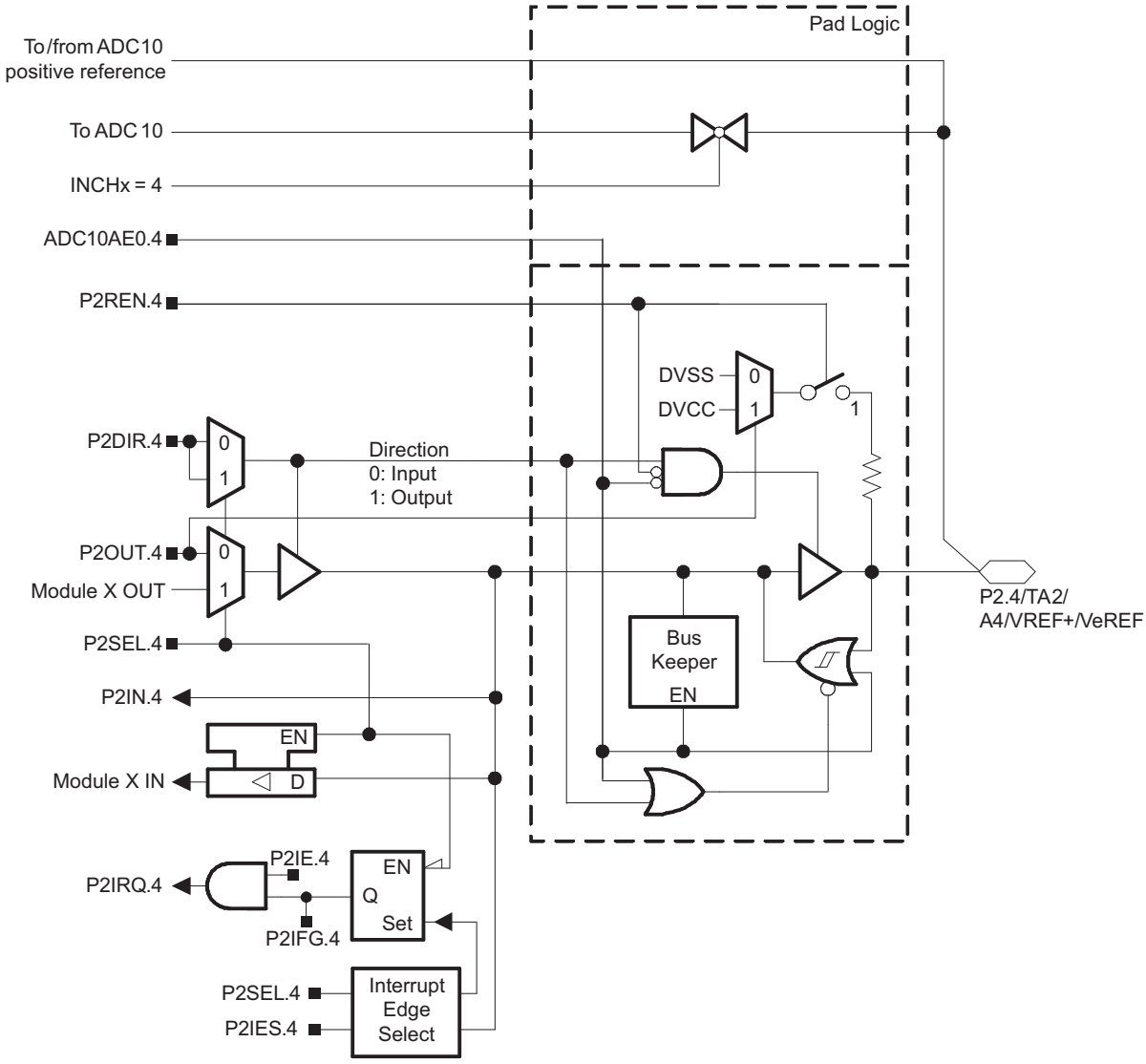

Table 6-21. Port P2 (P2.4) Pin Functions

PIN NAME (P2.x)	x	y	FUNCTION	CONTROL BITS OR SIGNALS(1)		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.4/TA2/A4/ VREF+/VeREF+	4	4	P2.4(2) (I/O)	I: 0; O: 1	0	0
			Timer_A3.TA2	1	1	0
			A4/VREF+/VeREF+(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) Setting the ADC10AE0.y bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.19.8 Port P2 Pin Schematic: P2.5, Input/Output With Schmitt Trigger and External R_{OSC} for DCO

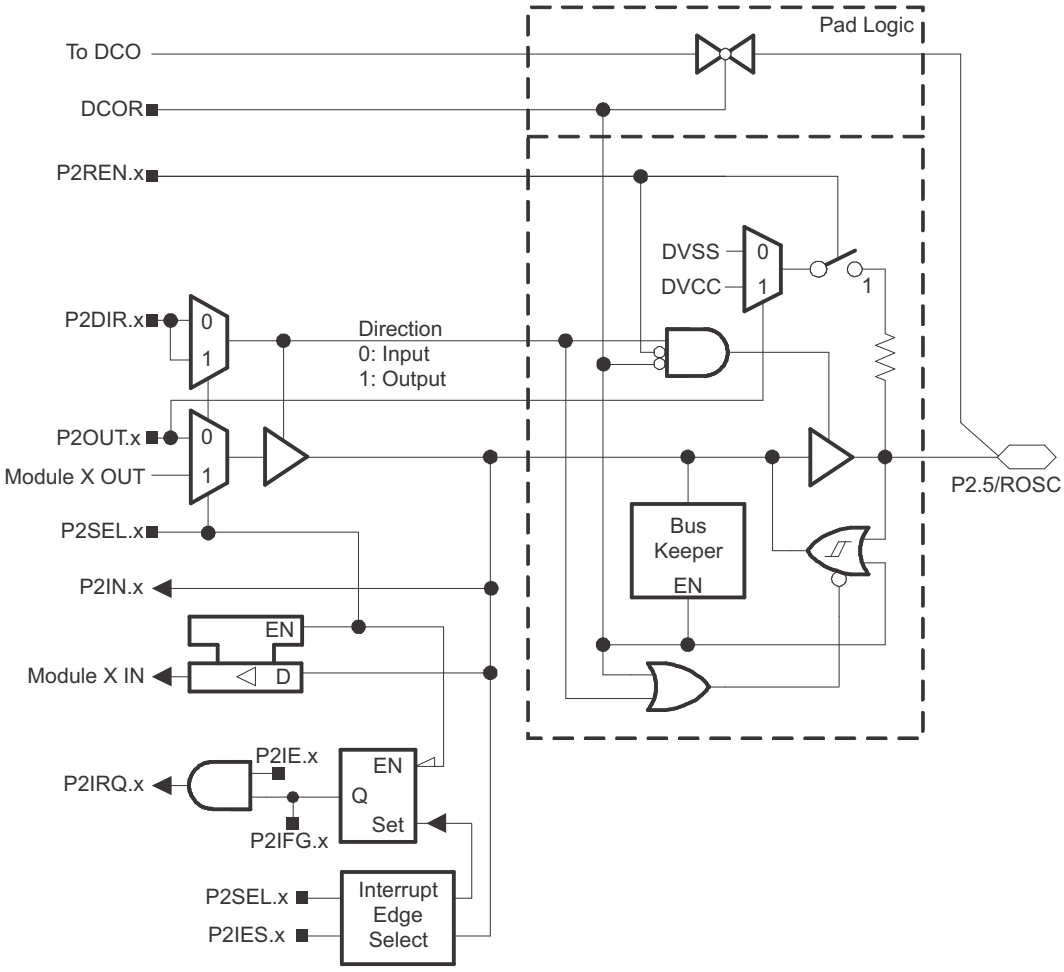

Table 6-22. Port P2 (P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P2DIR.x	P2SEL.x	DCOR
P2.5/R_{OSC}	5	P2.5(2) (I/O)	I: 0; O: 1	0	0
		N/A(3)	0	1	0
		DV_{SS}	1	1	0
		R_{OSC}	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) N/A = Not available or not applicable

6.19.9 Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger and Crystal Oscillator Input

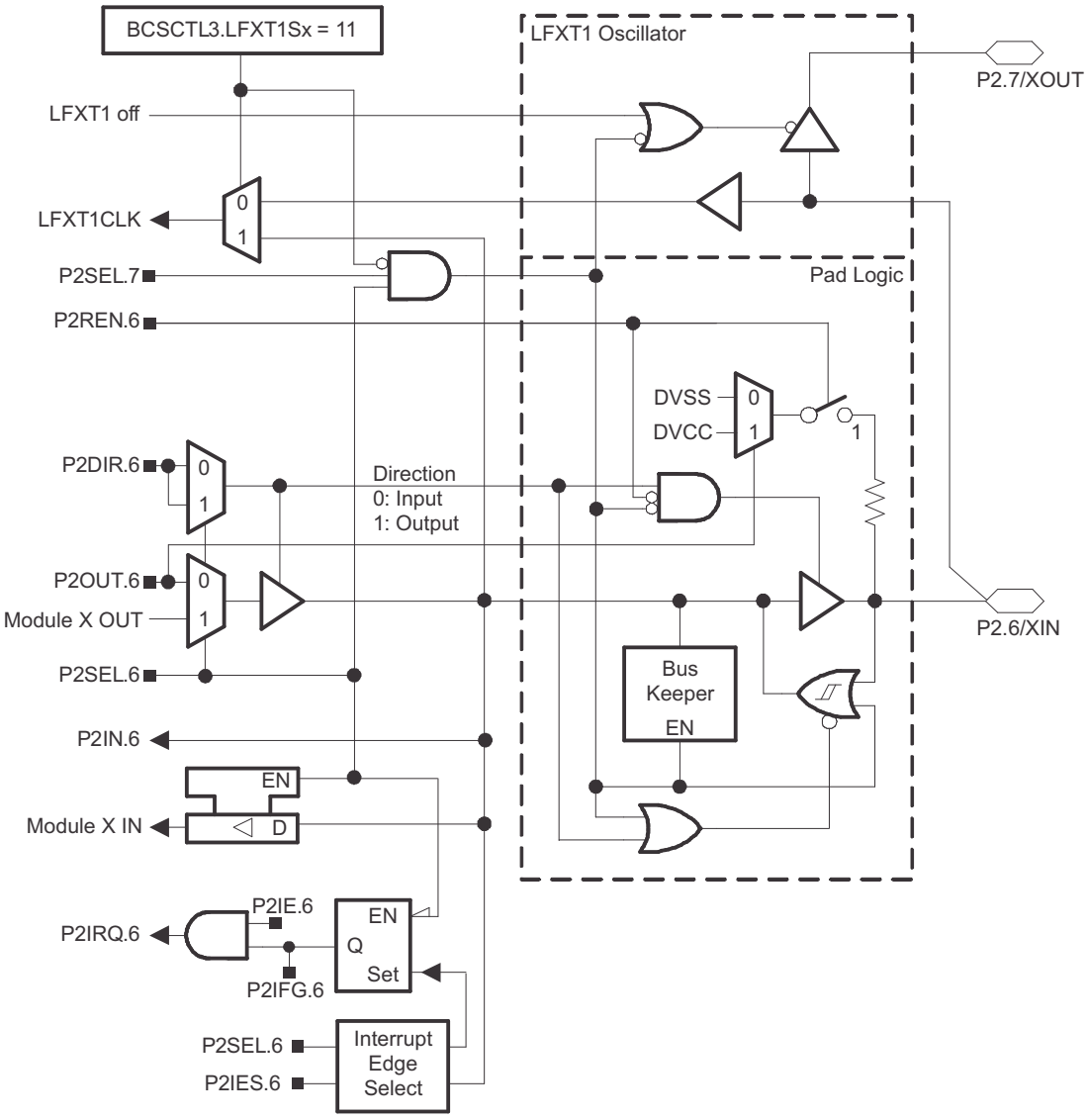

Table 6-23. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P2DIR.x	P2SEL.x
P2.6/XIN	6	P2.6 (I/O)	I: 0; O: 1	0
		XIN(2)	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)

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6.19.10 Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger and Crystal Oscillator Output

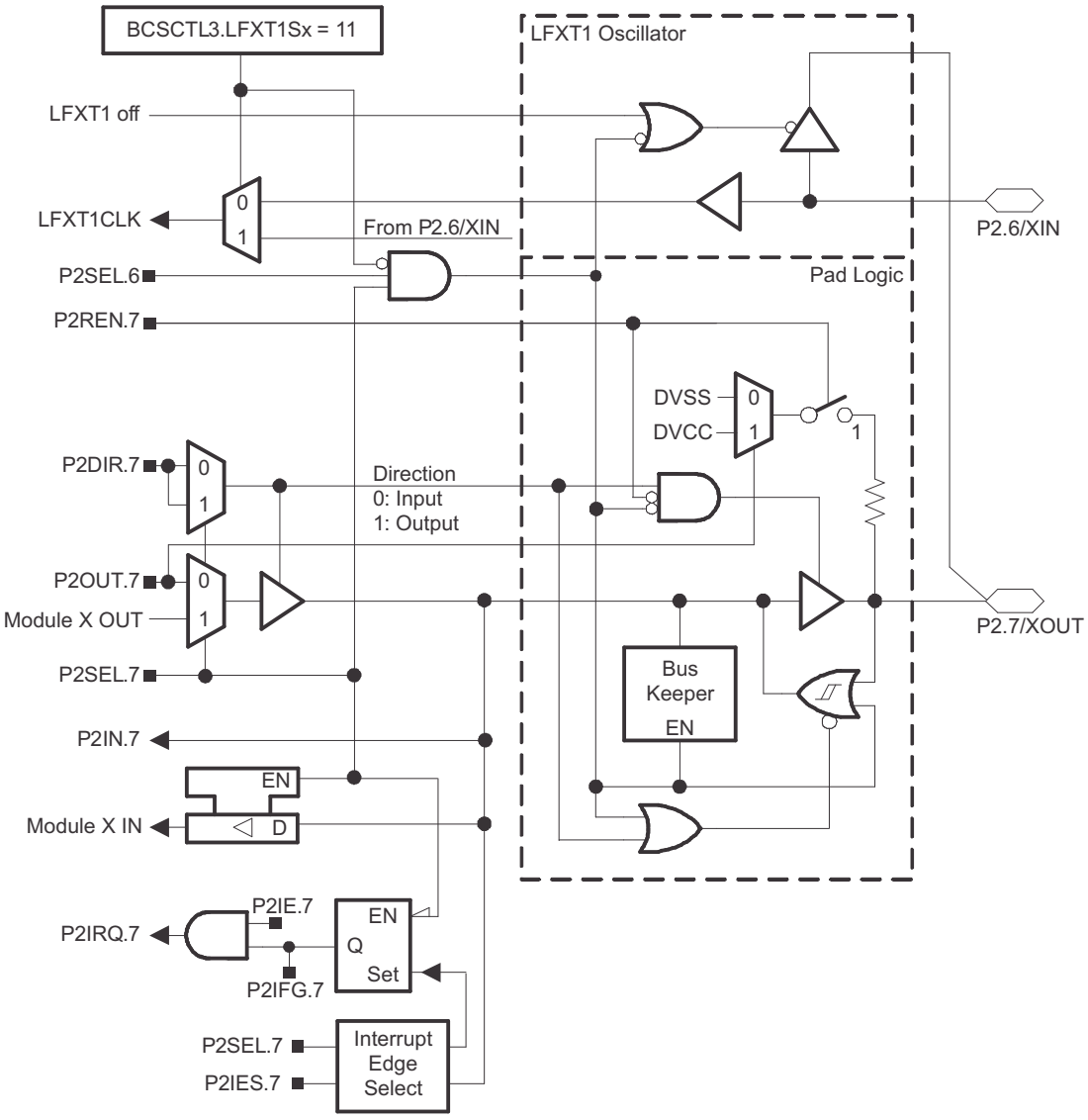

Table 6-24. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P2DIR.x	P2SEL.x
XOUT/P2.7	7	P2.7 (I/O)	I: 0; O: 1	0
		XOUT(2) (3)	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) If the pin XOUT/P2.7 is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

6.19.11 Port P3 Pin Schematic: P3.0, Input/Output With Schmitt Trigger

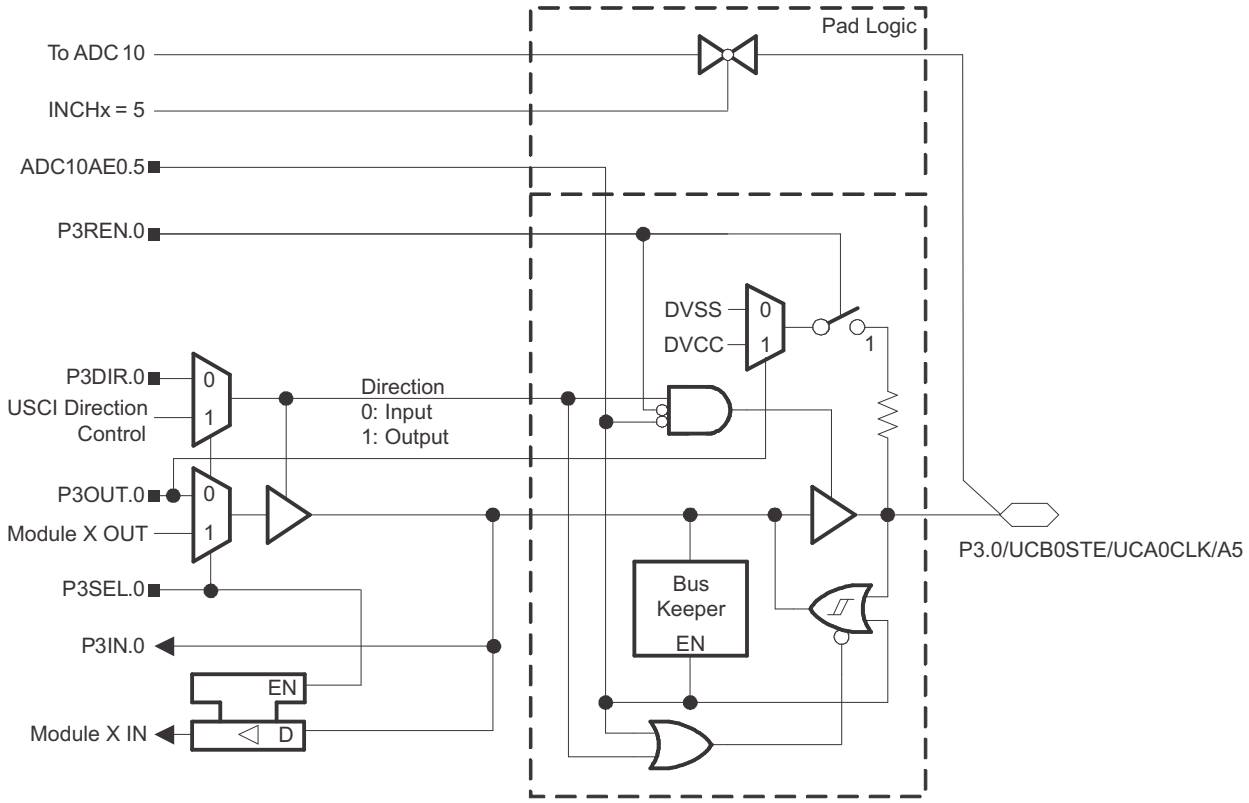

Table 6-25. Port P3 (P3.0) Pin Functions

PIN NAME (P1.x)	x	y	FUNCTION	CONTROL BITS OR SIGNALS(1)		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.0/UCB0STE/ UCA0CLK/A5	0	5	P3.0(2) (I/O)	I: 0; O: 1	0	0
			UCB0STE/UCA0CLK(3) (4)	X	1	0
			A5(5)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) The pin direction is controlled by the USCI module.
(4) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(5) Setting the ADC10AE0.y bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.19.12 Port P3 Pin Schematic: P3.1 to P3.5, Input/Output With Schmitt Trigger

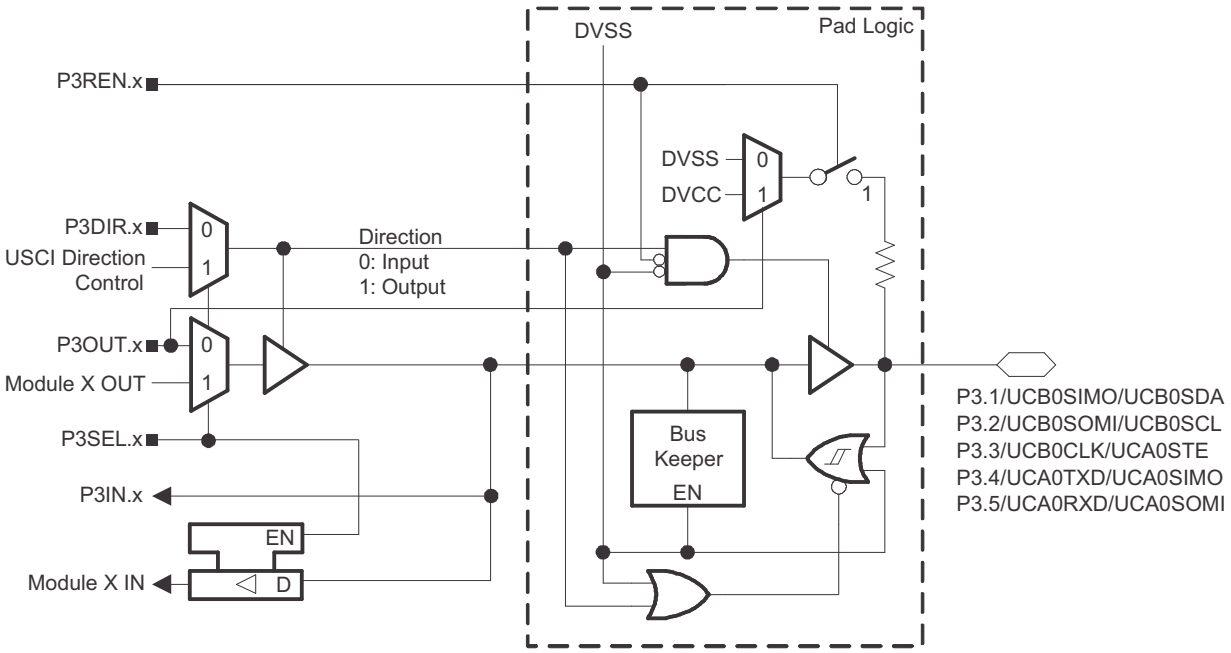

Table 6-26. Port P3 (P3.1 to P3.5) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P3DIR.x	P3SEL.x
P3.1/UCB0SIMO/UCB0SDA	1	P3.1(2) (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA(3)	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2(2) (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL(3)	X	1
P3.3/UCB0CLK/UCA0STE	3	P3.3(2) (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE(3) (4)	X	1
P3.4/UCA0TXD/UCA0SIMO	4	P3.4(2) (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO(3)	X	1
P3.5/UCA0RXD/UCA0SOMI	5	P3.5(2) (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI(3)	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) The pin direction is controlled by the USCI module.
(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode even if 4-wire SPI mode is selected.

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6.19.13 Port P3 Pin Schematic: P3.6 to P3.7, Input/Output With Schmitt Trigger

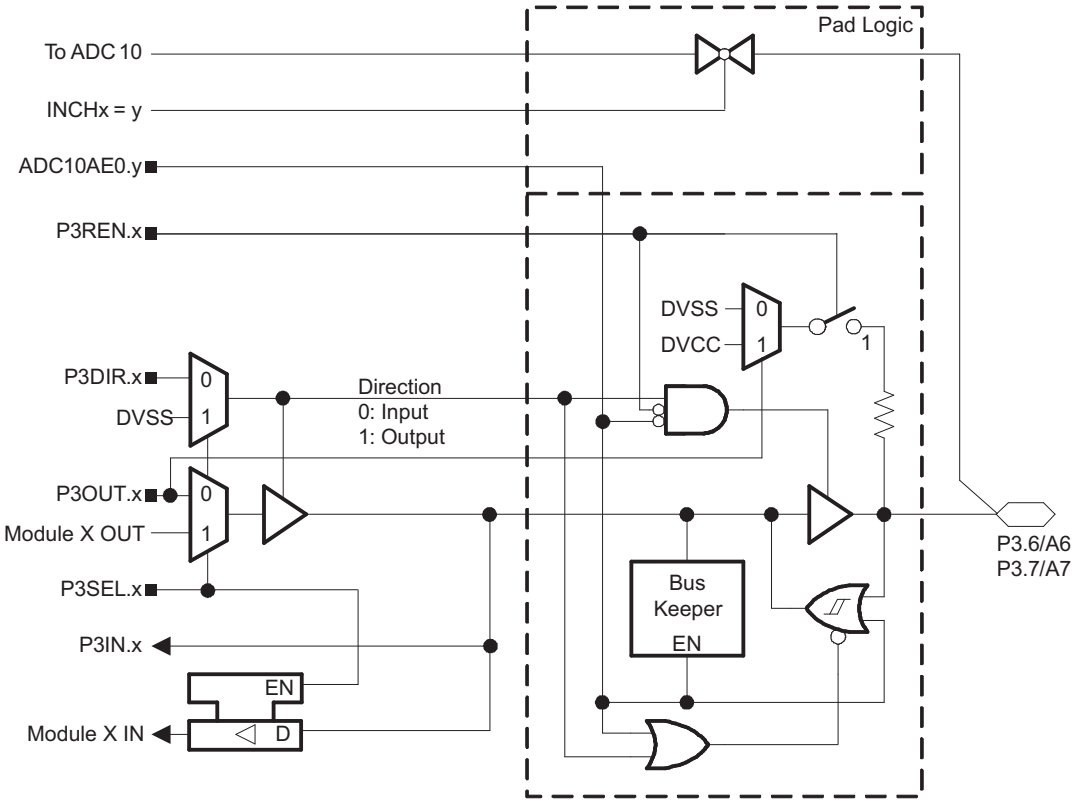

Table 6-27. Port P3 (P3.6, P3.7) Pin Functions

PIN NAME (P3.x)	x	y	FUNCTION	CONTROL BITS OR SIGNALS(1)		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.6/A6	6	6	P3.6(2) (I/O)	I: 0; O: 1	0	0
			A6/(3)	X	X	1
P3.7/A7	7	7	P3.7(2) (I/O)	I: 0; O: 1	0	0
			A7(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) Setting the ADC10AE0.y bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.19.14 Port P4 Pin Schematic: P4.0 to P4.2, Input/Output With Schmitt Trigger

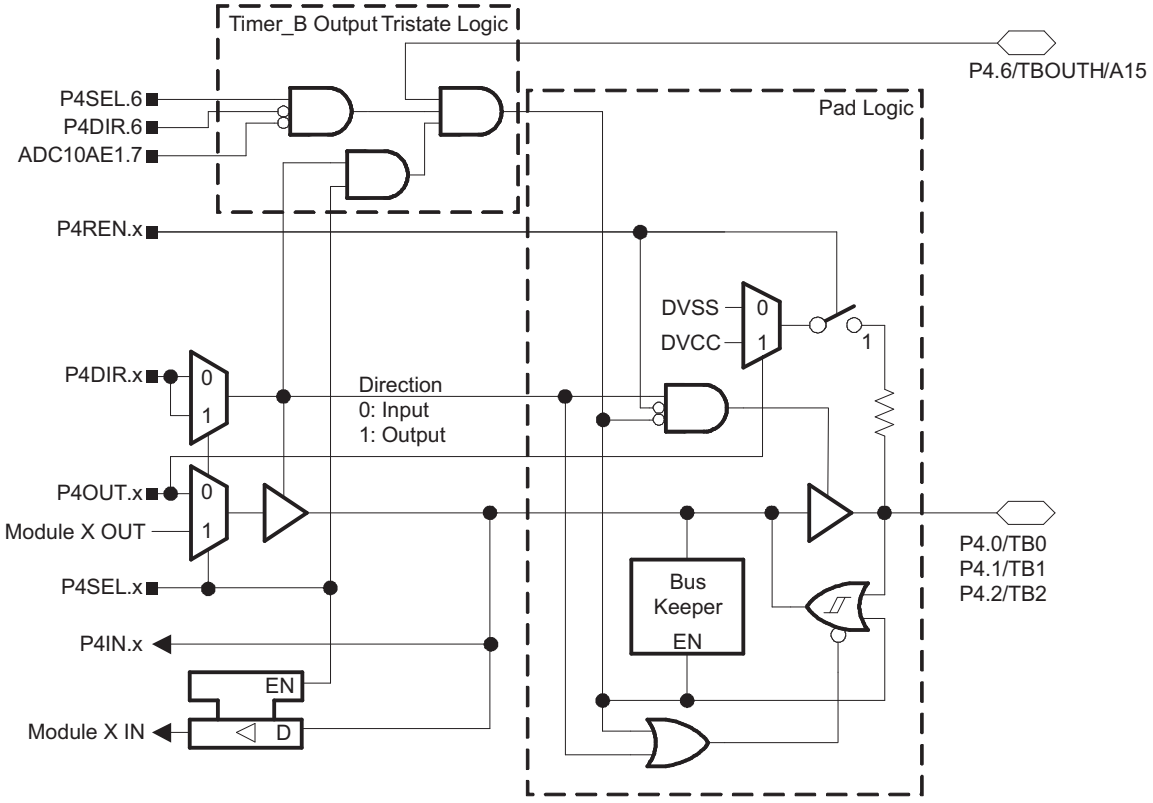

Table 6-28. Port P4 (P4.0 to P4.2) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0(1) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI0A	0	1
		Timer_B3.TB0	1	1
P4.1/TB1	1	P4.1(1) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.TB1	1	1
P4.2/TB2	2	P4.2(1) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI2A	0	1
		Timer_B3.TB2	1	1

(1) Default after reset (PUC, POR)

6.19.15 Port P4 Pin Schematic: P4.3 to P4.4, Input/Output With Schmitt Trigger

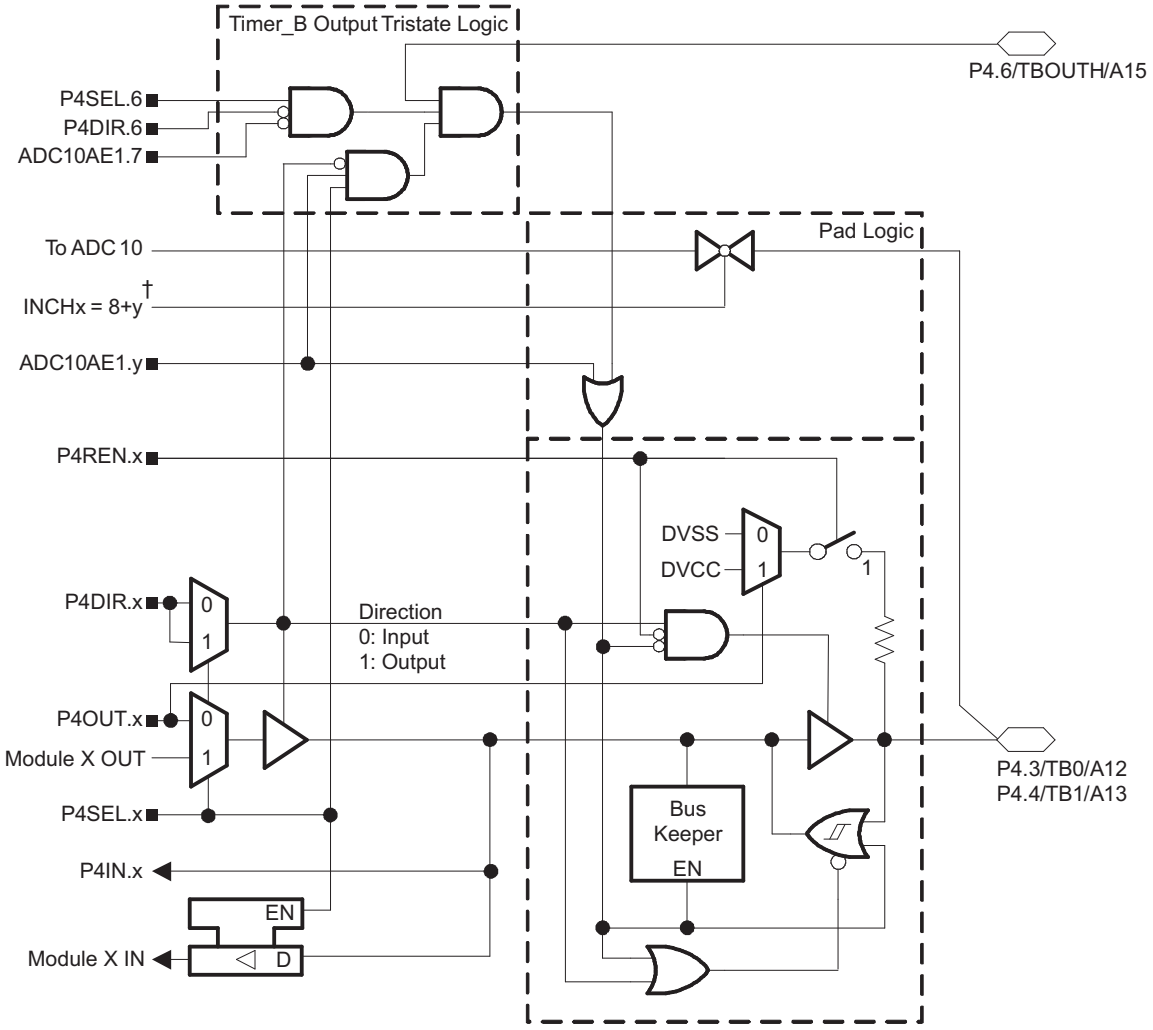

Table 6-29. Port P4 (P4.3 to P4.4) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS OR SIGNALS(1)		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.3/TB0/A12	3	4	P4.3(2) (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI0B	0	1	0
			Timer_B3.TB0	1	1	0
			A12(3)	X	X	1
P4.4/TB1/A13	4	5	P4.4(2) (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI1B	0	1	0
			Timer_B3.TB1	1	1	0
			A13(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) Setting the ADC10AE1.y bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.19.16 Port P4 Pin Schematic: P4.5, Input/Output With Schmitt Trigger

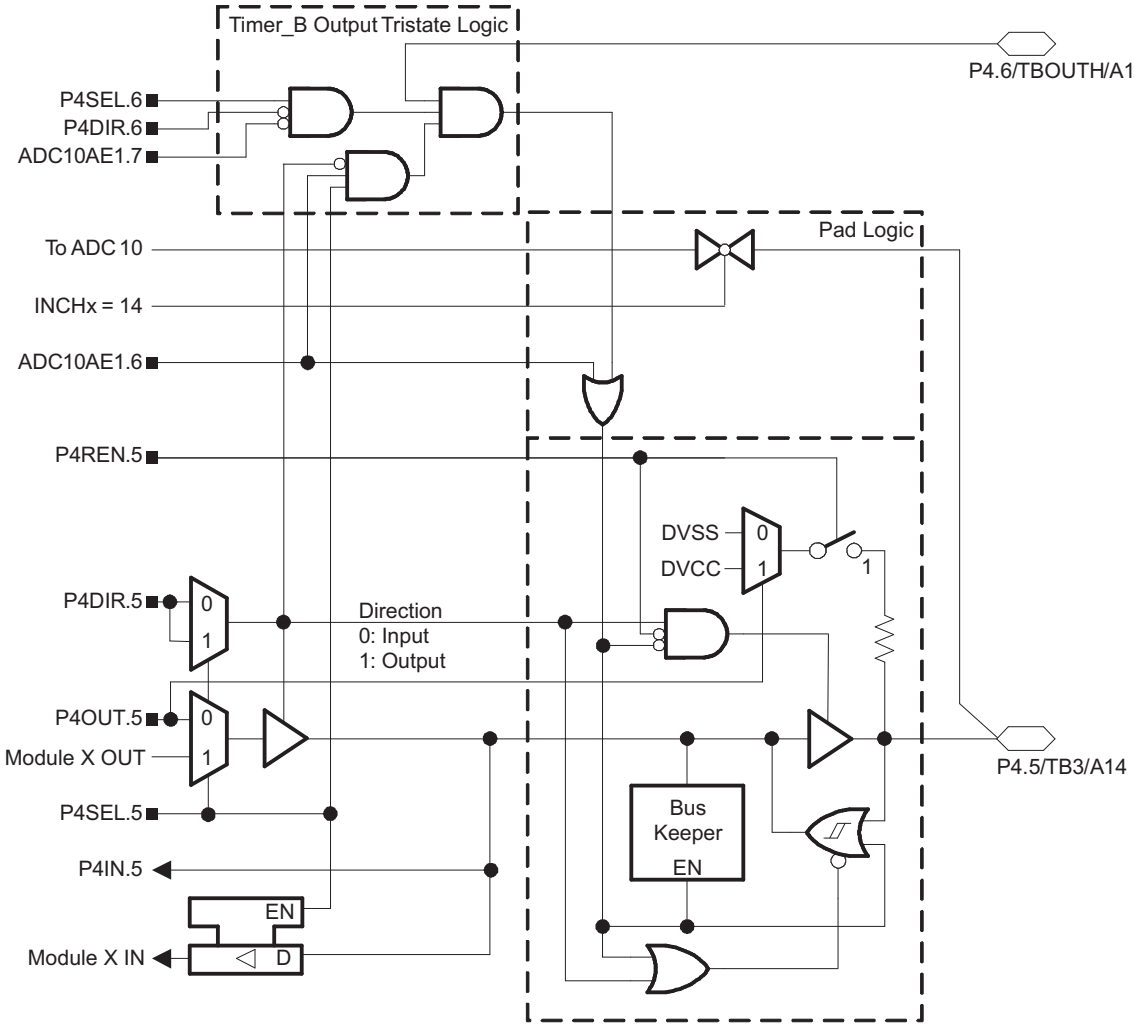

Table 6-30. Port P4 (P4.5) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS OR SIGNALS(1)		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.5/TB3/A14	5	6	P4.5(2) (I/O)	I: 0; O: 1	0	0
			Timer_B3.TB2	1	1	0
			A14(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) Setting the ADC10AE1.y bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.19.17 Port P4 Pin Schematic: P4.6, Input/Output With Schmitt Trigger

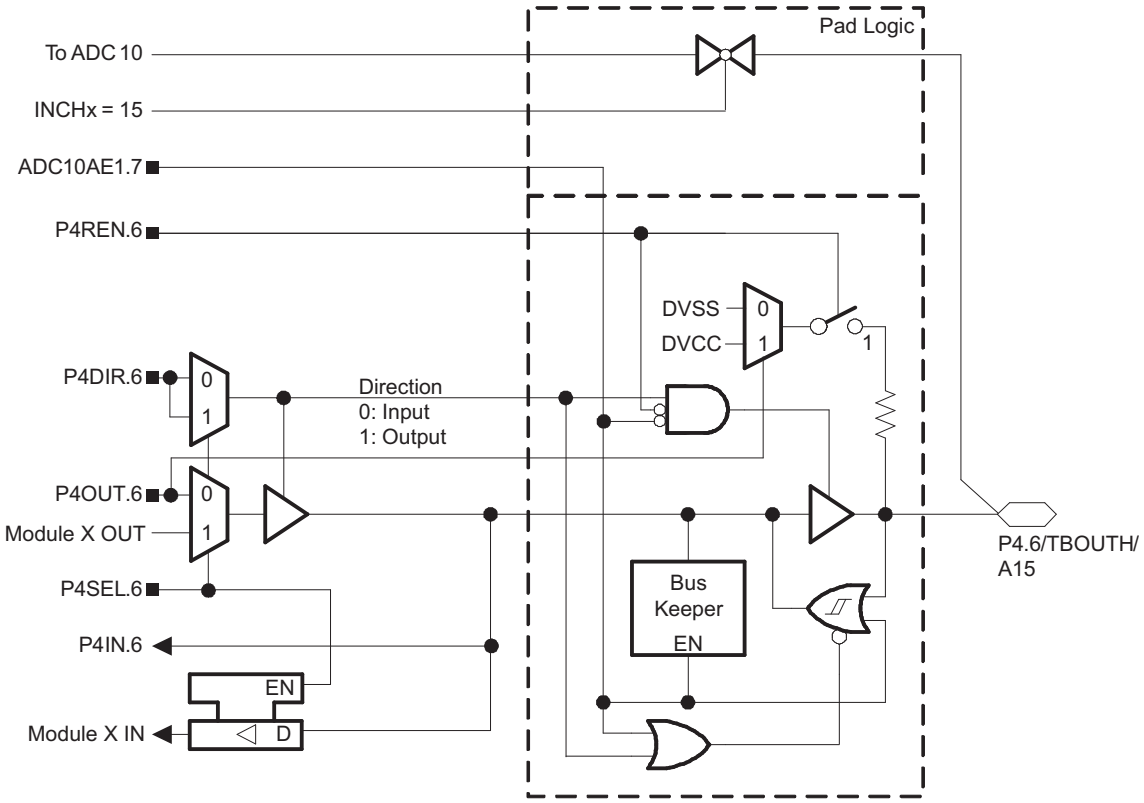

Table 6-31. Port P4 (P4.6) Pin Functions

PIN NAME (P4.x)	x	y	FUNCTION	CONTROL BITS OR SIGNALS(1)		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.6/TBOUTH/A15	6	7	P4.6(2) (I/O)	I: 0; O: 1	0	0
			TBOUTH	0	1	0
			DV_{SS}	1	1	0
			A15(3)	X	X	1

(1) X = Don't care
(2) Default after reset (PUC, POR)
(3) Setting the ADC10AE1.y bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

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6.19.18 Port P4 Pin Schematic: P4.7, Input/Output With Schmitt Trigger

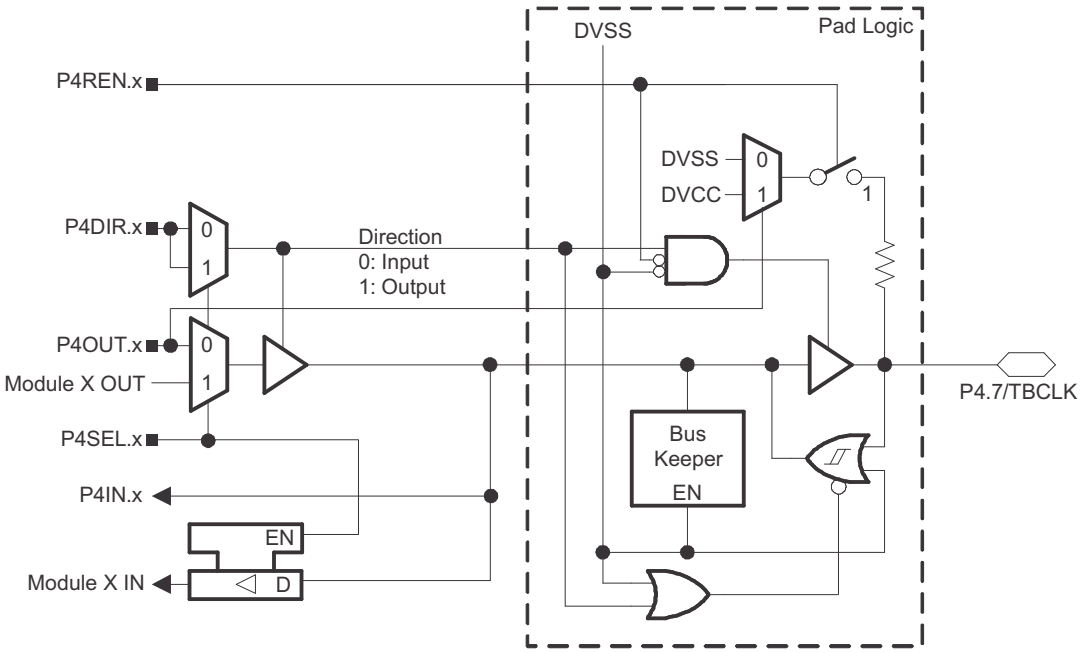

Table 6-32. Port P4 (Pr.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P4DIR.x	P4SEL.x
P4.7/TBCLK	7	P4.7[1] (I/O)	I: 0; O: 1	0
		Timer_B3.TBCLK	0	1
		DV_{SS}	1	1

(1) Default after reset (PUC, POR)

6.19.19 JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR, the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 6-1). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

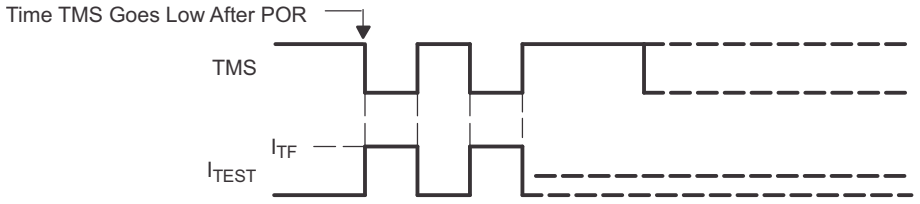

Figure 6-1. Fuse Check Mode Current

NOTE

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the Bootstrap Loader section for more information.

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7 器件和文档支持

7.1 器件支持

7.1.1 *开始使用*

有关 MSP430™ 系列器件、工具和库相关信息，请访问入门页面。

7.1.2 Development Tools Support

All MSP430™ microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp430tools.

7.1.2.1 Hardware Features

See the *Code Composer Studio for MSP430 User's Guide* (SLAU157) for details on the available features.

MSP430 Architecture	4-Wire JTAG	2-Wire JTAG	Break-points (N)	Range Break-points	Clock Control	State Sequencer	Trace Buffer	LPMx.5 Debugging Support
MSP430	Yes	Yes	2	No	Yes	No	No	No

7.1.2.2 Recommended Hardware Options

7.1.2.2.1 Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

Package	Target Board and Programmer Bundle	Target Board Only
38-pin TSSOP (DA)	MSP-FET430U38	MSP-TS430DA38

7.1.2.2.2 Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See www.ti.com/msp430tools for details.

7.1.2.2.3 Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third party suppliers. See the full list of available tools at www.ti.com/msp430tools.

7.1.2.2.4 Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

Part Number	PC Port	Features	Provider
MSP-GANG	Serial and USB	Program up to eight devices at a time. Works with PC or standalone.	Texas Instruments

7.1.2.3 Recommended Software Options

7.1.2.3.1 Integrated Development Environments

Software development tools are available from TI or from third parties. Open source solutions are also available.

This device is supported by Code Composer Studio™ IDE (CCS).

7.1.2.3.2 MSP430Ware

MSP430Ware is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. MSP430Ware is available as a component of CCS or as a standalone package.

7.1.2.3.3 Command-Line Programmer

MSP430 Flasher is an open-source, shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 Flash without the need for an IDE.

7.1.3 器件和开发工具命名规则

为了指明产品开发周期所处的阶段，TI 为所有 MSP430 MCU 器件和支持工具的产品型号分配了前缀。 每个 MSP430 MCU 商用系列产品成员具有以下三个前缀中的一个：MSP，PMS 或 XMS（例如，MSP430F5259）。 德州仪器 (TI) 建议为其支持的工具使用三个可能前缀指示符中的两个：MSP 和 MSPX。 这些前缀代表了产品从工程原型机（其中 XMS 针对器件，而 MSPX 针对工具）直到完全合格的生产器件和工具（其中 MSP 针对器件，而 MSP 针对工具）的产品开发进化阶段。

器件开发进化流程：

XMS - 试验器件不一定代表最终器件的电气技术规格

PMS - 最终的芯片模型符合器件的电气技术规格，但是未经完整的质量和可靠性验证

MSP - 完全合格的生产器件

支持工具开发进化流程：

MSPX - 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品。

MSP – 完全合格的开发支持产品

XMS 和 PMS 器件和 MSPX 开发支持工具在供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

MSP 器件和 MSP 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。 TI 的标准保修证书适用。

预测显示原型器件（XMS 和 PMS）的故障率大于标准生产器件。 由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。 只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。 这个后缀包括封装类型（例如，PZP）和温度范围（如，T）。图 7-1 提供了读取任一系列产品成员完整器件名称的图例。

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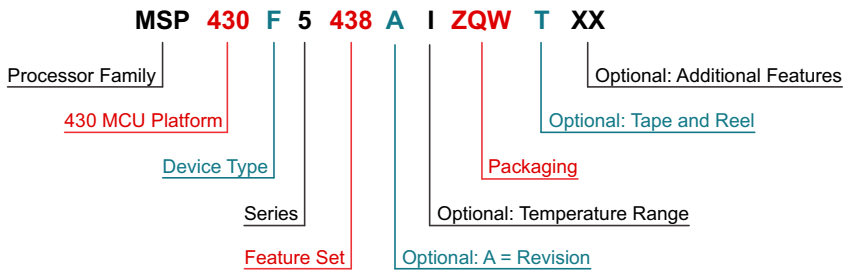

Processor Family	CC = Embedded RF Radio MSP = Mixed Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
430 MCU Platform	TI's Low Power Microcontroller Platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BT = Preprogrammed with Bluetooth BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 Series = Up to 8 MHz 2 Series = Up to 16 MHz 3 Series = Legacy 4 Series = Up to 16 MHz w/ LCD	5 Series = Up to 25 MHz 6 Series = Up to 25 MHz w/ LCD 0 = Low Voltage Series
Feature Set	Various Levels of Integration Within a Series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105°C	
Packaging	www.ti.com/packaging	
Optional: Tape and Reel	T = Small Reel (7 inch) R = Large Reel (11 inch) No Markings = Tube or Tray	
Optional: Additional Features	-EP = Enhanced Product (-40°C to 105°C) -HT = Extreme Temperature Parts (-55°C to 150°C) -Q1 = Automotive Q100 Qualified	

图 **7-1.** 器件命名规则

7.2 文档支持

以下文档描述了 MSP430G2x44 器件。 www.ti.com 网站上提供了这些文档的副本。

SLAU144 《***MSP430x2xx 系列用户指南***》。详细介绍此器件系列中提供的模块和外设。

SLAZ497 《***MSP430G2744 器件勘误表***》。 描述了针对此器件的所有芯片修订版本功能技术规格的已知例外情况。

SLAZ498 《***MSP430G2544 器件勘误表***》。 描述了针对此器件的所有芯片修订版本功能技术规格的已知例外情况。

SLAZ499 《***MSP430G2444 器件勘误表***》。 描述了针对此器件的所有芯片修订版本功能技术规格的已知例外情况。

7.3 相关链接

表 7-1 列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 7-1. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
MSP430G2744	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430G2544	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430G2444	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.5 商标

MSP430, Code Composer Studio, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

7.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

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8 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430G2444IDA38	Active	Production	TSSOP (DA) | 38	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2444
MSP430G2444IDA38.B	Active	Production	TSSOP (DA) | 38	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2444
MSP430G2444IDA38R	Active	Production	TSSOP (DA) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2444
MSP430G2444IDA38R.B	Active	Production	TSSOP (DA) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2444
MSP430G2444IRHA40R	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2444
MSP430G2444IRHA40R.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2444
MSP430G2444IRHA40T	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2444
MSP430G2444IRHA40T.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2444
MSP430G2444IYFFT	Active	Production	DSBGA (YFF) | 49	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430G2444
MSP430G2444IYFFT.B	Active	Production	DSBGA (YFF) | 49	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430G2444
MSP430G2544IDA38	Active	Production	TSSOP (DA) | 38	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2544
MSP430G2544IDA38.B	Active	Production	TSSOP (DA) | 38	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2544
MSP430G2544IDA38R	Active	Production	TSSOP (DA) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2544
MSP430G2544IDA38R.B	Active	Production	TSSOP (DA) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2544
MSP430G2544IRHA40R	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2544
MSP430G2544IRHA40R.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2544
MSP430G2544IRHA40T	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2544
MSP430G2544IRHA40T.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2544
MSP430G2744IDA38	Active	Production	TSSOP (DA) | 38	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2744
MSP430G2744IDA38.B	Active	Production	TSSOP (DA) | 38	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2744
MSP430G2744IDA38R	Active	Production	TSSOP (DA) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2744
MSP430G2744IDA38R.B	Active	Production	TSSOP (DA) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430G2744

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430G2744IRHA40R	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2744
MSP430G2744IRHA40R.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2744
MSP430G2744IRHA40T	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2744
MSP430G2744IRHA40T.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 G2744
MSP430G2744IYFFR	Active	Production	DSBGA (YFF) | 49	2500 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430G2744
MSP430G2744IYFFR.B	Active	Production	DSBGA (YFF) | 49	2500 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430G2744

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

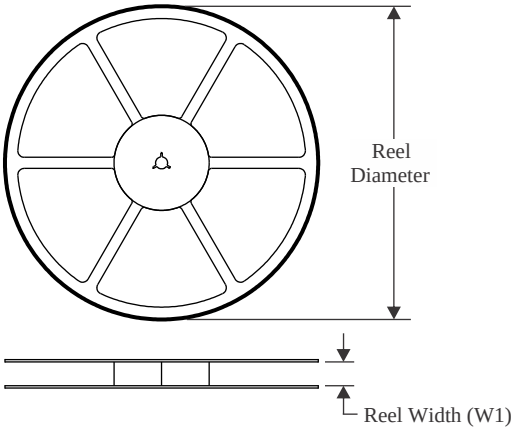
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

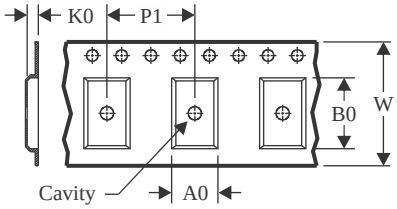
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

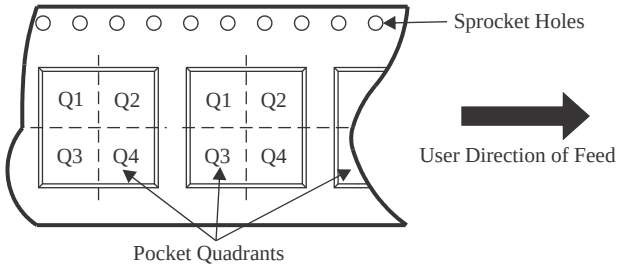


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

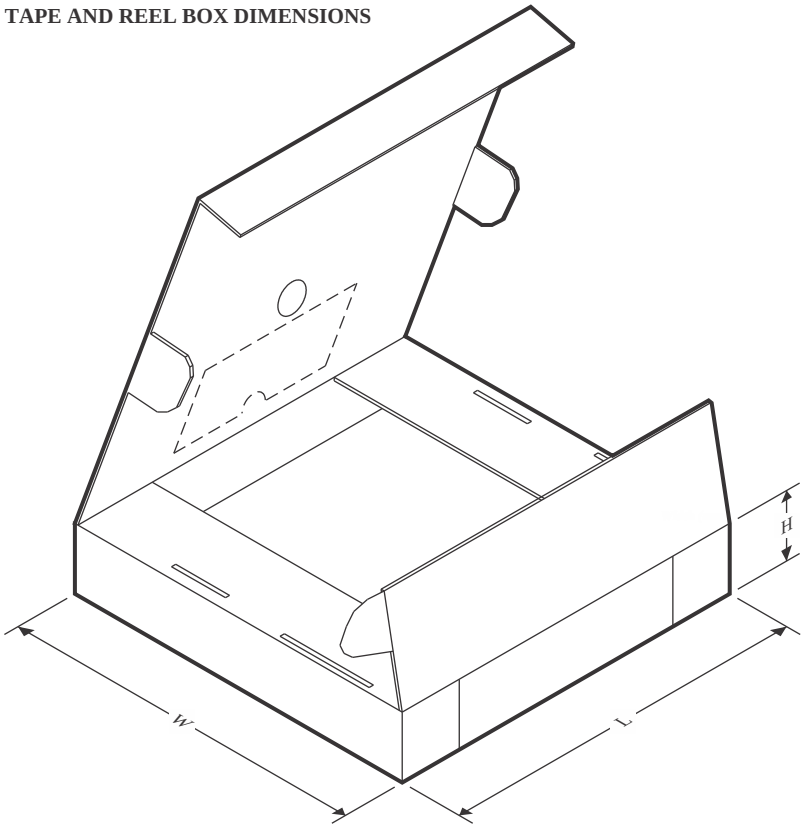


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430G2444IDA38R	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430G2444IRHA40R	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2444IRHA40R	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2444IRHA40T	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2444IRHA40T	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2444IYFFT	DSBGA	YFF	49	250	180.0	12.4	3.5	3.7	0.81	8.0	12.0	Q2
MSP430G2544IDA38R	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430G2544IRHA40R	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2544IRHA40R	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2544IRHA40T	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2544IRHA40T	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2744IDA38R	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430G2744IRHA40R	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2744IRHA40R	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2744IRHA40T	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430G2744IRHA40T	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430G2744IYFFR	DSBGA	YFF	49	2500	330.0	12.4	3.5	3.7	0.81	8.0	12.0	Q2

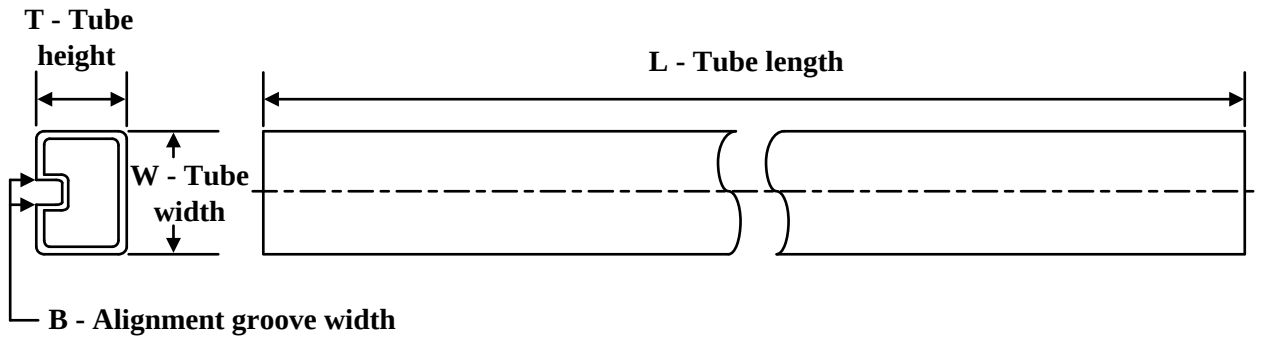
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430G2444IDA38R	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430G2444IRHA40R	VQFN	RHA	40	2500	367.0	367.0	35.0
MSP430G2444IRHA40R	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430G2444IRHA40T	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430G2444IRHA40T	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430G2444IYFFT	DSBGA	YFF	49	250	182.0	182.0	20.0
MSP430G2544IDA38R	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430G2544IRHA40R	VQFN	RHA	40	2500	367.0	367.0	35.0
MSP430G2544IRHA40R	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430G2544IRHA40T	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430G2544IRHA40T	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430G2744IDA38R	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430G2744IRHA40R	VQFN	RHA	40	2500	367.0	367.0	35.0
MSP430G2744IRHA40R	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430G2744IRHA40T	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430G2744IRHA40T	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430G2744IYFFR	DSBGA	YFF	49	2500	335.0	335.0	25.0

TUBE

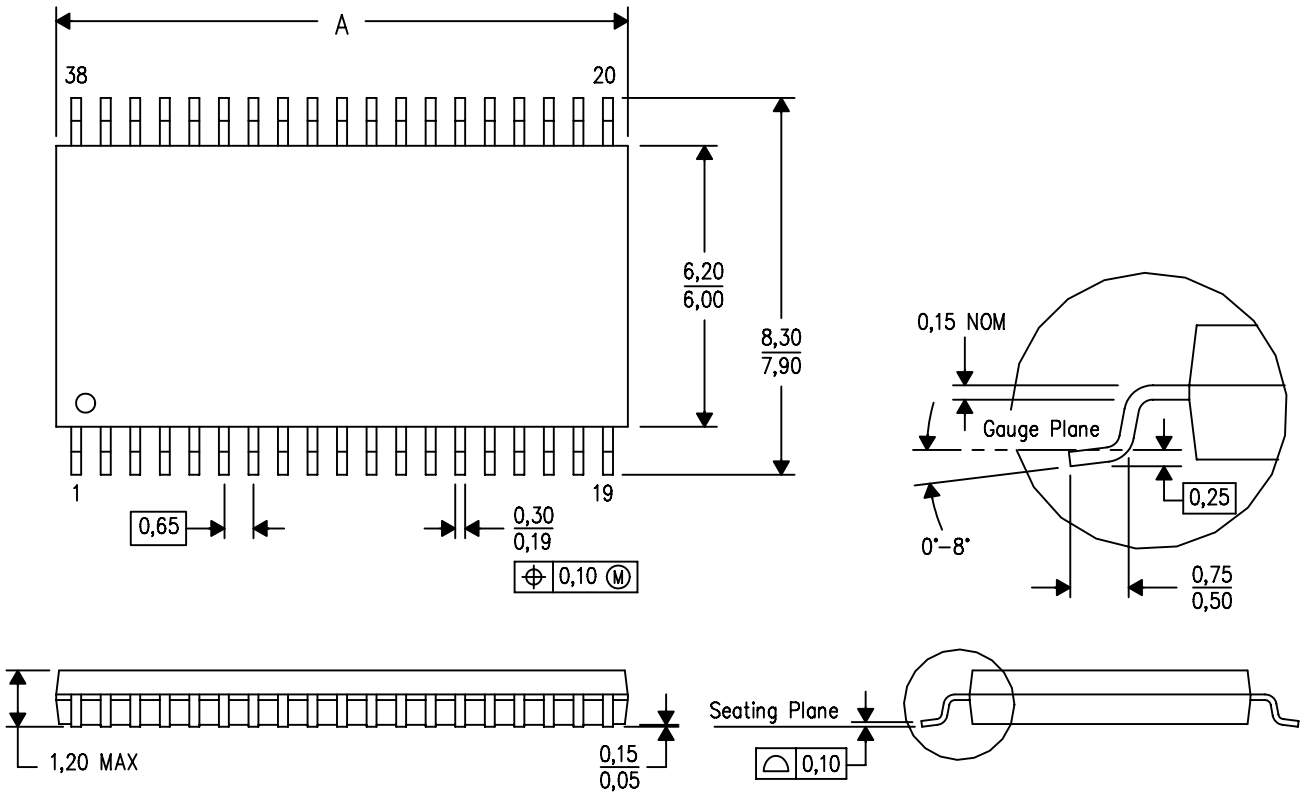


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430G2444IDA38	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430G2444IDA38.B	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430G2544IDA38	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430G2544IDA38.B	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430G2744IDA38	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430G2744IDA38.B	DA	TSSOP	38	40	530	11.89	3600	4.9

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN

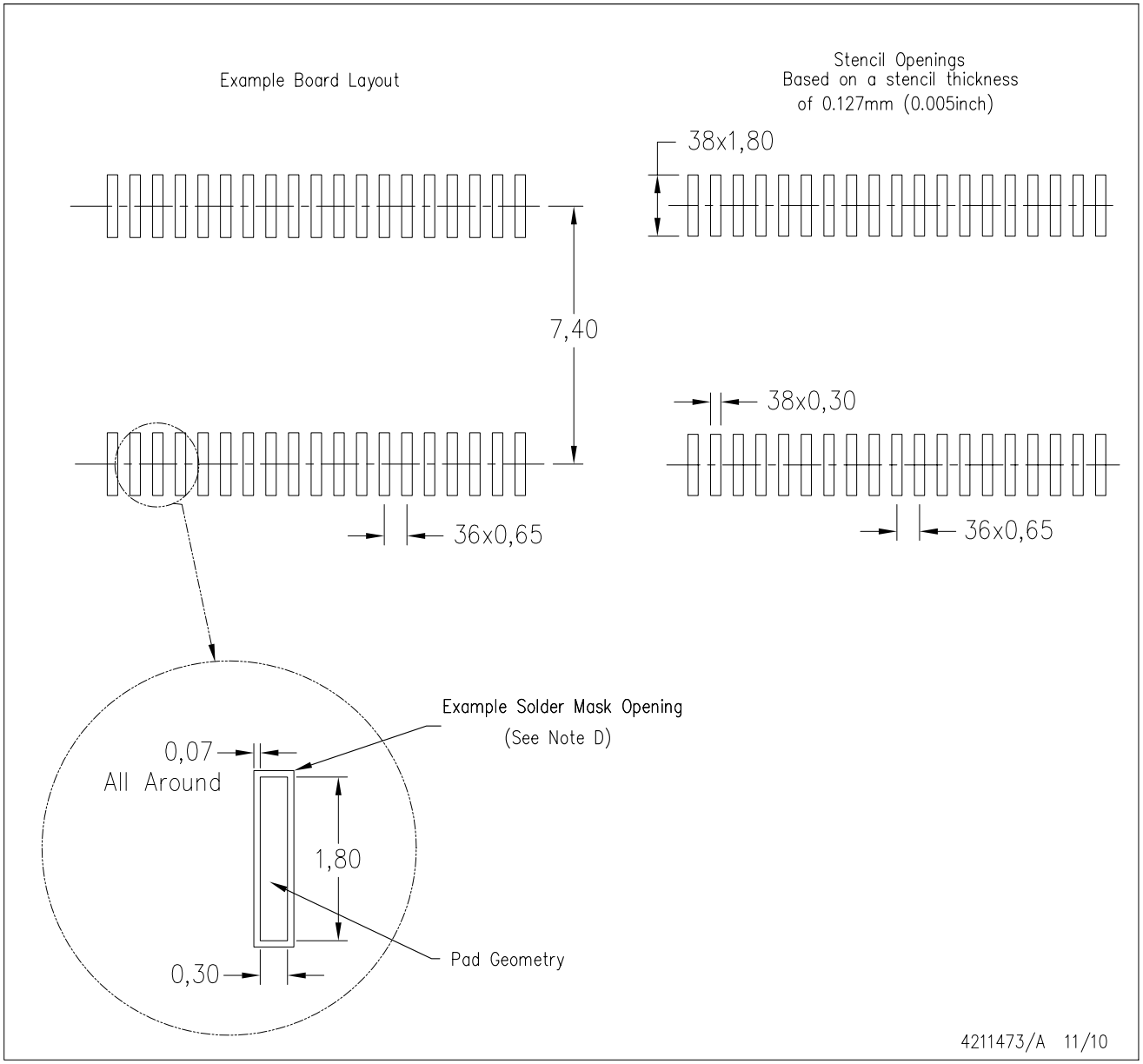


DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
△D MO–153 Variation	DB–1	DC	DD–1

4040066/F 01/2009

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
△D Falls within JEDEC MO–153, except 30 pin body length.

DA (R–PDSO–G38) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Contact the board fabrication site for recommended soldermask tolerances.

GENERIC PACKAGE VIEW

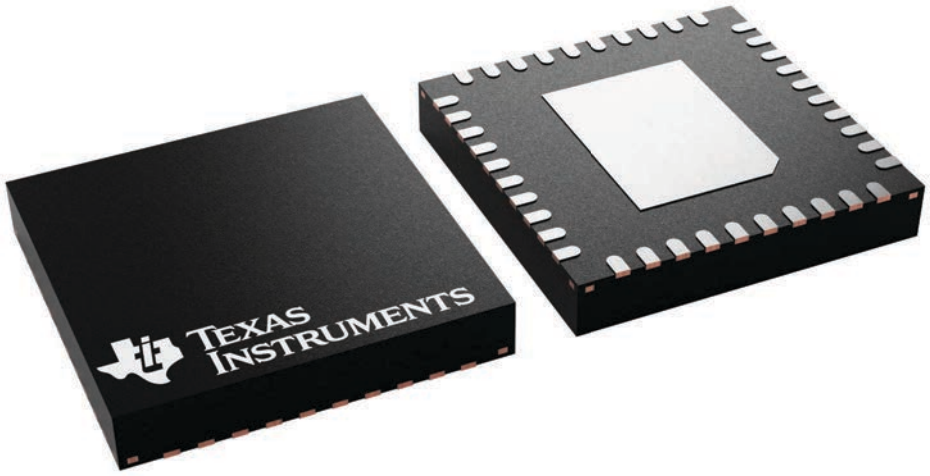
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



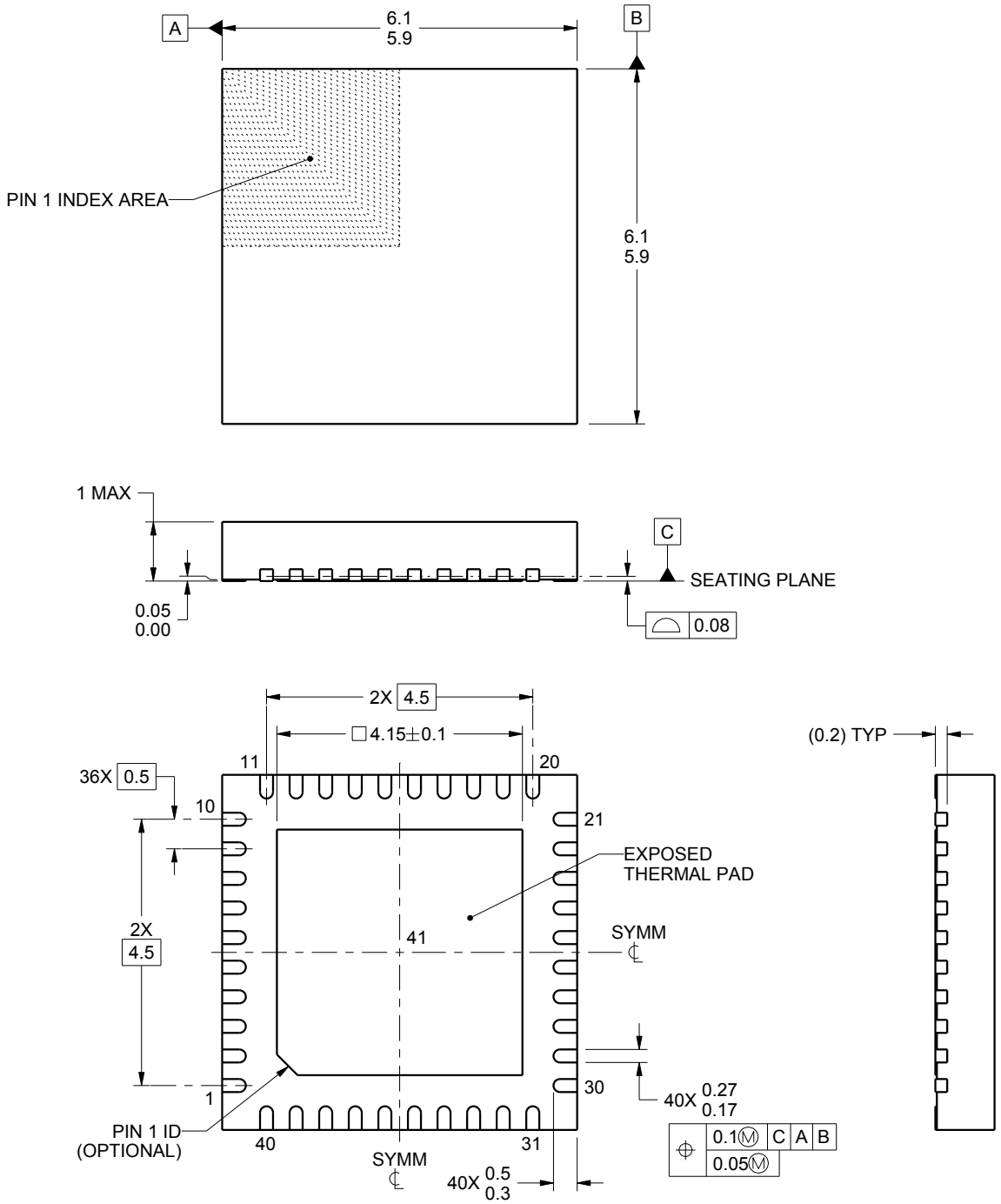
4225870/A

PACKAGE OUTLINE

RHA0040B

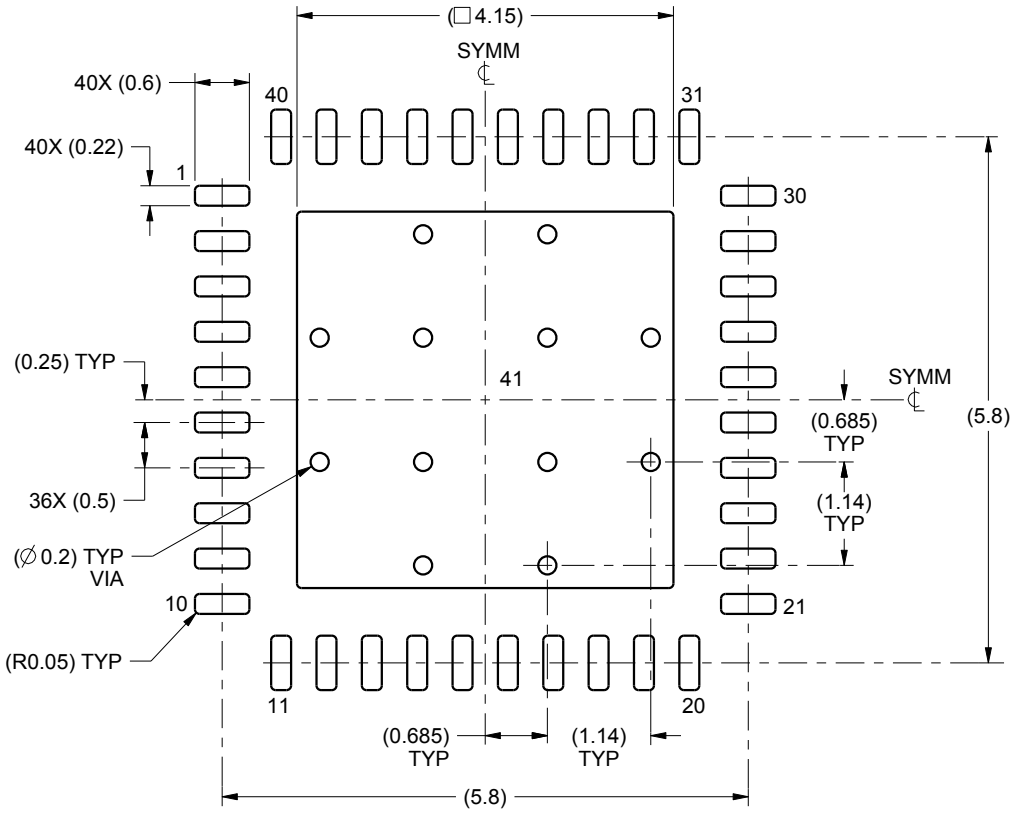
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

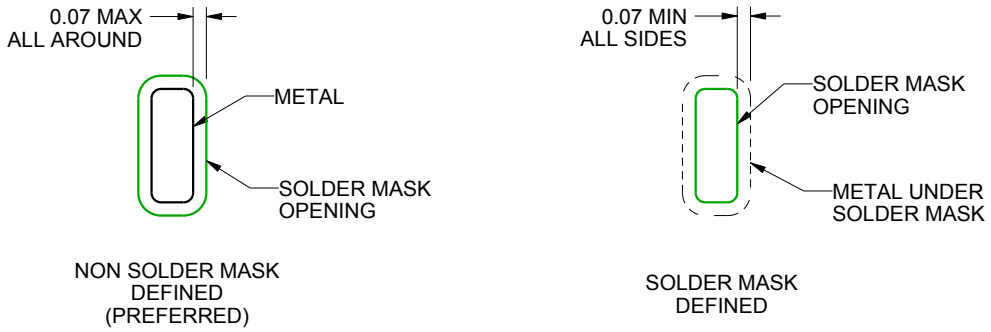


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X

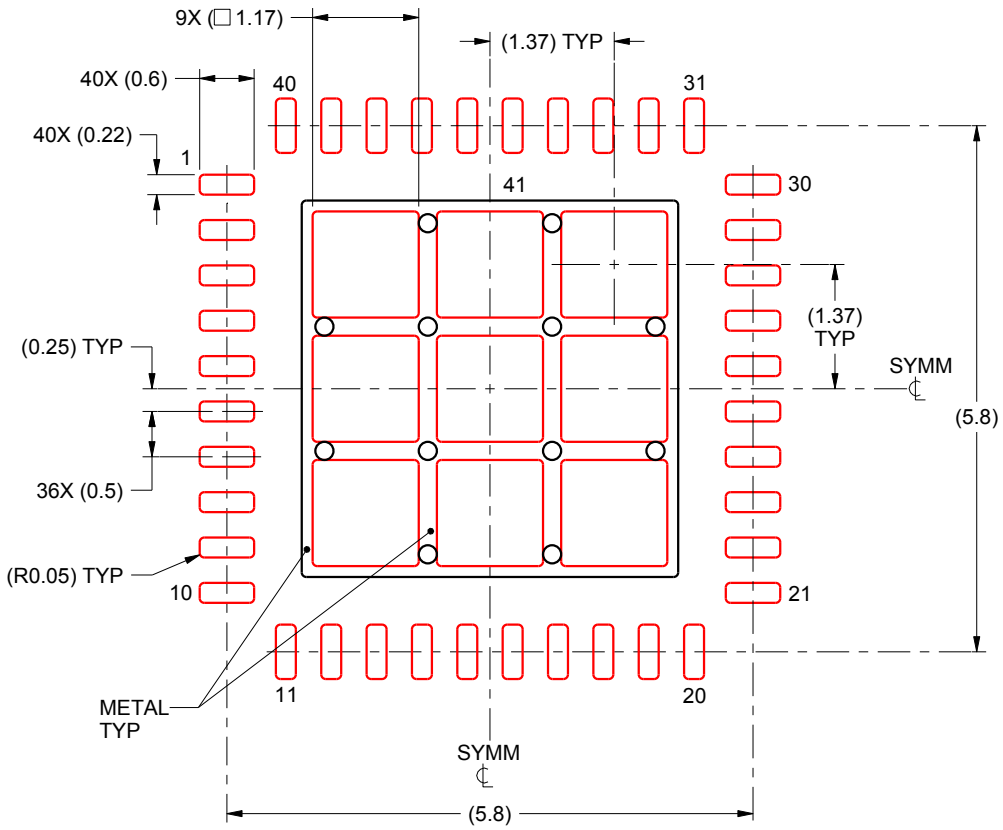


SOLDER MASK DETAILS

4219052/A 06/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

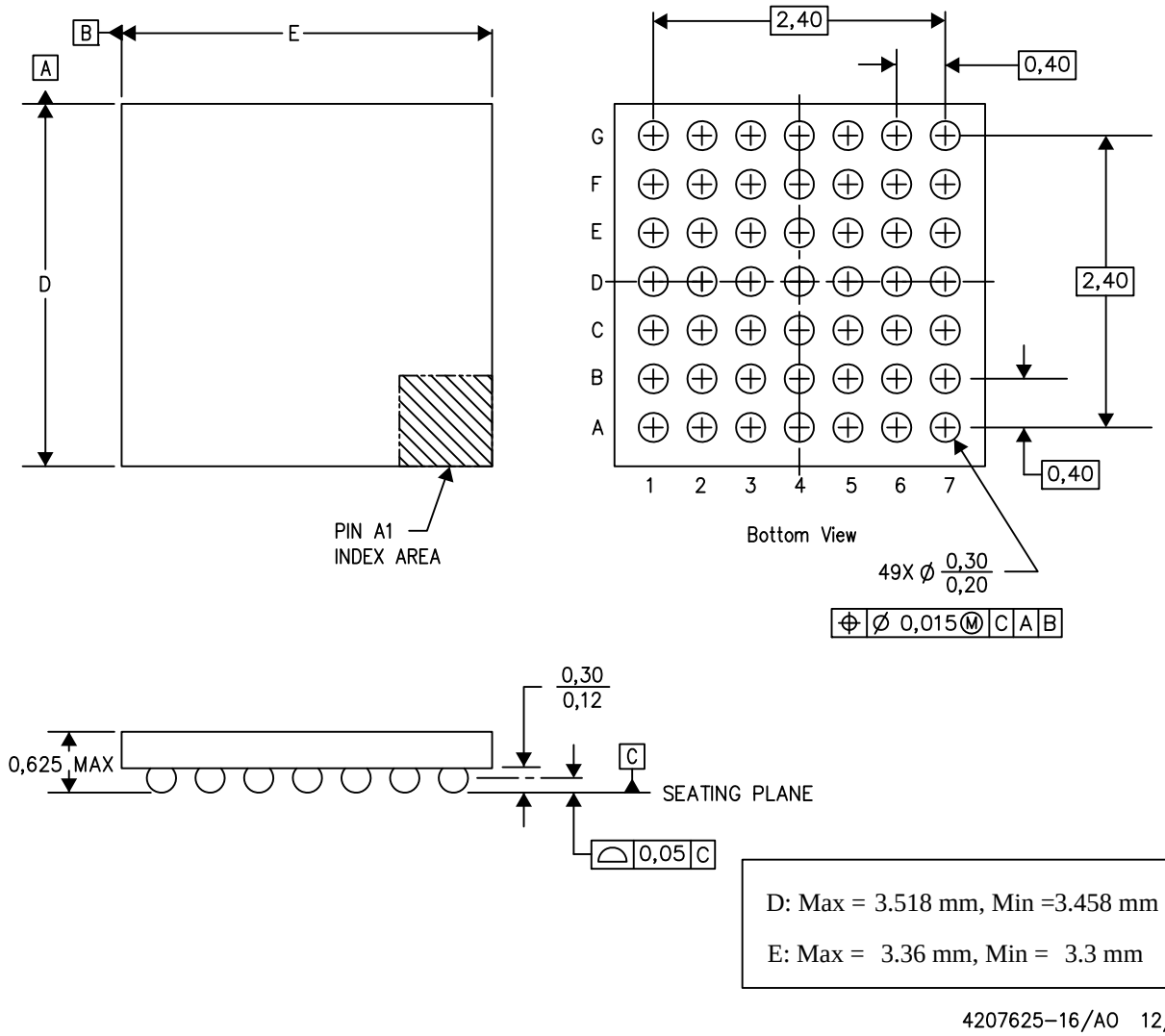
EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4219052/A 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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最后更新日期：2025 年 10 月