TEXAS INSTRUMENTS
MSP430FR6989, MSP430FR69891, MSP430FR6988, MSP430FR6987
MSP430FR5989, MSP430FR59891, MSP430FR5988, MSP430FR5987, MSP430FR5986
ZHCSCU7D – JUNE 2014 – REVISED AUGUST 2018

# MSP430FR698x(1)、MSP430FR598x(1) 混合信号微控制器

## 1 器件概述

### 1.1 特性

- 嵌入式微控制器
  - 高达 16MHz 时钟频率的 16 位 RISC 架构
  - 3.6V 至 1.8V 的宽电源电压范围（最低电源电压受限于 SVS 电平，请参阅 SVS 规格）
- 经优化的超低功耗模式
  - 工作模式：大约 100µA/MHz
  - 待机（具有低功率低频内部时钟源 (VLO) 的 LPM3）：0.4µA（典型值）
  - 实时时钟 (RTC) (LPM3.5)：0.35µA（典型值）(1)
  - 关断 (LPM4.5)：0.02µA（典型值）
- 超低功耗铁电 RAM (FRAM)
  - 高达 128KB 的非易失性存储器
  - 超低功耗写入
  - 125ns 每个字的快速写入（4ms 内写入 64KB）
  - 统一标准存储器 = 单个空间内的程序 + 数据 + 存储
  - $10^{15}$ 写入周期持久性
  - 抗辐射和非磁性
- 智能数字外设
  - 32 位硬件乘法器 (MPY)
  - 三通道内部直接存储器存取 (DMA)
  - 带有日历和和报警功能的 RTC
  - 5 个 16 位计时器，每个计时器具有多达 7 个捕捉/比较寄存器
  - 16 位和 32 位循环冗余校验器（CRC16、CRC32）
- 高性能模拟
  - 扩展扫描接口 (ESI)，可用于在后台测量水容积、热量和气体体积
  - 16 通道模拟比较器
  - 12 位模数转换器 (ADC)，具有内部基准和采样保持以及多达 16 个外部输入通道
  - 具有高达 320 段对比度控制的集成 LCD 驱动器
- 多功能输入/输出端口
  - 所有 P1 至 P10 以及 PJ 引脚均支持电容式触控功能，无需外部组件
  - 可每位、每字节和每字访问（成对访问）
  - 可通过 P1、P2、P3 和 P4 端口从 LPM 唤醒，边沿可选
  - 所有端口上可编程上拉和下拉
- 代码安全性和加密
  - 128 位或 256 位 AES 安全加密和解密协处理器
  - 针对随机数生成算法的真随机种子
- 增强型串行通信
  - eUSCI_A0 和 eUSCI_A1 支持：
    - 支持自动波特率侦测的通用异步收发器 (UART)
    - IrDA 编码和解码
    - SPI
  - eUSCI_B0 和 eUSCI_B1 均支持：
    - 支持多从设备寻址的 $I^2C$
    - SPI
  - 硬件 UART 和 $I^2C$ 引导加载程序 (BSL)
- 灵活时钟系统
  - 具有 10 个可选厂家调整频率的定频数控振荡器 (DCO)
  - 低功率低频内部时钟源 (VLO)
  - 32kHz 晶振 (LFXT)
  - 高频晶振 (HFXT)
- 开发工具和软件
  - 自由的专业开发环境 具有 EnergyTrace++™技术
  - 实验和开发套件
- 系列产品成员
  - *器件比较* 总结了器件型号和可用封装类型
- 要获得完整的模块说明，请参见 *《MSP430FR58xx、MSP430FR59xx 和 MSP430FR6xx 系列用户指南》*

(1) 实时时钟 (RTC) 由 3.7pF 晶振计时。

## 1.2 应用

- 水表
- 热量计
- 热量分配表
- 便携式医疗仪表
- 数据日志
- 有关 TI Designs，请参阅 *扩展扫描接口 (ESI) 外设*

## 1.3 说明

MSP430™超低功耗 (ULP) FRAM 平台将独特的嵌入式 FRAM 和整体超低功耗系统架构组合在一起，从而使得创新人员能够以较少的能源预算增加性能。FRAM 技术以低很多的功耗将 SRAM 的速度、灵活性和耐久性与闪存的稳定性和可靠性组合在一起。

MSP430 ULP FRAM 产品系列由多种采用 FRAM 、ULP 16 位 MSP430 CPU 的器件和智能外设组成，可适用于各种 应用。ULP 架构具有七种低功耗模式，这些模式都经过优化，可在能源受限的应用中实现较长的 电池寿命。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸(2) |
|---|---|---|
| MSP430FR6989IPZ | LQFP (100) | 14mm x 14mm |
| MSP430FR6989IPN | LQFP (80) | 12mm x 12mm |
| MSP430FR5989IPM | LQFP (64) | 10mm x 10mm |
| MSP430FR5989IRGC | VQFN (64) | 9mm x 9mm |

(1) 要获得最新的产品、封装和订购信息，请参见*封装选项附录*（节 9），或者访问德州仪器 (TI) 网站 www.ti.com.cn。
(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见*机械数据*（节 9）。

## 1.4 功能方框图

图 1-1 和图 1-2 显示 功能方框图。

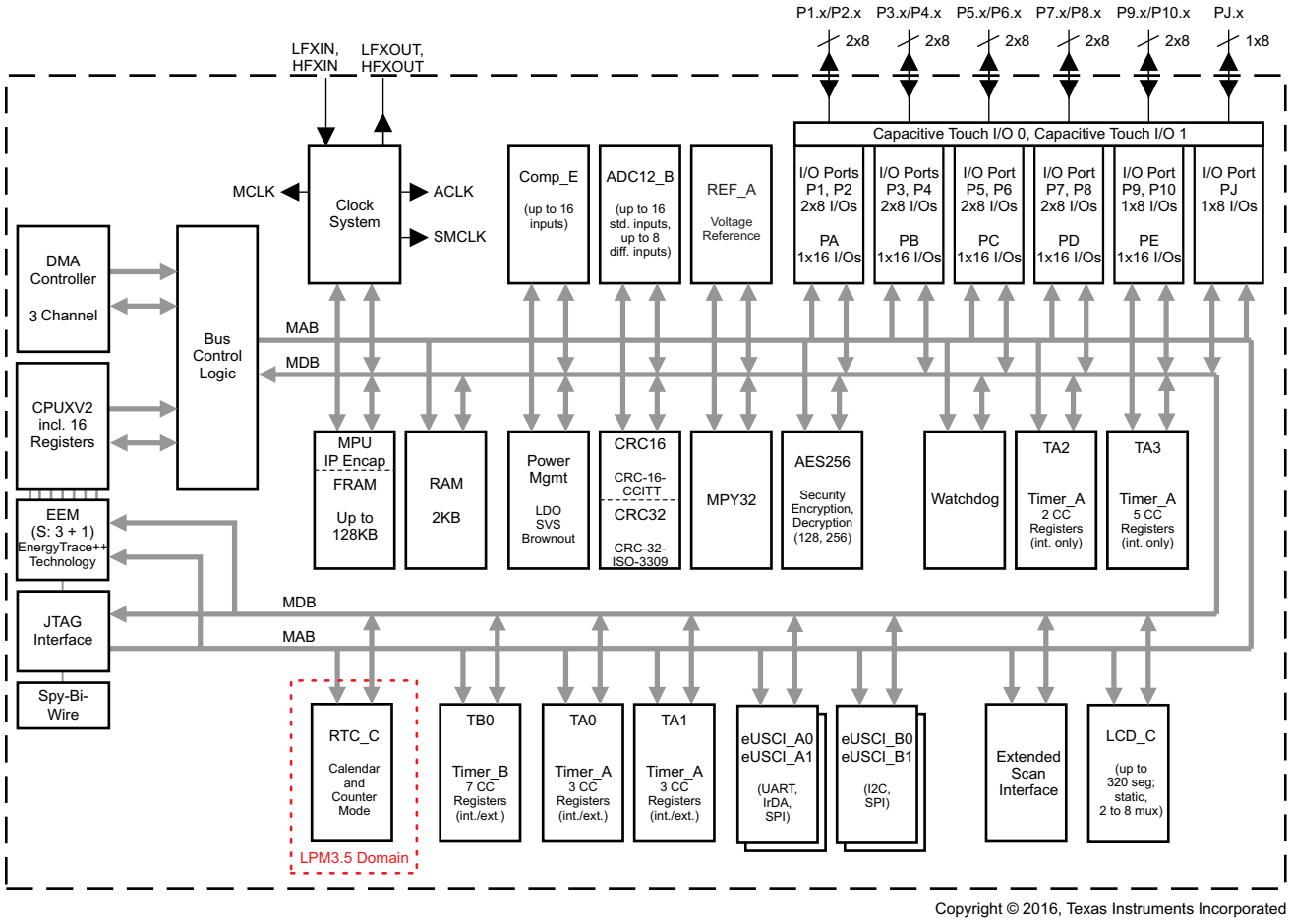



**图 1-1. 功能方框图 – MSP430FR698x、MSP430FR698x1**

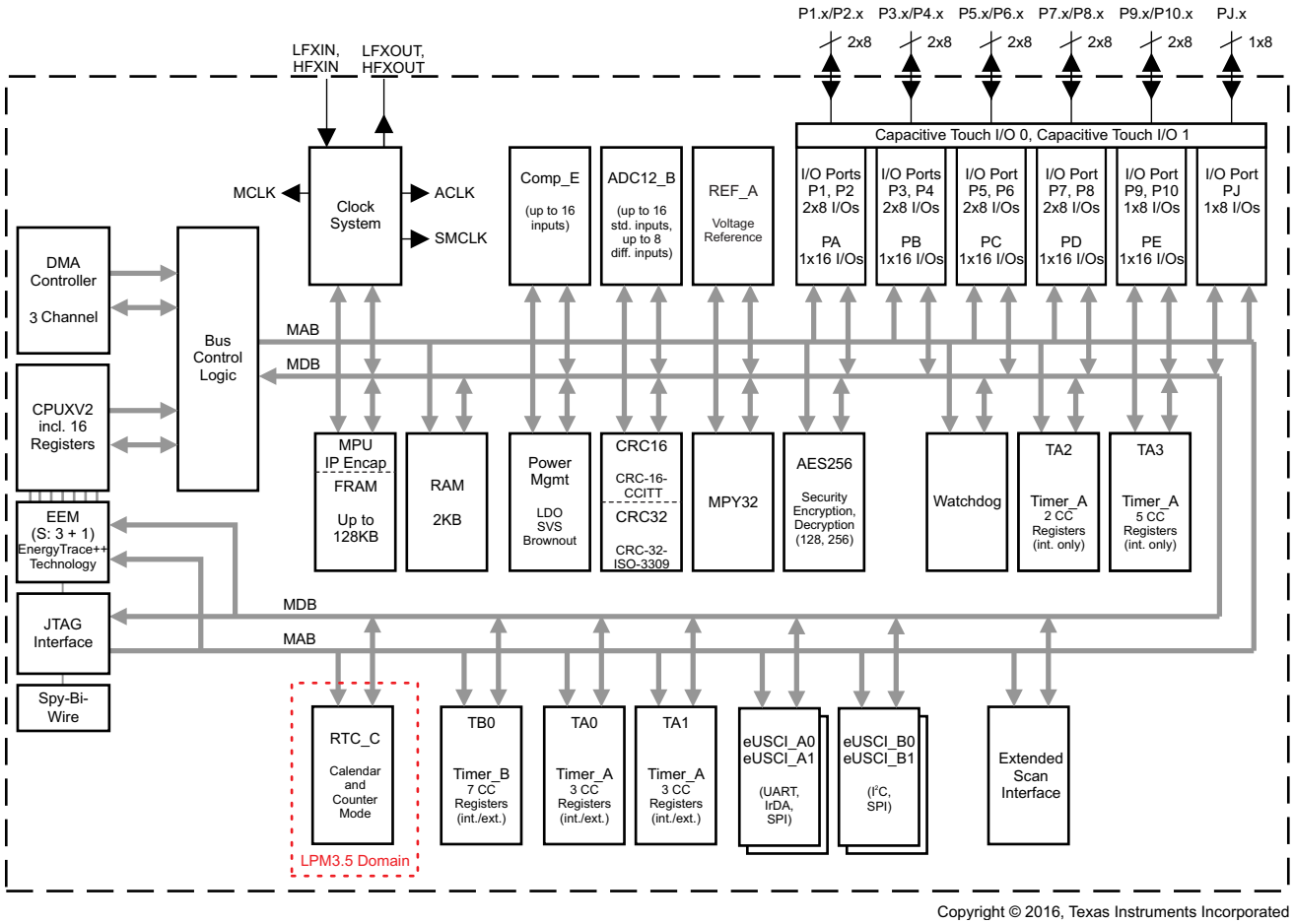





图 **1-2.** 功能方框图 **– MSP430FR598x、MSP430FR598x1**

# 内容

## 2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from March 10, 2017 to August 29, 2018** **Page**

- Updated Section 3.1, *Related Products* ..... 8
- Added note (1) to 表 5-2, *SVS*..... 40
- Changed capacitor value from 4.7 µF to 470 nF in 图 7-5, *ADC12_B Grounding and Noise Considerations* ..... 156
- Changed capacitor value from 4.7 µF to 470 nF in the last paragraph of 节 7.2.1.2, *Design Requirements* ..... 157
- 更新了 节 8.2，*器件命名规则* 中的文本和图 ..... 162

# 3 Device Comparison

Table 3-1 and Table 3-2 summarize the available family members.

**Table 3-1. Device Comparison (With UART BSL)(1) (2)**

| DEVICE | FRAM (KB) | SRAM (KB) | CLOCK SYSTEM | Timer_A (3) | Timer_B (4) | eUSCI | | AES | ADC12_B | LCD_C | I/O | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | A(5) | B(6) | | | | | |
| MSP430FR6989 | 128 | 2 | DCO **HFXT LFXT** | 3, 3 (7)<br>2, 5 (8) | 7 | 2 | 2 | yes | 12 ext<br>16 ext | 240 seg<br>320 seg | 63<br>83 | 80 PN<br>100 PZ |
| MSP430FR6988 | 96 | 2 | DCO **HFXT LFXT** | 3, 3 (7)<br>2, 5 (8) | 7 | 2 | 2 | yes | 12 ext<br>16 ext | 240 seg<br>320 seg | 63<br>83 | 80 PN<br>100 PZ |
| MSP430FR6987 | 64 | 2 | DCO **HFXT LFXT** | 3, 3 (7)<br>2, 5 (8) | 7 | 2 | 2 | yes | 12 ext<br>16 ext | 240 seg<br>320 seg | 63<br>83 | 80 PN<br>100 PZ |
| MSP430FR5989 | 128 | 2 | DCO **HFXT LFXT** | 3, 3 (7)<br>2, 5 (8) | 7 | 2 | 2 | yes | 12 ext | N/A | 48 | 64 PM<br>64 RGC |
| MSP430FR5988 | 96 | 2 | DCO **HFXT LFXT** | 3, 3 (7)<br>2, 5 (8) | 7 | 2 | 2 | yes | 12 ext | N/A | 48 | 64 PM<br>64 RGC |
| MSP430FR5987 | 64 | 2 | DCO **HFXT LFXT** | 3, 3 (7)<br>2, 5 (8) | 7 | 2 | 2 | yes | 12 ext | N/A | 48 | 64 PM<br>64 RGC |
| MSP430FR5986 | 48 | 2 | DCO **HFXT LFXT** | 3, 3 (7)<br>2, 5 (8) | 7 | 2 | 2 | yes | 12 ext | N/A | 48 | 64 PM |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/package.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(5) eUSCI_A supports UART with automatic baud-rate detection, IrDA encode and decode, and SPI.
(6) eUSCI_B supports $I^2C$ with multiple slave addresses and SPI.
(7) Timer_A TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
(8) Timer_A TA2 and TA3 provide only internal capture/compare inputs and only internal PWM outputs (if any).

**Table 3-2. Device Comparison (With $I^2C$ BSL) (1) (2)**

| DEVICE | FRAM (KB) | SRAM (KB) | CLOCK SYSTEM | Timer_A (3) | Timer_B (4) | eUSCI | | AES | ADC12_B | LCD_C | I/O | PACKAGE TYPE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | A(5) | B(6) | | | | | |
| MSP430FR69891 | 128 | 2 | DCO **HFXT LFXT** | 3, 3 (7)<br>2, 5 (8) | 7 | 2 | 2 | yes | 12 ext<br>16 ext | 240 seg<br>320 seg | 63<br>83 | 80 PN<br>100 PZ |
| MSP430FR59891 | 128 | 2 | DCO **HFXT LFXT** | 3, 3 (7)<br>2, 5 (8) | 7 | 2 | 2 | yes | 12 ext | N/A | 48 | 64 PM<br>64 RGC |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/package.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(5) eUSCI_A supports UART with automatic baud-rate detection, IrDA encode and decode, and SPI.
(6) eUSCI_B supports $I^2C$ with multiple slave addresses and SPI.
(7) Timer_A TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
(8) Timer_A TA2 and TA3 provide only internal capture/compare inputs and only internal PWM outputs (if any).

## 3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

**TI 16-bit and 32-bit microcontrollers** High-performance, low-power solutions to enable the autonomous future

**Products for MSP430 ultra-low-power sensing and measurement microcontrollers** One platform. One ecosystem. Endless possibilities.

**Products for MSP430 ultrasonic and performance sensing microcontrollers** Ultra-low-power single-chip MCUs with integrated sensing peripherals

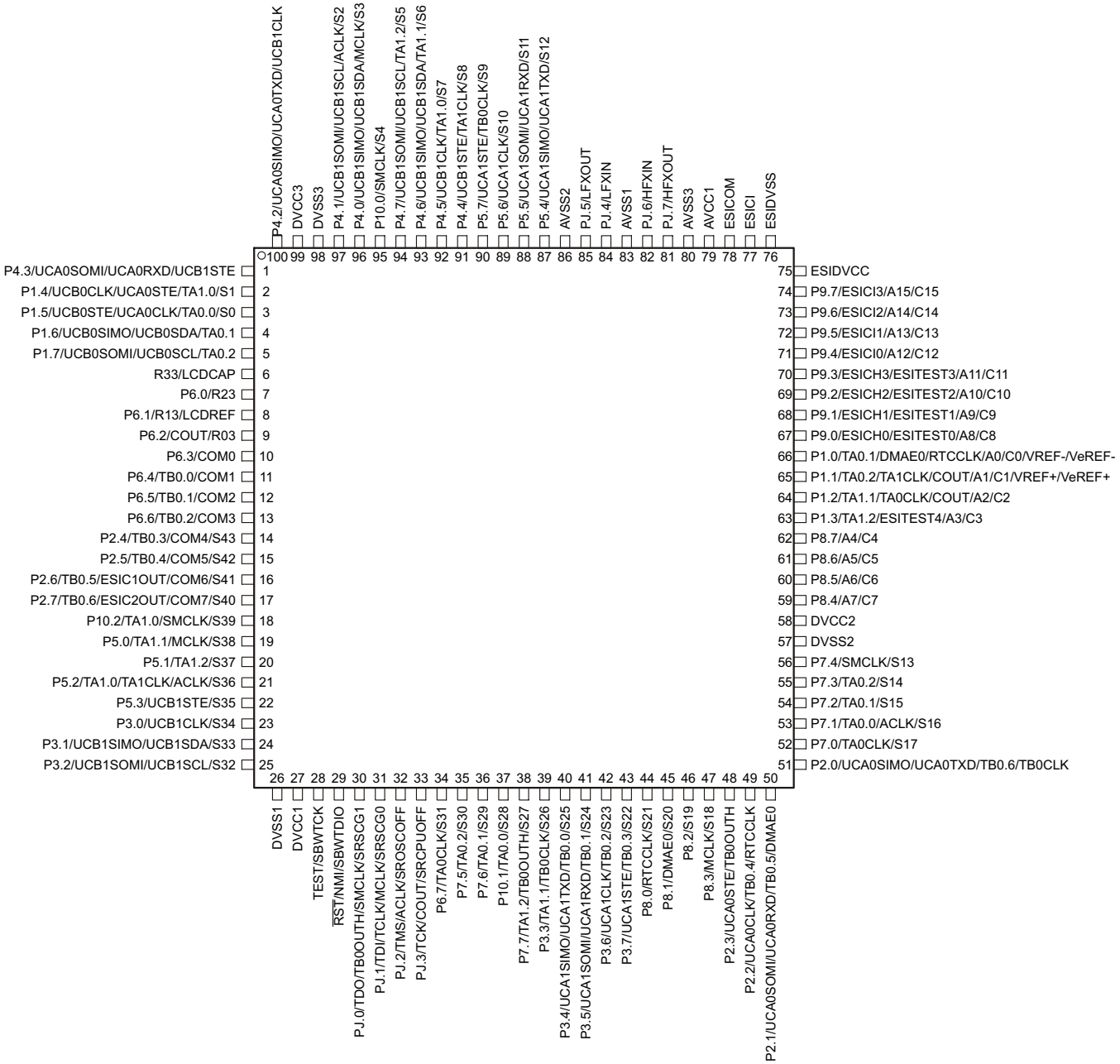
**Companion products for MSP430FR6989** Review products that are frequently purchased or used with this product.

**Reference designs for MSP430FR6989** The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

# 4 Terminal Configuration and Functions

## 4.1 Pin Diagrams

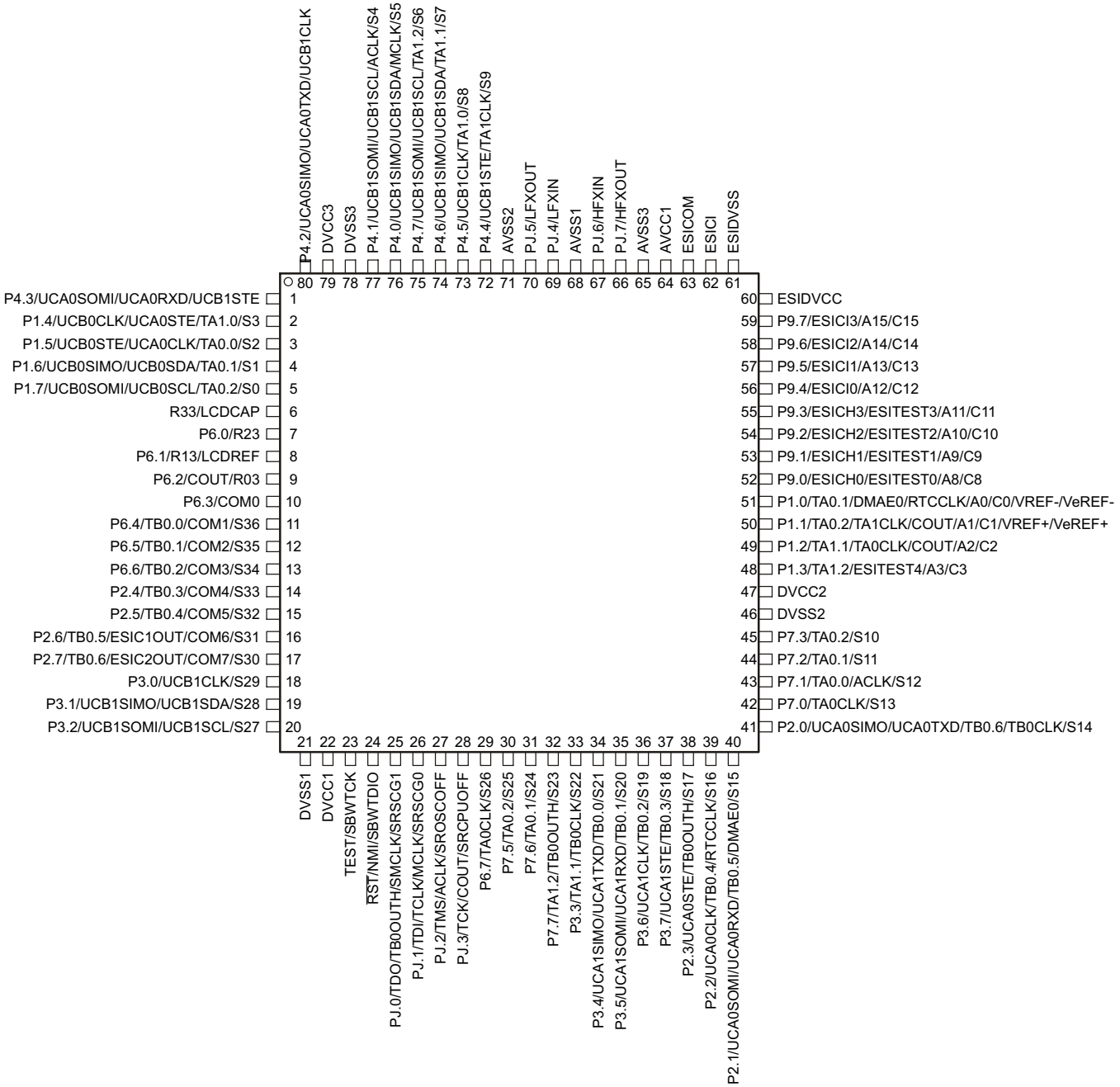
Figure 4-1 shows the pinout of the 100-pin PZ package for the MSP430FR698x and MSP430FR698x1 MCUs.




NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX
NOTE: On devices with I$^2$C BSL: P1.6: BSLSDA; P1.7: BSLSCL

**Figure 4-1. 100-Pin PZ Package (Top View) – MSP430FR698x and MSP430FR698x1**

Figure 4-2 shows the pinout of the 80-pin PN package for the MSP430FR698x and MSP430FR698x1 MCUs.

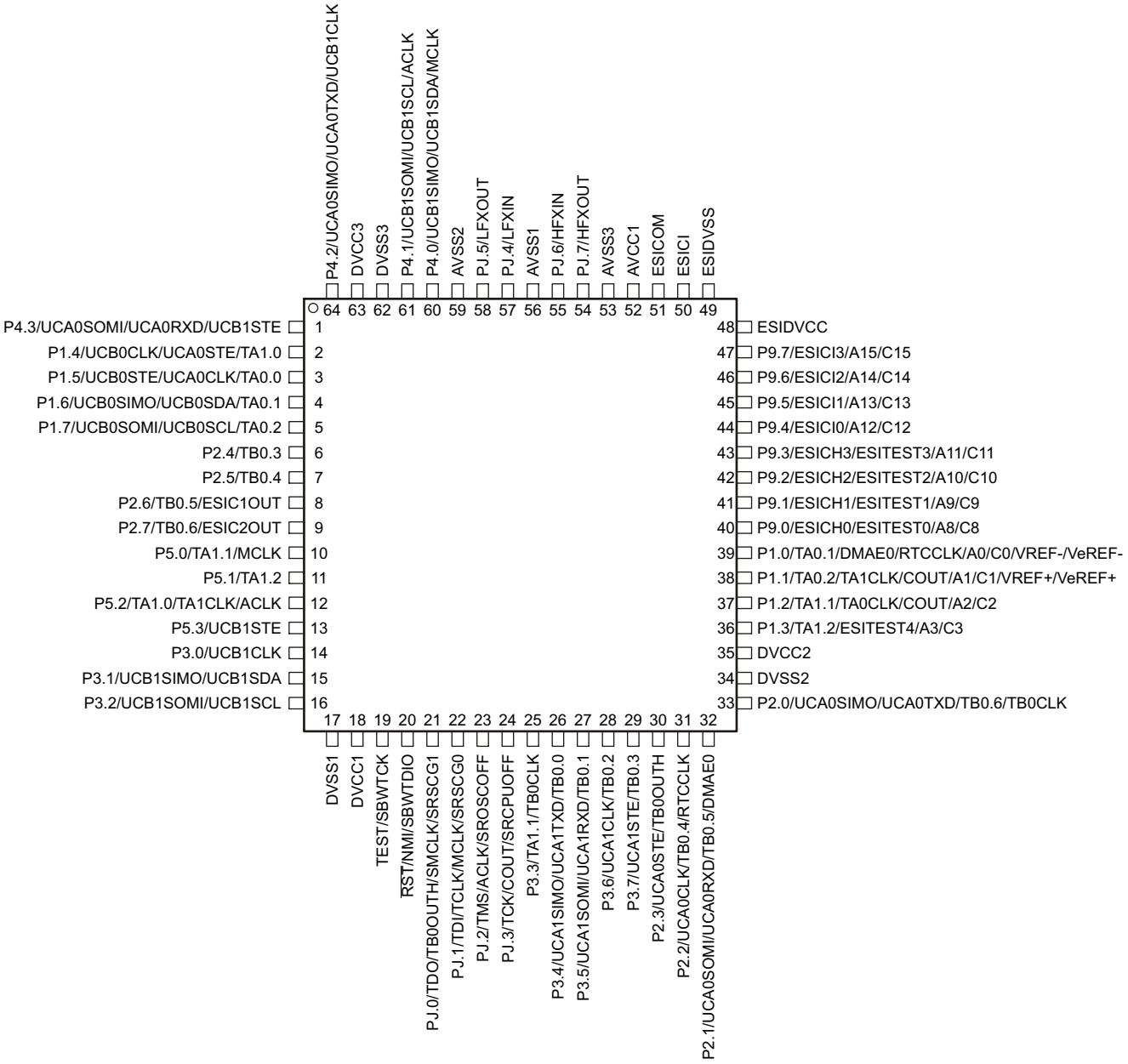



NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX

NOTE: On devices with $I^2C$ BSL: P1.6: BSLSDA; P1.7: BSLSCL

**Figure 4-2. 80-Pin PN Package (Top View) – MSP430FR698x and MSP430FR698x1**

Figure 4-3 shows the pinout of the 64-pin PM and RGC packages for the MSP430FR598x and MSP430FR598x1 MCUs.




NOTE: TI recommends connecting the RGC package pad to VSS.
NOTE: On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX
NOTE: On devices with $I^2C$ BSL: P1.6: BSLSDA; P1.7: BSLSCL

**Figure 4-3. 64-Pin PM or RGC Package (Top View) – MSP430FR598x and MSP430FR598x1**

## 4.2 Signal Descriptions

Table 4-1 and Table 4-2 describe the device signals.

**Table 4-1. Signal Descriptions – MSP430FR698x and MSP430FR698x1**

| TERMINAL | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PZ | | PN | | |
| | NO. | Seg. | NO. | Seg. | |
| P4.3/UCA0SOMI/UCA0RXD/ UCB1STE | 1 | | 1 | | General-purpose digital I/O<br>USCI_A0: Slave out, master in (SPI mode)<br>USCI_A0: Receive data (UART mode)<br>USCI_B1: Slave transmit enable (SPI mode) |
| P1.4/UCB0CLK/UCA0STE/ TA1.0/Sx | 2 | S1 | 2 | S3 | General-purpose digital I/O<br>USCI_B0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>USCI_A0: Slave transmit enable (SPI mode)<br>Timer_A TA1 CCR0 capture: CCI0A input, compare: Out0 output<br>LCD segment output (segment number is package specific) |
| P1.5/UCB0STE/ UCA0CLK/TA0.0/Sx | 3 | S0 | 3 | S2 | General-purpose digital I/O<br>USCI_B0: Slave transmit enable (SPI mode)<br>USCI_A0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>Timer_A TA0 CCR0 capture: CCI0A input, compare: Out0 output<br>LCD segment output (segment number is package specific) |
| P1.6/UCB0SIMO/UCB0SDA/ TA0.1/Sx | 4 | | 4 | S1 | General-purpose digital I/O<br>USCI_B0: Slave in, master out (SPI mode)<br>USCI_B0: $I^2C$ data ($I^2C$ mode)<br>BSL data ($I^2C$ BSL)<br>Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>LCD segment output (segment number is package specific) |
| P1.7/UCB0SOMI/UCB0SCL/ TA0.2/Sx | 5 | | 5 | S0 | General-purpose digital I/O<br>USCI_B0: Slave out, master in (SPI mode)<br>USCI_B0: $I^2C$ clock ($I^2C$ mode)<br>BSL clock ($I^2C$ BSL)<br>Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output<br>LCD segment output (segment number is package specific) |
| R33/LCDCAP | 6 | | 6 | | Input/output port of most positive analog LCD voltage (V1)<br>LCD capacitor connection |
| P6.0/R23 | 7 | | 7 | | General-purpose digital I/O<br>Input/output port of second most positive analog LCD voltage (V2) |
| P6.1/R13/LCDREF | 8 | | 8 | | General-purpose digital I/O<br>Input/output port of third most positive analog LCD voltage (V3 or V4)<br>External reference voltage input for regulated LCD voltage |
| P6.2/COUT/R03 | 9 | | 9 | | General-purpose digital I/O<br>Comparator output<br>Input/output port of lowest analog LCD voltage (V5) |

**Table 4-1. Signal Descriptions – MSP430FR698x and MSP430FR698x1 (continued)**

| TERMINAL | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PZ | | PN | | |
| | NO. | Seg. | NO. | Seg. | |
| P6.3/COM0 | 10 | | 10 | | General-purpose digital I/O<br>LCD common output COM0 for LCD backplane |
| P6.4/TB0.0/COM1/Sx | 11 | | 11 | S36 | General-purpose digital I/O<br>Timer_B TB0 CCR0 capture: CCI0B input, compare: Out0 output<br>LCD common output COM1 for LCD backplane<br>LCD segment output (segment number is package specific) |
| P6.5/TB0.1/COM2/Sx | 12 | | 12 | S35 | General-purpose digital I/O<br>Timer_B TB0 CCR1 capture: CCI1A input, compare: Out1 output<br>LCD common output COM2 for LCD backplane<br>LCD segment output (segment number is package specific) |
| P6.6/TB0.2/COM3/Sx | 13 | | 13 | S34 | General-purpose digital I/O<br>Timer_B TB0 CCR2 capture: CCI2A input, compare: Out2 output<br>LCD common output COM3 for LCD backplane<br>LCD segment output (segment number is package specific) |
| P2.4/TB0.3/COM4/Sx | 14 | S43 | 14 | S33 | General-purpose digital I/O<br>Timer_B TB0 CCR3 capture: CCI3A input, compare: Out3 output<br>LCD common output COM4 for LCD backplane<br>LCD segment output (segment number is package specific) |
| P2.5/TB0.4/COM5/Sx | 15 | S42 | 15 | S32 | General-purpose digital I/O<br>Timer_B TB0 CCR4 capture: CCI4A input, compare: Out4 output<br>LCD common output COM5 for LCD backplane<br>LCD segment output (segment number is package specific) |
| P2.6/TB0.5/ESIC1OUT/<br>COM6/Sx | 16 | S41 | 16 | S31 | General-purpose digital I/O<br>Timer_B TB0 CCR5 capture: CCI5A input, compare: Out5 output<br>ESI Comparator 1 output<br>LCD common output COM6 for LCD backplane<br>LCD segment output (segment number is package specific) |
| P2.7/TB0.6/ESIC2OUT/<br>COM7/Sx | 17 | S40 | 17 | S30 | General-purpose digital I/O<br>Timer_B TB0 CCR6 capture: CCI6A input, compare: Out6 output<br>ESI comparator 2 output<br>LCD common output COM7 for LCD backplane<br>LCD segment output (segment number is package specific) |
| P10.2/TA1.0/SMCLK/Sx | 18 | S39 | | | General-purpose digital I/O<br>Timer_A TA1 CCR0 capture: CCI0B input, compare: Out0 output<br>SMCLK output<br>LCD segment output (segment number is package specific) |
| P5.0/TA1.1/MCLK/Sx | 19 | S38 | | | General-purpose digital I/O<br>Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output<br>MCLK output<br>LCD segment output (segment number is package specific) |

**Table 4-1. Signal Descriptions – MSP430FR698x and MSP430FR698x1 (continued)**

| TERMINAL | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PZ | | PN | | |
| | NO. | Seg. | NO. | Seg. | |
| P5.1/TA1.2/Sx | 20 | S37 | | | General-purpose digital I/O<br>Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output<br>LCD segment output (segment number is package specific) |
| P5.2/TA1.0/TA1CLK/ACLK/Sx | 21 | S36 | | | General-purpose digital I/O<br>Timer_A TA1 CCR0 capture: CCI0B input, compare: Out0 output<br>Timer_A TA1 clock signal TA0CLK input<br>ACLK output<br>LCD segment output (segment number is package specific) |
| P5.3/UCB1STE/Sx | 22 | S35 | | | General-purpose digital I/O<br>USCI_B1: Slave transmit enable (SPI mode)<br>LCD segment output (segment number is package specific) |
| P3.0/UCB1CLK/Sx | 23 | S34 | 18 | S29 | General-purpose digital I/O<br>USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>LCD segment output (segment number is package specific) |
| P3.1/UCB1SIMO/UCB1SDA/ Sx | 24 | S33 | 19 | S28 | General-purpose digital I/O<br>USCI_B1: Slave in, master out (SPI mode)<br>USCI_B1: $I^2C$ data ($I^2C$ mode)<br>LCD segment output (segment number is package specific) |
| P3.2/UCB1SOMI/UCB1SCL/ Sx | 25 | S32 | 20 | S27 | General-purpose digital I/O<br>USCI_B1: Slave out, master in (SPI mode)<br>USCI_B1: $I^2C$ clock ($I^2C$ mode)<br>LCD segment output (segment number is package specific) |
| DVSS1 | 26 | | 21 | | Digital ground supply |
| DVCC1 | 27 | | 22 | | Digital power supply |
| TEST/SBWTCK | 28 | | 23 | | Test mode pin - select digital I/O on JTAG pins<br>Spy-Bi-Wire input clock |
| $\overline{\text{RST}}$/NMI/SBWTDIO | 29 | | 24 | | Reset input, active low<br>Nonmaskable interrupt input<br>Spy-Bi-Wire data input/output |
| PJ.0/TDO/TB0OUTH/ SMCLK/SRSCG1 | 30 | | 25 | | General-purpose digital I/O<br>Test data output port<br>Switch all PWM outputs high impedance input - Timer_B TB0<br>SMCLK output<br>Low-power debug: CPU Status register SCG1 |
| PJ.1/TDI/TCLK/MCLK/ SRSCG0 | 31 | | 26 | | General-purpose digital I/O<br>Test data input or test clock input<br>MCLK output<br>Low-power debug: CPU Status register SCG0 |

**Table 4-1. Signal Descriptions – MSP430FR698x and MSP430FR698x1 (continued)**

| TERMINAL | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PZ | | PN | | |
| | NO. | Seg. | NO. | Seg. | |
| PJ.2/TMS/ACLK/SROSCOFF | 32 | | 27 | | General-purpose digital I/O<br>Test mode select<br>ACLK output<br>Low-power debug: CPU Status register OSCOFF |
| PJ.3/TCK/COUT/SRCPUOFF | 33 | | 28 | | General-purpose digital I/O<br>Test clock<br>Comparator output<br>Low-power debug: CPU Status register CPUOFF |
| P6.7/TA0CLK/Sx | 34 | S31 | 29 | S26 | General-purpose digital I/O<br>Timer_A TA0 clock signal TA0CLK input<br>LCD segment output (segment number is package specific) |
| P7.5/TA0.2/Sx | 35 | S30 | 30 | S25 | General-purpose digital I/O<br>Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output<br>LCD segment output (segment number is package specific) |
| P7.6/TA0.1/Sx | 36 | S29 | 31 | S24 | General-purpose digital I/O<br>Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>LCD segment output (segment number is package specific) |
| P10.1/TA0.0/Sx | 37 | S28 | | | General-purpose digital I/O<br>Timer_A TA0 CCR0 capture: CCI0B input, compare: Out0 output<br>LCD segment output (segment number is package specific) |
| P7.7/TA1.2/TB0OUTH/Sx | 38 | S27 | 32 | S23 | General-purpose digital I/O<br>Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output<br>Switch all PWM outputs high impedance input - Timer_B TB0<br>LCD segment output (segment number is package specific) |
| P3.3/TA1.1/TB0CLK/Sx | 39 | S26 | 33 | S22 | General-purpose digital I/O<br>Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output<br>Timer_B TB0 clock signal TB0CLK input<br>LCD segment output (segment number is package specific) |
| P3.4/UCA1SIMO/UCA1TXD/<br>TB0.0/Sx | 40 | S25 | 34 | S21 | General-purpose digital I/O<br>USCI_A1: Slave in, master out (SPI mode)<br>USCI_A1: Transmit data (UART mode)<br>Timer_B TB0 CCR0 capture: CCI0A input, compare: Out0 output<br>LCD segment output (segment number is package specific) |
| P3.5/UCA1SOMI/UCA1RXD/<br>TB0.1/Sx | 41 | S24 | 35 | S20 | General-purpose digital I/O<br>USCI_A1: Slave out, master in (SPI mode)<br>USCI_A1: Receive data (UART mode)<br>Timer_B TB0 CCR1 capture: CCI1A input, compare: Out1 output<br>LCD segment output (segment number is package specific) |

**Table 4-1. Signal Descriptions – MSP430FR698x and MSP430FR698x1 (continued)**

| TERMINAL | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PZ | | PN | | |
| | NO. | Seg. | NO. | Seg. | |
| P3.6/UCA1CLK/TB0.2/Sx | 42 | S23 | 36 | S19 | General-purpose digital I/O<br>USCI_A1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>Timer_B TB0 CCR2 capture: CCI2A input, compare: Out2 output<br>LCD segment output (segment number is package specific) |
| P3.7/UCA1STE/TB0.3/Sx | 43 | S22 | 37 | S18 | General-purpose digital I/O<br>USCI_A1: Slave transmit enable (SPI mode)<br>Timer_B TB0 CCR3 capture: CCI3B input, compare: Out3 output<br>LCD segment output (segment number is package specific) |
| P8.0/RTCCLK/Sx | 44 | S21 | | | General-purpose digital I/O<br>RTC clock output for calibration<br>LCD segment output (segment number is package specific) |
| P8.1/DMAE0/Sx | 45 | S20 | | | General-purpose digital I/O<br>DMA external trigger input<br>LCD segment output (segment number is package specific) |
| P8.2/Sx | 46 | S19 | | | General-purpose digital I/O<br>LCD segment output (segment number is package specific) |
| P8.3/MCLK/Sx | 47 | S18 | | | General-purpose digital I/O<br>MCLK output<br>LCD segment output (segment number is package specific) |
| P2.3/UCA0STE/TB0OUTH/Sx | 48 | | 38 | S17 | General-purpose digital I/O<br>USCI_A0: Slave transmit enable (SPI mode)<br>Switch all PWM outputs high impedance input - Timer_B TB0<br>LCD segment output (segment number is package specific) |
| P2.2/UCA0CLK/TB0.4/ RTCCLK/Sx | 49 | | 39 | S16 | General-purpose digital I/O<br>USCI_A0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>Timer_B TB0 CCR4 capture: CCI4B input, compare: Out4 output<br>RTC clock output for calibration<br>LCD segment output (segment number is package specific) |
| P2.1/UCA0SOMI/UCA0RXD/ TB0.5/DMAE0/Sx | 50 | | 40 | S15 | General-purpose digital I/O<br>USCI_A0: Slave out, master in (SPI mode)<br>USCI_A0: Receive data (UART mode)<br>BSL receive (UART BSL)<br>Timer_B TB0 CCR5 capture: CCI5B input, compare: Out5 output<br>DMA external trigger input<br>LCD segment output (segment number is package specific) |

**Table 4-1. Signal Descriptions – MSP430FR698x and MSP430FR698x1 (continued)**

| TERMINAL | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PZ | | PN | | |
| | NO. | Seg. | NO. | Seg. | |
| P2.0/UCA0SIMO/UCA0TXD/ TB0.6/TB0CLK/Sx | 51 | | 41 | S14 | General-purpose digital I/O<br>USCI_A0: Slave in, master out (SPI mode)<br>USCI_A0: Transmit data (UART mode)<br>BSL transmit (UART BSL)<br>Timer_B TB0 CCR6 capture: CCI6B input, compare: Out6 output<br>Timer_B TB0 clock signal TB0CLK input<br>LCD segment output (segment number is package specific) |
| P7.0/TA0CLK/Sx | 52 | S17 | 42 | S13 | General-purpose digital I/O<br>Timer_A TA0 clock signal TA0CLK input<br>LCD segment output (segment number is package specific) |
| P7.1/TA0.0/ACLK/Sx | 53 | S16 | 43 | S12 | General-purpose digital I/O<br>Timer_A TA0 CCR0 capture: CCI0B input, compare: Out0 output<br>ACLK output<br>LCD segment output (segment number is package specific) |
| P7.2/TA0.1/Sx | 54 | S15 | 44 | S11 | General-purpose digital I/O<br>Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>LCD segment output (segment number is package specific) |
| P7.3/TA0.2/Sx | 55 | S14 | 45 | S10 | General-purpose digital I/O<br>Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output<br>LCD segment output (segment number is package specific) |
| P7.4/SMCLK/Sx | 56 | S13 | | | General-purpose digital I/O<br>SMCLK output<br>LCD segment output (segment number is package specific) |
| DVSS2 | 57 | | 46 | | Digital ground supply |
| DVCC2 | 58 | | 47 | | Digital power supply |
| P8.4/A7/C7 | 59 | | | | General-purpose digital I/O<br>Analog input A7<br>Comparator input C7 |
| P8.5/A6/C6 | 60 | | | | General-purpose digital I/O<br>Analog input A6<br>Comparator input C6 |
| P8.6/A5/C5 | 61 | | | | General-purpose digital I/O<br>Analog input A5<br>Comparator input C5 |
| P8.7/A4/C4 | 62 | | | | General-purpose digital I/O<br>Analog input A4<br>Comparator input C4 |

**Table 4-1. Signal Descriptions – MSP430FR698x and MSP430FR698x1 (continued)**

| TERMINAL | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PZ | | PN | | |
| | NO. | Seg. | NO. | Seg. | |
| P1.3/ESITEST4/TA1.2/A3/C3 | 63 | | 48 | | General-purpose digital I/O<br>ESI test signal 4<br>Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output<br>Analog input A3<br>Comparator input C3 |
| P1.2/TA1.1/TA0CLK/ COUT/A2/C2 | 64 | | 49 | | General-purpose digital I/O<br>Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output<br>Timer_A TA0 clock signal TA0CLK input<br>Comparator output<br>Analog input A2<br>Comparator input C2 |
| P1.1/TA0.2/TA1CLK/ COUT/A1/C1/VREF+/VeREF+ | 65 | | 50 | | General-purpose digital I/O<br>Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output<br>Timer_A TA1 clock signal TA1CLK input<br>Comparator output<br>Analog input A1<br>Comparator input C1<br>Output of positive reference voltage<br>Input for an external positive reference voltage to the ADC |
| P1.0/TA0.1/DMAE0/ RTCCLK/A0/C0/ VREF-/VeREF- | 66 | | 51 | | General-purpose digital I/O<br>Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>DMA external trigger input<br>RTC clock output for calibration<br>Analog input A0<br>Comparator input C0<br>Output of negative reference voltage<br>Input for an external negative reference voltage to the ADC |
| P9.0/ESICH0/ESITEST0/ A8/C8 | 67 | | 52 | | General-purpose digital I/O<br>ESI channel 0 sensor excitation output and signal input<br>ESI test signal 0<br>Analog input A8<br>Comparator input C8 |
| P9.1/ESICH1/ESITEST1/ A9/C9 | 68 | | 53 | | General-purpose digital I/O<br>ESI channel 1 sensor excitation output and signal input<br>ESI test signal 1<br>Analog input A9<br>Comparator input C9 |
| P9.2/ESICH2/ESITEST2/ A10/C10 | 69 | | 54 | | General-purpose digital I/O<br>ESI channel 2 sensor excitation output and signal input<br>ESI test signal 2<br>Analog input A10; comparator input C10 |

**Table 4-1. Signal Descriptions – MSP430FR698x and MSP430FR698x1 (continued)**

| TERMINAL | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PZ | | PN | | |
| | NO. | Seg. | NO. | Seg. | |
| P9.3/ESICH3/ESITEST3/ A11/C11 | 70 | | 55 | | General-purpose digital I/O<br>ESI channel 3 sensor excitation output and signal input<br>ESI test signal 3<br>Analog input A11<br>Comparator input C11 |
| P9.4/ESICI0/A12/C12 | 71 | | 56 | | General-purpose digital I/O<br>ESI channel 0 signal input to comparator<br>Analog input A12<br>Comparator input C12 |
| P9.5/ESICI1/A13/C13 | 72 | | 57 | | General-purpose digital I/O<br>ESI channel 1 signal input to comparator<br>Analog input A13<br>Comparator input C13 |
| P9.6/ESICI2/A14/C14 | 73 | | 58 | | General-purpose digital I/O<br>ESI channel 2 signal input to comparator<br>Analog input A14<br>Comparator input C14 |
| P9.7/ESICI3/A15/C15 | 74 | | 59 | | General-purpose digital I/O<br>ESI channel 3 signal input to comparator<br>Analog input A15<br>Comparator input C15 |
| ESIDVCC | 75 | | 60 | | ESI power supply |
| ESIDVSS | 76 | | 61 | | ESI ground supply |
| ESICI | 77 | | 62 | | ESI Scan IF input to Comparator |
| ESICOM | 78 | | 63 | | ESI Common termination for Scan IF sensors |
| AVCC1 | 79 | | 64 | | Analog power supply |
| AVSS3 | 80 | | 65 | | Analog ground supply |
| PJ.7/HFXOUT | 81 | | 66 | | General-purpose digital I/O<br>Output terminal of crystal oscillator XT2 |
| PJ.6/HFXIN | 82 | | 67 | | General-purpose digital I/O<br>Input terminal for crystal oscillator XT2 |
| AVSS1 | 83 | | 68 | | Analog ground supply |
| PJ.4/LFXIN | 84 | | 69 | | General-purpose digital I/O<br>Input terminal for crystal oscillator XT1 |
| PJ.5/LFXOUT | 85 | | 70 | | General-purpose digital I/O<br>Output terminal of crystal oscillator XT1 |
| AVSS2 | 86 | | 71 | | Analog ground supply |
| P5.4/UCA1SIMO/UCA1TXD/Sx | 87 | S12 | | | General-purpose digital I/O<br>USCI_A1: Slave in, master out (SPI mode)<br>USCI_A1: Transmit data (UART mode)<br>LCD segment output (segment number is package specific) |

**Table 4-1. Signal Descriptions – MSP430FR698x and MSP430FR698x1 (continued)**

| TERMINAL | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PZ | | PN | | |
| | NO. | Seg. | NO. | Seg. | |
| P5.5/UCA1SOMI/UCA1RXD/ Sx | 88 | S11 | | | General-purpose digital I/O<br>USCI_A1: Slave out, master in (SPI mode)<br>USCI_A1: Receive data (UART mode)<br>LCD segment output (segment number is package specific) |
| P5.6/UCA1CLK/Sx | 89 | S10 | | | General-purpose digital I/O<br>USCI_A1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>LCD segment output (segment number is package specific) |
| P5.7/UCA1STE/TB0CLK/Sx | 90 | S9 | | | General-purpose digital I/O<br>USCI_A1: Slave transmit enable (SPI mode)<br>Timer_B TB0 clock signal TB0CLK input<br>LCD segment output (segment number is package specific) |
| P4.4/UCB1STE/TA1CLK/Sx | 91 | S8 | 72 | S9 | General-purpose digital I/O<br>USCI_B1: Slave transmit enable (SPI mode)<br>Timer_A TA1 clock signal TA1CLK input<br>LCD segment output (segment number is package specific) |
| P4.5/UCB1CLK/TA1.0/Sx | 92 | S7 | 73 | S8 | General-purpose digital I/O<br>USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>Timer_A TA1 CCR0 capture: CCI0A input, compare: Out0 output<br>LCD segment output (segment number is package specific) |
| P4.6/UCB1SIMO/UCB1SDA/ TA1.1/Sx | 93 | S6 | 74 | S7 | General-purpose digital I/O<br>USCI_B1: Slave in, master out (SPI mode)<br>USCI_B1: $I^2C$ data ($I^2C$ mode)<br>Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output<br>LCD segment output (segment number is package specific) |
| P4.7/UCB1SOMI/UCB1SCL/ TA1.2/Sx | 94 | S5 | 75 | S6 | General-purpose digital I/O<br>USCI_B1: Slave out, master in (SPI mode)<br>USCI_B1: $I^2C$ clock ($I^2C$ mode)<br>Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output<br>LCD segment output (segment number is package specific) |
| P10.0/SMCLK/Sx | 95 | S4 | | | General-purpose digital I/O<br>SMCLK output<br>LCD segment output (segment number is package specific) |
| P4.0/UCB1SIMO/UCB1SDA/ MCLK/Sx | 96 | S3 | 76 | S5 | General-purpose digital I/O<br>USCI_B1: Slave in, master out (SPI mode)<br>USCI_B1: $I^2C$ data ($I^2C$ mode)<br>MCLK output<br>LCD segment output (segment number is package specific) |

**Table 4-1. Signal Descriptions – MSP430FR698x and MSP430FR698x1 (continued)**

| TERMINAL | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PZ | | PN | | |
| | NO. | Seg. | NO. | Seg. | |
| P4.1/UCB1SOMI/UCB1SCL/ ACLK/Sx | 97 | S2 | 77 | S4 | General-purpose digital I/O<br>USCI_B1: Slave out, master in (SPI mode)<br>USCI_B1: $I^2C$ clock ($I^2C$ mode)<br>ACLK output<br>LCD segment output (segment number is package specific) |
| DVSS3 | 98 | | 78 | | Digital ground supply |
| DVCC3 | 99 | | 79 | | Digital power supply |
| P4.2/UCA0SIMO/UCA0TXD/ UCB1CLK | 100 | | 80 | | General-purpose digital I/O<br>USCI_A0: Slave in, master out (SPI mode)<br>USCI_A0: Transmit data (UART mode)<br>USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) |

**Table 4-2. Signal Descriptions – MSP430FR598x and MSP430FR598x1**

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | PM RGC NO. | |
| P4.3/UCA0SOMI/ UCA0RXD/UCB1STE | 1 | General-purpose digital I/O<br>USCI_A0: Slave out, master in (SPI mode), Receive data (UART mode)<br>USCI_B1: Slave transmit enable (SPI mode) |
| P1.4/UCB0CLK/ UCA0STE/TA1.0 | 2 | General-purpose digital I/O<br>USCI_B0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>USCI_A0: Slave transmit enable (SPI mode)<br>Timer_A TA1 CCR0 capture: CCI0A input, compare: Out0 output |
| P1.5/UCB0STE/ UCA0CLK/TA0.0 | 3 | General-purpose digital I/O<br>USCI_B0: Slave transmit enable (SPI mode)<br>USCI_A0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>Timer_A TA0 CCR0 capture: CCI0A input, compare: Out0 output |
| P1.6/UCB0SIMO/ UCB0SDA/TA0.1 | 4 | General-purpose digital I/O<br>USCI_B0: Slave in, master out (SPI mode), $I^2C$ data ($I^2C$ mode)<br>BSL Data ($I^2C$ BSL)<br>Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output |
| P1.7/UCB0SOMI/ UCB0SCL/TA0.2 | 5 | General-purpose digital I/O<br>USCI_B0: Slave out, master in (SPI mode), $I^2C$ clock ($I^2C$ mode)<br>BSL Clock ($I^2C$ BSL)<br>Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output |
| P2.4/TB0.3 | 6 | General-purpose digital I/O<br>Timer_B TB0 CCR3 capture: CCI3A input, compare: Out3 output |
| P2.5/TB0.4 | 7 | General-purpose digital I/O<br>Timer_B TB0 CCR4 capture: CCI4A input, compare: Out4 output |
| P2.6/TB0.5/ESIC1OUT | 8 | General-purpose digital I/O<br>Timer_B TB0 CCR5 capture: CCI5A input, compare: Out5 output<br>ESI Comparator 1 output |
| P2.7/TB0.6/ESIC2OUT | 9 | General-purpose digital I/O<br>Timer_B TB0 CCR6 capture: CCI6A input, compare: Out6 output<br>ESI Comparator 2 output |
| P5.0/TA1.1/MCLK | 10 | General-purpose digital I/O<br>Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output<br>MCLK output |
| P5.1/TA1.2 | 11 | General-purpose digital I/O<br>Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output |
| P5.2/TA1.0/TA1CLK/ACLK | 12 | General-purpose digital I/O<br>Timer_A TA1 CCR0 capture: CCI0B input, compare: Out0 output<br>Timer_A TA1 clock signal TA0CLK input<br>ACLK output |
| P5.3/UCB1STE | 13 | General-purpose digital I/O<br>USCI_B1: Slave transmit enable (SPI mode) |

**Table 4-2. Signal Descriptions – MSP430FR598x and MSP430FR598x1 (continued)**

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | PM RGC NO. | |
| P3.0/UCB1CLK | 14 | General-purpose digital I/O<br>USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) |
| P3.1/UCB1SIMO/UCB1SDA | 15 | General-purpose digital I/O<br>USCI_B1: Slave in, master out (SPI mode)<br>USCI_B1: $I^2C$ data ($I^2C$ mode) |
| P3.2/UCB1SOMI/UCB1SCL | 16 | General-purpose digital I/O<br>USCI_B1: Slave out, master in (SPI mode)<br>USCI_B1: $I^2C$ clock ($I^2C$ mode) |
| DVSS1 | 17 | Digital ground supply |
| DVCC1 | 18 | Digital power supply |
| TEST/SBWTCK | 19 | Test mode pin - select digital I/O on JTAG pins<br>Spy-Bi-Wire input clock |
| $\overline{\text{RST}}$/NMI/SBWTDIO | 20 | Reset input, active low<br>Nonmaskable interrupt input<br>Spy-Bi-Wire data input/output |
| PJ.0/TDO/TB0OUTH/<br>SMCLK/SRSCG1 | 21 | General-purpose digital I/O<br>Test data output port<br>Switch all PWM outputs high impedance input - Timer_B TB0<br>SMCLK output<br>Low-power debug: CPU Status register SCG1 |
| PJ.1/TDI/TCLK/MCLK/SRSCG0 | 22 | General-purpose digital I/O<br>Test data input or test clock input<br>MCLK output<br>Low-power debug: CPU Status register SCG0 |
| PJ.2/TMS/ACLK/SROSCOFF | 23 | General-purpose digital I/O<br>Test mode select<br>ACLK output<br>Low-power debug: CPU Status register OSCOFF |
| PJ.3/TCK/COUT/SRCPUOFF | 24 | General-purpose digital I/O<br>Test clock<br>Comparator output<br>Low-power debug: CPU Status register CPUOFF |
| P3.3/TA1.1/TB0CLK | 25 | General-purpose digital I/O<br>Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output<br>Timer_B TB0 clock signal TB0CLK input |
| P3.4/UCA1SIMO/UCA1TXD/TB0.0 | 26 | General-purpose digital I/O<br>USCI_A1: Slave in, master out (SPI mode)<br>USCI_A1: Transmit data (UART mode)<br>Timer_B TB0 CCR0 capture: CCI0A input, compare: Out0 output |

**Table 4-2. Signal Descriptions – MSP430FR598x and MSP430FR598x1 (continued)**

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | PM RGC NO. | |
| P3.5/UCA1SOMI/UCA1RXD/TB0.1 | 27 | General-purpose digital I/O<br>USCI_A1: Slave out, master in (SPI mode)<br>USCI_A1: Receive data (UART mode)<br>Timer_B TB0 CCR1 capture: CCI1A input, compare: Out1 output |
| P3.6/UCA1CLK/TB0.2 | 28 | General-purpose digital I/O<br>USCI_A1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>Timer_B TB0 CCR2 capture: CCI2A input, compare: Out2 output |
| P3.7/UCA1STE/TB0.3 | 29 | General-purpose digital I/O<br>USCI_A1: Slave transmit enable (SPI mode)<br>Timer_B TB0 CCR3 capture: CCI3B input, compare: Out3 output |
| P2.3/UCA0STE/TB0OUTH | 30 | General-purpose digital I/O<br>USCI_A0: Slave transmit enable (SPI mode)<br>Switch all PWM outputs high impedance input - Timer_B TB0 |
| P2.2/UCA0CLK/TB0.4/RTCCLK | 31 | General-purpose digital I/O<br>USCI_A0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)<br>Timer_B TB0 CCR4 capture: CCI4B input, compare: Out4 output<br>RTC clock output for calibration |
| P2.1/UCA0SOMI/UCA0RXD/TB0.5/ DMAE0 | 32 | General-purpose digital I/O<br>USCI_A0: Slave out, master in (SPI mode)<br>USCI_A0: Receive data (UART mode)<br>BSL receive (UART BSL)<br>Timer_B TB0 CCR5 capture: CCI5B input, compare: Out5 output<br>DMA external trigger input |
| P2.0/UCA0SIMO/UCA0TXD/TB0.6/ TB0CLK | 33 | General-purpose digital I/O<br>USCI_A0: Slave in, master out (SPI mode)<br>USCI_A0: Transmit data (UART mode)<br>BSL transmit (UART BSL)<br>Timer_B TB0 CCR6 capture: CCI6B input, compare: Out6 output<br>Timer_B TB0 clock signal TB0CLK input |
| DVSS2 | 34 | Digital ground supply |
| DVCC2 | 35 | Digital power supply |
| P1.3/ESITEST4/TA1.2/A3/C3 | 36 | General-purpose digital I/O<br>ESI test signal 4<br>Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output<br>Analog input A3<br>Comparator input C3 |

**Table 4-2. Signal Descriptions – MSP430FR598x and MSP430FR598x1 (continued)**

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | PM RGC NO. | |
| P1.2/TA1.1/TA0CLK/COUT/A2/C2 | 37 | General-purpose digital I/O<br>Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output<br>Timer_A TA0 clock signal TA0CLK input<br>Comparator output<br>Analog input A2<br>Comparator input C2 |
| P1.1/TA0.2/TA1CLK/ COUT/A1/C1/VREF+/ VeREF+ | 38 | General-purpose digital I/O<br>Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output<br>Timer_A TA1 clock signal TA1CLK input<br>Comparator output<br>Analog input A1<br>Comparator input C1<br>Output of positive reference voltage<br>Input for an external positive reference voltage to the ADC |
| P1.0/TA0.1/DMAE0/ RTCCLK/A0/C0/ VREF-/VeREF- | 39 | General-purpose digital I/O<br>Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>DMA external trigger input<br>RTC clock output for calibration<br>Analog input A0<br>Comparator input C0<br>Output of negative reference voltage<br>Input for an external negative reference voltage to the ADC |
| P9.0/ESICH0/ESITEST0/ A8/C8 | 40 | General-purpose digital I/O<br>ESI channel 0 sensor excitation output and signal input<br>ESI test signal 0<br>Analog input A8; comparator input C8 |
| P9.1/ESICH1/ESITEST1/ A9/C9 | 41 | General-purpose digital I/O<br>ESI channel 1 sensor excitation output and signal input<br>ESI test signal 1<br>Analog input A9<br>Comparator input C9 |
| P9.2/ESICH2/ESITEST2/ A10/C10 | 42 | General-purpose digital I/O<br>ESI channel 2 sensor excitation output and signal input<br>ESI test signal 2<br>Analog input A10<br>Comparator input C10 |

**Table 4-2. Signal Descriptions – MSP430FR598x and MSP430FR598x1 (continued)**

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | PM RGC NO. | |
| P9.3/ESICH3/ESITEST3/ A11/C11 | 43 | General-purpose digital I/O<br>ESI channel 3 sensor excitation output and signal input<br>ESI test signal 3<br>Analog input A11<br>Comparator input C11 |
| P9.4/ESICI0/A12/C12 | 44 | General-purpose digital I/O<br>ESI channel 0 signal input to comparator<br>Analog input A12<br>Comparator input C12 |
| P9.5/ESICI1/A13/C13 | 45 | General-purpose digital I/O<br>ESI channel 1 signal input to comparator<br>Analog input A13<br>Comparator input C13 |
| P9.6/ESICI2/A14/C14 | 46 | General-purpose digital I/O<br>ESI channel 2 signal input to comparator<br>Analog input A14<br>Comparator input C14 |
| P9.7/ESICI3/A15/C15 | 47 | General-purpose digital I/O<br>ESI channel 3 signal input to comparator<br>Analog input A15<br>Comparator input C15 |
| ESIDVCC | 48 | ESI Power supply |
| ESIDVSS | 49 | ESI Ground supply |
| ESICI | 50 | ESI Scan IF input to Comparator |
| ESICOM | 51 | ESI Common termination for Scan IF sensors |
| AVCC1 | 52 | Analog power supply |
| AVSS3 | 53 | Analog ground supply |
| PJ.7/HFXOUT | 54 | General-purpose digital I/O<br>Output terminal of crystal oscillator XT2 |
| PJ.6/HFXIN | 55 | General-purpose digital I/O<br>Input terminal for crystal oscillator XT2 |
| AVSS1 | 56 | Analog ground supply |
| PJ.4/LFXIN | 57 | General-purpose digital I/O<br>Input terminal for crystal oscillator XT1 |
| PJ.5/LFXOUT | 58 | General-purpose digital I/O<br>Output terminal of crystal oscillator XT1 |
| AVSS2 | 59 | Analog ground supply |
| P4.0/UCB1SIMO/UCB1SDA/MCLK | 60 | General-purpose digital I/O<br>USCI_B1: Slave in, master out (SPI mode)<br>USCI_B1: $I^2C$ data ($I^2C$ mode)<br>MCLK output |

**Table 4-2. Signal Descriptions – MSP430FR598x and MSP430FR598x1 (continued)**

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | PM RGC NO. | |
| P4.1/UCB1SOMI/UCB1SCL/ACLK | 61 | General-purpose digital I/O<br>USCI_B1: Slave out, master in (SPI mode)<br>USCI_B1: $I^2C$ clock ($I^2C$ mode)<br>ACLK output |
| DVSS3 | 62 | Digital ground supply |
| DVCC3 | 63 | Digital power supply |
| P4.2/UCA0SIMO/UCA0TXD/ UCB1CLK | 64 | General-purpose digital I/O<br>USCI_A0: Slave in, master out (SPI mode)<br>USCI_A0: Transmit data (UART mode)<br>USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode) |
| Thermal pad | Pad | RGC package only. QFN package exposed thermal pad. TI recommends connection to $V_{SS}$. |

## 4.3 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see 节 6.11.24.

## 4.4 Connection of Unused Pins

Table 4-3 lists the correct termination of all unused pins.

**Table 4-3. Connection of Unused Pins(1)**

| PIN | POTENTIAL | COMMENT |
|---|---|---|
| AVCC | $DV_{CC}$ | |
| AVSS | $DV_{SS}$ | |
| Px.0 to Px.7 | Open | Set to port function, output direction (PxDIR.n = 1) |
| R33/LCDCAP | $DV_{SS}$ or $DV_{CC}$ | If the pin is not used, it can be tied to either supply. |
| ESIDVCC | $DV_{CC}$ | |
| ESIDVSS | $DV_{SS}$ | |
| ESICOM | Open | |
| ESICI | Open | |
| $\overline{RST}$/NMI | $DV_{CC}$ or $V_{CC}$ | 47-kΩ pullup or internal pullup selected with 2.2-nF (10-nF(2)) pulldown |
| PJ.0/TDO<br>PJ.1/TDI<br>PJ.2/TMS<br>PJ.3/TCK | Open | The JTAG pins are shared with general-purpose I/O function (PJ.x). If not used as JTAG pins, these pins should be switched to port function, output direction. When used as JTAG pins, these pins should remain open. |
| TEST | Open | This pin always has an internal pulldown enabled. |

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
(2) The pulldown capacitor should not exceed 2.2 nF when using devices in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers. If JTAG or Spy-Bi-Wire access is not needed, up to a 10-nF pulldown capacitor may be used.

# 5 Specifications

## 5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Voltage applied at DVCC and AVCC pins to $V_{SS}$ | –0.3 | 4.1 | V |
| Voltage difference between DVCC and AVCC pins(2) | | ±0.3 | V |
| Voltage applied to any pin (3) | –0.3 | $V_{CC}$ + 0.3 V (4.1 Max) | V |
| Diode current at any device pin | | ±2 | mA |
| Storage temperature, $T_{stg}$(4) | –40 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage differences between DVCC and AVCC exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
(3) All voltages referenced to $V_{SS}$.
(4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

## 5.3 Recommended Operating Conditions

Typical data are based on $V_{CC}$ = 3.0 V, $T_A$ = 25°C unless otherwise noted.

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range applied at all DVCC, AVCC, and ESIDVCC pins(1) (2) (3) | | 1.8(4) | | 3.6 | V |
| $V_{SS}$ | Supply voltage applied at all DVSS, AVSS, and ESIDVSS pins | | | 0 | | V |
| $T_A$ | Operating free-air temperature | | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | | 85 | °C |
| $C_{DVCC}$ | Capacitor value at DVCC and ESIDVCC (5) | | $1_{-20\%}$ | | | µF |
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency)(6) | No FRAM wait states (NWAITSx = 0) | 0 | | 8(7) | MHz |
| | | With FRAM wait states (NWAITSx = 1)(8) | 0 | | 16(9) | |
| $f_{ACLK}$ | Maximum ACLK frequency | | | | 50 | kHz |
| $f_{SMCLK}$ | Maximum SMCLK frequency | | | | 16(9) | MHz |

(1) TI recommends powering the DVCC, AVCC, and ESIDVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between DVCC, AVCC, and ESIDVCC must not exceed the limits specified in *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
(2) See 表 5-1 for additional important information.
(3) Modules may have a different supply voltage range specification. See the specification of each module in this data sheet.
(4) The minimum supply voltage is defined by the supervisor SVS levels. See 表 5-2 for the exact values.
(5) Connect a low-ESR capacitor with at least the value specified and a maximum tolerance of 20% as close as possible to the DVCC and ESIDVCC pins.
(6) Modules may have a different maximum input clock specification. See the specification of each module in this data sheet.
(7) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted.
(8) Wait states only occur on actual FRAM accesses; that is, on FRAM cache misses. RAM and peripheral accesses are always executed without wait states.
(9) DCO settings and HF crystals with a typical value less than or equal to the specified MAX value are permitted. If a clock sources with a larger typical value is used, the clock must be divided in the clock system.

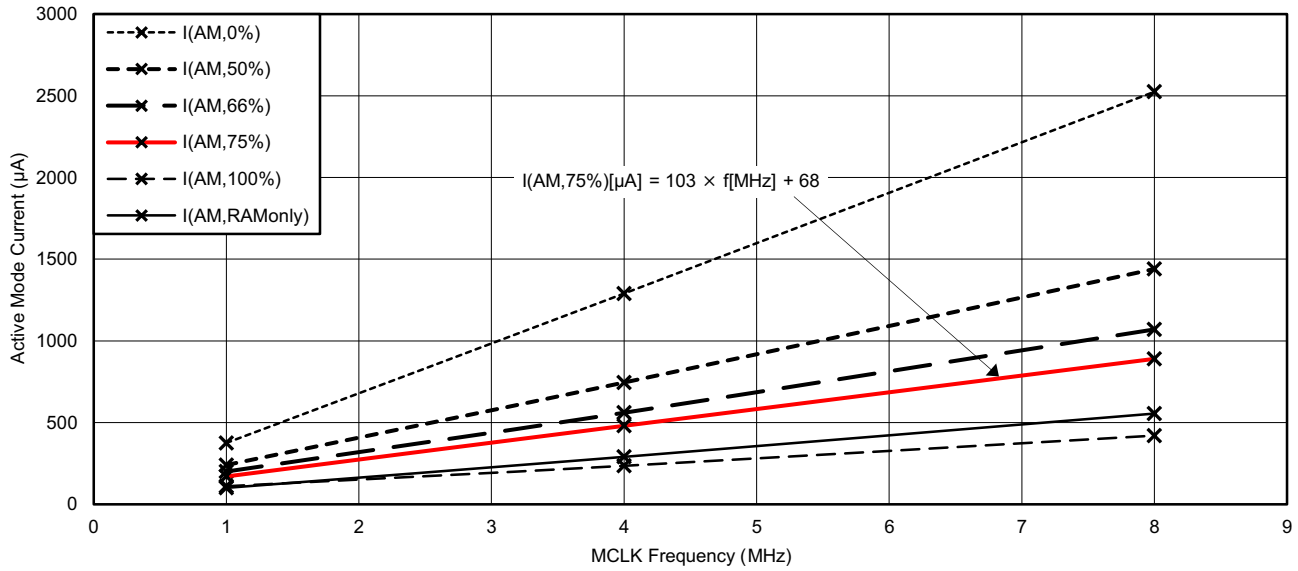
## 5.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2)

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | FREQUENCY ($f_{MCLK} = f_{SMCLK}$) | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 MHz 0 WAIT STATES (NWAITSx = 0) | | 4 MHz 0 WAIT STATES (NWAITSx = 0) | | 8 MHz 0 WAIT STATES (NWAITSx = 0) | | 12 MHz 1 WAIT STATE (NWAITSx = 1) | | 16 MHz 1 WAIT STATE (NWAITSx = 1) | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM,\ FRAM\_UNI}$ (Unified memory)(3) | FRAM | 3.0 V | 210 | | 640 | | 1220 | | 1475 | | 1845 | | µA |
| $I_{AM,\ FRAM}$(0%)(4) (5) | FRAM 0% cache hit ratio | 3.0 V | 375 | | 1290 | | 2525 | | 2100 | | 2675 | | µA |
| $I_{AM,\ FRAM}$(50%)(4) (5) | FRAM 50% cache hit ratio | 3.0 V | 240 | | 745 | | 1440 | | 1575 | | 1990 | | µA |
| $I_{AM,\ FRAM}$(66%)(4) (5) | FRAM 66% cache hit ratio | 3.0 V | 200 | | 560 | | 1070 | | 1300 | | 1620 | | µA |
| $I_{AM,\ FRAM}$(75%)(4) (5) | FRAM 75% cache hit ratio | 3.0 V | 170 | 255 | 480 | | 890 | 1085 | 1155 | 1310 | 1420 | 1620 | µA |
| $I_{AM,\ FRAM}$(100%(4) (5) | FRAM 100% cache hit ratio | 3.0 V | 110 | | 235 | | 420 | | 640 | | 730 | | µA |
| $I_{AM,\ RAM}$ (6) (5) | RAM | 3.0 V | 130 | | 320 | | 585 | | 890 | | 1070 | | µA |
| $I_{AM,\ RAM\ only}$ (7) (5) | RAM | 3.0 V | 100 | 180 | 290 | | 555 | | 860 | | 1040 | 1300 | µA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) Characterized with program executing typical data processing.
$f_{ACLK}$ = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency, except for 12 MHz. For 12 MHz, $f_{DCO}$ = 24 MHz and $f_{MCLK} = f_{SMCLK} = f_{DCO} / 2$.
At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency ($f_{MCLK,eff}$) decreases. The effective MCLK frequency also depends on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio.
The following equation can be used to compute $f_{MCLK,eff}$:
$f_{MCLK,eff} = f_{MCLK} / [\text{wait states} \times (1 - \text{cache hit ratio}) + 1]$
For example, with 1 wait state and 75% cache hit ratio $f_{MCKL,eff} = f_{MCLK} / [1 \times (1 - 0.75) + 1] = f_{MCLK} / 1.25$.
(3) Represents typical program execution. Program and data reside entirely in FRAM. All execution is from FRAM.
(4) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.
(5) See Figure 5-1 for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in Section 5.4.
(6) Program and data reside entirely in RAM. All execution is from RAM.
(7) Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

## 5.5 Typical Characteristics, Active Mode Supply Currents




I(AM, cache hit ratio): Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.
I(AM, RAMonly): Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

**Figure 5-1. Typical Active Mode Supply Currents, No Wait States**

## 5.6 Low-Power Mode (LPM0, LPM1) Supply Currents Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2)

| PARAMETER | $V_{CC}$ | FREQUENCY ($f_{SMCLK}$) | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 MHz | | 4 MHz | | 8 MHz | | 12 MHz | | 16 MHz | | |
| | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0}$ | 2.2 V | 75 | | 105 | | 165 | | 250 | | 230 | | µA |
| | 3.0 V | 85 | 120 | 115 | | 175 | | 260 | | 240 | 275 | |
| $I_{LPM1}$ | 2.2 V | 40 | | 65 | | 130 | | 215 | | 195 | | µA |
| | 3.0 V | 40 | 65 | 65 | | 130 | | 215 | | 195 | 220 | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
$f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ at specified frequency, except for 12 MHz: here $f_{DCO}$ = 24 MHz and $f_{SMCLK}$ = $f_{DCO}$ / 2.

## 5.7 Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | $V_{CC}$ | TEMPERATURE ($T_A$) | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | −40°C | | 25°C | | 60°C | | 85°C | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM2,XT12}$ | Low-power mode 2, 12-pF crystal (2) (3) (4) | 2.2 V | 0.6 | | 1.2 | | 3.1 | | 8.8 | | µA |
| | | 3.0 V | 0.6 | | 1.2 | 2.2 | 3.1 | | 8.8 | 20.8 | |
| $I_{LPM2,XT3.7}$ | Low-power mode 2, 3.7-pF crystal (2) (5) (4) | 2.2 V | 0.5 | | 1.1 | | 3.0 | | 8.7 | | µA |
| | | 3.0 V | 0.5 | | 1.1 | | 3.0 | | 8.7 | | |
| $I_{LPM2,VLO}$ | Low-power mode 2, VLO, includes SVS (6) | 2.2 V | 0.3 | | 0.9 | | 2.8 | | 8.5 | | µA |
| | | 3.0 V | 0.3 | | 0.9 | 2.0 | 2.8 | | 8.5 | 20.5 | |
| $I_{LPM3,XT12}$ | Low-power mode 3, 12-pF crystal, excludes SVS (2) (3) (7) | 2.2 V | 0.5 | | 0.7 | | 1.2 | | 2.5 | | µA |
| | | 3.0 V | 0.5 | | 0.7 | 1.0 | 1.2 | | 2.5 | 6.4 | |
| $I_{LPM3,XT3.7}$ | Low-power mode 3, 3.7-pF crystal, excludes SVS (2) (5) (8) (also see Figure 5-2) | 2.2 V | 0.4 | | 0.6 | | 1.1 | | 2.4 | | µA |
| | | 3.0 V | 0.4 | | 0.6 | | 1.1 | | 2.4 | | |
| $I_{LPM3,VLO}$ | Low-power mode 3, VLO, excludes SVS (9) | 2.2 V | 0.3 | | 0.4 | | 0.9 | | 2.2 | | µA |
| | | 3.0 V | 0.3 | | 0.4 | 0.8 | 0.9 | | 2.2 | 6.1 | |
| $I_{LPM3,VLO,RAMoff}$ | Low-power mode 3, VLO, excludes SVS, RAM powered-down completely (10) | 2.2 V | 0.3 | | 0.4 | | 0.8 | | 2.1 | | µA |
| | | 3.0 V | 0.3 | | 0.4 | 0.7 | 0.8 | | 2.1 | 5.2 | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF load.
(4) Low-power mode 2, crystal oscillator test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
(6) Low-power mode 2, VLO test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout and SVS included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),
$f_{XT1}$ = 0 Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(7) Low-power mode 3, 12-pF crystal excluding SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.
(8) Low-power mode 3, 3.7-pF crystal excluding SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.
(9) Low-power mode 3, VLO excluding SVS test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
$f_{XT1}$ = 0 Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.
(10) Low-power mode 3, VLO excluding SVS test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). RAM disabled (RCCTL0 = 5A55h). Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
$f_{XT1}$ = 0 Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

## Low-Power Mode (LPM2, LPM3, LPM4) Supply Currents (Into $V_{CC}$) Excluding External Current *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | $V_{CC}$ | TEMPERATURE ($T_A$) | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | –40°C | | 25°C | | 60°C | | 85°C | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM4,SVS}$ | Low-power mode 4, includes SVS(11) | 2.2 V | 0.4 | | 0.5 | | 0.9 | | 2.3 | | µA |
| | | 3.0 V | 0.4 | | 0.5 | 0.8 | 0.9 | | 2.3 | 6.2 | |
| $I_{LPM4}$ | Low-power mode 4, excludes SVS(12) | 2.2 V | 0.2 | | 0.3 | | 0.7 | | 2.0 | | µA |
| | | 3.0 V | 0.2 | | 0.3 | 0.6 | 0.7 | | 2.0 | 6.0 | |
| $I_{LPM4,RAMoff}$ | Low-power mode 4, excludes SVS, RAM powered-down completely(13) | 2.2 V | 0.2 | | 0.3 | | 0.7 | | 1.9 | | µA |
| | | 3.0 V | 0.2 | | 0.3 | 0.6 | 0.7 | | 1.9 | 5.1 | |
| $I_{IDLE,GroupA}$ | Additional idle current if one or more modules from Group A (see 表 6-3) are activated in LPM3 or LPM4 | 3.0V | | | 0.02 | | | | 0.3 | 1.2 | µA |
| $I_{IDLE,GroupB}$ | Additional idle current if one or more modules from Group B (see 表 6-3) are activated in LPM3 or LPM4 | 3.0V | | | 0.02 | | | | 0.3 | 1.2 | µA |
| $I_{IDLE,GroupC}$ | Additional idle current if one or more modules from Group C (see 表 6-3) are activated in LPM3 or LPM4 | 3.0V | | | 0.02 | | | | 0.38 | 1.5 | µA |
| $I_{IDLE,GroupD}$ | Additional idle current if one or more modules from Group D (see 表 6-3) are activated in LPM3 or LPM4 | 3.0V | | | 0.015 | | | | 0.25 | 1.0 | µA |

(11) Low-power mode 4 including SVS test conditions:
Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
$f_{XT1}$ = 0 Hz, $f_{ACLK}$ = 0 Hz, $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

(12) Low-power mode 4 excluding SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
$f_{XT1}$ = 0 Hz, $f_{ACLK}$ = 0 Hz, $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

(13) Low-power mode 4 excluding SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). RAM disabled (RCCTL0 = 5A55h).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
$f_{XT1}$ = 0 Hz, $f_{ACLK}$ = 0 Hz, $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. See the idle currents specified for the respective peripheral groups.

## 5.8 Low-Power Mode With LCD Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $V_{CC}$ | TEMPERATURE ($T_A$) | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | –40°C | | 25°C | | 60°C | | 85°C | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3,XT12}$ LCD, ext. bias | Low-power mode 3 (LPM3) current,12-pF crystal, LCD 4-mux mode, external biasing, excludes SVS(1) (2) | 3.0 V | 0.7 | | 0.9 | | 1.5 | | 3.1 | | µA |
| $I_{LPM3,XT12}$ LCD, int. bias | Low-power mode 3 (LPM3) current, 12-pF crystal, LCD 4-mux mode, internal biasing, charge pump disabled, excludes SVS(1) (3) | 3.0 V | 2.0 | | 2.2 | 2.9 | 2.8 | | 4.4 | 9.3 | µA |
| $I_{LPM3,XT12}$ LCD,CP | Low-power mode 3 (LPM3) current,12-pF crystal, LCD 4-mux mode, internal biasing, charge pump enabled, 1/3 bias, excludes SVS(1) (4) | 2.2 V | 5.0 | | 5.2 | | 5.8 | | 7.4 | | µA |
| | | 3.0 V | 4.5 | | 4.7 | | 5.3 | | 6.9 | | |

(1) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current - idle current of Group containing LCD module already included. See the idle currents specified for the respective peripheral groups.

(2) LCDMx = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD}$ = 32768 Hz / 32 / 4 = 256 Hz)
Current through external resistors not included (voltage levels are supplied by test equipment).
Even segments S0, S2, ... = 0, odd segments S1, S3, ... = 1. No LCD panel load.

(3) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD}$ = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ...=0, odd segments S1, S3, ... = 1. No LCD panel load.

(4) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 ($V_{LCD}$= 3 V typical), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD}$ = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ...=0, odd segments S1, S3, ... = 1. No LCD panel load. $C_{LCDCAP}$ = 10 µF

## 5.9 Low-Power Mode LPMx.5 Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | $V_{CC}$ | –40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3.5,XT12}$ | Low-power mode 3.5, 12-pF crystal including SVS(2) (3) (4) | 2.2 V | 0.4 | | 0.45 | | 0.55 | | 0.75 | | µA |
| | | 3.0 V | 0.4 | | 0.45 | 0.7 | 0.55 | | 0.75 | 1.6 | |
| $I_{LPM3.5,XT3.7}$ | Low-power mode 3.5, 3.7-pF crystal excluding SVS(2) (5) (6) | 2.2 V | 0.3 | | 0.35 | | 0.4 | | 0.65 | | µA |
| | | 3.0 V | 0.3 | | 0.35 | | 0.4 | | 0.65 | | |
| $I_{LPM4.5,SVS}$ | Low-power mode 4.5, including SVS(7) | 2.2 V | 0.2 | | 0.2 | | 0.25 | | 0.35 | | µA |
| | | 3.0 V | 0.2 | | 0.2 | 0.4 | 0.25 | | 0.35 | 0.7 | |
| $I_{LPM4.5}$ | Low-power mode 4.5, excluding SVS(8) | 2.2 V | 0.02 | | 0.02 | | 0.03 | | 0.14 | | µA |
| | | 3.0 V | 0.02 | | 0.02 | | 0.03 | | 0.13 | 0.5 | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF load.
(4) Low-power mode 3.5, 1-pF crystal including SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
(6) Low-power mode 3.5, 3.7-pF crystal excluding SVS test conditions:
Current for RTC clocked by XT1 included.Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(7) Low-power mode 4.5 including SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
$f_{XT1}$ = 0 Hz, $f_{ACLK}$ = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(8) Low-power mode 4.5 excluding SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
$f_{XT1}$ = 0 Hz, $f_{ACLK}$ = 0 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz

## 5.10 Typical Characteristics, Low-Power Mode Supply Currents

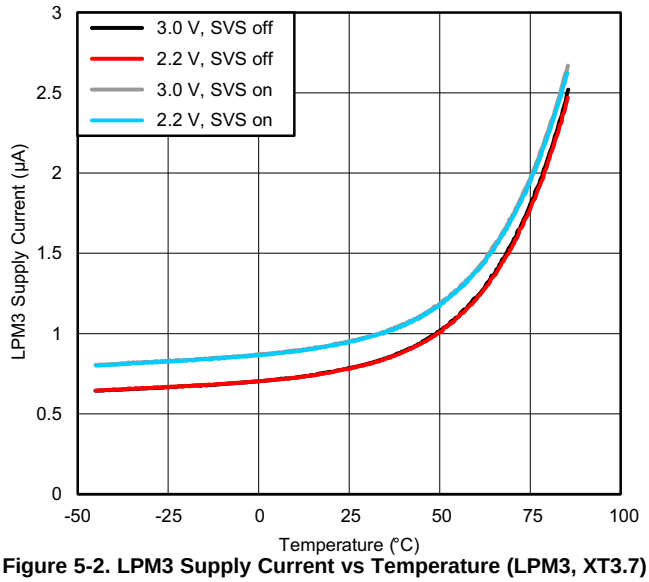



**Figure 5-2. LPM3 Supply Current vs Temperature (LPM3, XT3.7)**

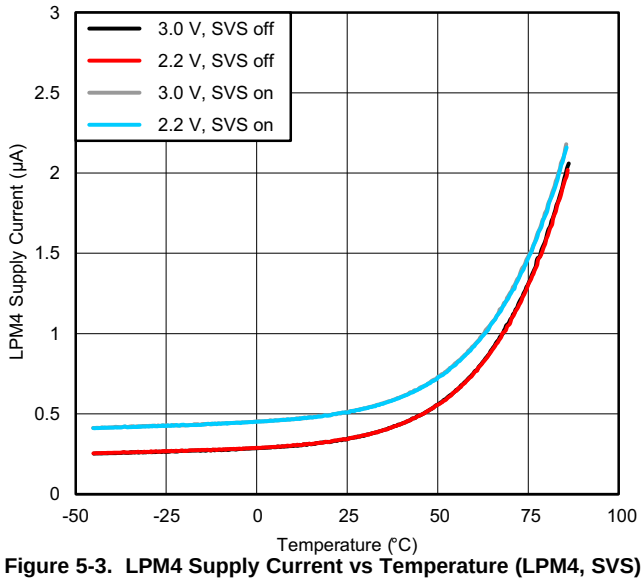



**Figure 5-3. LPM4 Supply Current vs Temperature (LPM4, SVS)**

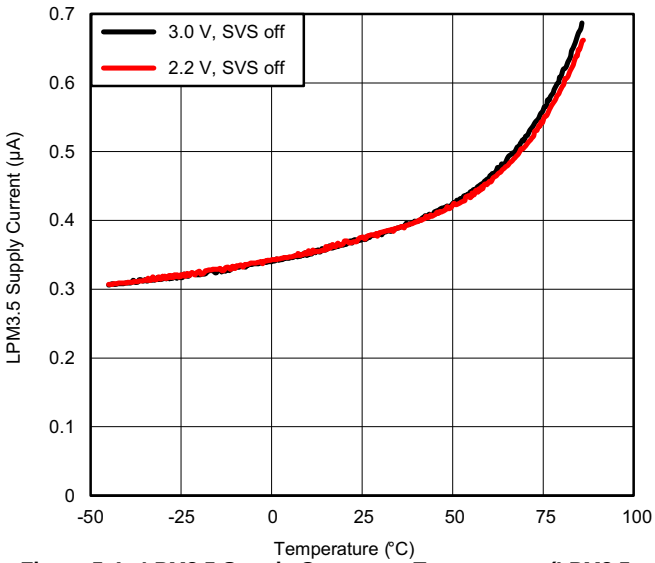



**Figure 5-4. LPM3.5 Supply Current vs Temperature (LPM3.5, XT3.7)**

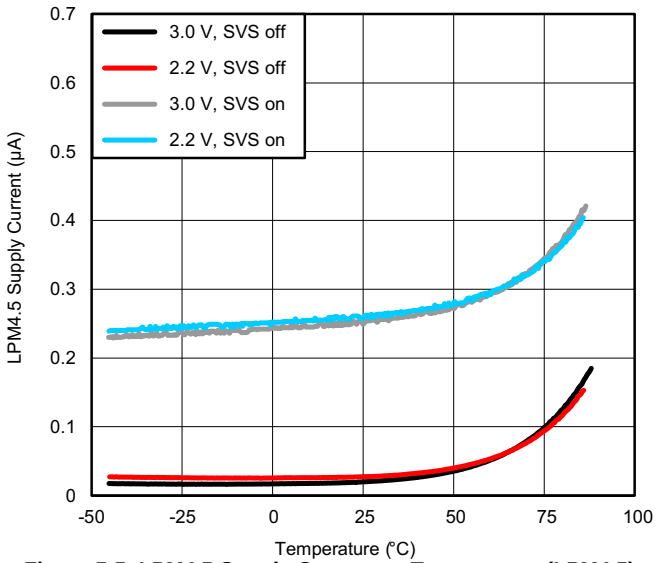



**Figure 5-5. LPM4.5 Supply Current vs Temperature (LPM4.5)**

## 5.11 Typical Characteristics, Current Consumption per Module(1)

| MODULE | TEST CONDITIONS | REFERENCE CLOCK | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Timer_A | | Module input clock | | 3 | | µA/MHz |
| Timer_B | | Module input clock | | 5 | | µA/MHz |
| eUSCI_A | UART mode | Module input clock | | 5.5 | | µA/MHz |
| eUSCI_A | SPI mode | Module input clock | | 3.5 | | µA/MHz |
| eUSCI_B | SPI mode | Module input clock | | 3.5 | | µA/MHz |
| eUSCI_B | $I^2C$ mode, 100 kbaud | Module input clock | | 3.5 | | µA/MHz |
| RTC_C | | 32 kHz | | 100 | | nA |
| MPY | Only from start to end of operation | MCLK | | 25 | | µA/MHz |
| AES | Only from start to end of operation | MCLK | | 21 | | µA/MHz |
| CRC16 | Only from start to end of operation | MCLK | | 2.5 | | µA/MHz |
| CRC32 | Only from start to end of operation | MCLK | | 2.5 | | µA/MHz |

(1) LCD_C: See Section 5.8. For other module currents not listed here, see the module-specific parameter sections.

## 5.12 Thermal Resistance Characteristics

| THERMAL METRIC[1] | | PACKAGE | VALUE[2] | UNIT |
|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance, still air[3] | LQFP-100 (PZ) | 49.8 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance[4] | | 9.7 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance[5] | | 26.0 | °C/W |
| $\Psi_{JB}$ | Junction-to-board thermal characterization parameter | | 25.7 | °C/W |
| $\Psi_{JT}$ | Junction-to-top thermal characterization parameter | | 0.2 | °C/W |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance[6] | | N/A | °C/W |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance, still air[3] | LQFP-80 (PN) | 49.5 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance[4] | | 14.7 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance[5] | | 24.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board thermal characterization parameter | | 23.8 | °C/W |
| $\Psi_{JT}$ | Junction-to-top thermal characterization parameter | | 0.7 | °C/W |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance[6] | | N/A | °C/W |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance, still air[3] | LQFP-64 (PM) | 55.3 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance[4] | | 16.8 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance[5] | | 26.8 | °C/W |
| $\Psi_{JB}$ | Junction-to-board thermal characterization parameter | | 26.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top thermal characterization parameter | | 0.8 | °C/W |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance[6] | | N/A | °C/W |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance, still air[3] | VQFN-64 (RGC) | 29.2 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance[4] | | 13.9 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance[5] | | 8.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board thermal characterization parameter | | 8.0 | °C/W |
| $\Psi_{JT}$ | Junction-to-top thermal characterization parameter | | 0.2 | °C/W |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance[6] | | 1.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) N/A = not applicable
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## 5.13 Timing and Switching Characteristics

### 5.13.1 Power Supply Sequencing

TI recommends powering the AVCC, DVCC, and ESIDVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC, DVCC, and ESIDVCC must not exceed the limits specified in *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

At power up, the device does not start executing code before the supply voltage reached $V_{SVSH+}$ if the supply rises monotonically to this level.

表 5-1 lists the power ramp requirements.

**表 5-1. Brownout and Device Reset Power Ramp Requirements**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{VCC\_BOR-}$ | Brownout power-down level(1)(2) | $\lvert dDV_{CC}/d_t \rvert$ < 3 V/s(3) | 0.7 | 1.66 | V |
| | | $\lvert dDV_{CC}/d_t \rvert$ > 300 V/s(3) | 0 | | |
| $V_{VCC\_BOR+}$ | Brownout power-up level(2) | $\lvert dDV_{CC}/d_t \rvert$ < 3 V/s(4) | 0.79 | 1.68 | V |

(1) In case of a supply voltage brownout, the device supply voltages must ramp down to the specified brownout power-down level ($V_{VCC\_BOR-}$) before the voltage is ramped up again to ensure a reliable device start-up and performance according to the data sheet including the correct operation of the on-chip SVS module.
(2) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond (±0.05 V/µs). Following the data sheet recommendation for capacitor $C_{DVCC}$ should limit the slopes accordingly.
(3) The brownout levels are measured with a slowly changing supply. With faster slopes, the MIN level required to reset the device properly can decrease to 0 V. Use the graph in 图 5-6 to estimate the $V_{VCC\_BOR-}$ level based on the down slope of the supply voltage. After removing $V_{CC}$, the down slope can be estimated based on the current consumption and the capacitance on DVCC: dV/dt = I/C where dV/dt = slope, I = current, C = capacitance.
(4) The brownout levels are measured with a slowly changing supply.

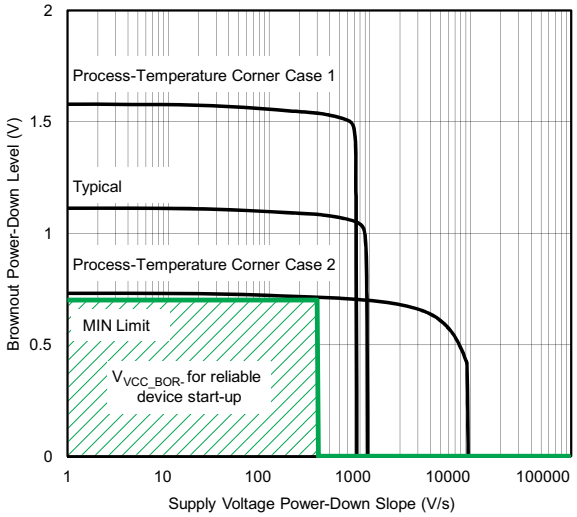



**图 5-6. Brownout Power-Down Level vs Supply Voltage Down Slope**

表 5-2 lists the characteristics of the SVS.

**表 5-2. SVS**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SVSH,LPM}$ | $SVS_H$ current consumption, low-power modes | | | 170 | 300 | nA |
| $V_{SVSH-}$ | $SVS_H$ power-down level(1) | | 1.75 | 1.80 | 1.85 | V |
| $V_{SVSH+}$ | $SVS_H$ power-up level(1) | | 1.77 | 1.88 | 1.99 | V |
| $V_{SVSH\_hys}$ | $SVS_H$ hysteresis | | 40 | | 120 | mV |
| $t_{PD,SVSH,\ AM}$ | $SVS_H$ propagation delay, active mode | $dV_{Vcc}/dt$ = –10 mV/µs | | | 10 | µs |

(1) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.

### 5.13.2 Reset Timing

Table 5-11 lists the input requirements for the $\overline{RST}$ signal.

**表 5-3. Reset Input**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{(RST)}$ | External reset pulse duration on $\overline{RST}$(1) | 2.2 V, 3.0 V | 2 | | µs |

(1) Not applicable if $\overline{RST}$/NMI pin configured as NMI.

### 5.13.3 Clock Specifications

Table 5-4 lists the characteristics of the LFXT.

**Table 5-4. Low-Frequency Crystal Oscillator, LFXT(1)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{VCC.LFXT}$ | Current consumption | $f_{OSC}$ = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, $T_A$ = 25°C, $C_{L,eff}$ = 3.7 pF, ESR ≈ 44 kΩ | 3.0 V | | 180 | | nA |
| | | $f_{OSC}$ = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {1}, $T_A$ = 25°C, $C_{L,eff}$ = 6 pF, ESR ≈ 40 kΩ | | | 185 | | |
| | | $f_{OSC}$ = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {2}, $T_A$ = 25°C, $C_{L,eff}$ = 9 pF, ESR ≈ 40 kΩ | | | 225 | | |
| | | $f_{OSC}$ = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 12.5 pF, ESR ≈ 40 kΩ | | | 330 | | |
| $f_{LFXT}$ | LFXT oscillator crystal frequency | LFXTBYPASS = 0 | | | 32768 | | Hz |
| $DC_{LFXT}$ | LFXT oscillator duty cycle | Measured at ACLK, $f_{LFXT}$ = 32768 Hz | | 30% | | 70% | |
| $f_{LFXT,SW}$ | LFXT oscillator logic-level square-wave input frequency | LFXTBYPASS = 1 (2) (3) | | 10.5 | 32.768 | 50 | kHz |
| $DC_{LFXT, SW}$ | LFXT oscillator logic-level square-wave input duty cycle | LFXTBYPASS = 1 | | 30% | | 70% | |
| $OA_{LFXT}$ | Oscillation allowance for LF crystals (4) | LFXTBYPASS = 0, LFXTDRIVE = {1}, $f_{LFXT}$ = 32768 Hz, $C_{L,eff}$ = 6 pF | | | 210 | | kΩ |
| | | LFXTBYPASS = 0, LFXTDRIVE = {3}, $f_{LFXT}$ = 32768 Hz, $C_{L,eff}$ = 12.5 pF | | | 300 | | |
| $C_{LFXIN}$ | Integrated load capacitance at LFXIN terminal (5) (6) | | | | 2 | | pF |
| $C_{LFXOUT}$ | Integrated load capacitance at LFXOUT terminal (5) (6) | | | | 2 | | pF |

(1) To improve EMI on the LFXT oscillator, observe the following guidelines.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins LFXIN and LFXOUT.
- Avoid running PCB traces underneath or adjacent to the LFXIN and LFXOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator LFXIN and LFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT, SW}$.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF.
- For LFXTDRIVE = {1}, $C_{L,eff}$ = 6 pF
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF
- For LFXTDRIVE = {3}, 9 pF ≤ $C_{L,eff}$ ≤ 12.5 pF

(5) This represents all the parasitic capacitance present at the LFXIN and LFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, $C_{L,eff}$ can be computed as $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$, where $C_{IN}$ and $C_{OUT}$ are the total capacitance at the LFXIN and LFXOUT terminals, respectively.

(6) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.

**Table 5-4. Low-Frequency Crystal Oscillator, LFXT(1) (continued)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{START,LFXT}$ | Start-up time(7) | $f_{OSC}$ = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, $T_A$ = 25°C, $C_{L,eff}$ = 3.7 pF | 3.0 V | | 800 | | ms |
| | | $f_{OSC}$ = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 12.5 pF | 3.0 V | | 1000 | | |
| $f_{Fault,LFXT}$ | Oscillator fault frequency(8) (9) | | | 0 | | 3500 | Hz |

(7) Includes start-up counter of 1024 clock cycles.
(8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition sets the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-5 lists the characteristics of the HFXT.

**Table 5-5. High-Frequency Crystal Oscillator, HFXT(1)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DVCC.HFXT}$ | HFXT oscillator crystal current HF mode at typical ESR | $f_{OSC}$ = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1(2) $T_A$ = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, $C_{shunt}$ | 3.0 V | | 75 | | µA |
| | | $f_{OSC}$ = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $T_A$ = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, $C_{shunt}$ | | | 120 | | |
| | | $f_{OSC}$ = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 2, HFFREQ = 2, $T_A$ = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, $C_{shunt}$ | | | 190 | | |
| | | $f_{OSC}$ = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, $T_A$ = 25°C, $C_{L,eff}$ = 18 pF, Typical ESR, $C_{shunt}$ | | | 250 | | |
| $f_{HFXT}$ | HFXT oscillator crystal frequency, crystal mode | HFXTBYPASS = 0, HFFREQ = 1(2)(3) | | 4 | | 8 | MHz |
| | | HFXTBYPASS = 0, HFFREQ = 2(3) | | 8.01 | | 16 | |
| | | HFXTBYPASS = 0, HFFREQ = 3(3) | | 16.01 | | 24 | |
| $DC_{HFXT}$ | HFXT oscillator duty cycle | Measured at SMCLK, $f_{HFXT}$ = 16 MHz | | 40% | 50% | 60% | |
| $f_{HFXT,SW}$ | HFXT oscillator logic-level square-wave input frequency, bypass mode | HFXTBYPASS = 1, HFFREQ = 0(4)(3) | | 0.9 | | 4 | MHz |
| | | HFXTBYPASS = 1, HFFREQ = 1(4)(3) | | 4.01 | | 8 | |
| | | HFXTBYPASS = 1, HFFREQ = 2(4)(3) | | 8.01 | | 16 | |
| | | HFXTBYPASS = 1, HFFREQ = 3(4)(3) | | 16.01 | | 24 | |
| $DC_{HFXT, SW}$ | HFXT oscillator logic-level square-wave input duty cycle | HFXTBYPASS = 1 | | 40% | | 60% | |

(1) To improve EMI on the HFXT oscillator, observe the following guidelines.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins HFXIN and HFXOUT.
- Avoid running PCB traces underneath or adjacent to the HFXIN and HFXOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator HFXIN and HFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) HFFREQ = {0} is not supported for HFXT crystal mode of operation.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{HFXT, SW}$.

**Table 5-5. High-Frequency Crystal Oscillator, HFXT(1) (continued)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{START,HFXT}$ | Start-up time(5) | $f_{OSC}$ = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | 3.0 V | | 1.6 | | ms |
| | | $f_{OSC}$ = 24 MHz , HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | 3.0 V | | 0.6 | | |
| $C_{HFXIN}$ | Integrated load capacitance at HFXIN terminal(6) (7) | | | | 2 | | pF |
| $C_{HFXOUT}$ | Integrated load capacitance at HFXOUT terminal(6) (7) | | | | 2 | | pF |
| $f_{Fault,HFXT}$ | Oscillator fault frequency(8) (9) | | | 0 | | 800 | kHz |

(5) Includes start-up counter of 1024 clock cycles.
(6) This represents all the parasitic capacitance present at the HFXIN and HFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, $C_{L,eff}$ can be computed as $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$, where $C_{IN}$ and $C_{OUT}$ are the total capacitance at the HFXIN and HFXOUT terminals, respectively.
(7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
(8) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX might set the flag. A static condition or stuck at fault condition set the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-6 lists the characteristics of the DCO.

**Table 5-6. DCO**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{DCO1}$ | DCO frequency range 1 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 0, DCORSEL = 1, DCOFSEL = 0 | | | 1 | ±3.5% | MHz |
| $f_{DCO2.7}$ | DCO frequency range 2.7 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 1 | | | 2.667 | ±3.5% | MHz |
| $f_{DCO3.5}$ | DCO frequency range 3.5 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 2 | | | 3.5 | ±3.5% | MHz |
| $f_{DCO4}$ | DCO frequency range 4 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 3 | | | 4 | ±3.5% | MHz |
| $f_{DCO5.3}$ | DCO frequency range 5.3 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 4, DCORSEL = 1, DCOFSEL = 1 | | | 5.333 | ±3.5% | MHz |
| $f_{DCO7}$ | DCO frequency range 7 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 5, DCORSEL = 1, DCOFSEL = 2 | | | 7 | ±3.5% | MHz |
| $f_{DCO8}$ | DCO frequency range 8 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 6, DCORSEL = 1, DCOFSEL = 3 | | | 8 | ±3.5% | MHz |
| $f_{DCO16}$ | DCO frequency range 16 MHz, trimmed | Measured at SMCLK, divide by 1, DCORSEL = 1, DCOFSEL = 4 | | | 16 | ±3.5%(1) | MHz |
| $f_{DCO21}$ | DCO frequency range 21 MHz, trimmed | Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 5 | | | 21 | ±3.5%(1) | MHz |
| $f_{DCO24}$ | DCO frequency range 24 MHz, trimmed | Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 6 | | | 24 | ±3.5%(1) | MHz |
| $f_{DCO,DC}$ | Duty cycle | Measured at SMCLK, divide by 1, no external divide, all DCORSEL/DCOFSEL settings except DCORSEL = 1, DCOFSEL = 5 and DCORSEL = 1, DCOFSEL = 6 | | 48% | 50% | 52% | |
| $t_{DCO, JITTER}$ | DCO jitter | Based on $f_{signal}$ = 10 kHz and DCO used for 12-bit SAR ADC sampling source. This achieves >74 dB SNR due to jitter (that is, it is limited by ADC performance). | | | 2 | 3 | ns |
| $df_{DCO}/dT$ | DCO temperature drift(2) | | 3.0 V | | 0.01 | | %/ºC |

(1) After a wakeup from LPM1, LPM2, LPM3, or LPM4, the DCO frequency $f_{DCO}$ might exceed the specified frequency range for a few clock cycles by up to 5% before settling into the specified steady-state frequency range.
(2) Calculated using the box method: (MAX(–40ºC to 85ºC) – MIN(–40ºC to 85ºC)) / MIN(–40ºC to 85ºC) / (85ºC – (–40ºC))

Table 5-7 lists the characteristics of the VLO.

**Table 5-7. Internal Very-Low-Power Low-Frequency Oscillator (VLO)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{VLO}$ | Current consumption | | | 100 | | nA |
| $f_{VLO}$ | VLO frequency | Measured at ACLK | 6 | 9.4 | 14 | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift | Measured at ACLK(1) | | 0.2 | | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift | Measured at ACLK(2) | | 0.7 | | %/V |
| $f_{VLO,DC}$ | Duty cycle | Measured at ACLK | 40% | 50% | 60% | |

(1) Calculated using the box method: (MAX(–40ºC to 85°C) – MIN(–40ºC to 85°C)) / MIN(–40ºC to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-8 lists the characteristics of the MODOSC.

**Table 5-8. Module Oscillator (MODOSC)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{MODOSC}$ | Current consumption | Enabled | | 25 | | µA |
| $f_{MODOSC}$ | MODOSC frequency | | 4.0 | 4.8 | 5.4 | MHz |
| $f_{MODOSC}/dT$ | MODOSC frequency temperature drift(1) | | | 0.08 | | %/°C |
| $f_{MODOSC}/dV_{CC}$ | MODOSC frequency supply voltage drift(2) | | | 1.4 | | %/V |
| $DC_{MODOSC}$ | Duty cycle | Measured at SMCLK, divide by 1 | 40% | 50% | 60% | |

(1) Calculated using the box method: (MAX(–40ºC to 85°C) – MIN(–40ºC to 85°C)) / MIN(–40ºC to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

### 5.13.4 Wake-up Characteristics

Table 5-9 lists the wake-up times.

**Table 5-9. Wake-up Times From Low-Power Modes and Reset**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{WAKE-UP\ FRAM}$ | (Additional) wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from an LPM if immediate activation is selected for wakeup | | | | 6 | 10 | µs |
| $t_{WAKE-UP\ LPM0}$ | Wake-up time from LPM0 to active mode(1) | | 2.2 V, 3.0 V | | | 400 + 1.5 / $f_{DCO}$ | ns |
| $t_{WAKE-UP\ LPM1}$ | Wake-up time from LPM1 to active mode(1) | | 2.2 V, 3.0 V | | 6 | | µs |
| $t_{WAKE-UP\ LPM2}$ | Wake-up time from LPM2 to active mode(1) | | 2.2 V, 3.0 V | | 6 | | µs |
| $t_{WAKE-UP\ LPM3}$ | Wake-up time from LPM3 to active mode(1) | | 2.2 V, 3.0 V | | 7 | 10 | µs |
| $t_{WAKE-UP\ LPM4}$ | Wake-up time from LPM4 to active mode(1) | | 2.2 V, 3.0 V | | 7 | 10 | µs |
| $t_{WAKE-UP\ LPM3.5}$ | Wake-up time from LPM3.5 to active mode(2) | | 2.2 V, 3.0 V | | 250 | 375 | µs |
| $t_{WAKE-UP\ LPM4.5}$ | Wake-up time from LPM4.5 to active mode(2) | SVSHE = 1 | 2.2 V, 3.0 V | | 250 | 375 | µs |
| | | SVSHE = 0 | 2.2 V, 3.0 V | | 1 | 1.5 | ms |
| $t_{WAKE-UP-RST}$ | Wake-up time from a $\overline{RST}$ pin triggered reset to active mode(2) | | 2.2 V, 3.0 V | | 250 | 375 | µs |
| $t_{WAKE-UP-BOR}$ | Wake-up time from power-up to active mode (2) | | 2.2 V, 3.0 V | | 1 | 1.5 | ms |

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge. MCLK is sourced by the DCO and the MCLK divider is set to divide-by-1 (DIVMx = 000b, $f_{MCLK} = f_{DCO}$). This time includes the activation of the FRAM during wakeup.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

Table 5-10 lists the typical charge consumed during wakeup from various low-power modes.

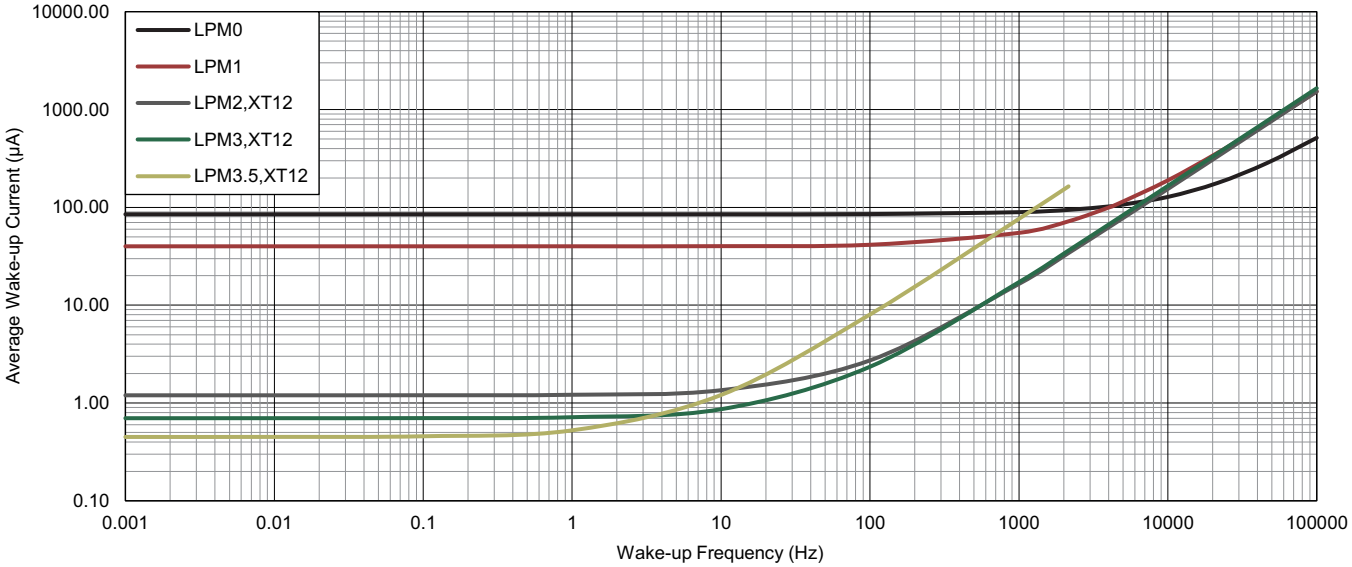
**Table 5-10. Typical Wake-up Charge(1)**

also see Figure 5-7 and Figure 5-8

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $Q_{WAKE-UP\ FRAM}$ | Charge used for activating the FRAM in AM or during wake-up from LPM0 if previously disabled by the FRAM controller. | | | 15.1 | | nAs |
| $Q_{WAKE-UP\ LPM0}$ | Charge used for wake-up from LPM0 to active mode (with FRAM active) | | | 4.4 | | nAs |
| $Q_{WAKE-UP\ LPM1}$ | Charge used for wake-up from LPM1 to active mode (with FRAM active) | | | 15.1 | | nAs |
| $Q_{WAKE-UP\ LPM2}$ | Charge used for wake-up from LPM2 to active mode (with FRAM active) | | | 15.3 | | nAs |
| $Q_{WAKE-UP\ LPM3}$ | Charge used for wake-up from LPM3 to active mode (with FRAM active) | | | 16.5 | | nAs |
| $Q_{WAKE-UP\ LPM4}$ | Charge used for wake-up from LPM4 to active mode (with FRAM active) | | | 16.5 | | nAs |
| $Q_{WAKE-UP\ LPM3.5}$ | Charge used for wake-up from LPM3.5 to active mode(2) | | | 76 | | nAs |
| $Q_{WAKE-UP\ LPM4.5}$ | Charge used for wake-up from LPM4.5 to active mode(2) | SVSHE = 1 | | 77 | | nAs |
| | | SVSHE = 0 | | 77.5 | | |
| $Q_{WAKE-UP-RESET}$ | Charge used for reset from $\overline{RST}$ or BOR event to active mode(2) | | | 75 | | nAs |

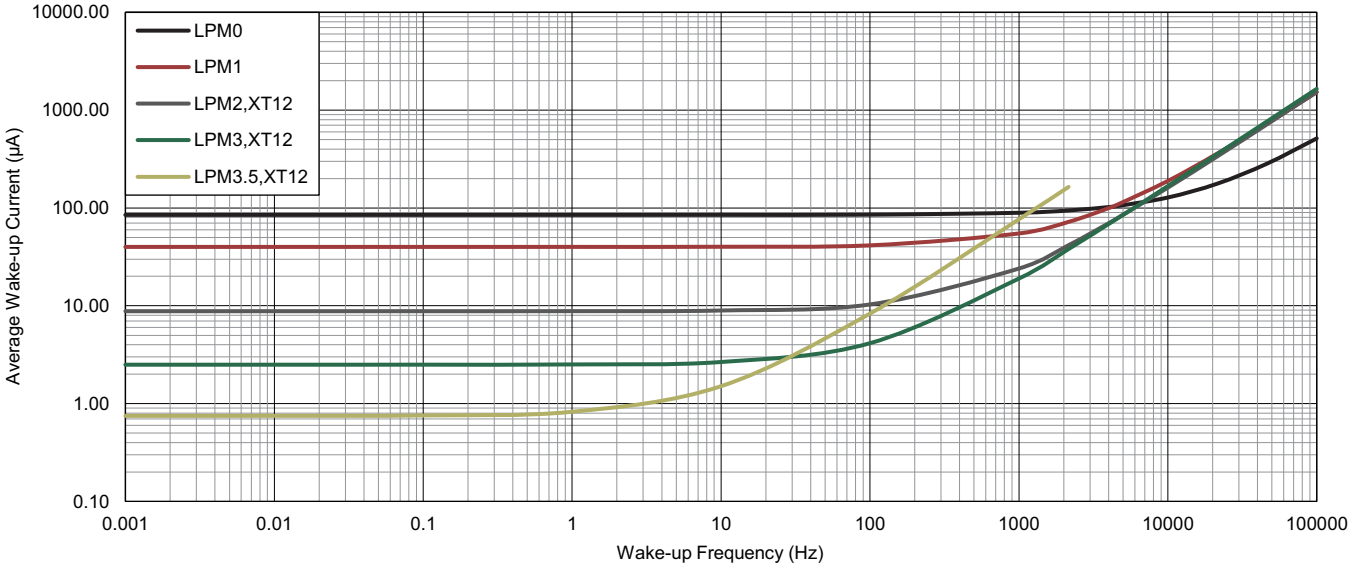
(1) Charge used during the wake-up time from a given low-power mode to active mode. This does not include the energy required in active mode (for example, for an interrupt service routine).
(2) Charge required until start of user code. This does not include the energy required to reconfigure the device.

### 5.13.4.1 Typical Characteristics, Average LPM Currents vs Wake-up Frequency




NOTE: The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

**Figure 5-7. Average LPM Currents vs Wake-up Frequency at 25°C**




NOTE: The average wake-up current does not include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

**Figure 5-8. Average LPM Currents vs Wake-up Frequency at 85°C**

## 5.13.5 Peripherals

### 5.13.5.1 Digital I/Os

Table 5-11 lists the characteristics of the digital inputs.

**Table 5-11. Digital Inputs**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | 2.2 V | 1.2 | | 1.65 | V |
| | | | 3.0 V | 1.65 | | 2.25 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | 2.2 V | 0.55 | | 1.00 | V |
| | | | 3.0 V | 0.75 | | 1.35 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | | 2.2 V | 0.44 | | 0.98 | V |
| | | | 3.0 V | 0.60 | | 1.30 | |
| $R_{Pull}$ | Pullup or pulldown resistor | For pullup: $V_{IN} = V_{SS}$<br>For pulldown: $V_{IN} = V_{CC}$ | | 20 | 35 | 50 | kΩ |
| $C_{I,dig}$ | Input capacitance, digital only port pins | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 3 | | pF |
| $C_{I,ana}$ | Input capacitance, port pins with shared analog functions(1) | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |
| $I_{lkg(Px.y)}$ | High-impedance input leakage current | See (2) (3) | 2.2 V, 3.0 V | –20 | | +20 | nA |
| $t_{(int)}$ | External interrupt timing (external trigger pulse duration to set interrupt flag)(4) | Ports with interrupt capability (see 节 1.4 and Section 4.2) | 2.2 V, 3.0 V | 20 | | | ns |
| $t_{(RST)}$ | External reset pulse duration on $\overline{RST}$(5) | | 2.2 V, 3.0 V | 2 | | | µs |

(1) If the port pins PJ.4/LFXIN and PJ.5/LFXOUT are used as digital I/Os, they are connected by a 4-pF capacitor and a 35-MΩ resistor in series. At frequencies of approximately 1 kHz and lower, the 4-pF capacitor can add to the pin capacitance of PJ.4/LFXIN or PJ.5/LFXOUT.
(2) The input leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pins, unless otherwise noted.
(3) The input leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
(4) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It might be set by trigger signals shorter than $t_{(int)}$.
(5) Not applicable if $\overline{RST}$/NMI pin configured as NMI.

Table 5-12 lists the characteristics of the digital outputs.

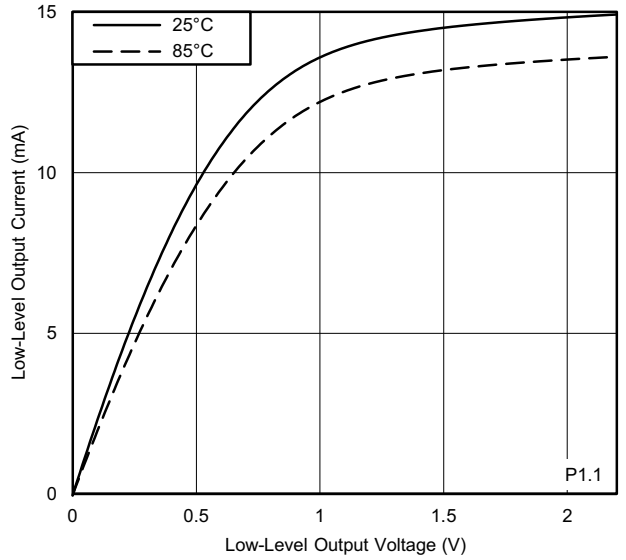
**Table 5-12. Digital Outputs**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-9, Figure 5-10, Figure 5-11, and Figure 5-12)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –1 mA(1) | 2.2 V | $V_{CC}$ – 0.25 | | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –3 mA(2) | | $V_{CC}$ – 0.60 | | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –2 mA(1) | 3.0 V | $V_{CC}$ – 0.25 | | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –6 mA(2) | | $V_{CC}$ – 0.60 | | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 1 mA(1) | 2.2 V | $V_{SS}$ | | $V_{SS}$ + 0.25 | V |
| | | $I_{(OLmax)}$ = 3 mA(2) | | $V_{SS}$ | | $V_{SS}$ + 0.60 | |
| | | $I_{(OLmax)}$ = 2 mA(1) | 3.0 V | $V_{SS}$ | | $V_{SS}$ + 0.25 | |
| | | $I_{(OLmax)}$ = 6 mA(2) | | $V_{SS}$ | | $V_{SS}$ + 0.60 | |
| $f_{Px.y}$ | Port output frequency (with load)(3) | $C_L$ = 20 pF, $R_L$ (4) (5) | 2.2 V | 16 | | | MHz |
| | | | 3.0 V | 16 | | | |
| $f_{Port\_CLK}$ | Clock output frequency(3) | ACLK, MCLK, or SMCLK at configured output port, $C_L$ = 20 pF(5) | 2.2 V | 16 | | | MHz |
| | | | 3.0 V | 16 | | | |
| $t_{rise,dig}$ | Port output rise time, digital only port pins | $C_L$ = 20 pF | 2.2 V | | 4 | 15 | ns |
| | | | 3.0 V | | 3 | 15 | |
| $t_{fall,dig}$ | Port output fall time, digital only port pins | $C_L$ = 20 pF | 2.2 V | | 4 | 15 | ns |
| | | | 3.0 V | | 3 | 15 | |
| $t_{rise,ana}$ | Port output rise time, port pins with shared analog functions | $C_L$ = 20 pF | 2.2 V | | 6 | 15 | ns |
| | | | 3.0 V | | 4 | 15 | |
| $t_{fall,ana}$ | Port output fall time, port pins with shared analog functions | $C_L$ = 20 pF | 2.2 V | | 6 | 15 | ns |
| | | | 3.0 V | | 4 | 15 | |

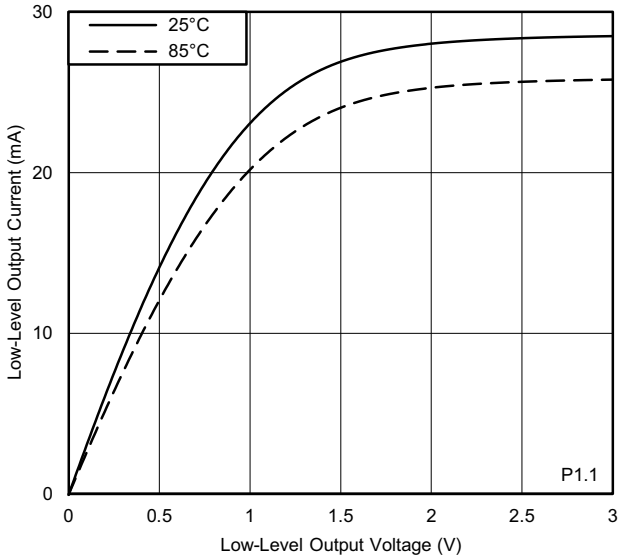
(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) The port can output frequencies at least up to the specified limit - it might support higher frequencies.
(4) A resistive divider with 2 × R1 and R1 = 1.6 kΩ between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider. $C_L$ = 20 pF is connected from the output to $V_{SS}$.
(5) The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.

#### 5.13.5.1.1 Typical Characteristics, Digital Outputs at 3.0 V and 2.2 V



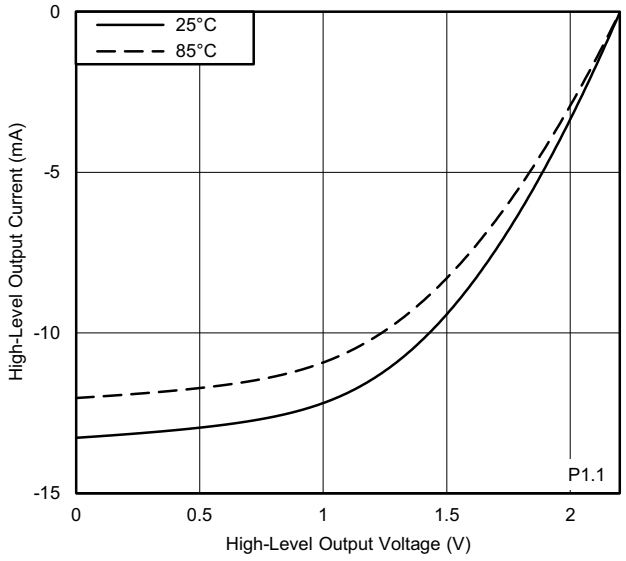

$V_{CC}$ = 2.2 V

**Figure 5-9. Typical Low-Level Output Current vs Low-Level Output Voltage**



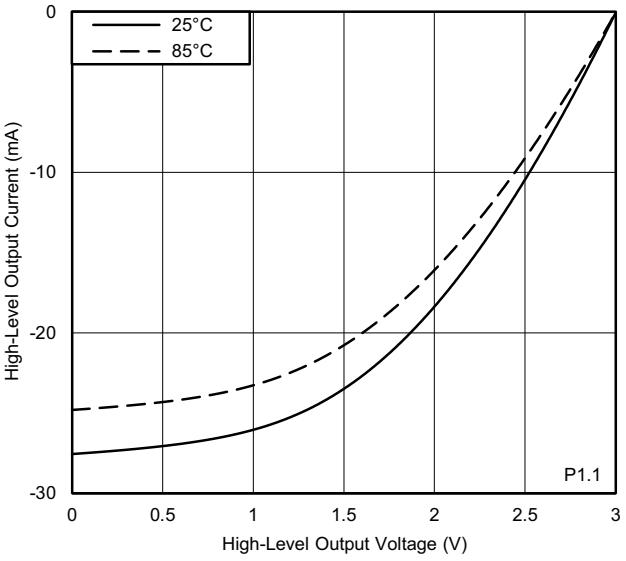

$V_{CC}$ = 3.0 V

**Figure 5-10. Typical Low-Level Output Current vs Low-Level Output Voltage**




$V_{CC}$ = 2.2 V

**Figure 5-11. Typical High-Level Output Current vs High-Level Output Voltage**




$V_{CC}$ = 3.0 V

**Figure 5-12. Typical High-Level Output Current vs High-Level Output Voltage**

Table 5-13 lists the frequencies of the pin oscillator.

**Table 5-13. Pin-Oscillator Frequency, Ports Px**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-13 and Figure 5-14)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $fo_{Px.y}$ | Pin-oscillator frequency | Px.y, $C_L$ = 10 pF(1) | 3.0 V | | 1200 | | kHz |
| | | Px.y, $C_L$ = 20 pF(1) | | | 650 | | |

(1) $C_L$ is the external load capacitance connected from the output to $V_{SS}$ and includes all parasitic effects such as PCB traces.

### 5.13.5.1.2 Typical Characteristics, Pin-Oscillator Frequency

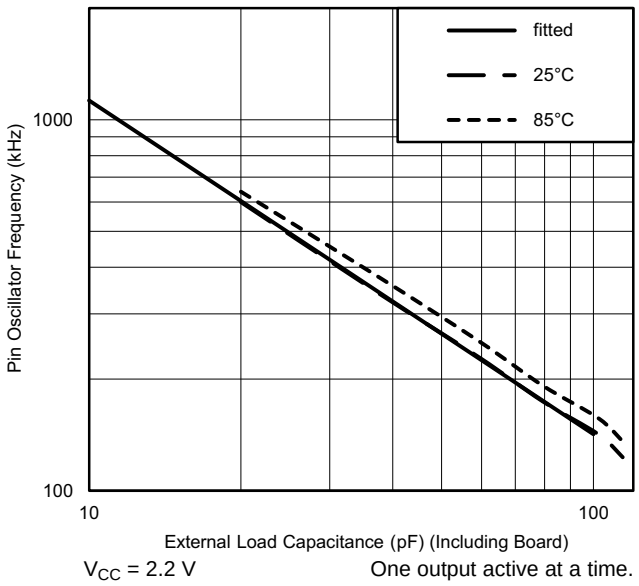



**Figure 5-13. Typical Oscillation Frequency vs Load Capacitance**

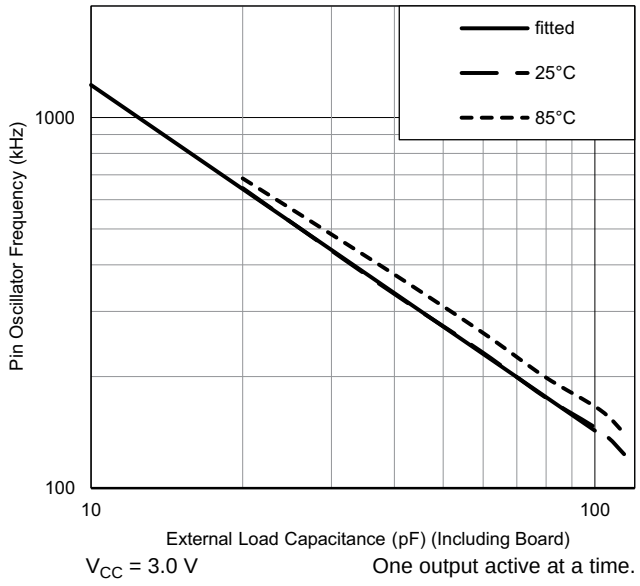



**Figure 5-14. Typical Oscillation Frequency vs Load Capacitance**

### 5.13.5.2 Timer_A and Timer_B

Table 5-14 lists the characteristics of the Timer_A.

**Table 5-14. Timer_A**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A input clock frequency | Internal: SMCLK or ACLK,<br>External: TACLK,<br>Duty cycle = 50% ±10% | 2.2 V,<br>3.0 V | | | 16 | MHz |
| $t_{TA,cap}$ | Timer_A capture timing | All capture inputs, minimum pulse duration required for capture | 2.2 V,<br>3.0 V | 20 | | | ns |

Table 5-15 lists the characteristics of the Timer_B.

**Table 5-15. Timer_B**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TB}$ | Timer_B input clock frequency | Internal: SMCLK or ACLK,<br>External: TBCLK,<br>Duty cycle = 50% ±10% | 2.2 V,<br>3.0 V | | | 16 | MHz |
| $t_{TB,cap}$ | Timer_B capture timing | All capture inputs, minimum pulse duration required for capture | 2.2 V,<br>3.0 V | 20 | | | ns |

#### 5.13.5.3 eUSCI

Table 5-16 lists the supported clock frequencies of the eUSCI in UART mode.

**Table 5-16. eUSCI (UART Mode) Clock Frequency**

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or ACLK,<br>External: UCLK,<br>Duty cycle = 50% ±10% | | 16 | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency<br>(equals baud rate in MBaud) | | | 4 | MHz |

Table 5-17 lists the characteristics of the eUSCI in UART mode.

**Table 5-17. eUSCI (UART Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_t$ | UART receive deglitch time(1) | UCGLITx = 0 | 2.2 V, 3.0 V | 5 | | 30 | ns |
| | | UCGLITx = 1 | | 20 | | 90 | |
| | | UCGLITx = 2 | | 35 | | 160 | |
| | | UCGLITx = 3 | | 50 | | 220 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum useable baud rate. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-18 lists the supported clock frequencies of the eUSCI in SPI master mode.

**Table 5-18. eUSCI (SPI Master Mode) Clock Frequency**

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or ACLK,<br>Duty cycle = 50% ±10% | | 16 | MHz |

Table 5-19 lists the characteristics of the eUSCI in SPI master mode.

**Table 5-19. eUSCI (SPI Master Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | UCSTEM = 1, UCMODEx = 01 or 10 | | 1 | | | UCxCLK cycles |
| $t_{STE,LAG}$ | STE lag time, last clock to STE inactive | UCSTEM = 1, UCMODEx = 01 or 10 | | 1 | | | UCxCLK cycles |
| $t_{STE,ACC}$ | STE access time, STE active to SIMO data out | UCSTEM = 0, UCMODEx = 01 or 10 | 2.2 V, 3.0 V | | | 60 | ns |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SOMI high impedance | UCSTEM = 0, UCMODEx = 01 or 10 | 2.2 V, 3.0 V | | | 80 | ns |
| $t_{SU,MI}$ | SOMI input data setup time | | 2.2 V | 40 | | | ns |
| | | | 3.0 V | 40 | | | |
| $t_{HD,MI}$ | SOMI input data hold time | | 2.2 V | 0 | | | ns |
| | | | 3.0 V | 0 | | | |
| $t_{VALID,MO}$ | SIMO output data valid time(2) | UCLK edge to SIMO valid, $C_L$ = 20 pF | 2.2 V | | | 10 | ns |
| | | | 3.0 V | | | 10 | |
| $t_{HD,MO}$ | SIMO output data hold time(3) | $C_L$ = 20 pF | 2.2 V | | 0 | | ns |
| | | | 3.0 V | | 0 | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} = max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-15 and Figure 5-16.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-15 and Figure 5-16.

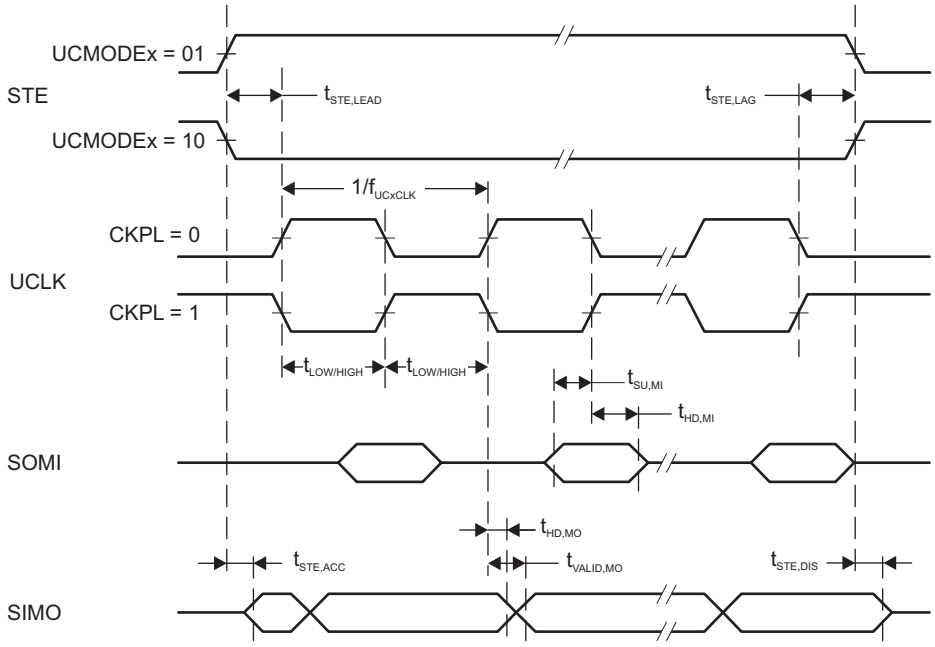



**Figure 5-15. SPI Master Mode, CKPH = 0**

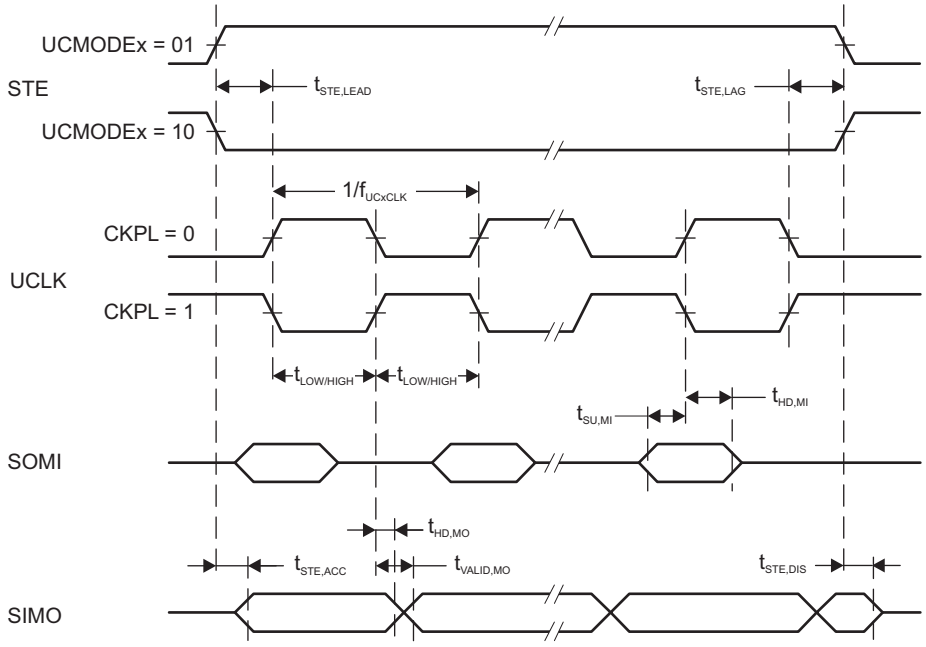



**Figure 5-16. SPI Master Mode, CKPH = 1**

Table 5-20 lists the characteristics of the eUSCI in SPI slave mode.

**Table 5-20. eUSCI (SPI Slave Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | | 2.2 V | 45 | | ns |
| | | | 3.0 V | 40 | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | | 2.2 V | 2 | | ns |
| | | | 3.0 V | 3 | | |
| $t_{STE,ACC}$ | STE access time, STE active to SOMI data out | | 2.2 V | | 45 | ns |
| | | | 3.0 V | | 40 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SOMI high impedance | | 2.2 V | | 50 | ns |
| | | | 3.0 V | | 45 | |
| $t_{SU,SI}$ | SIMO input data setup time | | 2.2 V | 4 | | ns |
| | | | 3.0 V | 4 | | |
| $t_{HD,SI}$ | SIMO input data hold time | | 2.2 V | 7 | | ns |
| | | | 3.0 V | 7 | | |
| $t_{VALID,SO}$ | SOMI output data valid time(2) | UCLK edge to SOMI valid, $C_L$ = 20 pF | 2.2 V | | 35 | ns |
| | | | 3.0 V | | 35 | |
| $t_{HD,SO}$ | SOMI output data hold time(3) | $C_L$ = 20 pF | 2.2 V | 0 | | ns |
| | | | 3.0 V | 0 | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-17 and Figure 5-18.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams inFigure 5-17 and Figure 5-18.

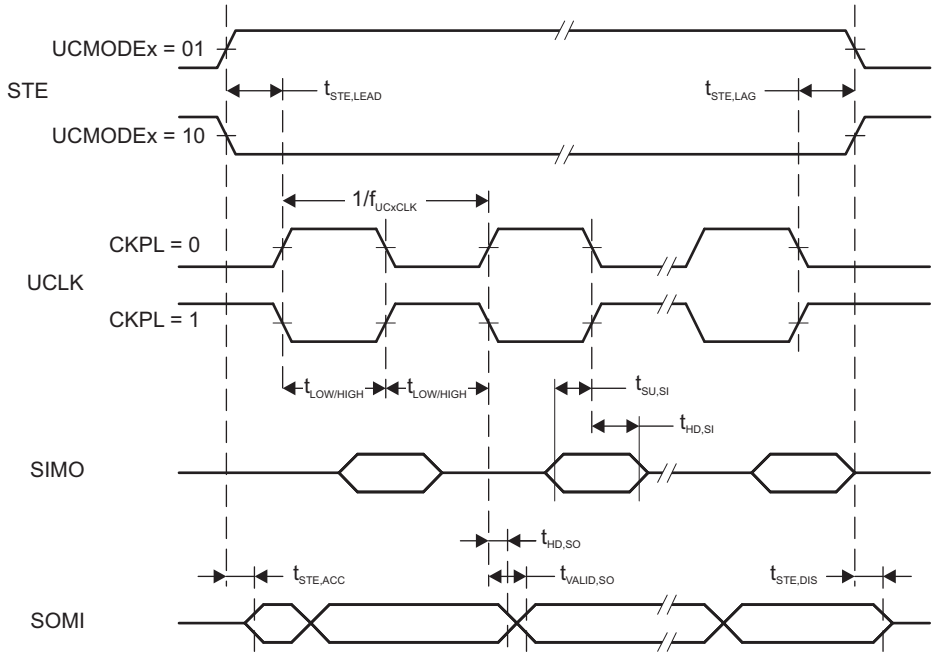



**Figure 5-17. SPI Slave Mode, CKPH = 0**

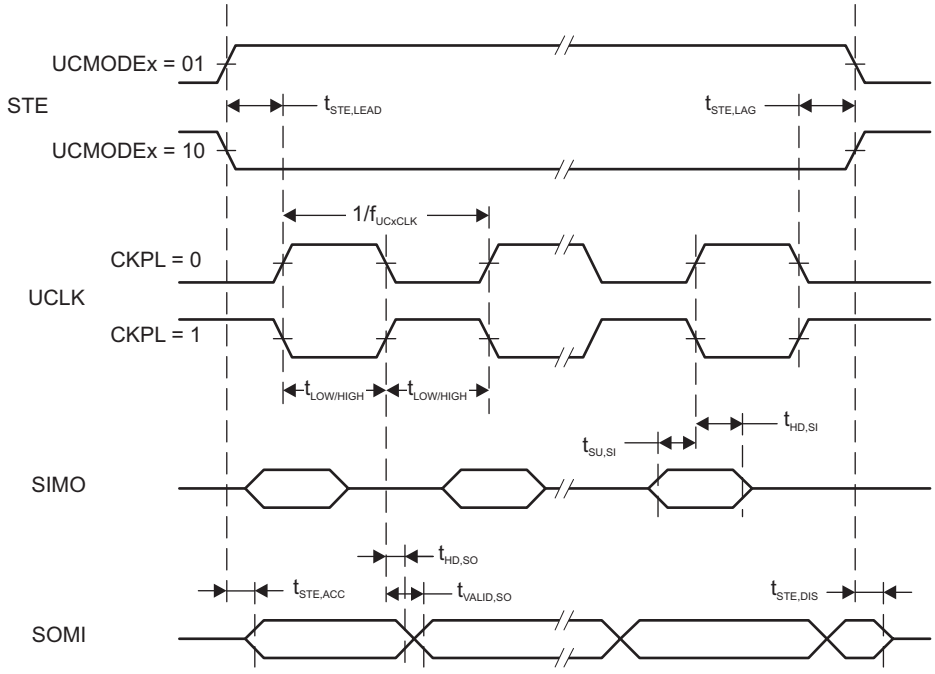



**Figure 5-18. SPI Slave Mode, CKPH = 1**

Table 5-21 lists the characteristics of the eUSCI in I²C mode.

**Table 5-21. eUSCI (I²C Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-19)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10% | | | | 16 | MHz |
| $f_{SCL}$ | SCL clock frequency | | 2.2 V, 3.0 V | 0 | | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL}$ = 100 kHz | 2.2 V, 3.0 V | 4.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL}$ = 100 kHz | 2.2 V, 3.0 V | 4.7 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{HD,DAT}$ | Data hold time | | 2.2 V, 3.0 V | 0 | | | ns |
| $t_{SU,DAT}$ | Data setup time | | 2.2 V, 3.0 V | 100 | | | ns |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL}$ = 100 kHz | 2.2 V, 3.0 V | 4.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{BUF}$ | Bus free time between STOP and START conditions | $f_{SCL}$ = 100 kHz | | 4.7 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 1.3 | | | |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | UCGLITx = 0 | 2.2 V, 3.0 V | 50 | | 250 | ns |
| | | UCGLITx = 1 | | 25 | | 125 | |
| | | UCGLITx = 2 | | 12.5 | | 62.5 | |
| | | UCGLITx = 3 | | 6.3 | | 31.5 | |
| $t_{TIMEOUT}$ | Clock low time-out | UCCLTOx = 1 | 2.2 V, 3.0 V | | 27 | | ms |
| | | UCCLTOx = 2 | | | 30 | | |
| | | UCCLTOx = 3 | | | 33 | | |

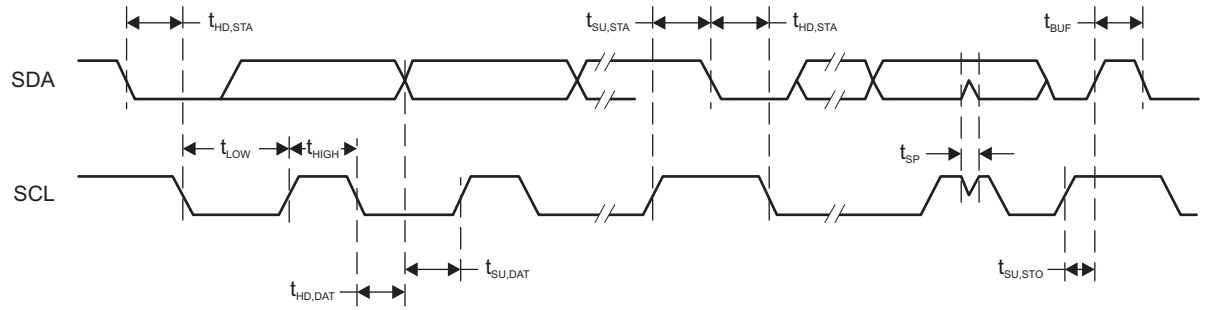



**Figure 5-19. I²C Mode Timing**

### 5.13.5.4 LCD Controller

Table 5-22 lists the operating conditions of the LCD_C.

**Table 5-22. LCD_C, Recommended Operating Conditions**

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC,LCD\_C,CP\ en,3.6}$ | Supply voltage range, charge pump enabled, $V_{LCD} \le 3.6$ V | LCDCPEN = 1, 0000b < VLCDx ≤ 1111b (charge pump enabled, $V_{LCD} \le 3.6$ V) | 2.2 | | 3.6 | V |
| $V_{CC,LCD\_C,CP\ en,3.3}$ | Supply voltage range, charge pump enabled, $V_{LCD} \le 3.3$ V | LCDCPEN = 1, 0000b < VLCDx ≤ 1100b (charge pump enabled, $V_{LCD} \le 3.3$ V) | 2.0 | | 3.6 | V |
| $V_{CC,LCD\_C,int.\ bias}$ | Supply voltage range, internal biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 0 | 2.4 | | 3.6 | V |
| $V_{CC,LCD\_C,ext.\ bias}$ | Supply voltage range, external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 0 | 2.4 | | 3.6 | V |
| $V_{CC,LCD\_C,VLCDEXT}$ | Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 1 | 2.0 | | 3.6 | V |
| $V_{LCDCAP}$ | External LCD voltage at LCDCAP, internal or external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 1 | 2.4 | | 3.6 | V |
| $C_{LCDCAP}$ | Capacitor value on LCDCAP when charge pump enabled | LCDCPEN = 1, VLCDx > 0000b (charge pump enabled) | $4.7_{-20\%}$ | 4.7 | $10_{+20\%}$ | µF |
| $f_{ACLK,in}$ | ACLK input frequency range | | 30 | 32.768 | 40 | kHz |
| $f_{LCD}$ | LCD frequency range | $f_{FRAME}$ = 1/(2 × mux) × $f_{LCD}$ with mux = 1 (static) to 8 | 0 | | 1024 | Hz |
| $f_{FRAME,4mux}$ | LCD frame frequency range | $f_{FRAME,4mux}$(MAX) = 1/(2 × 4) × $f_{LCD}$(MAX) = 1/(2 × 4) × 1024 Hz | | | 128 | Hz |
| $f_{FRAME,8mux}$ | LCD frame frequency range | $f_{FRAME,8mux}$(MAX) = 1/(2 × 4) × $f_{LCD}$(MAX) = 1/(2 × 8) × 1024 Hz | | | 64 | Hz |
| $C_{Panel}$ | Panel capacitance | $f_{LCD}$ = 1024 Hz, all common lines equally loaded | | | 10000 | pF |
| $V_{R33}$ | Analog input voltage at R33 | LCDCPEN = 0, VLCDEXT = 1 | 2.4 | | $V_{CC}$+0.2 | V |
| $V_{R23,1/3bias}$ | Analog input voltage at R23 | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | $V_{R13}$ | $V_{R03}$ + 2/3 × ($V_{R33}$-$V_{R03}$) | $V_{R33}$ | V |
| $V_{R13,1/3bias}$ | Analog input voltage at R13 with 1/3 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | $V_{R03}$ | $V_{R03}$ + 1/3 × ($V_{R33}$ – $V_{R03}$) | $V_{R23}$ | V |
| $V_{R13,1/2bias}$ | Analog input voltage at R13 with 1/2 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1 | $V_{R03}$ | $V_{R03}$ + 1/2 × ($V_{R33}$ – $V_{R03}$) | $V_{R33}$ | V |
| $V_{R03}$ | Analog input voltage at R03 | R0EXT = 1 | $V_{SS}$ | | | V |
| $V_{LCD}$-$V_{R03}$ | Voltage difference between $V_{LCD}$ and R03 | LCDCPEN = 0, R0EXT = 1 | 2.4 | | $V_{CC}$+0.2 | V |
| $V_{LCDREF}$ | External LCD reference voltage applied at LCDREF | VLCDREFx = 01 | 0.8 | 1.0 | 1.2 | V |

Table 5-23 lists the characteristics of the LCD_C.

**Table 5-23. LCD_C Electrical Characteristics**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{LCD,0}$ | LCD voltage | VLCDx = 0000, VLCDEXT = 0 | 2.4 V to 3.6 V | | $V_{CC}$ | | V |
| $V_{LCD,1}$ | | LCDCPEN = 1, VLCDx = 0001b | 2 V to 3.6 V | 2.49 | 2.60 | 2.72 | |
| $V_{LCD,2}$ | | LCDCPEN = 1, VLCDx = 0010b | 2 V to 3.6 V | | 2.66 | | |
| $V_{LCD,3}$ | | LCDCPEN = 1, VLCDx = 0011b | 2 V to 3.6 V | | 2.72 | | |
| $V_{LCD,4}$ | | LCDCPEN = 1, VLCDx = 0100b | 2 V to 3.6 V | | 2.78 | | |
| $V_{LCD,5}$ | | LCDCPEN = 1, VLCDx = 0101b | 2 V to 3.6 V | | 2.84 | | |
| $V_{LCD,6}$ | | LCDCPEN = 1, VLCDx = 0110b | 2 V to 3.6 V | | 2.90 | | |
| $V_{LCD,7}$ | | LCDCPEN = 1, VLCDx = 0111b | 2 V to 3.6 V | | 2.96 | | |
| $V_{LCD,8}$ | | LCDCPEN = 1, VLCDx = 1000b | 2 V to 3.6 V | | 3.02 | | |
| $V_{LCD,9}$ | | LCDCPEN = 1, VLCDx = 1001b | 2 V to 3.6 V | | 3.08 | | |
| $V_{LCD,10}$ | | LCDCPEN = 1, VLCDx = 1010b | 2 V to 3.6 V | | 3.14 | | |
| $V_{LCD,11}$ | | LCDCPEN = 1, VLCDx = 1011b | 2 V to 3.6 V | | 3.20 | | |
| $V_{LCD,12}$ | | LCDCPEN = 1, VLCDx = 1100b | 2 V to 3.6 V | | 3.26 | | |
| $V_{LCD,13}$ | | LCDCPEN = 1, VLCDx = 1101b | 2.2 V to 3.6 V | | 3.32 | | |
| $V_{LCD,14}$ | | LCDCPEN = 1, VLCDx = 1110b | 2.2 V to 3.6 V | | 3.38 | | |
| $V_{LCD,15}$ | | LCDCPEN = 1, VLCDx = 1111b | 2.2 V to 3.6 V | 3.32 | 3.44 | 3.6 | |
| $V_{LCD,7,0.8}$ | LCD voltage with external reference of 0.8 V | LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, $V_{LCDREF}$ = 0.8 V | 2 V to 3.6 V | | 2.96 × 0.8 V | | V |
| $V_{LCD,7,1.0}$ | LCD voltage with external reference of 1.0 V | LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, $V_{LCDREF}$ = 1.0 V | 2 V to 3.6 V | | 2.96 × 1.0 V | | V |
| $V_{LCD,7,1.2}$ | LCD voltage with external reference of 1.2 V | LCDCPEN = 1, VLCDx = 0111b, VLCDREFx = 01b, $V_{LCDREF}$ = 1.2 V | 2.2 V to 3.6 V | | 2.96 × 1.2 V | | V |
| $\Delta V_{LCD}$ | Voltage difference between consecutive VLCDx settings | $\Delta V_{LCD} = V_{LCD,x} - V_{LCD,x-1}$ with x = 0010b to 1111b | | 40 | 60 | 80 | mV |
| $I_{CC,Peak,CP}$ | Peak supply currents due to charge pump activities | LCDCPEN = 1, VLCDx = 1111b external, with decoupling capacitor on DVCC supply ≥ 1 µF | 2.2 V | | 600 | | µA |
| $t_{LCD,CP,on}$ | Time to charge $C_{LCD}$ when discharged | $C_{LCD}$ = 4.7 µF, LCDCPEN = 0→1, VLCDx = 1111b | 2.2 V | | 100 | 500 | ms |
| $I_{CP,Load}$ | Maximum charge pump load current | LCDCPEN = 1, VLCDx = 1111b | 2.2 V | 50 | | | µA |
| $R_{LCD,Seg}$ | LCD driver output impedance, segment lines | LCDCPEN = 0, $I_{LOAD}$ = ±10 µA | 2.2 V | | | 10 | kΩ |
| $R_{LCD,COM}$ | LCD driver output impedance, common lines | LCDCPEN = 0, $I_{LOAD}$ = ±10 µA | 2.2 V | | | 10 | kΩ |

### 5.13.5.5 ADC

表 5-24 lists the input requirements of the ADC.

**表 5-24. 12-Bit ADC, Power Supply and Input Range Conditions**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{(Ax)}$ | Analog input voltage range(1) | All ADC12 analog input pins Ax | | 0 | | AVCC | V |
| $I_{(ADC12\_B)}$ single-ended mode | Operating supply current into AVCC and DVCC terminals(2) (3) | $f_{ADC12CLK}$ = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 0, REFON = 0, ADC12SHTx = 0, ADC12DIV = 0 | 3.0 V | | 145 | 199 | µA |
| | | | 2.2 V | | 140 | 190 | |
| $I_{(ADC12\_B)}$ differential mode | Operating supply current into AVCC and DVCC terminals(2) (3) | $f_{ADC12CLK}$ = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 1, REFON = 0, ADC12SHTx= 0, ADC12DIV = 0 | 3.0 V | | 175 | 245 | µA |
| | | | 2.2 V | | 170 | 230 | |
| $C_I$ | Input capacitance | Only one terminal Ax can be selected at one time | 2.2 V | | 10 | 15 | pF |
| $R_I$ | Input MUX ON resistance | 0 V ≤ $V_{(Ax)}$ ≤ AVCC | >2 V | | 0.5 | 4 | kΩ |
| | | | <2 V | | 1 | 10 | |

(1) The analog input voltage range must be within the selected reference voltage range $V_{R+}$ to $V_{R-}$ for valid conversion results.
(2) The internal reference supply current is not included in current consumption parameter $I_{(ADC12\_B)}$.
(3) Approximately 60% (typical) of the total current into the AVCC and DVCC terminals is from AVCC.

Table 5-25 lists the timing parameters of the ADC.

**Table 5-25. 12-Bit ADC, Timing Parameters**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{ADC12CLK}$ | Frequency for specified performance | For specified performance of ADC12 linearity parameters with ADC12PWRMD = 0.<br>If ADC12PWRMD = 1, the maximum is 1/4 of the value shown here. | | 0.45 | | 5.4 | MHz |
| $f_{ADC12CLK}$ | Frequency for reduced performance | Linearity parameters have reduced performance | | | 32.768 | | kHz |
| $f_{ADC12OSC}$ | Internal oscillator(1) | ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$ from MODCLK | | 4 | 4.8 | 5.4 | MHz |
| $t_{CONVERT}$ | Conversion time | REFON = 0, Internal oscillator, $f_{ADC12CLK} = f_{ADC12OSC}$ from MODCLK, ADC12WINC = 0 | | 2.6 | | 3.5 | µs |
| | | External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0 | | See (2) | | | |
| $t_{ADC12ON}$ | Turnon settling time of the ADC | See (3) | | | | 100 | ns |
| $t_{ADC12OFF}$ | Time ADC must be off before it can be turned on again | $t_{ADC12OFF}$ must be met to make sure that $t_{ADC12ON}$ time holds. | | 100 | | | ns |
| $t_{Sample}$ | Sampling time | $R_S$ = 400 Ω, $R_I$ = 4 kΩ, $C_I$ = 15 pF, $C_{pext}$= 8 pF(4) | All pulse sample mode (ADC12SHP = 1) and extended sample mode (ADC12SHP = 0) with buffered reference (ADC12VRSEL = 0x1, 0x3, 0x5, 0x7, 0x9, 0xB, 0xD, 0xF) | 1 | | | µs |
| | | | Extended sample mode (ADC12SHP = 0) with unbuffered reference (ADC12VRSEL= 0x0, 0x2, 0x4, 0x6, 0xC, 0xE) | See (5) | | | µs |

(1) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(2) 14 × 1 / $f_{ADC12CLK}$. If ADC12WINC = 1, then 15 × 1 / $f_{ADC12CLK}$
(3) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(4) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB: $t_{sample} = \ln(2^{n+2}) \times (R_S + R_I) \times (C_I + C_{pext})$, $R_S < 10$ kΩ, where n = ADC resolution = 12, $R_S$= external source resistance, $C_{pext}$ = external parasitic capacitance.
(5) 6 × 1 / $f_{ADC12CLK}$

Table 5-26 lists the linearity parameters of the ADC when using an external reference.

**Table 5-26. 12-Bit ADC, Linearity Parameters With External Reference(1)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Resolution | Number of no missing code output-code bits | | 12 | | | bits |
| $E_I$ | Integral linearity error (INL) for differential input | 1.2 V ≤ $V_{R+}$ – $V_{R-}$ ≤ $AV_{CC}$ | | | ±1.8 | LSB |
| $E_I$ | Integral linearity error (INL) for single ended inputs | 1.2 V ≤ $V_{R+}$ – $V_{R-}$ ≤ $AV_{CC}$ | | | ±2.2 | LSB |
| $E_D$ | Differential linearity error (DNL) | | –0.99 | | +1.0 | LSB |
| $E_O$ | Offset error(2) (3) | ADC12VRSEL = 0x2 or 0x4 without TLV calibration, TLV calibration data can be used to improve the parameter(4) | | ±0.5 | ±1.5 | mV |
| $E_{G,ext}$ | Gain error | With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, TLV calibration data can be used to improve the parameter(4), $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | | ±0.8 | ±2.5 | LSB |
| | | With external voltage reference with internal buffer (ADC12VRSEL = 0x3), $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | | ±1 | ±20 | |
| $E_{T,ext}$ | Total unadjusted error | With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, TLV calibration data can be used to improve the parameter(4), $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | | ±1.4 | ±3.5 | LSB |
| | | With external voltage reference with internal buffer (ADC12VRSEL = 0x3), $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | | ±1.4 | ±21.0 | |

(1) See Table 5-28 and Table 5-34 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) Offset is measured as the input voltage (at which ADC output transitions from 0 to 1) minus 0.5 LSB.
(3) Offset increases as $I_R$ drop increases when $V_{R-}$ is AVSS.
(4) For details, see the device descriptor in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*.

Table 5-27 lists the dynamic performance characteristics of the ADC with differential inputs and an external reference.

**Table 5-27. 12-Bit ADC, Dynamic Performance for Differential Inputs With External Reference(1)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| SNR | Signal-to-noise | $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | 68 | 71 | | dB |
| ENOB | Effective number of bits(2) | $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | 10.7 | 11.2 | | bits |

(1) See Table 5-28 and Table 5-34 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-28 lists the dynamic performance characteristics of the ADC with differential inputs and an internal reference.

**Table 5-28. 12-Bit ADC, Dynamic Performance for Differential Inputs With Internal Reference(1)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits(2) | $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | 10.3 | 10.7 | | Bits |

(1) See Table 5-34 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-29 lists the dynamic performance characteristics of the ADC with single-ended inputs and an external reference.

**Table 5-29. 12-Bit ADC, Dynamic Performance for Single-Ended Inputs With External Reference(1)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| SNR | Signal-to-noise | $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | 64 | 68 | | dB |
| ENOB | Effective number of bits(2) | $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | 10.2 | 10.7 | | bits |

(1) See Table 5-30 and Table 5-34 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-30 lists the dynamic performance characteristics of the ADC with single-ended inputs and an internal reference.

**Table 5-30. 12-Bit ADC, Dynamic Performance for Single-Ended Inputs With Internal Reference(1)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits(2) | $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | 9.4 | 10.4 | | bits |

(1) See Table 5-34 for more information on internal reference performance, and see *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal or external reference.
(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-31 lists the dynamic performance characteristics of the ADC using a 32.678-kHz clock.

**Table 5-31. 12-Bit ADC, Dynamic Performance With 32.768-kHz Clock**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| ENOB | Effective number of bits(1) | Reduced performance with $f_{ADC12CLK}$ from ACLK LFXT 32.768 kHz, $V_{R+}$ = 2.5 V, $V_{R-}$ = AVSS | 10 | bits |

(1) ENOB = (SINAD – 1.76) / 6.02

Table 5-32 lists the characteristics of the temperature sensor and built-in $V_{1/2}$ of the ADC.

**Table 5-32. 12-Bit ADC, Temperature Sensor and Built-In $V_{1/2}$**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{SENSOR}$ | See (1) (2) (also see Figure 5-20) | ADC12ON = 1, ADC12TCMAP = 1, $T_A$ = 0°C | | 700 | | mV |
| $TC_{SENSOR}$ | See (2) | ADC12ON = 1, ADC12TCMAP = 1 | | 2.5 | | mV/°C |
| $t_{SENSOR(sample)}$ | Sample time required if ADCTCMAP = 1 and channel (MAX – 1) is selected(3) | ADC12ON = 1, ADC12TCMAP = 1, Error of conversion result ≤ 1 LSB | 30 | | | µs |
| $V_{1/2}$ | AVCC voltage divider for ADC12BATMAP = 1 on MAX input channel | ADC12ON = 1, ADC12BATMAP = 1 | 47.5% | 50% | 52.5% | |
| $I_{V\ 1/2}$ | Current for battery monitor during sample time | ADC12ON = 1, ADC12BATMAP = 1 | | 38 | 63 | µA |
| $t_{V\ 1/2\ (sample)}$ | Sample time required if ADC12BATMAP = 1 and channel MAX is selected(4) | ADC12ON = 1, ADC12BATMAP = 1 | 1.7 | | | µs |

(1) The temperature sensor offset can be as much as ±30°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The device descriptor structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each available reference voltage level. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, °C}) + V_{SENSOR}$, where $TC_{SENSOR}$ and $V_{SENSOR}$ can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 250 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{V1/2(on)}$ is included in the sampling time $t_{V1/2(sample)}$; no additional on time is needed.

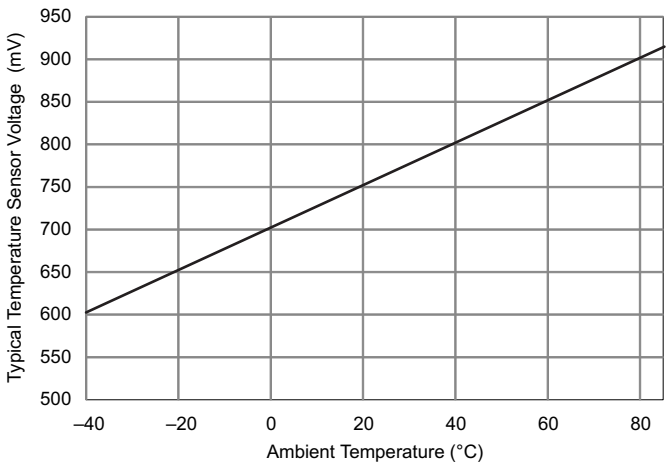



**Figure 5-20. Typical Temperature Sensor Voltage**

Table 5-33 lists the external reference requirements for the ADC.

**Table 5-33. 12-Bit ADC, External Reference(1)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{R+}$ | Positive external reference voltage input VeREF+ or VeREF- based on ADC12VRSEL bit | $V_{R+} > V_{R-}$ | 1.2 | | $AV_{CC}$ | V |
| $V_{R-}$ | Negative external reference voltage input VeREF+ or VeREF- based on ADC12VRSEL bit | $V_{R+} > V_{R-}$ | 0 | | 1.2 | V |
| $V_{R+} - V_{R-}$ | Differential external reference voltage input | $V_{R+} > V_{R-}$ | 1.2 | | $AV_{CC}$ | V |
| $I_{VeREF+}$, $I_{VeREF-}$ | Static input current, singled-ended input mode | 1.2 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V<br>$f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, ADC12DIF = 0, ADC12PWRMD = 0 | | | ±10 | µA |
| | | 1.2 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$ , $V_{eREF-}$ = 0 V<br>$f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, ADC12DIF = 0, ADC12PWRMD = 01 | | | ±2.5 | |
| $I_{VeREF+}$, $I_{VeREF-}$ | Static input current, differential input mode | 1.2 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V<br>$f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, ADC12DIF = 1, ADC12PWRMD = 0 | | | ±20 | µA |
| | | 1.2 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$ , $V_{eREF-}$ = 0 V<br>$f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, ADC12DIF = 1, ADC12PWRMD = 1 | | | ±5 | |
| $I_{VeREF+}$ | Peak input current with single-ended input | 0 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$, ADC12DIF = 0 | | | 1.5 | mA |
| $I_{VeREF+}$ | Peak input current with differential input | 0 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$, ADC12DIF = 1 | | | 3 | mA |
| $C_{VeREF+/-}$ | Capacitance at VeREF+ or VeREF- terminal | See (2) | 10 | | | µF |

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, $C_I$, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.

(2) Connect two decoupling capacitors, 10 µF and 470 nF, to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_B. Also see the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*.

### 5.13.5.6 Reference

Table 5-34 lists the characteristics of the built-in voltage reference.

**Table 5-34. REF, Built-In Reference**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF+}$ | Positive built-in reference voltage output | REFVSEL = {2} for 2.5 V, REFON = 1 | 2.7 V | | 2.5 | ±1.5% | V |
| | | REFVSEL = {1} for 2.0 V, REFON = 1 | 2.2 V | | 2.0 | ±1.5% | |
| | | REFVSEL = {0} for 1.2 V, REFON = 1 | 1.8 V | | 1.2 | ±1.8% | |
| Noise | RMS noise at VREF(1) | From 0.1 Hz to 10 Hz, REFVSEL = {0} | | | 110 | 600 | µV |
| $V_{OS\_BUF\_INT}$ | VREF ADC BUF_INT buffer offset(2) | $T_A$ = 25°C , ADC ON, REFVSEL = {0}, REFON = 1, REFOUT = 0 | | –12 | | +12 | mV |
| $V_{OS\_BUF\_EXT}$ | VREF ADC BUF_EXT buffer offset(2) | $T_A$ = 25°C, REFVSEL = {0} , REFOUT = 1, REFON = 1 or ADC ON | | –12 | | +12 | mV |
| $AV_{CC(min)}$ | AVCC minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.2 V | | 1.8 | | | V |
| | | REFVSEL = {1} for 2.0 V | | 2.2 | | | |
| | | REFVSEL = {2} for 2.5 V | | 2.7 | | | |
| $I_{REF+}$ | Operating supply current into AVCC terminal(3) | REFON = 1 | 3 V | | 8 | 15 | µA |
| $I_{REF+\_ADC\_BUF}$ | Operating supply current into AVCC terminal(3) | ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0, | 3 V | | 225 | 355 | µA |
| | | ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0 | | | 1030 | 1660 | |
| | | ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1 | | | 120 | 185 | |
| | | ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1 | | | 545 | 895 | |
| | | ADC OFF, REFON = 1, REFOUT = 1, REFVSEL = {0, 1, 2} | | | 1085 | 1780 | |
| $I_{O(VREF+)}$ | VREF maximum load current, VREF+ terminal | REFVSEL = {0, 1, 2}, AVCC = AVCC(min) for each reference level, REFON = REFOUT = 1 | | –1000 | | +10 | µA |
| ΔVout/ΔIo (VREF+) | Load-current regulation, VREF+ terminal | REFVSEL = {0, 1, 2}, $I_{O(VREF+)}$ = +10 µA or –1000 µA, $AV_{CC}$ = $AV_{CC(min)}$ for each reference level, REFON = REFOUT = 1 | | | | 2500 | µV/mA |
| $C_{VREF+/-}$ | Capacitance at VREF+ and VREF- terminals | REFON = REFOUT = 1 | | 0 | | 100 | pF |
| $TC_{REF+}$ | Temperature coefficient of built-in reference | REFVSEL = {0, 1, 2}, REFON = REFOUT = 1, $T_A$ = –40°C to 85°C(4) | | | 18 | 50 | ppm/K |
| PSRR_DC | Power supply rejection ratio (DC) | $AV_{CC}$ = $AV_{CC(min)}$ to $AV_{CC(max)}$, $T_A$ = 25°C, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1 | | | 120 | 400 | µV/V |
| PSRR_AC | Power supply rejection ratio (AC) | $dAV_{CC}$= 0.1 V at 1 kHz | | | 3.0 | | mV/V |
| $t_{SETTLE}$ | Settling time of reference voltage(5) | $AV_{CC}$ = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFON = 0 → 1 | | | 75 | 80 | µs |

(1) Internal reference noise affects ADC performance when ADC uses internal reference. See *Designing With the MSP430FR59xx and MSP430FR58xx ADC* for details on optimizing ADC performance for your application with the choice of internal versus external reference.
(2) Buffer offset affects ADC gain error and thus total unadjusted error.
(3) The internal reference current is supplied through the AVCC terminal.
(4) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
(5) The condition is that the error in a conversion started after $t_{REFON}$ is less than ±0.5 LSB.

### 5.13.5.7 Comparator

Table 5-35 lists the characteristics of the comparator.

**Table 5-35. Comparator_E**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{AVCC\_COMP}$ | Comparator operating supply current into AVCC, excludes reference resistor ladder | CEPWRMD = 00, CEON = 1, CERSx = 00 (fast) | 2.2 V, 3.0 V | | 11 | 20 | µA |
| | | CEPWRMD = 01, CEON = 1, CERSx = 00 (medium) | | | 9 | 17 | |
| | | CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), $T_A$ = 30°C | | | | 0.5 | |
| | | CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), $T_A$ = 85°C | | | | 1.3 | |
| $I_{AVCC\_REF}$ | Quiescent current of resistor ladder into AVCC, including REF module current | CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0, CEREFACC = 0 | 2.2 V, 3.0 V | | 12 | 15 | µA |
| | | CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0, CEREFACC = 1 | | | 5 | 7 | |
| $V_{REF}$ | Reference voltage level | CERSx = 11, CEREFLx = 01, CEREFACC = 0 | 1.8 V | 1.17 | 1.2 | 1.23 | V |
| | | CERSx = 11, CEREFLx = 10, CEREFACC = 0 | 2.2 V | 1.92 | 2.0 | 2.08 | |
| | | CERSx = 11, CEREFLx = 11, CEREFACC = 0 | 2.7 V | 2.40 | 2.5 | 2.60 | |
| | | CERSx = 11, CEREFLx = 01, CEREFACC = 1 | 1.8 V | 1.10 | 1.2 | 1.245 | |
| | | CERSx = 11, CEREFLx = 10, CEREFACC = 1 | 2.2 V | 1.90 | 2.0 | 2.08 | |
| | | CERSx = 11, CEREFLx = 11, CEREFACC = 1 | 2.7 V | 2.35 | 2.5 | 2.60 | |
| $V_{IC}$ | Common-mode input range | | | 0 | | $V_{CC}$ – 1 | V |
| $V_{OFFSET}$ | Input offset voltage | CEPWRMD = 00 | | –32 | | 32 | mV |
| | | CEPWRMD = 01 | | –32 | | 32 | |
| | | CEPWRMD = 10 | | –30 | | 30 | |
| $C_{IN}$ | Input capacitance | CEPWRMD = 00 or CEPWRMD = 01 | | | 9 | | pF |
| | | CEPWRMD = 10 | | | 9 | | |
| $R_{SIN}$ | Series input resistance | On (switch closed) | | | 1 | 3 | kΩ |
| | | Off (switch open) | | 50 | | | MΩ |
| $t_{PD}$ | Propagation delay, response time | CEPWRMD = 00, CEF = 0, Overdrive ≥ 20 mV | | | 260 | 330 | ns |
| | | CEPWRMD = 01, CEF = 0, Overdrive ≥ 20 mV | | | 350 | 460 | |
| | | CEPWRMD = 10, CEF = 0, Overdrive ≥ 20 mV | | | | 15 | µs |
| $t_{PD,filter}$ | Propagation delay with filter active | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 00 | | | 700 | 1000 | ns |
| | | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 01 | | | 1.0 | 1.8 | µs |
| | | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 10 | | | 2.0 | 3.5 | |
| | | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 11 | | | 4.0 | 7.0 | |
| $t_{EN\_CMP}$ | Comparator enable time | CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 00 | | | 0.9 | 1.5 | µs |
| | | CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 01 | | | 0.9 | 1.5 | |
| | | CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 10 | | | 15 | 100 | |
| $t_{EN\_CMP\_VREF}$ | Comparator and reference ladder and reference voltage enable time | CEON = 0 → 1, CEREFLX = 10, CERSx = 10 or 11, CEREF0 = CEREF1 = 0x0F, Overdrive ≥ 20 mV | | | 350 | 1500 | µs |
| $V_{CE\_REF}$ | Reference voltage for a given tap | VIN = reference into resistor ladder, n = 0 to 31 | | VIN × (n + 0.5) / 32 | VIN × (n + 1) / 32 | VIN × (n + 1.5) / 32 | V |

### 5.13.5.8 Scan Interface

Table 5-36 lists the port timing characteristics of the ESI.

**Table 5-36. Extended Scan Interface, Port Drive, Port Timing**

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OL(ESICHx)}$ | Voltage drop due to ON-resistance of excitation transistor (see Figure 5-21) | I(ESICHx) = 2 mA, ESITEN = 1 | 3 V | | | 0.3 | V |
| $V_{OH(ESICHx)}$ | Voltage drop due to ON-resistance of damping transistor(1) (see Figure 5-21) | $I_{(ESICHx)}$ = –200 µA, ESITEN = 1 | 3 V | | | 0.1 | V |
| $V_{OL(ESICOM)}$ | | $I_{(ESICOM)}$ = 3 mA, ESISH = 1 | 2.2 V, 3 V | 0 | | 0.1 | V |
| $I_{ESICHx(tri-state)}$ | | $V_{(ESICHx)}$ = 0 V to $AV_{CC}$, port function disabled, ESISH = 1 | 3 V | –50 | | 50 | nA |

(1) ESICOM = 1.5 V, supplied externally (see Figure 5-22)

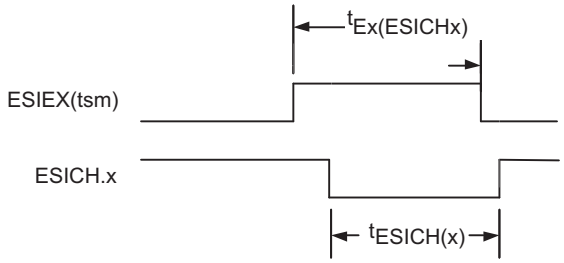



**Figure 5-21. P6.x/ESICHx Timing, ESICHx Function Selected**

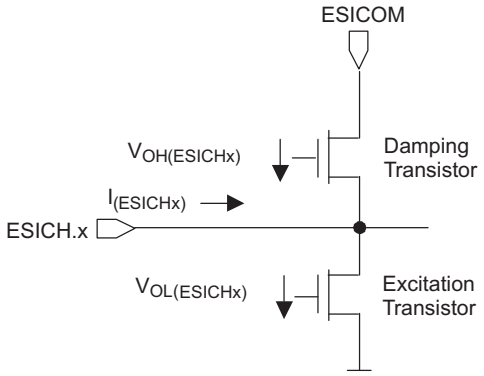



**Figure 5-22. Voltage Drop Due to ON-Resistance**

Table 5-37 lists the sample timing of the ESI.

**Table 5-37. Extended Scan Interface, Sample Capacitor/Ri Timing (1)**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{SHC(ESICHx)}$ | Sample capacitance on selected ESICHx pin | ESIEx(tsm) = 1, ESISH = 1 | 2.2 V, 3 V | | 7 | 9 | pF |
| $Ri_{(ESICHx)}$ | Serial input resistance at the ESICHx pin | ESIEx(tsm) = 1, ESISH = 1 | 2.2 V, 3 V | | 1.5 | | kΩ |
| $t_{Hold}$ | Maximum hold time (2) | ESISHTSM(3) = 1, measurement sequence uses at least two ESICHx inputs, $\Delta V_{sample}$ < 3 mV | | 62 | | | µs |

(1) The minimum sampling time (7.6 tau for 1/2 LSB accuracy) with maximum $C_{SHC(ESICHx)}$ and $Ri_{(ESICHx)}$ and $Ri_{(source)}$ is $t_{sample(min)} \approx 7.6 \times C_{SHC(ESICHx)} \times (Ri_{(ESICHx)} + Ri_{(source)})$ with $Ri_{(source)}$ estimated at 3 kΩ, $t_{sample(min)}$ = 319 ns.
(2) The sampled voltage at the sample capacitance varies less than 3 mV ($\Delta V_{sample}$) during the hold time $t_{Hold}$. If the voltage is sampled after $t_{Hold}$, the sampled voltage may be any other value.
(3) The control bit ESIVSS was renamed to ESISHTSM to avoid confusion with supply pin naming.

Table 5-38 lists the characteristics of the ESI $V_{CC}$/2 generator.

**Table 5-38. Extended Scan Interface, $V_{CC}$/2 Generator**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | ESI $V_{CC}$/2 generator supply voltage | AVCC = DVCC = ESIDVCC (connected together), AVSS = DVSS = ESIDVSS (connected together) | | 2.2 | | 3.6 | V |
| $I_{VMID}$ | ESI $V_{CC}$/2 generator quiescent current | $C_L$ at ESICOM pin = 470 nF ±20%, $f_{refresh(ESICOM)}$ = 32768 Hz, T = 0°C to 85°C, $R_{ext}$ = 1k in series to $C_L$ | 2.2 V, 3 V | | 370 | 500 | nA |
| | | $C_L$ at ESICOM pin = 470 nF ±20%, $f_{refresh(ESICOM)}$ = 32768 Hz, T = –40°C to 85°C | | | 370 | 1600 | |
| $f_{refresh(ESICOM)}$ | $V_{CC}$/2 refresh frequency | Source clock = ACLK | 2.2 V, 3 V | | 32.768 | | kHz |
| $V_{(ESICOM)}$ | Output voltage at pin ESICOM | $C_L$ at ESICOM pin = 470 nF ±20%, $I_{Load}$ = 1 µA | | $AV_{CC}$ / 2 –0.07 | $AV_{CC}$ / 2 | $AV_{CC}$ / 2 + 0.07 | V |
| $t_{on(ESICOM)}$ | Time to reach 98% after $V_{CC}$ / 2 is switched on | $C_L$ at ESICOM pin = 470 nF ±20%, $f_{refresh(ESICOM)}$ = 32768 Hz | 2.2 V, 3 V | | 1.7 | 6 | ms |
| $t_{VccSettle}$ (ESICOM) | Settling time to ±$V_{CC}$ / 2560 (2 LSB) after $AV_{CC}$ voltage change | ESIEN = 1, ESIVMIDEN(1) = 1, ESISH = 0, $AV_{CC}$ = $AV_{CC}$ –100 mV, $f_{refresh(ESICOM)}$ = 32768 Hz | 2.2 V, 3 V | | 3 | | ms |
| | | $AV_{CC}$ = $AV_{CC}$ + 100 mV, $f_{refresh(ESICOM)}$ = 32768 Hz | 2.2 V, 3 V | | 3 | | |

(1) The control bit ESIVCC2 was renamed to ESIVMIDEN to avoid confusion with supply pin naming.

Table 5-39 lists the characteristics of the ESI DAC.

**Table 5-39. Extended Scan Interface, 12-Bit DAC**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | ESI DAC supply voltage | ESIDVCC = AVCC = DVCC (connected together), ESIDVSS = AVSS = DVSS (connected together) | | 2.2 | | 3.6 | V |
| $I_{CC}$ | ESI 12-bit DAC operating supply current into AVCC terminal (1) | | 2.2 V | | 10 | 27 | µA |
| | | | 3 V | | 14 | 35 | |
| | Resolution | | | | 12 | | bit |
| INL | Integral nonlinearity | $R_L$ = 1000 MΩ, $C_L$ = 20 pF With autozeroing | 2.2 V, 3 V | –10 | ±2 | +10 | LSB |
| DNL | Differential nonlinearity | $R_L$ = 1000 MΩ, $C_L$ = 20 pF, Without autozeroing | 2.2 V, 3 V | –10 | | +10 | LSB |
| | | $R_L$ = 1000 MΩ, $C_L$ = 20 pF, With autozeroing | 2.2 V, 3 V | –10 | | +10 | LSB |
| $E_{OS}$ | Offset error | With autozeroing | 2.2 V, 3 V | | 0 | | V |
| $E_G$ | Gain error | With autozeroing | 2.2 V, 3 V | | | 0.6% | |
| $t_{on(ESIDAC)}$ | On time after $AV_{CC}$ of ESIDAC is switched on | $V_{+ESICA} – V_{ESIDAC}$ = ±6 mV | 2.2 V, 3 V | | | 2 | µs |
| $t_{Settle(ESIDAC)}$ | Settling time | ESIDAC code = 0h → A0h | 2.2 V, 3 V | | | 2 | µs |
| | | ESIDAC code = A0h → 0h | 2.2 V, 3 V | | | 2 | |

(1) This parameter covers one ESI 12-bit DAC, either ESI AFE1 12-bit DAC or ESI AFE2 12-bit DAC.

Table 5-40 lists the characteristics of the ESI comparator.

**Table 5-40. Extended Scan Interface, Comparator**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | ESI comparator supply voltage | ESIDVCC = AVCC = DVCC (connected together), ESIDVSS = AVSS = DVSS (connected together) | | 2.2 | | 3.6 | V |
| $I_{CC}$ | ESI comparator operating supply current into AVCC terminal (1) | | 2.2 V, 3 V | | 25 | 42 | µA |
| $V_{IC}$ | Common-mode input voltage range (2) | | 2.2 V, 3 V | 0 | | $V_{CC}$ –1 | V |
| $V_{Offset}$ | Input offset voltage | After autozeroing | 2.2 V, 3 V | –1.5 | | 1.5 | mV |
| $dV_{Offset}/dT$ | Temperature coefficient of $V_{Offset}$ (3) | Without autozeroing | 2.2 V, 3 V | | 40 | | µV/°C |
| | | After autozeroing | | | 2 | | |
| $dV_{Offset}/dV_{CC}$ | $V_{Offset}$ supply voltage ($V_{CC}$) sensitivity (4) | Without autozeroing | | | 0.3 | | mV/V |
| | | After autozeroing | | | 0.2 | | |
| $V_{hys}$ | Input voltage hysteresis | V+ terminal = V- terminal = 0.5 × $V_{CC}$ | 2.2 V, 3 V | | 0.5 | | LSB |
| $t_{on(ESICA)}$ | On time after ESICA is switched on | $V_{+ESICA} – V_{ESIDAC}$ = +6 mV, $V_{+ESICA}$ = 0.5 × $AV_{CC}$ | 2.2 V, 3 V | | | 2.0 | µs |
| $t_{Settle(ESICA)}$ | Settle time | $V_{+ESICA} – V_{ESIDAC}$ = –12 mV → 6 mV, $V_{+ESICA}$ = 0.5 × $AV_{CC}$ | 2.2 V, 3 V | | | 3.0 | µs |
| $t_{autozero}$ | Autozeroing time of comparator | $V_{input}$ = $V_{CC}$ / 2, $\lvert V_{offset} \rvert$ < 1 mV | 2.2 V, 3 V | | | 3.0 | µs |

(1) This parameter covers one single ESI comparator; either ESI AFE1 comparator or ESI AFE2 comparator.
(2) The comparator output is reliable when at least one of the input signals is within the common-mode input voltage range.
(3) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(4) Calculated using the box method: ABS((Voffset_Vcc_max – Voffset_Vcc_min)/(Vcc_max – Vcc_min))

Table 5-41 lists the characteristics of the ESI oscillator and clock.

**Table 5-41. Extended Scan Interface, ESICLK Oscillator and TSM Clock Signals**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | ESI oscillator supply voltage | ESIDVCC = AVCC = DVCC (connected together), ESIDVSS = AVSS = DVSS (connected together) | | 2.2 | | 3.6 | V |
| $I_{CC}$ | ESI oscillator operating supply current | $f_{ESIOSC}$= 4.8 MHz, ESIDIV1x = 00b, ESICLKGON = 1, ESIEN = 1, no TSM sequence running | 2.2 V | | 45 | | µA |
| | | | 3 V | | 50 | | |
| $f_{ESIOSC\_min}$ | ESI oscillator at minimum setting | $T_A$ = 30ºC, ESICLKFQ = 000000 | | | 2.3 | | MHz |
| $f_{ESIOSC\_max}$ | ESI oscillator at maximum setting | $T_A$ = 30ºC, ESICLKFQ = 111111 | | | 7.9 | | MHz |
| $t_{on(ESIOSC)}$ | Start-up time including synchronization cycles | $f_{ESIOSC}$ = 4.8 MHz | 2.2 V, 3 V | | 400 | 700 | ns |
| $f_{ESIOSC}/dT$ | ESIOSC frequency temperature drift(1) | $f_{ESIOSC}$= 4.8 MHz | 2.2 V, 3 V | | 0.15 | | %/°C |
| $f_{ESIOSC}/dV_{CC}$ | ESIOSC frequency supply voltage drift (2) | $f_{ESIOSC}$= 4.8 MHz | 2.2 V, 3 V | | 2 | | %/V |
| $f_{ESILFCLK}$ | TSM low-frequency state clock | | | | 32.768 | 50 | kHz |
| $f_{ESIHFCLK}$ | TSM high-frequency state clock | | | 0.25 | | 8 | MHz |

(1) Calculated using the box method: (MAX(–40 to 85°C) – MIN(–40 to 85°C)) / MIN(–40 to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(2.2 V to 3.6 V) – MIN(2.2 V to 3.6 V)) / MIN(2.2 V to 3.6 V) / (3.6 V – 2.2 V)

#### 5.13.5.9 FRAM Controller

Table 5-42 lists the characteristics of the FRAM.

**Table 5-42. FRAM**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Read and write endurance | | $10^{15}$ | | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J$ = 25°C | 100 | | | years |
| | | $T_J$ = 70°C | 40 | | | |
| | | $T_J$ = 85°C | 10 | | | |
| $I_{WRITE}$ | Current to write into FRAM | | | $I_{READ}$ (1) | | nA |
| $I_{ERASE}$ | Erase current | | | n/a (2) | | nA |
| $t_{WRITE}$ | Write time | | | $t_{READ}$ (3) | | ns |
| $t_{READ}$ | Read time | NWAITSx = 0 | | 1 / $f_{SYSTEM}$ (4) | | ns |
| | | NWAITSx = 1 | | 2 / $f_{SYSTEM}$ (4) | | |

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current $I_{READ}$ is included in the active mode current consumption numbers $I_{AM,FRAM}$.
(2) FRAM does not require a special erase sequence.
(3) Writing into FRAM is as fast as reading.
(4) The maximum read (and write) speed is specified by $f_{SYSTEM}$ using the appropriate wait state settings (NWAITSx).

### *5.13.6 Emulation and Debug*

Table 5-43 lists the characteristics of the JTAG and Spy-Bi-Wire interface.

**Table 5-43. JTAG and Spy-Bi-Wire Interface**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{JTAG}$ | Supply current adder when JTAG active (but not clocked) | 2.2 V, 3.0 V | | 40 | 100 | µA |
| $f_{SBW}$ | Spy-Bi-Wire input frequency | 2.2 V, 3.0 V | 0 | | 10 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse duration | 2.2 V, 3.0 V | 0.04 | | 15 | µs |
| $t_{SBW,\ En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1) | 2.2 V, 3.0 V | | | 110 | µs |
| $t_{SBW,Rst}$ | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | µs |
| $f_{TCK}$ | TCK input frequency, 4-wire JTAG (2) | 2.2 V | 0 | | 16 | MHz |
| | | 3.0 V | 0 | | 16 | MHz |
| $R_{internal}$ | Internal pulldown resistance on TEST | 2.2 V, 3.0 V | 20 | 35 | 50 | kΩ |
| $f_{TCLK}$ | TCLK/MCLK frequency during JTAG access, no FRAM access (limited by $f_{SYSTEM}$) | | | | 16 | MHz |
| $t_{TCLK,Low/High}$ | TCLK low or high clock pulse duration, no FRAM access | | | | 25 | ns |
| $f_{TCLK,FRAM}$ | TCLK/MCLK frequency during JTAG access, including FRAM access (limited by $f_{SYSTEM}$ with no FRAM wait states) | | | | 4 | MHz |
| $t_{TCLK,FRAM,Low/High}$ | TCLK low or high clock pulse duration, including FRAM accesses | | | | 100 | ns |

(1) Tools that access the Spy-Bi-Wire and BSL interfaces must wait for the $t_{SBW,En}$ time after the first transition of the TEST/SBWTCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.
(2) $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.

# 6 Detailed Description

## 6.1 Overview

The TI MSP430FR698x and MSP430FR598x families of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals. The architecture, combined with seven low-power modes, is optimized to achieve extended battery life for example in flow metering applications. The devices features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The MSP430FR698x and MSP430FR598x devices are microcontroller configurations with an extended scan interface (ESI) for background water, heat and gas volume metering together with up to five 16-bit timers, a comparator, eUSCIs that support UART, SPI, and $I^2C$, a hardware multiplier, an AES accelerator, DMA, an RTC module with alarm capabilities, up to 83 I/O pins, and a high-performance 12-bit ADC. The MSP430FR698x devices also include an LCD module with contrast control for displays with up to 320 segments.

## 6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

## 6.3 Operating Modes

The MSP430FR698x(1) and MSP430FR598x(1) MCUs have one active mode and seven software selectable low-power modes of operation (see 表 6-1). An interrupt event can wake up the device from a low-power mode (LPM0 to LPM4), service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

**表 6-1. Operating Modes**

| MODE | AM | | LPM0 | LPM1 | LPM2 | LPM3 | LPM4 | LPM3.5 | LPM4.5 | |
|---|---|---|---|---|---|---|---|---|---|---|
| | ACTIVE | ACTIVE, FRAM OFF (1) | CPU OFF (2) | CPU OFF | STANDBY | STANDBY | OFF | RTC ONLY | SHUTDOWN WITH SVS | SHUTDOWN WITHOUT SVS |
| Maximum system clock | 16 MHz | | 16 MHz | 16 MHz | 50 kHz | 50 kHz | 0 (3) | 50 kHz | 0 (3) | |
| Typical current consumption, $T_A$ = 25°C | 103 µA/MHz | 65 µA/MHz | 75 µA at 1 MHz | 40 µA at 1 MHz | 0.9 µA | 0.4 µA | 0.3 µA | 0.35 µA | 0.2 µA | 0.02 µA |
| Typical wake-up time | N/A | | instant. | 6 µs | 6 µs | 7 µs | 7 µs | 250 µs | 250 µs | 1000 µs |
| Wake-up events | N/A | | all | all | LF<br>I/O<br>Comp | LF<br>I/O<br>Comp | I/O<br>Comp | RTC<br>I/O | I/O | |
| CPU | **on** | | off | off | off | off | off | reset | reset | |
| FRAM | **on** | off (1) | standby (or off (1)) | off | off | off | off | off | off | |
| High-frequency peripherals (4) | **available** | | **available** | **available** | off | off | off | reset | reset | |
| Low-frequency peripherals (4) | **available** | | **available** | **available** | **available** | **available** (5) | off | RTC | reset | |
| Unclocked peripherals (4) | **available** | | **available** | **available** | **available** | **available** (5) | **available** (5) | reset | reset | |
| MCLK | **on** ($16MHz_{MAX}$) | | off | off | off | off | off | off | off | |
| SMCLK | opt. (6) ($16MHz_{MAX}$) | | opt. (6) ($16MHz_{MAX}$) | opt. (6) ($16MHz_{MAX}$) | off | off | off | off | off | |
| ACLK | **on** ($50\ kHz_{MAX}$) | | **on** ($50\ kHz_{MAX}$) | **on** ($50\ kHz_{MAX}$) | **on** ($50\ kHz_{MAX}$) | **on** ($50\ kHz_{MAX}$) | off | off | off | |
| External clock | optional ($16MHz_{MAX}$) | | optional ($16MHz_{MAX}$) | optional ($16MHz_{MAX}$) | optional ($50\ kHz_{MAX}$) | optional ($50\ kHz_{MAX}$) | optional ($50\ kHz_{MAX}$) | off | off | |
| Full retention | **yes** | | **yes** | **yes** | **yes** | **yes** (7) | **yes** (7) | no | no | |
| SVS | always | | always | always | opt. (8) | opt. (8) | opt. (8) | opt. (8) | on (9) | off (10) |
| Brownout | **always** | | **always** | **always** | **always** | **always** | **always** | **always** | **always** | |

(1) FRAM disabled in FRAM controller
(2) Disabling the FRAM through the FRAM controller decreases the LPM current consumption, but the wake-up time can increase. If the wake-up is for FRAM access (for example, to fetch an interrupt vector), wake-up time is increased. If the wake-up is for an operation other than FRAM access (for example, DMA transfer to RAM), wake-up time is not increased.
(3) All clocks disabled
(4) See 表 6-2 for a detailed description of peripherals in high-frequency, low-frequency, or unclocked state.
(5) See 节 6.3.1, which describes the use of peripherals in LPM3 and LPM4.
(6) Controlled by SMCLKOFF
(7) Using the RAM controller, the RAM can be completely powered down to save leakage; however, all data are lost.
(8) Activated SVS (SVSHE = 1) results in higher current consumption. SVS is not included in typical current consumption.
(9) SVSHE = 1
(10) SVSHE = 0

### 6.3.1 Peripherals in Low-Power Modes

Peripherals can be in different states that impact the achievable power modes of the device. The states depend on the operational modes of the peripherals (see 表 6-2). The states are:

- A peripheral is in a *high-frequency state* if it requires or uses a clock with a "high" frequency of more than 50 kHz.
- A peripheral is in a *low-frequency state* if it requires or uses a clock with a "low" frequency of 50 kHz or less.
- A peripheral is in an *unclocked state* if it does not require or use an internal clock.

If the CPU requests a power mode that does not support the current state of all active peripherals, the device does not enter the requested power mode and instead enters a power mode that still supports the current state of the peripherals, unless an external clock is used. If an external clock is used, the application must ensure that the correct frequency range for the requested power mode is selected.

**表 6-2. Peripheral States**

| PERIPHERAL | IN HIGH-FREQUENCY STATE(1) | IN LOW-FREQUENCY STATE(2) | IN UNCLOCKED STATE(3) |
|---|---|---|---|
| WDT | Clocked by SMCLK | Clocked by ACLK | Not applicable |
| DMA(4) | Not applicable | Not applicable | Waiting for a trigger |
| RTC_C | Not applicable | Clocked by LFXT | Not applicable |
| LCD_C | Not applicable | Clocked by ACLK or VLOCLK | Not applicable |
| Timer_A, TAx | Clocked by SMCLK or clocked by external clock >50 kHz | Clocked by ACLK or clocked by external clock ≤50 kHz. | Clocked by external clock ≤50 kHz. |
| Timer_B, TBx | Clocked by SMCLK or clocked by external clock >50 kHz | Clocked by ACLK or clocked by external clock ≤50 kHz | Clocked by external clock ≤50 kHz |
| eUSCI_Ax in UART mode | Clocked by SMCLK | Clocked by ACLK | Waiting for first edge of START bit |
| eUSCI_Ax in SPI master mode | Clocked by SMCLK | Clocked by ACLK | Not applicable |
| eUSCI_Ax in SPI slave mode | Clocked by external clock >50 kHz | Clocked by external clock ≤50 kHz | Clocked by external clock ≤50 kHz |
| eUSCI_Bx in $I^2C$ master mode | Clocked by SMCLK or clocked by external clock >50 kHz | Clocked by ACLK or clocked by external clock ≤50 kHz | Not applicable |
| eUSCI_Bx in $I^2C$ slave mode | Clocked by external clock >50 kHz | Clocked by external clock ≤50 kHz | Waiting for START condition or clocked by external clock ≤50 kHz |
| eUSCI_Bx in SPI master mode | Clocked by SMCLK | Clocked by ACLK | Not applicable |
| eUSCI_Bx in SPI slave mode | Clocked by external clock >50 kHz | Clocked by external clock ≤50 kHz | Clocked by external clock ≤50 kHz |
| ESI | Clocked by SMCLK | Clocked by ACLK or ESIOSC | Not applicable |
| ADC12_B | Clocked by SMCLK or by MODOSC | Clocked by ACLK | Waiting for a trigger |
| REF_A | Not applicable | Not applicable | Always |
| COMP_E | Not applicable | Not applicable | Always |
| CRC(5) | Not applicable | Not applicable | Not applicable |
| MPY(5) | Not applicable | Not applicable | Not applicable |
| AES(5) | Not applicable | Not applicable | Not applicable |

(1) Peripherals are in a state that requires or uses a clock with a "high" frequency of more than 50 kHz.
(2) Peripherals are in a state that requires or uses a clock with a "low" frequency of 50 kHz or less.
(3) Peripherals are in a state that does not require or does not use an internal clock.
(4) The DMA always transfers data in active mode but can wait for a trigger in any low-power mode. A DMA trigger during a low-power mode will cause a temporary transition into active mode for the time of the transfer.
(5) Operates only during active mode and will delay the transition into a low-power mode until its operation is completed.

#### 6.3.1.1 Idle Currents of Peripherals in LPM3 and LPM4

Most peripherals can be activated to be operational in LPM3 if clocked by ACLK. Some modules are even operational in LPM4 because they do not require a clock to operate (for example, the comparator). Activating a peripheral in LPM3 or LPM4 increases the current consumption due to its active supply current contribution but also due to an additional idle current. To limit the idle current adder certain peripherals are group together. To achieve optimal current consumption try to use modules within one group and to limit the number of groups with active modules. 表 6-3 lists the group for each peripheral. Modules not listed in this table are either already included in the standard LPM3 current consumption specifications or cannot be used in LPM3 or LPM4.

The idle current adder is very small at room temperature (25°C) but increases at high temperatures (85°C). See the $I_{IDLE}$ parameters in Section 5.7 for details.

**表 6-3. Peripheral Groups**

| GROUP A | GROUP B | GROUP C | GROUP D |
|---|---|---|---|
| Timer TA0 | Timer TA1 | Timer TA2 | Timer TA3 |
| Comparator | Extended Scan Interface (ESI) | Timer B0 | LCD_C |
| ADC12_B | | eUSCI_A0 | eUSCI_A1 |
| REF_A | | eUSCI_B0 | |
| | | eUSCI_B1 | |

## 6.4 Interrupt Vector Table and Signatures

The interrupt vectors, the power-up start address and signatures are in the address range 0FFFFh to 0FF80h. 图 6-1 summarizes the content of this address range.

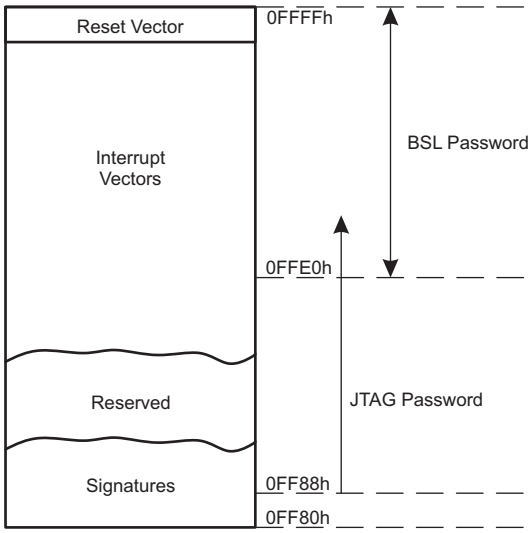



**图 6-1. Interrupt Vectors, Signatures, and Passwords**

The power-up start address or reset vector is located at 0FFFFh to 0FFFEh. It contains the 16-bit address pointing to the start address of the application program.

The interrupt vectors start at 0FFFDh and extend to lower addresses. Each vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. 表 6-4 shows the device-specific interrupt vector locations.

The vectors programmed into the address range from 0FFFFh to 0FFE0h are used as the BSL password (if enabled by the corresponding signature).

The signatures are located at 0FF80h and extend to higher addresses. Signatures are evaluated during device start-up. 表 6-5 shows the device-specific signature locations.

A JTAG password can be programmed starting at address 0FF88h and extending to higher addresses. The password can extend into the interrupt vector locations using the interrupt vector addresses as additional bits for the password. The length of the JTAG password depends on the JTAG signature.

See the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS)* chapter in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, MSP430FR69xx Family User's Guide* for details.

**表 6-4. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| **System Reset**<br>Power up, Brownout, Supply Supervisor<br>External Reset RST<br>Watchdog time-out (watchdog mode)<br>WDT, FRCTL MPU, CS, PMM password violation<br>FRAM uncorrectable bit error detection<br>MPU segment violation<br>FRAM access time error<br>Software POR, BOR | SVSHIFG<br>PMMRSTIFG<br>WDTIFG<br>WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW<br>UBDIFG<br>MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG<br>ACCTEIFG<br>PMMPORIFG, PMMBORIFG<br>(SYSRSTIV) (1) (2) | Reset | 0FFFEh | Highest |
| **System NMI**<br>Vacant memory access<br>JTAG mailbox<br>FRAM bit error detection<br>MPU segment violation | VMAIFG<br>JMBINIFG, JMBOUTIFG<br>CBDIFG, UBDIFG<br>MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG<br>(SYSSNIV) (1) (3) | (Non)maskable | 0FFFCh | |
| **User NMI**<br>External NMI<br>Oscillator fault | NMIIFG, OFIFG<br>(SYSUNIV) (1) (3) | (Non)maskable | 0FFFAh | |
| Comparator_E | Comparator_E interrupt flags<br>(CEIV) (1) | Maskable | 0FFF8h | |
| Timer_B TB0 | TB0CCR0.CCIFG | Maskable | 0FFF6h | |
| Timer_B TB0 | TB0CCR1.CCIFG to TB0CCR6.CCIFG, TB0CTL.TBIFG<br>(TB0IV)(1) | Maskable | 0FFF4h | |
| Watchdog timer (interval timer mode) | WDTIFG | Maskable | 0FFF2h | |
| Extended Scan IF | ESIIFG0 to ESIIFG8<br>(ESIIV) (1) | Maskable | 0FFF0h | |
| eUSCI_A0 receive or transmit | UCA0IFG: UCRXIFG, UCTXIFG (SPI mode)<br>UCA0IFG:UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode)<br>(UCA0IV)(1) | Maskable | 0FFEEh | |
| eUSCI_B0 receive or transmit | UCB0IFG: UCRXIFG, UCTXIFG (SPI mode)<br>UCB0IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG ($I^2C$ mode)<br>(UCB0IV)(1) | Maskable | 0FFECh | |
| ADC12_B | ADC12IFG0 to ADC12IFG31<br>ADC12LOIFG, ADC12INIFG, ADC12HIIFG, ADC12RDYIFG, ADC12OVIFG, ADC12TOVIFG<br>(ADC12IV) (1) | Maskable | 0FFEAh | |
| Timer_A TA0 | TA0CCR0.CCIFG | Maskable | 0FFE8h | |
| Timer_A TA0 | TA0CCR1.CCIFG to TA0CCR2.CCIFG, TA0CTL.TAIFG<br>(TA0IV)(1) | Maskable | 0FFE6h | |
| eUSCI_A1 receive or transmit | UCA1IFG:UCRXIFG, UCTXIFG (SPI mode)<br>UCA1IFG:UCSTTIFG, UCTXCPTIFG, UCRXIFG, UCTXIFG (UART mode)<br>(UCA1IV)(1) | Maskable | 0FFE4h | |

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space
(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

**表 6-4. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| eUSCI_B1 receive or transmit) | UCB1IFG: UCRXIFG, UCTXIFG (SPI mode) UCB1IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG ($I^2C$ mode) (UCB1IV)(1) | Maskable | 0FFE2h | |
| DMA | DMA0CTL.DMAIFG, DMA1CTL.DMAIFG, DMA2CTL.DMAIFG (DMAIV)(1) | Maskable | 0FFE0h | |
| Timer_A TA1 | TA1CCR0.CCIFG | Maskable | 0FFDEh | |
| Timer_A TA1 | TA1CCR1.CCIFG to TA1CCR2.CCIFG, TA1CTL.TAIFG (TA1IV)(1) | Maskable | 0FFDCh | |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV)(1) | Maskable | 0FFDAh | |
| Timer_A TA2 | TA2CCR0.CCIFG | Maskable | 0FFD8h | |
| Timer_A TA2 | TA2CCR1.CCIFG TA2CTL.TAIFG (TA2IV)(1) | Maskable | 0FFD6h | |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV) (1) | Maskable | 0FFD4h | |
| Timer_A TA3 | TA3CCR0.CCIFG | Maskable | 0FFD2h | |
| Timer_A TA3 | TA3CCR1.CCIFG TA3CTL.TAIFG (TA3IV)(1) | Maskable | 0FFD0h | |
| I/O Port P3 | P3IFG.0 to P3IFG.7 (P3IV) (1) | Maskable | 0FFCEh | |
| I/O Port P4 | P4IFG.0 to P4IFG.7 (P4IV) (1) | Maskable | 0FFCCh | |
| LCD_C (Reserved on MSP430FR5xxx) | LCD_C interrupt flags (LCDCIV) (1) | Maskable | 0FFCAh | |
| RTC_C | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) (1) | Maskable | 0FFC8h | |
| AES | AESRDYIFG | Maskable | 0FFC6h | Lowest |

**表 6-5. Signatures**

| SIGNATURE | WORD ADDRESS |
|---|---|
| IP Encapsulation Signature2 | 0FF8Ah |
| IP Encapsulation Signature1 (1) | 0FF88h |
| BSL Signature2 | 0FF86h |
| BSL Signature1 | 0FF84h |
| JTAG Signature2 | 0FF82h |
| JTAG Signature1 | 0FF80h |

(1) Must not contain 0AAAAh if used as JTAG password and IP encapsulation functionality is not desired.

## 6.5 Bootloader (BSL)

The BSL enables programming of the FRAM or RAM using a UART serial interface (FRxxxx devices) or an $I^2C$ interface (FRxxxx1 devices). Access to the device memory through the BSL is protected by an user-defined password. 表 6-6 lists the BSL pin requirements. BSL entry requires a specific entry sequence on the $\overline{RST}$/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see *MSP430 Programming With the Bootloader (BSL)*.

**表 6-6. BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{RST}$/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P2.0 | Devices with UART BSL (FRxxxx): Data transmit |
| P2.1 | Devices with UART BSL (FRxxxx): Data receive |
| P1.6 | Devices with $I^2C$ BSL (FRxxxx1): Data |
| P1.7 | Devices with $I^2C$ BSL (FRxxxx1): Clock |
| VCC | Power supply |
| VSS | Ground supply |

## 6.6 JTAG Operation

### 6.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/Os. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{RST}$/NMI/SBWTDIO signal is required to interface with MSP430 development tools and device programmers. 表 6-7 lists the JTAG pin requirements. For details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For details on the JTAG implementation in MSP MCUs, see *MSP430 Programming With the JTAG Interface*.

**表 6-7. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{RST}$/NMI/SBWTDIO | IN | External reset |
| VCC | | Power supply |
| VSS | | Ground supply |

### 6.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 6-8 lists the Spy-Bi-Wire interface pin requirements. For details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For details on the SBW implementation in MSP MCUs, see *MSP430 Programming With the JTAG Interface*.

**表 6-8. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN, OUT | Spy-Bi-Wire data input/output |
| VCC | | Power supply |
| VSS | | Ground supply |

## 6.7 FRAM

The FRAM can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in system by the CPU. Features of the FRAM include:

- Ultra-low-power ultra-fast-write nonvolatile memory
- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

**注**

**Wait States**

For MCLK frequencies > 8 MHz, wait states must be configured following the flow described in the "FRAM Controller (FRCTRL)" chapter, section "Wait State Control" of the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, MSP430FR69xx Family User's Guide*.

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the memory protection unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see *MSP430 FRAM Technology – How To and Best Practices*.

## 6.8 RAM

The RAM is made up of one sector. The sector can be completely powered down in LPM3 and LPM4 to save leakage; however, all data is lost during shutdown.

## 6.9 Tiny RAM

The Tiny RAM can be used to hold data or a very small stack if the complete RAM is powered down in LPM3 and LPM4.

## 6.10 Memory Protection Unit Including IP Encapsulation

The FRAM can be protected from inadvertent CPU execution, read or write access by the MPU. Features of the MPU include:

- IP Encapsulation with programmable boundaries (prevents reads from "outside" like JTAG or non-IP software) in steps of 1KB.
- Main memory partitioning programmable up to three segments in steps of 1KB.
- The access rights of each segment (main and information memory) can be individually selected.
- Access violation flags with interrupt capability for easy servicing of access violations.

## 6.11 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, MSP430FR69xx Family User's Guide*.

### 6.11.1 Digital I/O

Up to eleven 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for all pins of ports P1, P2, P3, and P4.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- Capacitive touch functionality is supported on all pins of ports P1 to P10 and PJ.
- No cross-currents during start-up

**注**

**Configuration of Digital I/Os After BOR Reset**

To prevent any cross-currents during start-up of the device all port pins are high-impedance with Schmitt triggers and their module functions disabled. To enable the I/O functionality after a BOR reset the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section of the *Digital I/O* chapter in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, MSP430FR69xx Family User's Guide*.

### 6.11.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch crystal oscillator XT1 (LF), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2 (HF). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external low frequency (<50 kHz) clock source.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced from a high-frequency crystal (HFXT2), the internal digitally controlled oscillator DCO, a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external clock source.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to MCLK.

### 6.11.3 Power-Management Module (PMM)

The primary functions of the PMM are:

- Supply regulated voltages to the core logic
- Supervise voltages that are connected to the device (at DVCC pins)
- Give reset signals to the device during power on and power off

### 6.11.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

### 6.11.5 Real-Time Clock (RTC_C)

The RTC_C module contains an integrated real-time clock (RTC) with the following features implemented:

- Calendar mode with leap year correction
- General-purpose counter mode

The internal calendar compensates months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 modes to minimize power consumption.

### 6.11.6 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals. 表 6-9 lists the clocks that can be used by the WDT.

**注**

In watchdog mode, the watchdog timer prevents entry into LPM3.5 or LPM4.5 because this would deactivate the watchdog.

**表 6-9. WDT_A Clocks**

| WDTSSEL | NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE) |
|---|---|
| 00 | SMCLK |
| 01 | ACLK |
| 10 | VLOCLK |
| 11 | LFMODCLK |

### 6.11.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These system functions include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. 表 6-10 lists the interrupt vector registers of the SYS module.

**表 6-10. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---|---|---|---|---|
| SYSRSTIV, System Reset | 019Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RSTIFG $\overline{\text{RST}}$/NMI (BOR) | 04h | |
| | | PMMSWBOR software BOR (BOR) | 06h | |
| | | LPMx.5 wakeup (BOR) | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | Reserved | 0Ch | |
| | | SVSHIFG SVSH event (BOR) | 0Eh | |
| | | Reserved | 10h | |
| | | Reserved | 12h | |
| | | PMMSWPOR software POR (POR) | 14h | |
| | | WDTIFG watchdog time-out (PUC) | 16h | |
| | | WDTPW password violation (PUC) | 18h | |
| | | FRCTLPW password violation (PUC) | 1Ah | |
| | | Uncorrectable FRAM bit error detection (PUC) | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMMPW PMM password violation (PUC) | 20h | |
| | | MPUPW MPU password violation (PUC) | 22h | |
| | | CSPW CS password violation (PUC) | 24h | |
| | | MPUSEGPIFG encapsulated IP memory segment violation (PUC) | 26h | |
| | | MPUSEGIIFG information memory segment violation (PUC) | 28h | |
| | | MPUSEG1IFG segment 1 memory violation (PUC) | 2Ah | |
| | | MPUSEG2IFG segment 2 memory violation (PUC) | 2Ch | |
| | | MPUSEG3IFG segment 3 memory violation (PUC) | 2Eh | |
| | | ACCTEIFG access time error (PUC)(1) | 30h | |
| | | Reserved | 32h to 3Eh | Lowest |
| SYSSNIV, System NMI | 019Ch | No interrupt pending | 00h | |
| | | Reserved | 02h | Highest |
| | | Uncorrectable FRAM bit error detection | 04h | |
| | | Reserved | 06h | |
| | | MPUSEGPIFG encapsulated IP memory segment violation | 08h | |
| | | MPUSEGIIFG information memory segment violation | 0Ah | |
| | | MPUSEG1IFG segment 1 memory violation | 0Ch | |
| | | MPUSEG2IFG segment 2 memory violation | 0Eh | |
| | | MPUSEG3IFG segment 3 memory violation | 10h | |
| | | VMAIFG Vacant memory access | 12h | |
| | | JMBINIFG JTAG mailbox input | 14h | |
| | | JMBOUTIFG JTAG mailbox output | 16h | |
| | | Correctable FRAM bit error detection | 18h | |
| | | Reserved | 1Ah to 1Eh | Lowest |
| SYSUNIV, User NMI | 019Ah | No interrupt pending | 00h | |
| | | NMIIFG NMI pin | 02h | Highest |
| | | OFIFG oscillator fault | 04h | |
| | | Reserved | 06h | |
| | | Reserved | 08h | |
| | | Reserved | 0Ah to 1Eh | Lowest |

(1) Indicates incorrect wait state settings.

### 6.11.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. 表 6-11 lists the triggers that can be used to start DMA operation.

**表 6-11. DMA Trigger Assignments(1)**

| TRIGGER | CHANNEL 0 | CHANNEL 1 | CHANNEL 2 |
|---|---|---|---|
| 0 | DMAREQ | DMAREQ | DMAREQ |
| 1 | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2 | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3 | TA1CCR0 CCIFG | TA1CCR0 CCIFG | TA1CCR0 CCIFG |
| 4 | TA1CCR2 CCIFG | TA1CCR2 CCIFG | TA1CCR2 CCIFG |
| 5 | TA2 CCR0 CCIFG | TA2 CCR0 CCIFG | TA2 CCR0 CCIFG |
| 6 | TA3 CCR0 CCIFG | TA3 CCR0 CCIFG | TA3 CCR0 CCIFG |
| 7 | TB0CCR0 CCIFG | TB0CCR0 CCIFG | TB0CCR0 CCIFG |
| 8 | TB0CCR2 CCIFG | TB0CCR2 CCIFG | TB0CCR2 CCIFG |
| 9 | Reserved | Reserved | Reserved |
| 10 | Reserved | Reserved | Reserved |
| 11 | AES Trigger 0 | AES Trigger 0 | AES Trigger 0 |
| 12 | AES Trigger 1 | AES Trigger 1 | AES Trigger 1 |
| 13 | AES Trigger 2 | AES Trigger 2 | AES Trigger 2 |
| 14 | UCA0RXIFG | UCA0RXIFG | UCA0RXIFG |
| 15 | UCA0TXIFG | UCA0TXIFG | UCA0TXIFG |
| 16 | UCA1RXIFG | UCA1RXIFG | UCA1RXIFG |
| 17 | UCA1TXIFG | UCA1TXIFG | UCA1TXIFG |
| 18 | UCB0RXIFG (SPI)<br>UCB0RXIFG0 ($I^2C$) | UCB0RXIFG (SPI)<br>UCB0RXIFG0 ($I^2C$) | UCB0RXIFG (SPI)<br>UCB0RXIFG0 ($I^2C$) |
| 19 | UCB0TXIFG (SPI)<br>UCB0TXIFG0 ($I^2C$) | UCB0TXIFG (SPI)<br>UCB0TXIFG0 ($I^2C$) | UCB0TXIFG (SPI)<br>UCB0TXIFG0 ($I^2C$) |
| 20 | UCB0RXIFG1 ($I^2C$) | UCB0RXIFG1 ($I^2C$) | UCB0RXIFG1 ($I^2C$) |
| 21 | UCB0TXIFG1 ($I^2C$) | UCB0TXIFG1 ($I^2C$) | UCB0TXIFG1 ($I^2C$) |
| 22 | UCB0RXIFG2 ($I^2C$) | UCB0RXIFG2 ($I^2C$) | UCB0RXIFG2 ($I^2C$) |
| 23 | UCB0TXIFG2 ($I^2C$) | UCB0TXIFG2 ($I^2C$) | UCB0TXIFG2 ($I^2C$) |
| 24 | UCB1RXIFG (SPI)<br>UCB1RXIFG0 ($I^2C$) | UCB1RXIFG (SPI)<br>UCB1RXIFG0 ($I^2C$) | UCB1RXIFG (SPI)<br>UCB1RXIFG0 ($I^2C$) |
| 25 | UCB1TXIFG (SPI)<br>UCB1TXIFG0 ($I^2C$) | UCB1TXIFG (SPI)<br>UCB1TXIFG0 ($I^2C$) | UCB1TXIFG (SPI)<br>UCB1TXIFG0 ($I^2C$) |
| 26 | ADC12 end of conversion | ADC12 end of conversion | ADC12 end of conversion |
| 27 | Reserved | Reserved | Reserved |
| 28 | ESI | ESI | ESI |
| 29 | MPY ready | MPY ready | MPY ready |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | DMAE0 | DMAE0 | DMAE0 |

(1) If a reserved trigger source is selected, no trigger is generated.

### 6.11.9 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and $I^2C$, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3 pin or 4 pin) and $I^2C$.

Two eUSCI_A modules and one or two eUSCI_B module are implemented.

### 6.11.10 Extended Scan Interface (ESI)

The ESI peripheral automatically scans sensors and measures linear or rotational motion with the lowest possible power consumption. The ESI incorporates a $V_{CC}/2$ generator, a comparator, and a 12-bit DAC and supports up to four sensors.

### 6.11.11 Timer_A TA0, Timer_A TA1

TA0 and TA1 are 16-bit timers/counters (Timer_A type) with three capture/compare registers each. TA0 and TA1 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-12 and 表 6-13). TA0 and TA1 have extensive interrupt capabilities. Interrupts can be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-12. Timer_A TA0 Signal Connections**

| INPUT PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PORT PIN |
|---|---|---|---|---|---|---|
| P1.2 or P6.7 or P7.0 | TA0CLK | TACLK | Timer | N/A | N/A | |
| | ACLK (internal) | ACLK | | | | |
| | SMCLK (internal) | SMCLK | | | | |
| P1.2 or P6.7 or P7.0 | $\overline{\text{TA0CLK}}$ | INCLK | | | | |
| P1.5 | TA0.0 | CCI0A | CCR0 | TA0 | TA0.0 | P1.5 |
| P7.1 or P10.1 | TA0.0 | CCI0B | | | | P7.1 |
| | $DV_{SS}$ | GND | | | | P10.1 |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| P1.0 or P1.6 or P7.2 or P7.6 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | P1.0 |
| | | | | | | P1.6 |
| | COUT (internal) | CCI1B | | | | P7.2 |
| | | | | | | P7.6 |
| | $DV_{SS}$ | GND | | | | ADC12 (internal) ADC12SHSx = {1} |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| P1.1 or P1.7 or P7.3 or P7.5 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | P1.1 |
| | ACLK (internal) | CCI2B | | | | P1.7 |
| | $DV_{SS}$ | GND | | | | P7.3 |
| | $DV_{CC}$ | $V_{CC}$ | | | | P7.5 |

**表 6-13. Timer_A TA1 Signal Connections**

| INPUT PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PORT PIN |
|---|---|---|---|---|---|---|
| P1.1 or P4.4 or P5.2 | TA1CLK | TACLK | Timer | N/A | N/A | |
| | ACLK (internal) | ACLK | | | | |
| | SMCLK (internal) | SMCLK | | | | |
| P1.1 or P4.4 or P5.2 | $\overline{\text{TA1CLK}}$ | INCLK | | | | |
| P1.4 or P4.5 | TA1.0 | CCI0A | CCR0 | TA0 | TA1.0 | P1.4 |
| P5.2 or P10.2 | TA1.0 | CCI0B | | | | P4.5 |
| | $DV_{SS}$ | GND | | | | P5.2 |
| | $DV_{CC}$ | $V_{CC}$ | | | | P10.2 |
| P1.2 or P3.3 or P4.6 or P5.0 | TA1.1 | CCI1A | CCR1 | TA1 | TA1.1 | P1.2 |
| | | | | | | P4.6 |
| | COUT (internal) | CCI1B | | | | P3.3 |
| | | | | | | P5.0 |
| | $DV_{SS}$ | GND | | | | ADC12 (internal) ADC12SHSx = {4} |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| P1.3 or P4.7 or P5.1 or P7.7 | TA1.2 | CCI2A | CCR2 | TA2 | TA1.2 | P1.3 |
| | ACLK (internal) | CCI2B | | | | P4.7 |
| | $DV_{SS}$ | GND | | | | P5.1 |
| | $DV_{CC}$ | $V_{CC}$ | | | | P7.7 |

### *6.11.12 Timer_A TA2*

TA2 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers each and with internal connections only. TA2 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-14). TA2 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-14. Timer_A TA2 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| COUT (internal) | TACLK | Timer | N/A | |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| From Capacitive Touch I/O 0 (internal) | INCLK | | | |
| TA3 CCR0 output (internal) | CCI0A | CCR0 | TA0 | TA3 CCI0A input |
| ACLK (internal) | CCI0B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| From Capacitive Touch I/O 0 (internal) | CCI1A | CCR1 | TA1 | ADC12 (internal) ADC12SHSx = {5} |
| COUT (internal) | CCI1B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |

### 6.11.13 Timer_A TA3

TA3 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers each and with internal connections only. TA3 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-15). TA3 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-15. Timer_A TA3 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| COUT (internal) | TACLK | Timer | N/A | |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| From Capacitive Touch I/O 1 (internal) | INCLK | | | |
| TA2 CCR0 output (internal) | CCI0A | CCR0 | TA0 | TA2 CCI0A input |
| ACLK (internal) | CCI0B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| From Capacitive Touch I/O 1 (internal) | CCI1A | CCR1 | TA1 | ADC12 (internal) ADC12SHSx = {6} |
| COUT (internal) | CCI1B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| $DV_{SS}$ | CCI2A | CCR2 | TA2 | |
| ESIO0 (internal) | CCI2B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| $DV_{SS}$ | CCI3A | CCR3 | TA3 | |
| ESIO1 (internal) | CCI3B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| $DV_{SS}$ | CCI4A | CCR4 | TA4 | |
| ESIO2 (internal) | CCI4B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |

### 6.11.14 Timer_B TB0

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers each. TB0 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-16). TB0 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**表 6-16. Timer_B TB0 Signal Connections**

| INPUT PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PORT PIN |
|---|---|---|---|---|---|---|
| P2.0 or P3.3 or P5.7 | TB0CLK | TBCLK | Timer | N/A | N/A | |
| | ACLK (internal) | ACLK | | | | |
| | SMCLK (internal) | SMCLK | | | | |
| P2.0 or P3.3 or P5.7 | $\overline{\text{TB0CLK}}$ | INCLK | | | | |
| P3.4 | TB0.0 | CCI0A | CCR0 | TB0 | TB0.0 | P3.4 |
| P6.4 | TB0.0 | CCI0B | | | | P6.4 |
| | $DV_{SS}$ | GND | | | | ADC12 (internal) ADC12SHSx = {2} |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| P3.5 or P6.5 | TB0.1 | CCI1A | CCR1 | TB1 | TB0.1 | P3.5 |
| | COUT (internal) | CCI1B | | | | P6.5 |
| | $DV_{SS}$ | GND | | | | ADC12 (internal) ADC12SHSx = {3} |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| P3.6 or P6.6 | TB0.2 | CCI2A | CCR2 | TB2 | TB0.2 | P3.6 |
| | ACLK (internal) | CCI2B | | | | P6.6 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| P2.4 | TB0.3 | CCI3A | CCR3 | TB3 | TB0.3 | P2.4 |
| P3.7 | TB0.3 | CCI3B | | | | P3.7 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| P2.5 | TB0.4 | CCI4A | CCR4 | TB4 | TB0.4 | P2.5 |
| P2.2 | TB0.4 | CCI4B | | | | P2.2 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| P2.6 | TB0.5 | CCI5A | CCR5 | TB5 | TB0.5 | P2.6 |
| P2.1 | TB0.5 | CCI5B | | | | P2.1 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |
| P2.7 | TB0.6 | CCI6A | CCR6 | TB6 | TB0.6 | P2.7 |
| P2.0 | TB0.6 | CCI6B | | | | P2.0 |
| | $DV_{SS}$ | GND | | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | | |

### 6.11.15 ADC12_B

The ADC12_B module supports fast 12-bit analog-to-digital conversions with differential and single-ended inputs. The module implements a 12-bit SAR core, sample select control, a reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

表 6-17 lists the external trigger sources. 表 6-18 lists the available multiplexing between internal and external analog inputs.

**表 6-17. ADC12_B Trigger Signal Connections**

| ADC12SHSx | | CONNECTED TRIGGER SOURCE |
|---|---|---|
| BINARY | DECIMAL | |
| 000 | 0 | Software (ADC12SC) |
| 001 | 1 | Timer_A TA0 CCR1 output |
| 010 | 2 | Timer_B TB0 CCR0 output |
| 011 | 3 | Timer_B TB0 CCR1 output |
| 100 | 4 | Timer_A TA1 CCR1 output |
| 101 | 5 | Timer_A TA2 CCR1 output |
| 110 | 6 | Timer_A TA3 CCR1 output |
| 111 | 7 | Reserved (DVSS) |

**表 6-18. ADC12_B External and Internal Signal Mapping**

| CONTROL BIT | EXTERNAL (CONTROL BIT = 0) | INTERNAL (CONTROL BIT = 1) |
|---|---|---|
| ADC12BATMAP | A31 | Battery Monitor |
| ADC12TCMAP | A30 | Temperature Sensor |
| ADC12CH0MAP | A29 | N/A(1) |
| ADC12CH1MAP | A28 | N/A(1) |
| ADC12CH2MAP | A27 | N/A(1) |
| ADC12CH3MAP | A26 | N/A(1) |

(1) N/A = No internal signal available on this device.

### 6.11.16 Comparator_E

The primary function of the Comparator_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

### 6.11.17 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 signature is based on the CRC-CCITT standard.

### 6.11.18 CRC32

The CRC32 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC32 signature is based on the ISO 3309 standard.

### 6.11.19 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-, 192-, or 256-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

### 6.11.20 True Random Seed

The Device Descriptor Information (TLV) section contains a 128-bit true random seed that can be used to implement a deterministic random number generator.

### 6.11.21 Shared Reference (REF_A)

The reference module (REF_A) generates all critical reference voltages that can be used by the various analog peripherals in the device.

### 6.11.22 LCD_C

The LCD_C driver generates the segment and common signals required to drive a liquid crystal display (LCD). The LCD_C controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static and 2-mux to 8-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage and thus contrast by software. The module also provides an automatic blinking capability for individual segments in static, 2-mux, 3-mux, and 4-mux modes.

To reduce system noise, the charge pump can be temporarily disabled. 表 6-19 lists the available automatic charge pump disable options.

**表 6-19. LCD Automatic Charge Pump Disable Bits (LCDCPDISx)**

| CONTROL BIT | DESCRIPTION |
|---|---|
| LCDCPDIS0 | LCD charge pump disable during ADC12 conversion<br>0b = LCD charge pump not automatically disabled during conversion<br>1b = LCD charge pump automatically disabled during conversion |
| LCDCPDIS1 to LCDCPDIS7 | No functionality |

### 6.11.23 Embedded Emulation

#### 6.11.23.1 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers that can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

#### 6.11.23.2 EnergyTrace++™ Technology

These MCUs implement circuitry to support EnergyTrace++ technology. The EnergyTrace++ technology allows you to observe information about the internal states of the microcontroller. These states include the CPU Program Counter (PC), the ON or OFF status of the peripherals and the system clocks (regardless of the clock source), and the low-power mode currently in use. These states can always be read by a debug tool, even when the microcontroller sleeps in LPMx.5 modes.

The activity of the following modules can be observed:

- MPY is calculating.
- WDT is counting.
- RTC is counting.
- ADC: a sequence, sample, or conversion is active.
- REF: REFBG or REFGEN active and BG in static mode.

- COMP is on.
- AES is encrypting or decrypting.
- eUSCI_A0 is transferring (receiving or transmitting) data.
- eUSCI_A1 is transferring (receiving or transmitting) data.
- eUSCI_B0 is transferring (receiving or transmitting) data.
- eUSCI_B1 is transferring (receiving or transmitting) data.
- TB0 is counting.
- TA0 is counting.
- TA1 is counting.
- TA2 is counting.
- TA3 is counting.
- LCD: timing generator is active.
- ESI:
  - ESI is active using LF clock source
  - ESI is active using HF clock source

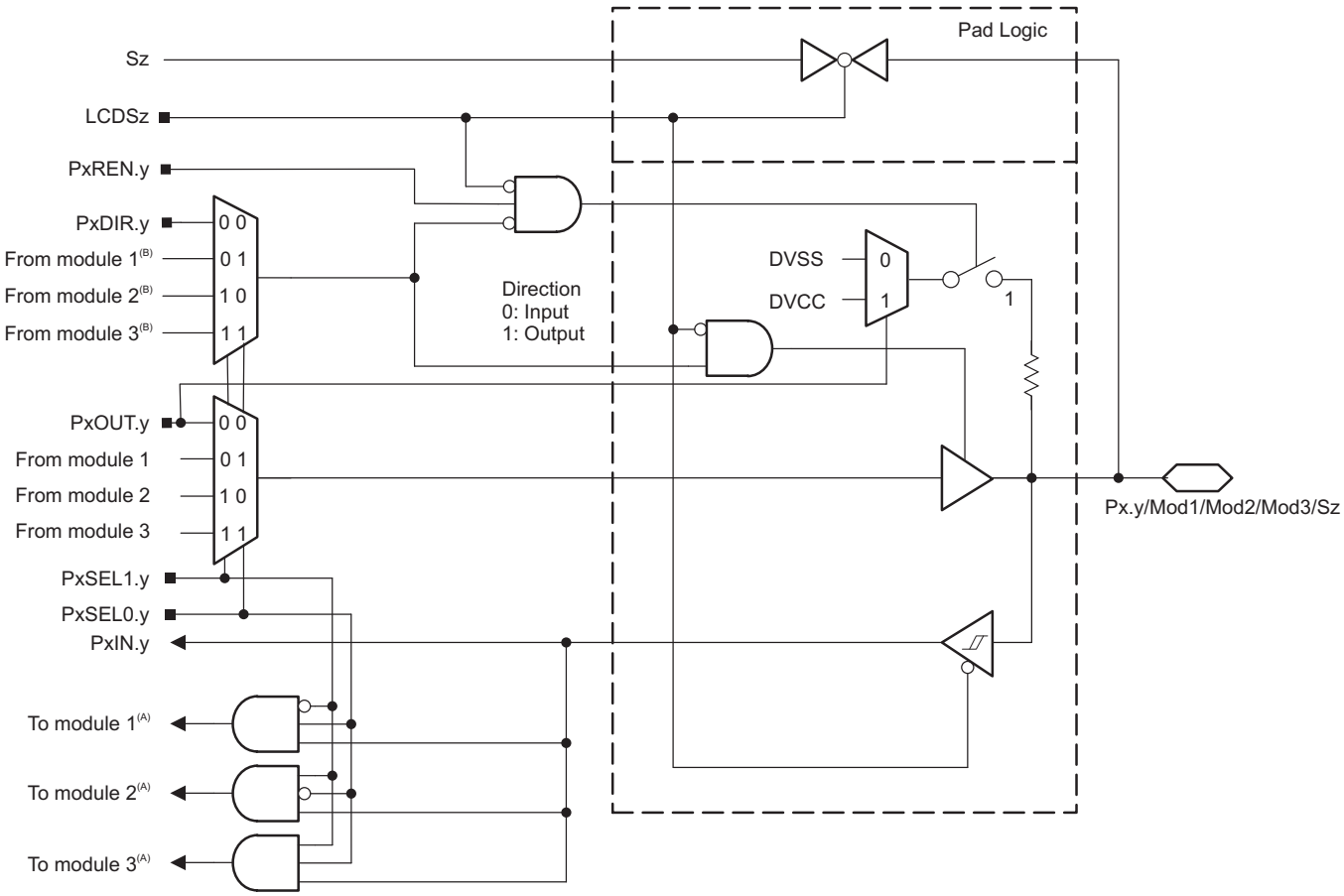
### 6.11.24 Input/Output Diagrams

#### 6.11.24.1 Digital I/O Functionality – Ports P1 to P10

The port pins provide the following features:

- Interrupt and wakeup from LPMx.5 capability for ports P1, P2, P3, and P4
- Capacitive touch functionality (see 节 6.11.24.2)
- Up to three digital module input or output functions
- LCD segment functionality (not all pins, package dependent)

图 6-2 shows the features and the corresponding control logic (not including the capacitive touch logic). It is applicable for all port pins P1.0 to P10.2 unless a dedicated diagram is available in the following sections. The module functions provided per pin and whether the direction is controlled by the module or by the port direction register for the selected secondary function are described in the pin function tables.

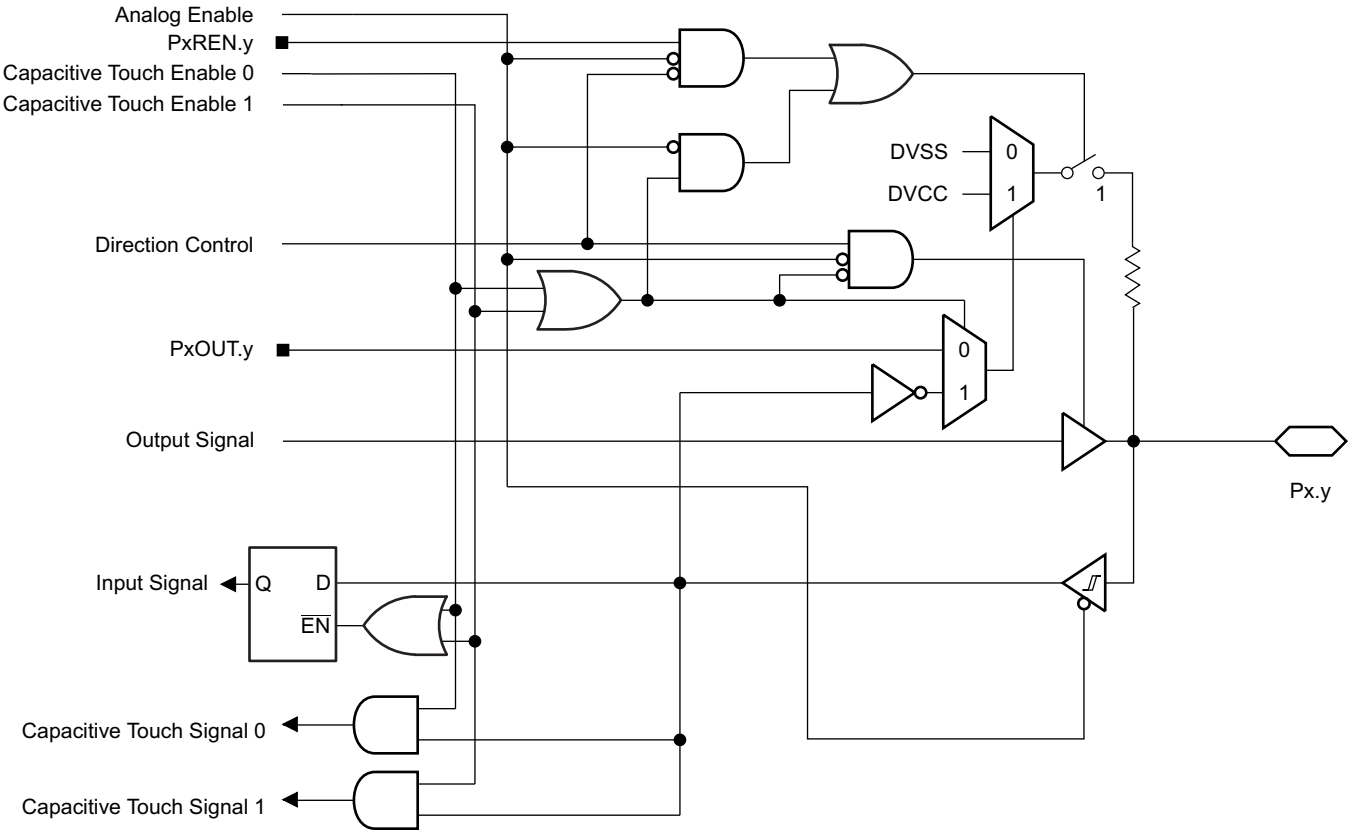



A. The inputs from several pins toward a module are ORed together.
B. The direction is controlled either by the connected module or by the corresponding PxDIR.y bit. See the pin function tables.
NOTE: Functional representation only.

**图 6-2. General Port Pin Diagram**

### 6.11.24.2 Capacitive Touch Functionality Ports P1 to P10 and PJ

图 6-3 shows the Capacitive Touch functionality that all port pins provide. The Capacitive Touch functionality is controlled using the Capacitive Touch I/O control registers CAPTIO0CTL and CAPTIO1CTL as described in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*. The Capacitive Touch functionality is not shown in the other pin diagrams.

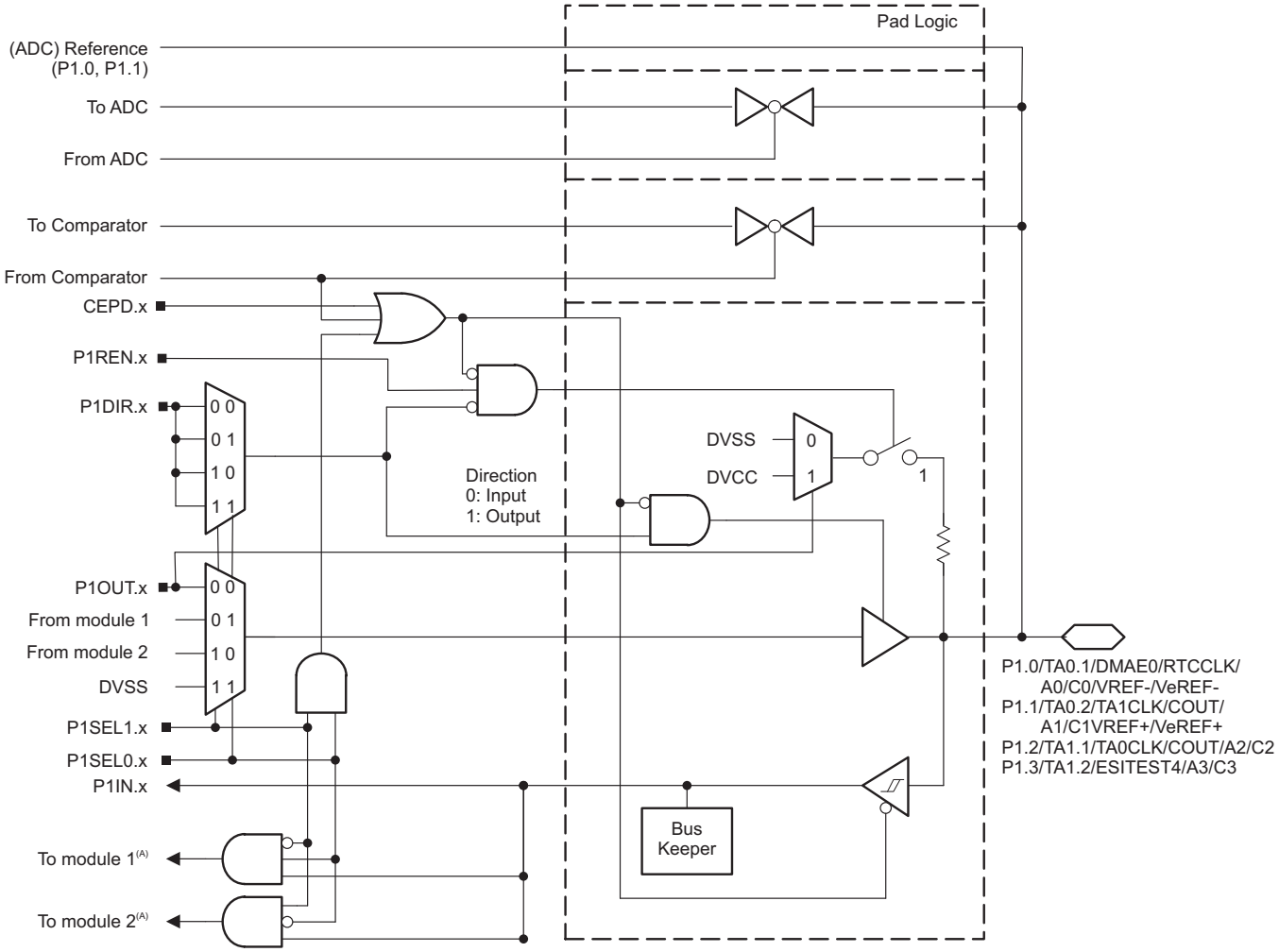



NOTE: Functional representation only.

**图 6-3. Capacitive Touch I/O Diagram**

### 6.11.24.3 Port P1 (P1.0 to P1.3) Input/Output With Schmitt Trigger

图 6-4 shows the port diagram. 表 6-20 summarizes the selection of the pin function.




A. The inputs from several pins toward a module are ORed together.
NOTE: Functional representation only.

**图 6-4. Port P1 (P1.0 to P1.3) Diagram**

**表 6-20. Port P1 (P1.0 to P1.3) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.0/TA0.1/DMAE0/RTCCLK/A0/C0/ VREF-/VeREF- | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CCI1A | 0 | 0 | 1 |
| | | TA0.1 | 1 | | |
| | | DMAE0 | 0 | 1 | 0 |
| | | RTCCLK(2) | 1 | | |
| | | A0, C0, VREF-, VeREF- (3) (4) | X | 1 | 1 |
| P1.1/TA0.2/TA1CLK/COUT/A1/C1/ VREF+/VeREF+ | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CCI2A | 0 | 0 | 1 |
| | | TA0.2 | 1 | | |
| | | TA1CLK | 0 | 1 | 0 |
| | | COUT(5) | 1 | | |
| | | A1, C1, VREF+, VeREF+ (3) (4) | X | 1 | 1 |
| P1.2/TA1.1/TA0CLK/COUT/A2/C2 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CCI1A | 0 | 0 | 1 |
| | | TA1.1 | 1 | | |
| | | TA0CLK | 0 | 1 | 0 |
| | | COUT(6) | 1 | | |
| | | A2, C2 (3) (4) | X | 1 | 1 |
| P1.3/TA1.2/ESITEST4/A3/C3 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CCI2A | 0 | 0 | 1 |
| | | TA1.2 | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | ESITEST4 | 1 | | |
| | | A3, C3 (3) (4) | X | 1 | 1 |

(1) X = Don't care
(2) Do not use this pin as RTCCLK output if the DMAE0 functionality is used on any other pin. Select an alternative RTCCLK output pin.
(3) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.
(5) Do not use this pin as COUT output if the TA1CLK functionality is used on any other pin. Select an alternative COUT output pin.
(6) Do not use this pin as COUT output if the TA0CLK functionality is used on any other pin. Select an alternative COUT output pin.

### 6.11.24.4 Port P1 (P1.4 to P1.7) Input/Output With Schmitt Trigger

For the pin diagram, see 图 6-2. 表 6-21 summarizes the selection of the pin function.

**表 6-21. Port P1 (P1.4 to P1.7) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | LCDSz |
| P1.4/UCB0CLK/UCA0STE/TA1.0/Sz | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCB0CLK | X (2) | 0 | 1 | 0 |
| | | UCA0STE | X (3) | 1 | 0 | 0 |
| | | TA1.CCI0A | 0 | 1 | 1 | 0 |
| | | TA1.0 | 1 | | | |
| | | Sz (4) | X | X | X | 1 |
| P1.5/UCB0STE/UCA0CLK/TA0.0/Sz | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCB0STE | X (2) | 0 | 1 | 0 |
| | | UCA0CLK | X (3) | 1 | 0 | 0 |
| | | TA0.CCI0A | 0 | 1 | 1 | 0 |
| | | TA0.0 | 1 | | | |
| | | Sz (4) | X | X | X | 1 |
| P1.6/UCB0SIMO/UCB0SDA/TA0.1/Sz | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCB0SIMO/UCB0SDA | X (2) | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | TA0.CCI1A | 0 | 1 | 1 | 0 |
| | | TA0.1 | 1 | | | |
| | | Sz (4) | X | X | X | 1 |
| P1.7/UCB0SOMI/UCB0SCL/TA0.2/Sz | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCB0SOMI/UCB0SCL | X (2) | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | TA0.CCI2A | 0 | 1 | 1 | 0 |
| | | TA0.2 | 1 | | | |
| | | Sz (4) | X | X | X | 1 |

(1) X = Don't care
(2) Direction controlled by eUSCI_B0 module.
(3) Direction controlled by eUSCI_A0 module.
(4) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

### 6.11.24.5 Port P2 (P2.0 to P2.3) Input/Output With Schmitt Trigger

For the pin diagram, see 图 6-2. 表 6-22 summarizes the selection of the pin function.

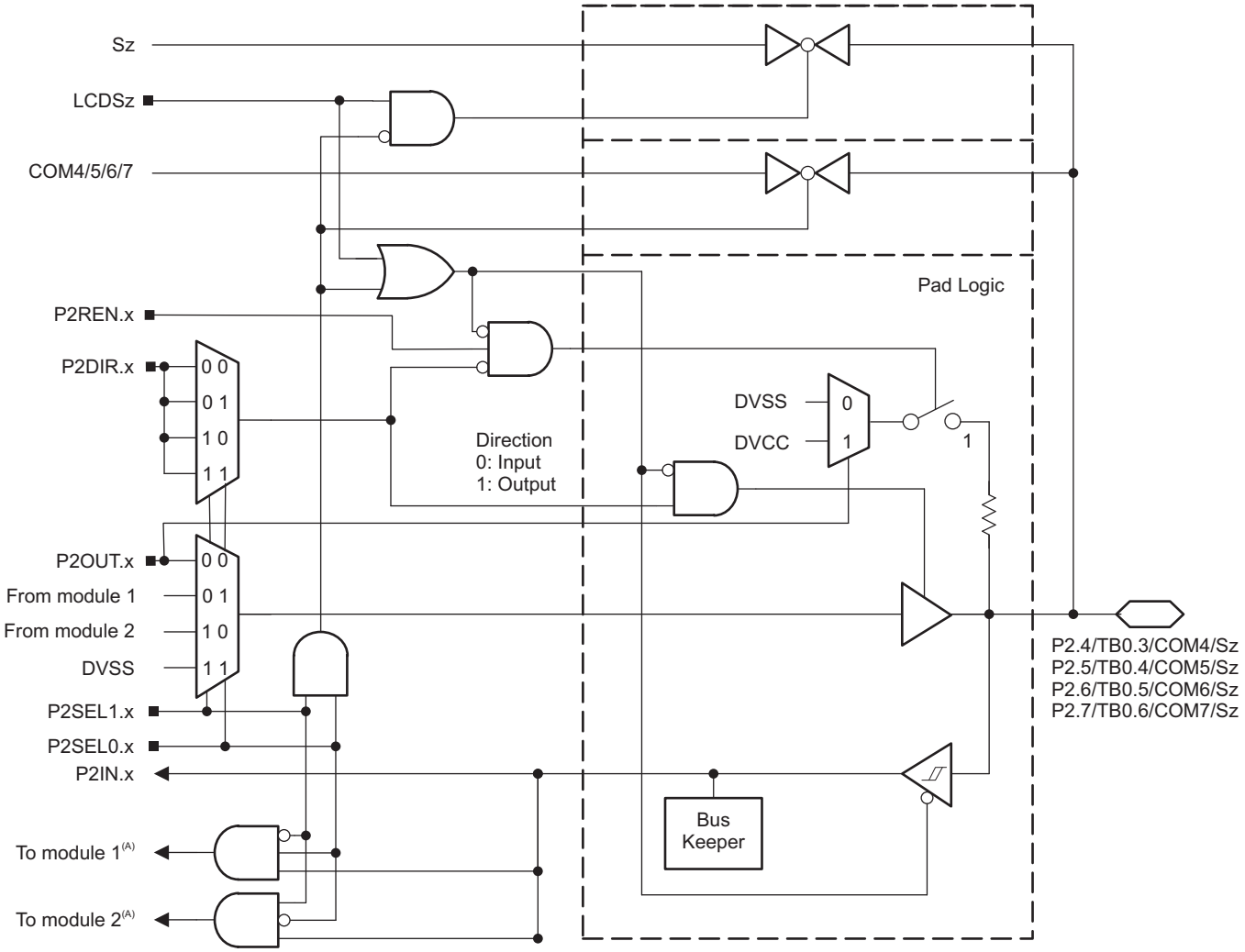
**表 6-22. Port P2 (P2.0 to P2.3) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x | LCDSz |
| P2.0/UCA0SIMO/UCA0TXD/TB0.6/TB0CLK/Sz | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA0SIMO/UCA0TXD | X (2) | 0 | 1 | 0 |
| | | TB0.CCI6B | 0 | 1 | 0 | 0 |
| | | TB0.6 | 1 | | | |
| | | TB0CLK | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P2.1/UCA0SOMI/UCA0RXD/TB0.5/DMAE0/Sz | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA0SOMI/UCA0RXD | X (2) | 0 | 1 | 0 |
| | | TB0.CCI5B | 0 | 1 | 0 | 0 |
| | | TB0.5 | 1 | | | |
| | | DMA0E | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P2.2/UCA0CLK/TB0.4/RTCCLK/Sz | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA0CLK | X (2) | 0 | 1 | 0 |
| | | TB0.CCI4B | 0 | 1 | 0 | 0 |
| | | TB0.4 | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | RTCCLK | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P2.3/UCA0STE/TB0OUTH/Sz | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA0STE | X (2) | 0 | 1 | 0 |
| | | TB0OUTH | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |

(1) X = Don't care
(2) Direction controlled by eUSCI_A0 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

### 6.11.24.6 Port P2 (P2.4 to P2.7) Input/Output With Schmitt Trigger

图 6-5 shows the port diagram. 表 6-23 summarizes the selection of the pin function.




A. The inputs from several pins toward a module are ORed together.
NOTE: Functional representation only.

**图 6-5. Port P2 (P2.4 to P2.7) Diagram**

**表 6-23. Port P2 (P2.4 to P2.7) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x | LCDSz |
| P2.4/TB0.3/COM4/Sz | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TB0.CCI3A | 0 | 0 | 1 | 0 |
| | | TB0.3 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | COM4 | X | 1 | 1 | 0 |
| | | Sz (2) | X | X | X | 1 |
| P2.5/TB0.4/COM5/Sz | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TB0.CCI4A | 0 | 0 | 1 | 0 |
| | | TB0.4 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | COM5 | X | 1 | 1 | 0 |
| | | Sz (2) | X | X | X | 1 |
| P2.6/TB0.5/ESIC1OUT/COM6/Sx | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TB0.CCI5A | 0 | 0 | 1 | 0 |
| | | TB0.5 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | ESIC1OUT | 1 | | | |
| | | COM6 | X | 1 | 1 | 0 |
| | | Sz (2) | X | X | X | 1 |
| P2.7/TB0.6/ESIC2OUT/COM7/Sx | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TB0.CCI6A | 0 | 0 | 1 | 0 |
| | | TB0.6 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | ESIC2OUT | 1 | | | |
| | | COM7 | X | 1 | 1 | 0 |
| | | Sz (2) | X | X | X | 1 |

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

### 6.11.24.7 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

For the pin diagram, see 图 6-2. 表 6-24 and 表 6-25 summarize the selection of the pin function.

**表 6-24. Port P3 (P3.0 to P3.3) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x | LCDSz |
| P3.0/UCB1CLK/Sz | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCB1CLK | X (2) | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P3.1/UCB1SIMO/UCB1SDA/Sz | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCB1SIMO/UCB1SDA | X (2) | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P3.2/UCB1SOMI/UCB1SCL/Sz | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCB1SOMI/UCB1SCL | X (2) | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | | 0 | 1 | 1 | 0 |
| | | | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P3.3/TA1.1/TB0CLK/Sz | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | TA1.CCI1A | 0 | 1 | 0 | 0 |
| | | TA1.1 | 1 | | | |
| | | TB0CLK | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |

(1) X = Don't care
(2) Direction controlled by eUSCI_B1 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

**表 6-25. Port P3 (P3.4 to P3.7) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x | LCDSz |
| P3.4/UCA1SIMO/UCA1TXD/TB0.0/Sz | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA1SIMO/UCA1TXD | X (2) | 0 | 1 | 0 |
| | | TB0CCI0A | 0 | 1 | 0 | 0 |
| | | TB0.0 | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P3.5/UCA1SOMI/UCA1RXD/TB0.1/Sz | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA1SOMI/UCA1RXD | X (2) | 0 | 1 | 0 |
| | | TB0CCI1A | 0 | 1 | 0 | 0 |
| | | TB0.1 | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P3.6/UCA1CLK/TB0.2/Sz | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA1CLK | X (2) | 0 | 1 | 0 |
| | | TB0CCI2A | 0 | 1 | 0 | 0 |
| | | TB0.2 | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P3.7/UCA1STE/TB0.3/Sz | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA1STE | X (2) | 0 | 1 | 0 |
| | | TB0CCI3B | 0 | 1 | 0 | 0 |
| | | TB0.3 | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

### 6.11.24.8 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

For the pin diagram, see 图 6-2. 表 6-26 and 表 6-27 summarize the selection of the pin function.

**表 6-26. Port P4 (P4.0 to P4.3) Pin Functions**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL1.x | P4SEL0.x | LCDSz |
| P4.0/UCB1SIMO/UCB1SDA/MCLK/Sz | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | UCB1SIMO/UCB1SDA | X (2) | 1 | 0 | 0 |
| | | N/A | 0 | 1 | 1 | 0 |
| | | MCLK | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P4.1/UCB1SOMI/UCB1SCL/ACLK/Sz | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | UCB1SOMI/UCB1SCL | X (2) | 1 | 0 | 0 |
| | | N/A | 0 | 1 | 1 | 0 |
| | | ACLK | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P4.2/UCA0SIMO/UCA0TXD/UCB1CLK/Sz | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA0SIMO/UCA0TXD | X (4) | 0 | 1 | 0 |
| | | UCB1CLK | X (2) | 1 | 0 | 0 |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P4.3/UCA0SOMI/UCA0RXD/UCB1STE/Sz | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA0SOMI/UCA0RXD | X (4) | 0 | 1 | 0 |
| | | UCB1STE | X (2) | 1 | 0 | 0 |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |

(1) X = Don't care
(2) Direction controlled by eUSCI_B1 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.
(4) Direction controlled by eUSCI_A0 module.

**表 6-27. Port P4 (P4.4 to P4.7) Pin Functions**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL1.x | P4SEL0.x | LCDSz |
| P4.4/UCB1STE/TA1CLK/Sz | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | UCB1STE | X (2) | 1 | 0 | 0 |
| | | TA1CLK | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P4.5/UCB1CLK/TA1.0/Sz | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | UCB1CLK | X (2) | 1 | 0 | 0 |
| | | TA1CCI0A | 0 | 1 | 1 | 0 |
| | | TA1.0 | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P4.6/UCB1SIMO/UCB1SDA/TA1.1/Sz | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | UCB1SIMO/UCB1SDA | X (2) | 1 | 0 | 0 |
| | | TA1CCI1A | 0 | 1 | 1 | 0 |
| | | TA1.1 | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P4.7/UCB1SOMI/UCB1SCL/TA1.2/Sz | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | UCB1SOMI/UCB1SCL | X (2) | 1 | 0 | 0 |
| | | TA1CCI2A | 0 | 1 | 1 | 0 |
| | | TA1.2 | 1 | | | |
| | | Sz (3) | X | X | X | 1 |

(1) X = Don't care
(2) Direction controlled by eUSCI_B1 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

### 6.11.24.9 Port P5 (P5.0 to P5.7) Input/Output With Schmitt Trigger

For the pin diagram, see 图 6-2. 表 6-28 and 表 6-29 summarize the selection of the pin function.

**表 6-28. Port P5 (P5.0 to P5.3) Pin Functions**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x | LCDSz |
| P5.0/TA1.1/MCLK/Sz | 0 | P5.0 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA1CCI1A | 0 | 0 | 1 | 0 |
| | | TA1.1 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | MCLK | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P5.1/TA1.2/Sz | 1 | P5.1 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA1CCI2A | 0 | 0 | 1 | 0 |
| | | TA1.2 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | N/A | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P5.2/TA1.0/TA1CLK/ACLK/Sz | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA1CCI0B | 0 | 0 | 1 | 0 |
| | | TA1.0 | 1 | | | |
| | | TA1CLK | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | ACLK | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P5.3/UCB1STE/Sz | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | UCB1STE | X (3) | 1 | 0 | 0 |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (2) | X | X | X | 1 |

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.
(3) Direction controlled by eUSCI_B1 module.

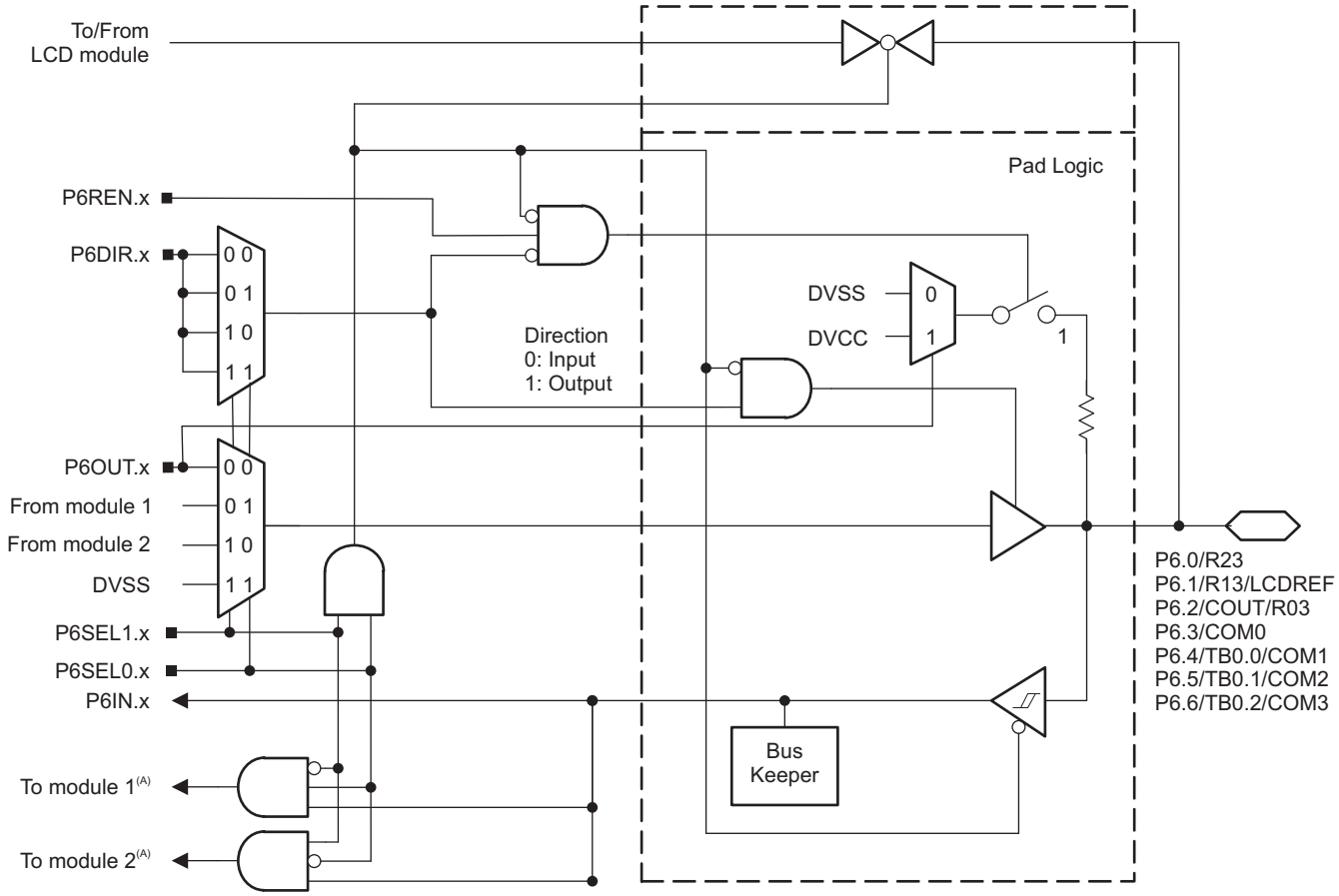
**表 6-29. Port P5 (P5.4 to P5.7) Pin Functions**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x | LCDSz |
| P5.4/UCA1SIMO/UCA1TXD/Sz | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA1SIMO/UCA1TXD | X (2) | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P5.5/UCA1SOMI/UCA1RXD/Sz | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA1SOMI/UCA1RXD | X (2) | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P5.6/UCA1CLK/Sz | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA1CLK | X (2) | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |
| P5.7/UCA1STE/TB0CLK/Sz | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | UCA1STE | X (2) | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | TB0CLK | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (3) | X | X | X | 1 |

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.
(3) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

### 6.11.24.10 Port P6 (P6.0 to P6.6) Input/Output With Schmitt Trigger

图 6-6 shows the port diagram. 表 6-30 and 表 6-31 summarize the selection of the pin function.




A. The inputs from several pins toward a module are ORed together.
NOTE: Functional representation only.

**图 6-6. Port P6 (P6.0 to P6.6) Diagram**

**表 6-30. Port P6 (P6.0 to P6.2) Pin Functions**

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL1.x | P6SEL0.x | LCDSz |
| P6.0/R23 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 | – |
| | | N/A | 0 | 0 | 1 | – |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | – |
| | | Internally tied to DVSS | 1 | | | |
| | | R23 (2) | X | 1 | 1 | – |
| P6.1/R13/LCDREF | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 | – |
| | | N/A | 0 | 0 | 1 | – |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | – |
| | | Internally tied to DVSS | 1 | | | |
| | | R13/LCDREF (2) | X | 1 | 1 | – |
| P6.2/COUT/R03 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 | – |
| | | N/A | 0 | 0 | 1 | – |
| | | COUT | 1 | | | |
| | | N/A | 0 | 1 | 0 | – |
| | | Internally tied to DVSS | 1 | | | |
| | | R03 (2) | X | 1 | 1 | – |

(1) X = Don't care
(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

**表 6-31. Port P6 (P6.3 to P6.6) Pin Functions**

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL1.x | P6SEL0.x | LCDSz |
| P6.3/COM0 | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | 0 | – |
| | | N/A | 0 | 0 | 1 | – |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | – |
| | | Internally tied to DVSS | 1 | | | |
| | | COM0 (2) | X | 1 | 1 | – |
| P6.4/TB0.0/COM1 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 | – |
| | | TB0CCI0B | 0 | 0 | 1 | – |
| | | TB0.0 | 1 | | | |
| | | N/A | 0 | 1 | 0 | – |
| | | Internally tied to DVSS | 1 | | | |
| | | COM1 (2) | X | 1 | 1 | – |
| P6.5/TB0.1/COM2 | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 | – |
| | | TB0CCI1A | 0 | 0 | 1 | – |
| | | TB0.1 | 1 | | | |
| | | N/A | 0 | 1 | 0 | – |
| | | Internally tied to DVSS | 1 | | | |
| | | COM2 (2) | X | 1 | 1 | – |
| P6.6/TB0.2/COM3 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 | – |
| | | TB0CCI2A | 0 | 0 | 1 | – |
| | | TB0.2 | 1 | | | |
| | | N/A | 0 | 1 | 0 | – |
| | | Internally tied to DVSS | 1 | | | |
| | | COM3 (2) | X | 1 | 1 | – |

(1) X = Don't care
(2) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

### 6.11.24.11 Port P6 (P6.7) Input/Output With Schmitt Trigger

For the pin diagram, see 图 6-2. 表 6-32 summarizes the selection of the pin function.

**表 6-32. Port P6 (P6.7) Pin Functions**

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL1.x | P6SEL0.x | LCDSz |
| P6.7/TA0CLK/Sz | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA0CLK | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (2) | X | X | X | 1 |

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

### 6.11.24.12 Port P7 (P7.0 to P7.7) Input/Output With Schmitt Trigger

For the pin diagram, see 图 6-2. 表 6-33 and 表 6-34 summarize the selection of the pin function.

**表 6-33. Port P7 (P7.0 to P7.3) Pin Functions**

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL1.x | P7SEL0.x | LCDSz |
| P7.0/TA0CLK/Sz | 0 | P7.0 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA0CLK | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P7.1/TA0.0/ACLK/Sz | 1 | P7.1 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA0CCI0B | 0 | 0 | 1 | 0 |
| | | TA0.0 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | ACLK | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P7.2/TA0.1/Sz | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA0CCI1A | 0 | 0 | 1 | 0 |
| | | TA0.1 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | N/A | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P7.3/TA0.2/Sz | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA0CCI2A | 0 | 0 | 1 | 0 |
| | | TA0.2 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (2) | X | X | X | 1 |

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

**表 6-34. Port P7 (P7.4 to P7.7) Pin Functions**

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL1.x | P7SEL0.x | LCDSz |
| P7.4/SMCLK/Sz | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | SMCLK | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P7.5/TA0.2/Sz | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA0CCI2A | 0 | 0 | 1 | 0 |
| | | TA0.2 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P7.6/TA0.1/Sz | 6 | P7.6 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA0CCI1A | 0 | 0 | 1 | 0 |
| | | TA0.1 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P7.7/TA1.2/TB0OUTH/Sz | 7 | P7.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | TA1.CCI2A | 0 | 1 | 0 | 0 |
| | | TA1.2 | 1 | | | |
| | | TB0OUTH | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (2) | X | X | X | 1 |

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

### 6.11.24.13 Port P8 (P8.0 to P8.3) Input/Output With Schmitt Trigger

For the pin diagram, see 图 6-2. 表 6-35 summarizes the selection of the pin function.

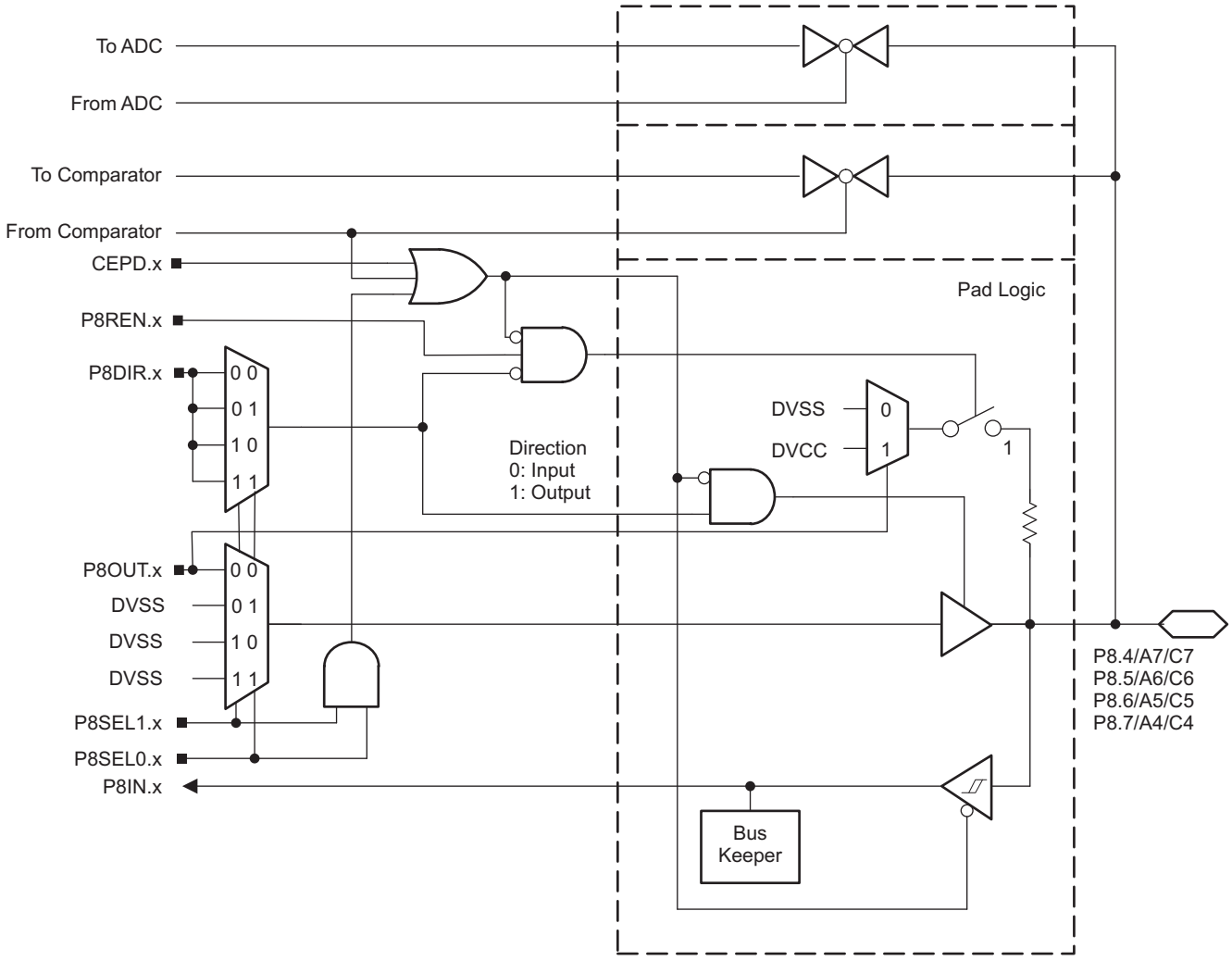
**表 6-35. Port P8 (P8.0 to P8.3) Pin Functions**

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL1.x | P8SEL0.x | LCDSz |
| P8.0/RTCCLK/Sz | 0 | P8.0 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | RTCCLK | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P8.1/DMAE0/Sz | 1 | P8.1 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | DMA0E | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P8.2/Sz | 2 | P8.2 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P8.3/MCLK/Sz | 3 | P8.3 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | MCLK | 1 | | | |
| | | Sz (2) | X | X | X | 1 |

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

### 6.11.24.14 Port P8 (P8.4 to P8.7) Input/Output With Schmitt Trigger

图 6-7 shows the port diagram. 表 6-36 summarizes the selection of the pin function.




NOTE: Functional representation only.

**图 6-7. Port P8 (P8.4 to P8.7) Diagram**

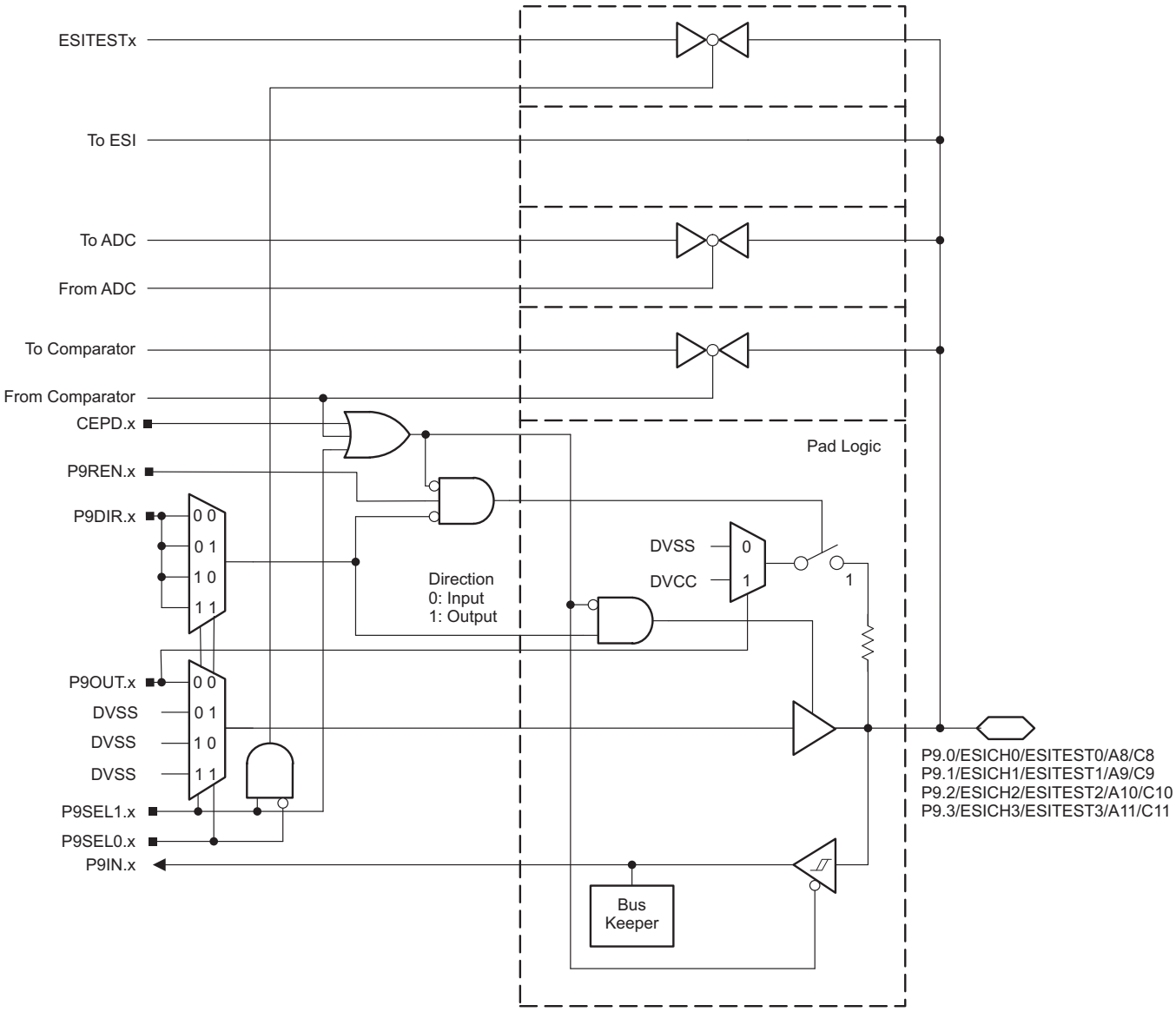
**表 6-36. Port P8 (P8.4 to P8.7) Pin Functions**

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | |
|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL1.x | P8SEL0.x |
| P8.4/A7/C7 | 4 | P8.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | |
| | | A7/C7 (2) (3) | X | 1 | 1 |
| P8.5/A6/C6 | 5 | P8.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | |
| | | A6/C6 (2) (3) | X | 1 | 1 |
| P8.6/A5/C5 | 6 | P8.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | |
| | | A5/C5 (2) (3) | X | 1 | 1 |
| P8.7/A4/C4 | 7 | P8.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | |
| | | A4/C4 (2) (3) | X | 1 | 1 |

(1) X = Don't care
(2) Setting P8SEL1.x and P8SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.

### 6.11.24.15 Port P9 (P9.0 to P9.3) Input/Output With Schmitt Trigger

图 6-8 shows the port diagram. 表 6-37 summarizes the selection of the pin function.




NOTE: Functional representation only.

**图 6-8. Port P9 (P9.0 to P9.3) Diagram**

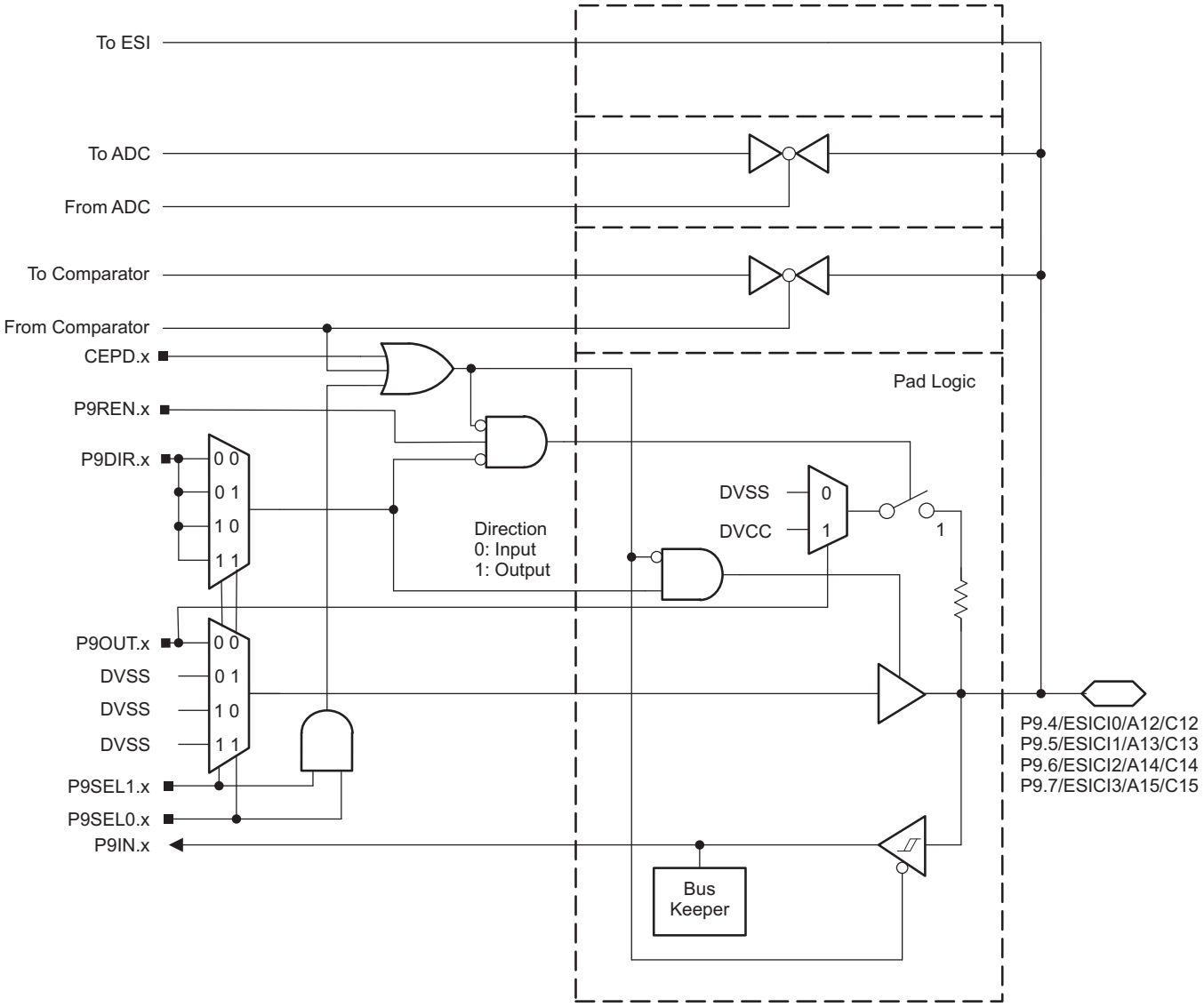
**表 6-37. Port P9 (P9.0 to P9.3) Pin Functions**

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | |
|---|---|---|---|---|---|
| | | | P9DIR.x | P9SEL1.x | P9SEL0.x |
| P9.0/ESICH0/ESITEST0/A8/C8 | 0 | P9.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | ESITEST0 (2) | X | 1 | 0 |
| | | ESICH0/A8/C8 (2)(3)(4) | X | 1 | 1 |
| P9.1/ESICH1/ESITEST1/A9/C9 | 1 | P9.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | ESITEST1 (2) | X | 1 | 0 |
| | | ESICH1/A9/C9 (2)(3)(4) | X | 1 | 1 |
| P9.2/ESICH2/ESITEST2/A10/C10 | 2 | P9.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | ESITEST2 (2) | X | 1 | 0 |
| | | ESICH2/A10/C10 (2)(3)(4) | X | 1 | 1 |
| P9.3/ESICH3/ESITEST3/A11/C11 | 3 | P9.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | ESITEST3 (2) | X | 1 | 0 |
| | | ESICH3/A11/C11 (2) (3)(4) | X | 1 | 1 |

(1) X = Don't care
(2) Setting P9SEL1.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.
(4) Depending on the configuration of the ESI module other ESICHx pins are stimulated as well and thus should have the input Schmitt triggers disabled (with P9SEL1.x = 1) and cannot be used as digital I/O, ADC or comparator inputs.

### 6.11.24.16 Port P9 (P9.4 to P9.7) Input/Output With Schmitt Trigger

图 6-9 shows the port diagram. 表 6-38 summarizes the selection of the pin function.




NOTE: Functional representation only.

**图 6-9. Port P9 (P9.4 to P9.7) Diagram**

**表 6-38. Port P9 (P9.4 to P9.7) Pin Functions**

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | |
|---|---|---|---|---|---|
| | | | P9DIR.x | P9SEL1.x | P9SEL0.x |
| P9.4/ESICI0/A12/C12 | 4 | P9.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | |
| | | ESICI0/A12/C12 (2) (3)(4) | X | 1 | 1 |
| P9.5/ESICI1/A13/C13 | 5 | P9.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | |
| | | ESICI1/A13/C13 (2) (3)(4) | X | 1 | 1 |
| P9.6/ESICI2/A14/C14 | 6 | P9.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | |
| | | ESICI2/A14/C14 (2) (3)(4) | X | 1 | 1 |
| P9.7/ESICI3/A15/C15 | 7 | P9.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | Internally tied to DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | |
| | | ESICI3/A15/C15 (2) (3)(4) | X | 1 | 1 |

(1) X = Don't care
(2) Setting P9SEL1.x and P9SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.
(4) Depending on the configuration of the ESI module, other ESICI2/ pins are used, and thus should have the input Schmitt triggers disabled (with P9SEL1.x = 1 and P9SEL0.x = 1) and cannot be used as digital I/O, ADC, or comparator inputs.

### 6.11.24.17 Port P10 (P10.0 to P10.2) Input/Output With Schmitt Trigger

For the pin diagram, see 图 6-2. 表 6-39 summarizes the selection of the pin function.

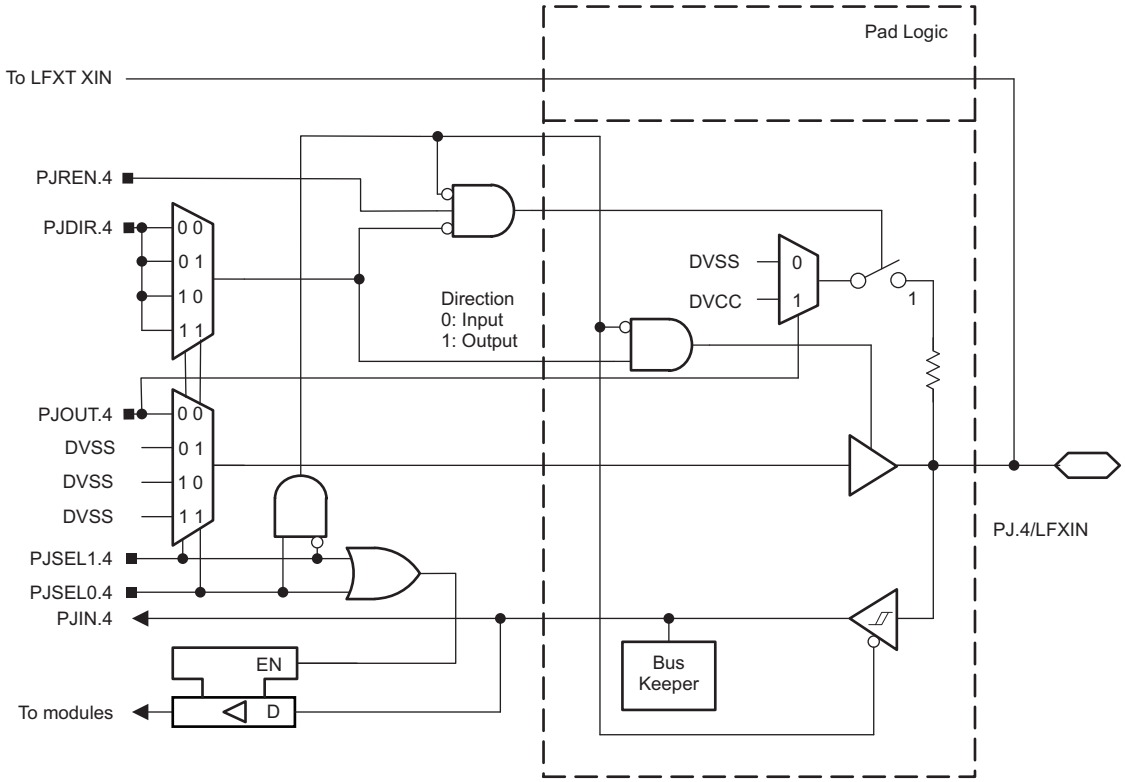
**表 6-39. Port P10 (P10.0 to P10.2) Pin Functions**

| PIN NAME (P10.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | |
|---|---|---|---|---|---|---|
| | | | P10DIR.x | P10SEL1.x | P10SEL0.x | LCDSz |
| P10.0/SMCLK/Sz | 0 | P10.0 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | N/A | 0 | 0 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | SMCLK | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P10.1/TA0.0/Sz | 1 | P10.1 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA0.CCI0B | 0 | 0 | 1 | 0 |
| | | TA0.0 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | Sz (2) | X | X | X | 1 |
| P10.2/TA1.0/SMCLK/Sz | 2 | P10.2 (I/O) | I: 0; O: 1 | 0 | 0 | 0 |
| | | TA1.CCI0B | 0 | 0 | 1 | 0 |
| | | TA1.0 | 1 | | | |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Internally tied to DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | 0 |
| | | SMCLK | 1 | | | |
| | | Sz (2) | X | X | X | 1 |

(1) X = Don't care
(2) The associated LCD segment is package dependent. See the Signal Descriptions tables and Pin Diagrams figures.

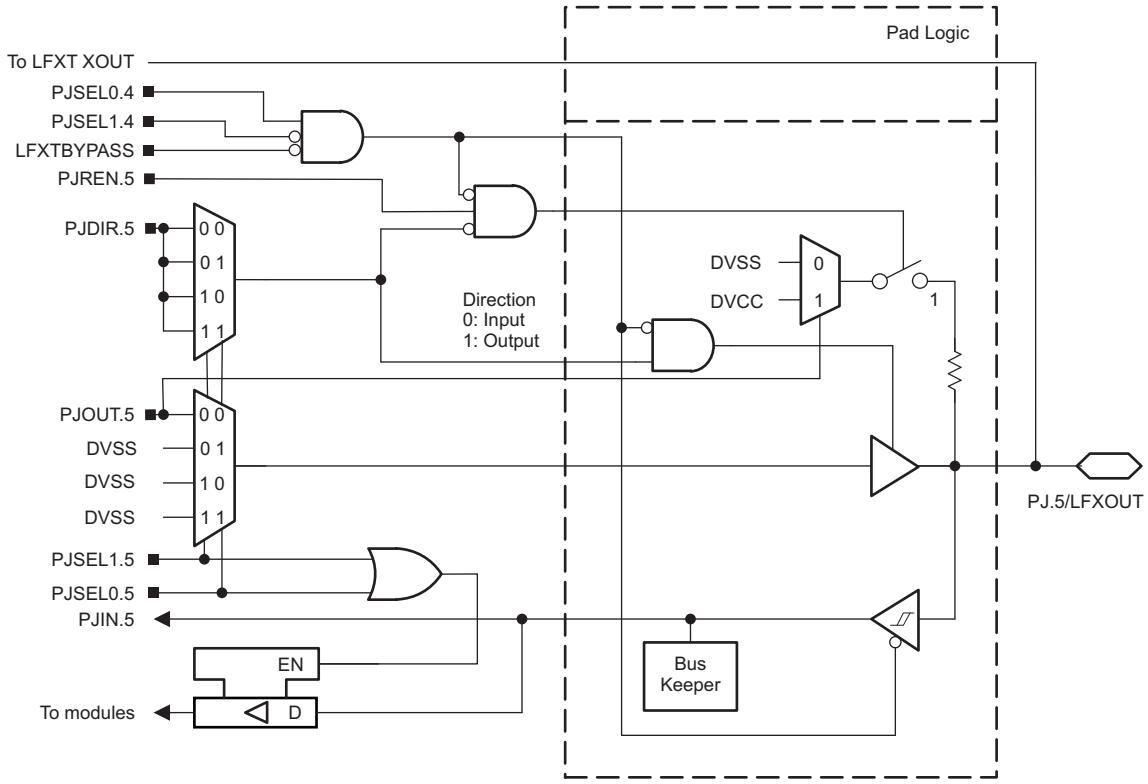
### 6.11.24.18 Port PJ (PJ.4 and PJ.5) Input/Output With Schmitt Trigger

图 6-10 and 图 6-11 show the port diagrams. 表 6-40 summarizes the selection of the pin function.




NOTE: Functional representation only.

**图 6-10. Port PJ (PJ.4) Diagram**




NOTE: Functional representation only.

**图 6-11. Port PJ (PJ.5) Diagram**

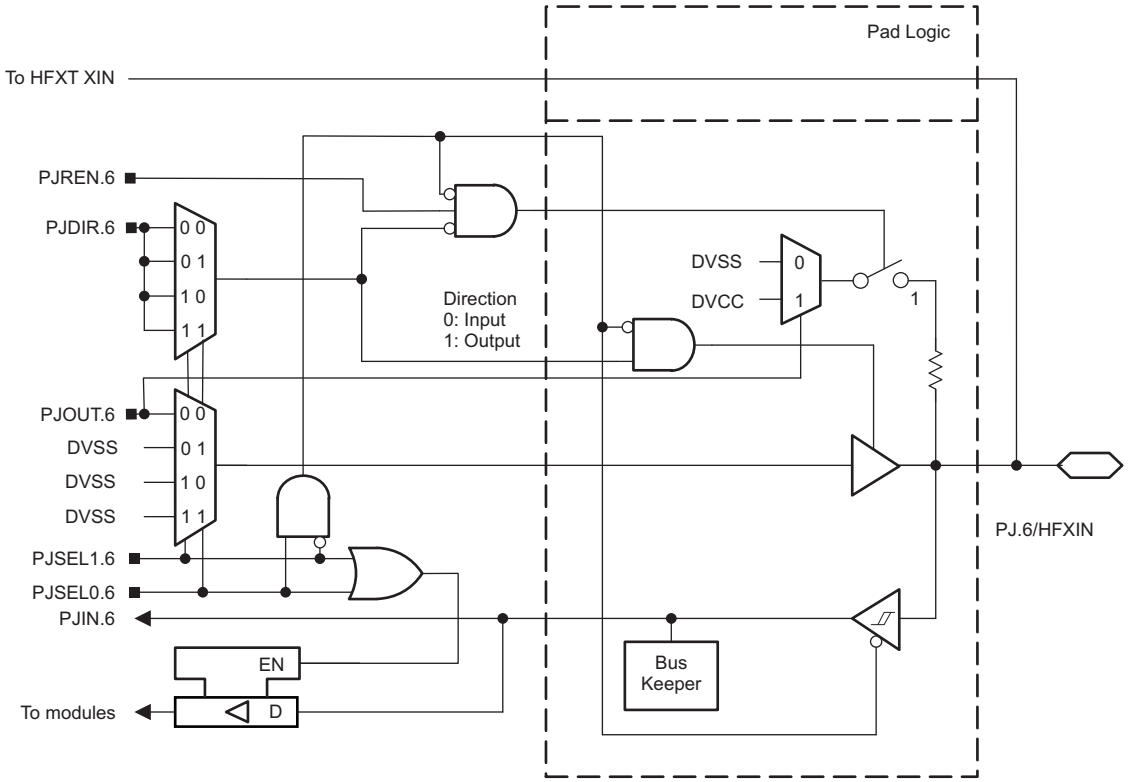
## 表 6-40. Port PJ (PJ.4 and PJ.5) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.5 | PJSEL0.5 | PJSEL1.4 | PJSEL0.4 | LFXT BYPASS |
| PJ.4/LFXIN | 4 | PJ.4 (I/O) | I: 0; O: 1 | X | X | 0 | 0 | X |
| | | N/A | 0 | X | X | 1 | X | X |
| | | Internally tied to DVSS | 1 | | | | | |
| | | LFXIN crystal mode (2) | X | X | X | 0 | 1 | 0 |
| | | LFXIN bypass mode (2) | X | X | X | 0 | 1 | 1 |
| PJ.5/LFXOUT | 5 | PJ.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1 (3) |
| | | N/A | 0 | see (4) | see (4) | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1 (3) |
| | | Internally tied to DVSS | 1 | see (4) | see (4) | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1 (3) |
| | | LFXOUT crystal mode (2) | X | X | X | 0 | 1 | 0 |

(1) X = Don't care
(2) Setting PJSEL1.4 = 0 and PJSEL0.4 = 1 causes the general-purpose I/O to be disabled. When LFXTBYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are don't care. When LFXTBYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.
(3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.
(4) With PJSEL0.5 = 1 or PJSEL1.5 =1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.

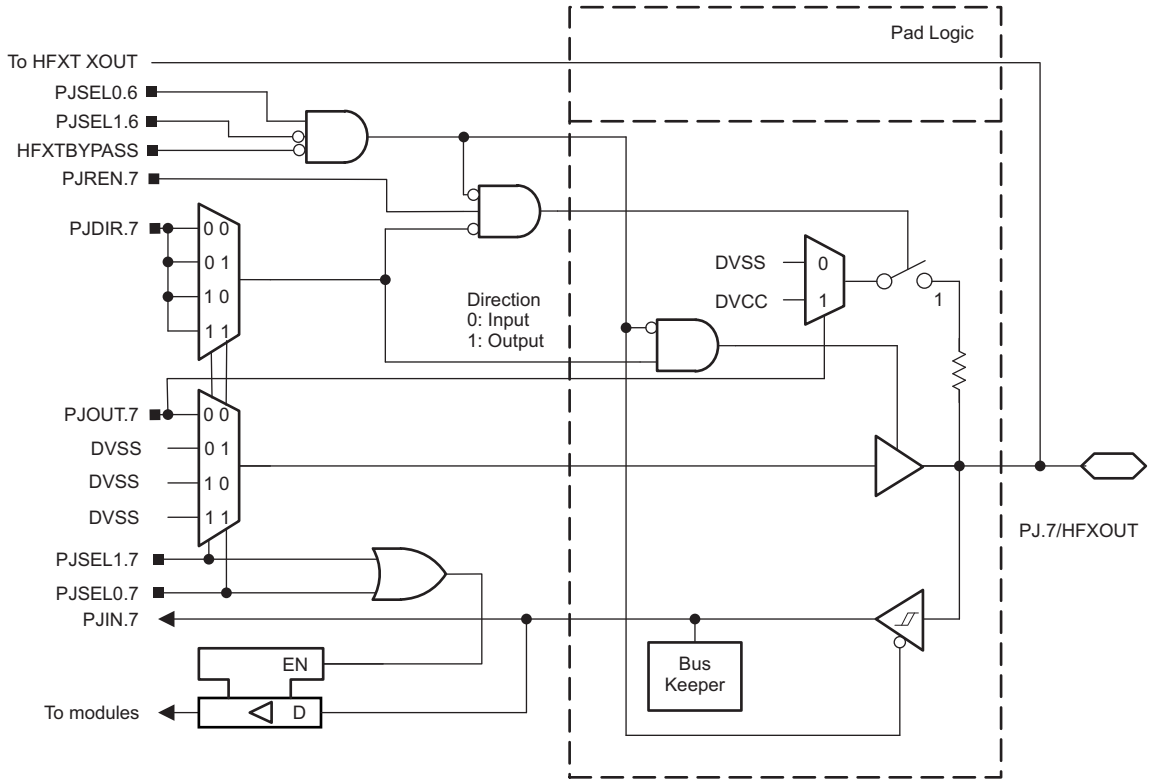
### 6.11.24.19 Port PJ (PJ.6 and PJ.7) Input/Output With Schmitt Trigger

图 6-12 and 图 6-13 show the port diagrams. 表 6-41 summarizes the selection of the pin function.




NOTE: Functional representation only.

**图 6-12. Port PJ (PJ.6) Diagram**




NOTE: Functional representation only.

**图 6-13. Port PJ (PJ.7) Diagram**

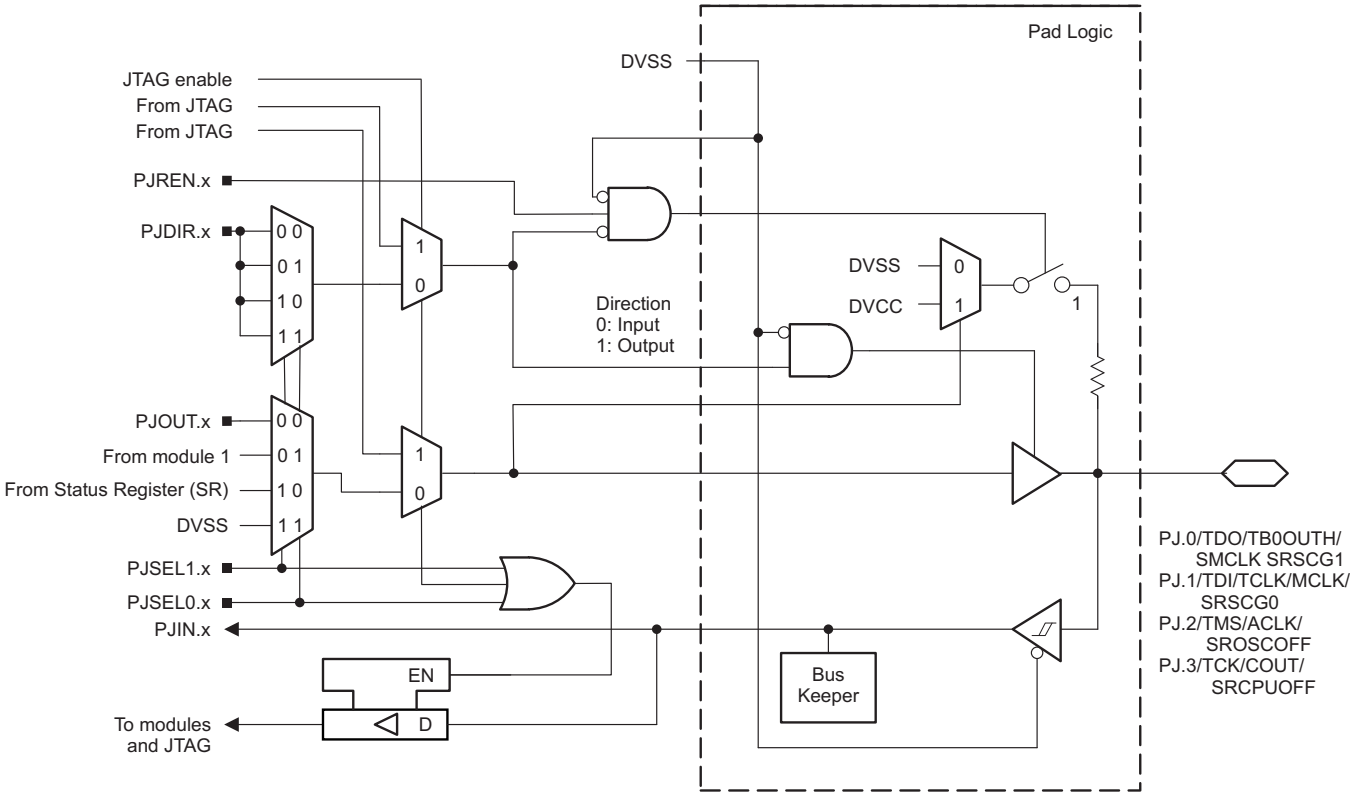
**表 6-41. Port PJ (PJ.6 and PJ.7) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS AND SIGNALS (1) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.7 | PJSEL0.7 | PJSEL1.6 | PJSEL0.6 | HFXT BYPASS |
| PJ.6/HFXIN | 6 | PJ.6 (I/O) | I: 0; O: 1 | X | X | 0 | 0 | X |
| | | N/A | 0 | X | X | 1 | X | X |
| | | Internally tied to DVSS | 1 | | | | | |
| | | HFXIN crystal mode (2) | X | X | X | 0 | 1 | 0 |
| | | HFXIN bypass mode (2) | X | X | X | 0 | 1 | 1 |
| PJ.7/HFXOUT | 7 | PJ.7 (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1 (3) |
| | | N/A | 0 | see (4) | see (4) | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1 (3) |
| | | Internally tied to DVSS | 1 | see (4) | see (4) | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1 (3) |
| | | HFXOUT crystal mode (2) | X | X | X | 0 | 1 | 0 |

(1) X = Don't care
(2) Setting PJSEL1.6 = 0 and PJSEL0.6 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.6 and PJ.7 are configured for crystal operation and PJSEL1.6 and PJSEL0.7 are don't care. When HFXTBYPASS = 1, PJ.6 is configured for bypass operation and PJ.7 is configured as general-purpose I/O.
(3) When PJ.6 is configured in bypass mode, PJ.7 is configured as general-purpose I/O.
(4) With PJSEL0.7 = 1 or PJSEL1.7 =1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.

### 6.11.24.20 Port PJ (PJ.0 to PJ.3) JTAG Pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger

图 6-14 shows the port diagram. 表 6-42 summarizes the selection of the pin function.




NOTE: Functional representation only.

**图 6-14. Port PJ (PJ.0 to PJ.3) Diagram**

**表 6-42. Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS (1) | | |
|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.x | PJSEL0.x |
| PJ.0/TDO/TB0OUTH/ SMCLK/SRSCG1 | 0 | PJ.0 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TDO (3) | X | X | X |
| | | TB0OUTH | 0 | 0 | 1 |
| | | SMCLK(4) | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | CPU Status Register Bit SCG1 | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | Internally tied to DVSS | 1 | | |
| PJ.1/TDI/TCLK/ MCLK/SRSCG0 | 1 | PJ.1 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TDI/TCLK (3) (5) | X | X | X |
| | | N/A | 0 | 0 | 1 |
| | | MCLK | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | CPU Status Register Bit SCG0 | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | Internally tied to DVSS | 1 | | |
| PJ.2/TMS/ACLK/ SROSCOFF | 2 | PJ.2 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TMS (3) (5) | X | X | X |
| | | N/A | 0 | 0 | 1 |
| | | ACLK | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | CPU Status Register Bit OSCOFF | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | Internally tied to DVSS | 1 | | |
| PJ.3/TCK/COUT/ SRCPUOFF | 3 | PJ.3 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TCK (3) (5) | X | X | X |
| | | N/A | 0 | 0 | 1 |
| | | COUT | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | CPU Status Register Bit CPUOFF | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | Internally tied to DVSS | 1 | | |

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made through the SYS module or by the Spy-Bi-Wire 4-wire entry sequence. Neither PJSEL1.x and PJSEL0.x nor CEPD.x bits have an effect in these cases.
(4) Do not use this pin as SMCLK output if the TB0OUTH functionality is used on any other pin. Select an alternative SMCLK output pin.
(5) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

## 6.12 Device Descriptors (TLV)

表 6-43 summarizes the Device IDs. 表 6-44 lists the contents of the device descriptor tag-length-value (TLV) structure for each device type.

**表 6-43. Device ID**

| DEVICE | DEVICE ID | |
|---|---|---|
| | 01A05h | 01A04h |
| MSP430FR6989 | 081h | 0A8h |
| MSP430FR6988 | 081h | 0A7h |
| MSP430FR6987 | 081h | 0A6h |
| MSP430FR5989 | 081h | 0ABh |
| MSP430FR5988 | 081h | 0AAh |
| MSP430FR5987 | 081h | 0A9h |
| MSP430FR5986 | 081h | 0DFh |
| MSP430FR69891 | 081h | 0A8h |
| MSP430FR59891 | 081h | 0ABh |

## 表 6-44. Device Descriptor Table (1)

| DESCRIPTION | | MSP430FRxxxx (UART BSL) | | MSP430FRxxxx1 ($I^2C$ BSL) | |
|---|---|---|---|---|---|
| | | ADDRESS | VALUE | ADDRESS | VALUE |
| Info Block | Info length | 01A00h | 06h | 01A00h | 06h |
| | CRC length | 01A01h | 06h | 01A01h | 06h |
| | CRC value | 01A02h | Per unit | 01A02h | Per unit |
| | | 01A03h | Per unit | 01A03h | Per unit |
| | Device ID | 01A04h | See 表 6-43. | 01A04h | See 表 6-43. |
| | | 01A05h | | 01A05h | |
| | Hardware revision | 01A06h | Per unit | 01A06h | Per unit |
| | Firmware revision | 01A07h | Per unit | 01A07h | Per unit |
| Die Record | Die record tag | 01A08h | 08h | 01A08h | 08h |
| | Die record length | 01A09h | 0Ah | 01A09h | 0Ah |
| | Lot/wafer ID | 01A0Ah | Per unit | 01A0Ah | Per unit |
| | | 01A0Bh | Per unit | 01A0Bh | Per unit |
| | | 01A0Ch | Per unit | 01A0Ch | Per unit |
| | | 01A0Dh | Per unit | 01A0Dh | Per unit |
| | Die X position | 01A0Eh | Per unit | 01A0Eh | Per unit |
| | | 01A0Fh | Per unit | 01A0Fh | Per unit |
| | Die Y position | 01A10h | Per unit | 01A10h | Per unit |
| | | 01A11h | Per unit | 01A11h | Per unit |
| | Test results | 01A12h | Per unit | 01A12h | Per unit |
| | | 01A13h | Per unit | 01A13h | Per unit |
| ADC12B Calibration | ADC12B calibration tag | 01A14h | 11h | 01A14h | 11h |
| | ADC12B calibration length | 01A15h | 10h | 01A15h | 10h |
| | ADC gain factor(2) | 01A16h | Per unit | 01A16h | Per unit |
| | | 01A17h | Per unit | 01A17h | Per unit |
| | ADC offset(3) | 01A18h | Per unit | 01A18h | Per unit |
| | | 01A19h | Per unit | 01A19h | Per unit |
| | ADC 1.2-V reference Temperature sensor 30°C | 01A1Ah | Per unit | 01A1Ah | Per unit |
| | | 01A1Bh | Per unit | 01A1Bh | Per unit |
| | ADC 1.2-V reference Temperature sensor 85°C | 01A1Ch | Per unit | 01A1Ch | Per unit |
| | | 01A1Dh | Per unit | 01A1Dh | Per unit |
| | ADC 2.0-V reference Temperature sensor 30°C | 01A1Eh | Per unit | 01A1Eh | Per unit |
| | | 01A1Fh | Per unit | 01A1Fh | Per unit |
| | ADC 2.0-V reference Temperature sensor 85°C | 01A20h | Per unit | 01A20h | Per unit |
| | | 01A21h | Per unit | 01A21h | Per unit |
| | ADC 2.5-V reference Temperature sensor 30°C | 01A22h | Per unit | 01A22h | Per unit |
| | | 01A23h | Per unit | 01A23h | Per unit |
| | ADC 2.5-V reference Temperature sensor 85°C | 01A24h | Per unit | 01A24h | Per unit |
| | | 01A25h | Per unit | 01A25h | Per unit |

(1) NA = Not applicable, Per unit = Content can differ from device to device
(2) ADC gain: The gain correction factor is measured using the internal voltage reference with REFOUT = 0. Other settings (for example, with REFOUT = 1) can result in different correction factors.
(3) ADC offset: The offset correction factor is measured using the internal 2.5-V reference.

**表 6-44. Device Descriptor Table (1) (continued)**

| DESCRIPTION | | MSP430FRxxxx (UART BSL) | | MSP430FRxxxx1 ($I^2C$ BSL) | |
|---|---|---|---|---|---|
| | | ADDRESS | VALUE | ADDRESS | VALUE |
| REF Calibration | REF calibration tag | 01A26h | 12h | 01A26h | 12h |
| | REF calibration length | 01A27h | 06h | 01A27h | 06h |
| | REF 1.2-V reference | 01A28h | Per unit | 01A28h | Per unit |
| | | 01A29h | Per unit | 01A29h | Per unit |
| | REF 2.0-V reference | 01A2Ah | Per unit | 01A2Ah | Per unit |
| | | 01A2Bh | Per unit | 01A2Bh | Per unit |
| | REF 2.5-V reference | 01A2Ch | Per unit | 01A2Ch | Per unit |
| | | 01A2Dh | Per unit | 01A2Dh | Per unit |
| Random Number | 128-bit random number tag | 01A2Eh | 15h | 01A2Eh | 15h |
| | Random number length | 01A2Fh | 10h | 01A2Fh | 10h |
| | 128-bit random number (4) | 01A30h | Per unit | 01A30h | Per unit |
| | | 01A31h | Per unit | 01A31h | Per unit |
| | | 01A32h | Per unit | 01A32h | Per unit |
| | | 01A33h | Per unit | 01A33h | Per unit |
| | | 01A34h | Per unit | 01A34h | Per unit |
| | | 01A35h | Per unit | 01A35h | Per unit |
| | | 01A36h | Per unit | 01A36h | Per unit |
| | | 01A37h | Per unit | 01A37h | Per unit |
| | | 01A38h | Per unit | 01A38h | Per unit |
| | | 01A39h | Per unit | 01A39h | Per unit |
| | | 01A3Ah | Per unit | 01A3Ah | Per unit |
| | | 01A3Bh | Per unit | 01A3Bh | Per unit |
| | | 01A3Ch | Per unit | 01A3Ch | Per unit |
| | | 01A3Dh | Per unit | 01A3Dh | Per unit |
| | | 01A3Eh | Per unit | 01A3Eh | Per unit |
| | | 01A3Fh | Per unit | 01A3Fh | Per unit |
| BSL Configuration | BSL tag | 01A40h | 1Ch | 01A40h | 1Ch |
| | BSL length | 01A41h | 02h | 01A41h | 02h |
| | BSL interface | 01A42h | 00h | 01A42h | 01h |
| | BSL interface configuration | 01A43h | 00h | 01A43h | 48h |

(4) 128-bit random number: The random number is generated during production test using the CryptGenRandom() function from Microsoft®.

## 6.13 Memory

表 6-45 summarizes the memory map.

**表 6-45. Memory Organization(1)**

| | | MSP430FRxxx9(1) | MSP430FRxxx8(1) | MSP430FRxxx7(1) | MSP430FRxxx6(1) |
|---|---|---|---|---|---|
| Memory (FRAM)<br>Main: interrupt vectors and signatures<br>Main: code memory | Total Size | 127KB<br>00FFFFh–00FF80h<br>023FFFh–004400h | 95KB<br>00FFFFh–00FF80h<br>01BFFFh–004400h | 63KB<br>00FFFFh–00FF80h<br>013FFFh–004400h | 47KB<br>00FFFFh–00FF80h<br>0FF7Fh–004400h |
| RAM | Sect 1 | 2KB<br>0023FFh–001C00h | 2KB<br>0023FFh–001C00h | 2KB<br>0023FFh–001C00h | 2KB<br>0023FFh–001C00h |
| Boot memory (ROM) | | 256 B<br>001BFFh–001B00h | 256 B<br>001BFFh–001B00h | 256 B<br>001BFFh–001B00h | 256 B<br>001BFFh–001B00h |
| Device Descriptor Info (TLV) | | 256 B<br>001AFFh–001A00h | 256 B<br>001AFFh–001A00h | 256 B<br>001AFFh–001A00h | 256 B<br>001AFFh–001A00h |
| Information memory (FRAM) | Info A | 128 B<br>0019FFh–001980h | 128 B<br>0019FFh–001980h | 128 B<br>0019FFh–001980h | 128 B<br>0019FFh–001980h |
| | Info B | 128 B<br>00197Fh–001900h | 128 B<br>00197Fh–001900h | 128 B<br>00197Fh–001900h | 128 B<br>00197Fh–001900h |
| | Info C | 128 B<br>0018FFh–001880h | 128 B<br>0018FFh–001880h | 128 B<br>0018FFh–001880h | 128 B<br>0018FFh–001880h |
| | Info D | 128 B<br>00187Fh–001800h | 128 B<br>00187Fh–001800h | 128 B<br>00187Fh–001800h | 128 B<br>00187Fh–001800h |
| Bootloader (BSL) memory (ROM) | BSL 3 | 512 B<br>0017FFh–001600h | 512 B<br>0017FFh–001600h | 512 B<br>0017FFh–001600h | 512 B<br>0017FFh–001600h |
| | BSL 2 | 512 B<br>0015FFh–001400h | 512 B<br>0015FFh–001400h | 512 B<br>0015FFh–001400h | 512 B<br>0015FFh–001400h |
| | BSL 1 | 512 B<br>0013FFh–001200h | 512 B<br>0013FFh–001200h | 512 B<br>0013FFh–001200h | 512 B<br>0013FFh–001200h |
| | BSL 0 | 512 B<br>0011FFh–001000h | 512 B<br>0011FFh–001000h | 512 B<br>0011FFh–001000h | 512 B<br>0011FFh–001000h |
| Peripherals | Size | 4KB<br>000FFFh–000020h | 4KB<br>000FFFh–000020h | 4KB<br>000FFFh–000020h | 4KB<br>000FFFh–000020h |
| Tiny RAM | Size | 26 B<br>000001Fh–000006h | 26 B<br>000001Fh–000006h | 26 B<br>000001Fh–000006h | 26 B<br>000001Fh–000006h |
| Reserved (ROM) | Size | 6 B<br>000005h–000000h | 6 B<br>000005h–000000h | 6 B<br>000005h–000000h | 6 B<br>000005h–000000h |

(1) All address space not listed is considered vacant memory.

### 6.13.1 Peripheral File Map

表 6-46 lists the base address for each available peripheral. 表 6-47 through 表 6-82 list the registers and their offsets for each peripheral.

**表 6-46. Peripherals**

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|---|---|---|
| Special Functions (see 表 6-47) | 0100h | 000h–01Fh |
| PMM (see 表 6-48) | 0120h | 000h–01Fh |
| FRAM Control (see 表 6-49) | 0140h | 000h–00Fh |
| CRC16 (see 表 6-50) | 0150h | 000h–007h |
| RAM Controller (see 表 6-51) | 0158h | 000h–001h |
| Watchdog Timer (see 表 6-52) | 015Ch | 000h–001h |
| CS (see 表 6-53) | 0160h | 000h–00Fh |
| SYS (see 表 6-54) | 0180h | 000h–01Fh |
| Shared Reference (see 表 6-55) | 01B0h | 000h–001h |
| Port P1, P2 (see 表 6-56) | 0200h | 000h–01Fh |
| Port P3, P4 (see 表 6-57) | 0220h | 000h–01Fh |
| Port P5, P6 (see 表 6-58) | 0240h | 000h–01Fh |
| Port P7, P8 (see 表 6-59) | 0260h | 000h–01Fh |
| Port P9, P10 (see 表 6-60) | 0280h | 000h–01Fh |
| Port PJ (see 表 6-61) | 0320h | 000h–01Fh |
| Timer_A TA0 (see 表 6-62) | 0340h | 000h–02Fh |
| Timer_A TA1 (see 表 6-63) | 0380h | 000h–02Fh |
| Timer_B TB0 (see 表 6-64) | 03C0h | 000h–02Fh |
| Timer_A TA2 (see 表 6-65) | 0400h | 000h–02Fh |
| Capacitive Touch I/O 0 (see 表 6-66) | 0430h | 000h–00Fh |
| Timer_A TA3 (see 表 6-67) | 0440h | 000h–02Fh |
| Capacitive Touch I/O 1 (see 表 6-68) | 0470h | 000h–00Fh |
| Real-Time Clock (RTC_C) (see 表 6-69) | 04A0h | 000h–01Fh |
| 32-Bit Hardware Multiplier (see 表 6-70) | 04C0h | 000h–02Fh |
| DMA General Control (see 表 6-71) | 0500h | 000h–00Fh |
| DMA Channel 0 (see 表 6-71) | 0510h | 000h–00Fh |
| DMA Channel 1 (see 表 6-71) | 0520h | 000h–00Fh |
| DMA Channel 2 (see 表 6-71) | 0530h | 000h–00Fh |
| MPU (see 表 6-72) | 05A0h | 000h–00Fh |
| eUSCI_A0 (see 表 6-73) | 05C0h | 000h–01Fh |
| eUSCI_A1 (see 表 6-74) | 05E0h | 000h–01Fh |
| eUSCI_B0 (see 表 6-75) | 0640h | 000h–02Fh |
| eUSCI_B1 (see 表 6-76) | 0680h | 000h–02Fh |
| ADC12_B (see 表 6-77) | 0800h | 000h–09Fh |
| Comparator_E (see 表 6-78) | 08C0h | 000h–00Fh |
| CRC32 (see 表 6-79) | 0980h | 000h–02Fh |
| AES (see 表 6-80) | 09C0h | 000h–00Fh |
| LCD_C (see 表 6-81) | 0A00h | 000h–05Fh |
| ESI (see 表 6-82) | 0D00h | 000h–09Fh |
| ESI RAM (128 bytes) | 0E00h | 00h–07Fh |

**表 6-47. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

**表 6-48. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| PMM control 0 | PMMCTL0 | 00h |
| PMM interrupt flags | PMMIFG | 0Ah |
| PM5 control 0 | PM5CTL0 | 10h |

**表 6-49. FRAM Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| FRAM control 0 | FRCTL0 | 00h |
| General control 0 | GCCTL0 | 04h |
| General control 1 | GCCTL1 | 06h |

**表 6-50. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

**表 6-51. RAM Controller Registers (Base Address: 0158h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RAM controller control 0 | RCCTL0 | 00h |

**表 6-52. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Watchdog timer control | WDTCTL | 00h |

**表 6-53. CS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CS control 0 | CSCTL0 | 00h |
| CS control 1 | CSCTL1 | 02h |
| CS control 2 | CSCTL2 | 04h |
| CS control 3 | CSCTL3 | 06h |
| CS control 4 | CSCTL4 | 08h |
| CS control 5 | CSCTL5 | 0Ah |
| CS control 6 | CSCTL6 | 0Ch |

**表 6-54. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| System control | SYSCTL | 00h |
| JTAG mailbox control | SYSJMBC | 06h |

**表 6-54. SYS Registers (Base Address: 0180h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

**表 6-55. Shared Reference Registers (Base Address: 01B0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Shared reference control | REFCTL | 00h |

**表 6-56. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 resistor enable | P1REN | 06h |
| Port P1 selection 0 | P1SEL0 | 0Ah |
| Port P1 selection 1 | P1SEL1 | 0Ch |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 complement selection | P1SELC | 16h |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 resistor enable | P2REN | 07h |
| Port P2 selection 0 | P2SEL0 | 0Bh |
| Port P2 selection 1 | P2SEL1 | 0Dh |
| Port P2 complement selection | P2SELC | 17h |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

**表 6-57. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 resistor enable | P3REN | 06h |
| Port P3 selection 0 | P3SEL0 | 0Ah |
| Port P3 selection 1 | P3SEL1 | 0Ch |
| Port P3 interrupt vector word | P3IV | 0Eh |

**表 6-57. Port P3, P4 Registers (Base Address: 0220h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P3 complement selection | P3SELC | 16h |
| Port P3 interrupt edge select | P3IES | 18h |
| Port P3 interrupt enable | P3IE | 1Ah |
| Port P3 interrupt flag | P3IFG | 1Ch |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 resistor enable | P4REN | 07h |
| Port P4 selection 0 | P4SEL0 | 0Bh |
| Port P4 selection 1 | P4SEL1 | 0Dh |
| Port P4 complement selection | P4SELC | 17h |
| Port P4 interrupt vector word | P4IV | 1Eh |
| Port P4 interrupt edge select | P4IES | 19h |
| Port P4 interrupt enable | P4IE | 1Bh |
| Port P4 interrupt flag | P4IFG | 1Dh |

**表 6-58. Port P5, P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 resistor enable | P5REN | 06h |
| Port P5 selection 0 | P5SEL0 | 0Ah |
| Port P5 selection 1 | P5SEL1 | 0Ch |
| Reserved | | 0Eh |
| Port P5 complement selection | P5SELC | 16h |
| Reserved | | 18h |
| Reserved | | 1Ah |
| Reserved | | 1Ch |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 resistor enable | P6REN | 07h |
| Port P6 selection 0 | P6SEL0 | 0Bh |
| Port P6 selection 1 | P6SEL1 | 0Dh |
| Port P6 complement selection | P6SELC | 17h |
| Reserved | | 1Eh |
| Reserved | | 19h |
| Reserved | | 1Bh |
| Reserved | | 1Dh |

**表 6-59. Port P7, P8 Registers (Base Address: 0260h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P7 input | P7IN | 00h |
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |
| Port P7 resistor enable | P7REN | 06h |

**表 6-59. Port P7, P8 Registers (Base Address: 0260h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P7 selection 0 | P7SEL0 | 0Ah |
| Port P7 selection 1 | P7SEL1 | 0Ch |
| Reserved | | 0Eh |
| Port P7 complement selection | P7SELC | 16h |
| Reserved | | 18h |
| Reserved | | 1Ah |
| Reserved | | 1Ch |
| Port P8 input | P8IN | 01h |
| Port P8 output | P8OUT | 03h |
| Port P8 direction | P8DIR | 05h |
| Port P8 resistor enable | P8REN | 07h |
| Port P8 selection 0 | P8SEL0 | 0Bh |
| Port P8 selection 1 | P8SEL1 | 0Dh |
| Port P8 complement selection | P8SELC | 17h |
| Reserved | | 1Eh |
| Reserved | | 19h |
| Reserved | | 1Bh |
| Reserved | | 1Dh |

**表 6-60. Port P9, P10 Registers (Base Address: 0280h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P9 input | P9IN | 00h |
| Port P9 output | P9OUT | 02h |
| Port P9 direction | P9DIR | 04h |
| Port P9 resistor enable | P9REN | 06h |
| Port P9 selection 0 | P9SEL0 | 0Ah |
| Port P9 selection 1 | P9SEL1 | 0Ch |
| Reserved | | 0Eh |
| Port P9 complement selection | P9SELC | 16h |
| Reserved | | 18h |
| Reserved | | 1Ah |
| Reserved | | 1Ch |
| Port P10 input | P10IN | 01h |
| Port P10 output | P10OUT | 03h |
| Port P10 direction | P10DIR | 05h |
| Port P10 resistor enable | P10REN | 07h |
| Port P10 selection 0 | P10SEL0 | 0Bh |
| Port P10 selection 1 | P10SEL1 | 0Dh |
| Port P10 complement selection | P10SELC | 17h |
| Reserved | | 1Eh |
| Reserved | | 19h |
| Reserved | | 1Bh |
| Reserved | | 1Dh |

**表 6-61. Port J Registers (Base Address: 0320h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ resistor enable | PJREN | 06h |
| Port PJ selection 0 | PJSEL0 | 0Ah |
| Port PJ selection 1 | PJSEL1 | 0Ch |
| Port PJ complement selection | PJSELC | 16h |

**表 6-62. Timer_A TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| Capture/compare control 3 | TA0CCTL3 | 08h |
| Capture/compare control 4 | TA0CCTL4 | 0Ah |
| TA0 counter | TA0R | 10h |
| Capture/compare 0 | TA0CCR0 | 12h |
| Capture/compare 1 | TA0CCR1 | 14h |
| Capture/compare 2 | TA0CCR2 | 16h |
| Capture/compare 3 | TA0CCR3 | 18h |
| Capture/compare 4 | TA0CCR4 | 1Ah |
| TA0 expansion 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

**表 6-63. Timer_A TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| Capture/compare 2 | TA1CCR2 | 16h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

**表 6-64. Timer_B TB0 Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TB0 control | TB0CTL | 00h |
| Capture/compare control 0 | TB0CCTL0 | 02h |
| Capture/compare control 1 | TB0CCTL1 | 04h |
| Capture/compare control 2 | TB0CCTL2 | 06h |
| Capture/compare control 3 | TB0CCTL3 | 08h |
| Capture/compare control 4 | TB0CCTL4 | 0Ah |

表 6-64. Timer_B TB0 Registers (Base Address: 03C0h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Capture/compare control 5 | TB0CCTL5 | 0Ch |
| Capture/compare control 6 | TB0CCTL6 | 0Eh |
| TB0 counter | TB0R | 10h |
| Capture/compare 0 | TB0CCR0 | 12h |
| Capture/compare 1 | TB0CCR1 | 14h |
| Capture/compare 2 | TB0CCR2 | 16h |
| Capture/compare 3 | TB0CCR3 | 18h |
| Capture/compare 4 | TB0CCR4 | 1Ah |
| Capture/compare 5 | TB0CCR5 | 1Ch |
| Capture/compare 6 | TB0CCR6 | 1Eh |
| TB0 expansion 0 | TB0EX0 | 20h |
| TB0 interrupt vector | TB0IV | 2Eh |

表 6-65. Timer_A TA2 Registers (Base Address: 0400h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA2 control | TA2CTL | 00h |
| Capture/compare control 0 | TA2CCTL0 | 02h |
| Capture/compare control 1 | TA2CCTL1 | 04h |
| TA2 counter | TA2R | 10h |
| Capture/compare 0 | TA2CCR0 | 12h |
| Capture/compare 1 | TA2CCR1 | 14h |
| TA2 expansion 0 | TA2EX0 | 20h |
| TA2 interrupt vector | TA2IV | 2Eh |

表 6-66. Capacitive Touch I/O 0 Registers (Base Address: 0430h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Capacitive Touch I/O 0 control | CAPTIO0CTL | 0Eh |

表 6-67. Timer_A TA3 Registers (Base Address: 0440h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA3 control | TA3CTL | 00h |
| Capture/compare control 0 | TA3CCTL0 | 02h |
| Capture/compare control 1 | TA3CCTL1 | 04h |
| Capture/compare control 2 | TA3CCTL2 | 06h |
| Capture/compare control 3 | TA3CCTL3 | 08h |
| Capture/compare control 4 | TA3CCTL4 | 0Ah |
| TA3 counter | TA3R | 10h |
| Capture/compare 0 | TA3CCR0 | 12h |
| Capture/compare 1 | TA3CCR1 | 14h |
| Capture/compare 2 | TA3CCR2 | 16h |
| Capture/compare 3 | TA3CCR3 | 18h |
| Capture/compare 4 | TA3CCR4 | 1Ah |
| TA3 expansion 0 | TA3EX0 | 20h |
| TA3 interrupt vector | TA3IV | 2Eh |

**表 6-68. Capacitive Touch I/O 1 Registers (Base Address: 0470h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Capacitive Touch I/O 1 control | CAPTIO1CTL | 0Eh |

**表 6-69. RTC_C Registers (Base Address: 04A0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RTC control 0 | RTCCTL0 | 00h |
| RTC password | RTCPWD | 01h |
| RTC control 1 | RTCCTL1 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC offset calibration | RTCOCAL | 04h |
| RTC temperature compensation | RTCTCMP | 06h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds/counter 1 | RTCSEC/RTCNT1 | 10h |
| RTC minutes/counter 2 | RTCMIN/RTCNT2 | 11h |
| RTC hours/counter 3 | RTCHOUR/RTCNT3 | 12h |
| RTC day of week/counter 4 | RTCDOW/RTCNT4 | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year | RTCYEAR | 16h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion | BIN2BCD | 1Ch |
| BCD-to-Binary conversion | BCD2BIN | 1Eh |

**表 6-70. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |

**表 6-70. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

**表 6-71. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 0 control | DMA0CTL | 00h |
| DMA channel 0 source address low | DMA0SAL | 02h |
| DMA channel 0 source address high | DMA0SAH | 04h |
| DMA channel 0 destination address low | DMA0DAL | 06h |
| DMA channel 0 destination address high | DMA0DAH | 08h |
| DMA channel 0 transfer size | DMA0SZ | 0Ah |
| DMA channel 1 control | DMA1CTL | 00h |
| DMA channel 1 source address low | DMA1SAL | 02h |
| DMA channel 1 source address high | DMA1SAH | 04h |
| DMA channel 1 destination address low | DMA1DAL | 06h |
| DMA channel 1 destination address high | DMA1DAH | 08h |
| DMA channel 1 transfer size | DMA1SZ | 0Ah |
| DMA channel 2 control | DMA2CTL | 00h |
| DMA channel 2 source address low | DMA2SAL | 02h |
| DMA channel 2 source address high | DMA2SAH | 04h |
| DMA channel 2 destination address low | DMA2DAL | 06h |
| DMA channel 2 destination address high | DMA2DAH | 08h |
| DMA channel 2 transfer size | DMA2SZ | 0Ah |
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Eh |

**表 6-72. MPU Control Registers (Base Address: 05A0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| MPU control 0 | MPUCTL0 | 00h |
| MPU control 1 | MPUCTL1 | 02h |
| MPU segmentation border 2 | MPUSEGB2 | 04h |
| MPU segmentation border 1 | MPUSEGB1 | 06h |
| MPU access management | MPUSAM | 08h |
| MPU IP control 0 | MPUIPC0 | 0Ah |
| MPU IP encapsulation segment border 2 | MPUIPSEGB2 | 0Ch |
| MPU IP encapsulation segment border 1 | MPUIPSEGB1 | 0Eh |

**表 6-73. eUSCI_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA0CTLW0 | 00h |
| eUSCI _A control word 1 | UCA0CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA0BR0 | 06h |
| eUSCI_A baud rate 1 | UCA0BR1 | 07h |
| eUSCI_A modulation control | UCA0MCTLW | 08h |
| eUSCI_A status word | UCA0STATW | 0Ah |
| eUSCI_A receive buffer | UCA0RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA0TXBUF | 0Eh |
| eUSCI_A LIN control | UCA0ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA0IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA0IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA0IE | 1Ah |
| eUSCI_A interrupt flags | UCA0IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA0IV | 1Eh |

**表 6-74. eUSCI_A1 Registers (Base Address:05E0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA1CTLW0 | 00h |
| eUSCI _A control word 1 | UCA1CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA1BR0 | 06h |
| eUSCI_A baud rate 1 | UCA1BR1 | 07h |
| eUSCI_A modulation control | UCA1MCTLW | 08h |
| eUSCI_A status word | UCA1STATW | 0Ah |
| eUSCI_A receive buffer | UCA1RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA1TXBUF | 0Eh |
| eUSCI_A LIN control | UCA1ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA1IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA1IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA1IE | 1Ah |
| eUSCI_A interrupt flags | UCA1IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA1IV | 1Eh |

**表 6-75. eUSCI_B0 Registers (Base Address: 0640h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_B control word 0 | UCB0CTLW0 | 00h |
| eUSCI_B control word 1 | UCB0CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB0BR0 | 06h |
| eUSCI_B bit rate 1 | UCB0BR1 | 07h |
| eUSCI_B status word | UCB0STATW | 08h |
| eUSCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB0RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB0TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B received address | UCB0ADDRX | 1Ch |

**表 6-75. eUSCI_B0 Registers (Base Address: 0640h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_B address mask | UCB0ADDMASK | 1Eh |
| eUSCI_B I2C slave address | UCB0I2CSA | 20h |
| eUSCI_B interrupt enable | UCB0IE | 2Ah |
| eUSCI_B interrupt flags | UCB0IFG | 2Ch |
| eUSCI_B interrupt vector word | UCB0IV | 2Eh |

**表 6-76. eUSCI_B1 Registers (Base Address: 0680h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_B control word 0 | UCB1CTLW0 | 00h |
| eUSCI_B control word 1 | UCB1CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB1BR0 | 06h |
| eUSCI_B bit rate 1 | UCB1BR1 | 07h |
| eUSCI_B status word | UCB1STATW | 08h |
| eUSCI_B byte counter threshold | UCB1TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB1RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB1TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB1I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB1I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB1I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB1I2COA3 | 1Ah |
| eUSCI_B received address | UCB1ADDRX | 1Ch |
| eUSCI_B address mask | UCB1ADDMASK | 1Eh |
| eUSCI_B I2C slave address | UCB1I2CSA | 20h |
| eUSCI_B interrupt enable | UCB1IE | 2Ah |
| eUSCI_B interrupt flags | UCB1IFG | 2Ch |
| eUSCI_B interrupt vector word | UCB1IV | 2Eh |

**表 6-77. ADC12_B Registers (Base Address: 0800h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ADC12_B control 0 | ADC12CTL0 | 00h |
| ADC12_B control 1 | ADC12CTL1 | 02h |
| ADC12_B control 2 | ADC12CTL2 | 04h |
| ADC12_B control 3 | ADC12CTL3 | 06h |
| ADC12_B window comparator low threshold | ADC12LO | 08h |
| ADC12_B window comparator high threshold | ADC12HI | 0Ah |
| ADC12_B interrupt flag 0 | ADC12IFGR0 | 0Ch |
| ADC12_B Interrupt flag 1 | ADC12IFGR1 | 0Eh |
| ADC12_B interrupt flag 2 | ADC12IFGR2 | 10h |
| ADC12_B interrupt enable 0 | ADC12IER0 | 12h |
| ADC12_B interrupt enable 1 | ADC12IER1 | 14h |
| ADC12_B interrupt enable 2 | ADC12IER2 | 16h |
| ADC12_B interrupt vector | ADC12IV | 18h |
| ADC12_B memory control 0 | ADC12MCTL0 | 20h |
| ADC12_B memory control 1 | ADC12MCTL1 | 22h |
| ADC12_B memory control 2 | ADC12MCTL2 | 24h |
| ADC12_B memory control 3 | ADC12MCTL3 | 26h |
| ADC12_B memory control 4 | ADC12MCTL4 | 28h |

**表 6-77. ADC12_B Registers (Base Address: 0800h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ADC12_B memory control 5 | ADC12MCTL5 | 2Ah |
| ADC12_B memory control 6 | ADC12MCTL6 | 2Ch |
| ADC12_B memory control 7 | ADC12MCTL7 | 2Eh |
| ADC12_B memory control 8 | ADC12MCTL8 | 30h |
| ADC12_B memory control 9 | ADC12MCTL9 | 32h |
| ADC12_B memory control 10 | ADC12MCTL10 | 34h |
| ADC12_B memory control 11 | ADC12MCTL11 | 36h |
| ADC12_B memory control 12 | ADC12MCTL12 | 38h |
| ADC12_B memory control 13 | ADC12MCTL13 | 3Ah |
| ADC12_B memory control 14 | ADC12MCTL14 | 3Ch |
| ADC12_B memory control 15 | ADC12MCTL15 | 3Eh |
| ADC12_B memory control 16 | ADC12MCTL16 | 40h |
| ADC12_B memory control 17 | ADC12MCTL17 | 42h |
| ADC12_B memory control 18 | ADC12MCTL18 | 44h |
| ADC12_B memory control 19 | ADC12MCTL19 | 46h |
| ADC12_B memory control 20 | ADC12MCTL20 | 48h |
| ADC12_B memory control 21 | ADC12MCTL21 | 4Ah |
| ADC12_B memory control 22 | ADC12MCTL22 | 4Ch |
| ADC12_B memory control 23 | ADC12MCTL23 | 4Eh |
| ADC12_B memory control 24 | ADC12MCTL24 | 50h |
| ADC12_B memory control 25 | ADC12MCTL25 | 52h |
| ADC12_B memory control 26 | ADC12MCTL26 | 54h |
| ADC12_B memory control 27 | ADC12MCTL27 | 56h |
| ADC12_B memory control 28 | ADC12MCTL28 | 58h |
| ADC12_B memory control 29 | ADC12MCTL29 | 5Ah |
| ADC12_B memory control 30 | ADC12MCTL30 | 5Ch |
| ADC12_B memory control 31 | ADC12MCTL31 | 5Eh |
| ADC12_B memory 0 | ADC12MEM0 | 60h |
| ADC12_B memory 1 | ADC12MEM1 | 62h |
| ADC12_B memory 2 | ADC12MEM2 | 64h |
| ADC12_B memory 3 | ADC12MEM3 | 66h |
| ADC12_B memory 4 | ADC12MEM4 | 68h |
| ADC12_B memory 5 | ADC12MEM5 | 6Ah |
| ADC12_B memory 6 | ADC12MEM6 | 6Ch |
| ADC12_B memory 7 | ADC12MEM7 | 6Eh |
| ADC12_B memory 8 | ADC12MEM8 | 70h |
| ADC12_B memory 9 | ADC12MEM9 | 72h |
| ADC12_B memory 10 | ADC12MEM10 | 74h |
| ADC12_B memory 11 | ADC12MEM11 | 76h |
| ADC12_B memory 12 | ADC12MEM12 | 78h |
| ADC12_B memory 13 | ADC12MEM13 | 7Ah |
| ADC12_B memory 14 | ADC12MEM14 | 7Ch |
| ADC12_B memory 15 | ADC12MEM15 | 7Eh |
| ADC12_B memory 16 | ADC12MEM16 | 80h |
| ADC12_B memory 17 | ADC12MEM17 | 82h |
| ADC12_B memory 18 | ADC12MEM18 | 84h |
| ADC12_B memory 19 | ADC12MEM19 | 86h |

**表 6-77. ADC12_B Registers (Base Address: 0800h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ADC12_B memory 20 | ADC12MEM20 | 88h |
| ADC12_B memory 21 | ADC12MEM21 | 8Ah |
| ADC12_B memory 22 | ADC12MEM22 | 8Ch |
| ADC12_B memory 23 | ADC12MEM23 | 8Eh |
| ADC12_B memory 24 | ADC12MEM24 | 90h |
| ADC12_B memory 25 | ADC12MEM25 | 92h |
| ADC12_B memory 26 | ADC12MEM26 | 94h |
| ADC12_B memory 27 | ADC12MEM27 | 96h |
| ADC12_B memory 28 | ADC12MEM28 | 98h |
| ADC12_B memory 29 | ADC12MEM29 | 9Ah |
| ADC12_B memory 30 | ADC12MEM30 | 9Ch |
| ADC12_B memory 31 | ADC12MEM31 | 9Eh |

**表 6-78. Comparator_E Registers (Base Address: 08C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Comparator control 0 | CECTL0 | 00h |
| Comparator control 1 | CECTL1 | 02h |
| Comparator control 2 | CECTL2 | 04h |
| Comparator control 3 | CECTL3 | 06h |
| Comparator interrupt | CEINT | 0Ch |
| Comparator interrupt vector word | CEIV | 0Eh |

**表 6-79. CRC32 Registers (Base Address: 0980h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CRC32 data input | CRC32DIW0 | 00h |
| Reserved | | 02h |
| Reserved | | 04h |
| CRC32 data input reverse | CRC32DIRBW0 | 06h |
| CRC32 initialization and result word 0 | CRC32INIRESW0 | 08h |
| CRC32 initialization and result word 1 | CRC32INIRESW1 | 0Ah |
| CRC32 result reverse word 1 | CRC32RESRW1 | 0Ch |
| CRC32 result reverse word 0 | CRC32RESRW1 | 0Eh |
| CRC16 data input | CRC16DIW0 | 10h |
| Reserved | | 12h |
| Reserved | | 14h |
| CRC16 data input reverse | CRC16DIRBW0 | 16h |
| CRC16 initialization and result word 0 | CRC16INIRESW0 | 18h |
| Reserved | | 1Ah |
| Reserved | | 1Ch |
| CRC16 result reverse word 0 | CRC16RESRW1 | 1Eh |
| Reserved | | 20h |
| Reserved | | 22h |
| Reserved | | 24h |
| Reserved | | 26h |
| Reserved | | 28h |
| Reserved | | 2Ah |
| Reserved | | 2Ch |

**表 6-79. CRC32 Registers (Base Address: 0980h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Reserved | | 2Eh |

**表 6-80. AES Accelerator Registers (Base Address: 09C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| AES accelerator control 0 | AESACTL0 | 00h |
| AES accelerator control 1 | AESACTL1 | 02h |
| AES accelerator status | AESASTAT | 04h |
| AES accelerator key | AESAKEY | 06h |
| AES accelerator data in | AESADIN | 008h |
| AES accelerator data out | AESADOUT | 00Ah |
| AES accelerator XORed data in | AESAXDIN | 00Ch |
| AES accelerator XORed data in (no trigger) | AESAXIN | 00Eh |

**表 6-81. LCD_C Registers (Base Address: 0A00h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| LCD_C control 0 | LCDCCTL0 | 000h |
| LCD_C control 1 | LCDCCTL1 | 002h |
| LCD_C blinking control | LCDCBLKCTL | 004h |
| LCD_C memory control | LCDCMEMCTL | 006h |
| LCD_C voltage control | LCDCVCTL | 008h |
| LCD_C port control 0 | LCDCPCTL0 | 00Ah |
| LCD_C port control 1 | LCDCPCTL1 | 00Ch |
| LCD_C port control 2 | LCDCPCTL2 | 00Eh |
| LCD_C charge pump control | LCDCCPCTL | 012h |
| LCD_C interrupt vector | LCDCIV | 01Eh |
| **Static and 2 to 4 mux modes** | | |
| LCD_C memory 1 | LCDM1 | 020h |
| LCD_C memory 2 | LCDM2 | 021h |
| LCD_C memory 3 | LCDM3 | 022h |
| LCD_C memory 4 | LCDM4 | 023h |
| LCD_C memory 5 | LCDM5 | 024h |
| LCD_C memory 6 | LCDM6 | 025h |
| LCD_C memory 7 | LCDM7 | 026h |
| LCD_C memory 8 | LCDM8 | 027h |
| LCD_C memory 9 | LCDM9 | 028h |
| LCD_C memory 10 | LCDM10 | 029h |
| LCD_C memory 11 | LCDM11 | 02Ah |
| LCD_C memory 12 | LCDM12 | 02Bh |
| LCD_C memory 13 | LCDM13 | 02Ch |
| LCD_C memory 14 | LCDM14 | 02Dh |
| LCD_C memory 15 | LCDM15 | 02Eh |
| LCD_C memory 16 | LCDM16 | 02Fh |
| LCD_C memory 17 | LCDM17 | 030h |
| LCD_C memory 18 | LCDM18 | 031h |
| LCD_C memory 19 | LCDM19 | 032h |
| LCD_C memory 20 | LCDM20 | 033h |
| LCD_C memory 21 | LCDM21 | 034h |

**表 6-81. LCD_C Registers (Base Address: 0A00h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| LCD_C memory 22 | LCDM22 | 035h |
| Reserved | | 036h |
| Reserved | | 037h |
| LCD_C blinking memory 1 | LCDBM1 | 040h |
| LCD_C blinking memory 2 | LCDBM2 | 041h |
| LCD_C blinking memory 3 | LCDBM3 | 042h |
| LCD_C blinking memory 4 | LCDBM4 | 043h |
| LCD_C blinking memory 5 | LCDBM5 | 044h |
| LCD_C blinking memory 6 | LCDBM6 | 045h |
| LCD_C blinking memory 7 | LCDBM7 | 046h |
| LCD_C blinking memory 8 | LCDBM8 | 047h |
| LCD_C blinking memory 9 | LCDBM9 | 048h |
| LCD_C blinking memory 10 | LCDBM10 | 049h |
| LCD_C blinking memory 11 | LCDBM11 | 04Ah |
| LCD_C blinking memory 12 | LCDBM12 | 04Bh |
| LCD_C blinking memory 13 | LCDBM13 | 04Ch |
| LCD_C blinking memory 14 | LCDBM14 | 04Dh |
| LCD_C blinking memory 15 | LCDBM15 | 04Eh |
| LCD_C blinking memory 16 | LCDBM16 | 04Fh |
| LCD_C blinking memory 17 | LCDBM17 | 050h |
| LCD_C blinking memory 18 | LCDBM18 | 051h |
| LCD_C blinking memory 19 | LCDBM19 | 052h |
| LCD_C blinking memory 20 | LCDBM20 | 053h |
| LCD_C blinking memory 21 | LCDBM21 | 054h |
| LCD_C blinking memory 22 | LCDBM22 | 055h |
| Reserved | | 056h |
| Reserved | | 057h |
| **5 to 8 mux modes** | | |
| LCD_C memory 1 | LCDM1 | 020h |
| LCD_C memory 2 | LCDM2 | 021h |
| LCD_C memory 3 | LCDM3 | 022h |
| LCD_C memory 4 | LCDM4 | 023h |
| LCD_C memory 5 | LCDM5 | 024h |
| LCD_C memory 6 | LCDM6 | 025h |
| LCD_C memory 7 | LCDM7 | 026h |
| LCD_C memory 8 | LCDM8 | 027h |
| LCD_C memory 9 | LCDM9 | 028h |
| LCD_C memory 10 | LCDM10 | 029h |
| LCD_C memory 11 | LCDM11 | 02Ah |
| LCD_C memory 12 | LCDM12 | 02Bh |
| LCD_C memory 13 | LCDM13 | 02Ch |
| LCD_C memory 14 | LCDM14 | 02Dh |
| LCD_C memory 15 | LCDM15 | 02Eh |
| LCD_C memory 16 | LCDM16 | 02Fh |
| LCD_C memory 17 | LCDM17 | 030h |
| LCD_C memory 18 | LCDM18 | 031h |
| LCD_C memory 19 | LCDM19 | 032h |

**表 6-81. LCD_C Registers (Base Address: 0A00h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| LCD_C memory 20 | LCDM20 | 033h |
| LCD_C memory 21 | LCDM21 | 034h |
| LCD_C memory 22 | LCDM22 | 035h |
| LCD_C memory 23 | LCDM23 | 036h |
| LCD_C memory 24 | LCDM24 | 037h |
| LCD_C memory 25 | LCDM25 | 038h |
| LCD_C memory 26 | LCDM26 | 039h |
| LCD_C memory 27 | LCDM27 | 03Ah |
| LCD_C memory 28 | LCDM28 | 03Bh |
| LCD_C memory 29 | LCDM29 | 03Ch |
| LCD_C memory 30 | LCDM30 | 03Dh |
| LCD_C memory 31 | LCDM31 | 03Eh |
| LCD_C memory 32 | LCDM32 | 03Fh |
| LCD_C memory 33 | LCDM33 | 040h |
| LCD_C memory 34 | LCDM34 | 041h |
| LCD_C memory 35 | LCDM35 | 042h |
| LCD_C memory 36 | LCDM36 | 043h |
| LCD_C memory 37 | LCDM37 | 044h |
| LCD_C memory 38 | LCDM38 | 045h |
| LCD_C memory 39 | LCDM39 | 046h |
| LCD_C memory 40 | LCDM40 | 047h |
| LCD_C memory 41 | LCDM41 | 048h |
| LCD_C memory 42 | LCDM42 | 049h |
| LCD_C memory 43 | LCDM43 | 04Ah |

**表 6-82. Extended Scan Interface (ESI) Registers (Base Address: 0D00h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ESI debug 1 | ESIDEBUG1 | 000h |
| ESI debug 2 | ESIDEBUG2 | 002h |
| ESI debug 3 | ESIDEBUG3 | 004h |
| ESI debug 4 | ESIDEBUG4 | 006h |
| ESI debug 5 | ESIDEBUG5 | 008h |
| Reserved | | 00Ah |
| Reserved | | 00Ch |
| Reserved | | 00Eh |
| ESI PSM counter 0 | ESICNT0 | 010h |
| ESI PSM counter 1 | ESICNT1 | 012h |
| ESI PSM counter 2 | ESICNT2 | 014h |
| ESI oscillator counter | ESICNT3 | 016h |
| Reserved | | 018h |
| ESI interrupt vector | ESIIV | 01Ah |
| ESI interrupt 1 | ESIINT1 | 01Ch |
| ESI interrupt 2 | ESIINT2 | 01Eh |
| ESI AFE control | ESIAFE | 020h |
| ESI PPU control | ESIPPU | 022h |
| ESI TSM control | ESITSM | 024h |
| ESI PSM control | ESIPSM | 026h |

**表 6-82. Extended Scan Interface (ESI) Registers (Base Address: 0D00h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ESI oscillator control | ESIOSC | 028h |
| ESI control | ESICTL | 02Ah |
| ESI PSM counter threshold 1 | ESITHR1 | 02Ch |
| ESI PSM counter threshold 2 | ESITHR2 | 02Eh |
| ESI A/D conversion memory 1 | ESIADMEM1 | 030h |
| ESI A/D conversion memory 2 | ESIADMEM2 | 032h |
| ESI A/D conversion memory 3 | ESIADMEM3 | 034h |
| ESI A/D conversion memory 4 | ESIADMEM4 | 036h |
| Reserved | | 038h |
| Reserved | | 03Ah |
| Reserved | | 03Ch |
| Reserved | | 03Eh |
| ESI DAC1 0 | ESIDAC1R0 | 040h |
| ESI DAC1 1 | ESIDAC1R1 | 042h |
| ESI DAC1 2 | ESIDAC1R2 | 044h |
| ESI DAC1 3 | ESIDAC1R3 | 046h |
| ESI DAC1 4 | ESIDAC1R4 | 048h |
| ESI DAC1 5 | ESIDAC1R5 | 04Ah |
| ESI DAC1 6 | ESIDAC1R6 | 04Ch |
| ESI DAC1 7 | ESIDAC1R7 | 04Eh |
| ESI DAC2 0 | ESIDAC2R0 | 050h |
| ESI DAC2 1 | ESIDAC2R1 | 052h |
| ESI DAC2 2 | ESIDAC2R2 | 054h |
| ESI DAC2 3 | ESIDAC2R3 | 056h |
| ESI DAC2 4 | ESIDAC2R4 | 058h |
| ESI DAC2 5 | ESIDAC2R5 | 05Ah |
| ESI DAC2 6 | ESIDAC2R6 | 05Ch |
| ESI DAC2 7 | ESIDAC2R7 | 05Eh |
| ESI TSM 0 | ESITSM0 | 060h |
| ESI TSM 1 | ESITSM1 | 062h |
| ESI TSM 2 | ESITSM2 | 064h |
| ESI TSM 3 | ESITSM3 | 066h |
| ESI TSM 4 | ESITSM4 | 068h |
| ESI TSM 5 | ESITSM5 | 06Ah |
| ESI TSM 6 | ESITSM6 | 06Ch |
| ESI TSM 7 | ESITSM7 | 06Eh |
| ESI TSM 8 | ESITSM8 | 070h |
| ESI TSM 9 | ESITSM9 | 072h |
| ESI TSM 10 | ESITSM10 | 074h |
| ESI TSM 11 | ESITSM11 | 076h |
| ESI TSM 12 | ESITSM12 | 078h |
| ESI TSM 13 | ESITSM13 | 07Ah |
| ESI TSM 14 | ESITSM14 | 07Ch |
| ESI TSM 15 | ESITSM15 | 07Eh |
| ESI TSM 16 | ESITSM16 | 080h |
| ESI TSM 17 | ESITSM17 | 082h |
| ESI TSM 18 | ESITSM18 | 084h |

表 6-82. Extended Scan Interface (ESI) Registers (Base Address: 0D00h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ESI TSM 19 | ESITSM19 | 086h |
| ESI TSM 20 | ESITSM20 | 088h |
| ESI TSM 21 | ESITSM21 | 08Ah |
| ESI TSM 22 | ESITSM22 | 08Ch |
| ESI TSM 23 | ESITSM23 | 08Eh |
| ESI TSM 24 | ESITSM24 | 090h |
| ESI TSM 25 | ESITSM25 | 092h |
| ESI TSM 26 | ESITSM26 | 094h |
| ESI TSM 27 | ESITSM27 | 096h |
| ESI TSM 28 | ESITSM28 | 098h |
| ESI TSM 29 | ESITSM29 | 09Ah |
| ESI TSM 30 | ESITSM30 | 09Ch |
| ESI TSM 31 | ESITSM31 | 09Eh |

## 6.14 Identification

### 6.14.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see 节 8.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in 节 6.12.

### 6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see 节 8.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in 节 6.12.

### 6.14.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in *MSP430 Programming With the JTAG Interface*.

# 7 Applications, Implementation, and Layout

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

### *7.1.1 Power Supply Decoupling and Bulk Capacitors*

TI recommends connecting a combination of a 1-µF plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC, DVCC, and ESIDVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, TI recommends separated grounds with a single-point connection for better noise isolation from digital to analog circuits on the board and to achieve high analog accuracy.

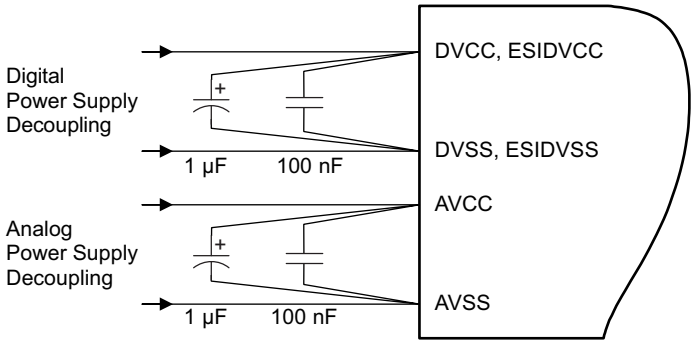



**图 7-1. Power Supply Decoupling**

### *7.1.2 External Oscillator*

Depending on the device variant (see Section 3), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If they are left unused, terminate them according to Section 4.4.

图 7-2 shows a typical connection diagram.

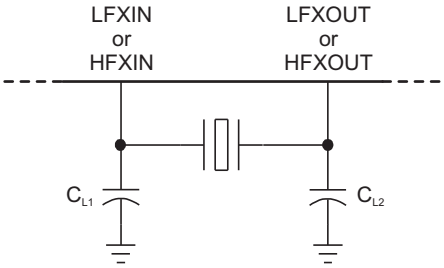



**图 7-2. Typical Crystal Connection**

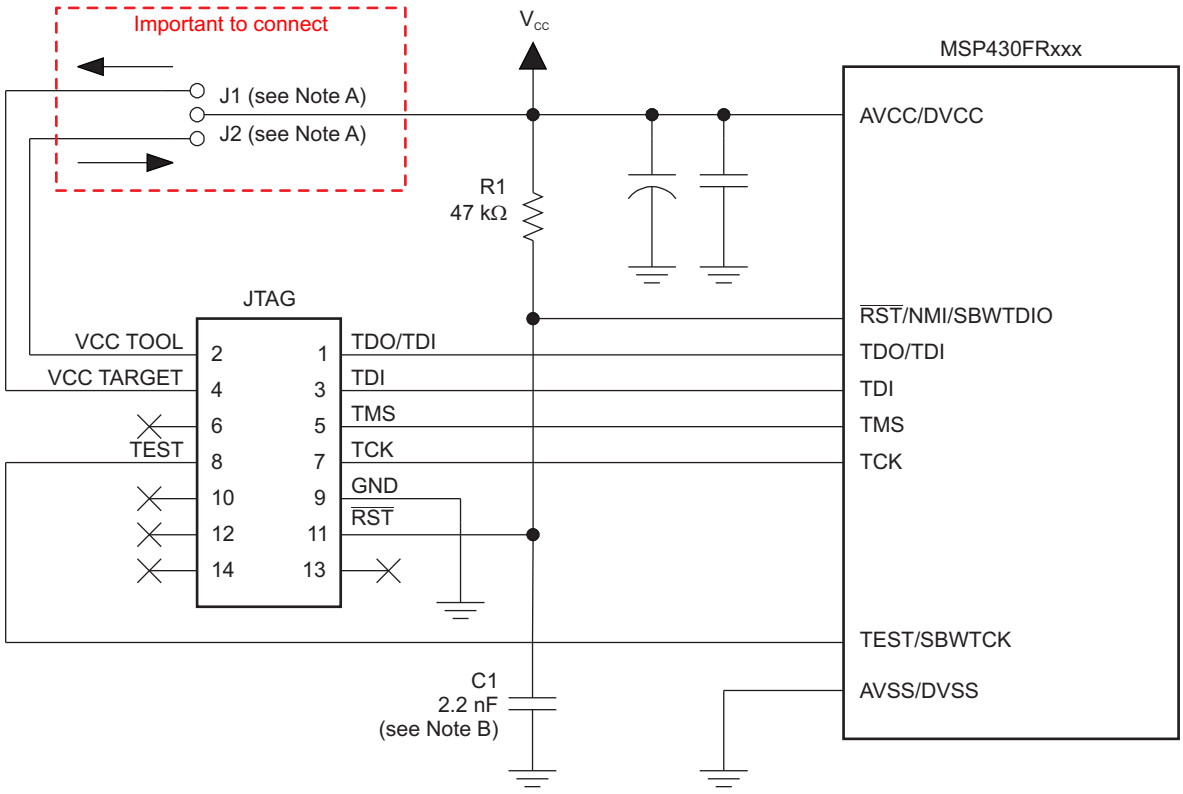
See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

### 7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. 图 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. 图 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. 图 7-3 and 图 7-4 show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide*.

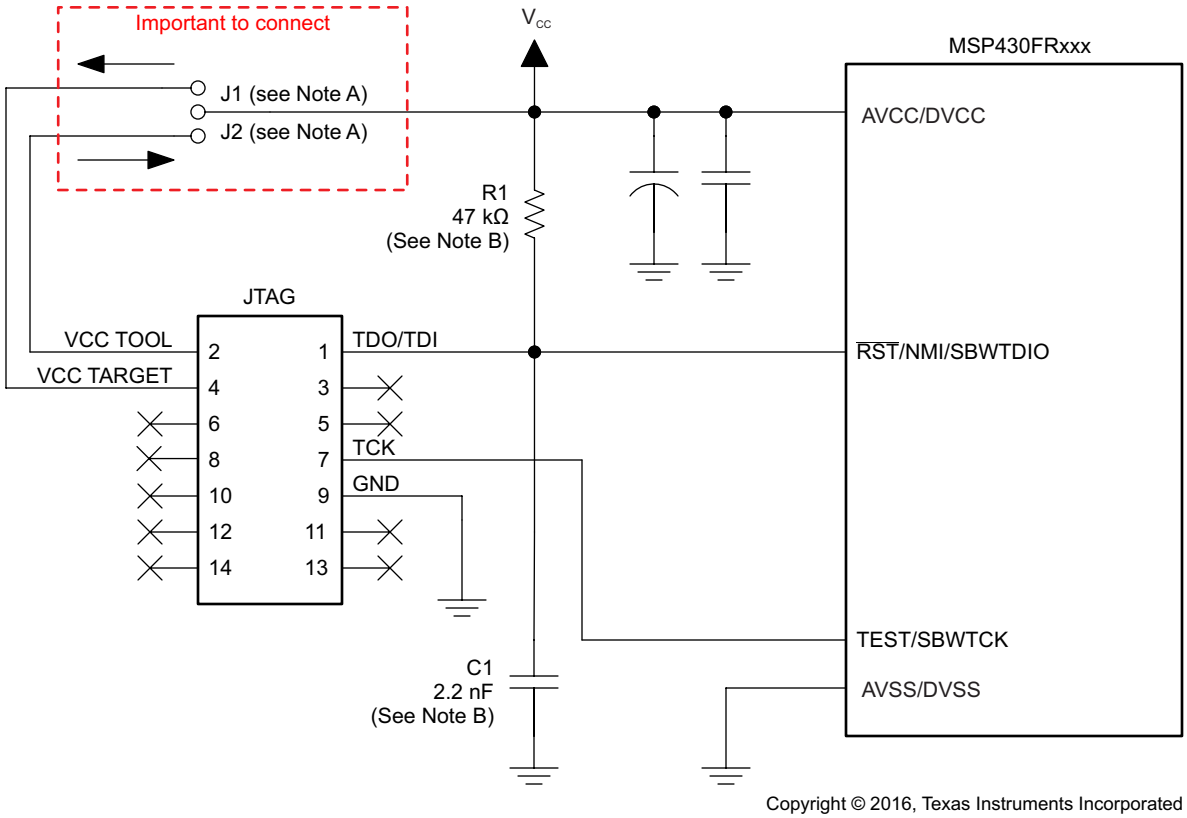





A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 2.2 nF when using current TI tools.

**图 7-3. Signal Connections for 4-Wire JTAG Communication**






A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device RST/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

**图 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)**

### 7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the RST/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the RST/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The RST/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the RST/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the RST/NMI pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers. If JTAG or Spy-Bi-Wire access is not needed, up to a 10-nF pulldown capacitor may be used.

See the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* for more information on the referenced control registers and bits.

### 7.1.5 Unused Pins

For details on the connection of unused pins, see Section 4.4.

### 7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- See *Circuit Board Layout Techniques* for a detailed discussion of PCB layout considerations. This document is written primarily about op amps, but the guidelines are generally applicable for all mixed-signal applications.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

### 7.1.7 Do's and Don'ts

TI recommends powering the AVCC, DVCC, and ESIDVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in the *Absolute Maximum Ratings* section. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

## 7.2 Peripheral- and Interface-Specific Design Information

### 7.2.1 ADC12_B Peripheral

#### 7.2.1.1 Partial Schematic

图 7-5 shows the recommended decoupling circuit when an external voltage reference is used.

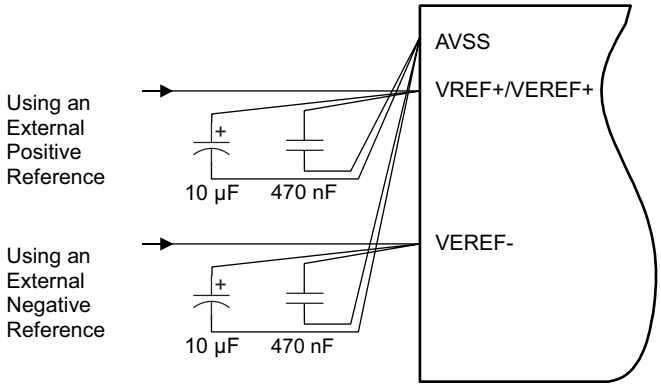



**图 7-5. ADC12_B Grounding and Noise Considerations**

#### 7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate PCB layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in 节 7.1.1 combined with the connections shown in 节 7.2.1.1 prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommend to achieve high accuracy.

图 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as specified in the Reference module's $I_{O(VREF+)}$ specification.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor is used to buffer the reference pin and filter any low-frequency ripple. A 470-nF bypass capacitor is used to filter out any high-frequency noise.

#### 7.2.1.3 Detailed Design Procedure

For additional design information, see *Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC*.

#### 7.2.1.4 Layout Guidelines

Component that are shown in the partial schematic (see 图 7-5) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC12_B, the analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

### 7.2.2 LCD_C Peripheral

#### 7.2.2.1 Partial Schematic

Required LCD connections greatly vary by the type of display that is used (static or multiplexed), whether external or internal biasing is used, and also whether the on-chip charge pump is employed. For any display used, there is flexibility as to how the segment (Sx) and common (COMx) signals are connected to the MCU, which (assuming that the correct choices are made) can be advantageous for the PCB layout and for the design of the application software.

Because LCD connections are application specific, it is difficult to provide a single one-fits-all schematic. However, for an example of connecting a 4-mux LCD with 40 segment lines that has a total of 4 × 40 = 160 individually addressable LCD segments to an MSP430FR6989, see the *Water Meter Reference Design for Two LC Sensors, Using Extended Scan Interface (ESI)*.

#### 7.2.2.2 Design Requirements

Due to the flexibility of the LCD_C peripheral module to accommodate various segment-based LCDs, selecting the correct display for the application in combination with determining specific design requirements is often an iterative process. There can be well defined requirements in terms of how many individually addressable LCD segments need to be controlled, what the requirements for LCD contrast are, which device pins are available for LCD use, and which are required by other application functions, and what the power budget is, to name just a few. TI recommends reviewing the LCD_C peripheral module chapter in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* during the initial design requirements and decision process. 表 7-1 is a brief overview over different choices that can be made and their effects.

**表 7-1. LCD Features and Use Cases**

| OPTION OR FEATURE | IMPACT OR USE CASE |
|---|---|
| Multiplexed LCD | • Enable displays with more segments<br>• Use fewer device pins<br>• LCD contrast decreases as mux level increases<br>• Power consumption increases with mux level<br>• Requires multiple intermediate bias voltages |
| Static LCD | • Limited number of segments that can be addressed<br>• Use a relatively large number of device pins<br>• Use the least amount of power<br>• Use only $V_{CC}$ and GND to drive LCD signals |
| Internal bias generation | • Simpler solution – no external circuitry<br>• Independent of $V_{LCD}$ source<br>• Somewhat higher power consumption |
| External bias generation | • Requires external resistor ladder divider<br>• Resistor size depends on display<br>• Ability to adjust drive strength to optimize tradeoff between power consumption and good drive of large segments (high capacitive load)<br>• External resistor ladder divider can be stabilized through capacitors to reduce ripple |
| Internal charge pump | • Helps ensure a constant level of contrast despite decaying supply voltage conditions (battery-powered applications)<br>• Programmable voltage levels allow software-driven contrast control<br>• Requires an external capacitor on the LCDCAP pin<br>• Higher current consumption than simply using $V_{CC}$ for the LCD driver |

#### 7.2.2.3 Detailed Design Procedure

A major component in designing the LCD solution is determining the exact connections between the LCD_C peripheral module and the display itself. Two basic design processes can be employed for this step, although in reality often a balanced co-design approach is recommended:

- PCB layout-driven design
- Software-driven design

In the PCB layout-driven design process, the segment Sx and common COMx signals are connected to respective MSP430 device pins so that the routing of the PCB can be optimized to minimize signal crossings and to keep signals on one side of the PCB only, typically the top layer. For example, using a multiplexed LCD, it is possible to arbitrarily connect the Sx and COMx signals between the LCD and the MSP430 device as long as segment lines are swapped with segment lines and common lines are swapped with common lines. It is also possible to not contiguously connect all segment lines but rather skip LCD_C module segment connections to optimize layout or to allow access to other functions that may be multiplexed on a particular device port pin. Employing a purely layout-driven design approach, however, can result in the LCD_C module control bits that are responsible for turning on and off segments to appear scattered throughout the memory map of the LCD controller (LCDMx registers). This approach potentially places a rather large burden on the software design that may also result in increased energy consumption due to the computational overhead required to work with the LCD.

The other extreme is a purely software-driven approach that starts with the idea that control bits for LCD segments that are frequently turned on and off together should be co-located in memory in the same LCDMx register or in adjacent registers. For example, in case of a 4-mux display that contains several 7-segment digits, from a software perspective it can be very desirable to control all 7 segments of each digit though a single byte-wide access to an LCDMx register. And consecutive segments are mapped to consecutive LCDMx registers. This allows use of simple look-up tables or software loops to output numbers on an LCD, reducing computational overhead and optimizing the energy consumption of an application. Establishing of the most convenient memory layout needs to be performed in conjunction with the specific LCD that is being used to understand its design constraints in terms of which segment and which common signals are connected to, for example, a digit.

For design information regarding the LCD controller input voltage selection including internal and external options, contrast control, and bias generation, see the *LCD_C Controller* chapter in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*.

For additional design information, see *Designing With MSP430 and Segment LCDs*.

#### 7.2.2.4 Layout Guidelines

LCD segment (Sx) and common (COMx) signal traces are continuously switching while the LCD is enabled and should, therefore, be kept away from sensitive analog signals such as ADC inputs to prevent any noise coupling. TI recommends keeping the LCD signal traces on one side of the PCB grouped together in a bus-like fashion. A ground plane underneath the LCD traces and guard traces employed alongside the LCD traces can provide shielding.

If the internal charge pump of the LCD module is used, the externally provided capacitor on the LCDCAP pin should be located as close as possible to the MCU. The capacitor should be connected to the device using a short and direct trace and also have a solid connection to the ground plane that is supplying the $V_{SS}$ pins of the MCU.

For an example layout of connecting a 4-mux LCD with 40 segments to an MSP430FR6989 and using the charge pump feature, see the *Water Meter Reference Design for Two LC Sensors, Using Extended Scan Interface (ESI)*.

### 7.2.3 Extended Scan Interface (ESI) Peripheral

#### 7.2.3.1 Overview

The external connections for using the Extended Scan Interface (ESI) peripheral module depend on the ESI operating mode and the application details. For example, using the ESI in conjunction with analog LC sensors requires different connections than using the ESI with resistive sensors. Also, using optical sensors and encoders that have a digital output require different considerations.

表 7-2 lists reference designs that use the ESI to interface with different types of sensors to perform rotation detection. These reference designs provide the hardware and software design files as well as analysis and user's guides to jumpstart your microcontroller-based projects.

**表 7-2. Reference Designs for ESI**

| DESIGN NAME | LINK |
|---|---|
| *Water Meter Reference Design for Two LC Sensors, Using Extended Scan Interface (ESI)* | TIDM-LC-WATERMTR |
| *Water Meter Reference Design for Three LC Sensors, Using Extended Scan Interface (ESI)* | TIDM-3LC-METER-CONV |
| *Water Meter Reference Design for GMR Sensors, Using Extended Scan Interface (ESI)* | TIDM-GMR-WATERMTR |
| *Water Meter Reference Design for Optical Sensors, Using Extended Scan Interface (ESI)* | TIDM-OPTICALWATERMTR |

For schematic information related to other types of sensors and application use cases, see the *Overview of Extended Scan Interface Applications* section in the *Extended Scan Interface (ESI)* chapter of the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide*.

#### 7.2.3.2 Design Requirements

The hardware design requirements are specific to the use case and are most affected by the specification of the interaction of the chosen analog or digital sensors with the analog front ends (AFE1 an AFE2) of the ESI. However, when designing the sensor circuit, the other digital parts of the ESI module, namely the preprocessing unit (PPU), the processing state machine (PSM) with its associated RAM, the timing state machine (TSM), and the Timer_A output stage must also be considered to ensure that the processing as required by the application can be performed in an autonomous manner inside the ESI. See the *Extended Scan Interface (ESI)* chapter of the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* for additional information regarding the design requirements and constraints of the module.

#### 7.2.3.3 Detailed Design Procedure

TI provides a variety of collateral to aid the design and implementation of the ESI into specific applications, most of which are related to metering. The following application notes are available as of this writing. Additional application notes may be available in the device-specific product folder.

*LC Sensor Rotation Detection With MSP430 Extended Scan Interface (ESI)*

*Method to Select the Value of LC Sensor for MSP430 Extended Scan Interface (ESI)*

*Adjustment of ESIOSC Oscillator Frequency*

*Migrating From MSP430FW42x Scan Interface to MSP430FR6x8x/FR5x8x Extended Scan Interface*

For complete and fully documented reference implementations that use the ESI to interface with different types of sensors to perform rotation detection, see 表 7-2.

#### 7.2.3.4 Layout Guidelines

The proper operation of the ESI and the connected sensor front end relies on a good analog board layout. Specifically in case of using the ESI analog front ends to interface with LC type or resistive sensors as typically employed in metering applications, the designer must make sure that the sensitive analog sensor signals are kept separated and guarded from any noise that might occur in the system including but not limited to the switching of LCD segment and common lines, communication signals, or any other type of digital I/O that is toggling. Failure to follow proper precautions may reduce the sensitivity of the solution or may render the application inoperable.

Customers are encouraged to study and follow one of the available TI Designs (see 表 7-2) for additional guidance. Also see 节 7.1.6 for more information that is applicable to this topic.

# 8 器件和文档支持

## 8.1 入门和后续步骤

有关 MSP430 系列器件以及有助于开发的工具和库的更多信息，请访问入门页面。

## 8.2 器件命名规则

为了标示产品开发周期所处的阶段，TI 为所有 MSP MCU 器件的部件号分配了前缀。每个 MSP MCU 商用系列产品成员都具有以下两个前缀之一：MSP 或 XMS。这些前缀代表了产品开发的发展阶段，即从工程原型 (XMS) 直到完全合格的生产器件 (MSP)。

**XMS** - 实验器件，不一定代表最终器件的电气规格

**MSP** - 完全合格的生产器件

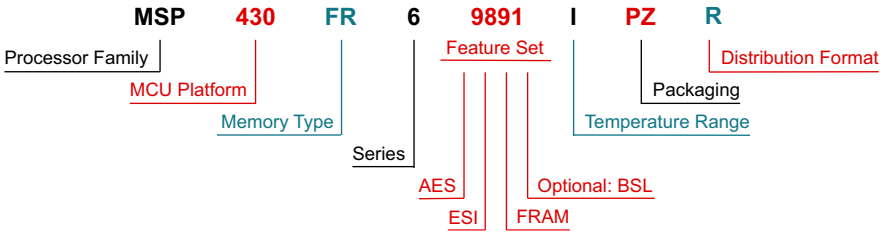
XMS 器件在供货时附带如下免责声明：

“开发中的产品用于内部评估用途。”

MSP 器件的特性已经全部明确，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书对该器件适用。

预测显示原型器件 (XMS) 的故障率大于标准生产器件。由于这些器件的预计最终使用故障率尚不确定，德州仪器 (TI) 建议不要将它们用于任何生产系统。请仅使用合格的生产器件。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。此后缀表示温度范围、封装类型和配送形式。图 8-1 提供了解读完整器件名称的图例。




| | | | | |
|---|---|---|---|---|
| **Processor Family** | MSP = Mixed-Signal Processor<br>XMS = Experimental Silicon | | | |
| **MCU Platform** | 430 = TI's 16-bit MSP430 Low-Power Microcontroller Platform | | | |
| **Memory Type** | FR = FRAM | | | |
| **Series** | 6 = FRAM 6 Series up to 16 MHz with LCD<br>5 = FRAM 5 Series up to 16 MHz without LCD | | | |
| **Feature Set** | **First Digit: AES**<br>9 = AES<br>8 = No AES | **Second Digit: Extended Scan Interface**<br>8 = ESI<br>7 = No ESI<br>2 = No ESI, LCD, 64 pins | **Third Digit: FRAM (KB)**<br>9 = 128<br>8 = 96<br>7 = 64<br>6 = 48 | **Optional Fourth Digit: BSL**<br>1 = $I^2C$<br>No value = UART |
| **Temperature Range** | I = –40°C to 85°C | | | |
| **Packaging** | www.ti.com/packaging | | | |
| **Distribution Format** | T = Small reel<br>R = Large reel<br>No markings = Tube or tray | | | |

NOTE: 该图不代表可用 特性 和选项的完整列表， 也不表示 和选项都可用于给定的器件或系列。

**图 8-1. 器件命名规则 – 部件号解码器**

## 8.3 工具和软件

表 8-1 列出 了 MSP430FR698x(1) 和 MSP430FR598x(1) 微控制器支持的调试特性。关于可用特性的详细信息，请参见*《适用于 MSP430 的 Code Composer Studio 用户指南》*。

**表 8-1. 硬件 特性**

| MSP430 架构 | 四线制 JTAG | 2 线 JTAG | 断点 (N) | 范围断点 | 时钟控制 | 状态序列发生器 | 跟踪缓冲器 | LPMX.5 调试支持 | EnergyTrace++ 技术 |
|---|---|---|---|---|---|---|---|---|---|
| MSP430Xv2 | 有 | 有 | 3 | 有 | 是 | 否 | 否 | 有 | 有 |

EnergyTrace™技术可用于 Code Composer Studio 6.0 及更高版本。它需要专用的调试器电路，而新一代板载 eZ-FET 闪存仿真工具和新一代独立 MSP-FET JTAG 仿真器支持这种电路。有关更多信息，请参阅：

*《使用 Code Composer Studio 版本 6 与增强型仿真模块 (EEM) 进行高级调试》*

*《MSP430™ 高级功耗优化：ULP Advisor™ 和 EnergyTrace™ 技术》*

设计套件与评估模块

**MSP430FR6989 LaunchPad™ 开发套件** MSP-EXP430FR6989 LaunchPad 开发套件是适用于 MSP40FR6989 微控制器 (MCU) 的易于使用的评估模块 (EVM)。它包含在超低功耗 MSP430FRx FRAM 微控制器平台上开始开发所需的全部资源，其中包括用于编程、调试和能量测量的板载仿真。

**适用于 MSP430FRxx FRAM MCU 的 MSP-TS430PZ100D 100 引脚目标开发板** MSP-TS430PZ100D 是一款独立的 100 引脚 ZIF 插座目标板，用于通过 JTAG 接口或 Spy-Bi-Wire（2 线 JTAG）协议对 MSP430 MCU 系统内置器件进行编程和调试。

**适用于 MSP430FRxx FRAM MCU 的 100 引脚目标开发板和 MSP-FET 编程器包** MSP-FET430U100D 是一款捆绑包，其中采用了具有 MSP-TS430PZ100D（独立的 100 引脚 ZIF 插座目标板）的 MSP-FET 编程器和调试器。该捆绑包可用于通过 JTAG 接口或 Spy-Bi-Wire（2 线 JTAG）协议对 MSP430 MCU 系统内置器件进行编程和调试。

软件

**MSP430Ware™ 软件** MSP430Ware 软件集合了所有 MSP430 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有 MSP430 MCU 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

**MSP430FR5x8x、MSP430FR692x、MSP430FR6x7x、MSP430FR6x8x 代码示例** 根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

**适用于 MSP 超低功耗微控制器的 FRAM 嵌入式软件实用程序** TI FRAM 实用程序软件旨在用作不断扩充的嵌入式软件实用程序集合，其中的实用程序充分利用了 FRAM 的超低功耗和近乎无限次的写入寿命。这些实用程序适用于 MSP430FRxx FRAM 微控制器并提供示例代码，以帮助开始进行应用程序开发。

**适用于采用扩展扫描接口 (ESI) 的流量计配置的 FlowESI GUI** 遵照简单的图形说明，将最多三个 LC 传感器连接至扩展扫描接口模块。该工具可提供完全实用的 CCS 和 IAR 项目，或可整合到定制项目中的源代码。

**MSP430 Touch Pro GUI** MSP430 Touch Pro 工具是基于 PC 的工具，可用于检验电容式触控按钮、滑块和滚轮设计。此工具可接收并显示 CapTouch 传感器数据，帮助用户快速轻松地评估、诊断和调整按钮、滑块和滚轮设计。

**MSP430 触控电源设计器 GUI** 使用 MSP430 电容式触控电源设计器，可以计算给定的 MSP430 电容式触控系统的估计平均电流消耗。通过输入系统参数（如工作电压、频率、按钮数量和按钮选通时间），用户可以在数分钟内估计给定的器件系列的指定电容式触控配置的功耗。

适用于 **MSP** 微控制器的数字信号处理 **(DSP)** 库 该数字信号处理库是一组经高度优化的函数，可针对 MSP430 和 MSP432 微控制器对定点数字执行许多常见的信号处理操作。该功能集通常 用于要求完成实时密集处理转换，从而以最低能耗实现高精度的应用。针对定点数学对 MSP 固有硬件的最佳利用可以极大地提高性能。

**MSP 驱动程序库** MSP 驱动程序库的抽象 API 提供易用的函数调用，无需直接操纵 MSP430 硬件的位与字节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可使用驱动程序库函数以尽可能低的费用编写全部项目。

**MSP EnergyTrace 技术** 适用于 MSP430 微控制器的 EnergyTrace 技术是基于电能的代码分析工具，适用于测量和显示应用的电能系统配置并帮助优化应用以实现超低功耗。

**ULP（超低功耗）Advisor** ULP Advisor™软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP430 和 MSP432 微控制器 独特 功能。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地减少应用程序的能耗。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

**IEC60730 软件包** IEC60730 MSP430 软件包经过专门开发，用于协助客户达到 IEC 60730-1:2010（家用及类似用途的自动化电气控制 - 第 1 部分：一般要求）B 类产品的要求。其中涵盖家用电器、电弧检测器、电源转换器、电动工具、电动自行车及其他诸多产品。IEC60730 MSP430 软件包可以嵌入在 MSP430 MCU 中 运行的客户应用， 从而帮助客户简化其消费类器件在功能安全方面遵循 IEC 60730-1:2010 B 类规范的认证工作。

适用于 **MSP** 的定点数学运算库 MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时 应用， 而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

适用于 **MSP430** 的浮点数学运算库 TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。该标量函数的浮点数学运算库能够利用我们的器件的智能外设，其速度最高可为标准 MSP430 数学函数的 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio IDE 和 IAR Embedded Workbench IDE 中。

开发工具

适用于 **MSP** 微控制器的 **Code Composer Studio™** 集成开发环境 Code Composer Studio (CCS) 集成开发环境 (IDE) 支持所有 MSP 微控制器器件。CCS 包含一整套用于开发和调试嵌入式 应用的嵌入式软件实用程序。CCS 包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他众多 功能。

命令行编程器 MSP Flasher 是一款基于 shell 的开源接口，可使用 JTAG 或 Spy-Bi-Wire (SBW) 通信通过 FET 编程器或 eZ430 对 MSP 微控制器进行编程。MSP Flasher 可用于将二进制文件（.txt 或 .hex 文件）直接下载到 MSP 微控制器，而无需使用 IDE。

**MSP MCU 编程器和调试器** MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件中，从而进行验证和调试。

**MSP-GANG 生产编程器** MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。

## 8.4 文档支持

以下文档介绍 MSP430FR698x(1) 和 MSP430FR598x(1) MCU。www.ti.com.cn 网站上提供了这些文档的副本。

### 接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见节 8.5）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

### 勘误

**《MSP430FR6989 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430FR69891 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430FR6988 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430FR6987 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430FR5989 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430FR59891 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430FR5988 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430FR5987 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430FR5986 器件勘误表》** 介绍功能规格的已知例外情况。

### 用户指南

**《MSP430FR58xx、MSP430FR59xx 和 MSP430FR6xx 系列用户指南》** 该器件系列提供的所有模块和外设的详细 说明 。

**《MSP430 FRAM 器件引导加载程序 (BSL) 用户指南》** MSP430 MCU 上的引导加载程序 (BSL) 允许用户在原型设计、投产和维护等各阶段与 MSP430 MCU 中的嵌入式存储器进行通信。可编程存储器（FRAM 存储器）和数据存储器 (RAM) 均可按要求予以修改。

**《通过 JTAG 接口对 MSP430 进行编程》** 此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还介绍了如何编程所有 MSP430 器件上均具备的 JTAG 访问安全保险丝。此文档介绍了使用标准四线制 JTAG 接口和两线制 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）的器件访问。

**《MSP430 硬件工具用户指南》** 此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

**MSP430 FRAM 技术 – 操作方法和最佳实践** FRAM 采用非易失性存储器技术，行为与 SRAM 类似，支持大量新 应用的同时，还改变了固件的设计方式。该应用程序报告从嵌入式软件开发方面概述了 FRAM 技术在 MSP430 中的使用方法和最佳实践。其中介绍了如何按照应用程序特定的代码、常量、数据空间要求实施存储器布局以及如何使用 FRAM 优化应用程序的能耗。

**《MSP430 32kHz 晶体振荡器》** 选择合适的晶体、正确的负载电路和适当的电路板布局是实现稳定的晶体振荡器的关键。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。

**《MSP430 系统级 ESD 注意事项》** 随着硅晶技术向更低电压方向发展以及设计具有成本效益的超低功耗组件的需求的出现，系统级 ESD 要求变得越来越苛刻。该应用报告介绍了三个不同的 ESD 主题，旨在帮助电路板设计人员和 OEM 理解并设计出稳健耐用的系统级设计。

## 8.5 相关链接

表 8-2 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

**表 8-2. 相关链接**

| 器件 | 产品文件夹 | 立即订购 | 技术文档 | 工具与软件 | 支持和社区 |
|---|---|---|---|---|---|
| MSP430FR6989 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR69891 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR6988 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR6987 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR5989 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR59891 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR5988 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR5987 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR5986 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

## 8.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的 《使用条款》。

TI E2E™ 社区
*TI 的工程师交流 (E2E) 社区*. 此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页
*德州仪器 (TI) 嵌入式处理器维基网页*。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

## 8.7 商标

EnergyTrace++, MSP430, EnergyTrace, LaunchPad, MSP430Ware, ULP Advisor, 适用于 MSP 微控制器的 Code Composer Studio, E2E are trademarks of Texas Instruments.
Microsoft is a registered trademark of Microsoft Corporation.
All other trademarks are the property of their respective owners.

## 8.8 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 8.9 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过非披露义务的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

## 8.10 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

# 9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430FR5986IPM | Active | Production | LQFP (PM) \| 64 | 160 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5986 |
| MSP430FR5986IPM.A | Active | Production | LQFP (PM) \| 64 | 160 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5986 |
| MSP430FR5986IPMR | Active | Production | LQFP (PM) \| 64 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5986 |
| MSP430FR5986IPMR.A | Active | Production | LQFP (PM) \| 64 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5986 |
| MSP430FR5987IPM | Active | Production | LQFP (PM) \| 64 | 160 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5987 |
| MSP430FR5987IPM.A | Active | Production | LQFP (PM) \| 64 | 160 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5987 |
| MSP430FR5987IPMR | Active | Production | LQFP (PM) \| 64 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5987 |
| MSP430FR5987IPMR.A | Active | Production | LQFP (PM) \| 64 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5987 |
| MSP430FR5987IRGCR | Active | Production | VQFN (RGC) \| 64 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5987 |
| MSP430FR5987IRGCR.A | Active | Production | VQFN (RGC) \| 64 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5987 |
| MSP430FR5987IRGCT | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5987 |
| MSP430FR5987IRGCT.A | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5987 |
| MSP430FR5988IPM | Active | Production | LQFP (PM) \| 64 | 160 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5988 |
| MSP430FR5988IPM.A | Active | Production | LQFP (PM) \| 64 | 160 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5988 |
| MSP430FR5988IRGCT | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5988 |
| MSP430FR5988IRGCT.A | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5988 |
| MSP430FR59891IPM | Active | Production | LQFP (PM) \| 64 | 160 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR59891 |
| MSP430FR59891IPM.A | Active | Production | LQFP (PM) \| 64 | 160 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR59891 |
| MSP430FR59891IRGCT | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR59891 |
| MSP430FR59891IRGCT.A | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR59891 |
| MSP430FR5989IPM | Active | Production | LQFP (PM) \| 64 | 160 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5989 |
| MSP430FR5989IPM.A | Active | Production | LQFP (PM) \| 64 | 160 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5989 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430FR5989IPMR | Active | Production | LQFP (PM) \| 64 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5989 |
| MSP430FR5989IPMR.A | Active | Production | LQFP (PM) \| 64 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5989 |
| MSP430FR5989IRGCR | Active | Production | VQFN (RGC) \| 64 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5989 |
| MSP430FR5989IRGCR.A | Active | Production | VQFN (RGC) \| 64 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5989 |
| MSP430FR5989IRGCT | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5989 |
| MSP430FR5989IRGCT.A | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR5989 |
| MSP430FR6987IPN | Active | Production | LQFP (PN) \| 80 | 119 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6987 |
| MSP430FR6987IPN.A | Active | Production | LQFP (PN) \| 80 | 119 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6987 |
| MSP430FR6987IPNR | Active | Production | LQFP (PN) \| 80 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6987 |
| MSP430FR6987IPNR.A | Active | Production | LQFP (PN) \| 80 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6987 |
| MSP430FR6987IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6987 |
| MSP430FR6987IPZ.A | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6987 |
| MSP430FR6988IPN | Active | Production | LQFP (PN) \| 80 | 119 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6988 |
| MSP430FR6988IPN.A | Active | Production | LQFP (PN) \| 80 | 119 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6988 |
| MSP430FR6988IPNR | Active | Production | LQFP (PN) \| 80 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6988 |
| MSP430FR6988IPNR.A | Active | Production | LQFP (PN) \| 80 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6988 |
| MSP430FR6988IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6988 |
| MSP430FR6988IPZ.A | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6988 |
| MSP430FR69891IPN | Active | Production | LQFP (PN) \| 80 | 119 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR69891 |
| MSP430FR69891IPN.A | Active | Production | LQFP (PN) \| 80 | 119 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR69891 |
| MSP430FR69891IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR69891 |
| MSP430FR69891IPZ.A | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR69891 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430FR69891IPZR | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR69891 |
| MSP430FR69891IPZR.A | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR69891 |
| MSP430FR6989IPN | Active | Production | LQFP (PN) \| 80 | 119 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6989 |
| MSP430FR6989IPN.A | Active | Production | LQFP (PN) \| 80 | 119 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6989 |
| MSP430FR6989IPNR | Active | Production | LQFP (PN) \| 80 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6989 |
| MSP430FR6989IPNR.A | Active | Production | LQFP (PN) \| 80 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6989 |
| MSP430FR6989IPZ | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6989 |
| MSP430FR6989IPZ.A | Active | Production | LQFP (PZ) \| 100 | 90 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6989 |
| MSP430FR6989IPZR | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6989 |
| MSP430FR6989IPZR.A | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6989 |
| MSP430FR6989IPZRG4 | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6989 |
| MSP430FR6989IPZRG4.A | Active | Production | LQFP (PZ) \| 100 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR6989 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF MSP430FR5989 :**

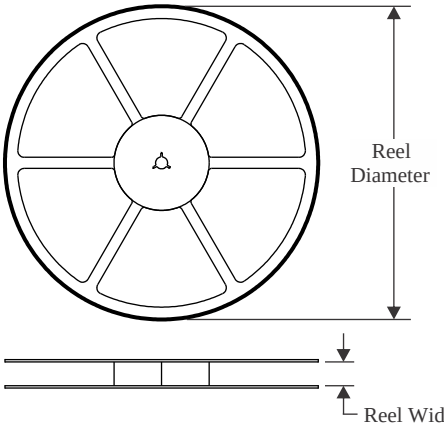
- Enhanced Product : MSP430FR5989-EP

NOTE: Qualified Version Definitions:

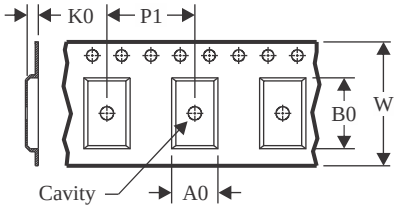
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

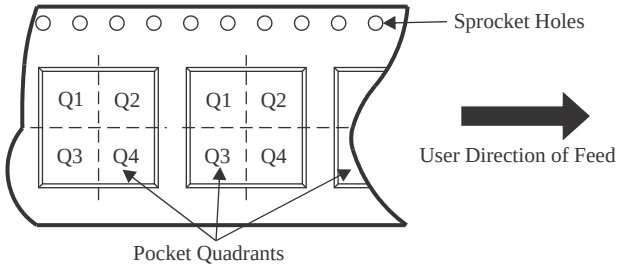



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

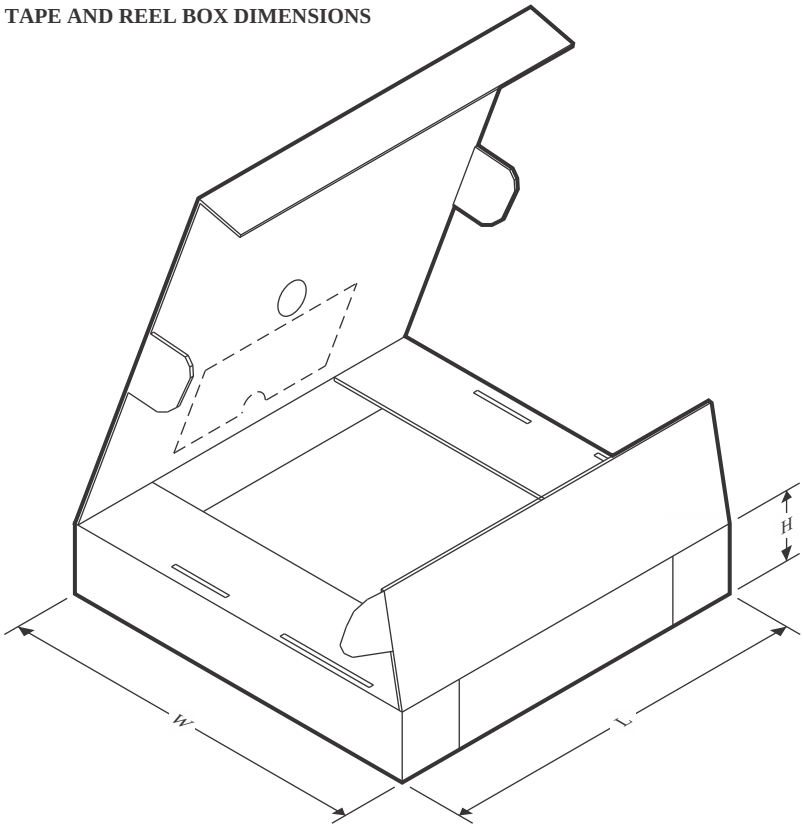
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430FR5986IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430FR5987IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430FR5987IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5987IRGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5988IRGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR59891IRGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5989IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430FR5989IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5989IRGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR6987IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430FR6988IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430FR69891IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430FR6989IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430FR6989IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430FR6989IPZRG4 | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430FR5986IPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430FR5987IPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430FR5987IRGCR | VQFN | RGC | 64 | 2000 | 367.0 | 367.0 | 38.0 |
| MSP430FR5987IRGCT | VQFN | RGC | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR5988IRGCT | VQFN | RGC | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR59891IRGCT | VQFN | RGC | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR5989IPMR | LQFP | PM | 64 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430FR5989IRGCR | VQFN | RGC | 64 | 2000 | 367.0 | 367.0 | 38.0 |
| MSP430FR5989IRGCT | VQFN | RGC | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR6987IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430FR6988IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430FR69891IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430FR6989IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430FR6989IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430FR6989IPZRG4 | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |

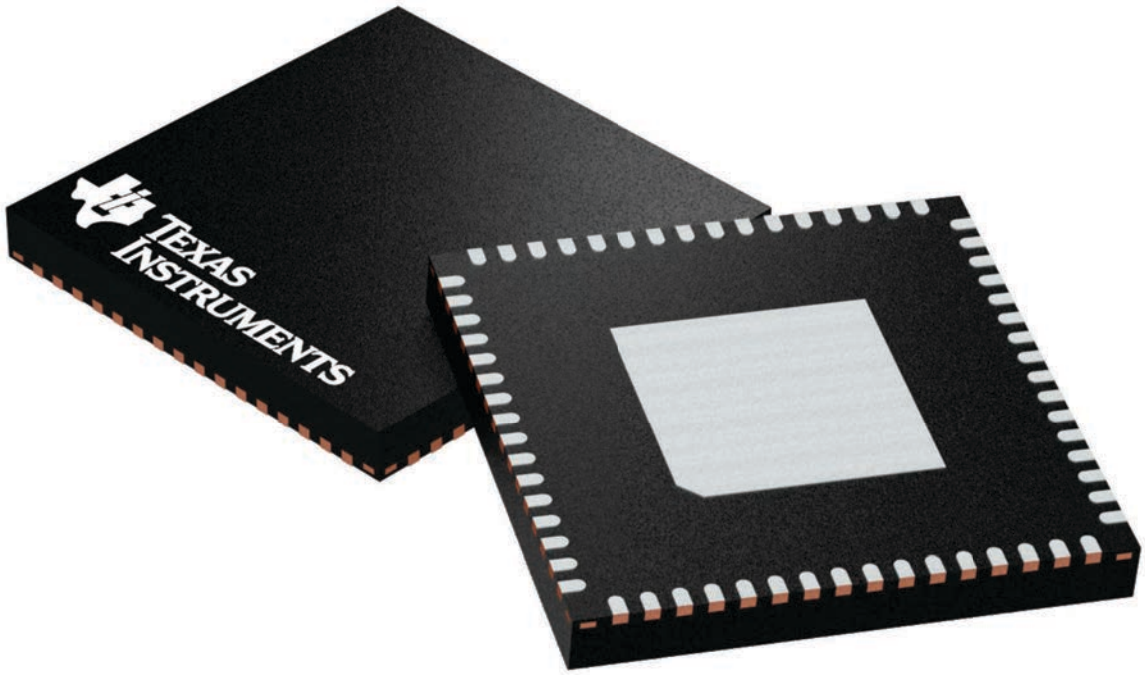
# GENERIC PACKAGE VIEW

## RGC 64

## VQFN - 1 mm max height

**9 x 9, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

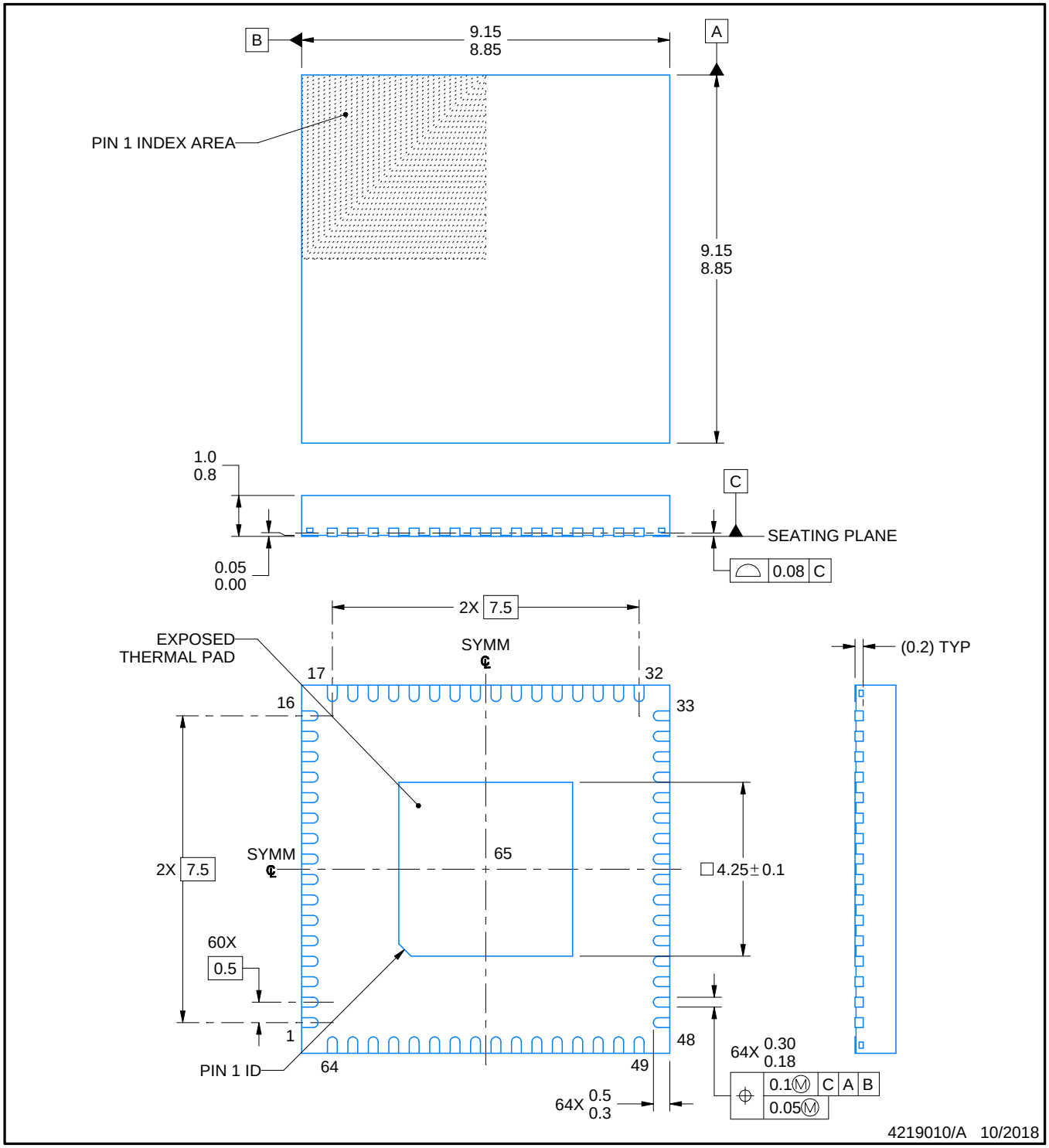
4224597/A

# PACKAGE OUTLINE

## RGC0064B

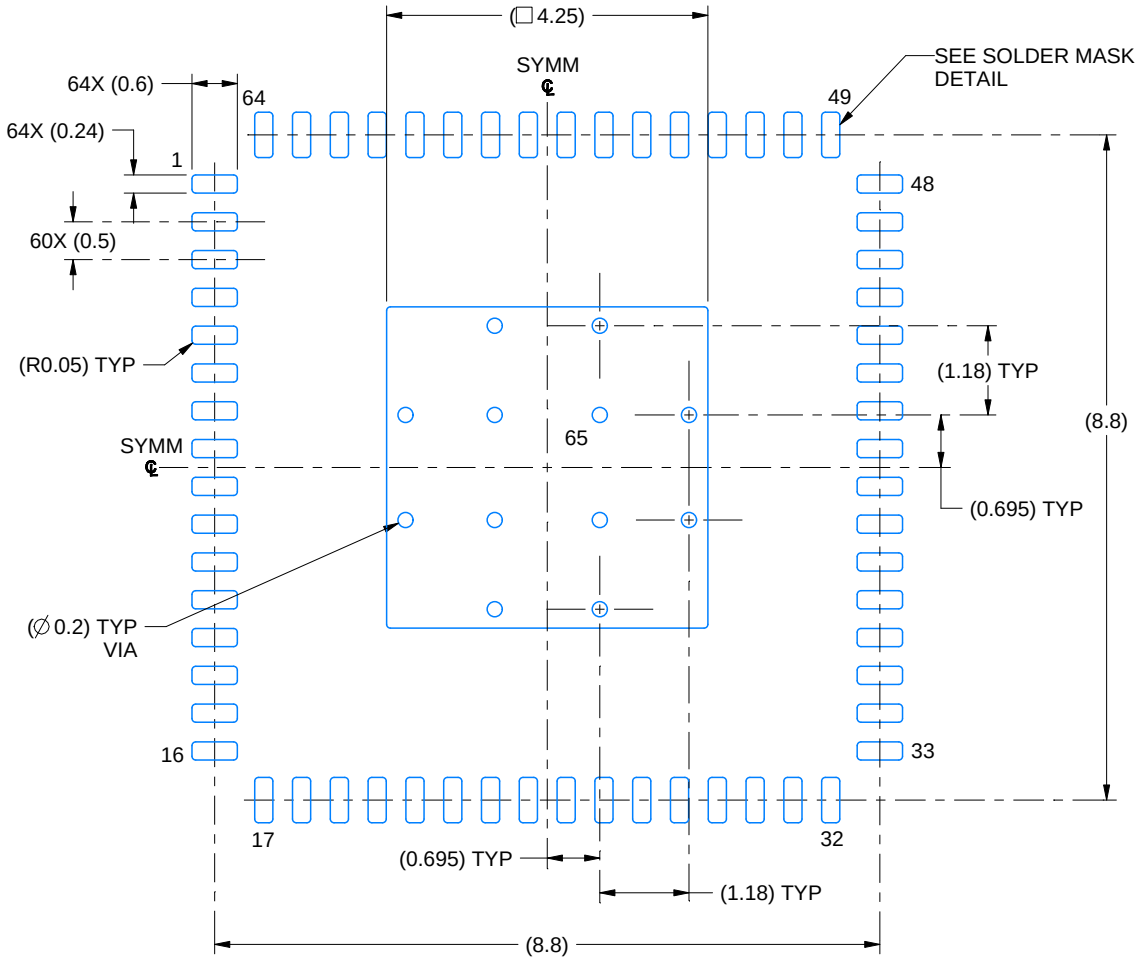
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

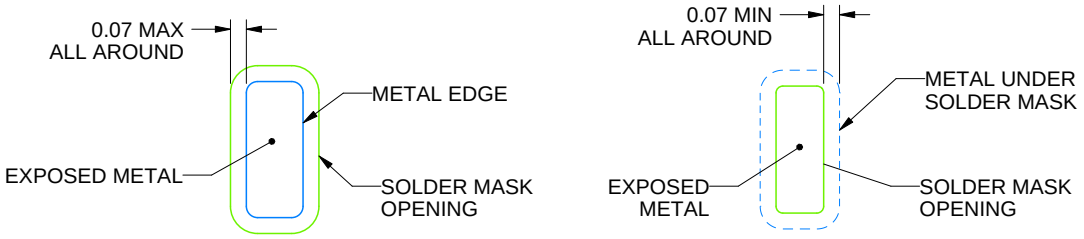



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

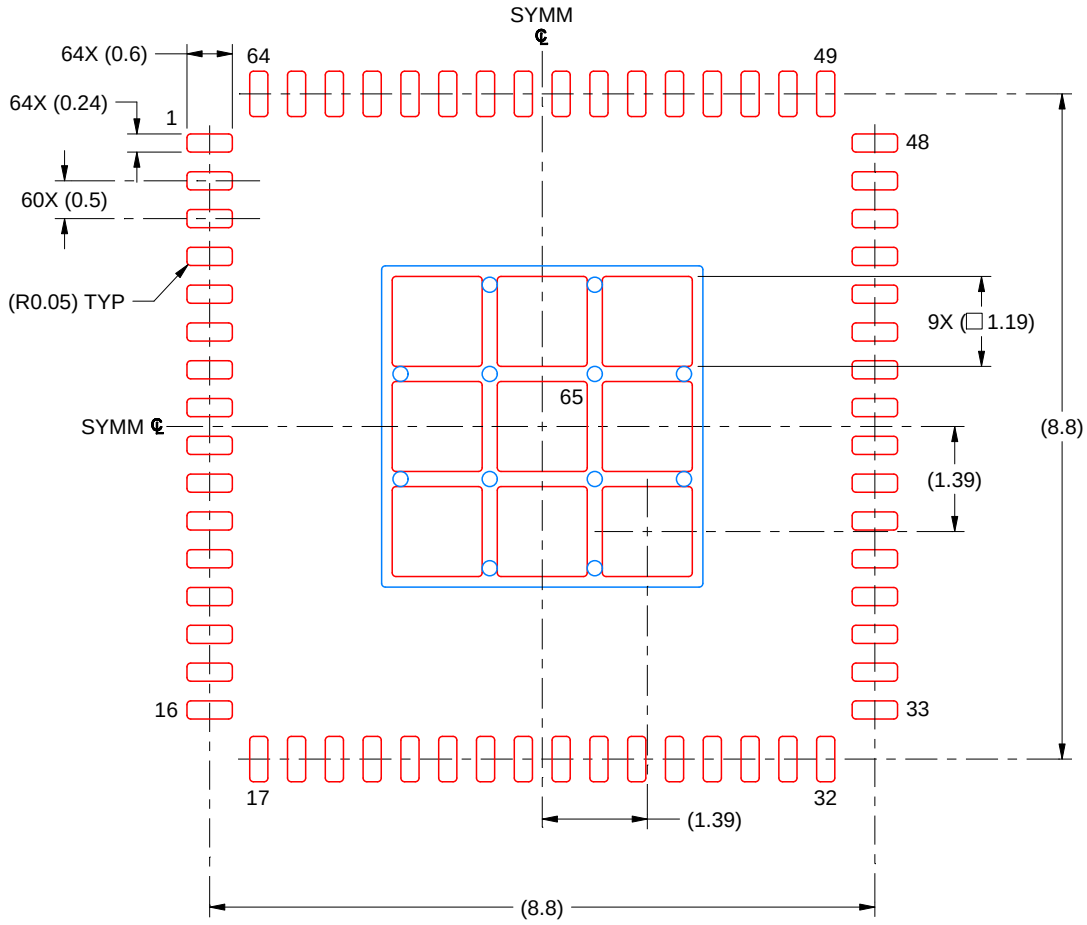



SOLDER MASK DETAILS

4219010/A 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219010/A 10/2018

NOTES: (continued)

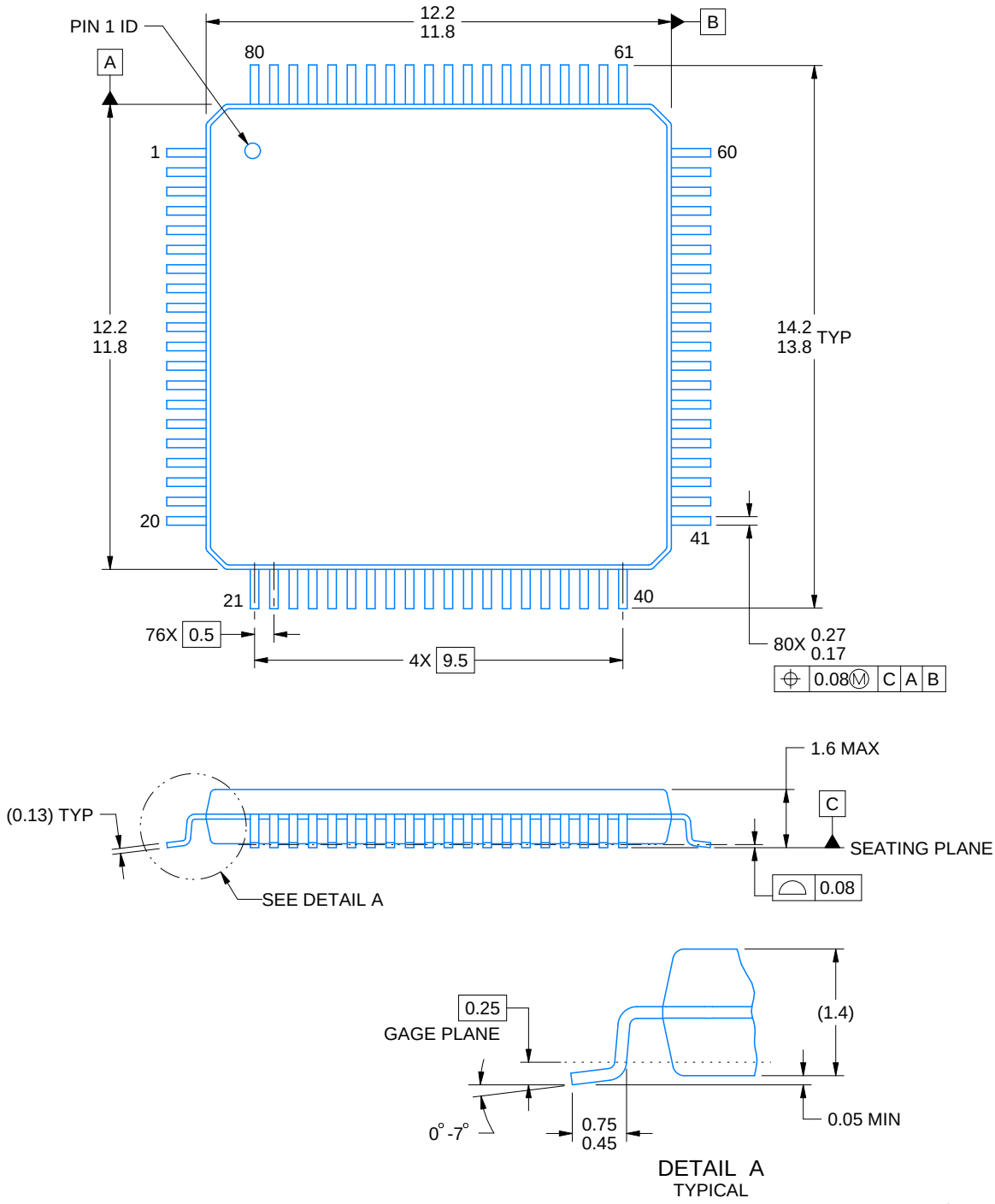
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## PN0080A

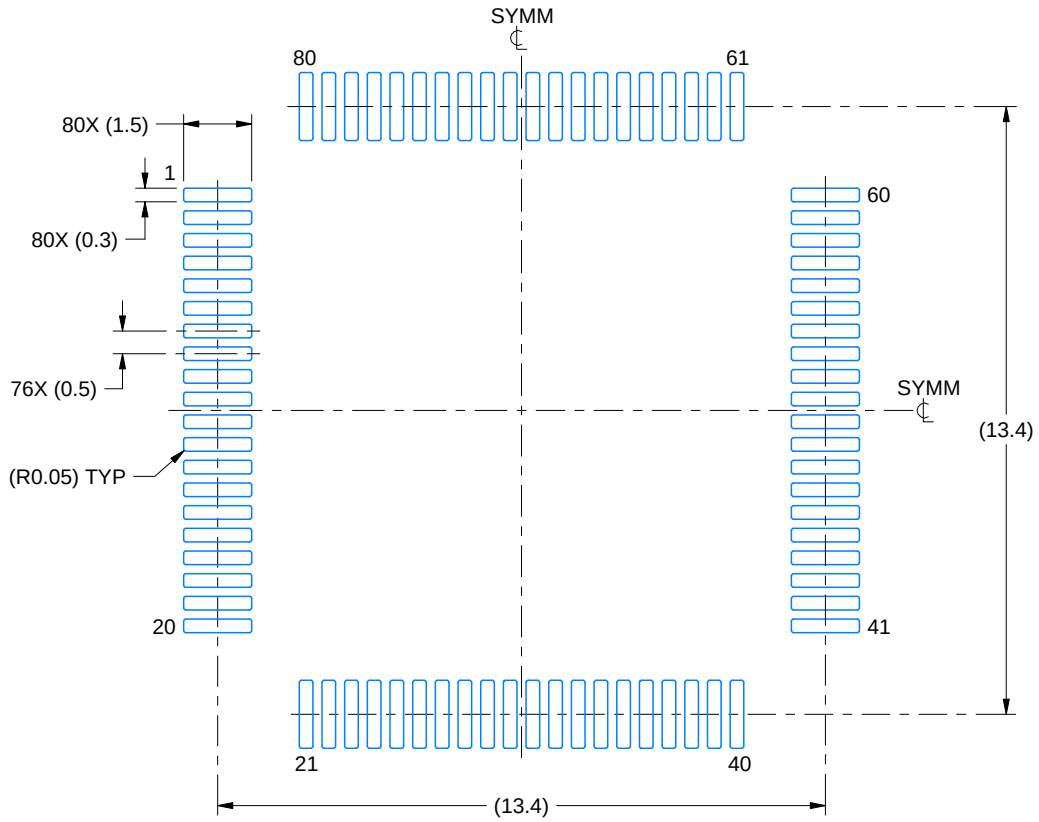
## LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

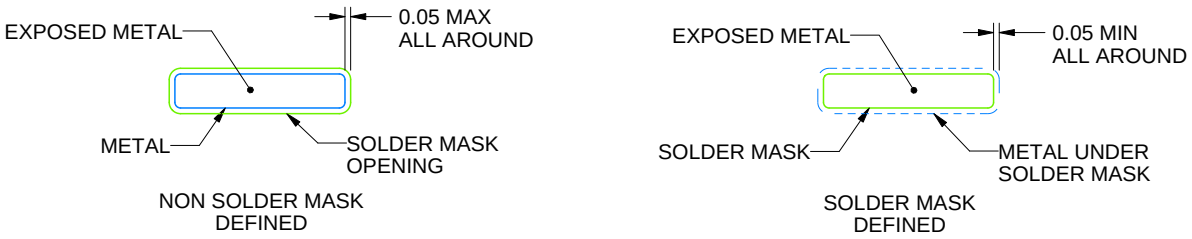



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

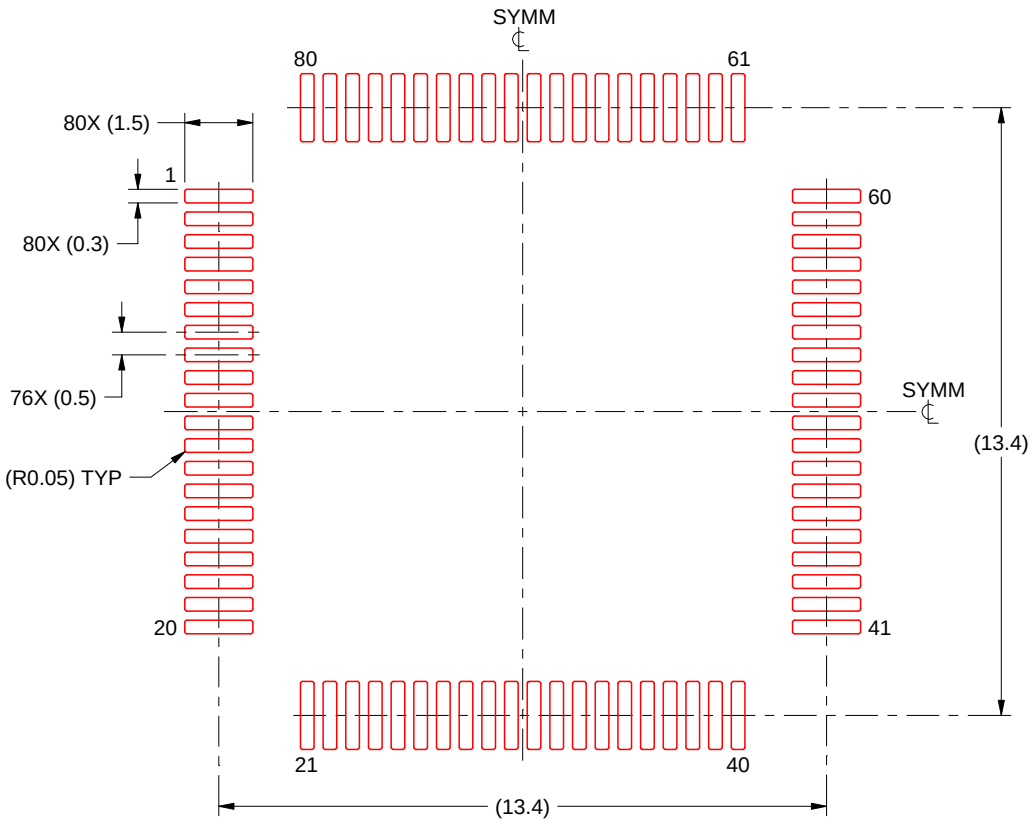



SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

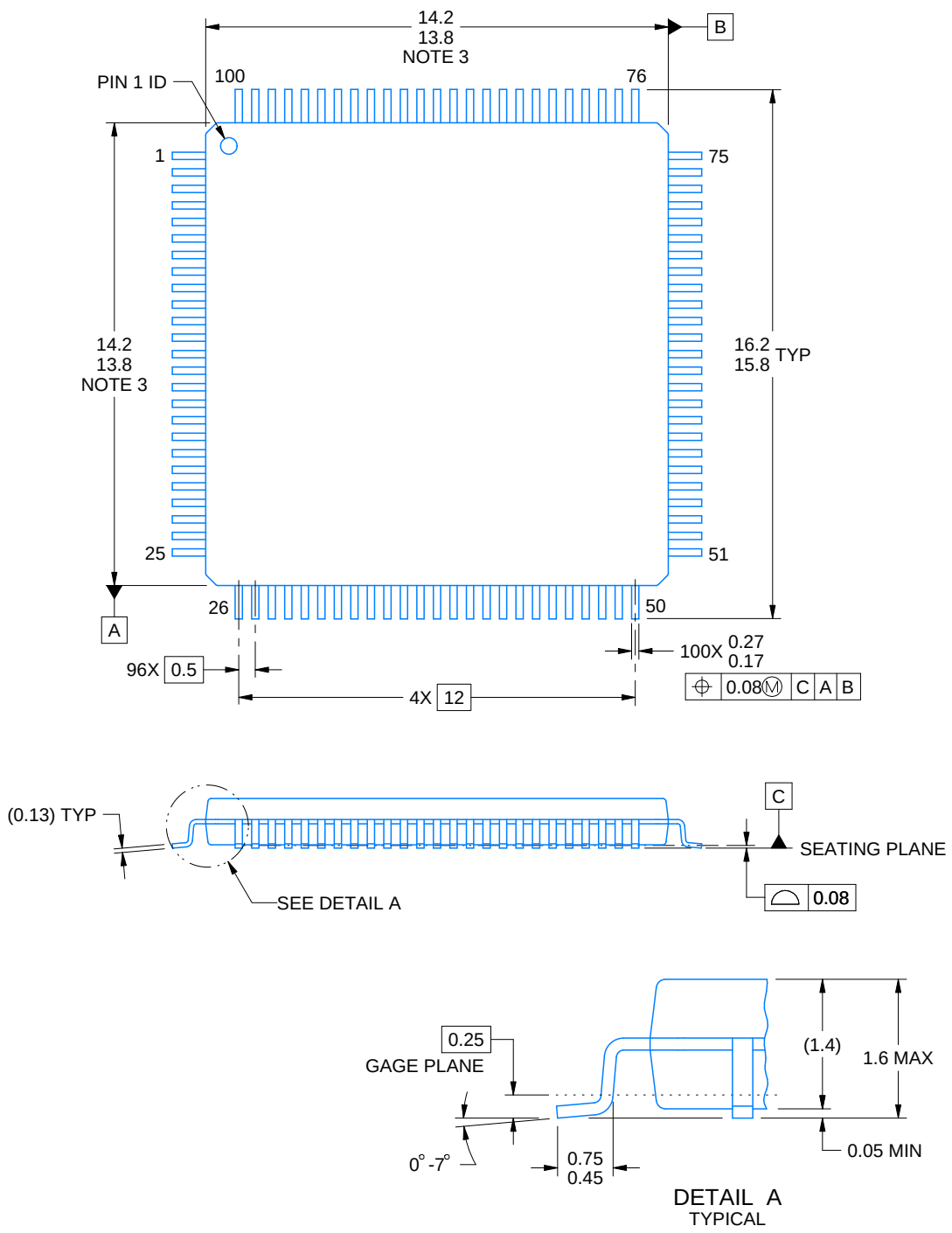
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PZ0100A

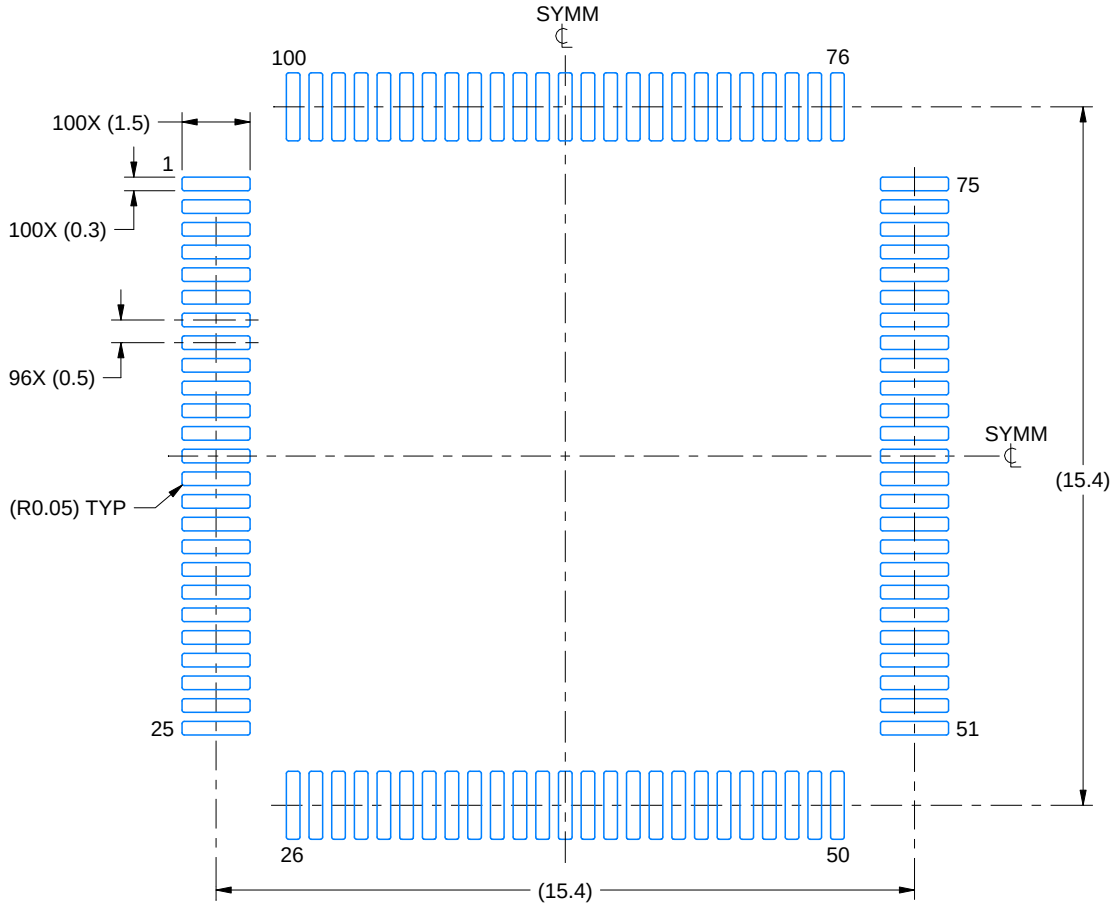
## LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

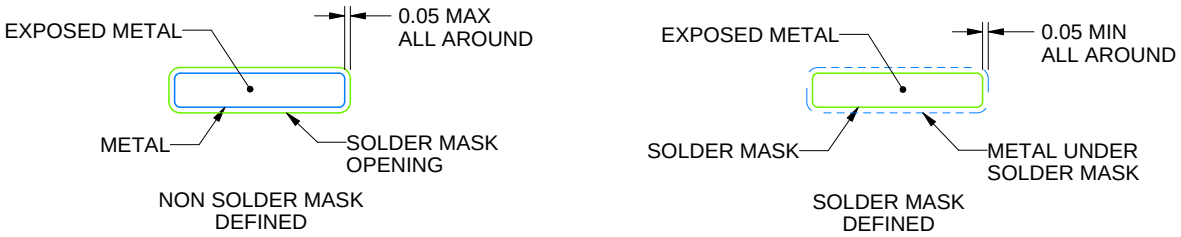



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

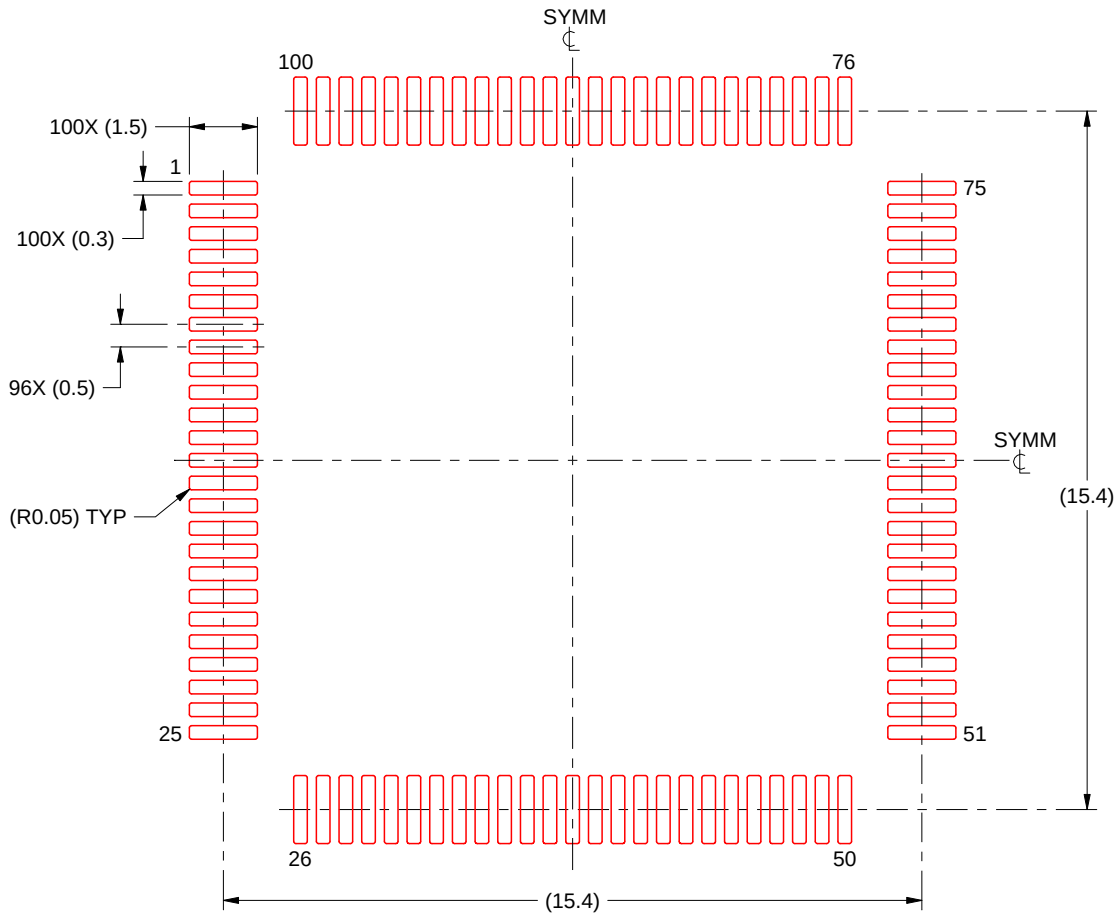



SOLDER MASK DETAILS

4215169/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215169/A 03/2017

NOTES: (continued)

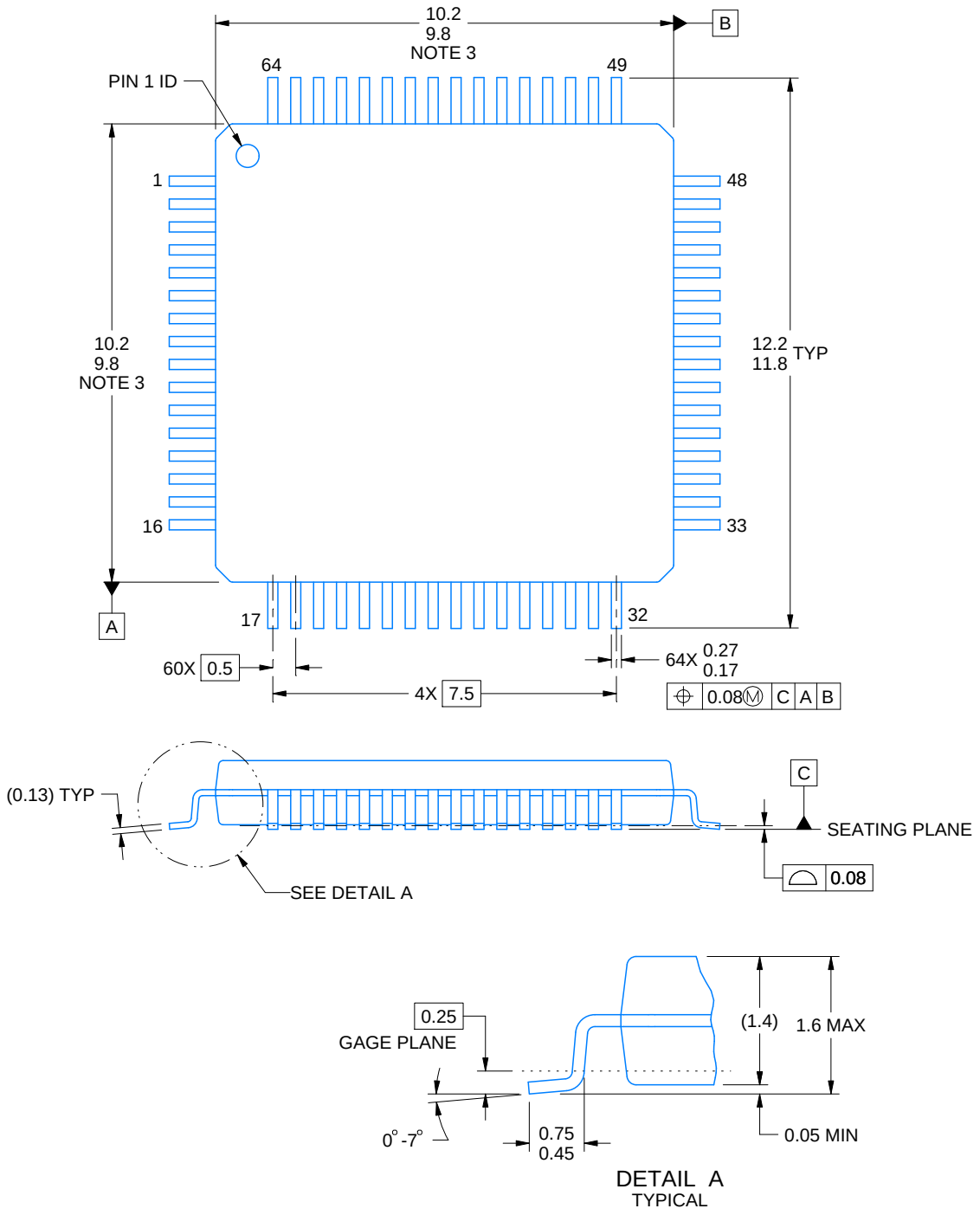
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PM0064A

## LQFP - 1.6 mm max height

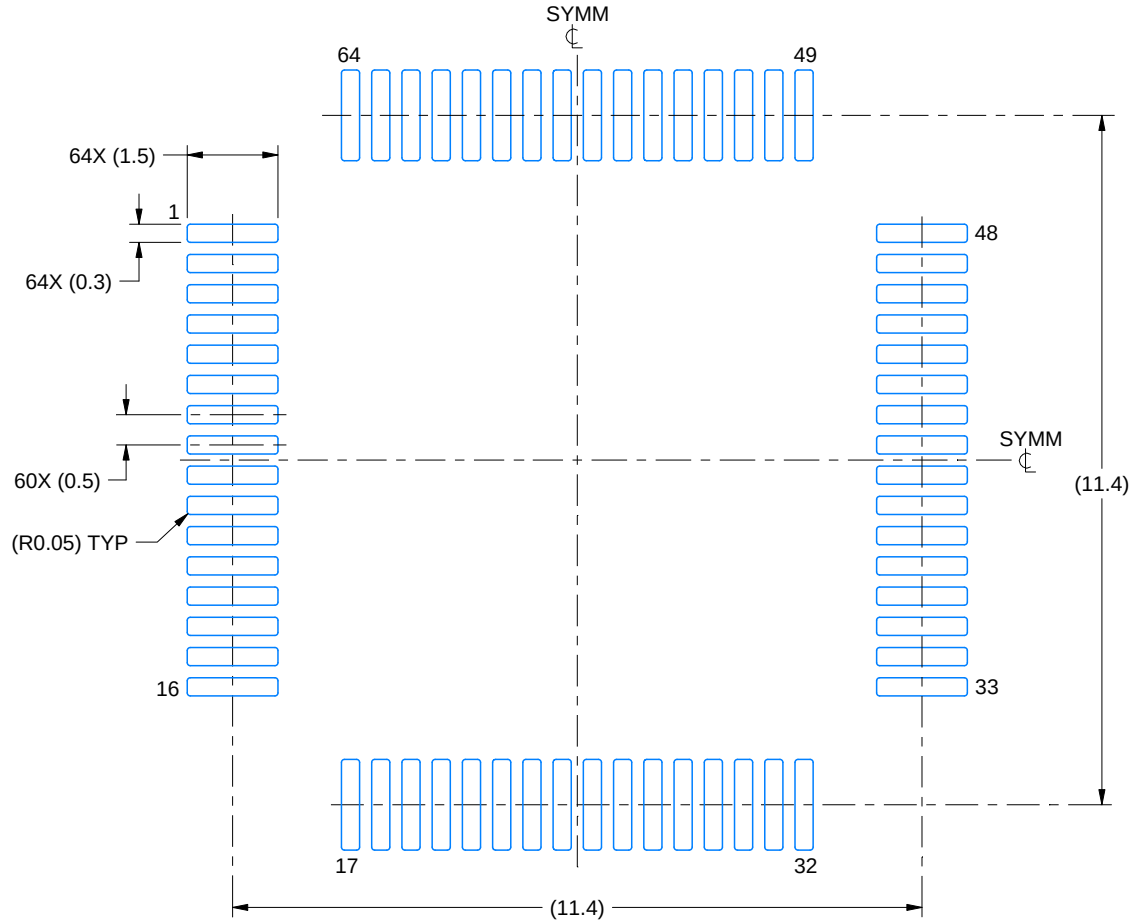
PLASTIC QUAD FLATPACK



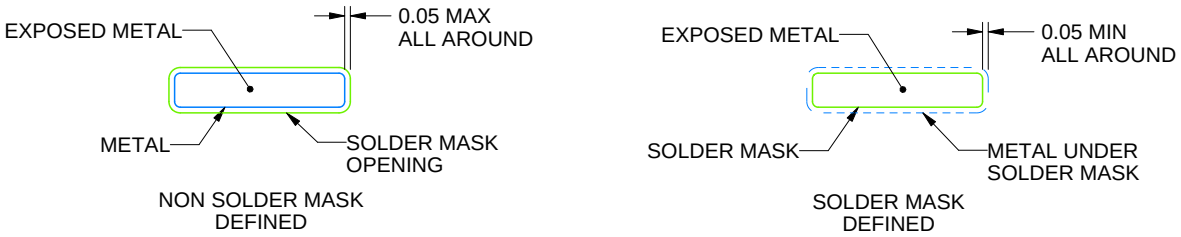

4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

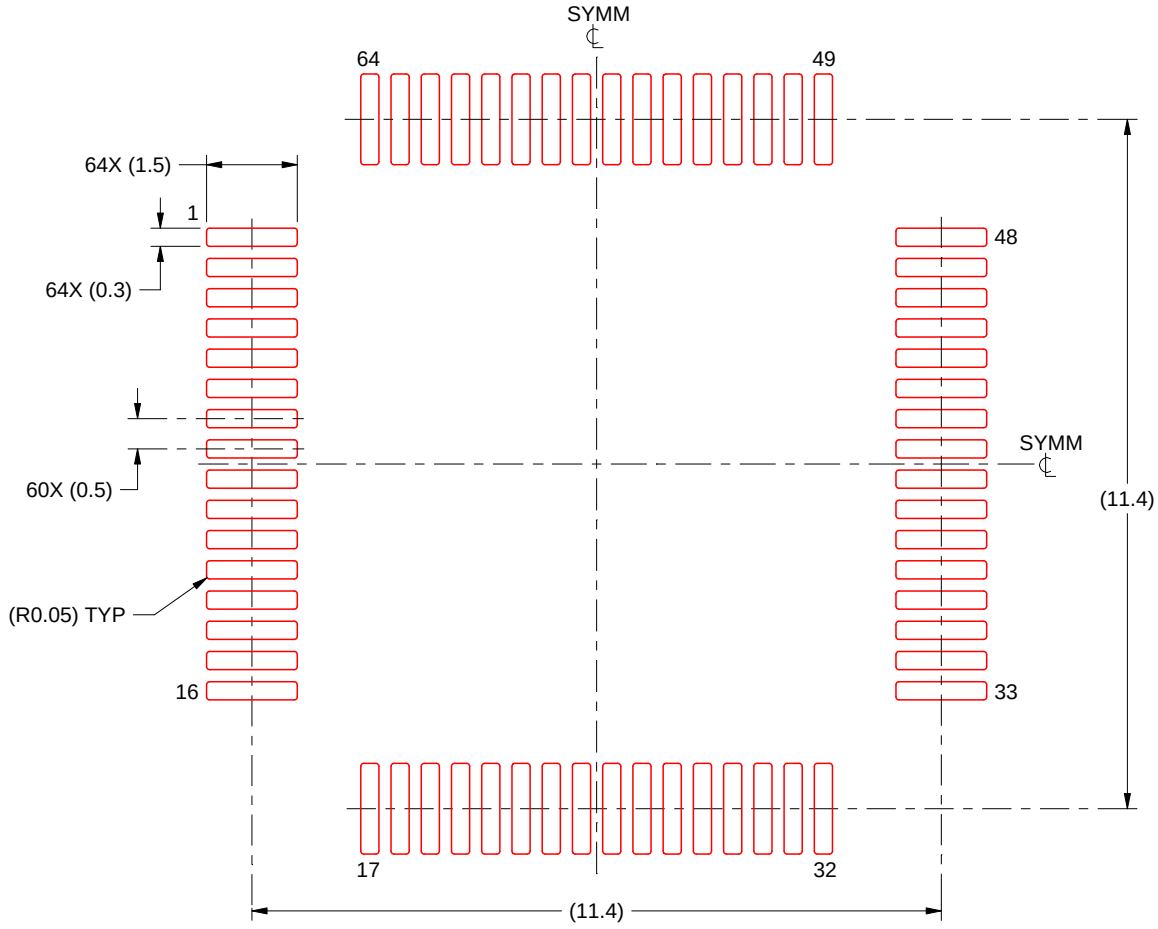



SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月