MSP430FR573x 混合信号微控制器

1 器件概述

1.1 特性

- 嵌入式微控制器
  - 高达 24MHz 时钟频率的 16 位精简指令集计算机 (RISC) 架构
  - 宽电源电压范围（2V 至 3.6V）
  - -40°C 至 85°C 运行
- 经优化超低功率模式
  - 激活模式：81.4µA/MHz（典型值）
  - 待机（具有 VLO 的 LPM3）：6.3µA（典型值）
  - 实时时钟 (RTC)（LPM3.5，采用晶振）：1.5µA（典型值）
  - 关断 (LPM4.5)：0.32µA（典型值）
- 超低功率铁电 RAM (FRAM)
  - 高达 16KB 的非易失性存储器
  - 超低功率写入
  - 125ns 每个字的快速写入（1ms 内写入 16KB）
  - 内置纠错编码 (ECC) 和存储器保护单元 (MPU)
  - 通用内存 = 程序 + 数据 + 存储
  - 10^{15} 写入周期持耐久性
  - 抗辐射和非磁性
- 智能数字外设
  - 32 位硬件乘法器 (MPY)
  - 3 通道内部直接存储器访问 (DMA)
  - 具有日历和报警功能的实时时钟 (RTC)
  - 5 个具有多达 3 个捕捉/比较寄存器的 16 位定时器
  - 16 位循环冗余校验器 (CRC)
- 高性能模拟
  - 支持电压基准和可编程滞后的 16 通道模拟比较器
  - 具有内部基准、采样与保持功能的 12 通道 10 位模数转换器 (ADC)
    - 在流耗为 100µA 时为 200ksps
- 增强型串行通信
  - eUSCI_A0 和 eUSCI_A1 支持：
    - 支持自动波特率侦测的通用异步收发器 (UART)
    - IrDA 编码和解码
    - 串行外设接口 (SPI)
  - eUSCI_B0 支持：
    - 支持多从器件寻址的 I^2C
    - 串行外设接口 (SPI)
  - 硬件通用异步收发器 (UART) 引导加载程序 (BSL)
- 电源管理系统
  - 完全集成的低压降稳压器 (LDO)
  - 具有复位功能的内核与电源电压监控器
  - 常开模式的零功率欠压检测
  - 串行板上编程，无需外部电压
- 灵活的时钟系统
  - 具有 6 个可选出厂校准频率的固定频率数控振荡器 (DCO)（视器件而定）
  - 低功率低频内部时钟源 (VLO)
  - 32kHz 晶振 (LFXT)
  - 高频晶振 (HFXT)
- 开发工具和软件
  - 免费的专业开发环境 (Code Composer Studio™ IDE)
  - 低成本全功能套件 ()
  - 完全开发套件(MSP-FET430U40A)
  - 目标板 (MSP-TS430RHA40A)
- 系列产品成员
  - 有关可用器件型号和封装的信息，请参见 *系列产品*
  - 欲了解完整的模块说明，请参见 *《MSP430FR57xx 系列产品用户指南》*

1.2 应用范围

- 家庭自动化
- 安全性
- 传感器管理
- 数据采集

注意事项 这些产品采用 FRAM 非易失性存储器技术。FRAM 保持对于极端温度环境敏感，例如那些回流焊接或者手工焊接时产生的温度。更多信息请参阅 最大绝对额定值。

注意事项 必须采用与器件级 ESD 规范兼容的系统级 ESD 保护以防止电气过载或者数据或代码内存的干扰。有关更多信息，请参阅 *《MSP430™ 系统级 ESD 注意事项》*。

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

1.3 说明

德州仪器 (TI) MSP430FR573x 系列超低功耗微控制器包含多个器件，该系列器件具有嵌入式 FRAM 非易失性存储器，超低功率 16 位 MSP430™CPU 以及专用于各种应用的不同 外设。这种架构、FRAM 和外设与 7 种低功耗模式相组合，专为在便携式无线感测应用中延长电池的使用寿命而进行了 优化。FRAM 是全新的非易失性存储器，其完美结合了 SRAM 的速度、灵活性和耐用性与闪存的稳定性和可靠性，并且总功耗更低。外设包括一个 10 位模数转换器 (ADC)，一个具有电压基准生成和滞后功能的 16 通道比较器，3 条支持 I^2C，SPI，或 UART 协议的增强型串行通道，一个内部 DMA，一个硬件乘法器，一个实时时钟 (RTC)，5 个 16 位定时器和数字 I/O。

器件信息(1)

器件型号	封装	封装尺寸(2)
MSP430FR5739RHA	超薄四方扁平无引线 (VQFN) (40)	6mm x 6mm
MSP430FR5739DA	TSSOP (38)	12.5mm x 6.2mm
MSP430FR5738RGE	VQFN (24)	4mm x 4mm
MSP430FR5738PW	TSSOP (28)	9.7mm x 4.4mm
MSP430FR5738YQD	芯片尺寸球状引脚栅格阵列 (DSBGA) (24)	2mm × 2mm

(1) 要获得最新的产品、封装和订购信息，请参见*封装选项附录*（节 8），或者访问德州仪器 (TI) 网站 www.ti.com.cn。
(2) 此处显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见*机械数据*（节 8）。

1.4 功能方框图

图 1-1 显示采用 RHA 封装的 MSP430FR5731，MSP430FR5735 和 MSP430FR5739 器件的功能方框图。要获得所有器件变量和封装选项的功能方框图，请见 节 6.1。

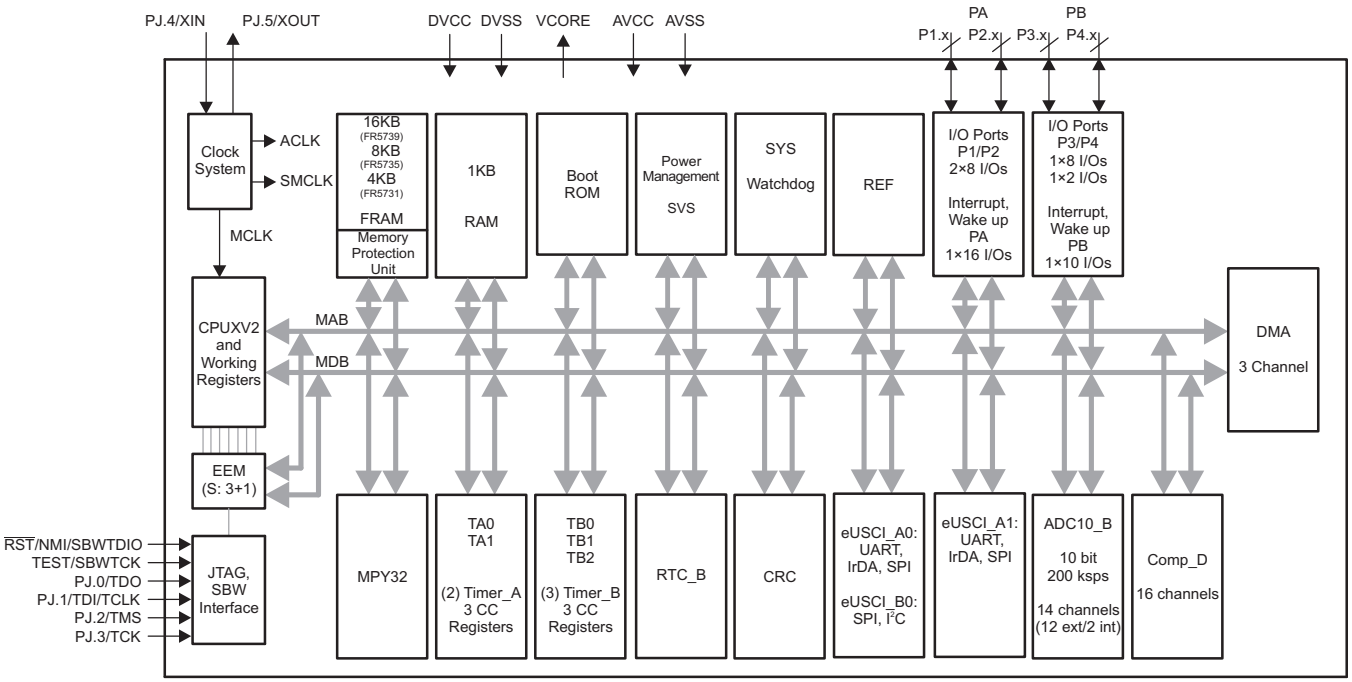

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图 **1-1.** 功能方框图 **- RHA** 封装 **- MSP430FR5731，MSP430FR5735，MSP430FR5739**

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内容

1 器件概述 1
1.1 特性 1
1.2 应用范围 1
1.3 说明 2
1.4 功能方框图 2
2 修订历史记录 4
3 Device Comparison 5
3.1 Related Products 6
4 Terminal Configuration and Functions 7
4.1 Pin Diagram – RHA Package – MSP430FR5731, MSP430FR5733, MSP430FR5735, MSP430FR5737, MSP430FR5739 7
4.2 Pin Diagram – DA Package – MSP430FR5731, MSP430FR5733, MSP430FR5735, MSP430FR5737, MSP430FR5739 8
4.3 Pin Diagram – RGE Package – MSP430FR5730, MSP430FR5732, MSP430FR5734, MSP430FR5736, MSP430FR5738 8
4.4 Pin Diagram – YQD Package – MSP430FR5738 9
4.5 Pin Diagram – PW Package – MSP430FR5730, MSP430FR5732, MSP430FR5734, MSP430FR5736, MSP430FR5738 9
4.6 Signal Descriptions 10
5 Specifications 15
5.1 Absolute Maximum Ratings 15
5.2 ESD Ratings 15
5.3 Recommended Operating Conditions 15
5.4 Active Mode Supply Current Into V_{CC} Excluding External Current 16
5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current 17
5.6 Thermal Resistance Characteristics 18
5.7 Schmitt-Trigger Inputs – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{RST}$/NMI) 19
5.8 Inputs – Ports P1 and P2 (P1.0 to P1.7, P2.0 to P2.7) 19
5.9 Leakage Current – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{RST}$/NMI) 19
5.10 Outputs – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5) 20
5.11 Output Frequency – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5) 20
5.12 Typical Characteristics – Outputs 21
5.13 Crystal Oscillator, XT1, Low-Frequency (LF) Mode 23
5.14 Crystal Oscillator, XT1, High-Frequency (HF) Mode 24
5.15 Internal Very-Low-Power Low-Frequency Oscillator (VLO) 25
5.16 DCO Frequencies 26
5.17 MODOSC 26
5.18 PMM, Core Voltage 27
5.19 PMM, SVS, BOR 27
5.20 Wake-up Times From Low-Power Modes 27
5.21 Timer_A 28
5.22 Timer_B 28
5.23 eUSCI (UART Mode) Clock Frequency 28
5.24 eUSCI (UART Mode) 28
5.25 eUSCI (SPI Master Mode) Clock Frequency 29
5.26 eUSCI (SPI Master Mode) 29
5.27 eUSCI (SPI Slave Mode) 31
5.28 eUSCI (I^2C Mode) 33
5.29 10-Bit ADC, Power Supply and Input Range Conditions 34
5.30 10-Bit ADC, Timing Parameters 34
5.31 10-Bit ADC, Linearity Parameters 34
5.32 REF, External Reference 35
5.33 REF, Built-In Reference 35
5.34 REF, Temperature Sensor and Built-In V_{MID} 36
5.35 Comparator_D 37
5.36 FRAM 37
5.37 JTAG and Spy-Bi-Wire Interface 38
6 Detailed Description 39
6.1 Functional Block Diagrams 39
6.2 CPU 44
6.3 Operating Modes 44
6.4 Interrupt Vector Addresses 45
6.5 Memory Organization 47
6.6 Bootloader (BSL) 48
6.7 JTAG Operation 48
6.8 FRAM 49
6.9 Memory Protection Unit (MPU) 49
6.10 Peripherals 49
6.11 Input/Output Diagrams 69
6.12 Device Descriptors (TLV) 90
7 器件和文档支持 93
7.1 开始使用 93
7.2 Device Nomenclature 93
7.3 工具和软件 95
7.4 文档支持 97
7.5 相关链接 99
7.6 社区资源 99
7.7 商标 99
7.8 静电放电警告 99
7.9 出口管制提示 99
7.10 术语表 99
8 机械、封装和可订购信息 99

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from October 1, 2016 to December 5, 2017	Page
• Added the note that begins "In LPM3, the VLO frequency varies..." following Section 5.15, *Internal Very-Low-Power Low-Frequency Oscillator (VLO)*	25

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3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Family Members(1)(2)

DEVICE	FRAM (KB)	SRAM (KB)	SYSTEM CLOCK (MHz)	ADC10_B	Comp_D	Timer_A(3)	Timer_B(4)	eUSCI		I/O	PACKAGE
								Channel A: UART, IrDA, SPI	Channel B: SPI, I²C		
MSP430FR5739	16	1	24	12 ext, 2 int ch.	16 ch.	3, 3	3, 3, 3	2	1	32	RHA
										30	DA
MSP430FR5738	16	1	24	6 ext, 2 int ch.	10 ch.	3, 3	3	1	1	17	RGE
				8 ext, 2 int ch.	12 ch.					21	PW
				6 ext, 2 int ch.	10 ch.					17	YQD
MSP430FR5737	16	1	24	–	16 ch.	3, 3	3, 3, 3	2	1	32	RHA
										30	DA
MSP430FR5736	16	1	24	–	10 ch.	3, 3	3	1	1	17	RGE
					12 ch.					21	PW
MSP430FR5735	8	1	24	12 ext, 2 int ch.	16 ch.	3, 3	3, 3, 3	2	1	32	RHA
										30	DA
MSP430FR5734	8	1	24	6 ext, 2 int ch.	10 ch.	3, 3	3	1	1	17	RGE
				8 ext, 2 int ch.	12 ch.					21	PW
MSP430FR5733	8	1	24	–	16 ch.	3, 3	3, 3, 3	2	1	32	RHA
										30	DA
MSP430FR5732	8	1	24	–	10 ch.	3, 3	3	1	1	17	RGE
					12 ch.					21	PW
MSP430FR5731	4	1	24	12 ext, 2 int ch.	16 ch.	3, 3	3, 3, 3	2	1	32	RHA
										30	DA
MSP430FR5730	4	1	24	6 ext, 2 int ch.	10 ch.	3, 3	3	1	1	17	RGE
				8 ext, 2 int ch.	12 ch.					21	PW

(1) For the most current package and ordering information, see the Package Option Addendum in 节 8, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

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3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for MSP 16-Bit and 32-Bit MCUs Low-power mixed-signal processors with smart analog and digital peripherals for a wide range of industrial and consumer applications.

Products for Ultra-Low-Power MCUs MSP Ultra-Low-Power microcontrollers (MCUs) from Texas Instruments (TI) offer the lowest power consumption and the perfect mix of integrated peripherals for a wide range of low power and portable applications.

Products for MSP430FRxx FRAM MCUs 16-bit microcontrollers for ultra-low-power sensing and system management in building automation, smart grid, and industrial designs.

Companion Products for MSP430FR5739 Review products that are frequently purchased or used in conjunction with this product.

Reference Designs for MSP430FR5739 TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

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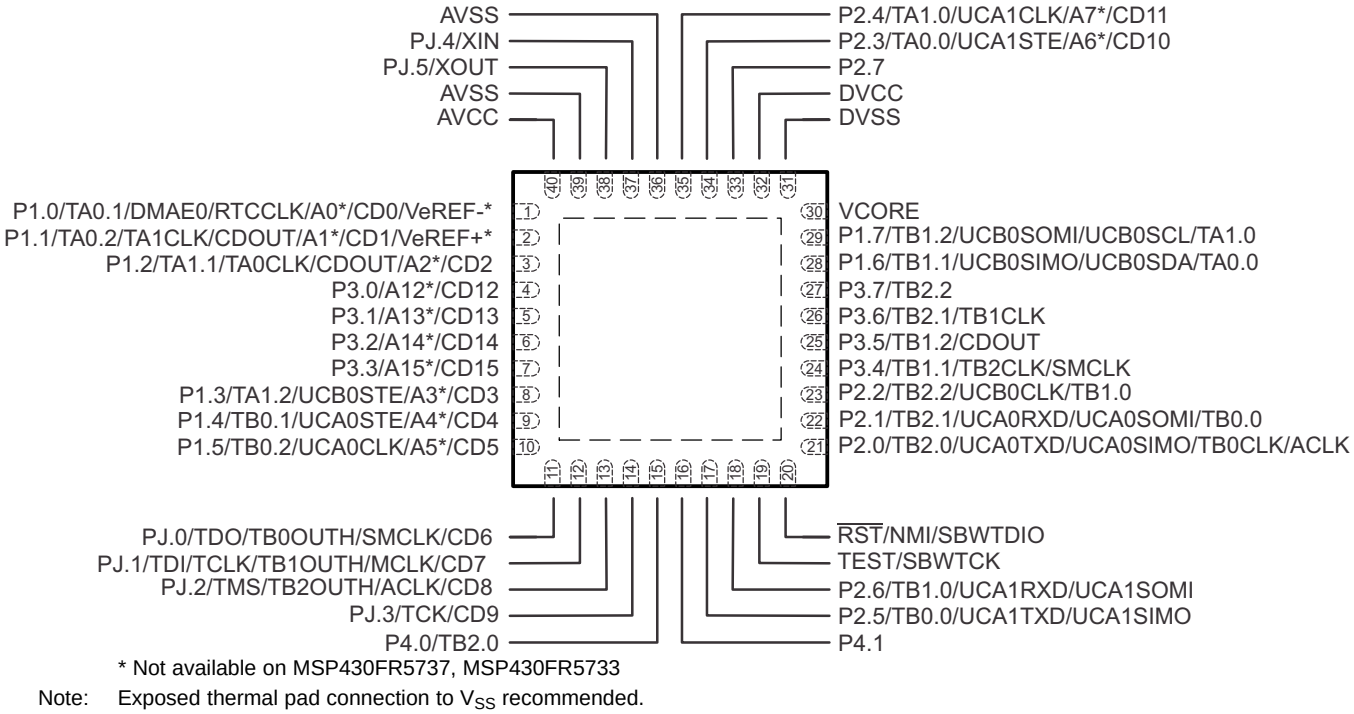
4 Terminal Configuration and Functions

4.1 Pin Diagram – RHA Package – MSP430FR5731, MSP430FR5733, MSP430FR5735, MSP430FR5737, MSP430FR5739

Figure 4-1 shows the pin diagram for the MSP430FR5731, MSP430FR5733, MSP430FR5735, MSP430FR5737, and MSP430FR5739 devices in the 40-pin RHA package.



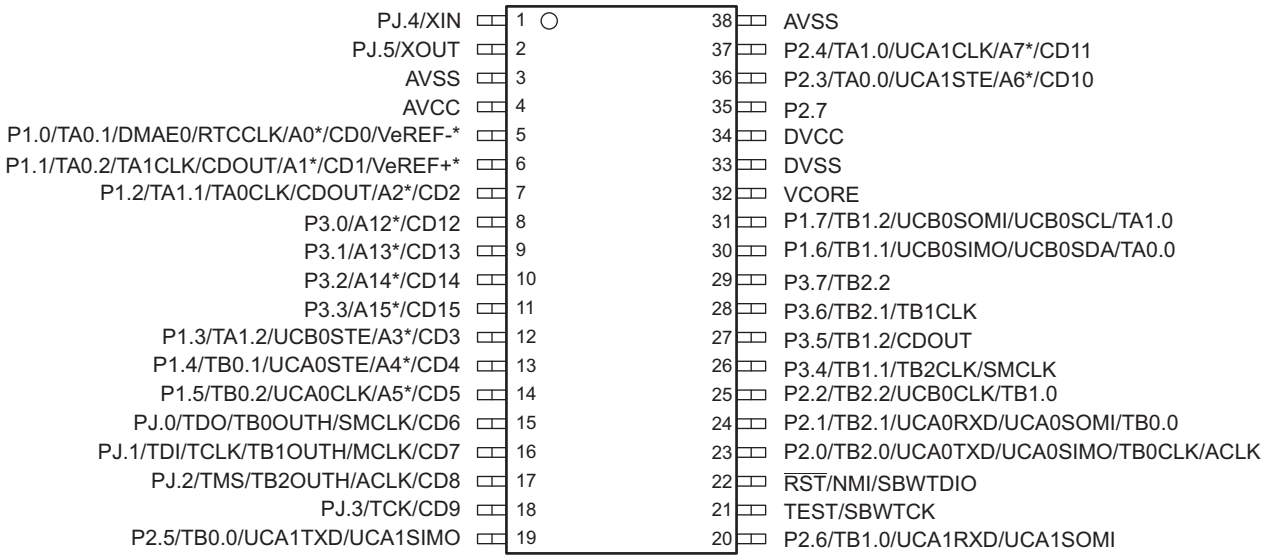
* Not available on MSP430FR5737, MSP430FR5733

Note: Exposed thermal pad connection to V_{SS} recommended.

Figure 4-1. 40-Pin RHA Package (Top View)

4.2 Pin Diagram – DA Package – MSP430FR5731, MSP430FR5733, MSP430FR5735, MSP430FR5737, MSP430FR5739

Figure 4-2 shows the pin diagram for the MSP430FR5731, MSP430FR5733, MSP430FR5735, MSP430FR5737, and MSP430FR5739 devices in the 38-pin DA package.

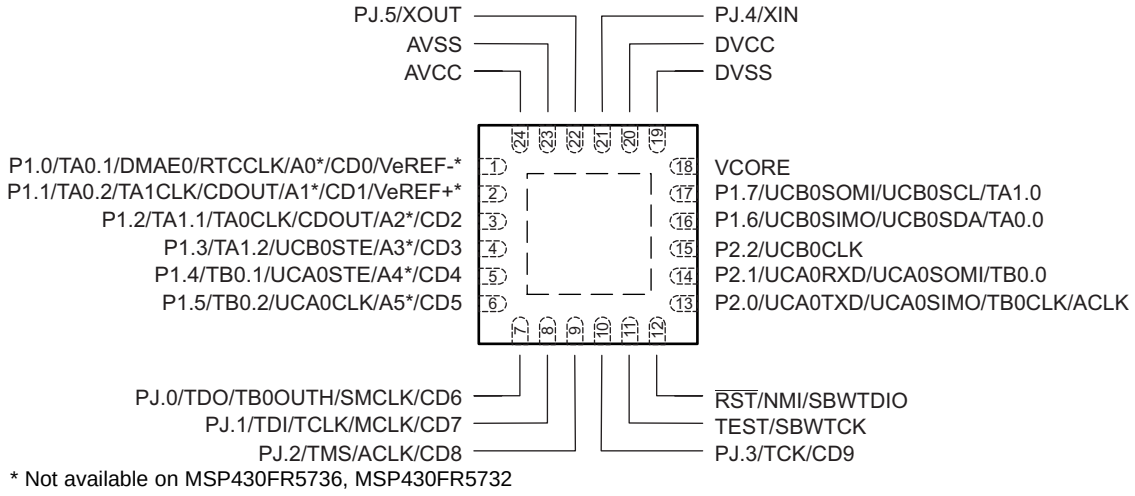


* Not available on MSP430FR5737, MSP430FR5733

Figure 4-2. 38-Pin DA Package (Top View)

4.3 Pin Diagram – RGE Package – MSP430FR5730, MSP430FR5732, MSP430FR5734, MSP430FR5736, MSP430FR5738

Figure 4-3 shows the pin diagram for the MSP430FR5730, MSP430FR5732, MSP430FR5734, MSP430FR5736, and MSP430FR5738 devices in the 24-pin RGE package.



* Not available on MSP430FR5736, MSP430FR5732

Note: Exposed thermal pad connection to V_{SS} recommended.

Figure 4-3. 24-Pin RGE Package (Top View)

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4.4 Pin Diagram – YQD Package – MSP430FR5738

Figure 4-4 shows the pin diagram for the MSP430FR5738 device in the 24-pin YQD package,

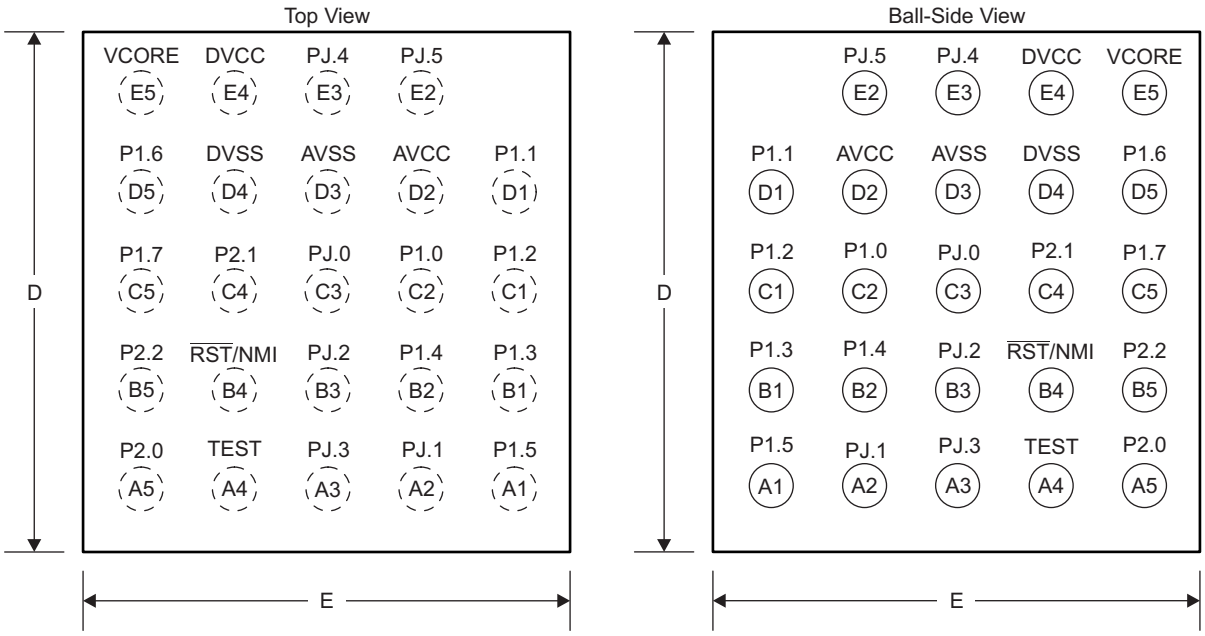
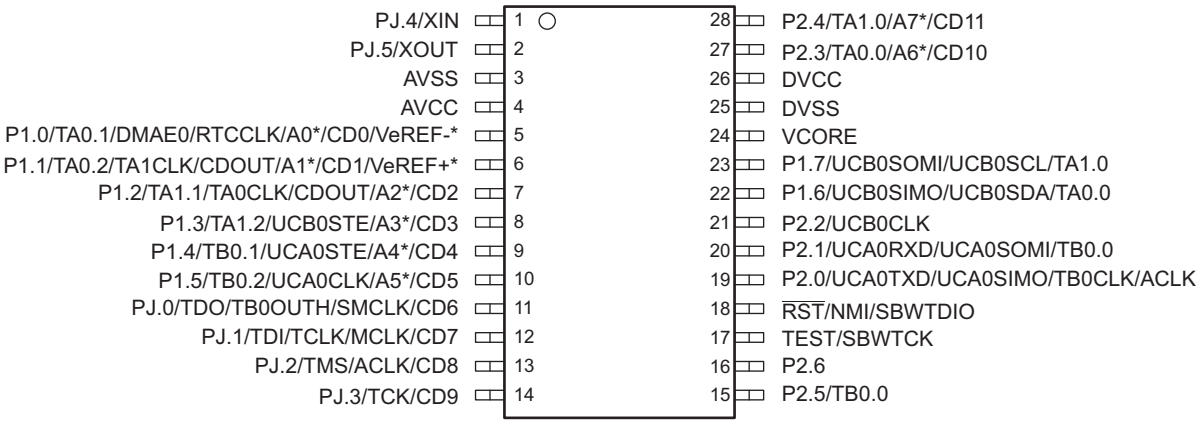


Figure 4-4. 24-Pin YQD Package

4.5 Pin Diagram – PW Package – MSP430FR5730, MSP430FR5732, MSP430FR5734, MSP430FR5736, MSP430FR5738

Figure 4-5 shows the pin diagram for the MSP430FR5730, MSP430FR5732, MSP430FR5734, MSP430FR5736, and MSP430FR5738 devices in the 28-pin PW package.



* Not available on MSP430FR5736, MSP430FR5732

Figure 4-5. 28-Pin PW Package (Top View)

4.6 Signal Descriptions

Table 4-1 describes the signals for all device variants and packages.

Table 4-1. Signal Descriptions

TERMINAL						I/O (1)	DESCRIPTION
NAME	NO.						
	RHA	RGE	DA	PW	YQD		
P1.0/TA0.1/DMAE0/ RTCCLK/A0/CD0/VeREF-	1	1	5	5	C2	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TA0 CCR1 capture: CCI1A input, compare: Out1 External DMA trigger RTC clock calibration output Analog input A0 – ADC (not available on devices without ADC) Comparator_D input CD0 External applied reference voltage (not available on devices without ADC)
P1.1/TA0.2/TA1CLK/ CDOUT/A1/CD1/VeREF+	2	2	6	6	D1	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TA0 CCR2 capture: CCI2A input, compare: Out2 TA1 input clock Comparator_D output Analog input A1 – ADC (not available on devices without ADC) Comparator_D input CD1 Input for an external reference voltage to the ADC (not available on devices without ADC)
P1.2/TA1.1/TA0CLK/ CDOUT/A2/CD2	3	3	7	7	C1	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TA1 CCR1 capture: CCI1A input, compare: Out1 TA0 input clock Comparator_D output Analog input A2 – ADC (not available on devices without ADC) Comparator_D input CD2
P3.0/A12/CD12	4	N/A	8	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE, YQD) Analog input A12 – ADC (not available on devices without ADC or package options PW, RGE, YQD) Comparator_D input CD12 (not available on package options PW, RGE, YQD)
P3.1/A13/CD13	5	N/A	9	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE, YQD) Analog input A13 – ADC (not available on devices without ADC or package options PW, RGE, YQD) Comparator_D input CD13 (not available on package options PW, RGE, YQD)
P3.2/A14/CD14	6	N/A	10	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE, YQD) Analog input A14 – ADC (not available on devices without ADC or package options PW, RGE, YQD) Comparator_D input CD14 (not available on package options PW, RGE, YQD)

(1) I = input, O = output, N/A = not available

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Table 4-1. Signal Descriptions (continued)

TERMINAL						I/O (1)	DESCRIPTION
NAME	NO.						
	RHA	RGE	DA	PW	YQD		
P3.3/A15/CD15	7	N/A	11	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE, YQD) Analog input A15 – ADC (not available on devices without ADC or package options PW, RGE, YQD) Comparator_D input CD15 (not available on package options PW, RGE, YQD)
P1.3/TA1.2/UCB0STE/ A3/CD3	8	4	12	8	B1	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TA1 CCR2 capture: CCI2A input, compare: Out2 Slave transmit enable – eUSCI_B0 SPI mode Analog input A3 – ADC (not available on devices without ADC) Comparator_D input CD3
P1.4/TB0.1/UCA0STE/ A4/CD4	9	5	13	9	B2	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB0 CCR1 capture: CCI1A input, compare: Out1 Slave transmit enable – eUSCI_A0 SPI mode Analog input A4 – ADC (not available on devices without ADC) Comparator_D input CD4
P1.5/TB0.2/UCA0CLK/ A5/CD5	10	6	14	10	A1	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB0 CCR2 capture: CCI2A input, compare: Out2 Clock signal input – eUSCI_A0 SPI slave mode, Clock signal output – eUSCI_A0 SPI master mode Analog input A5 – ADC (not available on devices without ADC) Comparator_D input CD5
PJ.0/TDO/TB0OUTH/ SMCLK/CD6 (2)	11	7	15	11	C3	I/O	General-purpose digital I/O Test data output port Switch all PWM outputs high impedance input – TB0 SMCLK output Comparator_D input CD6
PJ.1/TDI/TCLK/TB1OUTH/ MCLK/CD7 (2)	12	8	16	12	A2	I/O	General-purpose digital I/O Test data input or test clock input Switch all PWM outputs high impedance input – TB1 (not available on devices without TB1) MCLK output Comparator_D input CD7
PJ.2/TMS/TB2OUTH/ ACLK/CD8 (2)	13	9	17	13	B3	I/O	General-purpose digital I/O Test mode select Switch all PWM outputs high impedance input – TB2 (not available on devices without TB2) ACLK output Comparator_D input CD8
PJ.3/TCK/CD9 (2)	14	10	18	14	A3	I/O	General-purpose digital I/O Test clock Comparator_D input CD9

(2) See 节 6.7 for use with JTAG function.

Table 4-1. Signal Descriptions (continued)

TERMINAL						I/O (1)	DESCRIPTION
NAME	NO.						
	RHA	RGE	DA	PW	YQD		
P4.0/TB2.0	15	N/A	N/A	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE, YQD) TB2 CCR0 capture: CCI0B input, compare: Out0 (not available on devices without TB2 or package options DA, PW, RGE, YQD)
P4.1	16	N/A	N/A	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options DA, PW, RGE, YQD)
P2.5/TB0.0/UCA1TXD/ UCA1SIMO	17	N/A	19	15	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB0 CCR0 capture: CCI0A input, compare: Out0 Transmit data – eUSCI_A1 UART mode, Slave in, master out – eUSCI_A1 SPI mode (not available on devices without UCSI_A1)
P2.6/TB1.0/UCA1RXD/ UCA1SOMI	18	N/A	20	16	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB1 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB1) Receive data – eUSCI_A1 UART mode, Slave out, master in – eUSCI_A1 SPI mode (not available on devices without UCSI_A1)
TEST/SBWTCK (2) (3)	19	11	21	17	A4	I	Test mode pin – enable JTAG pins Spy-Bi-Wire input clock
$\overline{\text{RST}}$/NMI/SBWTDIO (2) (3)	20	12	22	18	B4	I/O	Reset input active low Non-maskable interrupt input Spy-Bi-Wire data input/output
P2.0/TB2.0/UCA0TXD/ UCA0SIMO/TB0CLK/ ACLK (3)	21	13	23	19	A5	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB2 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB2) Transmit data – eUSCI_A0 UART mode Slave in, master out – eUSCI_A0 SPI mode TB0 clock input ACLK output
P2.1/TB2.1/UCA0RXD/ UCA0SOMI/TB0.0 (3)	22	14	24	20	C4	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB2 CCR1 capture: CCI1A input, compare: Out1 (not available on devices without TB2) Receive data – eUSCI_A0 UART mode Slave out, master in – eUSCI_A0 SPI mode TB0 CCR0 capture: CCI0A input, compare: Out0
P2.2/TB2.2/UCB0CLK/ TB1.0	23	15	25	21	B5	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB2 CCR2 capture: CCI2A input, compare: Out2 (not available on devices without TB2) Clock signal input – eUSCI_B0 SPI slave mode, Clock signal output – eUSCI_B0 SPI master mode TB1 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB1)

(3) See 节 6.6 and 节 6.7 for use with BSL and JTAG functions.

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Table 4-1. Signal Descriptions (continued)

TERMINAL						I/O (1)	DESCRIPTION
NAME	NO.						
	RHA	RGE	DA	PW	YQD		
P3.4/TB1.1/TB2CLK/ SMCLK	24	N/A	26	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE, YQD) TB1 CCR1 capture: CCI1B input, compare: Out1 (not available on devices without TB1) TB2 clock input (not available on devices without TB2 or package options PW, RGE, YQD) SMCLK output (not available on package options PW, RGE, YQD)
P3.5/TB1.2/CDOUT	25	N/A	27	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE, YQD) TB1 CCR2 capture: CCI2B input, compare: Out2 (not available on devices without TB1) Comparator_D output (not available on package options PW, RGE, YQD)
P3.6/TB2.1/TB1CLK	26	N/A	28	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE, YQD) TB2 CCR1 capture: CCI1B input, compare: Out1 (not available on devices without TB2) TB1 clock input (not available on devices without TB1 or package options PW, RGE, YQD)
P3.7/TB2.2	27	N/A	29	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE, YQD) TB2 CCR2 capture: CCI2B input, compare: Out2 (not available on devices without TB2 or package options PW, RGE, YQD)
P1.6/TB1.1/UCB0SIMO/ UCB0SDA/TA0.0	28	16	30	22	D5	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB1 CCR1 capture: CCI1A input, compare: Out1 (not available on devices without TB1) Slave in, master out – eUSCI_B0 SPI mode I^2C data – eUSCI_B0 I^2C mode TA0 CCR0 capture: CCI0A input, compare: Out0
P1.7/TB1.2/UCB0SOMI/ UCB0SCL/TA1.0	29	17	31	23	C5	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB1 CCR2 capture: CCI2A input, compare: Out2 (not available on devices without TB1) Slave out, master in – eUSCI_B0 SPI mode I^2C clock – eUSCI_B0 I^2C mode TA1 CCR0 capture: CCI0A input, compare: Out0
VCORE (4)	30	18	32	24	E5		Regulated core power supply (internal use only, no external current loading)
DVSS	31	19	33	25	D4		Digital ground supply
DVCC	32	20	34	26	E4		Digital power supply
P2.7	33	N/A	35	N/A	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)

(4) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

Table 4-1. Signal Descriptions (continued)

TERMINAL						I/O (1)	DESCRIPTION
NAME	NO.						
	RHA	RGE	DA	PW	YQD		
P2.3/TA0.0/UCA1STE/ A6/CD10	34	N/A	36	27	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options RGE, YQD) TA0 CCR0 capture: CCI0B input, compare: Out0 (not available on package options RGE, YQD) Slave transmit enable – eUSCI_A1 SPI mode (not available on devices without eUSCI_A1) Analog input A6 – ADC (not available on devices without ADC) Comparator_D input CD10 (not available on package options RGE, YQD)
P2.4/TA1.0/UCA1CLK/ A7/CD11	35	N/A	37	28	N/A	I/O	General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options RGE, YQD) TA1 CCR0 capture: CCI0B input, compare: Out0 (not available on package options RGE, YQD) Clock signal input – eUSCI_A1 SPI slave mode, Clock signal output – eUSCI_A1 SPI master mode (not available on devices without eUSCI_A1) Analog input A7 – ADC (not available on devices without ADC) Comparator_D input CD11 (not available on package options RGE, YQD)
AVSS	36	N/A	38	N/A	N/A		Analog ground supply
PJ.4/XIN	37	21	1	1	E3	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
PJ.5/XOUT	38	22	2	2	E2	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
AVSS	39	23	3	3	D3		Analog ground supply
AVCC	40	24	4	4	D2		Analog power supply
QFN Pad	Pad	Pad	N/A	N/A	N/A		QFN package pad. Connection to VSS recommended.

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5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}	–0.3	4.1	V
Voltage applied to any pin (excluding VCORE) (2)	–0.3	V_{CC} + 0.3	V
Diode current at any device pin		±2	mA
Maximum junction temperature, T_J		95	°C
Storage temperatureT_{stg} (3) (4) (5)	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. V_{CORE} is for internal device use only. No external DC loading or voltage should be applied.
(3) Data retention on FRAM cannot be ensured when exceeding the specified maximum storage temperature, T_{stg}.
(4) For soldering during board manufacturing, it is required to follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
(5) Programming of devices with user application code should only be performed after reflow or hand soldering. Factory programmed information, such as calibration values, are designed to withstand the temperatures reached in the current JEDEC J-STD-020 specification.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and FRAM programming (AVCC = DVCC) (1)		2.0		3.6	V
V_{SS}	Supply voltage (AVSS = DVSS)			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{VCORE}	Required capacitor at VCORE(2)			470		nF
C_{VCC}/ C_{VCORE}	Capacitor ratio of VCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(3)	No FRAM wait states(4), 2 V ≤ V_{CC} ≤ 3.6 V	0		8.0	MHz
		With FRAM wait states(4), NACCESS = {2}, NPRECHG = {1}, 2 V ≤ V_{CC} ≤ 3.6 V	0		24.0	

(1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
(2) A capacitor tolerance of ±20% or better is required.
(3) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(4) When using manual wait state control, see the *MSP430FR57xx Family User's Guide* for recommended settings for common system frequencies.

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5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3)

PARAMETER	EXECUTION MEMORY	V_{CC}	Frequency ($f_{MCLK} = f_{SMCLK}$)(4)												UNIT
			1 MHz		4 MHz		8 MHz		16 MHz		20 MHz		24 MHz		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM,\ FRAM_UNI}$(5)	FRAM	3 V	0.27		0.58		1.0		1.53		1.9		2.2		mA
$I_{AM,0\%}$(6)	FRAM 0% cache hit ratio	3 V	0.42	0.73	1.2	1.6	2.2	2.8	2.3	2.9	2.8	3.6	3.45	4.3	mA
$I_{AM,50\%}$(6) (7)	FRAM 50% cache hit ratio	3 V	0.31		0.73		1.3		1.75		2.1		2.5		mA
$I_{AM,66\%}$(6) (7)	FRAM 66% cache hit ratio	3 V	0.27		0.58		1.0		1.55		1.9		2.2		mA
$I_{AM,75\%}$(6) (7)	FRAM 75% cache hit ratio	3 V	0.25		0.5		0.82		1.3		1.6		1.8		mA
$I_{AM,100\%}$(6) (7)	FRAM 100% cache hit ratio	3 V	0.2	0.43	0.3	0.55	0.42	0.8	0.73	1.15	0.88	1.3	1.0	1.5	mA
$I_{AM,\ RAM}$(7) (8)	RAM	3 V	0.2	0.4	0.35	0.55	0.55	0.75	1.0	1.25	1.20	1.45	1.45	1.75	mA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Characterized with program executing typical data processing.
(4) At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency, $f_{MCLK,eff}$, decreases. The effective MCLK frequency is also dependent on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio. The following equation can be used to compute $f_{MCLK,eff}$:
$f_{MCLK,eff,MHZ} = f_{MCLK,MHZ} \times 1$ / [number of wait states × ((1 – cache hit ratio percent/100)) + 1]
(5) Program and data reside entirely in FRAM. No wait states enabled. DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz). MCLK = SMCLK.
(6) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 25% ratio implies one of every four accesses is from cache, the remaining are FRAM accesses.
For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz). MCLK = SMCLK. No wait states enabled.
For 16 MHz, DCORSEL = 1, DCOFSELx = 0 (f_{DCO} = 16 MHz).MCLK = SMCLK. One wait state enabled.
For 20 MHz, DCORSEL = 1, DCOFSELx = 2 (f_{DCO} = 20 MHz).MCLK = SMCLK. Three wait states enabled.
For 24 MHz, DCORSEL = 1, DCOFSELx = 3 (f_{DCO} = 24 MHz).MCLK = SMCLK. Three wait states enabled.
(7) See Figure 5-1 for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in Section 5.4.
f_{ACLK} = 32786 Hz, $f_{MCLK} = f_{SMCLK}$ at specified frequency. No peripherals active.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.
(8) All execution is from RAM.
For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz). MCLK = SMCLK.
For 16 MHz, DCORSEL = 1, DCOFSELx = 0 (f_{DCO} = 16 MHz). MCLK = SMCLK.
For 20 MHz, DCORSEL = 1, DCOFSELx = 2 (f_{DCO} = 20 MHz). MCLK = SMCLK.
For 24 MHz, DCORSEL = 1, DCOFSELx = 3 (f_{DCO} = 24 MHz). MCLK = SMCLK.

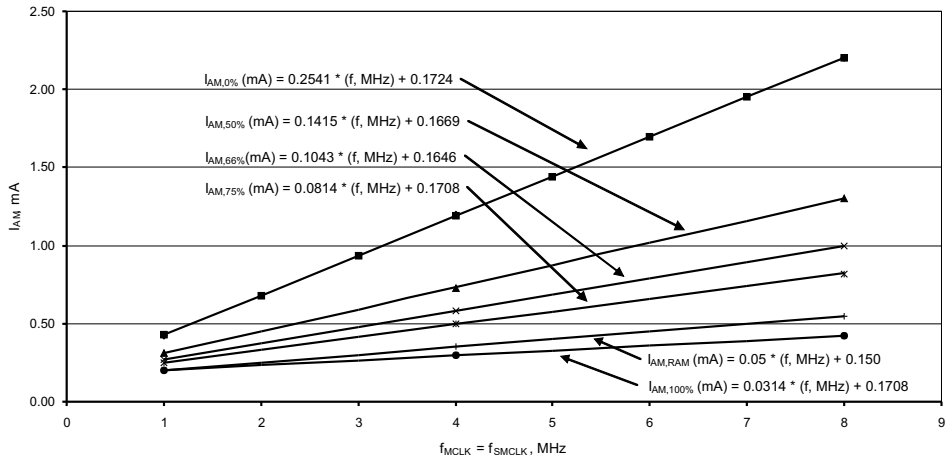

Figure 5-1. Typical Active Mode Supply Currents, No Wait States

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5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1) (2)

PARAMETER		V_{CC}	–40°C		25°C		60°C		85°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0 (3) (4)	2 V, 3 V	166		175		190		225		µA
$_{LPM0,8MHz}$	Low-power mode 0 (5) (4)	2 V, 3 V	170		177	244	195		225	360	µA
$_{LPM0,24MHz}$	Low-power mode 0 (6) (4)	2 V, 3 V	274		285	340	315		340	455	µA
I_{LPM2}	Low-power mode 2 (7) (8)	2 V, 3 V	56		61	80	75		110	210	µA
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode (9) (8)	2 V, 3 V	3.4		6.4	15	18		48	150	µA
$I_{LPM3,VLO}$	Low-power mode 3, VLO mode (10) (8)	2 V, 3 V	3.3		6.3	15	18		48	150	µA
I_{LPM4}	Low-power mode 4 (11) (8)	2 V, 3 V	2.9		5.9	15	18		48	150	µA
$I_{LPM3.5}$	Low-power mode 3.5 (12)	2 V, 3 V	1.3		1.5	2.2	1.9		2.8	5.0	µA
$I_{LPM4.5}$	Low-power mode 4.5 (13)	2 V, 3 V	0.3		0.32	0.66	0.38		0.57	2.55	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = 1 MHz. DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz)
(4) Current for brownout, high-side supervisor (SVS_H), and low-side supervisor (SVS_L) included.
(5) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = 8 MHz. DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz)
(6) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = 24 MHz. DCORSEL = 1, DCOFSELx = 3 (f_{DCO} = 24 MHz)
(7) Current for watchdog timer (clocked by ACLK) and RTC (clocked by XT1 LF mode) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz, DCORSEL = 0, DCOFSELx = 3, DCO bias generator enabled.
(8) Current for brownout and high-side supervisor (SVS_H) included. Low-side supervisor (SVS_L) disabled.
(9) Current for watchdog timer (clocked by ACLK) and RTC (clocked by XT1 LF mode) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
(10) Current for watchdog timer (clocked by ACLK) included. ACLK = VLO.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = f_{VLO}, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
(11) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
(12) Internal regulator disabled. No data retention. RTC active clocked by XT1 LF mode.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM3.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
(13) Internal regulator disabled. No data retention.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

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5.6 Thermal Resistance Characteristics

PARAMETER		PACKAGE	VALUE(1)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air(2)	TSSOP-24 (PW)	78.8	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(3)		19.4	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)		36.7	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		36.2	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.5	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(5)		N/A	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air(2)	QFN-24 (RGE)	42.1	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(3)		38.8	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)		18.1	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		18.0	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.6	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(5)		2.8	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air(2)	SOIC-38 (DA)	74.5	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(3)		22.0	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)		40.7	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		40.3	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.9	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(5)		N/A	°C/W
θ_{JA}	Junction-to-ambient thermal resistance, still air(2)	QFN-40 (RHA)	37.8	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(3)		27.4	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)		12.6	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		12.6	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.4	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(5)		3.6	°C/W

(1) N/A = Not applicable
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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5.7 Schmitt-Trigger Inputs – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		2 V	0.45		1.10	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)		2 V	0.25		0.8	V
			3 V	0.30		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

5.8 Inputs – Ports P1 and P2 (1) (P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing (2)	External trigger pulse duration to set interrupt flag	2 V, 3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

5.9 Leakage Current – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	(1) (2)	2 V, 3 V	–50	50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

5.10 Outputs – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA (1)	2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA (2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA (1)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA (2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA (1)	2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA (2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA (1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA (2)		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

5.11 Output Frequency – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	Px.y (1) (2)	2 V		16	MHz
			3 V		24	
f_{Port_CLK}	Clock output frequency	ACLK, SMCLK, or MCLK at configured output port, C_L = 20 pF, no DC loading (2)	2 V		16	MHz
			3 V		24	

(1) A resistive divider with 2 × 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected from the output to V_{SS}.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

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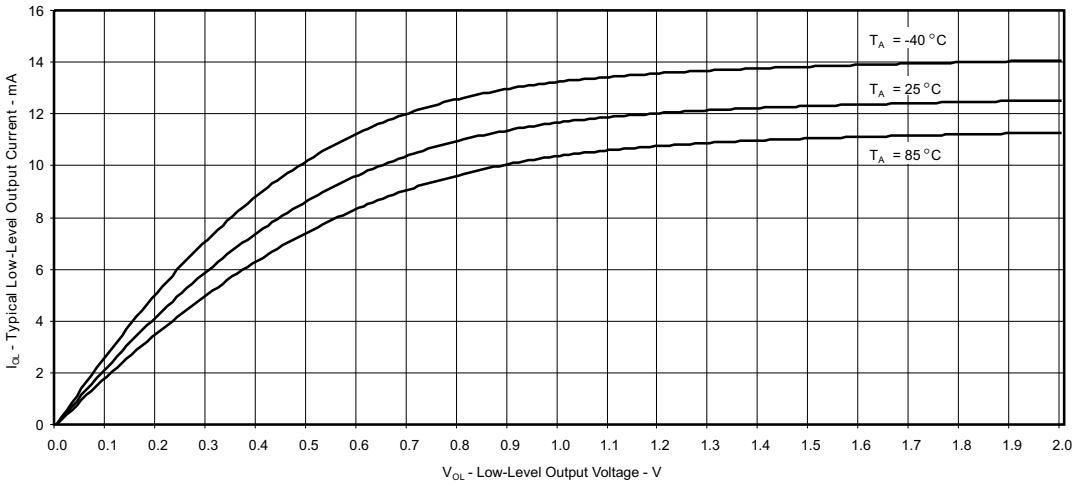
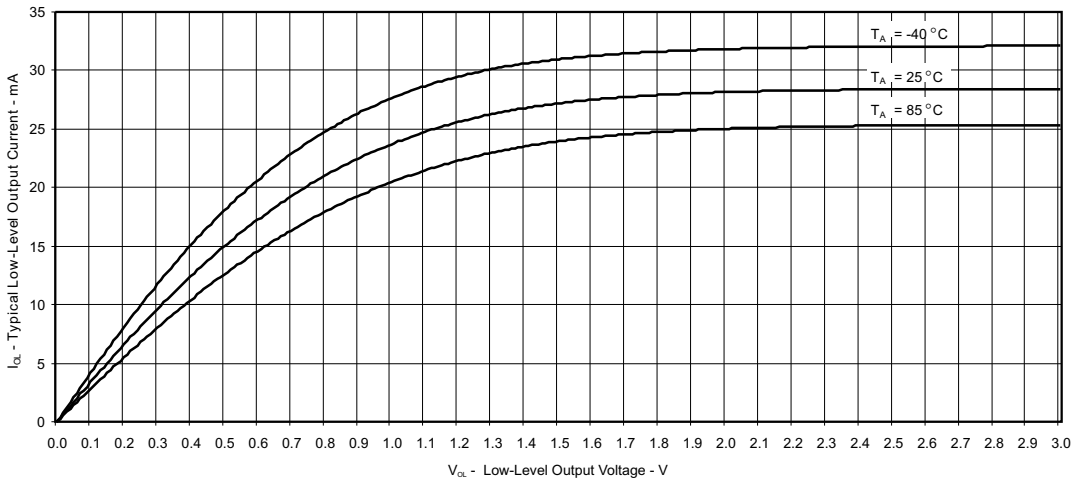
5.12 Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



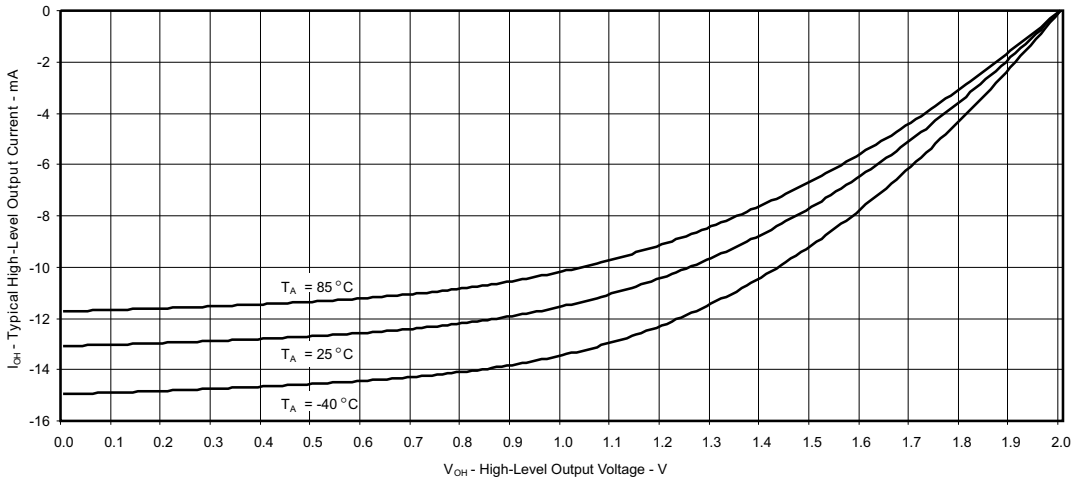
V_{CC} = 2.0 V Measured at Px.y

Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage



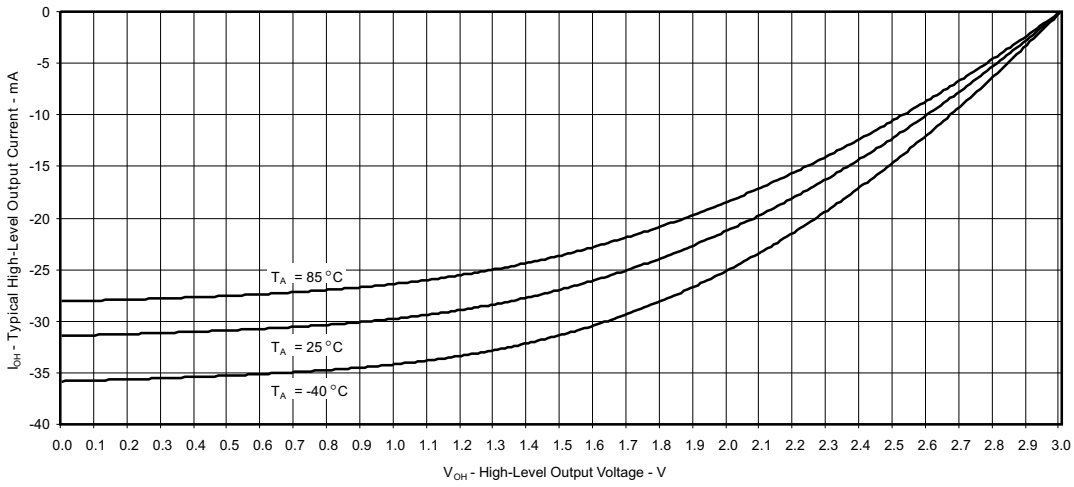
V_{CC} = 3.0 V Measured at Px.y

Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 2.0 V Measured at Px.y

Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage



V_{CC} = 3.0 V Measured at Px.y

Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

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5.13 Crystal Oscillator, XT1, Low-Frequency (LF) Mode (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{VCC.LF}$	Additional current consumption XT1 LF mode from lowest drive setting	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {1}, $C_{L,eff}$ = 9 pF, T_A = 25°C,	3 V		60		nA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {2}, T_A = 25°C, $C_{L,eff}$ = 9 pF	3 V		90		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12 pF	3 V		140		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1 (2) (3)		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals (4)	XTS = 0, XT1BYPASS = 0, XT1DRIVE = {0}, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30%		70%	
$f_{Fault,LF}$	Oscillator fault frequency, LF mode (5)	XTS = 0 (6)		10		10000	Hz
$t_{START,LF}$	Start-up time, LF mode (7)	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 6 pF	3 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12 pF			1000		
$C_{L,eff}$	Integrated effective load capacitance, LF mode (8) (9)	XTS = 0			1		pF

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVE = {0}, $C_{L,eff} \le 6$ pF.
- For XT1DRIVE = {1}, 6 pF $\le C_{L,eff} \le$ 9 pF.
- For XT1DRIVE = {2}, 6 pF $\le C_{L,eff} \le$ 10 pF.
- For XT1DRIVE = {3}, 6 pF $\le C_{L,eff} \le$ 12 pF.

(5) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(6) Measured with logic-level input frequency but also applies to operation with crystals.
(7) Includes start-up counter of 4096 clock cycles.
(8) Requires external capacitors at both terminals.
(9) Values are specified by crystal manufacturers. Include parasitic bond and package capacitance (approximately 2 pF per pin). Recommended values supported are 6 pF, 9 pF, and 12 pF. Maximum shunt capacitance of 1.6 pF.

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5.14 Crystal Oscillator, XT1, High-Frequency (HF) Mode (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{VCC,HF}$	XT1 oscillator crystal current HF mode	f_{OSC} = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 16 pF	3 V		175		µA
		f_{OSC} = 8 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {1}, T_A = 25°C, $C_{L,eff}$ = 16 pF			300		
		f_{OSC} = 16 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {2}, T_A = 25°C, $C_{L,eff}$ = 16 pF			350		
		f_{OSC} = 24 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 16 pF			550		
$f_{XT1,HF0}$	XT1 oscillator crystal frequency, HF mode 0	XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0} (2)		4		6	MHz
$f_{XT1,HF1}$	XT1 oscillator crystal frequency, HF mode 1	XTS = 1, XT1BYPASS = 0, XT1DRIVE = {1} (2)		6		10	MHz
$f_{XT1,HF2}$	XT1 oscillator crystal frequency, HF mode 2	XTS = 1, XT1BYPASS = 0, XT1DRIVE = {2} (2)		10		16	MHz
$f_{XT1,HF3}$	XT1 oscillator crystal frequency, HF mode 3	XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3} (2)		16		24	MHz
$f_{XT1,HF,SW}$	XT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, XT1BYPASS = 1 (3) (2)		1		24	MHz
OA_{HF}	Oscillation allowance for HF crystals (4)	XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0}, $f_{XT1,HF}$ = 4 MHz, $C_{L,eff}$ = 16 pF			450		Ω
		XTS = 1, XT1BYPASS = 0, XT1DRIVE = {1}, $f_{XT1,HF}$ = 8 MHz, $C_{L,eff}$ = 16 pF			320		
		XTS = 1, XT1BYPASS = 0, XT1DRIVE = {2}, $f_{XT1,HF}$ = 16 MHz, $C_{L,eff}$ = 16 pF			200		
		XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3}, $f_{XT1,HF}$ = 24 MHz, $C_{L,eff}$ = 16 pF			200		
$t_{START,HF}$	Start-up time, HF mode (5)	f_{OSC} = 4 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0}, T_A = 25°C, $C_{L,eff}$ = 16 pF	3 V		8		ms
		f_{OSC} = 24 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 16 pF			2		

(1) To improve EMI on the XT1 oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) Maximum frequency of operation of the entire device cannot be exceeded.
(3) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(5) Includes start-up counter of 4096 clock cycles.

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Crystal Oscillator, XT1, High-Frequency (HF) Mode [1] *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$C_{L,eff}$	Integrated effective load capacitance [6] [7]	XTS = 1			1		pF
	Duty cycle, HF mode	XTS = 1, Measured at ACLK, $f_{XT1,HF2}$ = 24 MHz		40%	50%	60%	
$f_{Fault,HF}$	Oscillator fault frequency, HF mode [8]	XTS = 1 [9]		145		900	kHz

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(7) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF.
(8) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specificiations might set the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

5.15 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	2 V to 3.6 V	5	8.3	13	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK [1]	2 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK [2]	2 V to 3.6 V		4		%/V
$f_{VLO,DC}$	Duty cycle	Measured at ACLK	2 V to 3.6 V	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(2.0 V to 3.6 V) – MIN(2.0 V to 3.6 V)) / MIN(2.0 V to 3.6 V) / (3.6 V – 2 V)

NOTE

In LPM3, the VLO frequency varies by up to ±6% (typical), due to bias current sampling. This frequency variation is not a violation VLO specifications (see Section 5.15).

5.16 DCO Frequencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC} T_A	MIN	TYP	MAX	UNIT
$f_{DCO,LO}$	DCO frequency low, trimmed	Measured at ACLK, DCORSEL = 0	2 V to 3.6 V –40°C to 85°C		5.37	±3.5%	MHz
			2 V to 3.6 V 0°C to 50°C		5.37	±2.0%	
		Measured at ACLK, DCORSEL = 1	2 V to 3.6 V –40°C to 85°C		16.2	±3.5%	
			2 V to 3.6 V 0°C to 50°C		16.2	±2.0%	
$f_{DCO,MID}$	DCO frequency mid, trimmed	Measured at ACLK, DCORSEL = 0	2 V to 3.6 V –40°C to 85°C		6.67	±3.5%	MHz
			2 V to 3.6 V 0°C to 50°C		6.67	±2.0%	
		Measured at ACLK, DCORSEL = 1	2 V to 3.6 V –40°C to 85°C		20	±3.5%	
			2 V to 3.6 V 0°C to 50°C		20	±2.0%	
$f_{DCO,HI}$	DCO frequency high, trimmed	Measured at ACLK, DCORSEL = 0	2 V to 3.6 V –40°C to 85°C		8	±3.5%	MHz
			2 V to 3.6 V 0°C to 50°C		8	±2.0%	
		Measured at ACLK, DCORSEL = 1	2 V to 3.6 V –40°C to 85°C		23.8	±3.5%	
			2 V to 3.6 V 0°C to 50°C		23.8	±2.0%	
$f_{DCO,DC}$	Duty cycle	Measured at ACLK, divide by 1, No external divide, all DCO settings	2 V to 3.6 V –40°C to 85°C	40%	50%	60%	

5.17 MODOSC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{MODOSC}	Current consumption	Enabled	2 V to 3.6 V		44	80	µA
f_{MODOSC}	MODOSC frequency		2 V to 3.6 V	4.5	5.0	5.5	MHz
$f_{MODOSC,DC}$	Duty cycle	Measured at ACLK, divide by 1	2 V to 3.6 V	40%	50%	60%	

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5.18 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CORE}(AM)	Core voltage, active mode	2 V ≤ DV_{CC} ≤ 3.6 V		1.5		V
V_{CORE}(LPM)	Core voltage, low-current mode	2 V ≤ DV_{CC} ≤ 3.6 V		1.5		V

5.19 PMM, SVS, BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SVSH,AM}$	SVS_H current consumption, active mode	V_{CC} = 3.6 V		5		µA
$I_{SVSH,LPM}$	SVS_H current consumption, low power modes	V_{CC} = 3.6 V		0.8	1.5	µA
V_{SVSH-}	SVS_H on voltage level, falling supply voltage		1.83	1.88	1.93	V
V_{SVSH+}	SVS_H off voltage level, rising supply voltage		1.88	1.93	1.98	V
$t_{PD,SVSH, AM}$	SVS_H propagation delay, active mode	dV_{CC}/dt = 10 mV/µs		10		µs
$t_{PD,SVSH, LPM}$	SVS_H propagation delay, low power modes	dV_{CC}/dt = 1 mV/µs		30		µs
I_{SVSL}	SVS_L current consumption			0.3	0.5	µA
$V_{SVSL–}$	SVS_L on voltage level			1.42		V
V_{SVSL+}	SVS_L off voltage level			1.47		V

5.20 Wake-up Times From Low-Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC} T_A	MIN	TYP	MAX	UNIT
$t_{WAKE-UP\ LPM0}$	Wake-up time from LPM0 to active mode (1)		2 V, 3 V –40°C to 85°C		0.58	1	µs
$t_{WAKE-UP\ LPM12}$	Wake-up time from LPM1, LPM2 to active mode (1)		2 V, 3 V –40°C to 85°C		12	25	µs
$t_{WAKE-UP\ LPM34}$	Wake-up time from LPM3 or LPM4 to active mode (1)		2 V, 3 V –40°C to 85°C		78	120	µs
$t_{WAKE-UP\ LPMx.5}$	Wake-up time from LPM3.5 or LPM4.5 to active mode (1)		2 V, 3 V 0°C to 85°C		310	575	µs
			2 V, 3 V –40°C to 85°C		310	1100	
$t_{WAKE-UP\ RESET}$	Wake-up time from $\overline{RST}$ to active mode (2)	V_{CC} stable	2 V, 3 V –40°C to 85°C		230	280	µs
$t_{WAKE-UP\ BOR}$	Wake-up time from BOR or power-up to active mode	dV_{CC}/dt = 2400 V/s	2 V, 3 V –40°C to 85°C		1.6		ms
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI terminal to accept a reset event (3)		2 V, 3 V –40°C to 85°C	4			ns

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.
(2) The wake-up time is measured from the rising edge of the $\overline{RST}$ signal until the first instruction of the user program is executed.
(3) Meeting or exceeding this time makes sures a reset event occurs. Pulses shorter than this minimum time may or may not cause a reset event to occur.

5.21 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ±10%	2 V, 3 V			24	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	2 V, 3 V	20			ns

5.22 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK, ACLK External: TBCLK Duty cycle = 50% ±10%	2 V, 3 V			24	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, Minimum pulse duration required for capture	2 V, 3 V	20			ns

5.23 eUSCI (UART Mode) Clock Frequency

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)					5	MHz

5.24 eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time(1)	UCGLITx = 0	2 V, 3 V	5	15	20	ns
		UCGLITx = 1		20	45	60	
		UCGLITx = 2		35	80	120	
		UCGLITx = 3		50	110	180	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

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5.25 eUSCI (SPI Master Mode) Clock Frequency

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, ACLK Duty cycle = 50% ±10%				f_{SYSTEM}	MHz

5.26 eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 0, UCMODEx = 01 or 10	2 V, 3 V	1			UCxCLK cycles
		UCSTEM = 1, UCMODEx = 01 or 10	2 V, 3 V	1			
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 0, UCMODEx = 01 or 10	2 V, 3 V	1			UCxCLK cycles
		UCSTEM = 1, UCMODEx = 01 or 10	2 V, 3 V	1			
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	2 V, 3 V			55	ns
		UCSTEM = 1, UCMODEx = 01 or 10	2 V, 3 V			35	
$t_{STE,DIS}$	STE disable time, STE inactive to SIMO high impedance	UCSTEM = 0, UCMODEx = 01 or 10	2 V, 3 V			40	ns
		UCSTEM = 1, UCMODEx = 01 or 10	2 V, 3 V			30	
$t_{SU,MI}$	SOMI input data setup time		2 V	35			ns
			3 V	35			
$t_{HD,MI}$	SOMI input data hold time		2 V	0			ns
			3 V	0			
$t_{VALID,MO}$	SIMO output data valid time (2)	UCLK edge to SIMO valid, C_L = 20 pF	2 V			30	ns
			3 V			30	
$t_{HD,MO}$	SIMO output data hold time (3)	C_L = 20 pF	2 V	0			ns
			3 V	0			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in 图 5-6 and 图 5-7.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in 图 5-6 and 图 5-7.

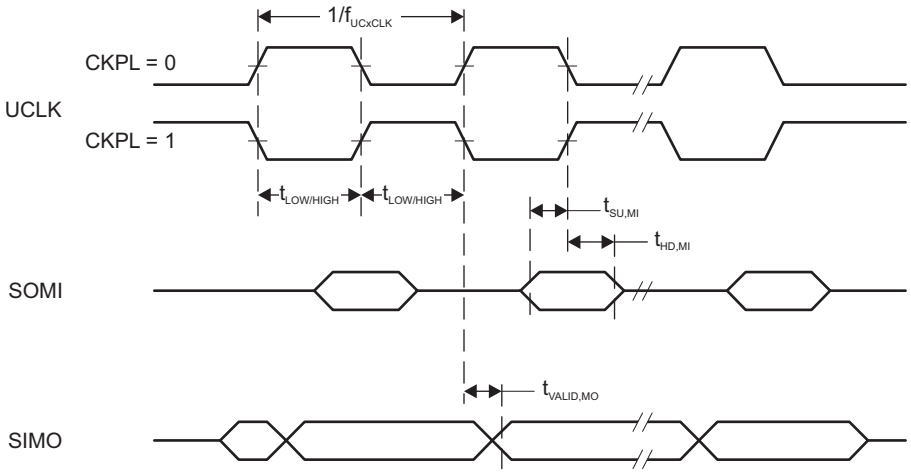

图 5-6. SPI Master Mode, CKPH = 0

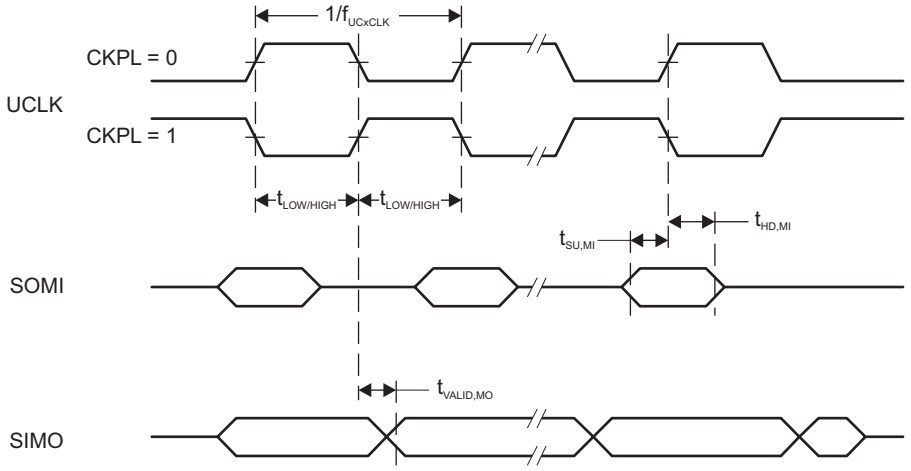

图 5-7. SPI Master Mode, CKPH = 1

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5.27 eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2 V	7			ns
			3 V	7			
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		2 V	0			ns
			3 V	0			
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2 V			65	ns
			3 V			40	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2 V			40	ns
			3 V			35	
$t_{SU,SI}$	SIMO input data setup time		2 V	2			ns
			3 V	2			
$t_{HD,SI}$	SIMO input data hold time		2 V	5			ns
			3 V	5			
$t_{VALID,SO}$	SOMI output data valid time (2)	UCLK edge to SOMI valid, C_L = 20 pF	2 V			30	ns
			3 V			30	
$t_{HD,SO}$	SOMI output data hold time (3)	C_L = 20 pF	2 V	4			ns
			3 V	4			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in 图 5-8 and 图 5-9.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in 图 5-8 and 图 5-9.

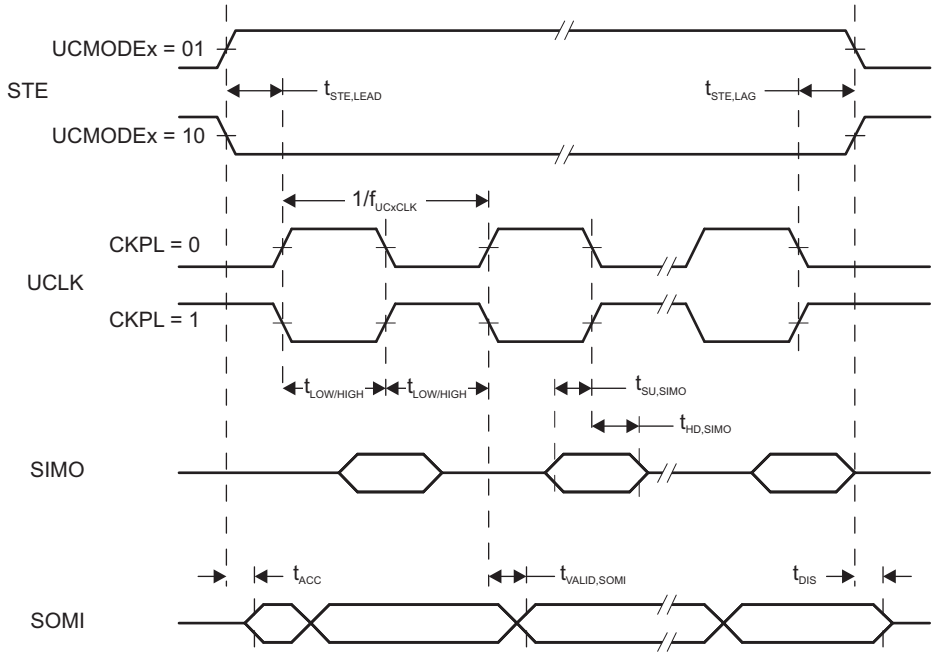

图 5-8. SPI Slave Mode, CKPH = 0

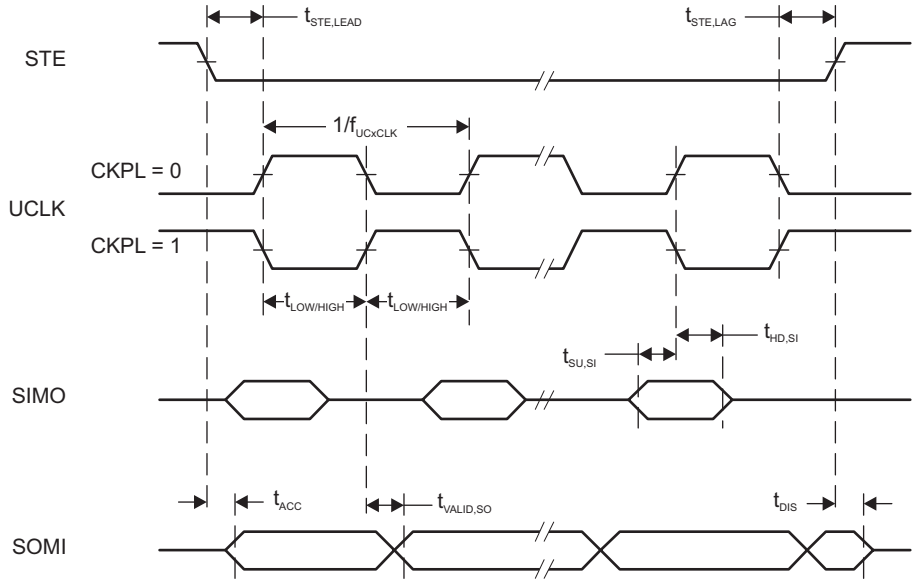

图 5-9. SPI Slave Mode, CKPH = 1

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5.28 eUSCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 5-10)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2 V, 3 V	50		600	ns
		UCGLITx = 1		25		300	
		UCGLITx = 2		12.5		150	
		UCGLITx = 3		6.25		75	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1	2 V, 3 V		27		ms
		UCCLTOx = 2			30		
		UCCLTOx = 3			33		

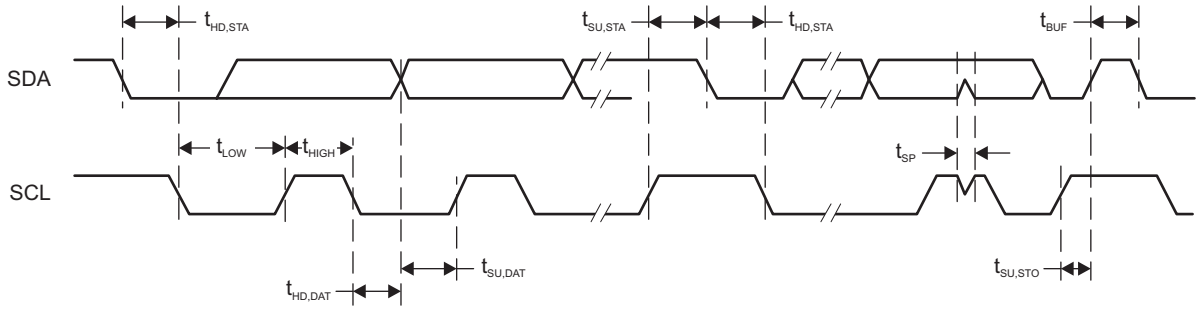

图 5-10. I^2C Mode Timing

5.29 10-Bit ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.0		3.6	V
$V_{(Ax)}$	Analog input voltage range	All ADC10 pins		0		AV_{CC}	V
I_{ADC10_A}	Operating supply current into AVCC terminal, reference current not included	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0	2 V		90	140	µA
			3 V		100	160	
C_I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad	2.2 V		6	8	pF
R_I	Input MUX ON resistance	$AV_{CC} \geq 2$ V, $0 V \leq V_{Ax} \leq AV_{CC}$				36	kΩ

5.30 10-Bit ADC, Timing Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$		For specified performance of ADC10 linearity parameters	2 V to 3.6 V	0.45	5	5.5	MHz
$f_{ADC10OSC}$	Internal ADC10 oscillator (MODOSC)	ADC10DIV = 0, $f_{ADC10CLK} = f_{ADC10OSC}$	2 V to 3.6 V	4.5	4.5	5.5	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, $f_{ADC10OSC}$ = 4.5 MHz to 5.5 MHz	2 V to 3.6 V	2.18		2.67	µs
		External $f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK, ADC10SSEL ≠ 0	2 V to 3.6 V		(1)		
$t_{ADC10ON}$	Turnon settling time of the ADC	The error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB, Reference and input signal already settled				100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I = 36000 Ω, C_I = 3.5 pF, Approximately eight Tau (τ) are required to get an error of less than ±0.5 LSB	2 V	1.5			µs
			3 V	2.0			

(1) $12 \times ADC10DIV \times 1/f_{ADC10CLK}$

5.31 10-Bit ADC, Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	$1.4 V \leq (V_{eREF+} - V_{REF-}/V_{eREF-})min \leq 1.6$ V	2 V to 3.6 V	–1.4		1.4	LSB
		$1.6 V < (V_{eREF+} - V_{REF-}/V_{eREF-})min \leq V_{AVCC}$		–1.1		1.1	
E_D	Differential linearity error	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$	2 V to 3.6 V	–1		1	LSB
E_O	Offset error	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$	2 V to 3.6 V	–6.5		6.5	mV
E_G	Gain error, external reference	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$	2 V to 3.6 V	–1.2		1.2	LSB
	Gain error, internal reference (1)			–4%		4%	
E_T	Total unadjusted error, external reference	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$	2 V to 3.6 V	–2		2	LSB
	Total unadjusted error, internal reference (1)			–4%		4%	

(1) Error is dominated by the internal reference.

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5.32 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{eREF-}$ (2)		1.4		AV_{CC}	V
V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{eREF-}$ (3)		0		1.2	V
(V_{eREF+} – V_{REF-}/V_{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{eREF-}$ (4)		1.4		AV_{CC}	V
I_{VeREF+}, I_{VeREF-}	Static input current	1.4 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 1h, Conversion rate 200 ksps	2.2 V, 3 V	–6		6	µA
		1.4 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 8h, Conversion rate 20 ksps	2.2 V, 3 V	–1		1	
C_{VREF+}, C_{VREF-}	Capacitance at VREF+ or VREF- terminal (5)			10			µF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_B. Also see the *MSP430FR57xx Family User's Guide*.

5.33 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = 1	3 V	2.4	2.5	2.6	V
		REFVSEL = {1} for 2 V, REFON = 1	3 V	1.92	2.0	2.08	
		REFVSEL = {0} for 1.5 V, REFON = 1	3 V	1.44	1.5	1.56	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.5 V		2.0			V
		REFVSEL = {1} for 2 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
I_{REF+}	Operating supply current into AVCC terminal (1)	$f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0	3 V		33	45	µA
T_{REF+}	Temperature coefficient of built-in reference	REFVSEL = (0, 1, 2}, REFON = 1			±35		ppm/°C
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, T_A = 25°C, REFON = 1, REFVSEL = (0} for 1.5 V			1600		µV/V
		AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, T_A = 25°C, REFON = 1, REFVSEL = (1} for 2 V			1900		
		AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, T_A = 25°C, REFON = 1, REFVSEL = (2} for 2.5 V			3600		
t_{SETTLE}	Settling time of reference voltage (2)	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, REFVSEL = (0, 1, 2}, REFON = 0 → 1			30		µs

(1) The internal reference current is supplied by terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
(2) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.34 REF, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	See (1)	ADC10ON = 1, INCH = 0Ah, T_A = 0°C	2 V, 3 V		790		mV
TC_{SENSOR}		ADC10ON = 1, INCH = 0Ah	2 V, 3 V		2.55		mV/°C
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (2)	ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2 V	30			µs
			3 V	30			
V_{MID}	AV_{CC} divider at channel 11	ADC10ON = 1, INCH = 0Bh, V_{MID} is ~0.5 × V_{AVCC}	2 V	0.97	1.0	1.03	V
			3 V	1.46	1.5	1.54	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (3)	ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2 V, 3 V	1000			ns

(1) The temperature sensor offset can vary significantly. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
(2) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(3) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

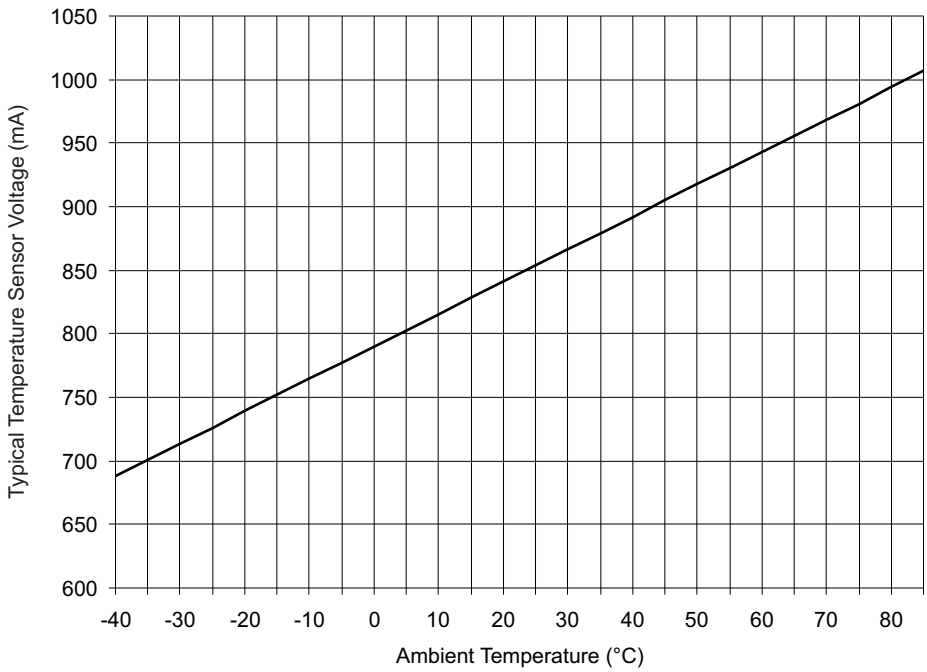

图 5-11. Typical Temperature Sensor Voltage

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5.35 Comparator_D

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay, AVCC = 2 V to 3.6 V	Overdrive = 10 mV, VIN- = (VIN+ – 400 mV) to (VIN+ + 10 mV)	50	100	200	ns
		Overdrive = 100 mV, VIN- = (VIN+ – 400 mV) to (VIN+ + 100 mV)		80		
		Overdrive = 250 mV, (VIN+ – 400 mV) to (VIN+ + 250 mV)		50		
t_{filter}	Filter timer added to the propagation delay of the comparator	CDF = 1, CDFDLY = 00	0.3	0.5	0.9	µs
		CDF = 1, CDFDLY = 01	0.5	0.9	1.5	
		CDF = 1, CDFDLY = 10	0.9	1.6	2.8	
		CDF = 1, CDFDLY = 11	1.6	3.0	5.5	
V_{offset}	Input offset	AVCC = 2 V to 3.6 V	–20		20	mV
V_{ic}	Common mode input range	AVCC = 2 V to 3.6 V	0		AVCC - 1	V
$I_{comp(AVCC)}$	Comparator only	CDON = 1, AVCC = 2 V to 3.6 V		29	34	µA
$I_{ref(AVCC)}$	Reference buffer and R-ladder	CDREFLx = 01, AVCC = 2 V to 3.6 V		20	24	µA
$t_{enable,comp}$	Comparator enable time	CDON = 0 to CDON = 1, AVCC = 2 V to 3.6 V		1.1	2.0	µs
$t_{enable,rladder}$	Resistor ladder enable time	CDON = 0 to CDON = 1, AVCC = 2 V to 3.6 V		1.1	2.0	µs
V_{CB_REF}	Reference voltage for a tap	VIN = voltage input to the R-ladder, n = 0 to 31	VIN × (n + 0.5) / 32	VIN × (n + 1) / 32	VIN × (n + 1.5) / 32	V

5.36 FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DV_{CC(WRITE)}$	Write supply voltage		2.0		3.6	V
t_{WRITE}	Word or byte write time				120	ns
t_{ACCESS}	Read access time (1)				60	ns
$t_{PRECHARGE}$	Precharge time (1)				60	ns
t_{CYCLE}	Cycle time, read or write operation (1)		120			ns
	Read and write endurance		10^{15}			cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
		T_J = 70°C	40			
		T_J = 85°C	10			

(1) When using manual wait state control, see the *MSP430FR57xx Family User's Guide* for recommended settings for common system frequencies.

5.37 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2 V, 3 V	0.025		15	µs
$t_{SBW,\ En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2 V, 3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		19		35	µs
f_{TCK}	TCK input frequency, 4-wire JTAG (2)	2 V	0		5	MHz
		3 V	0		10	
$R_{internal}$	Internal pulldown resistance on TEST	2 V, 3 V	20	35	50	kΩ

(1) Tools that access the Spy-Bi-Wire and BSL interfaces must wait for the $t_{SBW,En}$ time after the first transition of the TEST/SBWTCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

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6 Detailed Description

6.1 Functional Block Diagrams

图 6-1 shows the functional block diagram for the MSP430FR5731, MSP430FR5735, and MSP430FR5739 in the RHA package.

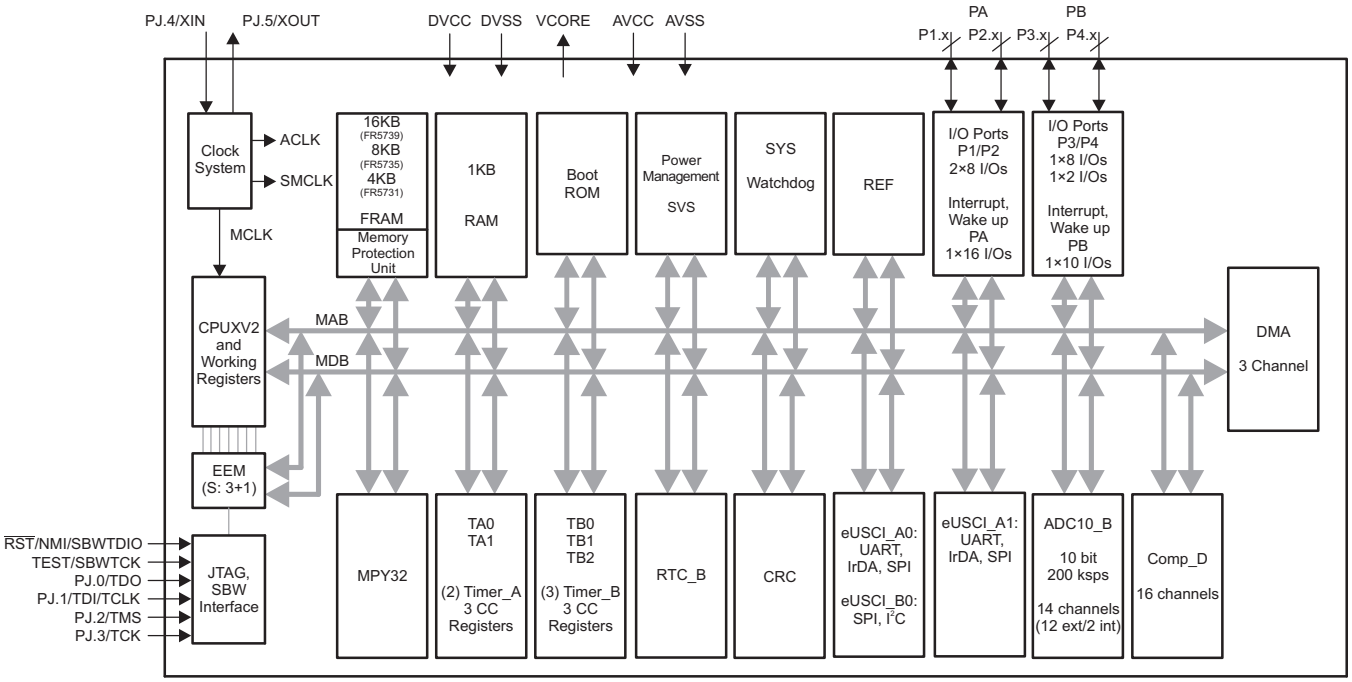

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图 6-1. Functional Block Diagram – RHA Package – MSP430FR5731, MSP430FR5735, MSP430FR5739

图 6-2 shows the functional block diagram for the MSP430FR5733 and MSP430FR5737 devices in the RHA package.

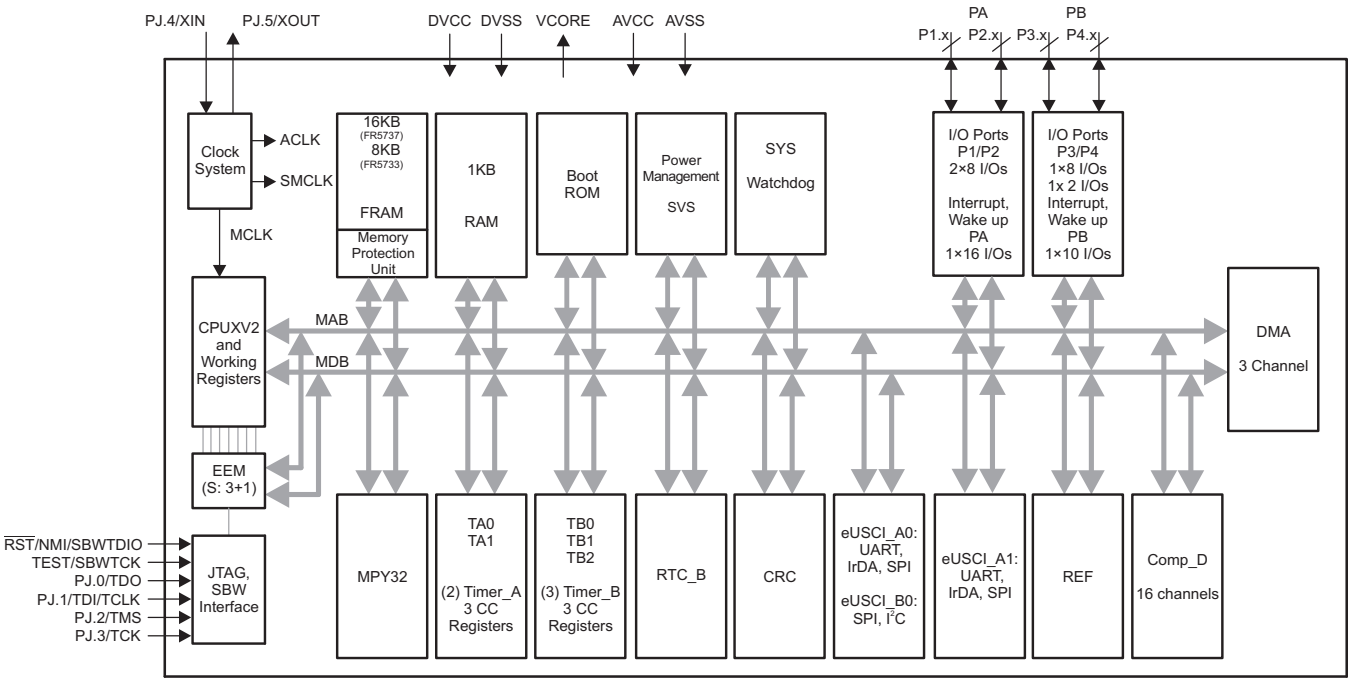

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图 6-2. Functional Block Diagram – RHA Package – MSP430FR5733, MSP430FR5737

图 6-3 shows the functional block diagram for the MSP430FR5731, MSP430FR5735, and MSP430FR5739 devices in the DA package.

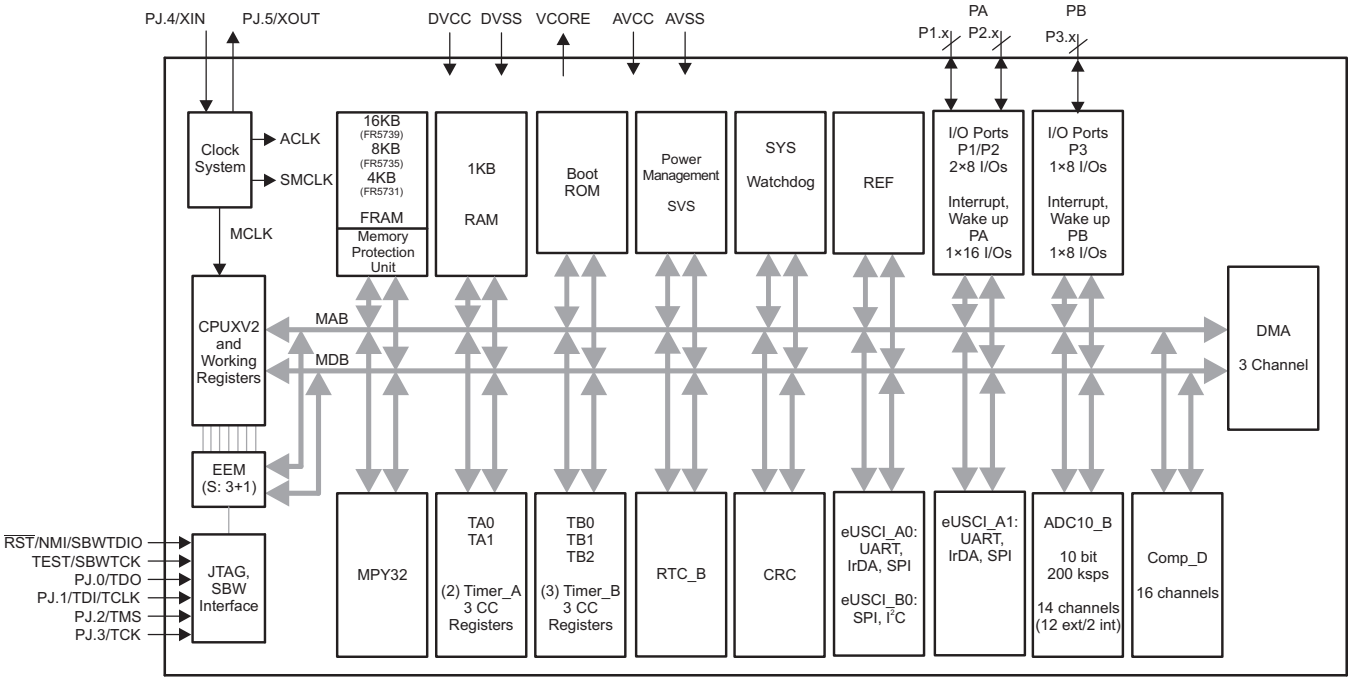

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图 6-3. Functional Block Diagram – DA Package – MSP430FR5731, MSP430FR5735, MSP430FR5739

图 6-4 shows the functional block diagram for the MSP430FR5733 and MSP430FR5737 devices in the DA package.

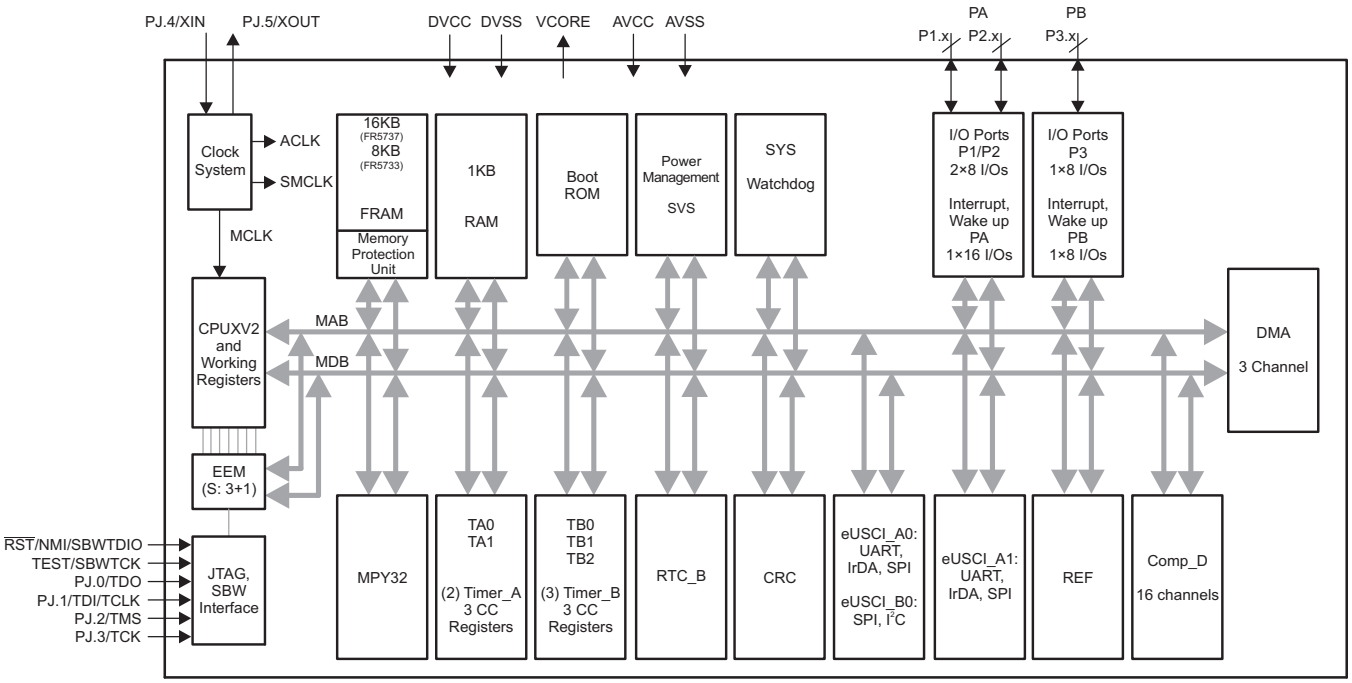

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图 6-4. Functional Block Diagram – DA Package – MSP430FR5733, MSP430FR5737

图 6-5 shows the functional block diagram for the MSP430FR5730, MSP430FR5734, and MSP430FR5738 devices in the RGE and YQD packages.

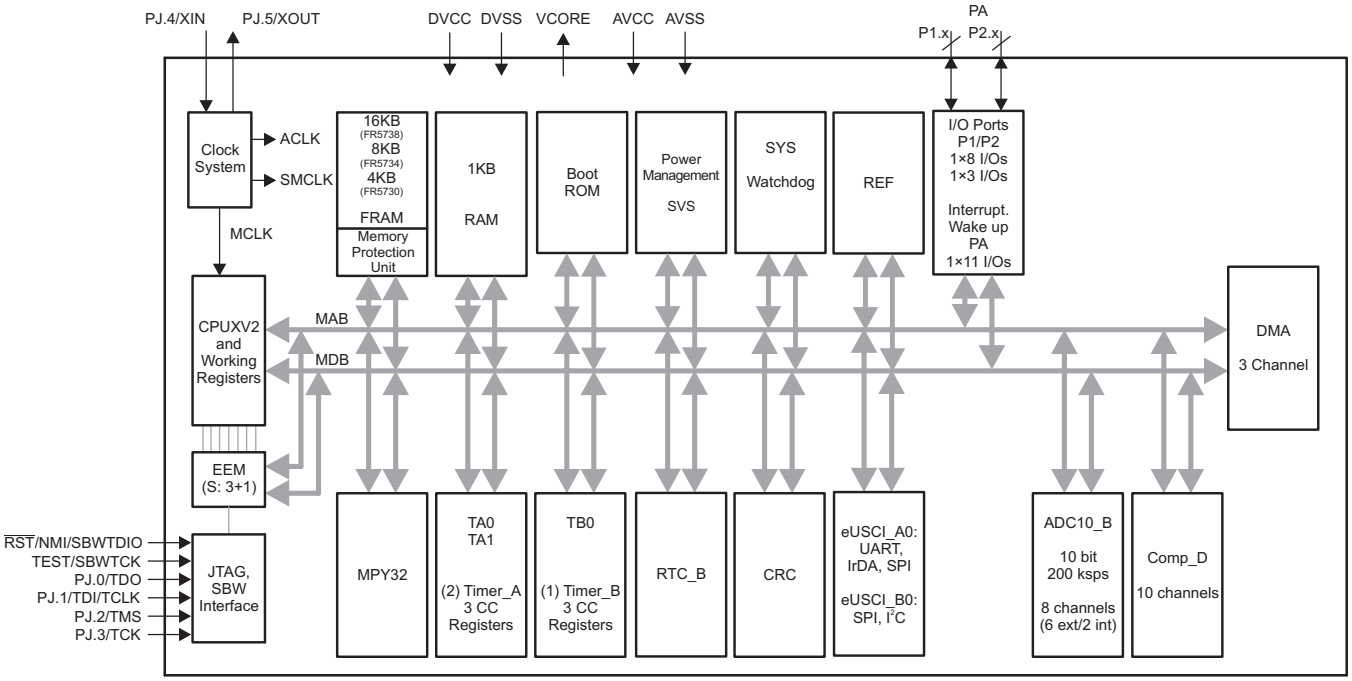

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图 6-5. Functional Block Diagram – RGE or YQD (FR5738 Only) Package – MSP430FR5730, MSP430FR5734, MSP430FR5738

图 6-6 shows the functional block diagram for the MSP430FR5732 and MSP430FR5736 devices in the RGE package.

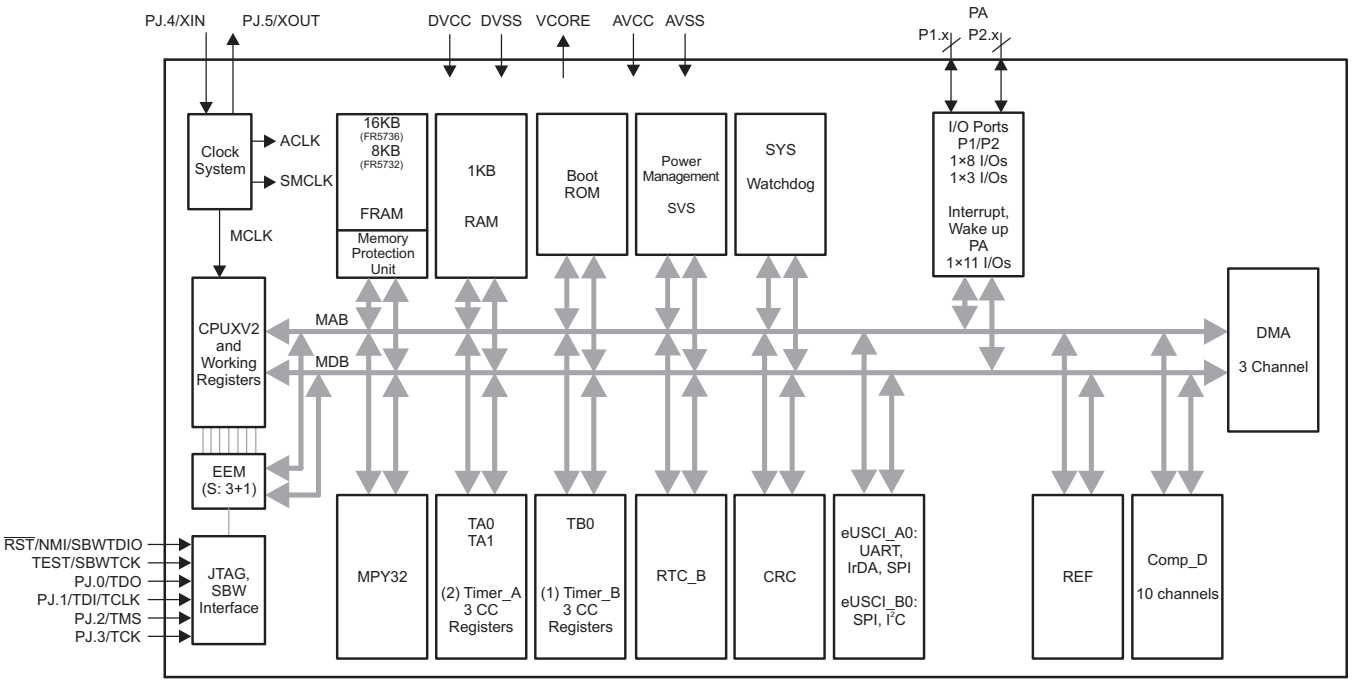

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图 6-6. Functional Block Diagram – RGE Package – MSP430FR5732, MSP430FR5736

图 6-7 shows the functional block diagram for the MSP430FR5730, MSP430FR5734, and MSP430FR5738 devices in the PW package.

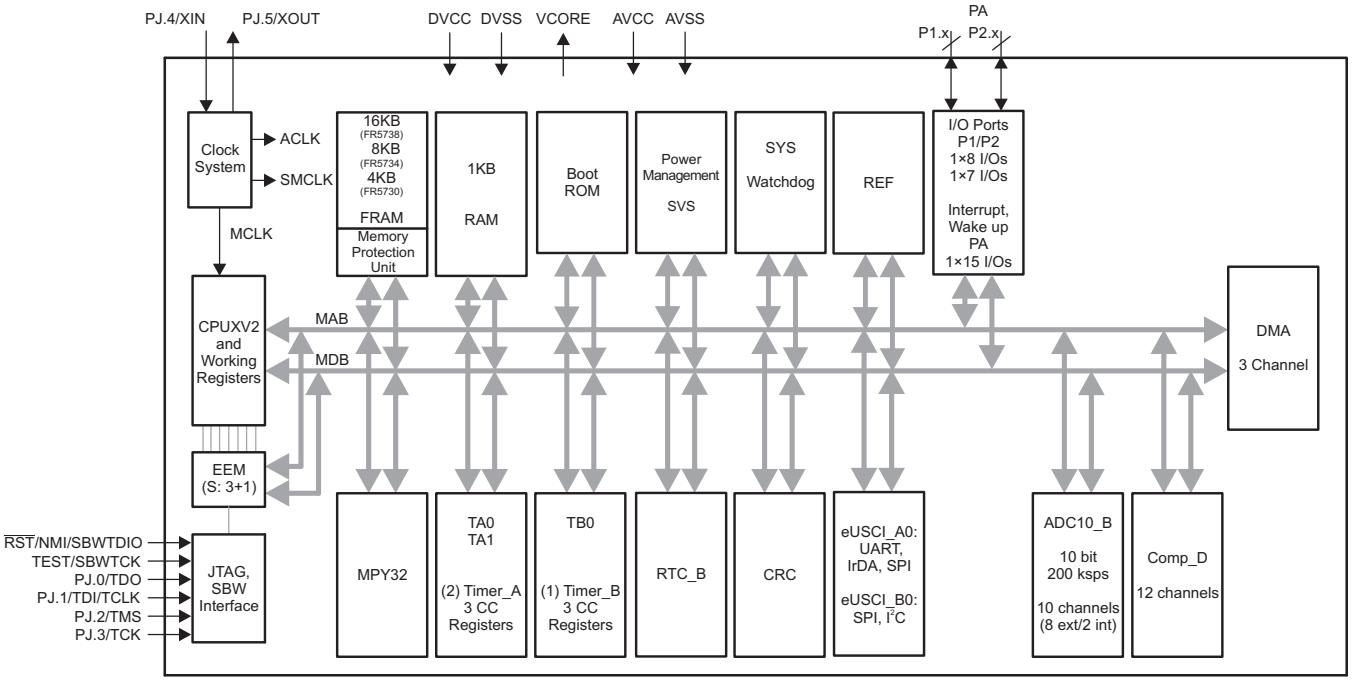

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图 6-7. Functional Block Diagram – PW Package – MSP430FR5730, MSP430FR5734, MSP430FR5738

图 6-8 shows the functional block diagram for the MSP430FR5732 and MSP430FR5736 devices in the PW package.

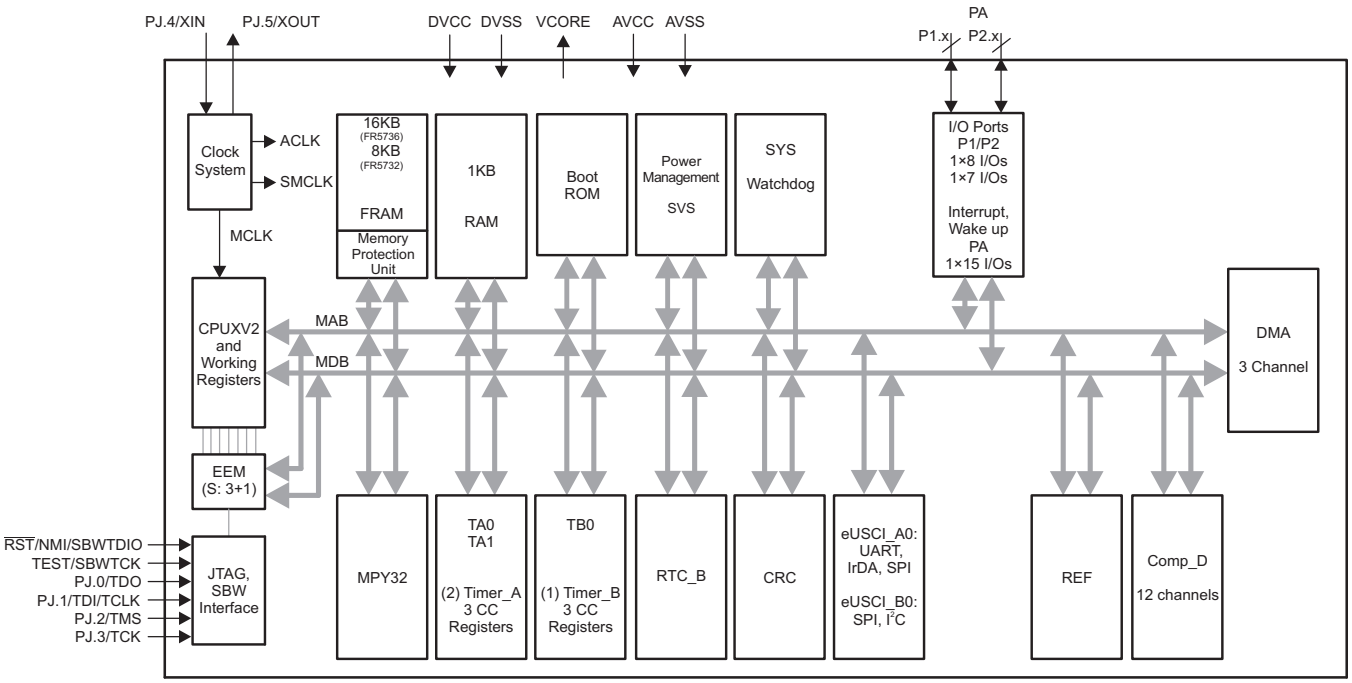

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图 6-8. Functional Block Diagram – PW Package – MSP430FR5732, MSP430FR5736

6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

6.3 Operating Modes

The MSP430 has one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from low-power modes LPM0 through LPM4, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

The following eight operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK active
  - MCLK disabled
  - SMCLK optionally active
  - Complete data retention
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK active
  - MCLK disabled
  - SMCLK optionally active
  - DCO disabled
  - Complete data retention
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - ACLK active
  - MCLK disabled
  - SMCLK optionally active
  - DCO disabled
  - Complete data retention
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - ACLK active
  - MCLK and SMCLK disabled
  - DCO disabled
  - Complete data retention
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK, MCLK, SMCLK disabled
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - RTC operation
  - Internal regulator disabled
  - No data retention
  - I/O pad state retention
  - Wake-up input from $\overline{\text{RST}}$, general-purpose I/O, RTC events
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - I/O pad state retention
  - Wake-up input from $\overline{\text{RST}}$ and general-purpose I/O

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6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see 表 6-1). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

表 6-1. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up, Brownout, Supply Supervisors External Reset $\overline{RST}$ Watchdog Time-out (Watchdog mode) WDT, FRCTL MPU, CS, PMM Password Violation FRAM double bit error detection MPU segment violation Software POR, BOR	SVSLIFG, SVSHIFG PMMRSTIFG WDTIFG WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW DBDIFG MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG PMMPORIFG, PMMBORIFG (SYSRSTIV) (1) (2)	Reset	0FFFEh	63, highest
System NMI Vacant Memory Access JTAG Mailbox FRAM access time error FRAM single, double bit error detection	VMAIFG JMBNIFG, JMBOUTIFG ACCTIMIFG SBDIFG, DBDIFG (SYSSNIV) (1)	(Non)maskable	0FFFCh	62
User NMI External NMI Oscillator Fault	NMIIFG, OFIFG (SYSUNIV) (1) (2)	(Non)maskable	0FFFAh	61
Comparator_D	Comparator_D interrupt flags (CBIV) (1) (3)	Maskable	0FFF8h	60
TB0	TB0CCR0 CCIFG0 (3)	Maskable	0FFF6h	59
TB0	TB0CCR1 CCIFG1 to TB0CCR2 CCIFG2, TB0IFG (TB0IV) (1) (3)	Maskable	0FFF4h	58
Watchdog Timer (Interval Timer Mode)	WDTIFG	Maskable	0FFF2h	57
eUSCI_A0 Receive and Transmit	UCA0RXIFG, UCA0TXIFG (SPI mode) UCA0STTIFG, UCA0TXCPTIFG, UCA0RXIFG, UXA0TXIFG (UART mode) (UCA0IV) (1) (3)	Maskable	0FFF0h	56
eUSCI_B0 Receive and Transmit	UCB0STTIFG, UCB0TXCPTIFG, UCB0RXIFG, UCB0TXIFG (SPI mode) UCB0ALIFG, UCB0NACKIFG, UCB0STTIFG, UCB0STPIFG, UCB0RXIFG0, UCB0TXIFG0, UCB0RXIFG1, UCB0TXIFG1, UCB0RXIFG2, UCB0TXIFG2, UCB0RXIFG3, UCB0TXIFG3, UCB0CNTIFG, UCB0BIT9IFG (I^2C mode) (UCB0IV) (1) (3)	Maskable	0FFEEh	55
ADC10_B	ADC10OVIFG, ADC10TOVIFG, ADC10HIIFG, ADC10LOIFG ADC10INIFG, ADC10IFG0 (ADC10IV) (1) (3) (4)	Maskable	0FFECh	54
TA0	TA0CCR0 CCIFG0 (3)	Maskable	0FFEAh	53
TA0	TA0CCR1 CCIFG1 to TA0CCR2 CCIFG2, TA0IFG (TA0IV) (1) (3)	Maskable	0FFE8h	52

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.
(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) Only on devices with ADC, otherwise reserved.

表 6-1. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
eUSCI_A1 Receive and Transmit	UCA1RXIFG, UCA1TXIFG (SPI mode) UCA1STTIFG, UCA1TXCPTIFG, UCA1RXIFG, UXA1TXIFG (UART mode) (UCA1IV) (1) (3)	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) (1) (3)	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0 (3)	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) (1) (3)	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV) (1) (3)	Maskable	0FFDEh	47
TB1	TB1CCR0 CCIFG0 (3)	Maskable	0FFDCh	46
TB1	TB1CCR1 CCIFG1 to TB1CCR2 CCIFG2, TB1IFG (TB1IV) (1) (3)	Maskable	0FFDAh	45
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV) (1) (3)	Maskable	0FFD8h	44
TB2	TB2CCR0 CCIFG0 (3)	Maskable	0FFD6h	43
TB2	TB2CCR1 CCIFG1 to TB2CCR2 CCIFG2, TB2IFG (TB2IV) (1) (3)	Maskable	0FFD4h	42
I/O Port P3	P3IFG.0 to P3IFG.7 (P3IV) (1) (3)	Maskable	0FFD2h	41
I/O Port P4	P4IFG.0 to P4IFG.2 (P4IV) (1) (3)	Maskable	0FFD0h	40
RTC_B	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) (1) (3)	Maskable	0FFCEh	39
Reserved	Reserved (5)		0FFCCh ⋮ 0FF80h	38 ⋮ 0, lowest

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

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6.5 Memory Organization

表 6-2 describes the memory organization for all device variants.

表 6-2. Memory Organization(1)(2)

		MSP430FR5736 MSP430FR5737 MSP430FR5738 MSP430FR5739	MSP430FR5732 MSP430FR5733 MSP430FR5734 MSP430FR5735	MSP430FR5730 MSP430FR5731
Memory (FRAM) Main: interrupt vectors Main: code memory	Total Size	15.5KB 00FFFFh–00FF80h 00FF7Fh–00C200h	8.0KB 00FFFFh–00FF80h 00FF7Fh–00E000h	4KB 00FFFFh–00FF80h 00FF7Fh–00F000h
RAM		1KB 001FFFh–001C00h	1KB 001FFFh–001C00h	1KB 001FFFh–001C00h
Device Descriptor Info (TLV) (FRAM)		128 B 001A7Fh–001A00h	128 B 001A7Fh–001A00h	128 B 001A7Fh–001A00h
Information memory (FRAM)	N/A	0019FFh–001980h Address space mirrored to Info A	0019FFh–001980h Address space mirrored to Info A	0019FFh–001980h Address space mirrored to Info A
	N/A	00197Fh–001900h Address space mirrored to Info B	00197Fh–001900h Address space mirrored to Info B	00197Fh–001900h Address space mirrored to Info B
	Info A	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h
	Info B	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h
Bootloader (BSL) memory (ROM)	BSL 3	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h
	BSL 2	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h
	BSL 1	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h
	BSL 0	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h
Peripherals	Size	4KB 000FFFh–0h	4KB 000FFFh–0h	4KB 000FFFh–0h

(1) N/A = Not available
(2) All address space not listed in this table is considered vacant memory.

6.6 Bootloader (BSL)

The BSL enables users to program the FRAM or RAM using a UART serial interface. Access to the device memory by the BSL is protected by an user-defined password. Use of the BSL requires four pins (see 表 6-3). BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming With the Bootloader User's Guide*.

表 6-3. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P2.0	Data transmit
P2.1	Data receive
VCC	Power supply
VSS	Ground supply

6.7 JTAG Operation

6.7.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. 表 6-4 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface*.

表 6-4. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

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6.7.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 6-5 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface*.

表 6-5. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input and output
VCC		Power supply
VSS		Ground supply

6.8 FRAM

The FRAM can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Low-power ultra-fast write nonvolatile memory
- Byte and word access capability
- Programmable and automated wait state generation
- Error correction coding (ECC) with single bit detection and correction, double bit detection

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the memory protection unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see *MSP430™ FRAM Technology – How To and Best Practices*.

6.9 Memory Protection Unit (MPU)

The FRAM can be protected from inadvertent CPU execution or write access by the MPU. Features of the MPU include:

- Main memory partitioning programmable up to three segments
- Access rights for each segment (main and information memory) can be individually selected
- Access violation flags with interrupt capability for easy servicing of access violations

6.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the *MSP430FR57xx Family User's Guide*.

6.10.1 Digital I/O

Up to four 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for all ports.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.

6.10.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch crystal oscillator XT1 (LF mode), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT1 (HF mode). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1 LF mode), a high-frequency crystal (XT1 HF mode), the internal VLO, or the internal DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by the same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by the same sources made available to ACLK.

6.10.3 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary and core supplies.

6.10.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

6.10.5 Real-Time Clock (RTC_B)

The RTC_B module contains an integrated real-time clock (RTC) (calendar mode). Calendar mode integrates an internal calendar which compensates for months with fewer than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 mode to minimize power consumption.

6.10.6 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.10.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators (see 表 6-6), bootloader entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism using JTAG called a JTAG mailbox that can be used in the application.

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表 6-6. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wake up (BOR)	08h	
		Security violation (BOR)	0Ah	
		SVSLIFG SVSL event (BOR)	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		DBDIFG FRAM double bit error (PUC)	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		MPUPW MPU password violation (PUC)	22h	
		CSPW CS password violation (PUC)	24h	
		MPUSEGIIFG information memory segment violation (PUC)	26h	
		MPUSEG1IFG segment 1 memory violation (PUC)	28h	
		MPUSEG2IFG segment 2 memory violation (PUC)	2Ah	
		MPUSEG3IFG segment 3 memory violation (PUC)	2Ch	
		Reserved	2Eh	
		Reserved	30h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		DBDIFG FRAM double bit error	02h	Highest
		ACCTIMIFG access time error	04h	
		Reserved	0Eh	
		VMAIFG Vacant memory access	10h	
		JMBINIFG JTAG mailbox input	12h	
		JMBOUTIFG JTAG mailbox output	14h	
		SBDIFG FRAM single bit error	16h	
		Reserved	18h to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIIFG NMI pin	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

6.10.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. 表 6-7 lists all triggers to start DMA transfers.

表 6-7. DMA Trigger Assignments (1)

TRIGGER	CHANNEL 0	CHANNEL 1	CHANNEL 2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	Reserved	Reserved	Reserved
6	Reserved	Reserved	Reserved
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	TB1CCR0 CCIFG (2)	TB1CCR0 CCIFG (2)	TB1CCR0 CCIFG (2)
10	TB1CCR2 CCIFG (2)	TB1CCR2 CCIFG (2)	TB1CCR2 CCIFG (2)
11	TB2CCR0 CCIFG (3)	TB2CCR0 CCIFG (3)	TB2CCR0 CCIFG (3)
12	TB2CCR2 CCIFG (3)	TB2CCR2 CCIFG (3)	TB2CCR2 CCIFG (3)
13	Reserved	Reserved	Reserved
14	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
15	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
16	UCA1RXIFG (4)	UCA1RXIFG (4)	UCA1RXIFG (4)
17	UCA1TXIFG (4)	UCA1TXIFG (4)	UCA1TXIFG (4)
18	UCB0RXIFG0	UCB0RXIFG0	UCB0RXIFG0
19	UCB0TXIFG0	UCB0TXIFG0	UCB0TXIFG0
20	UCB0RXIFG1	UCB0RXIFG1	UCB0RXIFG1
21	UCB0TXIFG1	UCB0TXIFG1	UCB0TXIFG1
22	UCB0RXIFG2	UCB0RXIFG2	UCB0RXIFG2
23	UCB0TXIFG2	UCB0TXIFG2	UCB0TXIFG2
24	UCB0RXIFG3	UCB0RXIFG3	UCB0RXIFG3
25	UCB0TXIFG3	UCB0TXIFG3	UCB0TXIFG3
26	ADC10IFGx (5)	ADC10IFGx (5)	ADC10IFGx (5)
27	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0 (6)	DMAE0 (6)	DMAE0 (6)

(1) If a reserved trigger source is selected, no trigger is generated.
(2) Only on devices with TB1, otherwise reserved
(3) Only on devices with TB2, otherwise reserved
(4) Only on devices with eUSCI_A1, otherwise reserved
(5) Only on devices with ADC, otherwise reserved
(6) This function is not available on YQD package types.

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6.10.9 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each eUSCI module contains two portions, A and B.

The eUSCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, or IrDA.

The eUSCI_Bn module provides support for SPI (3-pin or 4-pin) or I^2C.

The MSP430FR573x series include one or two eUSCI_An modules (eUSCI_A0, eUSCI_A1) and one eUSCI_Bn module (eUSCI_B).

6.10.10 TA0, TA1

TA0 and TA1 are 16-bit timers/counters (Timer_A type) with three capture/compare registers each. TA0 and TA1 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-8 and 表 6-9). TA0 and TA1 have extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-8. TA0 Signal Connections

INPUT PIN NUMBER				DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER			
RHA	RGE, YQD	DA	PW						RHA	RGE, YQD	DA	PW
3-P1.2	3-P1.2, C1-P1.2	7-P1.2	7-P1.2	TA0CLK	TACLK	Timer	N/A	N/A				
				ACLK (internal)	ACLK							
				SMCLK (internal)	SMCLK							
3-P1.2	3-P1.2, C1-P1.2	7-P1.2	7-P1.2	TA0CLK	$\overline{\text{TACLK}}$							
28-P1.6	16-P1.6, D5-P1.6	30-P1.6	22-P1.6	TA0.0	CCI0A	CCR0	TA0	TA0.0	28-P1.6	16-P1.6, D5-P1.6	30-P1.6	22-P1.6
34-P2.3	N/A	36-P2.3	27-P2.3	TA0.0	CCI0B				34-P2.3	N/A	36-P2.3	27-P2.3
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							
1-P1.0	1-P1.0, N/A	5-P1.0	5-P1.0	TA0.1	CCI1A	CCR1	TA1	TA0.1	1-P1.0	1-P1.0, N/A	5-P1.0	5-P1.0
				CDOUT (internal)	CCI1B				ADC10 (internal) (1) ADC10SHSx = {1}	ADC10 (internal) (1) ADC10SHSx = {1}	ADC10 (internal) (1) ADC10SHSx = {1}	ADC10 (internal) (1) ADC10SHSx = {1}
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							
2-P1.1	2-P1.1, D1-P1.1	6-P1.1	6-P1.1	TA0.2	CCI2A	CCR2	TA2	TA0.2	2-P1.1	2-P1.1, D1-P1.1	6-P1.1	6-P1.1
				ACLK (internal)	CCI2B							
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							

(1) Only on devices with ADC

表 6-9. TA1 Signal Connections

INPUT PIN NUMBER				DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER			
RHA	RGE, YQD	DA	PW						RHA	RGE, YQD	DA	PW
2-P1.1	2-P1.1, D1-P1.1	6-P1.1	6-P1.1	TA1CLK	TACLK	Timer	N/A	N/A				
				ACLK (internal)	ACLK							
				SMCLK (internal)	SMCLK							
2-P1.1	2-P1.1, D1-P1.1	6-P1.1	6-P1.1	TA1CLK	$\overline{\text{TACLK}}$							
29-P1.7	17-P1.7, C5-P1.7	31-P1.7	23-P1.7	TA1.0	CCI0A	CCR0	TA0	TA1.0	29-P1.7	17-P1.7, C5-P1.7	31-P1.7	23-P1.7
35-P2.4	N/A	37-P2.4	28-P2.4	TA1.0	CCI0B				35-P2.4	N/A	37-P2.4	28-P2.4
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							
3-P1.2	3-P1.2, N/A	7-P1.2	7-P1.2	TA1.1	CCI1A	CCR1	TA1	TA1.1	3-P1.2	3-P1.2, N/A	7-P1.2	7-P1.2
				CDOUT (internal)	CCI1B							
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							
8-P1.3	4-P1.3, B1-P1.3	12-P1.3	8-P1.3	TA1.2	CCI2A	CCR2	TA2	TA1.2	8-P1.3	4-P1.3, B1-P1.3	12-P1.3	8-P1.3
				ACLK (internal)	CCI2B							
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							

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6.10.11 TB0, TB1, TB2

TB0, TB1, and TB2 are 16-bit timers/counters (Timer_B type) with three capture/compare registers each. TB0, TB1, and TB2 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-10 through 表 6-12). TB0, TB1, and TB2 have extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-10. TB0 Signal Connections

INPUT PIN NUMBER				DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER			
RHA	RGE, YQD	DA	PW						RHA	RGE, YQD	DA	PW
21-P2.0	13-P2.0, A5-P2.0	23-P2.0	19-P2.0	TB0CLK	TBCLK	Timer	N/A	N/A				
				ACLK (internal)	ACLK							
				SMCLK (internal)	SMCLK							
21-P2.0	13-P2.0, A5-P2.0	23-P2.0	19-P2.0	TB0CLK	$\overline{\text{TBCLK}}$							
22-P2.1	14-P2.1, C4-P2.1	24-P2.1	20-P2.1	TB0.0	CCI0A	CCR0	TB0	TB0.0	22-P2.1	14-P2.1, C4-P2.1	24-P2.1	20-P2.1
17-P2.5	N/A	19-P2.5	15-P2.5	TB0.0	CCI0B				17-P2.5	N/A	19-P2.5	15-P2.5
				DV_{SS}	GND				ADC10 (internal) (1) ADC10SHSx = {2}	ADC10 (internal) (1) ADC10SHSx = {2}	ADC10 (internal) (1) ADC10SHSx = {2}	ADC10 (internal) (1) ADC10SHSx = {2}
				DV_{CC}	V_{CC}							
9-P1.4	5-P1.4, B2-P1.4	13-P1.4	9-P1.4	TB0.1	CCI1A	CCR1	TB1	TB0.1	9-P1.4	5-P1.4, B2-P1.4	13-P1.4	9-P1.4
				CDOUT (internal)	CCI1B				ADC10 (internal) (1) ADC10SHSx = {3}	ADC10 (internal) (1) ADC10SHSx = {3}	ADC10 (internal) (1) ADC10SHSx = {3}	ADC10 (internal) (1) ADC10SHSx = {3}
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							
10-P1.5	6-P1.5, A1-P1.5	14-P1.5	19-P1.5	TB0.2	CCI2A	CCR2	TB2	TB0.2	10-P1.5	6-P1.5, A1-P1.5	14-P1.5	19-P1.5
				ACLK (internal)	CCI2B							
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							

(1) Only on devices with ADC

表 6-11. TB1 Signal Connections (1)

INPUT PIN NUMBER				DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER			
RHA	RGE, YQD	DA	PW						RHA	RGE, YQD	DA	PW
26-P3.6	N/A (DV_{SS}), N/A (DV_{SS})	28-P3.6	N/A (DV_{SS})	TB1CLK	TBCLK	Timer	N/A	N/A				
				ACLK (internal)	ACLK							
				SMCLK (internal)	SMCLK							
26-P3.6	N/A (DV_{SS}), N/A (DV_{SS})	28-P3.6	N/A (DV_{SS})	TB1CLK	$\overline{TBCLK}$							
23-P2.2	N/A (DV_{SS}), N/A (DV_{SS})	25-P2.2	N/A (DV_{SS})	TB1.0	CCI0A	CCR0	TB0	TB1.0	23-P2.2	N/A	25-P2.2	N/A
18-P2.6	N/A (DV_{SS}), N/A (DV_{SS})	20-P2.6	N/A (DV_{SS})	TB1.0	CCI0B				18-P2.6	N/A	20-P2.6	N/A
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							
28-P1.6	N/A (DV_{SS}), N/A (DV_{SS})	30-P1.6	N/A (DV_{SS})	TB1.1	CCI1A	CCR1	TB1	TB1.1	28-P1.6	N/A	30-P1.6	N/A
24-P3.4	N/A (DV_{SS}), N/A (DV_{SS})	26-P3.4	N/A (DV_{SS})	TB1.1	CCI1B				24-P3.4	N/A	26-P3.4	N/A
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							
29-P1.7	N/A (DV_{SS}), N/A (DV_{SS})	31-P1.7	N/A (DV_{SS})	TB1.2	CCI2A	CCR2	TB2	TB1.2	29-P1.7	N/A	31-P1.7	N/A
25-P3.5	N/A (DV_{SS}), N/A (DV_{SS})	27-P3.5	N/A (DV_{SS})	TB1.2	CCI2B				25-P3.5	N/A	27-P3.5	N/A
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							

(1) TB1 is not present on all device types.

表 6-12. TB2 Signal Connections (1)

INPUT PIN NUMBER				DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER			
RHA	RGE, YQD	DA	PW						RHA	RGE, YQD	DA	PW
24-P3.4	N/A (DV_{SS}), N/A (DV_{SS})	26-P3.4	N/A (DV_{SS})	TB2CLK	TBCLK	Timer	N/A	N/A				
				ACLK (internal)	ACLK							
				SMCLK (internal)	SMCLK							
24-P3.4	N/A (DV_{SS}), N/A (DV_{SS})	26-P3.4	N/A (DV_{SS})	TB2CLK	$\overline{TBCLK}$							
21-P2.0	N/A (DV_{SS}), N/A (DV_{SS})	23-P2.0	N/A (DV_{SS})	TB2.0	CCI0A	CCR0	TB0	TB2.0	21-P2.0	N/A	23-P2.0	N/A
15-P4.0	N/A (DV_{SS}), N/A (DV_{SS})	N/A (DV_{SS})	N/A (DV_{SS})	TB2.0	CCI0B				15-P4.0	N/A	36-P4.0	N/A
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							
22-P2.1	N/A (DV_{SS}), N/A (DV_{SS})	24-P2.1	N/A (DV_{SS})	TB2.1	CCI1A	CCR1	TB1	TB2.1	22-P2.1	N/A	24-P2.1	N/A
26-P3.6	N/A (DV_{SS}), N/A (DV_{SS})	28-P3.6	N/A (DV_{SS})	TB2.1	CCI1B				26-P3.6	N/A	28-P3.6	N/A
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							
23-P2.2	N/A (DV_{SS}), N/A (DV_{SS})	25-P2.2	N/A (DV_{SS})	TB2.2	CCI2A	CCR2	TB2	TB2.2	23-P2.2	N/A	25-P2.2	N/A
27-P3.7	N/A (DV_{SS}), N/A (DV_{SS})	29-P3.7	N/A (DV_{SS})	TB2.2	CCI2B				27-P3.7	N/A	29-P3.7	N/A
				DV_{SS}	GND							
				DV_{CC}	V_{CC}							

(1) TB2 is not present on all device types.

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6.10.12 ADC10_B

The ADC10_B module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and an upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

6.10.13 Comparator_D

The primary function of the Comparator_D module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.10.14 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.10.15 Shared Reference (REF)

The REF module generates all of the critical reference voltages that can be used by the various analog peripherals in the device.

6.10.16 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.10.17 Peripheral File Map

表 6-13 lists the base address and offset range of all available peripherals.

表 6-13. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see 表 6-14)	0100h	000h–01Fh
PMM (see 表 6-15)	0120h	000h–010h
FRAM Control (see 表 6-16)	0140h	000h–00Fh
CRC16 (see 表 6-17)	0150h	000h–007h
Watchdog (see 表 6-18)	015Ch	000h–001h
CS (see 表 6-19)	0160h	000h–00Fh
SYS (see 表 6-20)	0180h	000h–01Fh
Shared Reference (see 表 6-21)	01B0h	000h–001h
Port P1, P2 (see 表 6-22)	0200h	000h–01Fh
Port P3, P4 (see 表 6-23)	0220h	000h–01Fh
Port PJ (see 表 6-24)	0320h	000h–01Fh
TA0 (see 表 6-25)	0340h	000h–02Fh
TA1 (see 表 6-26)	0380h	000h–02Fh
TB0 (see 表 6-27)	03C0h	000h–02Fh
TB1 (see 表 6-28)	0400h	000h–02Fh
TB2 (see 表 6-29)	0440h	000h–02Fh
Real-Time Clock (RTC_B) (see 表 6-30)	04A0h	000h–01Fh
32-Bit Hardware Multiplier (see 表 6-31)	04C0h	000h–02Fh
DMA General Control (see 表 6-32)	0500h	000h–00Fh
DMA Channel 0 (see 表 6-32)	0510h	000h–00Ah
DMA Channel 1 (see 表 6-32)	0520h	000h–00Ah
DMA Channel 2 (see 表 6-32)	0530h	000h–00Ah
MPU Control (see 表 6-33)	05A0h	000h–00Fh
eUSCI_A0 (see 表 6-34)	05C0h	000h–01Fh
eUSCI_A1 (see 表 6-35)	05E0h	000h–01Fh
eUSCI_B0 (see 表 6-36)	0640h	000h–02Fh
ADC10_B (see 表 6-37)	0700h	000h–03Fh
Comparator_D (see 表 6-38)	08C0h	000h–00Fh

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表 6-14. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

表 6-15. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM interrupt flags	PMMIFG	0Ah
PM5 control 0	PM5CTL0	10h

表 6-16. FRAM Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
FRAM control 0	FRCTLCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

表 6-17. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

表 6-18. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

表 6-19. CS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CS control 0	CSCTL0	00h
CS control 1	CSCTL1	02h
CS control 2	CSCTL2	04h
CS control 3	CSCTL3	06h
CS control 4	CSCTL4	08h
CS control 5	CSCTL5	0Ah
CS control 6	CSCTL6	0Ch

表 6-20. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

表 6-21. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

表 6-22. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 selection 0	P1SEL0	0Ah
Port P1 selection 1	P1SEL1	0Ch
Port P1 interrupt vector word	P1IV	0Eh
Port P1 complement selection	P1SELC	16h
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h
Port P2 selection 0	P2SEL0	0Bh
Port P2 selection 1	P2SEL1	0Dh
Port P2 complement selection	P2SELC	17h
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

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表 6-23. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 selection 0	P3SEL0	0Ah
Port P3 selection 1	P3SEL1	0Ch
Port P3 interrupt vector word	P3IV	0Eh
Port P3 complement selection	P3SELC	16h
Port P3 interrupt edge select	P3IES	18h
Port P3 interrupt enable	P3IE	1Ah
Port P3 interrupt flag	P3IFG	1Ch
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 selection 0	P4SEL0	0Bh
Port P4 selection 1	P4SEL1	0Dh
Port P4 complement selection	P4SELC	17h
Port P4 interrupt vector word	P4IV	1Eh
Port P4 interrupt edge select	P4IES	19h
Port P4 interrupt enable	P4IE	1Bh
Port P4 interrupt flag	P4IFG	1Dh

表 6-24. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ selection 0	PJSEL0	0Ah
Port PJ selection 1	PJSEL1	0Ch
Port PJ complement selection	PJSELC	16h

表 6-25. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

表 6-26. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

表 6-27. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

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表 6-28. TB1 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB1 control	TB1CTL	00h
Capture/compare control 0	TB1CCTL0	02h
Capture/compare control 1	TB1CCTL1	04h
Capture/compare control 2	TB1CCTL2	06h
TB1 counter	TB1R	10h
Capture/compare 0	TB1CCR0	12h
Capture/compare 1	TB1CCR1	14h
Capture/compare 2	TB1CCR2	16h
TB1 expansion 0	TB1EX0	20h
TB1 interrupt vector	TB1IV	2Eh

表 6-29. TB2 Registers (Base Address: 0440h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB2 control	TB2CTL	00h
Capture/compare control 0	TB2CCTL0	02h
Capture/compare control 1	TB2CCTL1	04h
Capture/compare control 2	TB2CCTL2	06h
TB2 counter	TB2R	10h
Capture/compare 0	TB2CCR0	12h
Capture/compare 1	TB2CCR1	14h
Capture/compare 2	TB2CCR2	16h
TB2 expansion 0	TB2EX0	20h
TB2 interrupt vector	TB2IV	2Eh

表 6-30. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds, RTC counter 1	RTCSEC, RTCNT1	10h
RTC minutes, RTC counter 2	RTCMIN, RTCNT2	11h
RTC hours, RTC counter 3	RTCHOUR, RTCNT3	12h
RTC day of week, RTC counter 4	RTCDOW, RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh
Binary-to-BCD conversion register	BIN2BCD	1Ch
BCD-to-binary conversion register	BCD2BIN	1Eh

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表 6-31. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch

表 6-32. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Ah

表 6-33. MPU Control Registers (Base Address: 05A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
MPU control 0	MPUCTL0	00h
MPU control 1	MPUCTL1	02h
MPU segmentation	MPUSEG	04h
MPU access management	MPUSAM	06h

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表 6-34. eUSCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI _A control word 1	UCA0CTLW1	02h
eUSCI_A baud rate 0	UCA0BR0	06h
eUSCI_A baud rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status	UCA0STAT	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	UCA0IRTCTL	12h
eUSCI_A IrDA receive control	UCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

表 6-35. eUSCI_A1 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA1CTLW0	00h
eUSCI _A control word 1	UCA1CTLW1	02h
eUSCI_A baud rate 0	UCA1BR0	06h
eUSCI_A baud rate 1	UCA1BR1	07h
eUSCI_A modulation control	UCA1MCTLW	08h
eUSCI_A status	UCA1STAT	0Ah
eUSCI_A receive buffer	UCA1RXBUF	0Ch
eUSCI_A transmit buffer	UCA1TXBUF	0Eh
eUSCI_A LIN control	UCA1ABCTL	10h
eUSCI_A IrDA transmit control	UCA1IRTCTL	12h
eUSCI_A IrDA receive control	UCA1IRRCTL	13h
eUSCI_A interrupt enable	UCA1IE	1Ah
eUSCI_A interrupt flags	UCA1IFG	1Ch
eUSCI_A interrupt vector word	UCA1IV	1Eh

表 6-36. eUSCI_B0 Registers (Base Address: 0640h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0TBCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh
eUSCI_B I2C own address 0	UCB0I2COA0	14h
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B received address	UCB0ADDRX	1Ch
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI I2C slave address	UCB0I2CSA	20h
eUSCI interrupt enable	UCB0IE	2Ah
eUSCI interrupt flags	UCB0IFG	2Ch
eUSCI interrupt vector word	UCB0IV	2Eh

表 6-37. ADC10_B Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC10_B control 0	ADC10CTL0	00h
ADC10_B control 1	ADC10CTL1	02h
ADC10_B control 2	ADC10CTL2	04h
ADC10_B window comparator low threshold	ADC10LO	06h
ADC10_B window comparator high threshold	ADC10HI	08h
ADC10_B memory control 0	ADC10MCTL0	0Ah
ADC10_B conversion memory	ADC10MEM0	12h
ADC10_B Interrupt enable	ADC10IE	1Ah
ADC10_B interrupt flags	ADC10IGH	1Ch
ADC10_B interrupt vector word	ADC10IV	1Eh

表 6-38. Comparator_D Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comparator_D control 0	CDCTL0	00h
Comparator_D control 1	CDCTL1	02h
Comparator_D control 2	CDCTL2	04h
Comparator_D control 3	CDCTL3	06h
Comparator_D interrupt	CDINT	0Ch
Comparator_D interrupt vector word	CDIV	0Eh

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6.11 Input/Output Diagrams

6.11.1 Port P1 (P1.0 to P1.2) Input/Output With Schmitt Trigger

图 6-9 shows the port diagram. 表 6-39 summarizes the selection of the pin functions.

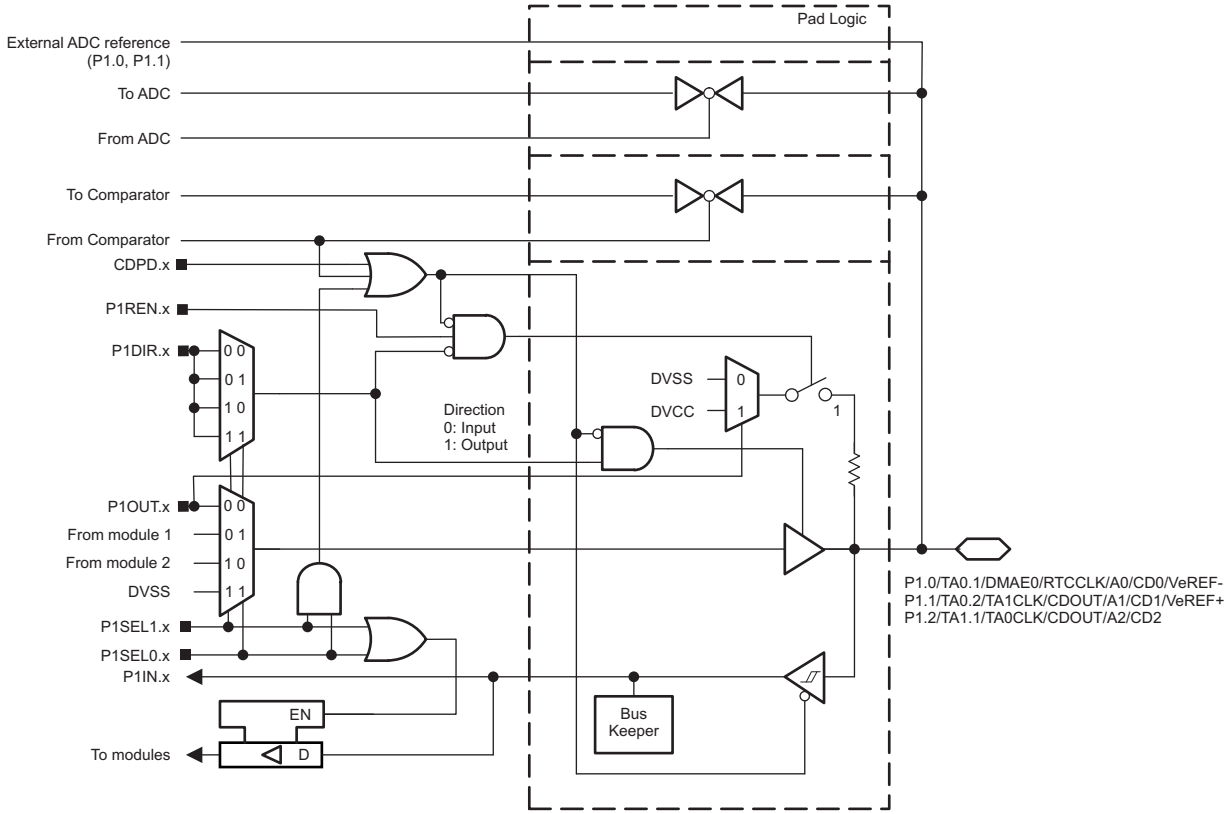

图 6-9. Port P1 (P1.0 to P1.2) Diagram

表 6-39. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/TA0.1/DMAE0/RTCCLK/A0/CD0/VeREF-	0	P1.0 (I/O)	I: 0; O: 1	0	0
		TA0.CCI1A	0	0	1
		TA0.1	1		
		DMAE0	0	1	0
		RTCCLK	1		
		A0 (1) (2) CD0 (1) (3) VeREF- (1) (2)	X	1	1
P1.1/TA0.2/TA1CLK/CDOUT/A1/CD1/VeREF+	1	P1.1 (I/O)	I: 0; O: 1	0	0
		TA0.CCI2A	0	0	1
		TA0.2	1		
		TA1CLK	0	1	0
		CDOUT	1		
		A1 (1) (2) CD1 (1) (3) VeREF+ (1) (2)	X	1	1
P1.2/TA1.1/TA0CLK/CDOUT/A2/CD2	2	P1.2 (I/O)	I: 0; O: 1	0	0
		TA1.CCI1A	0	0	1
		TA1.1	1		
		TA0CLK	0	1	0
		CDOUT	1		
		A2 (1) (2) CD2 (1) (3)	X	1	1

(1) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(2) Not available on all devices and package types.
(3) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.

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6.11.2 Port P1 (P1.3 to P1.5) Input/Output With Schmitt Trigger

图 6-10 shows the port diagram. 表 6-40 summarizes the selection of the pin functions.

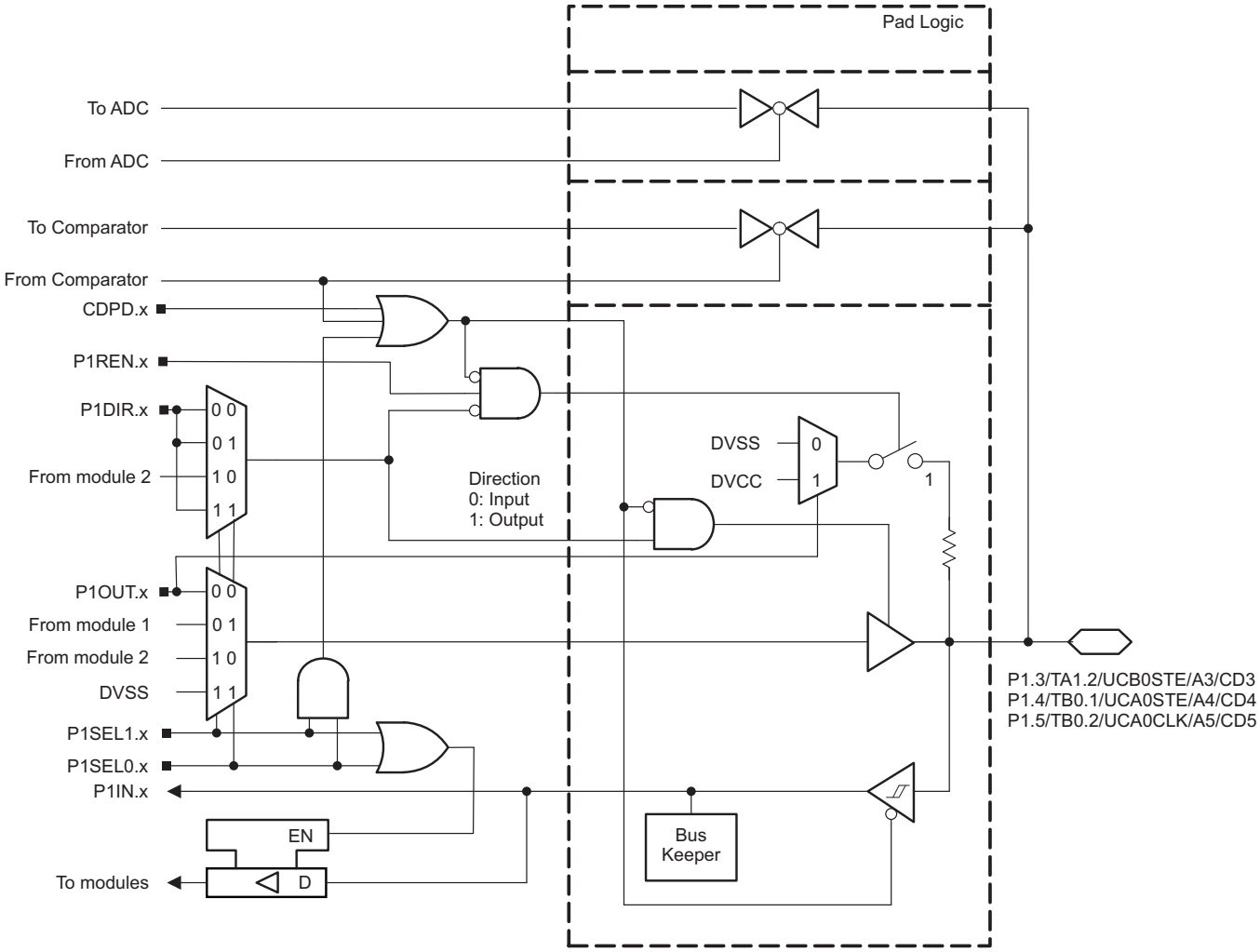

图 6-10. Port P1 (P1.3 to P1.5) Diagram

表 6-40. Port P1 (P1.3 to P1.5) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.3/TA1.2/UCB0STE/A3/CD3	3	P1.3 (I/O)	I: 0; O: 1	0	0
		TA1.CCI2A	0	0	1
		TA1.2	1		
		UCB0STE	X (1)	1	0
		A3 (2) (3) CD3 (2) (4)	X	1	1
P1.4/TB0.1/UCA0STE/A4/CD4	4	P1.4 (I/O)	I: 0; O: 1	0	0
		TB0.CCI1A	0	0	1
		TB0.1	1		
		UCA0STE	X (5)	1	0
		A4 (2) (3) CD4 (2) (4)	X	1	1
P1.5/TB0.2/UCA0CLK/A5/CD5	5	P1.5(I/O)	I: 0; O: 1	0	0
		TB0.CCI2A	0	0	1
		TB0.2	1		
		UCA0CLK	X (5)	1	0
		A5 (2) (3) CD5 (2) (4)	X	1	1

(1) Direction controlled by eUSCI_B0 module.
(2) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Not available on all devices and package types.
(4) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit
(5) Direction controlled by eUSCI_A0 module.

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6.11.3 Port P1 (P1.6 and P1.7) Input/Output With Schmitt Trigger

图 6-11 shows the port diagram. 表 6-41 summarizes the selection of the pin functions.

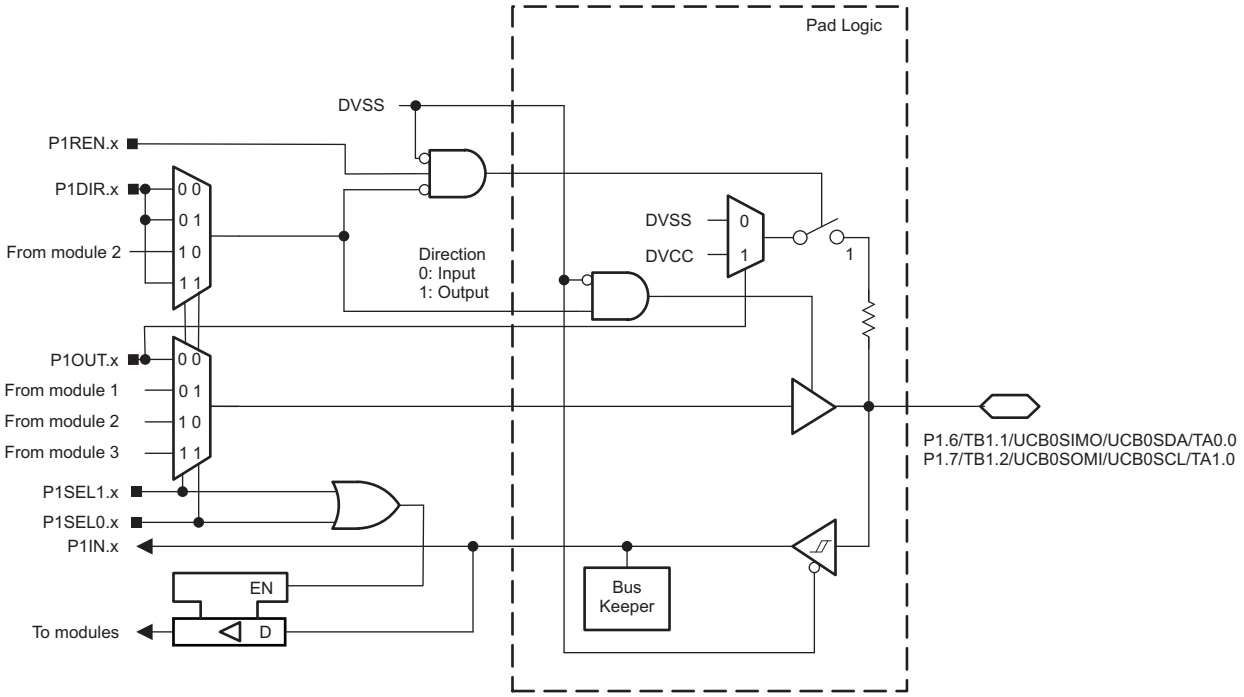

图 6-11. Port P1 (P1.6 and P1.7) Diagram

表 6-41. Port P1 (P1.6 and P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.6/TB1.1/UCB0SIMO/UCB0SDA/TA0.0	6	P1.6 (I/O)	I: 0; O: 1	0	0
		TB1.CCI1A (1)	0	0	1
		TB1.1 (1)	1		
		UCB0SIMO/UCB0SDA	X (2)	1	0
		TA0.CCI0A	0	1	1
		TA0.0	1		
P1.7/TB1.2/UCB0SOMI/UCB0SCL/TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0	0
		TB1.CCI2A (1)	0	0	1
		TB1.2 (1)	1		
		UCB0SOMI/UCB0SCL	X(2)	1	0
		TA1.CCI0A	0	1	1
		TA1.0	1		

(1) Not available on all devices and package types.
(2) Direction controlled by eUSCI_B0 module.

6.11.4 Port P2 (P2.0 to P2.2) Input/Output With Schmitt Trigger

图 6-12 shows the port diagram. 表 6-42 summarizes the selection of the pin functions.

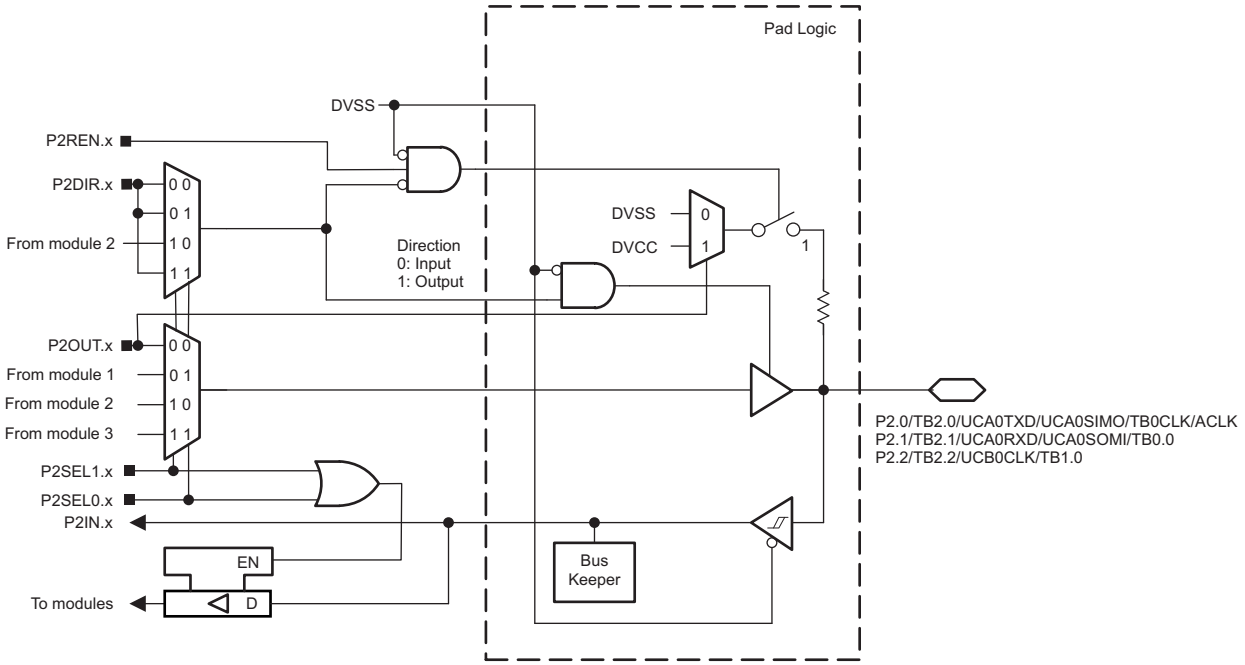

图 6-12. Port P2 (P2.0 to P2.2) Diagram

表 6-42. Port P2 (P2.0 to P2.2) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.0/TB2.0/UCA0TXD/UCA0SIMO/TB0CLK/ACLK	0	P2.0 (I/O)	I: 0; O: 1	0	0
		TB2.CCI0A (1)	0	0	1
		TB2.0 (1)	1		
		UCA0TXD/UCA0SIMO	X (2)	1	0
		TB0CLK	0	1	1
		ACLK	1		
P2.1/TB2.1/UCA0RXD/UCA0SOMI/TB0.0	1	P2.1 (I/O)	I: 0; O: 1	0	0
		TB2.CCI1A (1)	0	0	1
		TB2.1 (1)	1		
		UCA0RXD/UCA0SOMI	X (2)	1	0
		TB0.CCI0A	0	1	1
		TB0.0	1		
P2.2/TB2.2/UCB0CLK/TB1.0	2	P2.2 (I/O)	I: 0; O: 1	0	0
		TB2.CCI2A (1)	0	0	1
		TB2.2 (1)	1		
		UCB0CLK	X (3)	1	0
		TB1.CCI0A (1)	0	1	1
		TB1.0 (1)	1		

(1) Not available on all devices and package types.
(2) Direction controlled by eUSCI_A0 module.
(3) Direction controlled by eUSCI_B0 module.

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6.11.5 Port P2 (P2.3 and P2.4) Input/Output With Schmitt Trigger

图 6-13 shows the port diagram. 表 6-43 summarizes the selection of the pin functions.

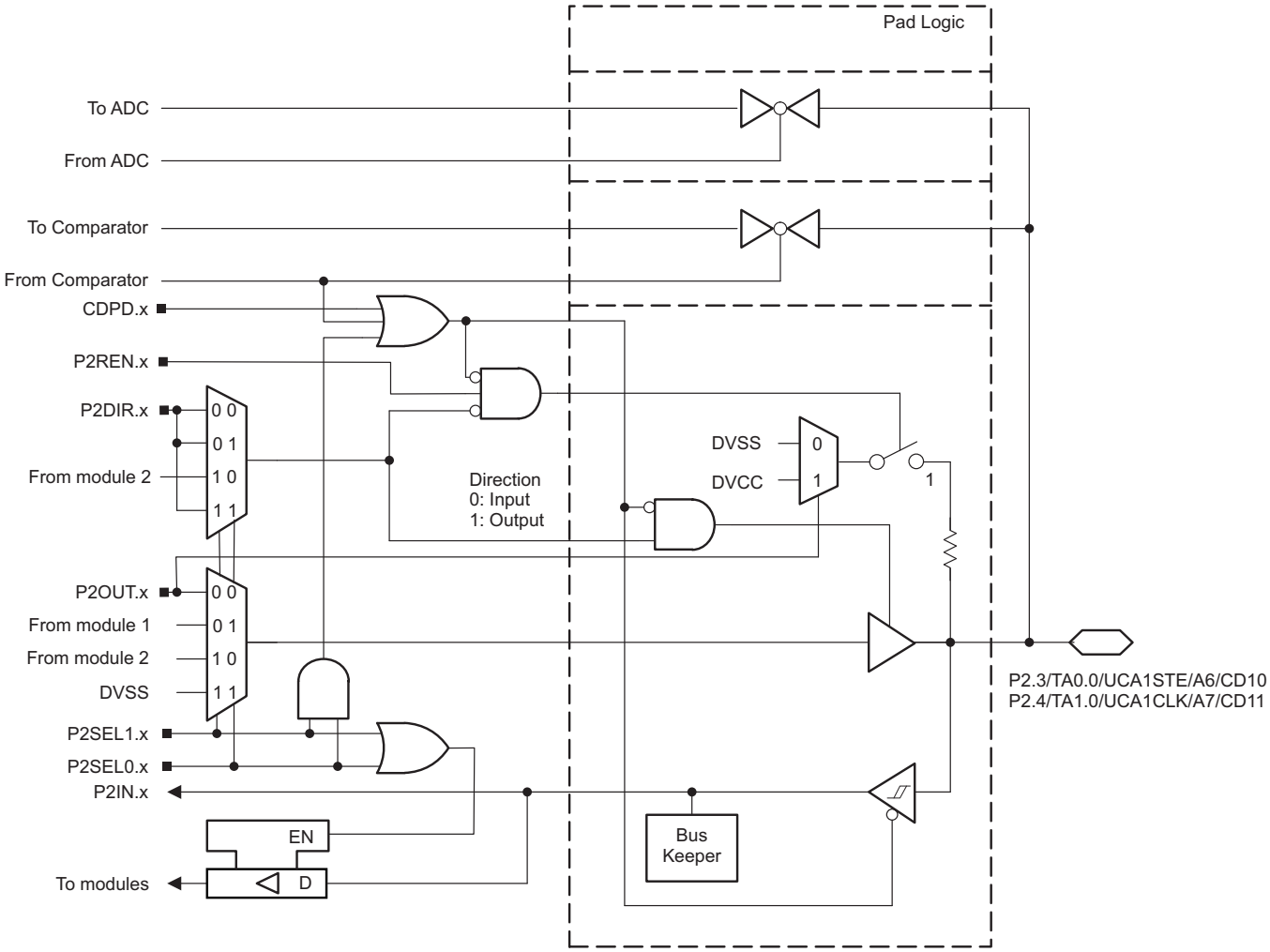

图 6-13. Port P2 (P2.3 and P2.4) Diagram

表 6-43. Port P2 (P2.3 and P2.4) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.3/TA0.0/UCA1STE/A6/CD10	3	P2.3 (I/O)	I: 0; O: 1	0	0
		TA0.CCI0B	0	0	1
		TA0.0	1		
		UCA1STE	X (1)	1	0
		A6 (2) (3) CD10 (2) (4)	X	1	1
P2.4/TA1.0/UCA1CLK/A7/CD11	4	P2.4 (I/O)	I: 0; O: 1	0	0
		TA1.CCI0B	0	0	1
		TA1.0	1		
		UCA1CLK	X (1)	1	0
		A7 (2) (3) CD11 (2) (4)	X	1	1

(1) Direction controlled by eUSCI_A1 module.
(2) Setting P2SEL1.x and P2SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Not available on all devices and package types.
(4) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.

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6.11.6 Port P2 (P2.5 and P2.6) Input/Output With Schmitt Trigger

图 6-14 shows the port diagram. 表 6-44 summarizes the selection of the pin functions.

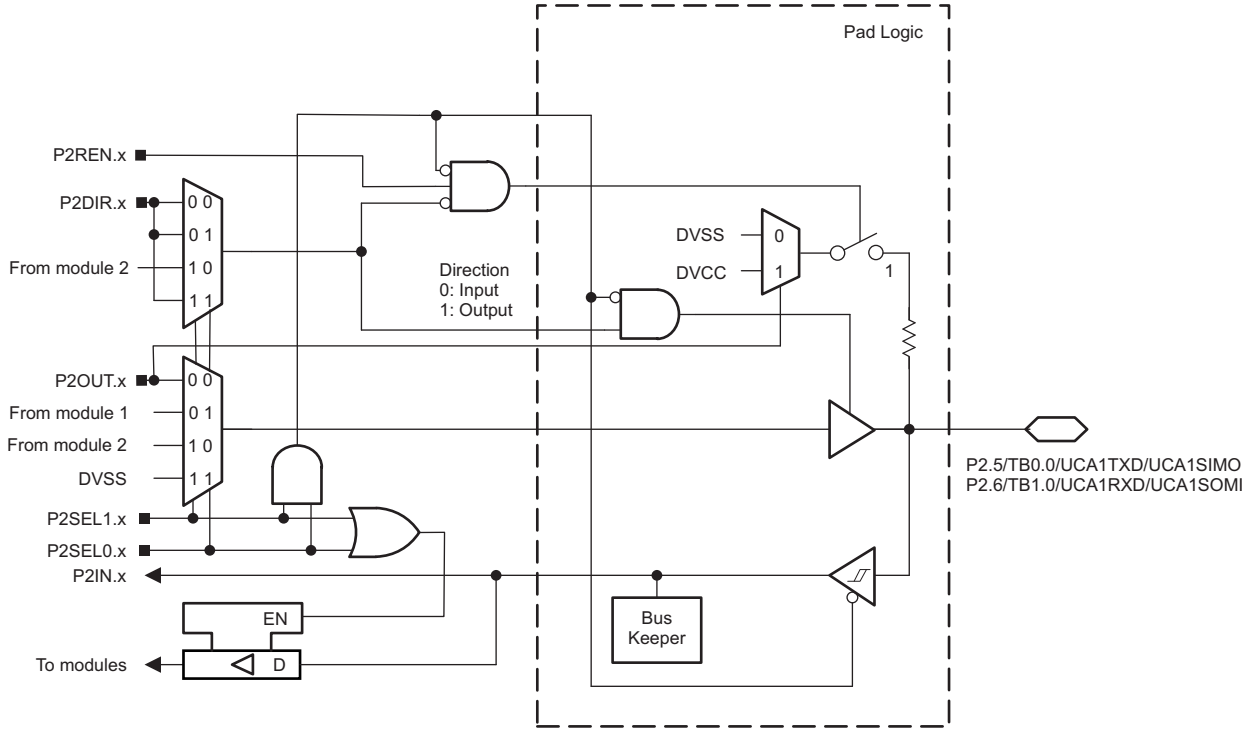

图 6-14. Port P2 (P2.5 and P2.6) Diagram

表 6-44. Port P2 (P2.5 and P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.5/TB0.0/UCA1TXD/UCA1SIMO	5	P2.5(I/O) (1)	I: 0; O: 1	0	0
		TB0.CCI0B (1)	0	0	1
		TB0.0 (1)	1		
		UCA1TXD/UCA1SIMO (1)	X (2)	1	0
P2.6/TB1.0/UCA1RXD/UCA1SOMI	6	P2.6(I/O) (1)	I: 0; O: 1	0	0
		TB1.CCI0B (1)	0	0	1
		TB1.0 (1)	1		
		UCA1RXD/UCA1SOMI (1)	X (2)	1	0

(1) Not available on all devices and package types.
(2) Direction controlled by eUSCI_A1 module.

6.11.7 Port P2 (P2.7) Input/Output With Schmitt Trigger

图 6-15 shows the port diagram. 表 6-45 summarizes the selection of the pin functions.

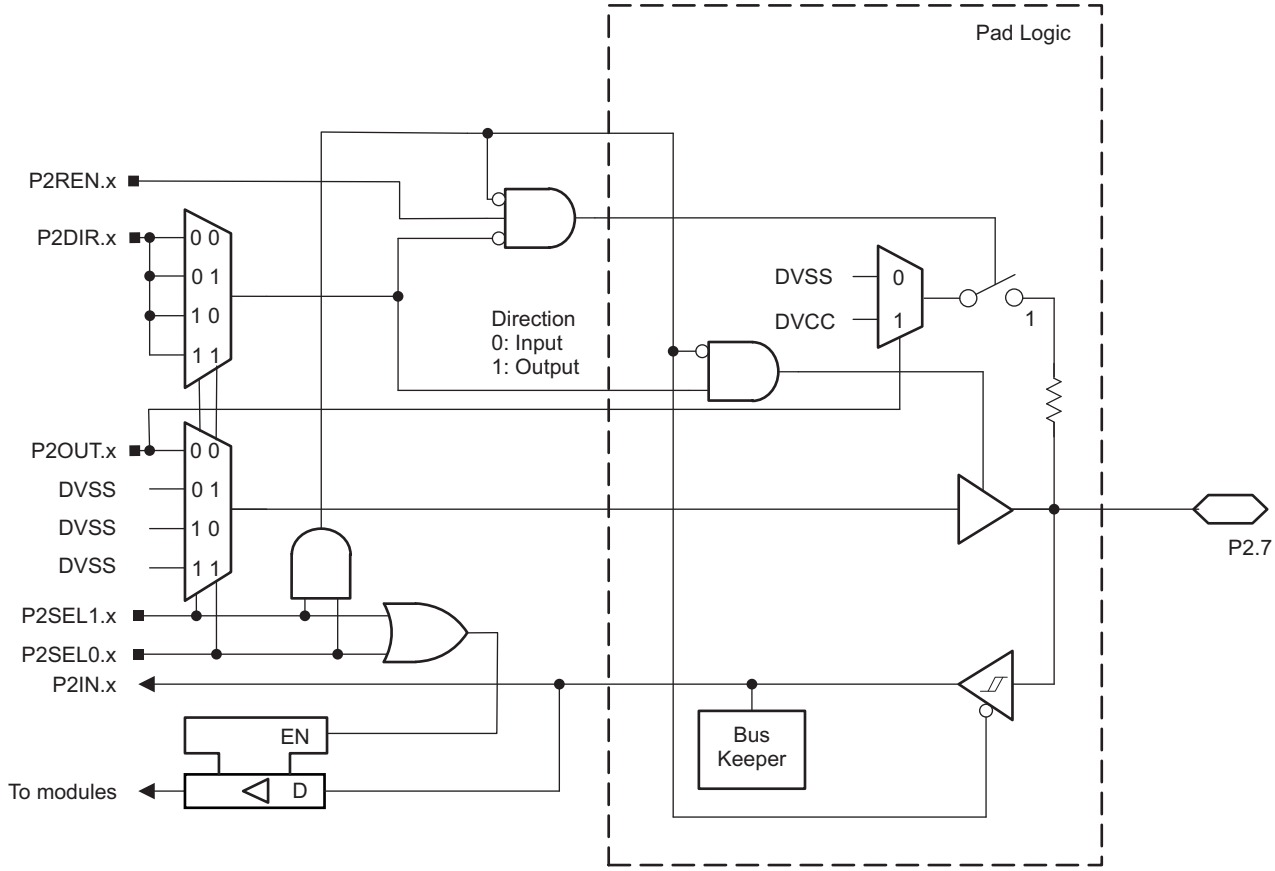

图 6-15. Port P2 (P2.7) Diagram

表 6-45. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.7	7	P2.7(I/O) (1)	I: 0; O: 1	0	0

(1) Not available on all devices and package types.

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6.11.8 Port P3 (P3.0 to P3.3) Input/Output With Schmitt Trigger

图 6-16 shows the port diagram. 表 6-46 summarizes the selection of the pin functions.

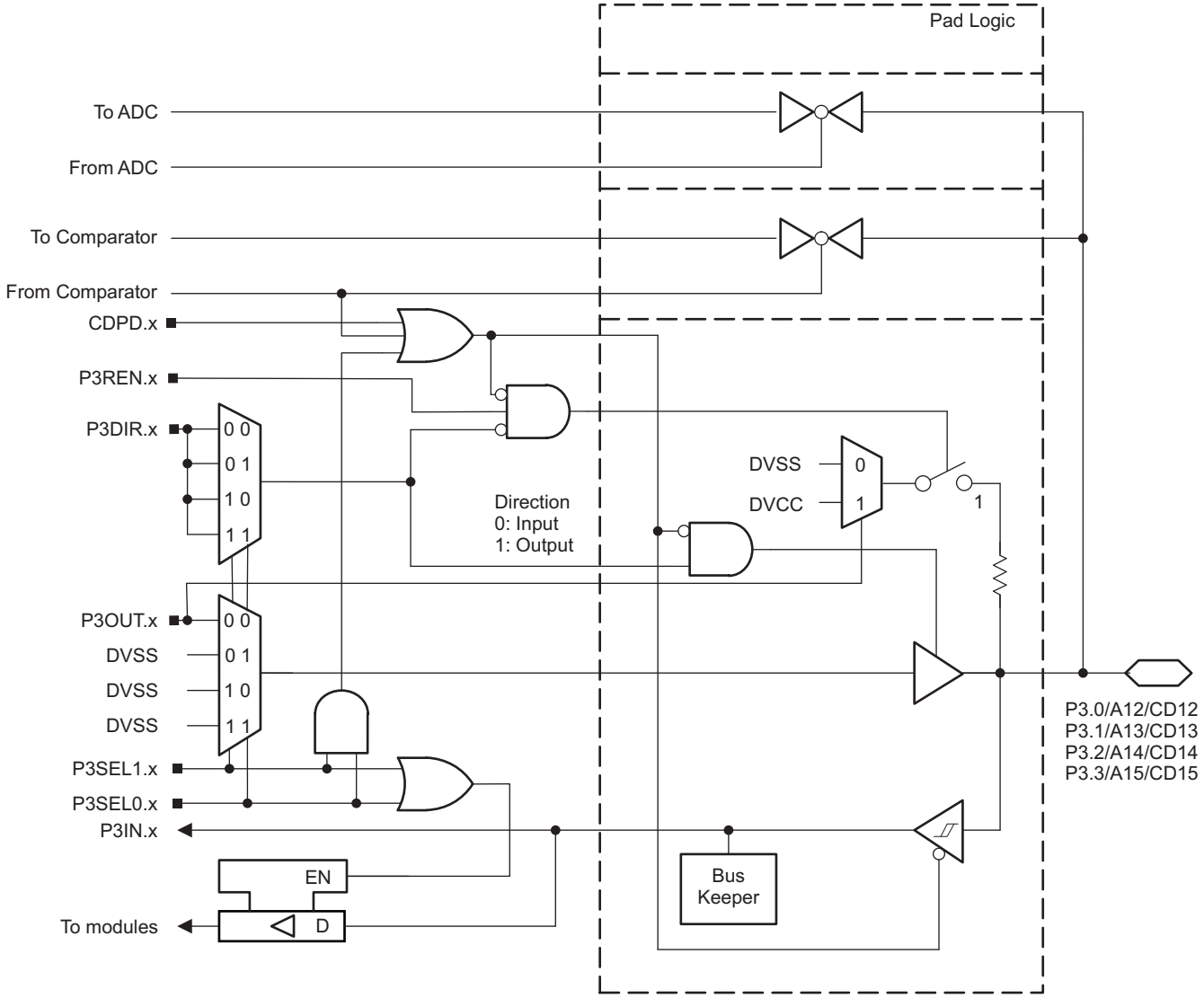

图 6-16. Port P3 (P3.0 to P3.3) Diagram

表 6-46. Port P3 (P3.0 to P3.3) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.0/A12/CD12	0	P3.0 (I/O)	I: 0; O: 1	0	0
		A12 (1) (2) CD12 (1) (3)	X	1	1
P3.1/A13/CD13	1	P3.1 (I/O)	I: 0; O: 1	0	0
		A13 (1) (2) CD13 (1) (3)	X	1	1
P3.2/A14/CD14	2	P3.2 (I/O)	I: 0; O: 1	0	0
		A14 (1) (2) CD14 (1) (3)	X	1	1
P3.3/A15/CD15	3	P3.3 (I/O)	I: 0; O: 1	0	0
		A15 (1) (2) CD15 (1) (3)	X	1	1

(1) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(2) Not available on all devices and package types.
(3) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.

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6.11.9 Port P3 (P3.4 to P3.6) Input/Output With Schmitt Trigger

图 6-17 shows the port diagram. 表 6-47 summarizes the selection of the pin functions.

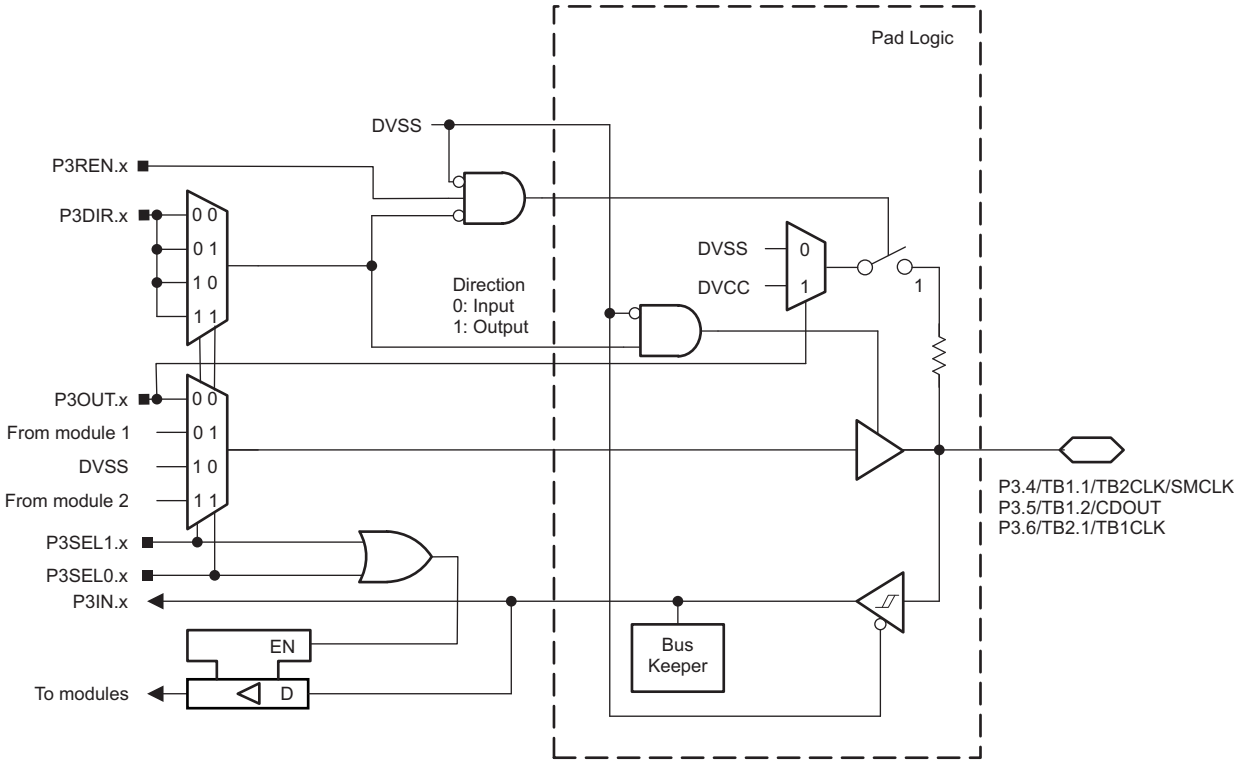

图 6-17. Port P3 (P3.4 to P3.6) Diagram

表 6-47. Port P3 (P3.4 to P3.6) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.4/TB1.1/TB2CLK/SMCLK	4	P3.4 (I/O) (1)	I: 0; O: 1	0	0
		TB1.CCI1B (1)	0	0	1
		TB1.1 (1)	1		
		TB2CLK (1)	0	1	1
		SMCLK (1)	1		
P3.5/TB1.2/CDOUT	5	P3.5 (I/O) (1)	I: 0; O: 1	0	0
		TB1.CCI2B (1)	0	0	1
		TB1.2 (1)	1		
		CDOUT (1)	1	1	1
P3.6/TB2.1/TB1CLK	6	P3.6 (I/O) (1)	I: 0; O: 1	0	0
		TB2.CCI1B (1)	0	0	1
		TB2.1 (1)	1		
		TB1CLK (1)	0	1	1

(1) Not available on all devices and package types.

6.11.10 Port Port P3 (P3.7) Input/Output With Schmitt Trigger

图 6-18 shows the port diagram. 表 6-48 summarizes the selection of the pin functions.

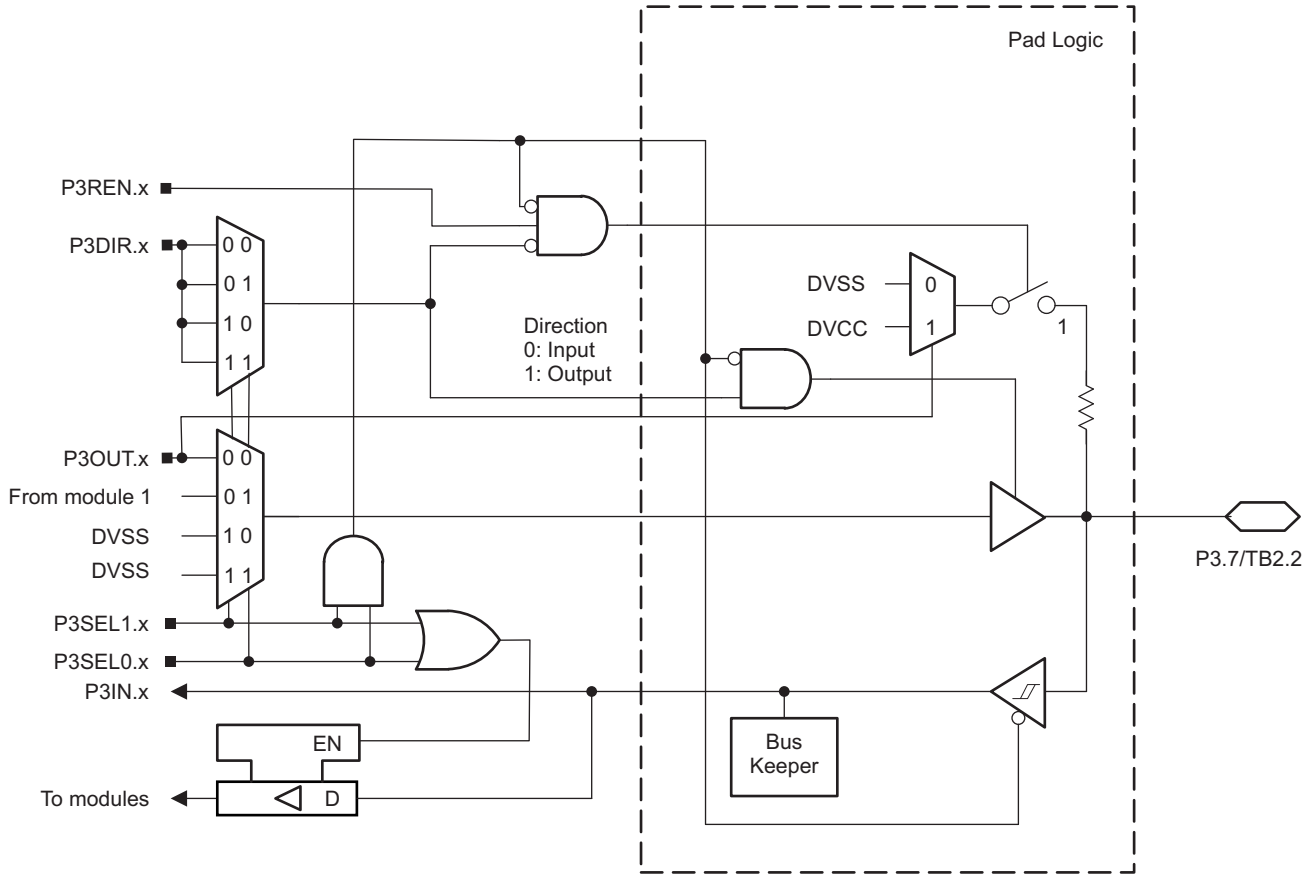

图 6-18. Port P3 (P3.7) Diagram

表 6-48. Port P3 (P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.7/TB2.2	7	P3.7 (I/O) (1)	I: 0; O: 1	0	0
		TB2.CCI2B (1)	0	0	1
		TB2.2 (1)	1		

(1) Not available on all devices and package types.

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6.11.11 Port Port P4 (P4.0) Input/Output With Schmitt Trigger

图 6-19 shows the port diagram. 表 6-49 summarizes the selection of the pin functions.

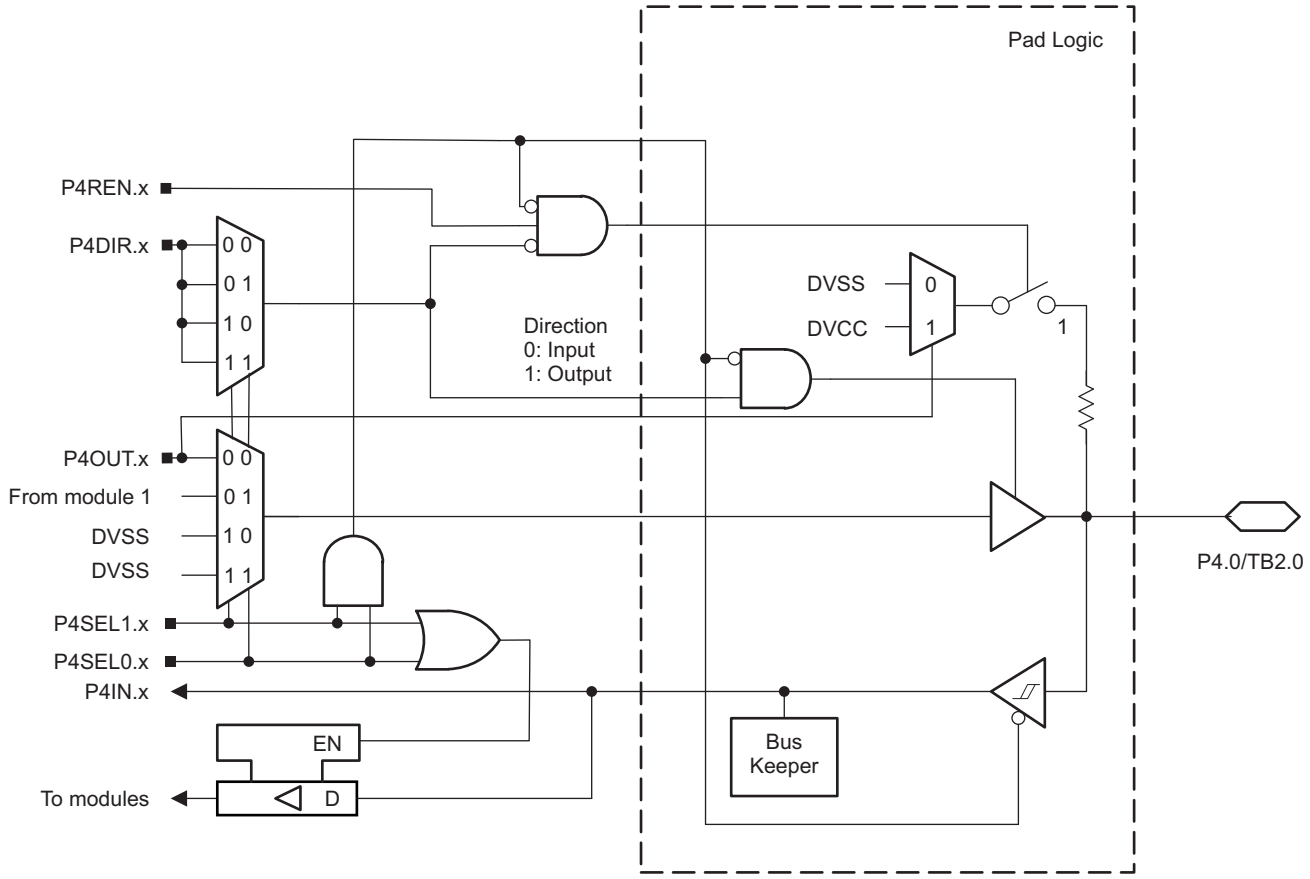

图 6-19. Port P4 (P4.0) Diagram

表 6-49. Port P4 (P4.0) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.0/TB2.0	0	P4.0 (I/O) (1)	I: 0; O: 1	0	0
		TB2.CCI0B (1)	0	0	1
		TB2.0 (1)	1		

(1) Not available on all devices and package types.

6.11.12 Port Port P4 (P4.1) Input/Output With Schmitt Trigger

图 6-20 shows the port diagram. 表 6-50 summarizes the selection of the pin functions.

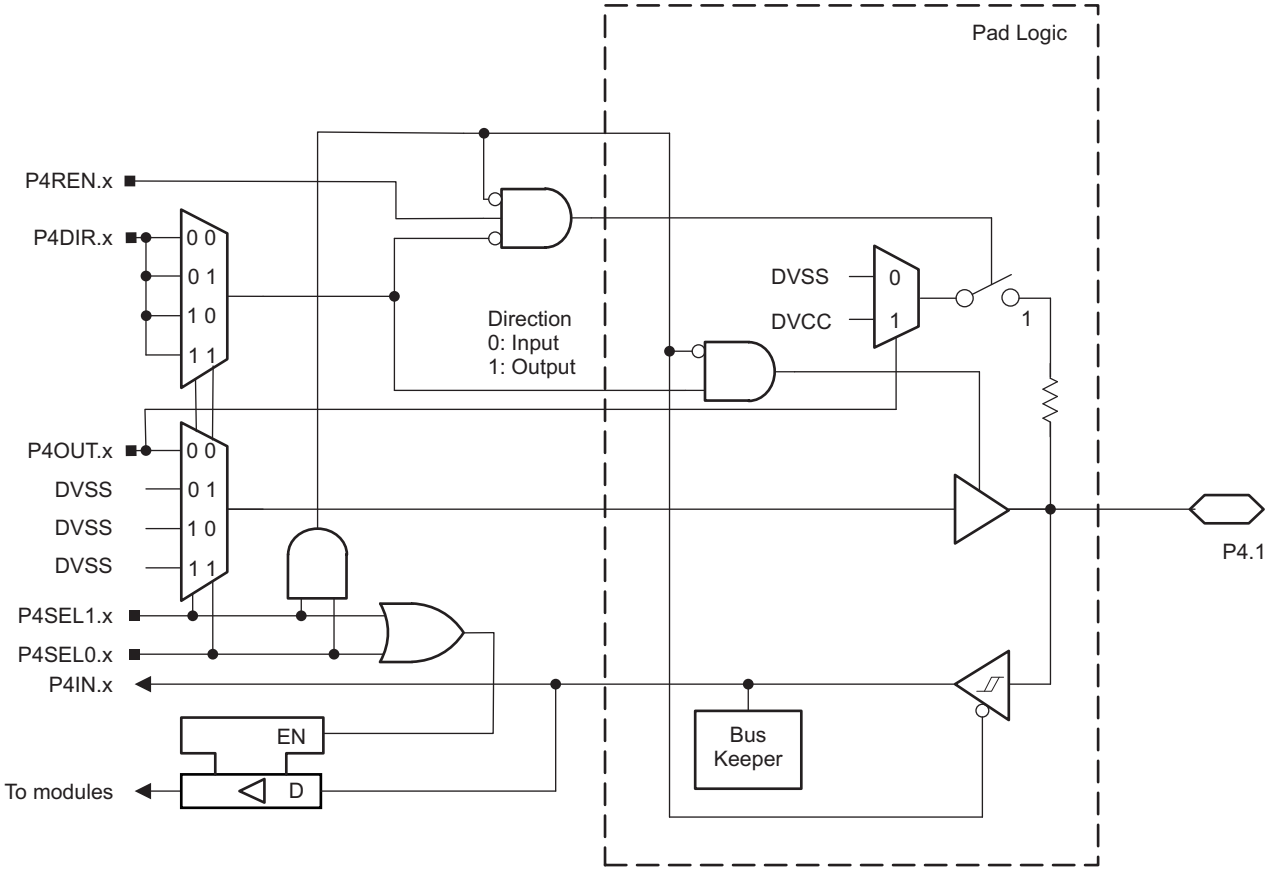

图 6-20. Port P4 (P4.1) Diagram

表 6-50. Port P4 (P4.1) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.1	1	P4.1 (I/O) (1)	I: 0; O: 1	0	0

(1) Not available on all devices and package types.

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6.11.13 Port Port PJ (PJ.0 to PJ.3) JTAG Pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

图 6-21 and 图 6-22 show the port diagrams. 表 6-51 summarizes the selection of the pin functions.

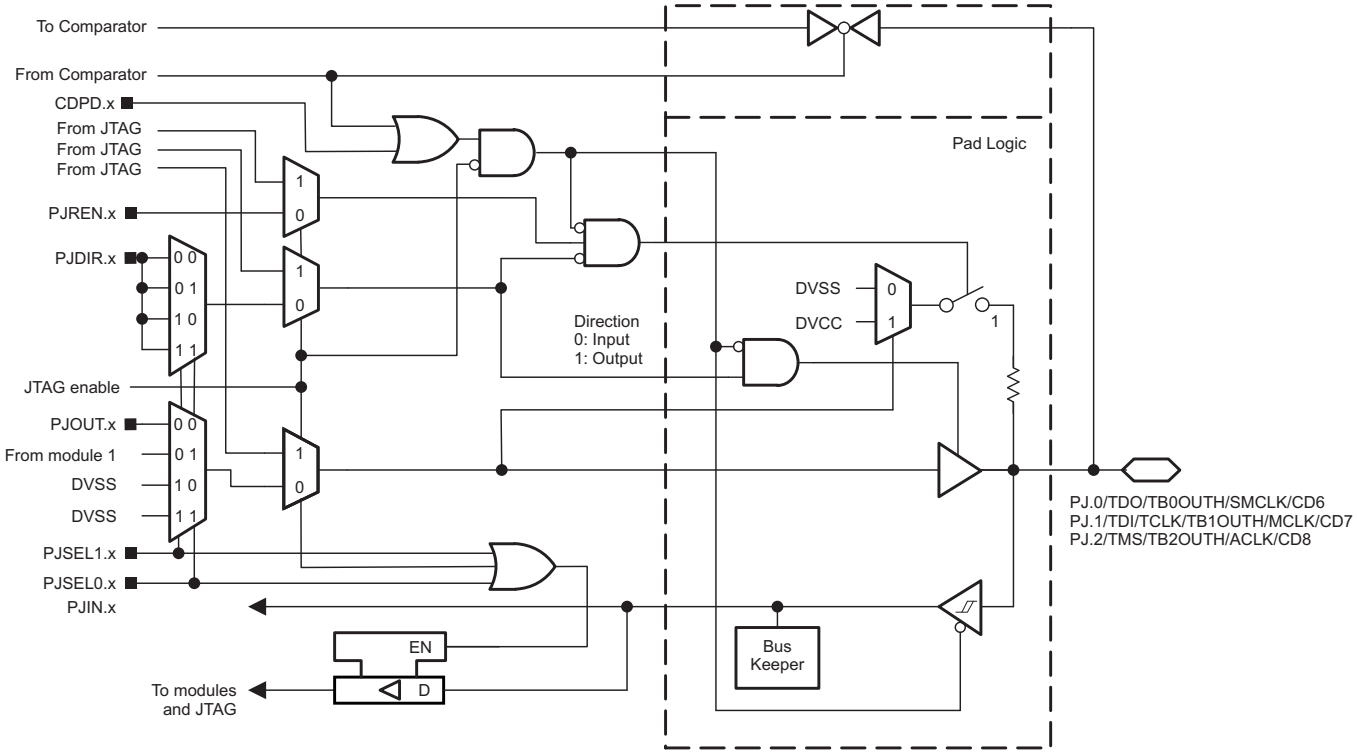

图 6-21. Port PJ (PJ.0 to PJ.2) Diagram

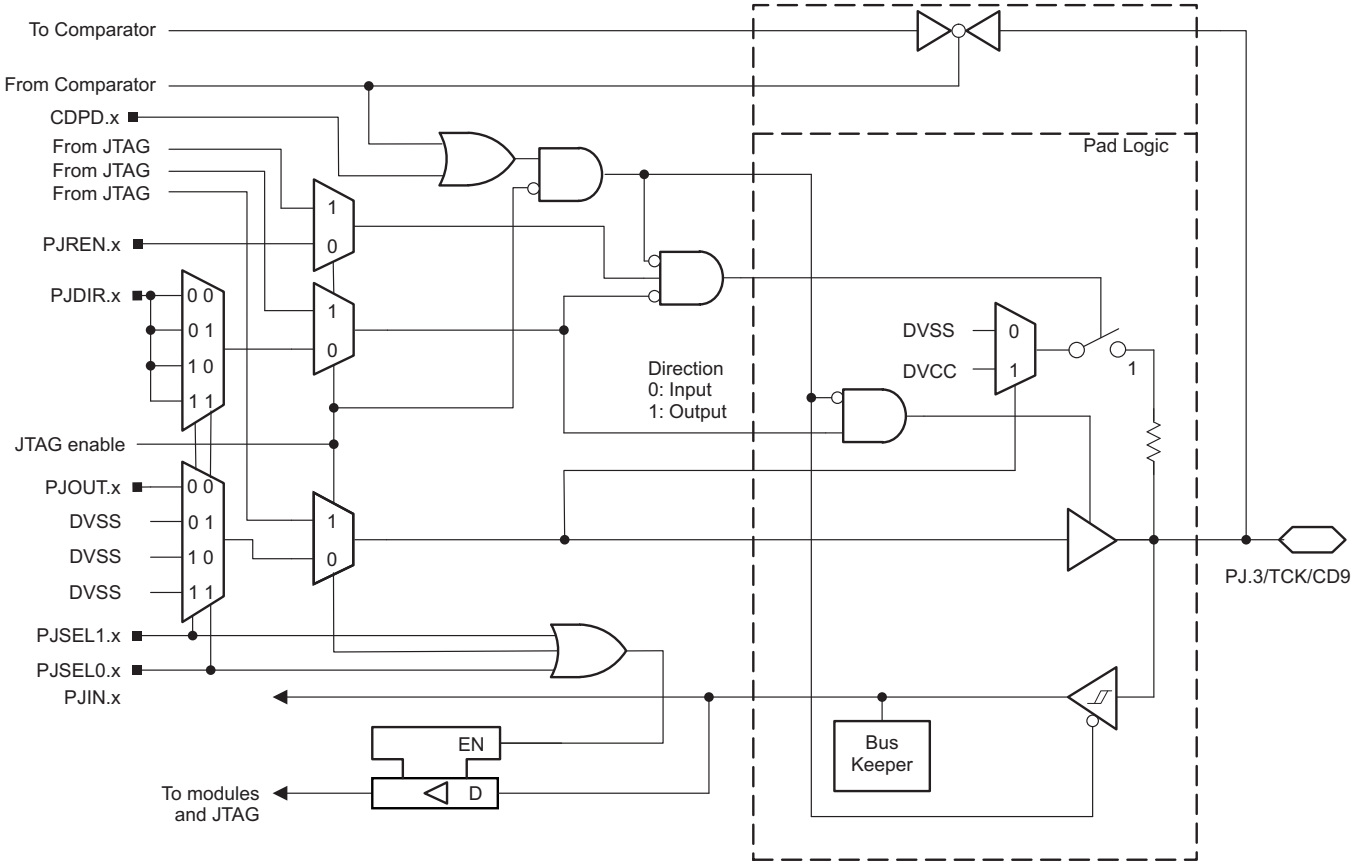

图 6-22. Port PJ (PJ.3) Diagram

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表 6-51. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			PJDIR.x	PJSEL1.x	PJSEL0.x
PJ.0/TDO/TB0OUTH/SMCLK/CD6	0	PJ.0 (I/O) (2)	I: 0; O: 1	0	0
		TDO (3)	X	X	X
		TB0OUTH	0	0	1
		SMCLK	1		
		CD6	X	1	1
PJ.1/TDI/TCLK/TB1OUTH/MCLK/CD7	1	PJ.1 (I/O) (2)	I: 0; O: 1	0	0
		TDI/TCLK (3) (4)	X	X	X
		TB1OUTH	0	0	1
		MCLK	1		
		CD7	X	1	1
PJ.2/TMS/TB2OUTH/ACLK/CD8	2	PJ.2 (I/O) (2)	I: 0; O: 1	0	0
		TMS (3) (4)	X	X	X
		TB2OUTH	0	0	1
		ACLK	1		
		CD8	X	1	1
PJ.3/TCK/CD9	3	PJ.3 (I/O) (2)	I: 0; O: 1	0	0
		TCK (3) (4)	X	X	X
		CD9	X	1	1

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made by the SYS module or by the Spy-Bi-Wire four-wire entry sequence. PJSEL1.x and PJSEL0.x have no effect in these cases.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

6.11.14 Port Port PJ (PJ.4 and PJ.5) Input/Output With Schmitt Trigger

图 6-23 and 图 6-24 show the port diagrams. 表 6-52 summarizes the selection of the pin functions.

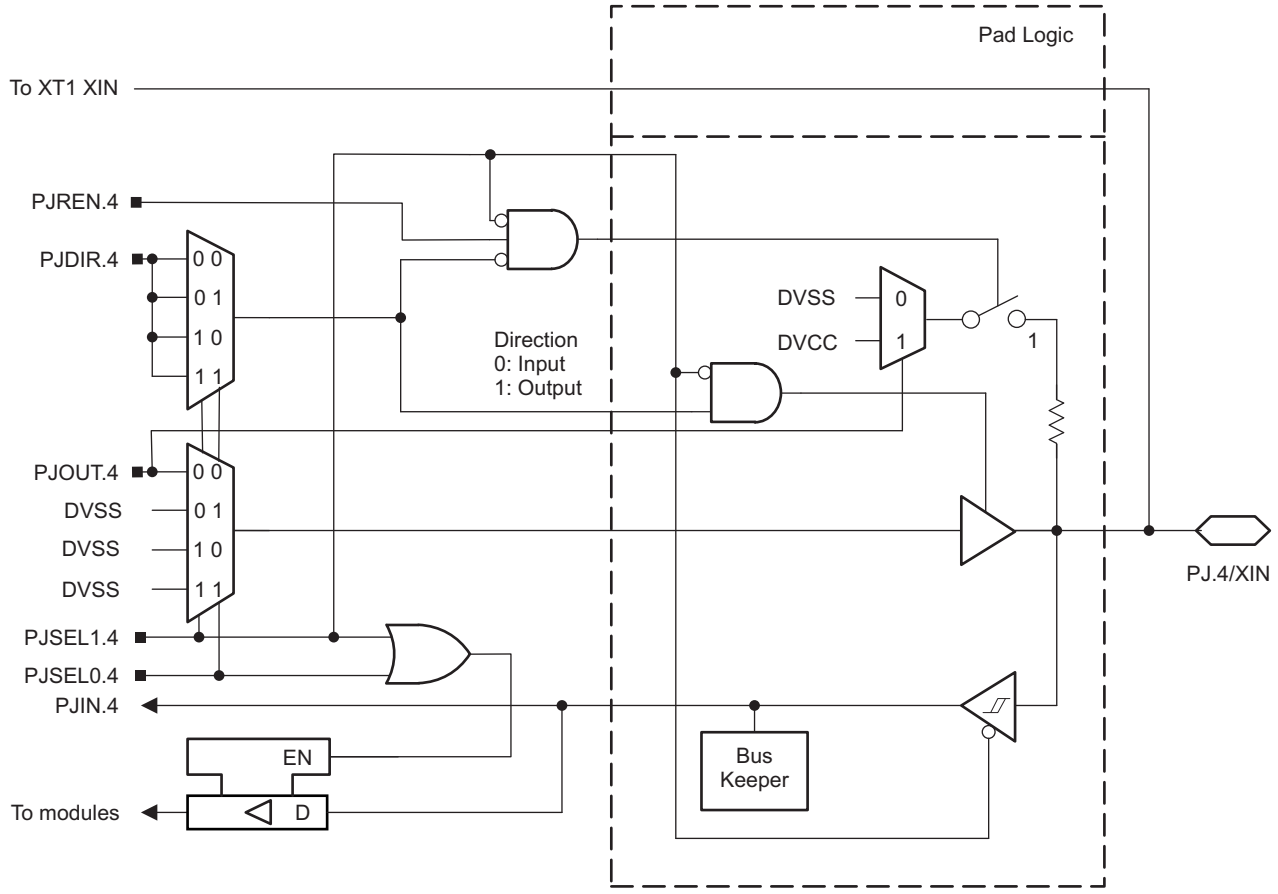

图 6-23. Port PJ (PJ.4) Diagram

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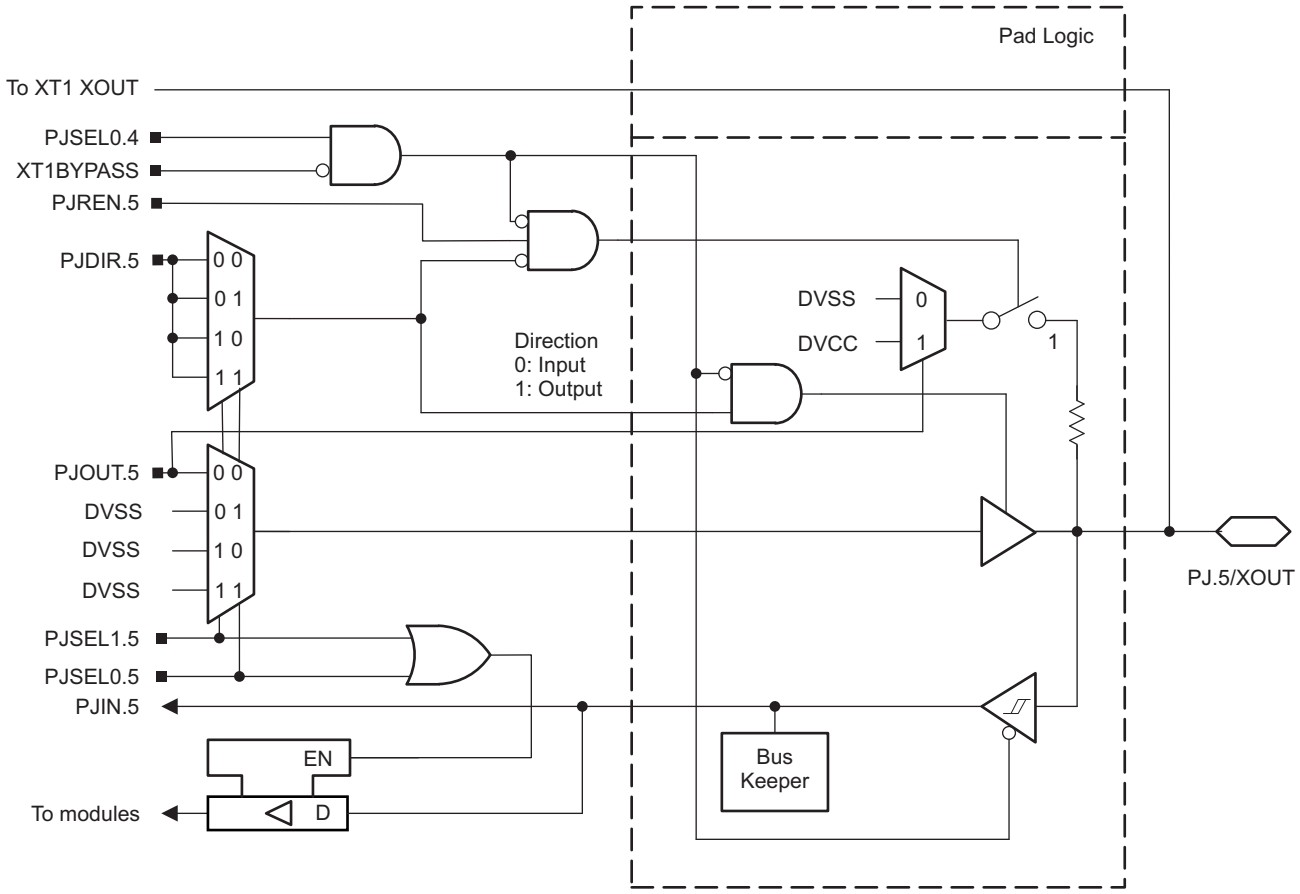

图 6-24. Port PJ (PJ.5) Diagram

表 6-52. Port PJ (PJ.4 and PJ.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)					
			PJDIR.x	PJSEL1.5	PJSEL0.5	PJSEL1.4	PJSEL0.4	XT1 BYPASS
PJ.4/XIN	4	PJ.4 (I/O)	I: 0; O: 1	X	X	0	0	X
		XIN crystal mode (2)	X	X	X	0	1	0
		XIN bypass mode (2)	X	X	X	0	1	1
PJ.5/XOUT	5	PJ.5 (I/O)	I: 0; O: 1	0	0	0	0	X
		XOUT crystal mode (2)	X	X	X	0	1	0
		PJ.5 (I/O) (3)	I: 0; O: 1	X	X	0	1	1

(1) X = Don't care
(2) Setting PJSEL1.4 = 0 and PJSEL0.4 = 1 causes the general-purpose I/O to be disabled. When XT1BYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are don't care. When XT1BYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.
(3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.

6.12 Device Descriptors (TLV)

表 6-53 and 表 6-54 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

表 6-53. Device Descriptor Table (1)

DESCRIPTION		ADDRESS	VALUE				
			FR5739	FR5738	FR5737	FR5736	FR5735
Info Block	Info length	01A00h	05h	05h	05h	05h	05h
	CRC length	01A01h	05h	05h	05h	05h	05h
	CRC value	01A02h	per unit	per unit	per unit	per unit	per unit
		01A03h	per unit	per unit	per unit	per unit	per unit
	Device ID	01A04h	03h	02h	01h	77h	76h
	Device ID	01A05h	81h	81h	81h	81h	81h
	Hardware revision	01A06h	per unit	per unit	per unit	per unit	per unit
	Firmware revision	01A07h	per unit	per unit	per unit	per unit	per unit
Die Record	Die record tag	01A08h	08h	08h	08h	08h	08h
	Die record length	01A09h	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	per unit	per unit	per unit	per unit	per unit
		01A0Bh	per unit	per unit	per unit	per unit	per unit
		01A0Ch	per unit	per unit	per unit	per unit	per unit
		01A0Dh	per unit	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	per unit	per unit	per unit	per unit	per unit
		01A0Fh	per unit	per unit	per unit	per unit	per unit
	Die Y position	01A10h	per unit	per unit	per unit	per unit	per unit
		01A11h	per unit	per unit	per unit	per unit	per unit
	Test results	01A12h	per unit	per unit	per unit	per unit	per unit
		01A13h	per unit	per unit	per unit	per unit	per unit
ADC10 Calibration	ADC10 calibration tag	01A14h	13h	13h	13h	05h	13h
	ADC10 calibration length	01A15h	10h	10h	10h	10h	10h
	ADC gain factor	01A16h	per unit	per unit	NA	NA	per unit
		01A17h	per unit	per unit	NA	NA	per unit
	ADC offset	01A18h	per unit	per unit	NA	NA	per unit
		01A19h	per unit	per unit	NA	NA	per unit
	ADC 1.5-V reference Temp. sensor 30°C	01A1Ah	per unit	per unit	NA	NA	per unit
		01A1Bh	per unit	per unit	NA	NA	per unit
	ADC 1.5-V reference Temp. sensor 85°C	01A1Ch	per unit	per unit	NA	NA	per unit
		01A1Dh	per unit	per unit	NA	NA	per unit
	ADC 2.0-V reference Temp. sensor 30°C	01A1Eh	per unit	per unit	NA	NA	per unit
		01A1Fh	per unit	per unit	NA	NA	per unit
	ADC 2.0-V reference Temp. sensor 85°C	01A20h	per unit	per unit	NA	NA	per unit
		01A21h	per unit	per unit	NA	NA	per unit
	ADC 2.5-V reference Temp. sensor 30°C	01A22h	per unit	per unit	NA	NA	per unit
		01A23h	per unit	per unit	NA	NA	per unit
	ADC 2.5-V reference Temp. sensor 85°C	01A24h	per unit	per unit	NA	NA	per unit
		01A25h	per unit	per unit	NA	NA	per unit

(1) NA = Not applicable

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表 6-53. Device Descriptor Table [(1)] (continued)

DESCRIPTION		ADDRESS	VALUE				
			FR5739	FR5738	FR5737	FR5736	FR5735
REF Calibration	REF calibration tag	01A26h	12h	12h	12h	12h	12h
	REF calibration length	01A27h	06h	06h	06h	06h	06h
	REF 1.5-V reference	01A28h	per unit	per unit	per unit	per unit	per unit
		01A29h	per unit	per unit	per unit	per unit	per unit
	REF 2.0-V reference	01A2Ah	per unit	per unit	per unit	per unit	per unit
		01A2Bh	per unit	per unit	per unit	per unit	per unit
	REF 2.5-V reference	01A2Ch	per unit	per unit	per unit	per unit	per unit
		01A2Dh	per unit	per unit	per unit	per unit	per unit

表 6-54. Device Descriptor Table [(1)]

DESCRIPTION		ADDRESS	VALUE				
			FR5734	FR5733	FR5732	FR5731	FR5730
Info Block	Info length	01A00h	05h	05h	05h	05h	05h
	CRC length	01A01h	05h	05h	05h	05h	05h
	CRC value	01A02h	per unit	per unit	per unit	per unit	per unit
		01A03h	per unit	per unit	per unit	per unit	per unit
	Device ID	01A04h	00h	7Fh	75h	7Eh	7Ch
	Device ID	01A05h	81h	80h	81h	80h	80h
	Hardware revision	01A06h	per unit	per unit	per unit	per unit	per unit
	Firmware revision	01A07h	per unit	per unit	per unit	per unit	per unit
Die Record	Die record tag	01A08h	08h	08h	08h	08h	08h
	Die record length	01A09h	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	per unit	per unit	per unit	per unit	per unit
		01A0Bh	per unit	per unit	per unit	per unit	per unit
		01A0Ch	per unit	per unit	per unit	per unit	per unit
		01A0Dh	per unit	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	per unit	per unit	per unit	per unit	per unit
		01A0Fh	per unit	per unit	per unit	per unit	per unit
	Die Y position	01A10h	per unit	per unit	per unit	per unit	per unit
		01A11h	per unit	per unit	per unit	per unit	per unit
	Test results	01A12h	per unit	per unit	per unit	per unit	per unit
		01A13h	per unit	per unit	per unit	per unit	per unit

(1) NA = Not applicable

表 6-54. Device Descriptor Table [(1)] (continued)

DESCRIPTION		ADDRESS	VALUE				
			FR5734	FR5733	FR5732	FR5731	FR5730
ADC10 Calibration	ADC10 calibration tag	01A14h	13h	13h	13h	05h	13h
	ADC10 calibration length	01A15h	10h	10h	10h	10h	10h
	ADC gain factor	01A16h	per unit	NA	NA	per unit	per unit
		01A17h	per unit	NA	NA	per unit	per unit
	ADC Offset	01A18h	per unit	NA	NA	per unit	per unit
		01A19h	per unit	NA	NA	per unit	per unit
	ADC 1.5-V reference Temp. sensor 30°C	01A1Ah	per unit	NA	NA	per unit	per unit
		01A1Bh	per unit	NA	NA	per unit	per unit
	ADC 1.5-V reference Temp. sensor 85°C	01A1Ch	per unit	NA	NA	per unit	per unit
		01A1Dh	per unit	NA	NA	per unit	per unit
	ADC 2.0-V reference Temp. sensor 30°C	01A1Eh	per unit	NA	NA	per unit	per unit
		01A1Fh	per unit	NA	NA	per unit	per unit
	ADC 2.0-V reference Temp. sensor 85°C	01A20h	per unit	NA	NA	per unit	per unit
		01A21h	per unit	NA	NA	per unit	per unit
	ADC 2.5-V reference Temp. sensor 30°C	01A22h	per unit	NA	NA	per unit	per unit
		01A23h	per unit	NA	NA	per unit	per unit
	ADC 2.5-V reference Temp. sensor 85°C	01A24h	per unit	NA	NA	per unit	per unit
		01A25h	per unit	NA	NA	per unit	per unit
REF Calibration	REF calibration tag	01A26h	12h	12h	12h	12h	12h
	REF Calibration length	01A27h	06h	06h	06h	06h	06h
	REF 1.5-V reference	01A28h	per unit	per unit	per unit	per unit	per unit
		01A29h	per unit	per unit	per unit	per unit	per unit
	REF 2.0-V reference	01A2Ah	per unit	per unit	per unit	per unit	per unit
		01A2Bh	per unit	per unit	per unit	per unit	per unit
	REF 2.5-V reference	01A2Ch	per unit	per unit	per unit	per unit	per unit
		01A2Dh	per unit	per unit	per unit	per unit	per unit

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7 器件和文档支持

7.1 开始使用

TI 还提供了立即入门必备的所有硬件平台和软件组件以及工具！不仅如此，TI 还拥有众多辅助组件以满足您的需求。要获得 MSP430™MCU 产品线、可用开发工具和评估套件，以及高级开发资源，请访问 MSP430 入门网页。

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430 MCU devices and support tools. Each MSP430 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430F5438A). TI recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the electrical specifications for the final device

PMS – Final silicon die that conforms to the electrical specifications for the device but has not completed quality and reliability verification

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed TI's internal qualification testing.

MSP – Fully-qualified development-support product

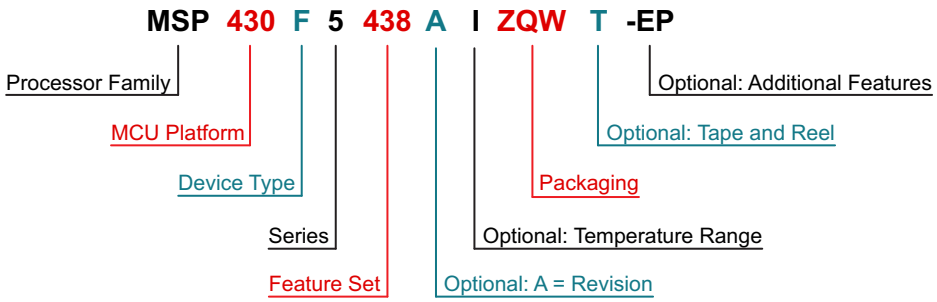
XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). 图 7-1 provides a legend for reading the complete device name for any family member.



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD 0 = Low-Voltage Series
Feature Set	Various levels of integration within a series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified	

图 **7-1. Device Nomenclature**

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7.3 工具和软件

表 7-1列出了这些微控制器 支持 的调试功能。关于可用特性的详细信息，请参见*《适用于 MSP430 的 Code Composer Studio 用户指南》*。

表 7-1. 硬件 功能

MSP430 架构	4 线 JTAG	2 线 JTAG	断点 (N)	范围断点	时钟控制	状态序列发生器	跟踪缓冲器	LPMx.5 调试支持
MSP430Xv2	有	有	3	有	是	否	否	有

设计套件与评估模块

《使用 MSP430 FRAM 微控制器实现 EEPROM 仿真和感测》 此 TI 参考设计描述了如何将 MSP430™ 超低功耗微控制器 (MCU) 上的铁电随机存取存储器 (FRAM) 技术与使用 MCU 时可启用的附加感测功能搭配用来仿真 EEPROM。此参考设计支持通过 I2C 和 SPI 接口连接至主机处理器，以进行多从器件寻址。

MSP-EXP430FR5739 实验板 MSP-EXP430FR5739 实验板是一套适用于 MSP430FR57xx 器件的开发平台。它支持集成有铁电随机存取存储器 (FRAM) 的新一代微控制器器件 MSP430。该实验板兼容多种 TI 低功耗 RF 无线评估模块（例如，CC2520EMK）。该实验板可帮助设计人员快速了解全新的 MSP430FR57xx MCU 并使用它来进行开发。MSP430FR57xx MCU 整体功耗极低，并且支持数据的快速读写，存储器的耐擦写次数无与伦比。MSP-EXP430FR5739 实验板能够帮助评估并促进数据日志 应用、能源采集、无线感测、自动计量基础设施 (AMI) 以及许多其他应用的开发。

《MSP-TS430RHA40A - 适用于 MSP430FRxx FRAM MCU 的 40 引脚目标开发板》 MSP-TS430RHA40A 是一款独立的 40 引脚 ZIF 插接目标板，适用于通过 JTAG 接口或 Spy Bi-Wire（双线制 JTAG）协议对 MSP430 MCU 系统进行在线编程和调试。

软件

MSP430Ware™ 软件 MSP430Ware 软件集合了所有 MSP430 器件的代码示例、产品说明书以及其他设计资源，打包提供给用户。除了提供已有 MSP430 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP430 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

MSP430FR573x、MSP430FR572x C 代码示例 根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

MSP 驱动程序库 驱动程序库的抽象化 API 通过提供易于使用的函数调用使您不再拘泥于 MSP430 硬件的细节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可以使用驱动程序库功能，以最低开销编写完整项目。

MSP EnergyTrace™ 技术 MSP430 微控制器的 EnergyTrace 技术是基于能量的代码分析工具，用于测量和显示应用的能量配置，同时协助优化应用以实现超低功耗。

ULP（超低功耗）Advisor ULP Advisor™软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP 和 MSP432 微控制器独特的 超低功耗 功能。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地利用应用程序。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

IEC60730 软件包 IEC60730 MSP430 软件包经过专门开发，用于协助客户达到 IEC 60730-1:2010（家用及类似用途的自动化电气控制 - 第 1 部分：一般要求）B 类产品的要求。其中涵盖家用电器、电弧检测器、电源转换器、电动工具、电动自行车及其他诸多产品。IEC60730 MSP430 软件包可以嵌入在 MSP430 中 运行的客户应用， 从而帮助客户简化其消费类器件在功能安全方面遵循 IEC 60730-1:2010 B 类规范的认证工作。

适用于 MSP 的定点数学运算库 MSP IQmath 和 Qmath 库是一套经过高度优化的高精度数学运算函数集合，适用于 C 语言开发者，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集的实时 应用， 而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

适用于 MSP430 的浮点数学运算库 TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。这是标量函数的浮点数学运算库，能够充分利用器件的智能外设，使性能提升高达 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio 和 IAR IDE 中。如需深入了解该数学运算库及相关基准，请阅读用户指南。

开发工具

适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境 Code Composer Studio 是一种集成开发环境 (IDE)，支持所有 MSP 微控制器。Code Composer Studio 包含一整套开发和调试嵌入式应用 的嵌入式软件实用程序。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种 功能。直观的 IDE 提供了单个用户界面，有助于完成应用程序开发流程的每个步骤。熟悉的实用程序和界面可提升用户的入门速度。Code Composer Studio 将 Eclipse 软件框架的优点和 TI 先进的嵌入式调试功能相结合，为嵌入式开发人员提供了一种功能丰富的优异开发环境。当 CCS 与 MSP MCU 搭配使用时，可以使用独特而强大的插件和嵌入式软件实用程序，从而充分利用 MSP 微控制器的功能。

命令行编程器 MSP Flasher 是一款基于 shell 的开源接口，可使用 JTAG 或 Spy-Bi-Wire (SBW) 通信通过 FET 编程器或 eZ430 对 MSP 微控制器进行编程。MSP Flasher 可用于将二进制文件（.txt 或 .hex 文件）直接下载到 MSP 微控制器，而无需使用 IDE。

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MSP MCU 编程器和调试器 MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件，以进行验证和调试。MSP-FET 在主机和目标 MSP 间提供调试通信通道。此外，MSP-FET 还可在计算机的 USB 接口和 MSP UART 间提供反向通道 UART 连接。这为 MSP 编程器提供了一种在 MSP 和计算机上运行的终端之间进行串行通信的便捷方法。它还支持使用 BSL（引导加载程序）通过 UART 和 I^2C 通信协议将程序（通常称为固件）加载到 MSP 目标中。

MSP-GANG 生产编程器 MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。MSP Gang 编程器配有扩展板，即“Gang 分离器”，可在 MSP Gang 编程器和多个目标器件间实施互连。提供了八条电缆，用于将扩展板与八个目标器件相连（通过 JTAG 或 SPY-Bi-Wire 连接器）。编程工作可在 PC 或独立设备上完成。PC 端具备基于 DLL 的图形化用户界面。

7.4 文档支持

以下文档介绍了 MSP430FR572x MCU。www.ti.com 网站上提供了这些文档的副本。

如需接收文档更新通知（包括芯片勘误表），请访问 ti.com 上您的器件对应的产品文件夹（例如，MSP430FR5739）。请单击右上角的“通知我”按钮。点击后，您将每周定期收到已更改的产品信息（如果有的话）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

《MSP430FR5739 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5738 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5737 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5736 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5735 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5734 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5733 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5732 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5731 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

《MSP430FR5730 器件勘误表》 描述了针对这款器件每个芯片修订版本功能技术规格的已知例外情况。

用户指南

MSP430FR57xx 系列用户指南 该器件系列提供的所有模块和 外设 的详细说明。

《使用引导加载程序 (BSL) 对 MSP430 进行编程》 MSP430 引导加载程序（BSL，之前称为引导装载程序）方便用户在原型建模阶段、最终生产和维修期间与 MSP430 微控制器中的嵌入式存储器进行通信。可编程存储器（闪存）和数据存储器 (RAM) 能够按照要求进行变更。不要将此处的引导加载程序与某些数字信号处理器 (DSP) 中将外部存储器中的程序代码（和数据）自动加载到 DSP 内部存储器的引导装载程序混为一谈。

《通过 JTAG 接口对 MSP430 进行编程》 本文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还描述了如何设定所有 MSP430 器件提供的 JTAG 访问安全熔丝。本文档介绍了使用标准 4 线 JTAG 接口和 2 线 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）访问 MCU。

《MSP430 硬件工具用户指南》 本手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

MSP430 FRAM 技术 – 操作方法和最佳实践 FRAM 采用非易失性存储器技术，行为与 SRAM 类似，支持大量新 应用的同时，还改变了固件的设计方式。该应用程序报告从嵌入式软件开发方面概述了 FRAM 技术在 MSP430 中的使用方法和最佳实践。其中讨论了如何根据应用特定的代码、常量和数据空间要求来实施存储器布局，如何使用 FRAM 来优化应用程序能耗以及如何使用存储器保护单元 (MPU) 为程序代码提供意外写访问保护，从而最大程度提高应用的稳健性。

《MSP430 FRAM 质量和可靠性》 FRAM 是一种非易失性嵌入式存储器技术并因其超低功耗特性而广为人知，同时它也是当今较为灵活且易于使用的通用型存储器解决方案。该应用报告旨在为 FRAM 的新用户和从基于闪存的 应用 转化来的用户提供有关 FRAM 如何满足关键质量和可靠性要求（诸如数据保存和耐擦写能力）的知识。

《最大限度提高 MSP430™ FRAM 的写入速度》 非易失性低功耗铁电 RAM (FRAM) 支持极其高速的写访问。该应用报告重点围绕 MSP430FRxx 系列讨论了如何使用简单技术最大限度地提高 FRAM 的写入速度。该文档以 MSP430FR5739 器件为例进行了基准测试（这些测试适用于所有基于 MSP430™ FRAM 的器件），并且讨论了 CPU 时钟频率和块大小等方面的权衡以及它们如何影响 FRAM 写入速度。

《MSP430 系统级 ESD 注意事项》 系统级 ESD 对于低电压下的硅晶技术以及经济高效型和超低功耗组件的需求日益增加。此应用报告重点讨论了三个不同的 ESD 主题，以帮助板卡设计师和原始设备制造商 (OEM) 理解和设计稳健的系统级设计产品：(1) 组件级 ESD 测试和系统级 ESD 测试，二者的差异以及为何组件级 ESD 无法确保达到系统级的稳健性。(2) 系统级 ESD 保护在不同电平下的通用设计指南（包括外壳、电缆、PCB 布局和板载 ESD 防护器件）。(3) 介绍了系统高效 ESD 设计 (SEED)。这是一种板上和片上 ESD 保护协同设计的方法论，用于实现系统级 ESD 的稳健性，配备仿真示例和测试结果。另外，还讨论了一些真实的系统级 ESD 保护设计示例及其成果。

MSP430 32kHz 晶体振荡器 对于稳定的晶体振荡器，选择合适的晶振、正确的负载电路和适当的电路板布局布线至关重要。该应用报告总结了晶体振荡器的功能，介绍了为实现 MSP430 超低功耗运行而选择正确晶体的参数。此外，还给出了正确电路板布局布线的提示和示例。本文档还包含与可能振荡器测试相关的详细信息以确保大批量生产中的稳定振荡器运行。

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7.5 相关链接

表 7-2 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **7-2.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
MSP430FR5739	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5738	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5737	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5736	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5735	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5734	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5733	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5732	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5731	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430FR5730	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

7.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的 《使用条款》。

TI E2E™ 社区
TI 的工程师交流 (E2E) 社区. 此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页
德州仪器 (TI) 嵌入式处理器维基网页。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

7.7 商标

MSP430, MSP430Ware, EnergyTrace, ULP Advisor, 适用于 MSP 微控制器的 Code Composer Studio, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

7.8 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.9 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过非披露义务的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

7.10 术语表

TI 术语表 这份术语表列出并解释术语、缩写和定义。

8 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M430FR5738IRGERG4	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5738
M430FR5738IRGERG4.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5738
MSP430FR5730IPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5730
MSP430FR5730IPW.A	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5730
MSP430FR5730IRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5730
MSP430FR5730IRGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5730
MSP430FR5730IRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5730
MSP430FR5730IRGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5730
MSP430FR5731IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5731
MSP430FR5731IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5731
MSP430FR5732IPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5732
MSP430FR5732IPW.A	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5732
MSP430FR5732IRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5732
MSP430FR5732IRGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5732
MSP430FR5733IRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5733
MSP430FR5733IRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5733
MSP430FR5733IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5733
MSP430FR5733IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5733
MSP430FR5734IPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5734

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430FR5734IPW.A	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5734
MSP430FR5734IPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5734
MSP430FR5734IPWR.A	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5734
MSP430FR5735IDA	Active	Production	TSSOP (DA) | 38	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FR5735
MSP430FR5735IDA.A	Active	Production	TSSOP (DA) | 38	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FR5735
MSP430FR5735IDAR	Active	Production	TSSOP (DA) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FR5735
MSP430FR5735IDAR.A	Active	Production	TSSOP (DA) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FR5735
MSP430FR5735IRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5735
MSP430FR5735IRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5735
MSP430FR5735IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5735
MSP430FR5735IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5735
MSP430FR5736IPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5736
MSP430FR5736IPW.A	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5736
MSP430FR5736IRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5736
MSP430FR5736IRGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5736
MSP430FR5736IRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5736
MSP430FR5736IRGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5736
MSP430FR5737IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5737
MSP430FR5737IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5737
MSP430FR5738IPW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5738
MSP430FR5738IPW.A	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5738
MSP430FR5738IPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5738
MSP430FR5738IPWR.A	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430FR5738

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430FR5738IRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5738
MSP430FR5738IRGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5738
MSP430FR5738IRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5738
MSP430FR5738IRGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	430FR 5738
MSP430FR5738IYQDR	Active	Production	DSBGA (YQD) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	430FR5738
MSP430FR5738IYQDR.A	Active	Production	DSBGA (YQD) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	430FR5738
MSP430FR5739CY	Active	Production	DIESALE (Y) | 0	780 | null	Yes	Call TI	N/A for Pkg Type	0 to 70	
MSP430FR5739CY.A	Active	Production	DIESALE (Y) | 0	780 | null	Yes	Call TI	N/A for Pkg Type	0 to 70	
MSP430FR5739IDA	Active	Production	TSSOP (DA) | 38	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FR5739
MSP430FR5739IDA.A	Active	Production	TSSOP (DA) | 38	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FR5739
MSP430FR5739IDAR	Active	Production	TSSOP (DA) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FR5739
MSP430FR5739IDAR.A	Active	Production	TSSOP (DA) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FR5739
MSP430FR5739IRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5739
MSP430FR5739IRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5739
MSP430FR5739IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5739
MSP430FR5739IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FR5739

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430FR5739 :

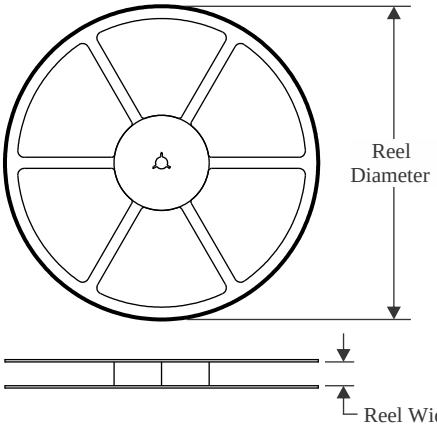
- Enhanced Product : MSP430FR5739-EP

NOTE: Qualified Version Definitions:

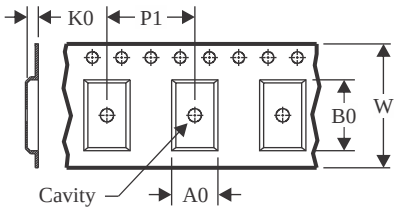
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

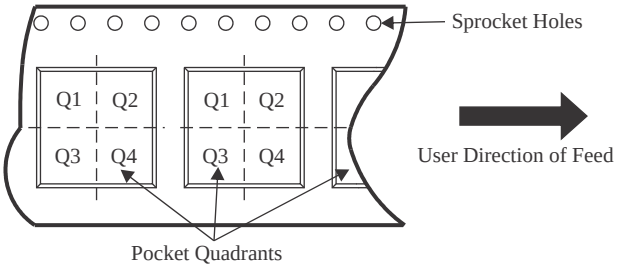


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

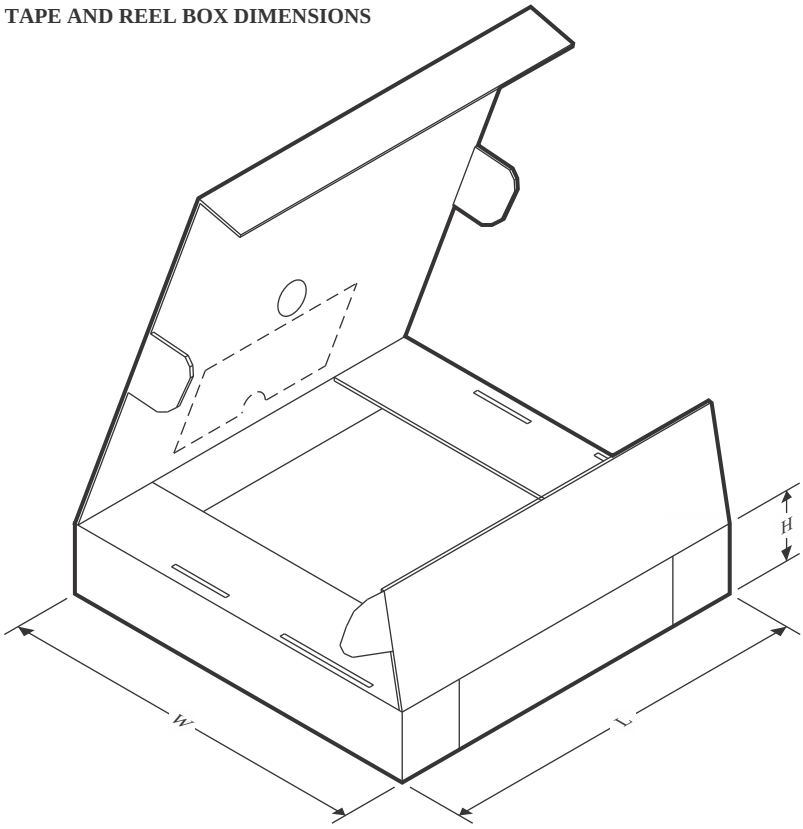


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
M430FR5738IRGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5730IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5730IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5730IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5730IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5731IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5731IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5732IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5732IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5733IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5733IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5733IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5733IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5734IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430FR5735IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR5735IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR5735IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5735IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5735IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5736IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5736IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5736IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5736IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5737IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5737IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5738IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430FR5738IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5738IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5738IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5738IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSP430FR5738IYQDR	DSBGA	YQD	24	3000	180.0	8.4	2.13	2.33	0.69	4.0	8.0	Q1
MSP430FR5739IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430FR5739IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5739IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5739IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
MSP430FR5739IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

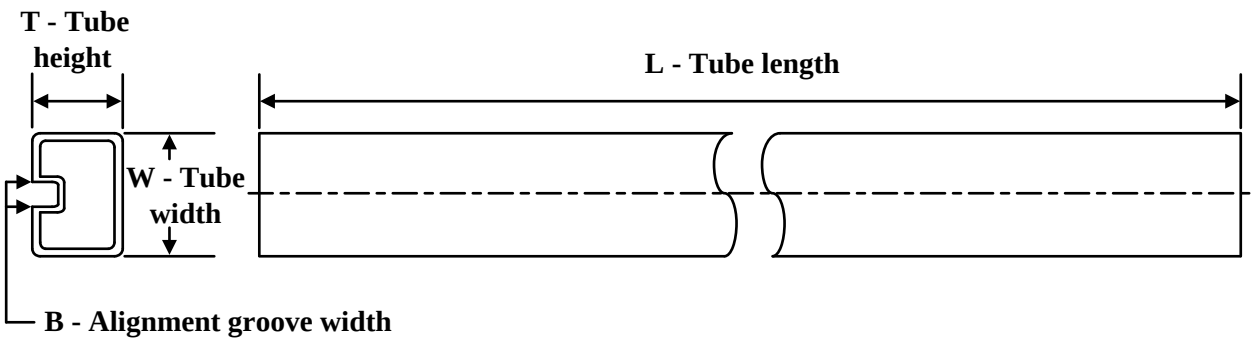


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
M430FR5738IRGERG4	VQFN	RGE	24	3000	346.0	346.0	33.0
MSP430FR5730IRGER	VQFN	RGE	24	3000	353.0	353.0	32.0
MSP430FR5730IRGER	VQFN	RGE	24	3000	346.0	346.0	33.0
MSP430FR5730IRGET	VQFN	RGE	24	250	213.0	191.0	35.0
MSP430FR5730IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430FR5731IRHAT	VQFN	RHA	40	250	213.0	191.0	35.0
MSP430FR5731IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5732IRGET	VQFN	RGE	24	250	213.0	191.0	35.0
MSP430FR5732IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430FR5733IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430FR5733IRHAR	VQFN	RHA	40	2500	353.0	353.0	32.0
MSP430FR5733IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5733IRHAT	VQFN	RHA	40	250	213.0	191.0	35.0
MSP430FR5734IPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430FR5735IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430FR5735IRHAR	VQFN	RHA	40	2500	353.0	353.0	32.0
MSP430FR5735IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430FR5735IRHAT	VQFN	RHA	40	250	213.0	191.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR5735IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5736IRGER	VQFN	RGE	24	3000	346.0	346.0	33.0
MSP430FR5736IRGER	VQFN	RGE	24	3000	353.0	353.0	32.0
MSP430FR5736IRGET	VQFN	RGE	24	250	213.0	191.0	35.0
MSP430FR5736IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430FR5737IRHAT	VQFN	RHA	40	250	213.0	191.0	35.0
MSP430FR5737IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
MSP430FR5738IPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
MSP430FR5738IRGER	VQFN	RGE	24	3000	346.0	346.0	33.0
MSP430FR5738IRGER	VQFN	RGE	24	3000	353.0	353.0	32.0
MSP430FR5738IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
MSP430FR5738IRGET	VQFN	RGE	24	250	213.0	191.0	35.0
MSP430FR5738IYQDR	DSBGA	YQD	24	3000	182.0	182.0	20.0
MSP430FR5739IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430FR5739IRHAR	VQFN	RHA	40	2500	353.0	353.0	32.0
MSP430FR5739IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
MSP430FR5739IRHAT	VQFN	RHA	40	250	213.0	191.0	35.0
MSP430FR5739IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0

TUBE

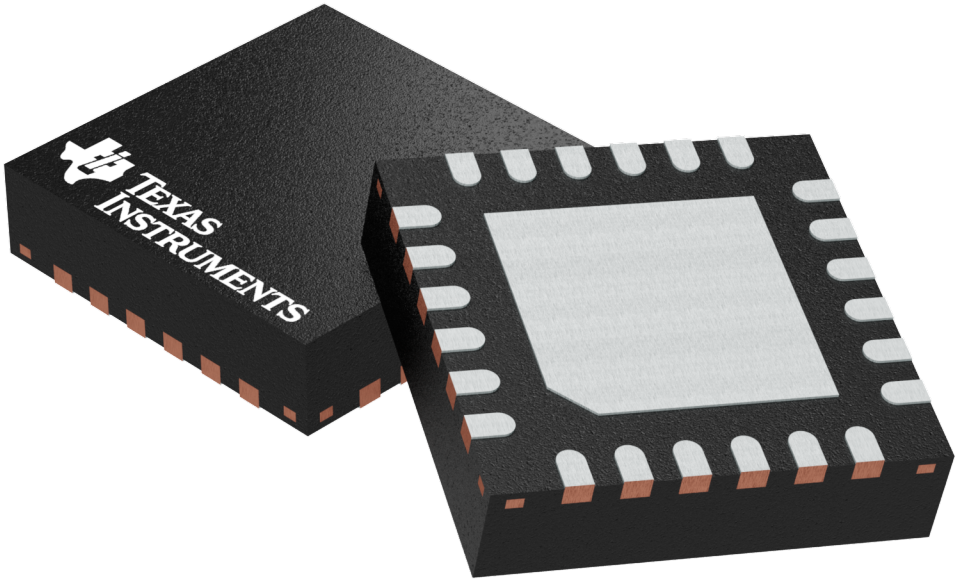


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430FR5730IPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430FR5730IPW.A	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430FR5732IPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430FR5732IPW.A	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430FR5734IPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430FR5734IPW.A	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430FR5735IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430FR5735IDA.A	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430FR5736IPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430FR5736IPW.A	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430FR5738IPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430FR5738IPW.A	PW	TSSOP	28	50	530	10.2	3600	3.5
MSP430FR5739IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430FR5739IDA.A	DA	TSSOP	38	40	530	11.89	3600	4.9

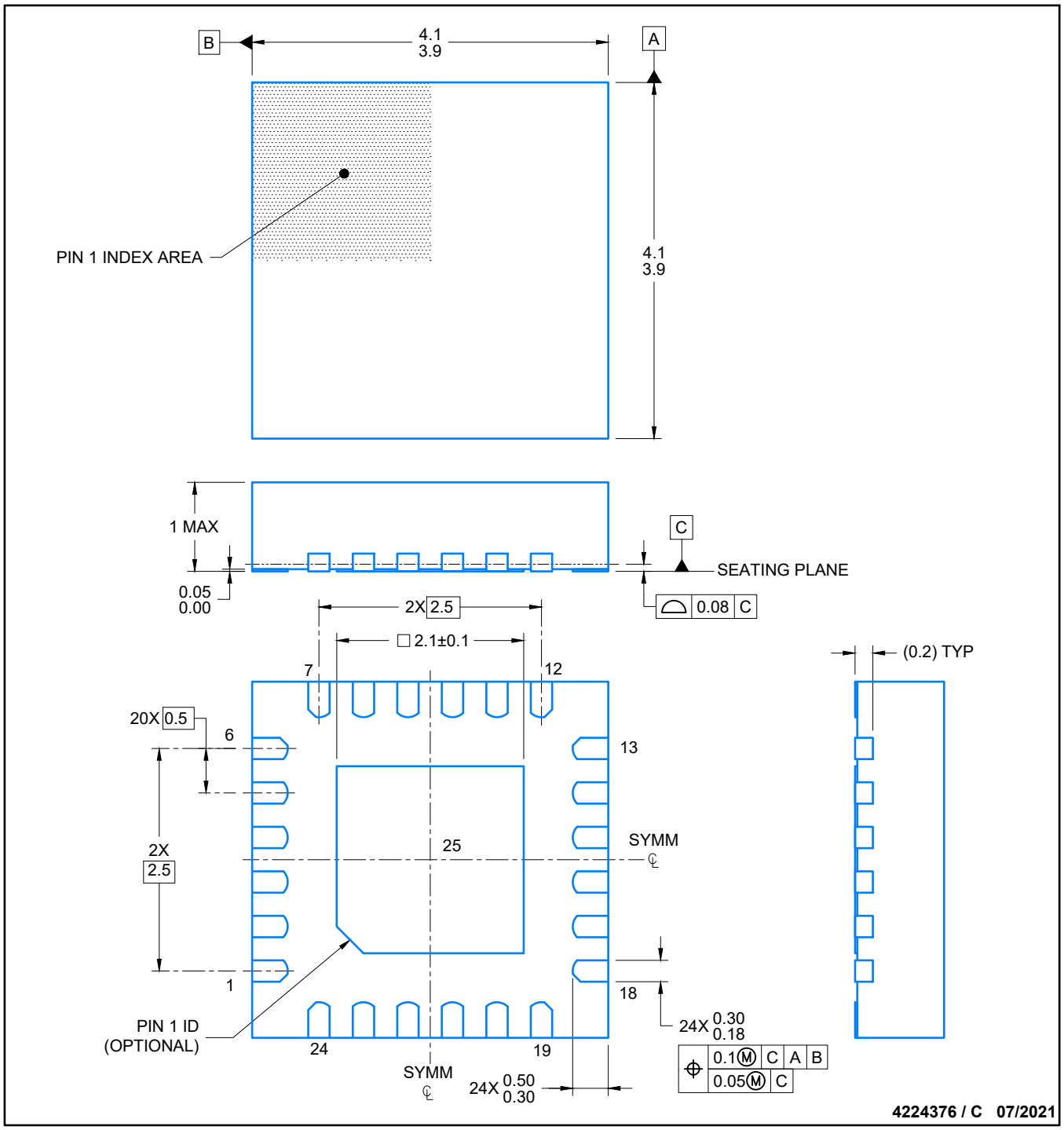
RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



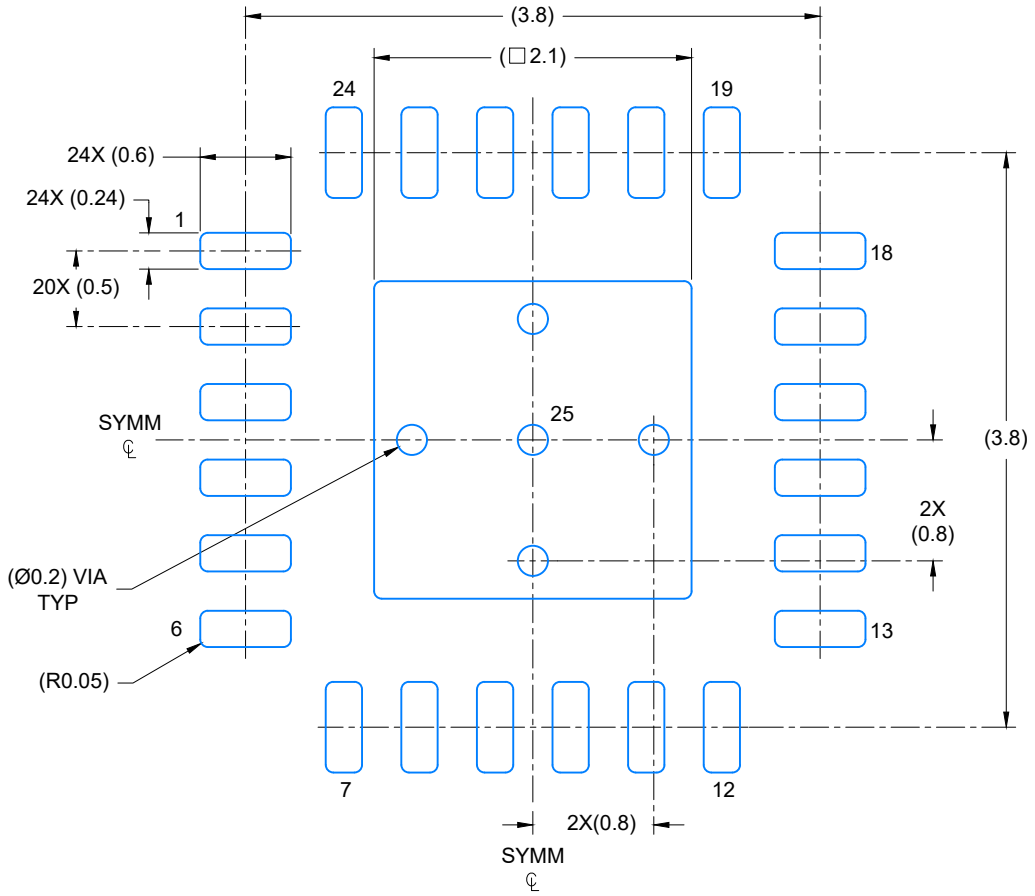
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC QUAD FLATPACK- NO LEAD

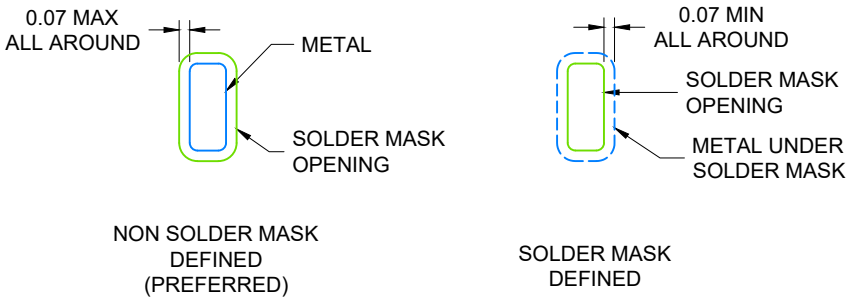


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X

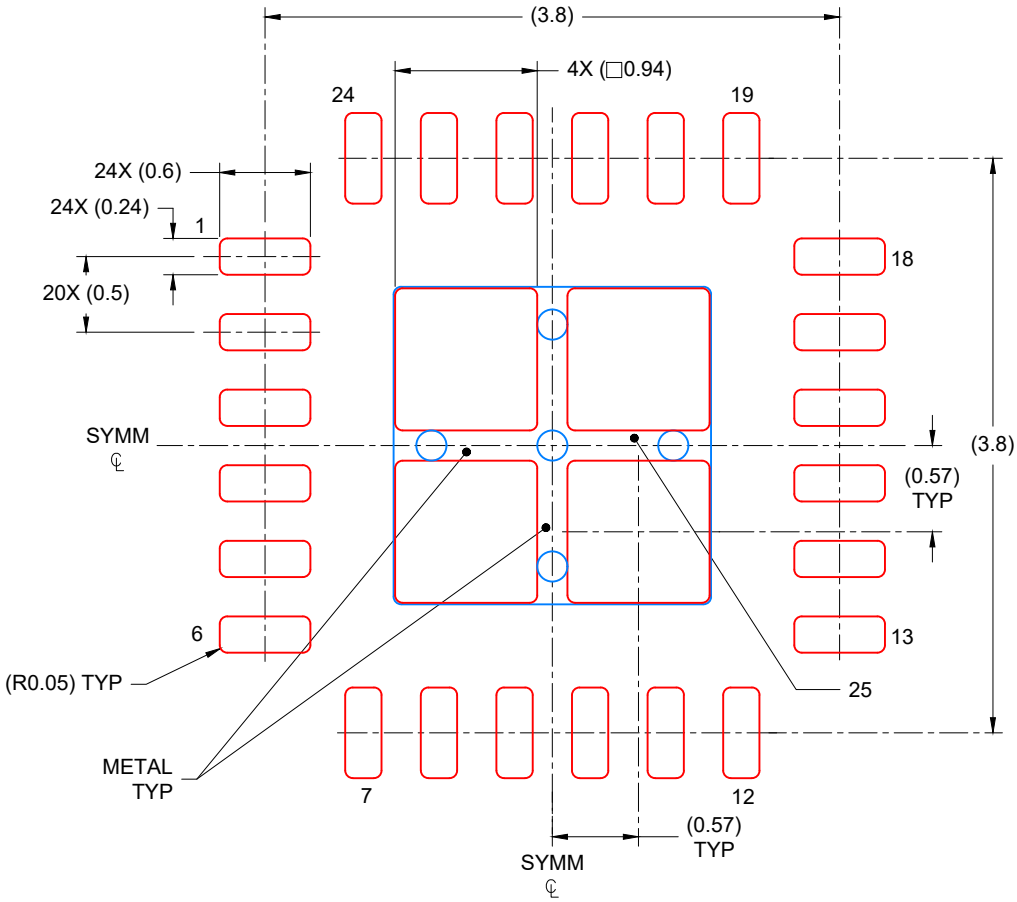


SOLDER MASK DETAILS

4224376 / C 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

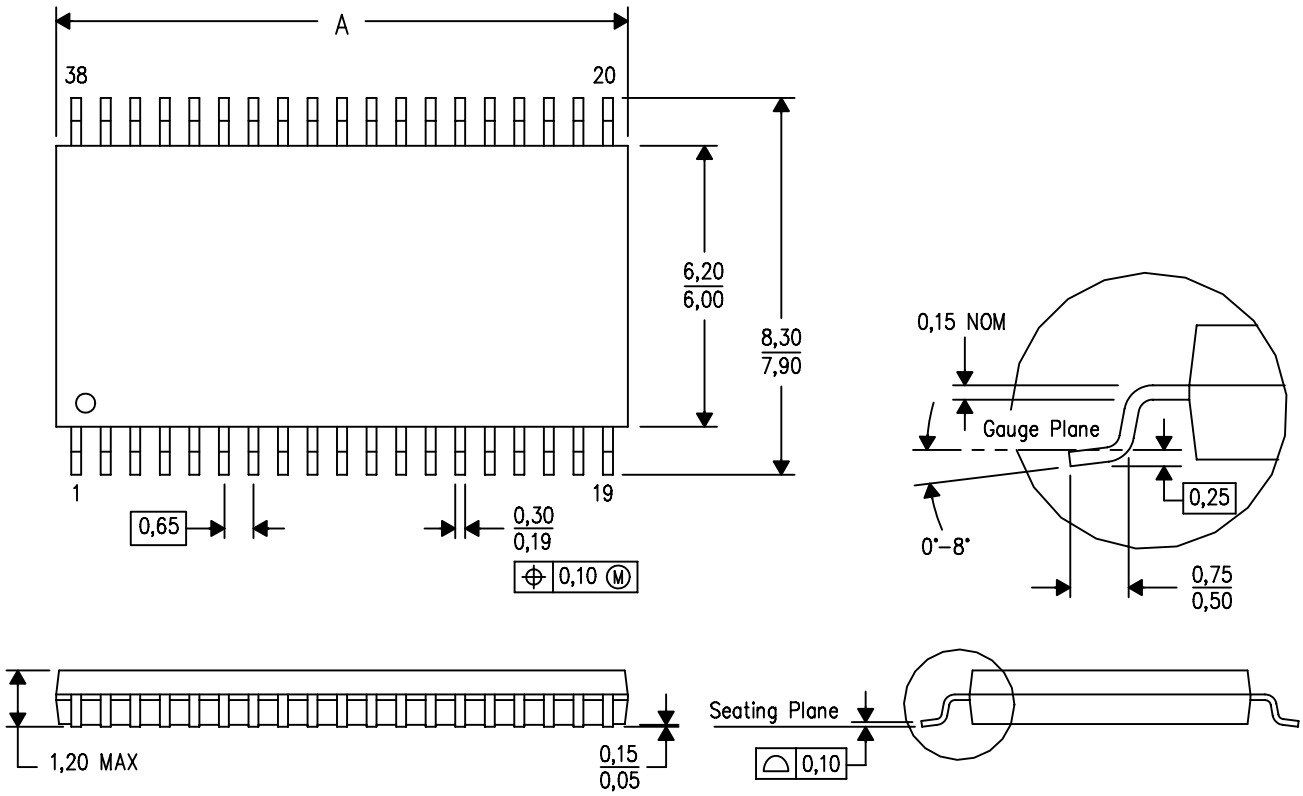
4224376 / C 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN

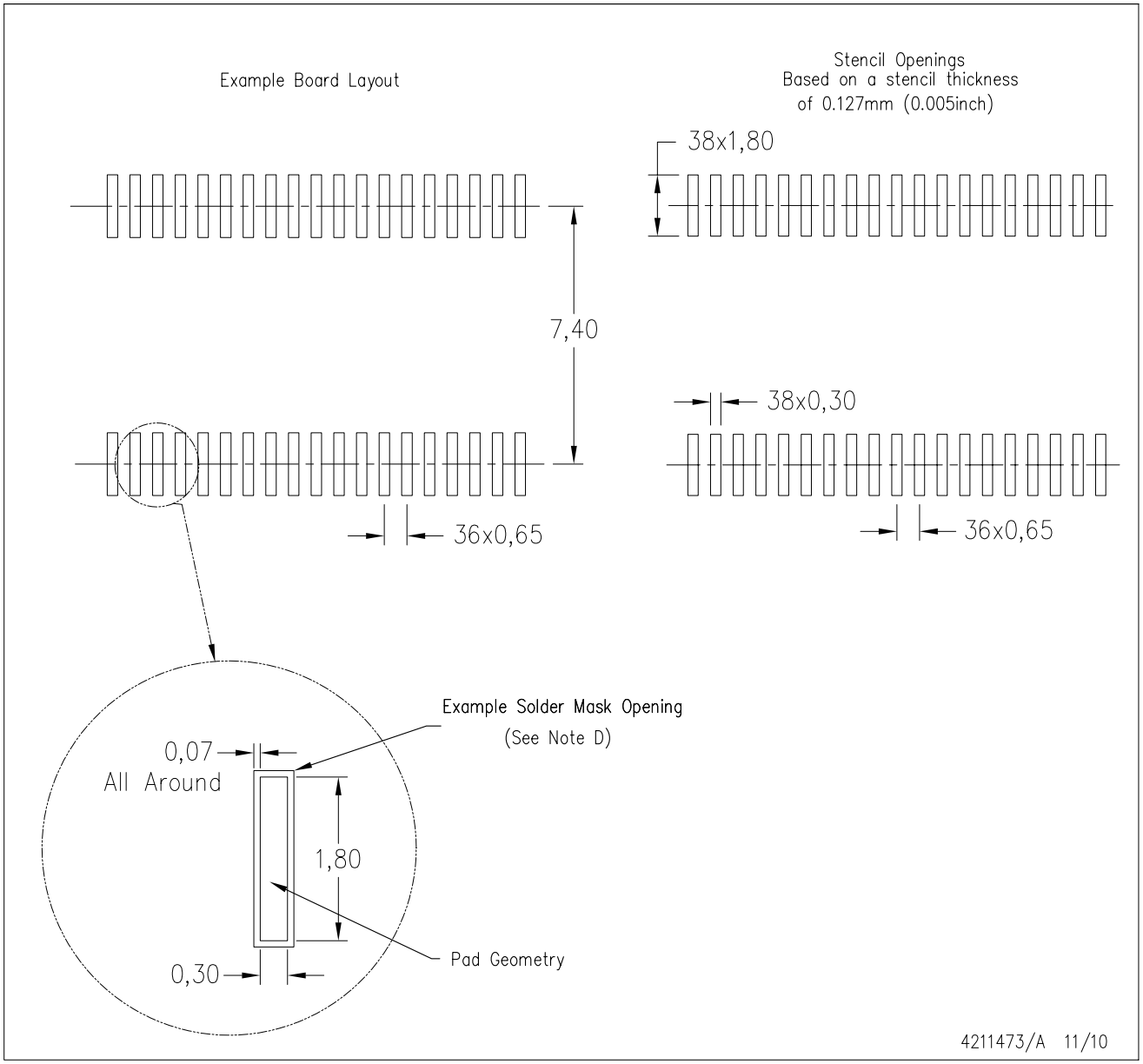


DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
D MO–153 Variation	DB–1	DC	DD–1

4040066/F 01/2009

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–153, except 30 pin body length.

DA (R-PDSO-G38) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
D. Contact the board fabrication site for recommended soldermask tolerances.

GENERIC PACKAGE VIEW

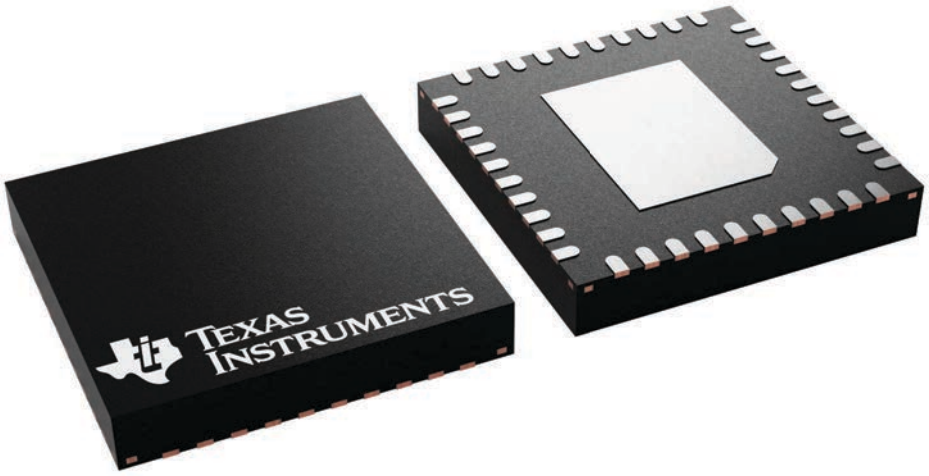
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



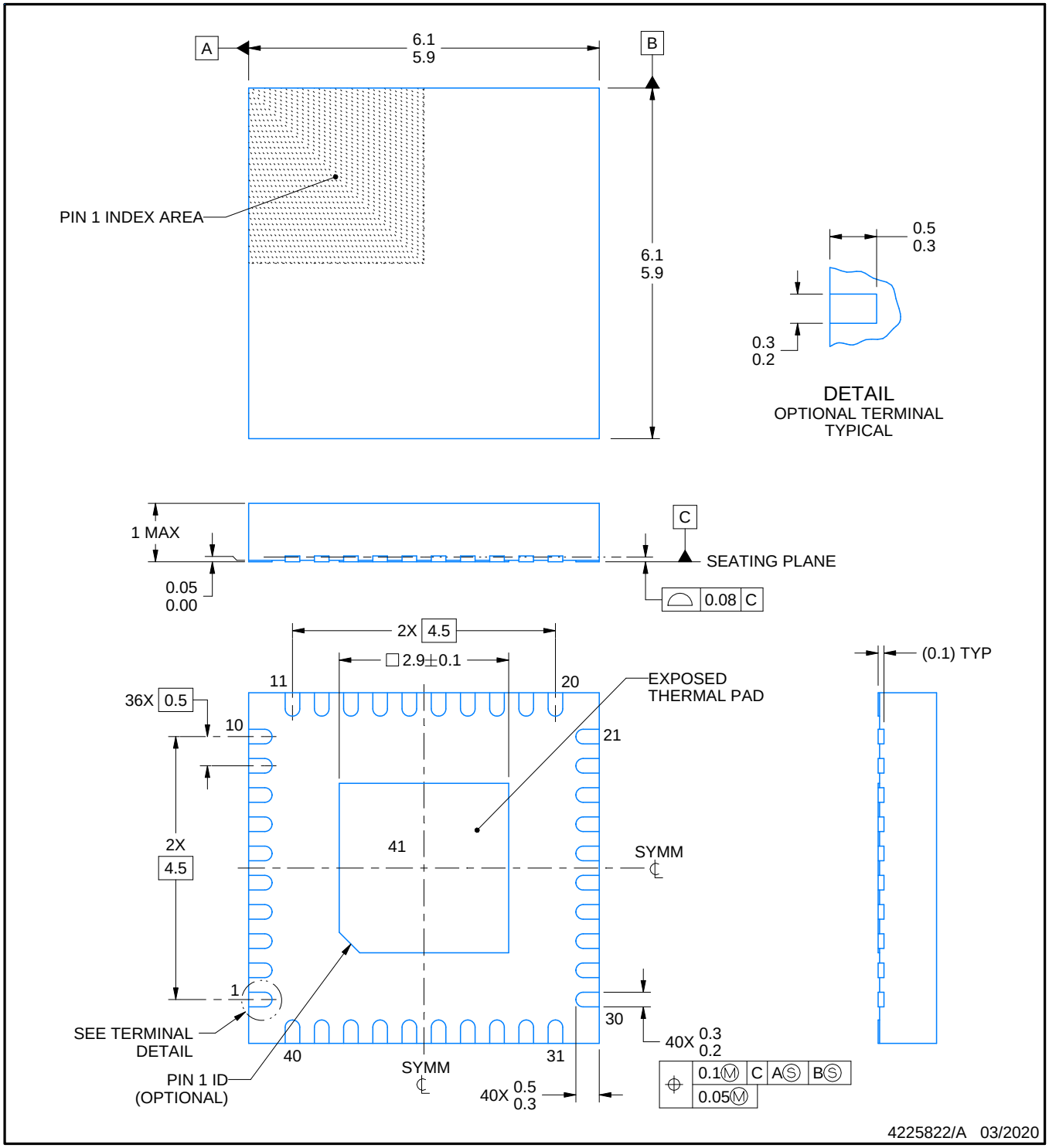
4225870/A

PACKAGE OUTLINE

RHA0040D

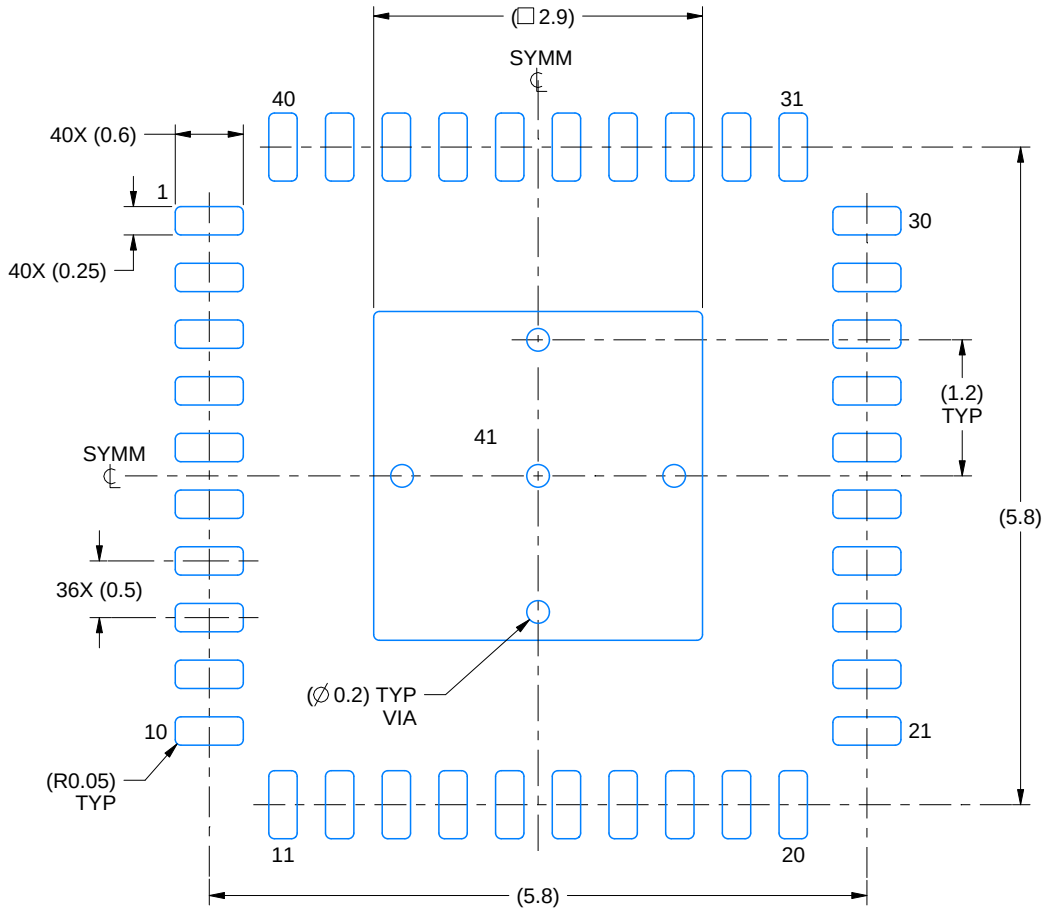
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

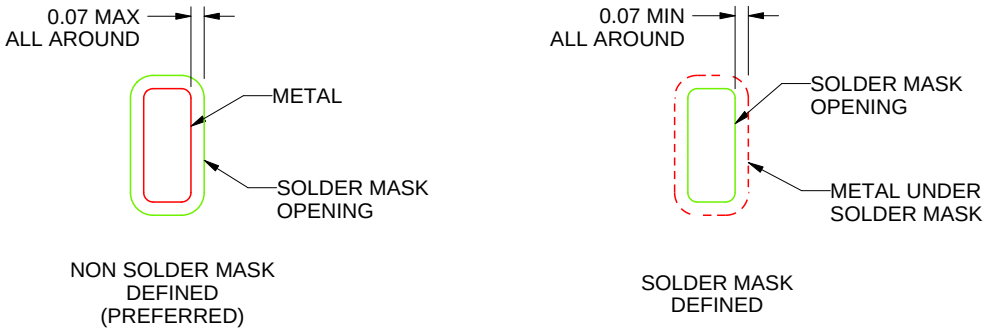


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

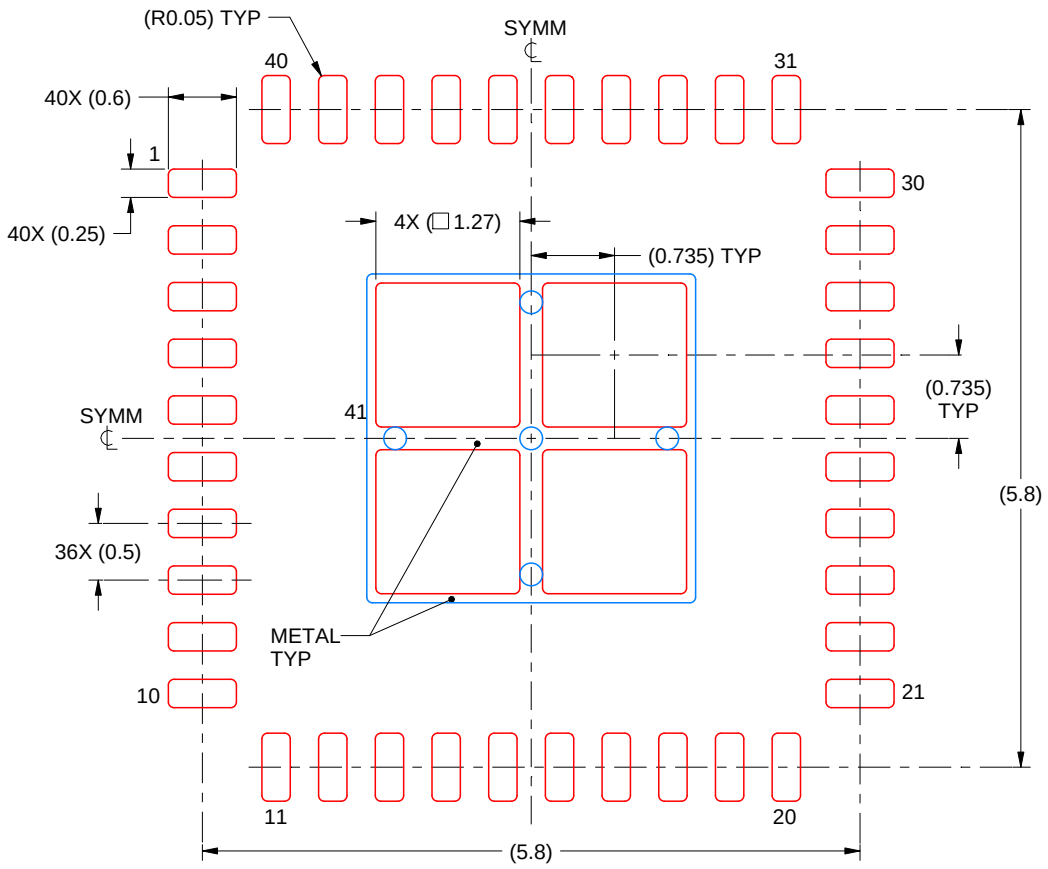


SOLDER MASK DETAILS

4225822/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

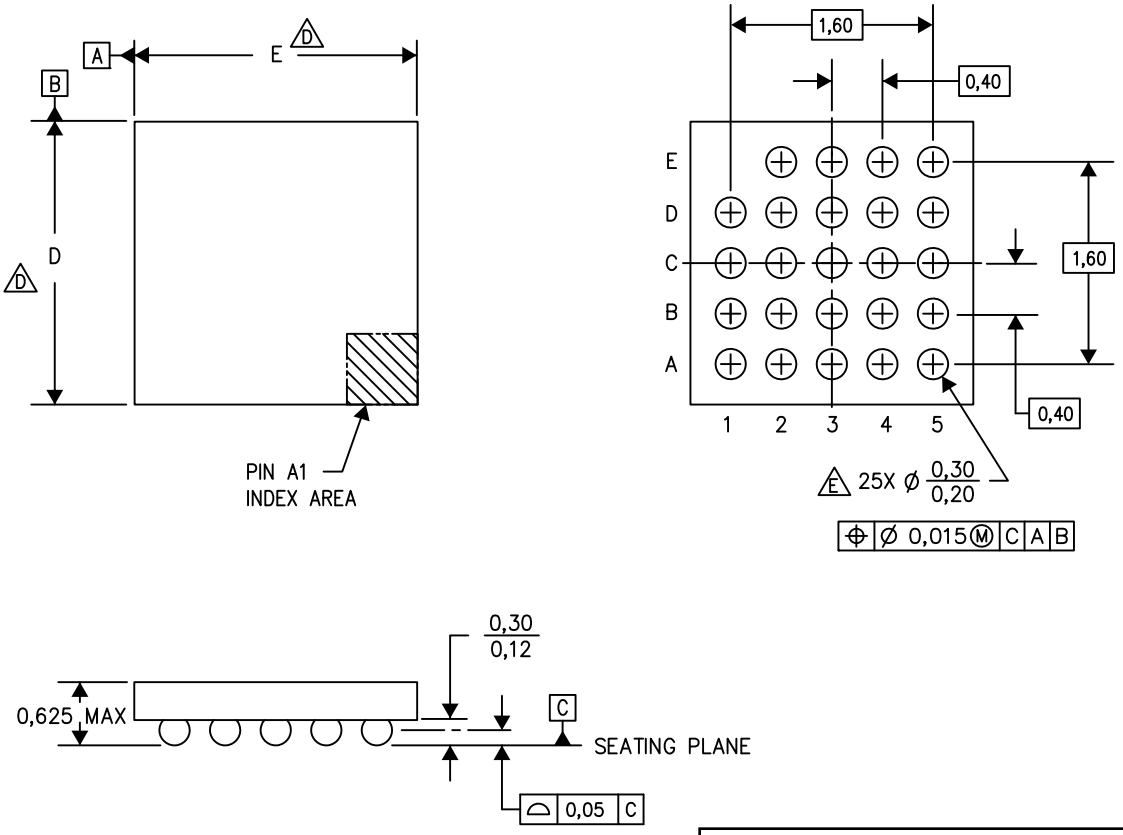
EXPOSED PAD 41:
76.46% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4225822/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YQD (S-XBGA-N24) DIE-SIZE BALL GRID ARRAY



D: Max = 2.271 mm, Min = 2.21 mm

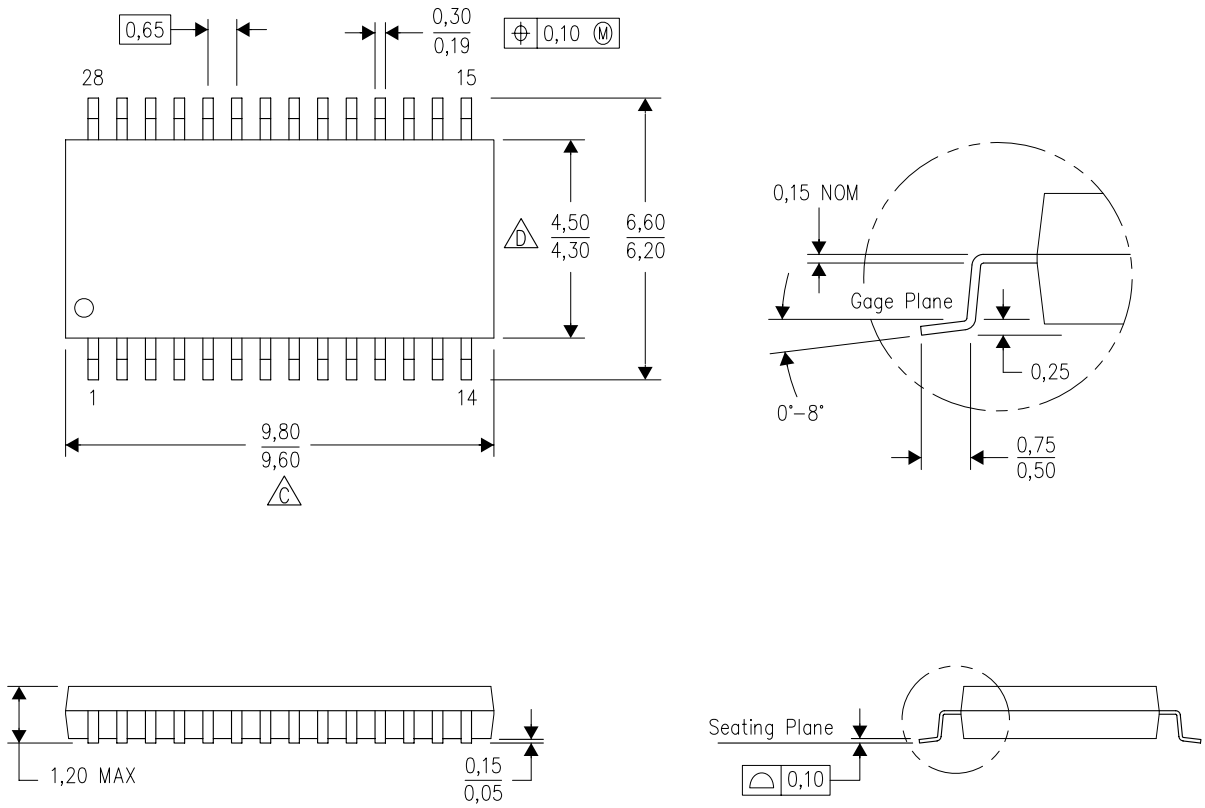
E: Max = 2.07 mm, Min = 2.01 mm

4218282/B 02/15

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. Reference Product Data Sheet for array population. 5 x 5 matrix pattern is shown for illustration only.
- F. This package contains Pb-free balls.

NanoFree is a trademark of Texas Instruments

PW (R-PDSO-G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

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