MSP430F5438A-ET 混合信号控制器

1 特性

- 工作温度版本 -ET 使用器件版本 **H**
- 低电源电压范围：
  3.6V 低至 1.8V
- 超低功耗
  - 激活模式 (AM)：
    所有系统时钟激活
    在 8MHz、3.0V 且闪存程序执行时为 230μA/MHz（典型值）
    在 8MHz、3.0V 且 RAM 程序执行时为 110μA/MHz（典型值）
  - 待机模式 (LPM3)：
    含晶体的实时时钟、看门狗、电源监控器可用、完全 RAM 保持、快速唤醒：
    2.2V 时为 1.7μA，3.0V 时为 2.1μA（典型值）
    低功耗振荡器 (VLO)，通用计数器，看门狗和电源监控器可用，完全 RAM 保持，快速唤醒：
    3.0V 时为 1.2μA（典型值）
  - 关闭模式 (LPM4)：
    完全 RAM 保持、电源监控器可用、快速唤醒：
    3.0V 时为 1.2μA（典型值）
  - 关断模式 (LPM4.5)：
    3.0V 时为 0.1μA（典型值）
- 3.5μs 内从待机模式唤醒（典型值）
- 16 位 RISC 架构
  - 扩展存储器
  - 高达 25MHz 系统时钟
- 灵活的电源管理系统
  - 具有可编程稳压内核电源电压的完全集成 LDO
  - 电源电压监控、监视和欠压保护
- 单一时钟系统
  - 针对频率稳定的锁相环 (FLL) 控制环路
  - 低功耗低频内部时钟源 (VLO)
  - 低频修整内部基准源 (REFO)
  - 32kHz 晶振
  - 高达 32MHz 的高频晶振 [1]
- 配有五个捕捉/比较寄存器的 16 位计时器 TA0，Timer_A
- 配有三个捕捉/比较寄存器的 16 位计时器 TA1，Timer_A
- 具有七个捕捉/比较影子寄存器的 16 位计时器 TB0，Timer_B
- 多达 4 个通用串行通信接口
  - USCI_A0、USCI_A1、USCI_A2 和 USCI_A3 均支持
    - 支持自动波特率检测功能的增强型 UART
    - 红外数据通讯 (IrDA) 编码器和解码器
    - 同步 SPI
  - USCI_B0、USCI_B1、USCI_B2 和 USCI_B3 均支持
    - I^2C
    - 同步 SPI
- 12 位模数转换器 (ADC)
  - 内部基准
  - 采样和保持功能
  - 自动扫描特性
  - 14 个外部通道，2 个内部通道
- 支持 32 位运算的硬件乘法器
- 串行板上编程，无需外部编程电压
- 3 通道内部 DMA
- 带有实时时钟特性的基本计时器
- 宽工作范围：-40°C 至 125°C（Q 级温度），-55°C 至 125°C（M 级温度）（某些标注的参数只是针对 -40°C 至 85°C 指定的）
- 可用的 SnAgCu (ZCA) 或 SnPb (GCA) 焊球材料

2 应用

- 支持国防、航天和医疗应用
  - 受控基线
  - 一个组装和测试基地
  - 一个制造基地
  - 在工作温度范围（-55°C 至 125°C）内可用
  - 延长了产品生命周期
  - 延长了产品变更通知
  - 产品可追溯性

[1] 对于 32kHz 和高频晶振，不能保证晶体在 85°C 以上使用晶振。

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

3 说明

MSP430F5438A-ET 是一款超低功耗微控制器。此架构与多种低功耗模式配合使用，经过优化，可在便携式测量应用中延长电池寿命。该器件具有一个强大的 16 位 RISC CPU、16 位寄存器和有助于实现出色编码效率的常数发生器。此数控振荡器 (DCO) 可在 3.5μs（典型值）内从低功率模式唤醒至激活模式。

MSP430F5438A-ET 是一种微控制器配置，具有三个 16 位计时器、一个高性能 12 位模数转换器 (ADC)、多达四个通用串行通信接口 (USCI)、一个硬件乘法器、一个 DMA、一个具有报警功能的实时时钟 (RTC) 模块和多达 87 个 I/O 引脚。有关完整的模块说明，请参阅 *MSP430F5xx 和 MSP430F6xx 系列用户指南*。

这个器件的典型应用包括模拟和数字传感器系统、数字电机控制、遥控、恒温器、数字计时器、手持仪表。

器件信息

器件型号 (1)	封装	封装尺寸 (2)
M430F5438AQZCARET	nFBGA (113)	7mm × 7mm
M430F5438AMZCARET	nFBGA (113)	7mm × 7mm
M430F5438AQGCARET	nFBGA (113)	7mm × 7mm
M430F5438AMGCARET	nFBGA (113)	7mm × 7mm
M430F5438AQZQWRET(3)	MicroStar Junior™ BGA (113)	7mm × 7mm

(1) 要获得新的器件、封装和订购信息，请参阅*封装选项附录*（在机械、封装和可订购信息中），或者访问 TI 网站 www.ti.com。
(2) 这里显示的尺寸为近似值。有关容差的封装尺寸，请参阅*机械数据*（在机械、封装和可订购信息中）。
(3) 采用 ZQW (MicroStar Junior BGA) 封装的所有可订购器件型号均已更改为最后可采购期限的状态。有关此状态的详细信息，请访问产品生命周期页面。

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4 功能方框图

图 4-1 展示了功能方框图。

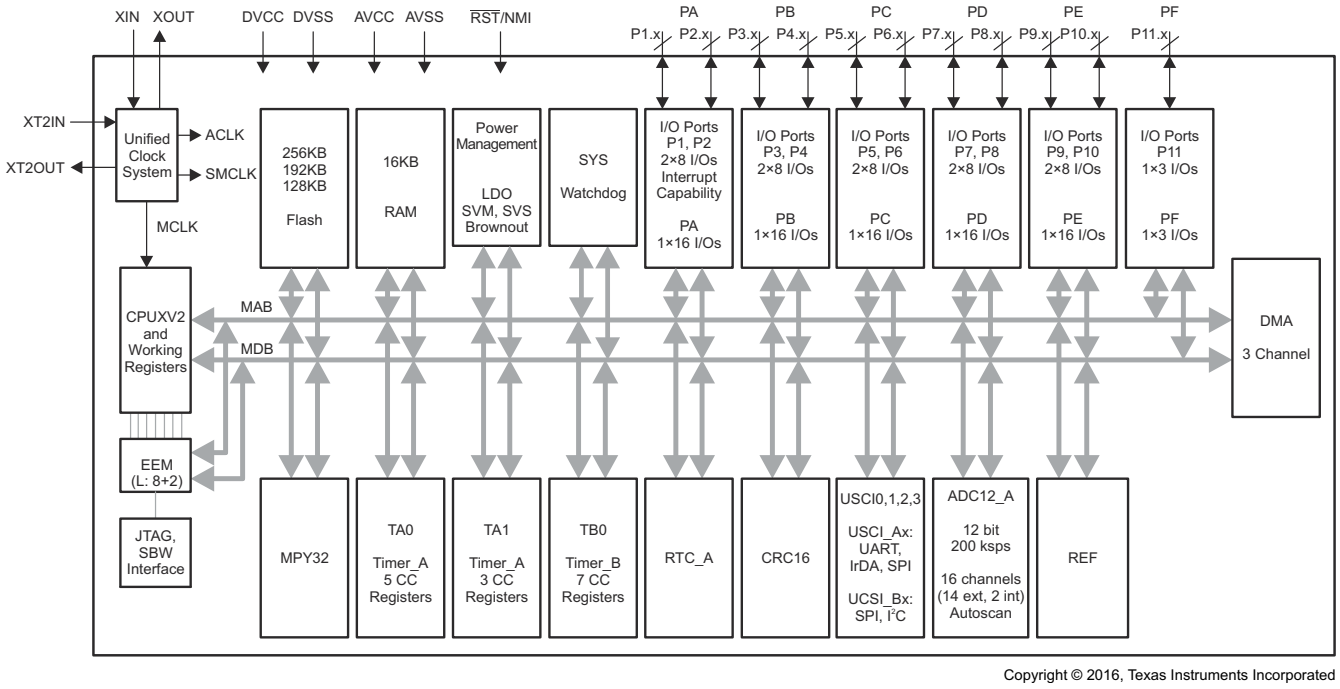

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图 4-1. MSP430F5438-ET 功能方框图

Table of Contents

1 特性 1
2 应用 1
3 说明 2
4 功能方框图 3
5 Revision History 4
6 Terminal Configuration and Functions 5
6.1 Pin Diagram 5
6.2 Signal Descriptions 5
7 Specifications 11
7.1 Absolute Maximum Ratings 11
7.2 Recommended Operating Conditions 12
7.3 Active Mode Supply Current Into V_{CC} Excluding External Current 13
7.4 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current 13
7.5 Thermal Resistance Characteristics 14
7.6 Schmitt-Trigger Inputs – General Purpose I/O 14
7.7 Inputs – Ports P1 and P2 14
7.8 Leakage Current – General Purpose I/O 15
7.9 Outputs – General Purpose I/O (Full Drive Strength) 15
7.10 Outputs – General Purpose I/O (Reduced Drive Strength) 15
7.11 Output Frequency – General Purpose I/O 16
7.12 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0) 16
7.13 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1) 17
7.14 Crystal Oscillator, XT1, Low-Frequency Mode 18
7.15 Crystal Oscillator, XT1, High-Frequency Mode 19
7.16 Crystal Oscillator, XT2 21
7.17 Internal Very-Low-Power Low-Frequency Oscillator (VLO) 22
7.18 Internal Reference, Low-Frequency Oscillator (REFO) 22
7.19 DCO Frequency 22
7.20 PMM, Brownout Reset (BOR) 24
7.21 PMM, Core Voltage 24
7.22 PMM, SVS High Side 24
7.23 PMM, SVM High Side 25
7.24 PMM, SVS Low Side 26
7.25 PMM, SVM Low Side 26
7.26 Wakeup From Low-Power Modes and Reset 26
7.27 Timer_A 27
7.28 Timer_B 27
7.29 USCI (UART Mode) Recommended Operating Conditions 27
7.30 USCI (UART Mode) 27
7.31 USCI (SPI Master Mode) Recommended Operating Conditions 27
7.32 USCI (SPI Master Mode) 28
7.33 USCI (SPI Slave Mode) 30
7.34 USCI (I^2C Mode) 32
7.35 12-Bit ADC, Power Supply and Input Range Conditions 33
7.36 12-Bit ADC, Timing Parameters 33
7.37 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage 34
7.38 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage 34
7.39 12-Bit ADC, Temperature Sensor and Built-In V_{MID} 35
7.40 REF, External Reference 35
7.41 REF, Built-In Reference 36
7.42 Flash Memory 37
7.43 JTAG and Spy-Bi-Wire Interface 37
8 Detailed Description 38
8.1 CPU 38
8.2 Operating Modes 39
8.3 Interrupt Vector Addresses 40
8.4 Memory Organization 41
8.5 Bootloader (BSL) 42
8.6 JTAG Operation 42
8.7 Flash Memory 43
8.8 RAM Memory 43
8.9 Peripherals 43
8.10 Device Descriptors (TLV) 86
9 Device and Documentation Support 89
9.1 Trademarks 89
9.2 静电放电警告 89
9.3 支持资源 89
9.4 术语表 89

5 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (October 2019) to Revision A (February 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 添加了 nFBGA (ZCA 和 GCA) 封装的信息；添加了有关 MicroStar Junior BGA (ZQW) 封装状态的注释	1

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6 Terminal Configuration and Functions

6.1 Pin Diagram

图 6-1 shows the pinout for the 113-pin ZCA, GCA, and ZQW packages. Only the default signal names are shown here; for all multiplexed signals, see 节 6.2.

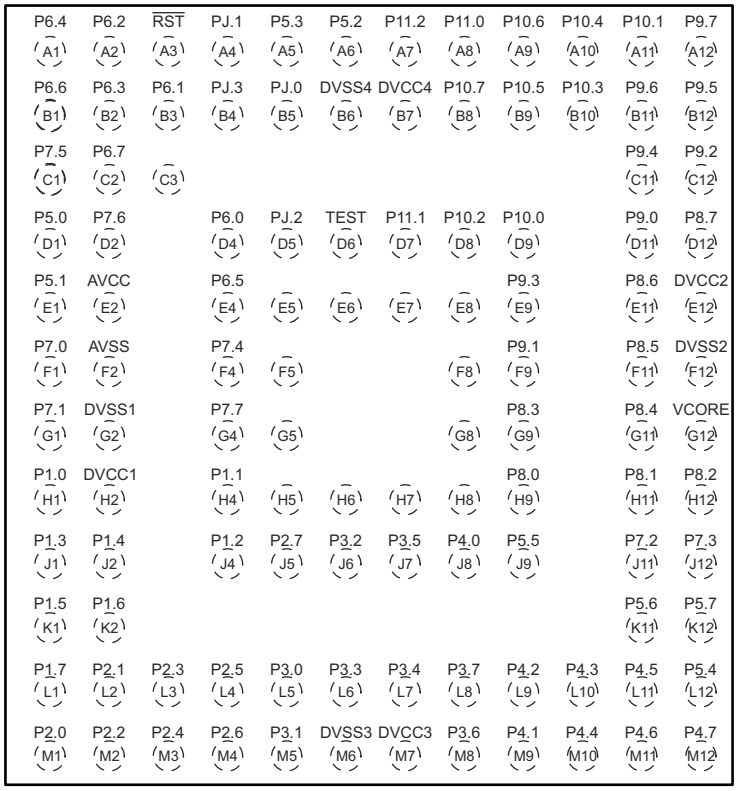

图 6-1. 113-Pin ZCA, GCA or ZQW Package (Top View)

6.2 Signal Descriptions

表 6-1 describes the signals.

表 6-1. Signal Descriptions

SIGNAL NAME	NO.	I/O	DESCRIPTION
P6.4/A4	A1	I/O	General-purpose digital I/O Analog input A4 – ADC
P6.5/A5	E4	I/O	General-purpose digital I/O Analog input A5 – ADC
P6.6/A6	B1	I/O	General-purpose digital I/O Analog input A6 – ADC
P6.7/A7	C2	I/O	General-purpose digital I/O Analog input A7 – ADC
P7.4/A12	F4	I/O	General-purpose digital I/O Analog input A12 – ADC
P7.5/A13	C1	I/O	General-purpose digital I/O Analog input A13 – ADC
P7.6/A14	D2	I/O	General-purpose digital I/O Analog input A14 – ADC
P7.7/A15	G4	I/O	General-purpose digital I/O Analog input A15 – ADC

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表 6-1. Signal Descriptions (continued)

SIGNAL NAME	NO.	I/O	DESCRIPTION
P5.0/A8/VREF+/VeREF+	D1	I/O	General-purpose digital I/O Analog input A8 – ADC Output of reference voltage to the ADC Input for an external reference voltage to the ADC
P5.1/A9/VREF-/VeREF-	E1	I/O	General-purpose digital I/O Analog input A9 – ADC Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
AVCC	E2		Analog power supply
AVSS	F2		Analog ground supply
P7.0/XIN	F1	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
P7.1/XOUT	G1	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
DVSS1	G2		Digital ground supply
DVCC1	H2		Digital power supply
P1.0/TA0CLK/ACLK	H1	I/O	General-purpose digital I/O with port interrupt TA0 clock signal TACLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P1.1/TA0.0	H4	I/O	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	J4	I/O	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input
P1.3/TA0.2	J1	I/O	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3	J2	I/O	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4	K1	I/O	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/SMCLK	K2	I/O	General-purpose digital I/O with port interrupt SMCLK output
P1.7	L1	I/O	General-purpose digital I/O with port interrupt
P2.0/TA1CLK/MCLK	M1	I/O	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input MCLK output
P2.1/TA1.0	L2	I/O	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output
P2.2/TA1.1	M2	I/O	General-purpose digital I/O with port interrupt TA1 CCR1 capture: CCI1A input, compare: Out1 output
P2.3/TA1.2	L3	I/O	General-purpose digital I/O with port interrupt TA1 CCR2 capture: CCI2A input, compare: Out2 output
P2.4/RTCCLK	M3	I/O	General-purpose digital I/O with port interrupt RTCCLK output
P2.5	L4	I/O	General-purpose digital I/O with port interrupt
P2.6/ACLK	M4	I/O	General-purpose digital I/O with port interrupt ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P2.7/ADC12CLK/DMAE0	J5	I/O	General-purpose digital I/O with port interrupt Conversion clock output ADC DMA external trigger input

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表 6-1. Signal Descriptions (continued)

SIGNAL NAME	NO.	I/O	DESCRIPTION
P3.0/UCB0STE/UCA0CLK	L5	I/O	General-purpose digital I/O Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode
P3.1/UCB0SIMO/UCB0SDA	M5	I/O	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I2C data – USCI_B0 I2C mode
P3.2/UCB0SOMI/UCB0SCL	J6	I/O	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I2C clock – USCI_B0 I2C mode
P3.3/UCB0CLK/UCA0STE	L6	I/O	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode
DVSS3	M6		Digital ground supply
DVCC3	M7		Digital power supply
P3.4/UCA0TXD/UCA0SIMO	L7	I/O	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode
P3.5/UCA0RXD/UCA0SOMI	J7	I/O	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode
P3.6/UCB1STE/UCA1CLK	M8	I/O	General-purpose digital I/O Slave transmit enable – USCI_B1 SPI mode Clock signal input – USCI_A1 SPI slave mode Clock signal output – USCI_A1 SPI master mode
P3.7/UCB1SIMO/UCB1SDA	L8	I/O	General-purpose digital I/O Slave in, master out – USCI_B1 SPI mode I2C data – USCI_B1 I2C mode
P4.0/TB0.0	J8	I/O	General-purpose digital I/O TB0 capture CCR0: CCI0A/CCI0B input, compare: Out0 output
P4.1/TB0.1	M9	I/O	General-purpose digital I/O TB0 capture CCR1: CCI1A/CCI1B input, compare: Out1 output
P4.2/TB0.2	L9	I/O	General-purpose digital I/O TB0 capture CCR2: CCI2A/CCI2B input, compare: Out2 output
P4.3/TB0.3	L10	I/O	General-purpose digital I/O TB0 capture CCR3: CCI3A/CCI3B input, compare: Out3 output
P4.4/TB0.4	M10	I/O	General-purpose digital I/O TB0 capture CCR4: CCI4A/CCI4B input, compare: Out4 output
P4.5/TB0.5	L11	I/O	General-purpose digital I/O TB0 capture CCR5: CCI5A/CCI5B input, compare: Out5 output
P4.6/TB0.6	M11	I/O	General-purpose digital I/O TB0 capture CCR6: CCI6A/CCI6B input, compare: Out6 output
P4.7/TB0CLK/SMCLK	M12	I/O	General-purpose digital I/O TB0 clock input SMCLK output
P5.4/UCB1SOMI/UCB1SCL	L12	I/O	General-purpose digital I/O Slave out, master in – USCI_B1 SPI mode I2C clock – USCI_B1 I2C mode
P5.5/UCB1CLK/UCA1STE	J9	I/O	General-purpose digital I/O Clock signal input – USCI_B1 SPI slave mode Clock signal output – USCI_B1 SPI master mode Slave transmit enable – USCI_A1 SPI mode

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表 6-1. Signal Descriptions (continued)

SIGNAL NAME	NO.	I/O	DESCRIPTION
P5.6/UCA1TXD/UCA1SIMO	K11	I/O	General-purpose digital I/O Transmit data – USCI_A1 UART mode Slave in, master out – USCI_A1 SPI mode
P5.7/UCA1RXD/UCA1SOMI	K12	I/O	General-purpose digital I/O Receive data – USCI_A1 UART mode Slave out, master in – USCI_A1 SPI mode
P7.2/TB0OUTH/SVMOUT	J11	I/O	General-purpose digital I/O Switch all PWM outputs high impedance – Timer TB0 SVM output
P7.3/TA1.2	J12	I/O	General-purpose digital I/O TA1 CCR2 capture: CCI2B input, compare: Out2 output
P8.0/TA0.0	H9	I/O	General-purpose digital I/O TA0 CCR0 capture: CCI0B input, compare: Out0 output
P8.1/TA0.1	H11	I/O	General-purpose digital I/O TA0 CCR1 capture: CCI1B input, compare: Out1 output
P8.2/TA0.2	H12	I/O	General-purpose digital I/O TA0 CCR2 capture: CCI2B input, compare: Out2 output
P8.3/TA0.3	G9	I/O	General-purpose digital I/O TA0 CCR3 capture: CCI3B input, compare: Out3 output
P8.4/TA0.4	G11	I/O	General-purpose digital I/O TA0 CCR4 capture: CCI4B input, compare: Out4 output
VCORE(2)	G12		Regulated core power supply output (internal use only, no external current loading)
DVSS2	F12		Digital ground supply
DVCC2	E12		Digital power supply
P8.5/TA1.0	F11	I/O	General-purpose digital I/O TA1 CCR0 capture: CCI0B input, compare: Out0 output
P8.6/TA1.1	E11	I/O	General-purpose digital I/O TA1 CCR1 capture: CCI1B input, compare: Out1 output
P8.7	D12	I/O	General-purpose digital I/O
P9.0/UCB2STE/UCA2CLK	D11	I/O	General-purpose digital I/O Slave transmit enable – USCI_B2 SPI mode Clock signal input – USCI_A2 SPI slave mode Clock signal output – USCI_A2 SPI master mode
P9.1/UCB2SIMO/UCB2SDA	F9	I/O	General-purpose digital I/O Slave in, master out – USCI_B2 SPI mode I2C data – USCI_B2 I2C mode
P9.2/UCB2SOMI/UCB2SCL	C12	I/O	General-purpose digital I/O Slave out, master in – USCI_B2 SPI mode I2C clock – USCI_B2 I2C mode
P9.3/UCB2CLK/UCA2STE	E9	I/O	General-purpose digital I/O Clock signal input – USCI_B2 SPI slave mode Clock signal output – USCI_B2 SPI master mode Slave transmit enable – USCI_A2 SPI mode
P9.4/UCA2TXD/UCA2SIMO	C11	I/O	General-purpose digital I/O Transmit data – USCI_A2 UART mode Slave in, master out – USCI_A2 SPI mode
P9.5/UCA2RXD/UCA2SOMI	B12	I/O	General-purpose digital I/O Receive data – USCI_A2 UART mode Slave out, master in – USCI_A2 SPI mode
P9.6	B11	I/O	General-purpose digital I/O
P9.7	A12	I/O	General-purpose digital I/O

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表 6-1. Signal Descriptions (continued)

SIGNAL NAME	NO.	I/O	DESCRIPTION
P10.0/UCB3STE/UCA3CLK	D9	I/O	General-purpose digital I/O Slave transmit enable – USCI_B3 SPI mode Clock signal input – USCI_A3 SPI slave mode Clock signal output – USCI_A3 SPI master mode
P10.1/UCB3SIMO/UCB3SDA	A11	I/O	General-purpose digital I/O Slave in, master out – USCI_B3 SPI mode I2C data – USCI_B3 I2C mode
P10.2/UCB3SOMI/UCB3SCL	D8	I/O	General-purpose digital I/O Slave out, master in – USCI_B3 SPI mode I2C clock – USCI_B3 I2C mode
P10.3/UCB3CLK/UCA3STE	B10	I/O	General-purpose digital I/O Clock signal input – USCI_B3 SPI slave mode Clock signal output – USCI_B3 SPI master mode Slave transmit enable – USCI_A3 SPI mode
P10.4/UCA3TXD/UCA3SIMO	A10	I/O	General-purpose digital I/O Transmit data – USCI_A3 UART mode Slave in, master out – USCI_A3 SPI mode
P10.5/UCA3RXD/UCA3SOMI	B9	I/O	General-purpose digital I/O Receive data – USCI_A3 UART mode Slave out, master in – USCI_A3 SPI mode
P10.6	A9	I/O	General-purpose digital I/O
P10.7	B8	I/O	General-purpose digital I/O
P11.0/ACLK	A8	I/O	General-purpose digital I/O ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P11.1/MCLK	D7	I/O	General-purpose digital I/O MCLK output
P11.2/SMCLK	A7	I/O	General-purpose digital I/O SMCLK output
DVCC4	B7		Digital power supply
DVSS4	B6		Digital ground supply
P5.2/XT2IN	A6	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P5.3/XT2OUT	A5	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTCK(3)	D6	I	Test mode pin – Selects four wire JTAG operation. Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated
PJ.0/TDO(4)	B5	I/O	General-purpose digital I/O JTAG test data output port
PJ.1/TDI/TCLK(4)	A4	I/O	General-purpose digital I/O JTAG test data input or test clock input
PJ.2/TMS(4)	D5	I/O	General-purpose digital I/O JTAG test mode select
PJ.3/TCK(4)	B4	I/O	General-purpose digital I/O JTAG test clock
$\overline{\text{RST}}$/NMI/SBWTDIO(3)	A3	I/O	Reset input active low Non-maskable interrupt input Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated.
P6.0/A0	D4	I/O	General-purpose digital I/O Analog input A0 – ADC
P6.1/A1	B3	I/O	General-purpose digital I/O Analog input A1 – ADC
P6.2/A2	A2	I/O	General-purpose digital I/O Analog input A2 – ADC

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表 6-1. Signal Descriptions (continued)

SIGNAL NAME	NO.	I/O	DESCRIPTION
P6.3/A3	B2	I/O	General-purpose digital I/O Analog input A3 – ADC
Reserved	(1)		

(1) C3, E5, E6, E7, E8, F5, F8, G5, G8, H5, H6, H7, H8 are reserved and should be connected to ground.
(2) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.
(3) See 节 8.5 and 节 8.6 for use with BSL and JTAG functions, respectively.
(4) See 节 6.2 for use with JTAG function.

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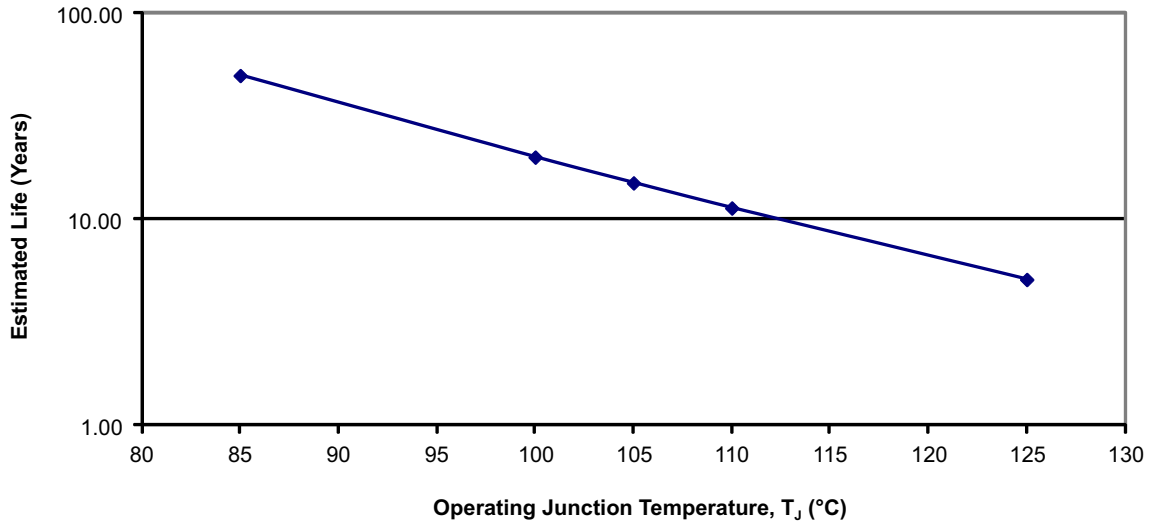
7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

Voltage applied at V_{CC} to V_{SS}	– 0.3 V to 4.1 V
Voltage applied to any pin (excluding VCORE) (2)	– 0.3 V to V_{CC} + 0.3 V
Diode current at any device pin	±2 mA
Storage temperature range, T_{stg} (3)	– 55°C to 125°C
Maximum junction temperature, T_J	125°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. VCORE is for internal device use only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.



A. See data sheet for absolute maximum and minimum recommended operating conditions.
B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

图 7-1. Electromigration Fail Mode Derating Chart

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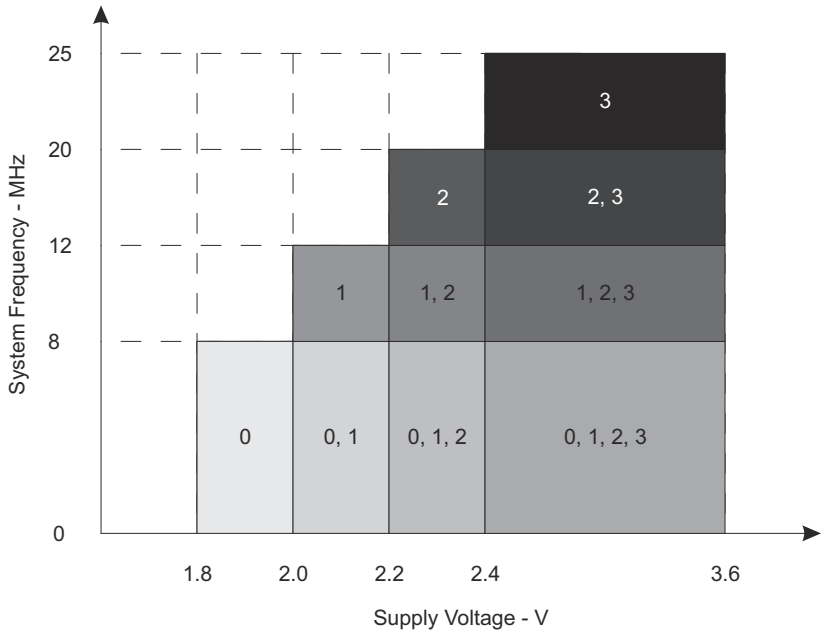
7.2 Recommended Operating Conditions

typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming (AV_{CC} = $DV_{CC1/2/3/4}$ = DV_{CC}) (1) (2)		1.8		3.6	V
V_{SS}	Supply voltage (AV_{SS} = $DV_{SS1/2/3/4}$ = DV_{SS})			0		V
T_A	Operating free-air temperature	Q temperature	-40		125	°C
		M temperature	-55		125	
T_J	Operating junction temperature	Q temperature	-40		125	°C
		M temperature	-55		125	
C_{VCORE}	Recommended capacitor at VCORE			470		nF
C_{DVCC}/ C_{VCORE}	Capacitor ratio of DVCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency) (3) (4) (see 图 7-2)	PMMCOREVx = 0, 1.8 V ⩽ V_{CC} ⩽ 3.6 V	0		8.0	MHz
		PMMCOREVx = 1, 2.0 V ⩽ V_{CC} ⩽ 3.6 V	0		12.0	
		PMMCOREVx = 2, 2.2 V ⩽ V_{CC} ⩽ 3.6 V	0		20.0	
		PMMCOREVx = 3, 2.4 V ⩽ V_{CC} ⩽ 3.6 V	0		25.0	

(1) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the SVS threshold parameters for the exact values and further details.
(3) The MSP430 CPU is clocked directly with MCLK. Both the high and low phases of MCLK must not exceed the pulse duration of the specified maximum frequency.
(4) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

图 7-2. Frequency vs Supply Voltage

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7.3 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3)

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)										UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, Flash}$	Flash	3.0 V	0	0.29	0.45	2.08	2.30							mA
			1	0.32		2.08		3.10						
			2	0.33		2.24		3.50		6.37				
			3	0.35		2.36		3.70		6.75		8.90	14	
$I_{AM, RAM}$	RAM	3.0 V	0	0.17	0.30	0.90	1.10							mA
			1	0.18		1.00		1.47						
			2	0.19		1.13		1.68		2.82				
			3	0.20		1.20		1.78		3.00		4.50	8	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing.
$f_{ACLK} = 32768$ Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.

7.4 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		V_{CC}	PMMCOREVx	-55°C		-40°C		25°C		125°C		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0(3) (9)	2.2 V	0	69	93	69	93	69	93	85	150	µA
		3.0 V	3	73	100	73	100	73	100	90	150	
I_{LPM2}	Low-power mode 2(4) (9)	2.2 V	0	11	15.5	11	15.5	11	15.5	12.5	30	µA
		3.0 V	3	11.7	17.5	11.7	17.5	11.7	17.5	12.5	34	
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(5) (9)	2.2 V	0	1.4		1.4		1.7		8.5		µA
			1	1.5		1.5		1.8		9.9		
			2	1.5		1.5		2.0		10.1		
		3.0 V	0	1.8		1.8		2.1	2.4	7.1	21	
			1	1.8		1.8		2.3		10.5		
			2	1.9		1.9		2.4		10.6		
			3	2.0		2.0		2.3	2.6	11.8	34	
$I_{LPM3,VLO}$	Low-power mode 3, VLO mode(6) (9)	3.0 V	0	1.0		1.0		1.2	1.42	7.5	32	µA
			1	1.0		1.0		1.3		8		
			2	1.1		1.1		1.4		8.5		
			3	1.2		1.2		1.4	1.62	8.5	32	
I_{LPM4}	Low-power mode 4(7) (9)	3.0 V	0	1.1		1.1		1.2	1.35	7.5	30	µA
			1	1.2		1.2		1.2		8		
			2	1.3		1.3		1.3		8.5		
			3	1.3		1.3		1.3	1.52	8.5	32	
$I_{LPM4.5}$	Low-power mode 4.5(8)	3.0 V		0.10		0.10		0.10	0.16	0.75	5	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).

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CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz

(4) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.

(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz

(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{VLO}, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz

(7) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

(8) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

(9) Current for brownout, high side supervisor (SVS_H) normal mode included. Low side supervisor and monitors disabled (SVS_L, SVM_L). High side monitor disabled (SVM_H). RAM retention enabled.

7.5 Thermal Resistance Characteristics

THERMAL METRIC(1) (2)		MSP430F5438A-ET			UNIT
		ZCA	GCA	ZQW	
		113 PINS			
θ_{JA}	Junction-to-ambient thermal resistance	36.2		43.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	13.5		16.6	
θ_{JB}	Junction-to-board thermal resistance	14.5		17.8	
ψ_{JT}	Junction-to-top characterization parameter	0.3		0.3	
ψ_{JB}	Junction-to-board characterization parameter	14.3		15.1	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

7.6 Schmitt-Trigger Inputs – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.75		1.45	V
			3 V	1.45		2.15	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.40		1.05	V
			3 V	0.70		1.7	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		1.8 V	0.25		0.9	V
			3 V	0.35		1.05	
R_{Pull}	Pullup or pulldown resistor(2)	For pullup: V_{IN} = V_{SS} For pulldown: V_{IN} = V_{CC}		21	35	51	kΩ
C_I	Input capacitance	V_{IN} = V_{SS} or V_{CC}			5		pF

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

(2) Also applies to the $\overline{RST}$ pin when the pullup or pulldown resistor is enabled.

7.7 Inputs – Ports P1 and P2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing(2)	Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag	2.2 V, 3 V		20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

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7.8 Leakage Current – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	(1) (2)	1.8 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

7.9 Outputs – General Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA(1)	1.8 V	V_{CC} – 0.35	V_{CC}	V
		$I_{(OHmax)}$ = –10 mA(2)		V_{CC} – 0.70	V_{CC}	
		$I_{(OHmax)}$ = –5 mA(1)	3 V	V_{CC} – 0.35	V_{CC}	
		$I_{(OHmax)}$ = –15 mA(2)		V_{CC} – 0.70	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA(1)	1.8 V	V_{SS}	V_{SS} + 0.35	V
		$I_{(OLmax)}$ = 10 mA(2)		V_{SS}	V_{SS} + 0.70	
		$I_{(OLmax)}$ = 5 mA(1)	3 V	V_{SS}	V_{SS} + 0.35	
		$I_{(OLmax)}$ = 15 mA(2)		V_{SS}	V_{SS} + 0.70	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

7.10 Outputs – General Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA(1)	1.8 V	V_{CC} – 0.35	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA(2)		V_{CC} – 0.70	V_{CC}	
		$I_{(OHmax)}$ = –2 mA(1)	3.0 V	V_{CC} – 0.35	V_{CC}	
		$I_{(OHmax)}$ = –6 mA(2)		V_{CC} – 0.70	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(1)	1.8 V	V_{SS}	V_{SS} + 0.35	V
		$I_{(OLmax)}$ = 3 mA(2)		V_{SS}	V_{SS} + 0.70	
		$I_{(OLmax)}$ = 2 mA(1)	3.0 V	V_{SS}	V_{SS} + 0.35	
		$I_{(OLmax)}$ = 6 mA(2)		V_{SS}	V_{SS} + 0.70	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.
(3) Selecting reduced drive strength may reduce EMI.

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7.11 Output Frequency – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.6/SMCLK (1) (2)	V_{CC} = 1.8 V, PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V, PMMCOREVx = 3		25	
f_{Port_CLK}	Clock output frequency	P1.0/TA0CLK/ACLK P1.6/SMCLK P2.0/TA1CLK/MCLK C_L = 20 pF(2)	V_{CC} = 1.8 V, PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V, PMMCOREVx = 3		25	

(1) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

7.12 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

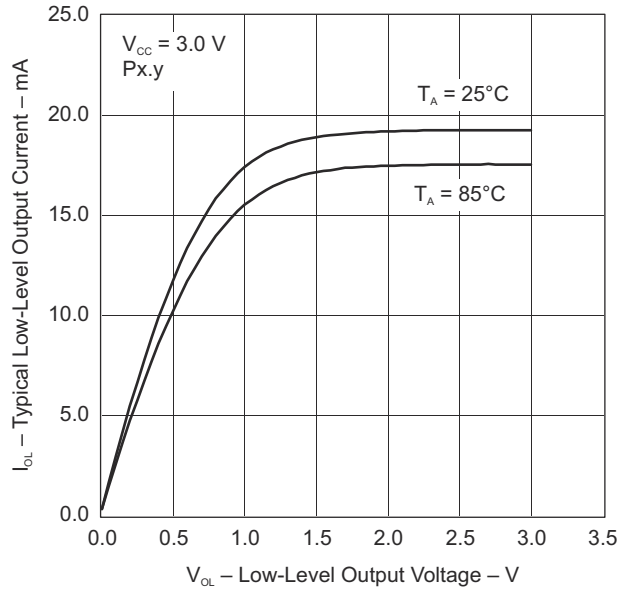

图 7-3. Typical Low-Level Output Current vs Low-Level Output Voltage

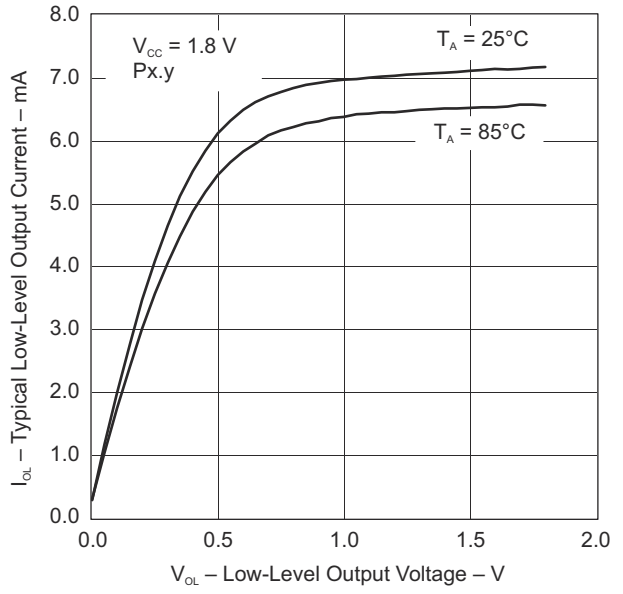

图 7-4. Typical Low-Level Output Current vs Low-Level Output Voltage

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7.12 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0) (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

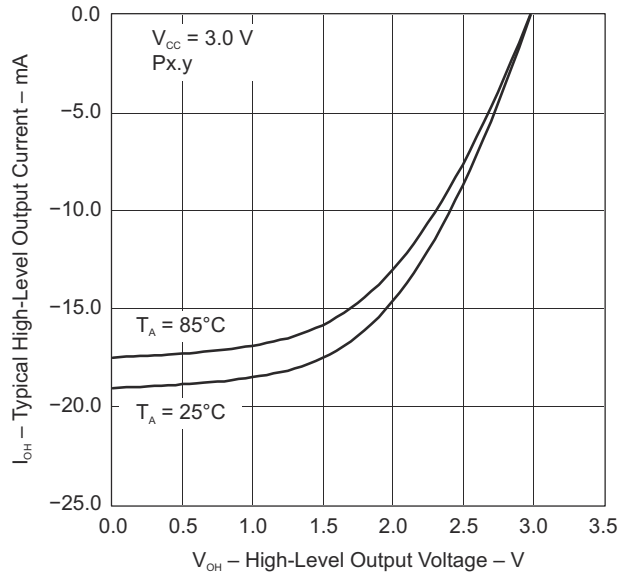

图 7-5. Typical High-Level Output Current vs High-Level Output Voltage

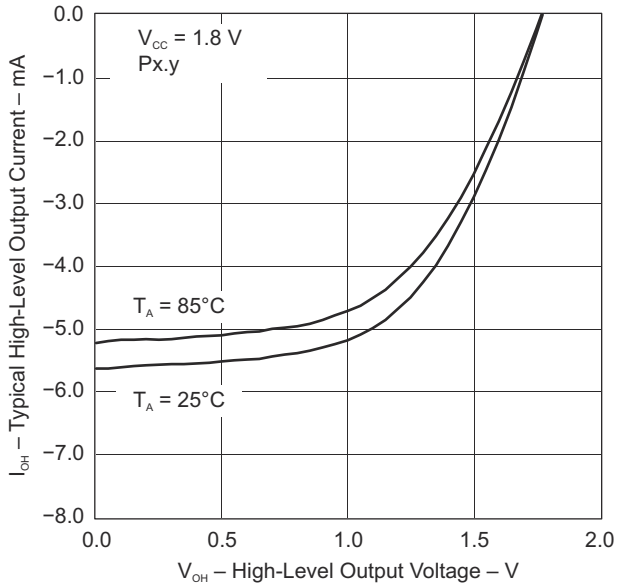

图 7-6. Typical High-Level Output Current vs High-Level Output Voltage

7.13 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

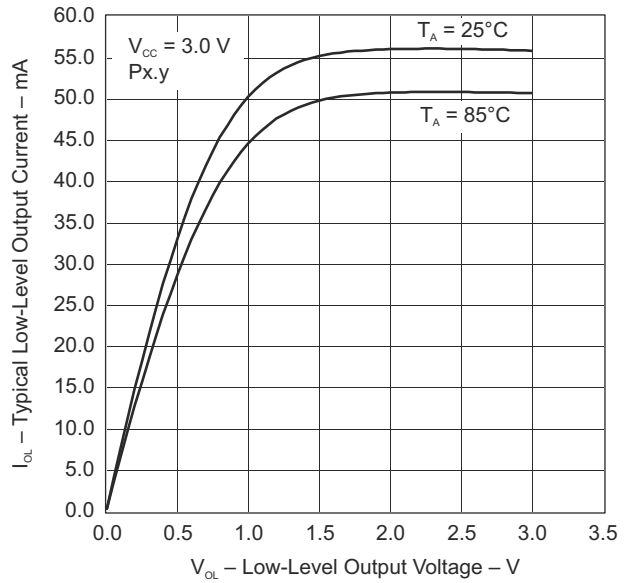

图 7-7. Typical Low-Level Output Current vs Low-Level Output Voltage

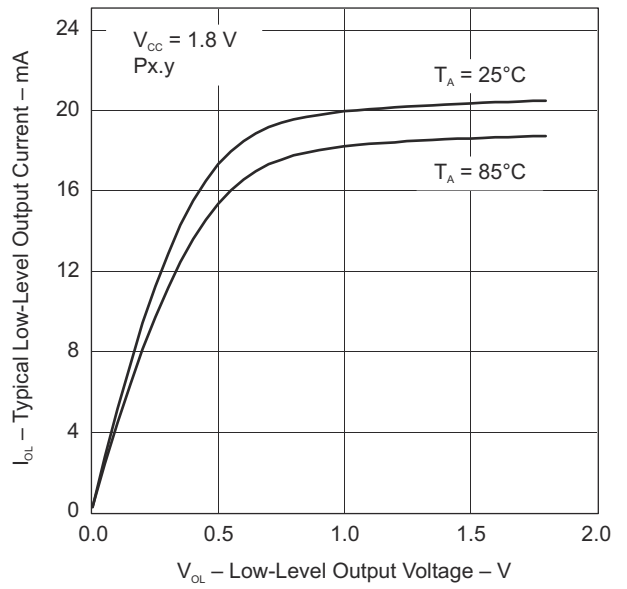

图 7-8. Typical Low-Level Output Current vs Low-Level Output Voltage

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7.13 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1) (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

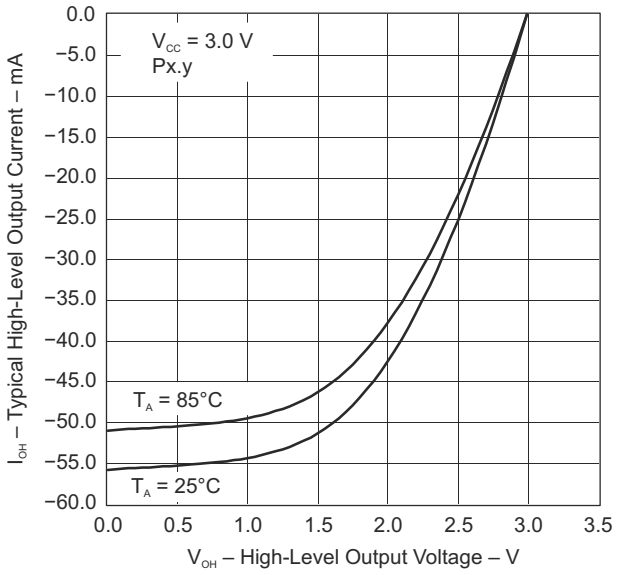

图 7-9. Typical High-Level Output Current vs High-Level Output Voltage

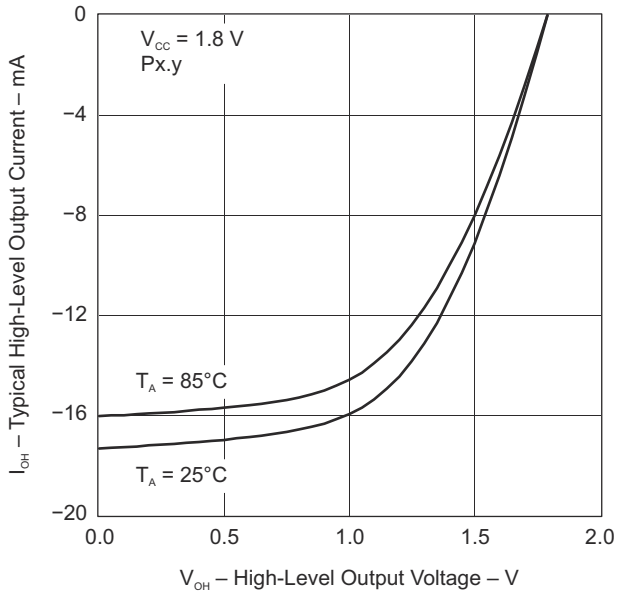

图 7-10. Typical High-Level Output Current vs High-Level Output Voltage

7.14 Crystal Oscillator, XT1, Low-Frequency Mode

over recommended ranges of supply voltage and T_J = – 40°C to 85°C (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC.LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C	3.0 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1 (3) (4)		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals (5)	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode (6)	XTS = 0, XCAPx = 0 (7)			2		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30		70	%

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7.14 Crystal Oscillator, XT1, Low-Frequency Mode (continued)

over recommended ranges of supply voltage and T_J = – 40°C to 85°C (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Fault,LF}$	Oscillator fault frequency, LF mode (8)	XTS = 0 (9)		10		10000	Hz
$t_{START,LF}$	Startup time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 6 pF	3.0 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 12 pF			500		

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) Use of crystal oscillator is not ensured above 85°C. It is recommended that an external digital clock source or other internally generated clock source.
(3) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
(4) Maximum frequency of operation of the entire device cannot be exceeded.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVEx = 0, $C_{L,eff} \leqslant 6$ pF.
- For XT1DRIVEx = 1, 6 pF $\leqslant C_{L,eff} \leqslant$ 9 pF.
- For XT1DRIVEx = 2, 6 pF $\leqslant C_{L,eff} \leqslant$ 10 pF.
- For XT1DRIVEx = 3, $C_{L,eff} \geqslant 6$ pF.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(7) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(8) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

7.15 Crystal Oscillator, XT1, High-Frequency Mode

over recommended ranges of supply voltage and T_J = – 40°C to 85°C (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.HF}$	XT1 oscillator crystal current, HF mode	f_{OSC} = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C	3.0 V		200		µA
		f_{OSC} = 12 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C			260		
		f_{OSC} = 20 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			325		
		f_{OSC} = 32 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			450		

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7.15 Crystal Oscillator, XT1, High-Frequency Mode (continued)

over recommended ranges of supply voltage and T_J = –40°C to 85°C (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{XT1,HF0}$	XT1 oscillator crystal frequency, HF mode 0	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0 (3)		4		8	MHz
$f_{XT1,HF1}$	XT1 oscillator crystal frequency, HF mode 1	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 1 (3)		8		16	MHz
$f_{XT1,HF2}$	XT1 oscillator crystal frequency, HF mode 2	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2 (3)		16		24	MHz
$f_{XT1,HF3}$	XT1 oscillator crystal frequency, HF mode 3	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3 (3)		24		32	MHz
$f_{XT1,HF,SW}$	XT1 oscillator logic-level square-wave input frequency, HF mode, bypass mode	XTS = 1, XT1BYPASS = 1 (3) (4)		0.7		32	MHz
OA_{HF}	Oscillation allowance for HF crystals (5)	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,HF}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,HF}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2, $f_{XT1,HF}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3, $f_{XT1,HF}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Startup time, HF mode	f_{OSC} = 6 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3.0 V		0.5		ms
		f_{OSC} = 20 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
$C_{L,eff}$	Integrated effective load capacitance, HF mode (6) (7)	XTS = 1			1		pF
	Duty cycle, HF mode	XTS = 1, Measured at ACLK, $f_{XT1,HF2}$ = 20 MHz		40	50	60	%
$f_{Fault,HF}$	Oscillator fault frequency, HF mode (8)	XTS = 1 (9)		30		300	kHz

(1) To improve EMI on the XT1 oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) Use of crystal oscillator is not ensured above 85°C. It is recommended that an external digital clock source or other internally generated clock source.

(3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.

(4) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(7) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. In general, an effective load capacitance of up to 18 pF can be supported.

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(8) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

7.16 Crystal Oscillator, XT2

over recommended ranges of supply voltage and T_J = – 40°C to 85°C (unless otherwise noted)(1) (2) (3)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.XT2}$	XT2 oscillator crystal current consumption	f_{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C	3.0 V		200		µA
		f_{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 1, T_A = 25°C			260		
		f_{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C			325		
		f_{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 3, T_A = 25°C			450		
$f_{XT2,HF0}$	XT2 oscillator crystal frequency, mode 0	XT2DRIVEx = 0, XT2BYPASS = 0 (4)		4		8	MHz
$f_{XT2,HF1}$	XT2 oscillator crystal frequency, mode 1	XT2DRIVEx = 1, XT2BYPASS = 0 (4)		8		16	MHz
$f_{XT2,HF2}$	XT2 oscillator crystal frequency, mode 2	XT2DRIVEx = 2, XT2BYPASS = 0 (4)		16		24	MHz
$f_{XT2,HF3}$	XT2 oscillator crystal frequency, mode 3	XT2DRIVEx = 3, XT2BYPASS = 0 (4)		24		32	MHz
$f_{XT2,HF,SW}$	XT2 oscillator logic-level square-wave input frequency, bypass mode	XT2BYPASS = 1 (4) (5)		0.7		32	MHz
OA_{HF}	Oscillation allowance for HF crystals (6)	XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XT2DRIVEx = 1, XT2BYPASS = 0, $f_{XT2,HF1}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XT2DRIVEx = 2, XT2BYPASS = 0, $f_{XT2,HF2}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XT2DRIVEx = 3, XT2BYPASS = 0, $f_{XT2,HF3}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Startup time	f_{OSC} = 6 MHz XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3.0 V		0.5		ms
		f_{OSC} = 20 MHz XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
$C_{L,eff}$	Integrated effective load capacitance, HF mode (2) (7)				1		pF
	Duty cycle	Measured at ACLK, $f_{XT2,HF2}$ = 20 MHz		40	50	60	%
$f_{Fault,HF}$	Oscillator fault frequency (8)	XT2BYPASS = 1 (9)		30		300	kHz

(1) Use of crystal oscillator is not ensured above 85°C. It is recommended that an external digital clock source or other internally generated clock source.
(2) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. In general, an effective load capacitance of up to 18 pF can be supported.
(3) To improve EMI on the XT2 oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.

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- Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(4) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.
(5) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
(6) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(7) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(8) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

7.17 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	5	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK (1)	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK (2)	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%

(1) Calculated using the box method:
Q temperature: (MAX(– 40 to 125°C) – MIN(– 40 to 125°C)) / MIN(– 40 to 125°C) / (125°C – (– 40°C))
M temperature: (MAX(– 55 to 125°C) – MIN(– 55 to 125°C)) / MIN(– 55 to 125°C) / (125°C – (– 55°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

7.18 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V		±3.5		%
		T_A = 25°C	3 V		±1.5		
df_{REFO}/d_T	REFO frequency temperature drift	Measured at ACLK (1)	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK (2)	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%
t_{START}	REFO startup time	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

(1) Calculated using the box method:
Q temperature: (MAX(-40 to 125°C) – MIN(-40 to 125°C)) / MIN(-40 to 125°C) / (125°C – (-40°C))
M temperature: (MAX(-55 to 125°C) – MIN(-55 to 125°C)) / MIN(-55 to 125°C) / (125°C – (-55°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

7.19 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)(1)	DCORSELx = 0, DCOx = 0, MODx = 0	0.065		0.25	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31)(1)	DCORSELx = 0, DCOx = 31, MODx = 0	0.65		1.75	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0)(1)	DCORSELx = 1, DCOx = 0, MODx = 0	0.10		0.41	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31)(1)	DCORSELx = 1, DCOx = 31, MODx = 0	1.42		3.5	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0)(1)	DCORSELx = 2, DCOx = 0, MODx = 0	0.27		0.8	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31)(1)	DCORSELx = 2, DCOx = 31, MODx = 0	3.12		7.43	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0)(1)	DCORSELx = 3, DCOx = 0, MODx = 0	0.59		1.56	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31)(1)	DCORSELx = 3, DCOx = 31, MODx = 0	6.02		14.05	MHz

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7.19 DCO Frequency (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(4,0)}$	DCO frequency (4, 0)(1)	DCORSELx = 4, DCOx = 0, MODx = 0	1.25		3.25	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31)(1)	DCORSELx = 4, DCOx = 31, MODx = 0	12.25		28.25	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0)(1)	DCORSELx = 5, DCOx = 0, MODx = 0	2.45		6.05	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31)(1)	DCORSELx = 5, DCOx = 31, MODx = 0	23.65		54.15	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0)(1)	DCORSELx = 6, DCOx = 0, MODx = 0	4.55		10.75	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31)(1)	DCORSELx = 6, DCOx = 31, MODx = 0	38.95		88.05	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0)(1)	DCORSELx = 7, DCOx = 0, MODx = 0	8.45		19.65	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31)(1)	DCORSELx = 7, DCOx = 31, MODx = 0	59.95		135.05	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40	50	60	%
df_{DCO}/dT	DCO frequency temperature drift(2)	f_{DCO} = 1 MHz		0.1		%/°C
df_{DCO}/dV_{CC}	DCO frequency voltage drift(3)	f_{DCO} = 1 MHz		1.9		%/V

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO}, should be set to reside within the range of $f_{DCO(n,0),MAX} \leqslant f_{DCO} \leqslant f_{DCO(n,31),MIN}$, where $f_{DCO(n,0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

(2) Calculated using the box method:
Q temperature: (MAX(– 40 to 125°C) – MIN(– 40 to 125°C)) / MIN(– 40 to 125°C) / (125°C – (– 40°C))
M temperature: (MAX(– 55 to 125°C) – MIN(– 55 to 125°C)) / MIN(– 55 to 125°C) / (125°C – (– 55°C))

(3) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

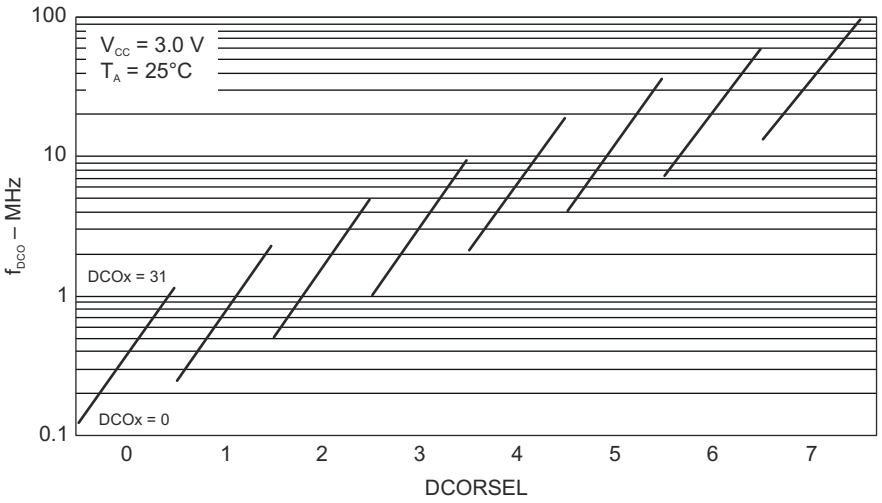

图 7-11. Typical DCO Frequency

7.20 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V(DV_{CC}_BOR_IT-)$	BOR_H on voltage, DV_{CC} falling level	$\lvert dDV_{CC}/d_t \rvert$ < 3 V/s			1.47	V
$V(DV_{CC}_BOR_IT+)$	BOR_H off voltage, DV_{CC} rising level	$\lvert dDV_{CC}/d_t \rvert$ < 3 V/s	0.78	1.30	1.52	V
$V(DV_{CC}_BOR_hys)$	BOR_H hysteresis		58		275	mV
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset		2			µs

7.21 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CORE3}(AM)$	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.90		V
$V_{CORE2}(AM)$	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.80		V
$V_{CORE1}(AM)$	Core voltage, active mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.60		V
$V_{CORE0}(AM)$	Core voltage, active mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.40		V
$V_{CORE3}(LPM)$	Core voltage, low-current mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.94		V
$V_{CORE2}(LPM)$	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.84		V
$V_{CORE1}(LPM)$	Core voltage, low-current mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.64		V
$V_{CORE0}(LPM)$	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.44		V

7.22 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		1.5		µA
$V_{(SVSH_IT-)}$	SVS_H on voltage level (1)	SVSHE = 1, SVSHRVL = 0	1.55	1.68	1.8	V
		SVSHE = 1, SVSHRVL = 1	1.77	1.88	2	
		SVSHE = 1, SVSHRVL = 2	1.96	2.08	2.23	
		SVSHE = 1, SVSHRVL = 3	2.07	2.18	2.33	
$V_{(SVSH_IT+)}$	SVS_H off voltage level (1)	SVSHE = 1, SVSMHRRL = 0	1.60	1.74	1.87	V
		SVSHE = 1, SVSMHRRL = 1	1.86	1.94	2.09	
		SVSHE = 1, SVSMHRRL = 2	2.05	2.14	2.3	
		SVSHE = 1, SVSMHRRL = 3	2.18	2.30	2.44	
		SVSHE = 1, SVSMHRRL = 4	2.30	2.40	2.57	
		SVSHE = 1, SVSMHRRL = 5	2.50	2.70	2.9	
		SVSHE = 1, SVSMHRRL = 6	2.85	3.10	3.25	
		SVSHE = 1, SVSMHRRL = 7	2.85	3.10	3.25	

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7.22 PMM, SVS High Side (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		20		
$t_{(SVSH)}$	SVS_H on or off delay time	SVSHE = 0 → 1, SVSHFP = 1		12.5		µs
		SVSHE = 0 → 1, SVSHFP = 0		100		
dV_{DVCC}/dt	DV_{CC} rise time		0		1000	V/s

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430F5xx and MSP430F6xx Family User's Guide*.on recommended settings and use.

7.23 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE= 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		1.5		µA
$V_{(SVMH)}$	SVM_H on or off voltage level (1)	SVMHE = 1, SVSMHRRL = 0	1.61	1.74	1.87	V
		SVMHE = 1, SVSMHRRL = 1	1.86	1.94	2.09	
		SVMHE = 1, SVSMHRRL = 2	2.05	2.14	2.30	
		SVMHE = 1, SVSMHRRL = 3	2.18	2.30	2.44	
		SVMHE = 1, SVSMHRRL = 4	2.30	2.40	2.58	
		SVMHE = 1, SVSMHRRL = 5	2.50	2.70	2.93	
		SVMHE = 1, SVSMHRRL = 6	2.85	3.10	3.25	
		SVMHE = 1, SVSMHRRL = 7	2.85	3.10	3.25	
		SVMHE = 1, SVMHOVPE = 1		3.75		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		2.5		µs
		SVMHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		20		
$t_{(SVMH)}$	SVM_H on or off delay time	SVMHE = 0 → 1, SVMHFP = 1		12.5		µs
		SVMHE = 0 → 1, SVMHFP = 0		100		

(1) The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide*.on recommended settings and use.

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7.24 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		1.5		µA
$t_{pd(SVSL)}$	SVS_L propagation delay	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		2.5		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		20		
$t_{(SVSL)}$	SVS_L on or off delay time	SVSLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		12.5		µs
		SVSLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		100		

7.25 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 0		200		nA
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 1		1.5		µA
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		20		
$t_{(SVML)}$	SVM_L on or off delay time	SVMLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		12.5		µs
		SVMLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		100		

7.26 Wakeup From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{WAKE-UP-FAST}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode (1) (2)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	$f_{MCLK} \geqslant$ 4.0 MHz		3.5	7.5	µs
			1.0 MHz < f_{MCLK} < 4.0 MHz		4.5	9.5	
$t_{WAKE-UP-SLOW}$	Wake-up time from LPM2, LPM3 or LPM4 to active mode (3)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0			150	170	µs
$t_{WAKE-UP-LPM5}$	Wake-up time from LPM4.5 to active mode (4)				2	3.5	ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode (4)				2	3.5	ms

(1) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS_L) and low side monitor (SVM_L). Fastest wakeup times are possible with SVS_L and SVM_L in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430F5xx and MSP430F6xx Family User's Guide*.

(2) Ensured only until T_J = 85°C.

(3) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS_L) and low side monitor (SVM_L). In this case, the SVS_L and SVM_L are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430F5xx and MSP430F6xx Family User's Guide*.

(4) This value represents the time from the wakeup event to the reset vector execution.

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7.27 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK, External: TACLK, Duty cycle = 50% ± 10%	1.8 V/ 3.0 V			25	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	1.8 V/ 3.0 V	20			ns

7.28 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ± 10%	1.8 V/ 3.0 V			25	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, Minimum pulse duration required for capture	1.8 V/ 3.0 V	20			ns

7.29 USCI (UART Mode) Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)					1	MHz

7.30 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
t_τ	UART receive deglitch time (1)	2.2 V	50		600	ns
		3 V	48		620	

(1) Pulses on the UART receive input (UCxRX) that are shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

7.31 USCI (SPI Master Mode) Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz

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7.32 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK, Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time	PMMCOREV = 0	1.8 V	55			ns
			3.0 V	38			
		PMMCOREV = 3	2.4 V	30			ns
			3.0 V	25			
$t_{HD,MI}$	SOMI input data hold time	PMMCOREV = 0	1.8 V	0			ns
			3.0 V	0			
		PMMCOREV = 3	2.4 V	0			ns
			3.0 V	0			
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 0	1.8 V			20	ns
			3.0 V			18	
		UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 3	2.4 V			16	ns
			3.0 V			15	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	-10			ns
			3.0 V	-8			
		C_L = 20 pF, PMMCOREV = 3	2.4 V	-10			ns
			3.0 V	-8			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in 图 7-12 and 图 7-13.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in 图 7-12 and 图 7-13.

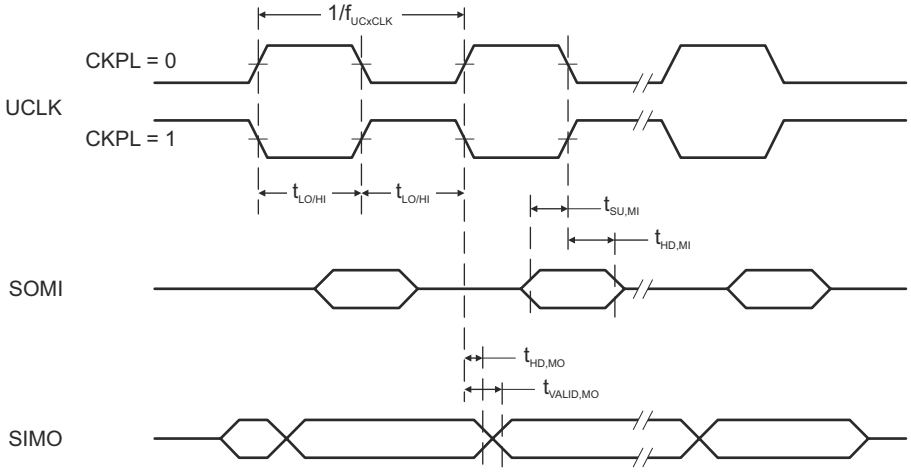

图 7-12. SPI Master Mode, CKPH = 0

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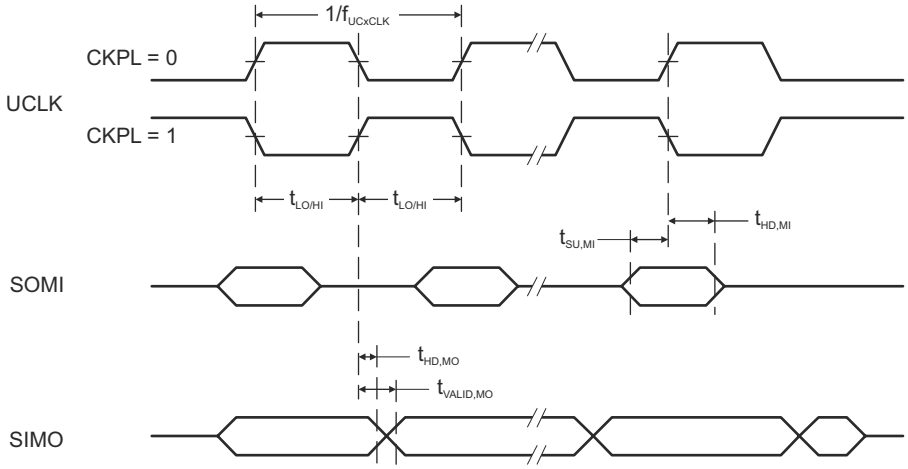

图 7-13. SPI Master Mode, CKPH = 1

7.33 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock	PMMCOREV = 0	1.8 V	11			ns
			3.0 V	8			
		PMMCOREV = 3	2.4 V	7			ns
			3.0 V	6			
$t_{STE,LAG}$	STE lag time, Last clock to STE high	PMMCOREV = 0	1.8 V	3			ns
			3.0 V	3			
		PMMCOREV = 3	2.4 V	3			ns
			3.0 V	3			
$t_{STE,ACC}$	STE access time, STE low to SOMI data out	PMMCOREV = 0	1.8 V			66	ns
			3.0 V			50	
		PMMCOREV = 3	2.4 V			36	ns
			3.0 V			30	
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance	PMMCOREV = 0	1.8 V			30	ns
			3.0 V			23	
		PMMCOREV = 3	2.4 V			16	ns
			3.0 V			13	
$t_{SU,SI}$	SIMO input data setup time	PMMCOREV = 0	1.8 V	5			ns
			3.0 V	5			
		PMMCOREV = 3	2.4 V	2			ns
			3.0 V	2			
$t_{HD,SI}$	SIMO input data hold time	PMMCOREV = 0	1.8 V	5			ns
			3.0 V	5			
		PMMCOREV = 3	2.4 V	5			ns
			3.0 V	5			
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 0	1.8 V			76	ns
			3.0 V			60	
		UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 3	2.4 V			44	ns
			3.0 V			40	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	18			ns
			3.0 V	12			
		C_L = 20 pF, PMMCOREV = 3	2.4 V	10			ns
			3.0 V	8			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, refer to the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in 图 7-14 and 图 7-15.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in 图 7-14 and 图 7-15.

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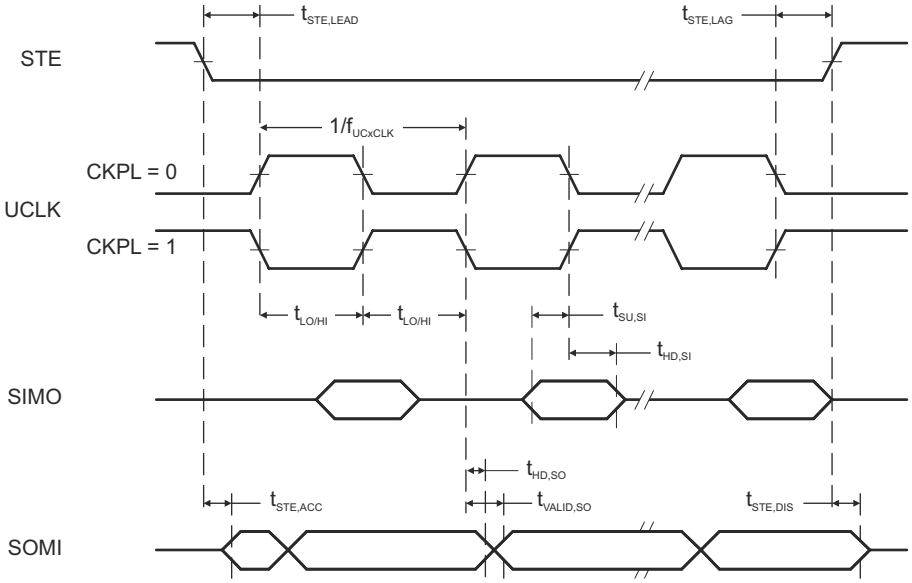

图 7-14. SPI Slave Mode, CKPH = 0

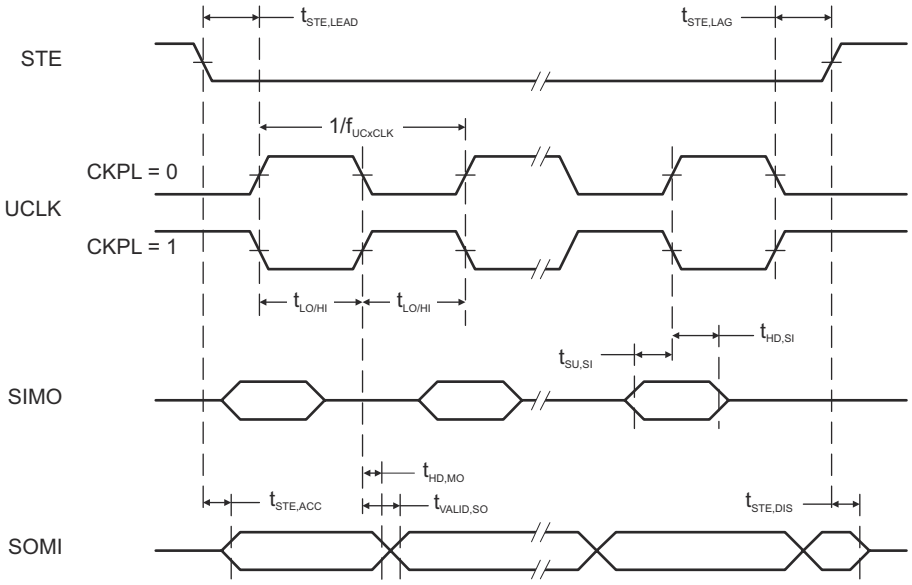

图 7-15. SPI Slave Mode, CKPH = 1

7.34 USCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 7-16)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \leqslant 100$ kHz	2.2 V, 3 V	4.0			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \leqslant 100$ kHz	2.2 V, 3 V	4.7			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP	$f_{SCL} \leqslant 100$ kHz	2.2 V, 3 V	4.0			µs
		$f_{SCL} > 100$ kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50		600	ns
			3 V	50		600	

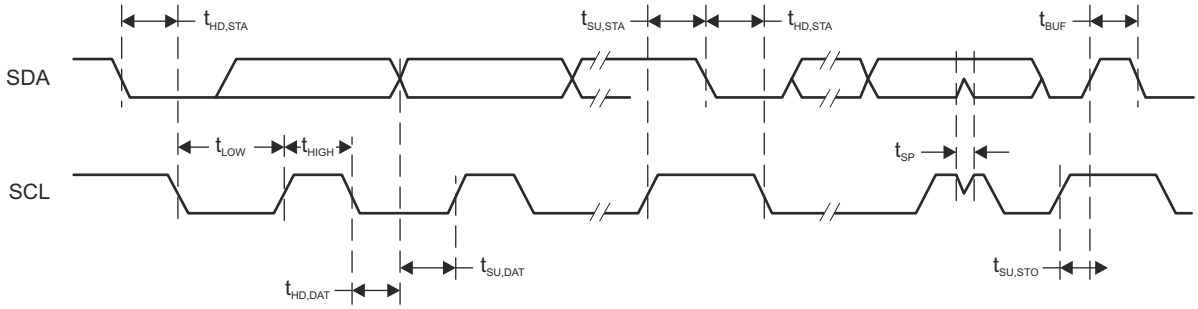

图 7-16. I2C Mode Timing

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7.35 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(Ax)}$	Analog input voltage range(2)	All ADC12 analog input pins Ax		0		AV_{CC}	V
I_{ADC12_A}	Operating supply current into AVCC terminal(3)	$f_{ADC12CLK}$ = 5.0 MHz(4)	2.2 V		125	200	µA
			3 V		150	270	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20		pF
R_I	Input MUX ON resistance	$0 V \leqslant V_{Ax} \leqslant AVCC$			200		Ω

(1) The leakage current is specified by the digital I/O input leakage.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See 节 7.40 and 节 7.41.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12_A}.
(4) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0.

7.36 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	ADC conversion clock	For specified performance of ADC12 linearity parameters using an external reference voltage or AVCC as reference. (1)	2.2 V, 3 V	0.45	4.8	5.0	MHz
		For specified performance of ADC12 linearity parameters using the internal reference. (2)		0.45	2.4	4.0	
		For specified performance of ADC12 linearity parameters using the internal reference. (3)		0.45	2.4	2.7	
$f_{ADC12OSC}$	Internal ADC12 oscillator (4)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock	2.2 V, 3 V	2.4		3.1	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0				(5)	
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 20 pF, τ = $[R_S + R_I] \times C_I$ (6)	2.2 V, 3 V	1000			ns

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with $f_{ADC12CLK}$ maximum of 5.0 MHz.
(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1
(3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.
(4) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(5) 13 × ADC12DIV × $1/f_{ADC12CLK}$
(6) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

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7.37 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (1)	1.4 V ≤ dVREF ≤ 1.6 V (2)	2.2 V, 3 V		±2.0		LSB
		1.6 V < dVREF (2)			±1.7		
E_D	Differential linearity error (1)	(2)	2.2 V, 3 V		±1.0		LSB
E_O	Offset error (3)	dVREF ≤ 2.2 V (2)	2.2 V, 3 V		±2.0		LSB
		dVREF > 2.2 V (2)	2.2 V, 3 V		±2.0		
E_G	Gain error (3)	(2)	2.2 V, 3 V		±2.0		LSB
E_T	Total unadjusted error	dVREF ≤ 2.2 V (2)	2.2 V, 3 V		±3.5		LSB
		dVREF > 2.2 V (2)	2.2 V, 3 V		±3.5		

(1) Parameters are derived using the histogram method.
(2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = V_{R+} - V_{R-}, V_{R+} < AVCC, V_{R-} > AVSS. Unless otherwise mentioned, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω and two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current. See also the *MSP430F5xx and MSP430F6xx Family User's Guide*.
(3) Parameters are derived using a best fit curve.

7.38 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)		V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±1.7		LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±2.5		
E_D	Differential linearity error (2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		+1.5		LSB
		ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 2.7 MHz			+1.0		
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			+2.5		
E_O	Offset error (3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±4.0		LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±4.0		
E_G	Gain error (3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±2.5		LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±1.5% (4)		VREF
E_T	Total unadjusted error	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±5		LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±1.5% (4)		VREF

(1) The internal reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 1. dVREF = V_{R+} - V_{R-}.
(2) Parameters are derived using the histogram method.
(3) Parameters are derived using a best fit curve.
(4) The gain error and total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode the reference voltage used by the ADC12_A is not available on a pin.

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7.39 12-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	See (2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		680		mV
			3 V		680		
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V		2.25		mV/°C
			3 V		2.25		
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	100			µs
			3 V	100			
V_{MID}	AV_{CC} divider at channel 11, V_{AVCC} factor	ADC12ON = 1, INCH = 0Bh		0.48	0.5	0.52	V_{AVCC}
	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh	2.2 V	1.04	1.1	1.14	V
			3 V	1.44	1.5	1.56	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (4)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V, 3 V	1000			ns

(1) The temperature sensor is provided by the REF module. See the REF module parametric I_{REF+} regarding the current consumption of the temperature sensor.
(2) The temperature sensor offset can be significant. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor. The TLV structure contains calibration values for 30°C ± 3°C and 85°C ± 3°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} * (Temperature,°C) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy. See also the *MSP430F5xx and MSP430F6xx Family User's Guide*.
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

7.40 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (1)		1.4		AV_{CC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (2)		0		1.2	V
$(V_{eREF+} - V_{REF-}/V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (3)		1.4		AV_{CC}	V
I_{VeREF+}, $I_{VREF-/VeREF-}$	Static input current	1.4 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC12CLK}$ = 5 MHz, T_J = 25°C, ADC12SHTx = 1h, Conversion rate 200 ksps	2.2 V, 3 V		±26		µA
		1.4 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, Conversion rate 20 ksps	2.2 V, 3 V	-2.5		2.5	µA
$C_{VREF+/-}$	Capacitance at V_{REF+} and V_{REF-} terminals	See (4)			10		µF

(1) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(2) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(4) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the *MSP430F5xx and MSP430F6xx Family User's Guide*.

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7.41 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = REFOUT = 1, I_{VREF+} = 0 A	3 V		2.50	±2.5%	V
		REFVSEL = {1} for 2.0 V, REFON = REFOUT = 1, I_{VREF+} = 0 A	3 V		1.98	±2.5%	
		REFVSEL = {0} for 1.5 V, REFON = REFOUT = 1, I_{VREF+} = 0 A	2.2 V, 3 V		1.49	±2.5%	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.5 V		2.2			V
		REFVSEL = {1} for 2.0 V		2.3			
		REFVSEL = {2} for 2.5 V		2.8			
I_{REF+}	Operating supply current into AV_{CC} terminal (2) (3)	ADC12SR = 1, REFON = 1, REFOUT = 0, REFBURST = 0	3 V		70		µA
		ADC12SR = 1, REFON = 1, REFOUT = 1, REFBURST = 0	3 V		0.45		mA
		ADC12SR = 0, REFON = 1, REFOUT = 0, REFBURST = 0	3 V		210	350	µA
		ADC12SR = 0, REFON = 1, REFOUT = 1, REFBURST = 0	3 V		0.95	2	mA
$I_{L(VREF+)}$	Load-current regulation, V_{REF+} terminal (4)	REFVSEL = (0, 1, 2) I_{VREF+} = +10 µA/ – 1000 µA AV_{CC} = $AV_{CC\ (min)}$ for each reference level, REFVSEL = (0, 1, 2), REFON = REFOUT = 1			2500		µV/mA
C_{VREF+}	Capacitance at VREF+ terminals	REFON = REFOUT = 1		20		100	pF
TC_{REF+}	Temperature coefficient of built-in reference (5)	I_{VREF+} = 0 A, REFVSEL = (0, 1, 2), REFON = 1, REFOUT = 0 or 1			30		ppm/°C
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, T_J = 25°C, REFVSEL = (0, 1, 2), REFON = 1, REFOUT = 0 or 1			120		µV/V
PSRR_AC	Power supply rejection ratio (AC)	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, T_J = 25°C, f = 1 kHz, ∆Vpp = 100 mV, REFVSEL = (0, 1, 2), REFON = 1, REFOUT = 0 or 1			6.4		mV/V
t_{SETTLE}	Settling time of reference voltage (6)	AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, REFVSEL = (0, 1, 2), REFOUT = 0, REFON = 0 → 1			75		µs
		AV_{CC} = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, C_{VREF} = C_{VREF}(max), REFVSEL = (0, 1, 2), REFOUT = 1, REFON = 0 → 1			75		

(1) The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger for driving the V_{REF+} terminal. When REFOUT = 1, the reference is available at the V_{REF+} terminal, as well as, used as the reference for the conversion and utilizes the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and utilizes the smaller buffer.

(2) The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.

(3) The temperature sensor is provided by the REF module. Its current is supplied via terminal AV_{CC} and is equivalent to I_{REF+} with REFON =1 and REFOUT = 0.

(4) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB trace, etc.

(5) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C)/(85°C – (–40°C)).

(6) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.

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7.42 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DV_{CC(PGM/ERASE)}$	Program and erase supply voltage		1.8		3.6	V
I_{PGM}	Average supply current from DVCC during program			3	7	mA
I_{ERASE}	Average supply current from DVCC during erase				7	mA
I_{MERASE}, I_{BANK}	Average supply current from DVCC during mass erase or bank erase				7	mA
t_{CPT}	Cumulative program time	See (1)			16	ms
	Program and erase endurance	T_J = -40°C to 105°C	10^4	10^5		cycles
$t_{Retention}$	Data retention duration (2)	T_J = 25°C	100			years
t_{Word}	Word or byte program time	See (3)	64		85	µs
$t_{Block, 0}$	Block program time for first byte or word	See (3)	49		65	µs
$t_{Block, 1-(N-1)}$	Block program time for each additional byte or word, except for last byte or word	See (3)	37		49	µs
$t_{Block, N}$	Block program time for last byte or word	See (3)	55		73	µs
t_{Erase}	Erase time for segment, mass erase, and bank erase when available.	See (3)	23		32	ms
$f_{MCLK,MGR}$	MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4. MGR1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the flash controller's state machine.
(3) The data retention specification is based on qualification stress testing at 170°C for 420 hours with temperature derating based on an Arrhenius model with activation energy of 0.6 eV. Additional flash retention documentation is provided in application report SLAA392.

7.43 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2.2 V, 3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG (2)	2.2 V	0		5	MHz
		3 V	0		10	MHz
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools accessing the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

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8 Detailed Description

8.1 CPU

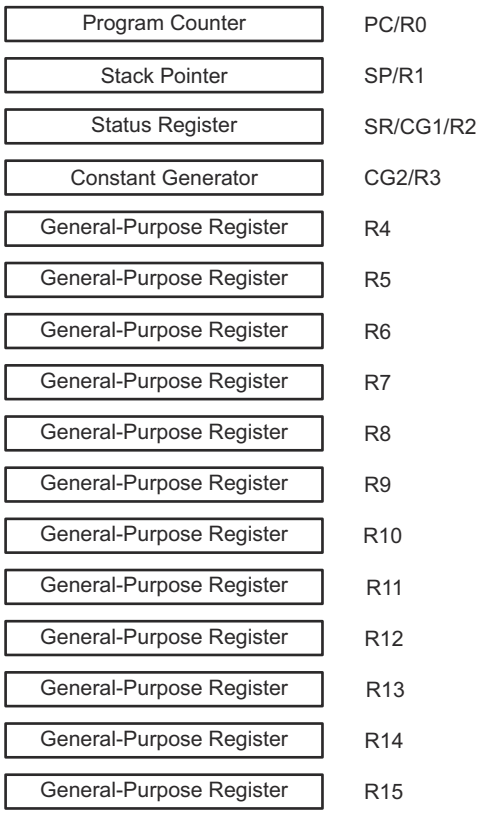
The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.



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8.2 Operating Modes

The MCU has one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL loop control and DCOCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wakeup from $\overline{\text{RST}}$, digital I/O

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8.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

表 8-1. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog Timeout, Password Violation Flash Memory Password Violation PMM Password Violation	WDTIFG, KEYV (SYSRSTIV) (1) (2)	Reset	0FFFEh	63, highest
System NMI PMM Vacant Memory Access JTAG Mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) (1)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator Fault Flash Memory Access Violation	NMIIFG, OFIFG, ACCVIFG (SYSUNIV) (1) (2)	(Non)maskable	0FFFAh	61
TB0	TBCCR0 CCIFG0 (3)	Maskable	0FFF8h	60
TB0	TBCCR1 CCIFG1 to TBCCR6 CCIFG6, TBIFG (TBIV) (1) (3)	Maskable	0FFF6h	59
Watchdog Timer_A Interval Timer Mode	WDTIFG	Maskable	0FFF4h	58
USCI_A0 Receive and Transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV) (1) (3)	Maskable	0FFF2h	57
USCI_B0 Receive and Transmit	UCB0RXIFG, UCB0TXIFG (UCB0IV) (1) (3)	Maskable	0FFF0h	56
ADC12_A	ADC12IFG0 to ADC12IFG15 (ADC12IV) (1) (3)	Maskable	0FFEEh	55
TA0	TA0CCR0 CCIFG0 (3)	Maskable	0FFECh	54
TA0	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV) (1) (3)	Maskable	0FFEAh	53
USCI_A2 Receive and Transmit	UCA2RXIFG, UCA2TXIFG (UCA2IV) (1) (3)	Maskable	0FFE8h	52
USCI_B2 Receive and Transmit	UCB2RXIFG, UCB2TXIFG (UCB2IV) (1) (3)	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) (1) (3)	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0 (3)	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) (1) (3)	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV) (1) (3)	Maskable	0FFDEh	47
USCI_A1 Receive and Transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV) (1) (3)	Maskable	0FFDCh	46
USCI_B1 Receive and Transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV) (1) (3)	Maskable	0FFDAh	45
USCI_A3 Receive and Transmit	UCA3RXIFG, UCA3TXIFG (UCA3IV) (1) (3)	Maskable	0FFD8h	44
USCI_B3 Receive and Transmit	UCB3RXIFG, UCB3TXIFG (UCB3IV) (1) (3)	Maskable	0FFD6h	43
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV) (1) (3)	Maskable	0FFD4h	42
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) (1) (3)	Maskable	0FFD2h	41
Reserved	Reserved (4)		0FFD0h	40
			⋮	⋮
			0FF80h	0, lowest

(1) Multiple source flags.
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

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8.4 Memory Organization

		MSP430F5438A
Memory (flash) Main: interrupt vector Main: code memory	Total Size Flash Flash	256 KB 00FFFFh – 00FF80h 045BFFh – 005C00h
Main: code memory	Bank D	64 KB 03FFFFh – 030000h
	Bank C	64 KB 02FFFFh – 020000h
	Bank B	64 KB 01FFFFh – 010000h
	Bank A	64 KB 045BFFh – 040000h 00FFFFh – 005C00h
RAM	Size	16 KB
	Sector 3	4 KB 005BFFh – 004C00h
	Sector 2	4 KB 004BFFh – 003C00h
	Sector 1	4 KB 003BFFh – 002C00h
	Sector 0	4 KB 002BFFh – 001C00h
Information memory (flash)	Info A	128 B 0019FFh – 001980h
	Info B	128 B 00197Fh – 001900h
	Info C	128 B 0018FFh – 001880h
	Info D	128 B 00187Fh – 001800h
Bootstrap loader (BSL) memory (Flash)	BSL 3	512 B 0017FFh – 001600h
	BSL 2	512 B 0015FFh – 001400h
	BSL 1	512 B 0013FFh – 001200h
	BSL 0	512 B 0011FFh – 001000h
Peripherals	Size	4KB 000FFFh – 000000h

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8.5 Bootloader (BSL)

The BSL lets users program the flash memory or RAM using a UART serial interface. Access to the device memory through the BSL is protected by an user-defined password. Use of the BSL requires four pins as shown in 表 8-2. BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see the MSP430™ Flash Devices Bootloader (BSL) User's Guide.

表 8-2. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.1	Data transmit
P1.2	Data receive
VCC	Power supply
VSS	Ground supply

8.6 JTAG Operation

8.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in 表 8-3. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For the description of the Spy-Bi-Wire interface and its implementation, see the *MSP430 Programming With the JTAG Interface User's Guide*.

表 8-3. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input/TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

8.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in 表 8-4. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For the description of the Spy-Bi-Wire interface and its implementation, see the *MSP430 Programming With the JTAG Interface User's Guide*.

表 8-4. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply

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表 8-4. Spy-Bi-Wire Pin Requirements and Functions (continued)

DEVICE SIGNAL	DIRECTION	FUNCTION
VSS		Ground supply

8.7 Flash Memory

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

8.8 RAM Memory

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage, however all data is lost. Features of the RAM memory include:

- RAM memory has n sectors. The size of a sector can be found in Memory Organization.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.
- For devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

8.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430F5xx and MSP430F6xx Family User's Guide*.

8.9.1 Digital I/O

There are up to ten 8-bit I/O ports implemented: For 100-pin options, P1 through P10 are complete. P11 contains three individual I/O ports. For 80-pin options, P1 through P7 are complete. P8 contains seven individual I/O ports. P9 through P11 do not exist. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wakeup input capability is available for all bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P11) or word-wise in pairs (PA through PF).

8.9.2 Oscillator and System Clock

The clock system in the MSP430x5xx family of devices is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (XT1 LF mode), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT1 HF mode or XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 5 µs. The UCS module provides the following clock signals:

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- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal, a high-frequency crystal, the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

8.9.3 Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

8.9.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

8.9.5 Real-Time Clock (RTC_A)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

8.9.6 Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

8.9.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, boot strap loader entry mechanisms, as well as, configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

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表 8-5. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		$\overline{\text{RST}}$/NMI (POR)	04h	
		PMMSWBOR (BOR)	06h	
		Wakeup from LPMx.5	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		PMMSWPOR (POR)	14h	
		WDT timeout (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		Reserved	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		SVSMLDLYIFG	06h	
		SVSMHDLYIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		SVMLVLRIFG	10h	
		SVMHVLRIFG	12h	
		Reserved	14h to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIFG	02h	Highest
		OFIFG	04h	
		ACCVIFG	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

8.9.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

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表 8-6. DMA Trigger Assignments

TRIGGER	CHANNEL		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
6	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
7	Reserved	Reserved	Reserved
8	Reserved	Reserved	Reserved
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG
24	ADC12IFGx	ADC12IFGx	ADC12IFGx
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

8.9.9 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3 pin or 4 pin) or I2C.

The MSP430F5438A, MSP430F5436A, and MSP430F5419A include four complete USCI modules (n = 0 to 3). The MSP430F5437A, MSP430F5435A, and MSP430F5418A include two complete USCI modules (n = 0 to 1).

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8.9.10 TA0

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 8-7. TA0 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
17, H1-P1.0	TA0CLK	TACLK	Timer	NA	NA	
	ACLK	ACLK				
	SMCLK	SMCLK				
17, H1-P1.0	TA0CLK	$\overline{\text{TACLK}}$				
18, H4-P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	18, H4-P1.1
57, H9-P8.0	TA0.0	CCI0B				57, H9-P8.0
	DV_{SS}	GND				ADC12 (internal) ADC12SHSx = {1}
	DV_{CC}	V_{CC}				
19, J4-P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	19, J4-P1.2
58, H11-P8.1	TA0.1	CCI1B				58, H11-P8.1
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
20, J1-P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	20, J1-P1.3
59, H12-P8.2	TA0.2	CCI2B				59, H12-P8.2
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
21, J2-P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	21, J2-P1.4
60, G9-P8.3	TA0.3	CCI3B				60, G9-P8.3
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
22, K1-P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	22, K1-P1.5
61, G11-P8.4	TA0.4	CCI4B				61, G11-P8.4
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				

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8.9.11 TA1

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 8-8. TA1 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
25, M1-P2.0	TA1CLK	TACLK	Timer	NA	NA	
	ACLK	ACLK				
	SMCLK	SMCLK				
25, M1-P2.0	TA1CLK	$\overline{\text{TACLK}}$				
26, L2-P2.1	TA1.0	CCI0A	CCR0	TA0	TA1.0	26, L2-P2.1
65, F11-P8.5	TA1.0	CCI0B				65, F11-P8.5
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
27, M2-P2.2	TA1.1	CCI1A	CCR1	TA1	TA1.1	27, M2-P2.2
66, E11-P8.6	TA1.1	CCI1B				66, E11-P8.6
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
28, L3-P2.3	TA1.2	CCI2A	CCR2	TA2	TA1.2	28, L3-P2.3
56, J12-P7.3	TA1.2	CCI2B				56, J12-P7.3
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				

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8.9.12 TB0

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 8-9. TB0 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
50, M12-P4.7	TB0CLK	TBCLK	Timer	NA	NA	
	ACLK	ACLK				
	SMCLK	SMCLK				
50, M12-P4.7	TB0CLK	$\overline{\text{TBCLK}}$				
43, J8-P4.0	TB0.0	CCI0A	CCR0	TB0	TB0.0	43, J8-P4.0
43, J8-P4.0	TB0.0	CCI0B				ADC12 (internal) ADC12SHSx = {2}
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
44, M9-P4.1	TB0.1	CCI1A	CCR1	TB1	TB0.1	44, M9-P4.1
44, M9-P4.1	TB0.1	CCI1B				ADC12 (internal) ADC12SHSx = {3}
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
45, L9-P4.2	TB0.2	CCI2A	CCR2	TB2	TB0.2	45, L9-P4.2
45, L9-P4.2	TB0.2	CCI2B				
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
46, L10-P4.3	TB0.3	CCI3A	CCR3	TB3	TB0.3	46, L10-P4.3
46, L10-P4.3	TB0.3	CCI3B				
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
47, M10-P4.4	TB0.4	CCI4A	CCR4	TB4	TB0.4	47, M10-P4.4
47, M10-P4.4	TB0.4	CCI4B				
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
48, L11-P4.5	TB0.5	CCI5A	CCR5	TB5	TB0.5	48, L11-P4.5
48, L11-P4.5	TB0.5	CCI5B				
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				
49, M11-P4.6	TB0.6	CCI6A	CCR6	TB6	TB0.6	49, M11-P4.6
	ACLK (internal)	CCI6B				
	DV_{SS}	GND				
	DV_{CC}	V_{CC}				

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8.9.13 ADC12_A

The ADC12_A module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

8.9.14 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

8.9.15 REF Voltage Reference

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

8.9.16 Embedded Emulation Module (EEM) (L Version)

The EEM supports real-time in-system debugging. The L version of the EEM implemented on all devices has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware trigger or breakpoint on CPU register write access
- Up to ten hardware triggers can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

8.9.17 Peripheral File Map

表 8-10. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see 表 8-11)	0100h	000h - 01Fh
PMM (see 表 8-12)	0120h	000h - 010h
Flash Control (see 表 8-13)	0140h	000h - 00Fh
CRC16 (see 表 8-14)	0150h	000h - 007h
RAM Control (see 表 8-15)	0158h	000h - 001h
Watchdog (see 表 8-16)	015Ch	000h - 001h
UCS (see 表 8-17)	0160h	000h - 01Fh
SYS (see 表 8-18)	0180h	000h - 01Fh
Shared Reference (see 表 8-19)	01B0h	000h - 001h
Port P1, P2 (see 表 8-20)	0200h	000h - 01Fh
Port P3, P4 (see 表 8-21)	0220h	000h - 00Bh
Port P5, P6 (see 表 8-22)	0240h	000h - 00Bh
Port P7, P8 (see 表 8-23)	0260h	000h - 00Bh
Port P9, P10 (see 表 8-24)	0280h	000h - 00Bh
Port P11 (see 表 8-25)	02A0h	000h - 00Ah
Port PJ (see 表 8-26)	0320h	000h - 01Fh
TA0 (see 表 8-27)	0340h	000h - 02Eh
TA1 (see 表 8-28)	0380h	000h - 02Eh
TB0 (see 表 8-29)	03C0h	000h - 02Eh
Real Timer Clock (RTC_A) (see 表 8-30)	04A0h	000h - 01Bh

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表 8-10. Peripherals (continued)

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
32-bit Hardware Multiplier (see 表 8-31)	04C0h	000h - 02Fh
DMA General Control (see 表 8-32)	0500h	000h - 00Fh
DMA Channel 0 (see 表 8-32)	0510h	000h - 00Ah
DMA Channel 1 (see 表 8-32)	0520h	000h - 00Ah
DMA Channel 2 (see 表 8-32)	0530h	000h - 00Ah
USCI_A0 (see 表 8-33)	05C0h	000h - 01Fh
USCI_B0 (see 表 8-34)	05E0h	000h - 01Fh
USCI_A1 (see 表 8-35)	0600h	000h - 01Fh
USCI_B1 (see 表 8-36)	0620h	000h - 01Fh
USCI_A2 (see 表 8-37)	0640h	000h - 01Fh
USCI_B2 (see 表 8-38)	0660h	000h - 01Fh
USCI_A3 (see 表 8-39)	0680h	000h - 01Fh
USCI_B3 (see 表 8-40)	06A0h	000h - 01Fh
ADC12_A (see 表 8-41)	0700h	000h - 03Eh

表 8-11. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

表 8-12. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high side control	SVSMHCTL	04h
SVS low side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

表 8-13. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

表 8-14. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

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表 8-15. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

表 8-16. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

表 8-17. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

表 8-18. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootstrap loader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

表 8-19. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

表 8-20. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch

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表 8-20. Port P1, P2 Registers (Base Address: 0200h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

表 8-21. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

表 8-22. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pullup/pulldown enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pullup/pulldown enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

表 8-23. Port P7, P8 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 pullup/pulldown enable	P7REN	06h

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表 8-23. Port P7, P8 Registers (Base Address: 0260h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 drive strength	P7DS	08h
Port P7 selection	P7SEL	0Ah
Port P8 input	P8IN	01h
Port P8 output	P8OUT	03h
Port P8 direction	P8DIR	05h
Port P8 pullup/pulldown enable	P8REN	07h
Port P8 drive strength	P8DS	09h
Port P8 selection	P8SEL	0Bh

表 8-24. Port P9, P10 Registers (Base Address: 0280h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P9 input	P9IN	00h
Port P9 output	P9OUT	02h
Port P9 direction	P9DIR	04h
Port P9 pullup/pulldown enable	P9REN	06h
Port P9 drive strength	P9DS	08h
Port P9 selection	P9SEL	0Ah
Port P10 input	P10IN	01h
Port P10 output	P10OUT	03h
Port P10 direction	P10DIR	05h
Port P10 pullup/pulldown enable	P10REN	07h
Port P10 drive strength	P10DS	09h
Port P10 selection	P10SEL	0Bh

表 8-25. Port P11 Registers (Base Address: 02A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P11 input	P11IN	00h
Port P11 output	P11OUT	02h
Port P11 direction	P11DIR	04h
Port P11 pullup/pulldown enable	P11REN	06h
Port P11 drive strength	P11DS	08h
Port P11 selection	P11SEL	0Ah

表 8-26. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ drive strength	PJDS	08h

表 8-27. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h

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表 8-27. TA0 Registers (Base Address: 0340h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter register	TA0R	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
Capture/compare register 3	TA0CCR3	18h
Capture/compare register 4	TA0CCR4	1Ah
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

表 8-28. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

表 8-29. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 register	TB0R	10h
Capture/compare register 0	TB0CCR0	12h
Capture/compare register 1	TB0CCR1	14h
Capture/compare register 2	TB0CCR2	16h
Capture/compare register 3	TB0CCR3	18h
Capture/compare register 4	TB0CCR4	1Ah
Capture/compare register 5	TB0CCR5	1Ch
Capture/compare register 6	TB0CCR6	1Eh
TB0 expansion register 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

表 8-30. Real Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h

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表 8-30. Real Time Clock Registers (Base Address: 04A0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds/counter register 1	RTCSEC/RTCNT1	10h
RTC minutes/counter register 2	RTCMIN/RTCNT2	11h
RTC hours/counter register 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter register 4	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

表 8-31. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah

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表 8-31. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
MPY32 control register 0	MPY32CTL0	2Ch

表 8-32. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

表 8-33. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA0CTL1	00h
USCI control 0	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

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表 8-34. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

表 8-35. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA1CTL1	00h
USCI control 0	UCA1CTL0	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

表 8-36. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB1CTL1	00h
USCI synchronous control 0	UCB1CTL0	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

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表 8-37. USCI_A2 Registers (Base Address: 0640h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA2CTL1	00h
USCI control 0	UCA2CTL0	01h
USCI baud rate 0	UCA2BR0	06h
USCI baud rate 1	UCA2BR1	07h
USCI modulation control	UCA2MCTL	08h
USCI status	UCA2STAT	0Ah
USCI receive buffer	UCA2RXBUF	0Ch
USCI transmit buffer	UCA2TXBUF	0Eh
USCI LIN control	UCA2ABCTL	10h
USCI IrDA transmit control	UCA2IRTCTL	12h
USCI IrDA receive control	UCA2IRRCTL	13h
USCI interrupt enable	UCA2IE	1Ch
USCI interrupt flags	UCA2IFG	1Dh
USCI interrupt vector word	UCA2IV	1Eh

表 8-38. USCI_B2 Registers (Base Address: 0660h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB2CTL1	00h
USCI synchronous control 0	UCB2CTL0	01h
USCI synchronous bit rate 0	UCB2BR0	06h
USCI synchronous bit rate 1	UCB2BR1	07h
USCI synchronous status	UCB2STAT	0Ah
USCI synchronous receive buffer	UCB2RXBUF	0Ch
USCI synchronous transmit buffer	UCB2TXBUF	0Eh
USCI I2C own address	UCB2I2COA	10h
USCI I2C slave address	UCB2I2CSA	12h
USCI interrupt enable	UCB2IE	1Ch
USCI interrupt flags	UCB2IFG	1Dh
USCI interrupt vector word	UCB2IV	1Eh

表 8-39. USCI_A3 Registers (Base Address: 0680h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA3CTL1	00h
USCI control 0	UCA3CTL0	01h
USCI baud rate 0	UCA3BR0	06h
USCI baud rate 1	UCA3BR1	07h
USCI modulation control	UCA3MCTL	08h
USCI status	UCA3STAT	0Ah
USCI receive buffer	UCA3RXBUF	0Ch
USCI transmit buffer	UCA3TXBUF	0Eh
USCI LIN control	UCA3ABCTL	10h
USCI IrDA transmit control	UCA3IRTCTL	12h
USCI IrDA receive control	UCA3IRRCTL	13h
USCI interrupt enable	UCA3IE	1Ch
USCI interrupt flags	UCA3IFG	1Dh
USCI interrupt vector word	UCA3IV	1Eh

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表 8-40. USCI_B3 Registers (Base Address: 06A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB3CTL1	00h
USCI synchronous control 0	UCB3CTL0	01h
USCI synchronous bit rate 0	UCB3BR0	06h
USCI synchronous bit rate 1	UCB3BR1	07h
USCI synchronous status	UCB3STAT	0Ah
USCI synchronous receive buffer	UCB3RXBUF	0Ch
USCI synchronous transmit buffer	UCB3TXBUF	0Eh
USCI I2C own address	UCB3I2COA	10h
USCI I2C slave address	UCB3I2CSA	12h
USCI interrupt enable	UCB3IE	1Ch
USCI interrupt flags	UCB3IFG	1Dh
USCI interrupt vector word	UCB3IV	1Eh

表 8-41. ADC12_A Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Control register 0	ADC12CTL0	00h
Control register 1	ADC12CTL1	02h
Control register 2	ADC12CTL2	04h
Interrupt-flag register	ADC12IFG	0Ah
Interrupt-enable register	ADC12IE	0Ch
Interrupt-vector-word register	ADC12IV	0Eh
ADC memory-control register 0	ADC12MCTL0	10h
ADC memory-control register 1	ADC12MCTL1	11h
ADC memory-control register 2	ADC12MCTL2	12h
ADC memory-control register 3	ADC12MCTL3	13h
ADC memory-control register 4	ADC12MCTL4	14h
ADC memory-control register 5	ADC12MCTL5	15h
ADC memory-control register 6	ADC12MCTL6	16h
ADC memory-control register 7	ADC12MCTL7	17h
ADC memory-control register 8	ADC12MCTL8	18h
ADC memory-control register 9	ADC12MCTL9	19h
ADC memory-control register 10	ADC12MCTL10	1Ah
ADC memory-control register 11	ADC12MCTL11	1Bh
ADC memory-control register 12	ADC12MCTL12	1Ch
ADC memory-control register 13	ADC12MCTL13	1Dh
ADC memory-control register 14	ADC12MCTL14	1Eh
ADC memory-control register 15	ADC12MCTL15	1Fh
Conversion memory 0	ADC12MEM0	20h
Conversion memory 1	ADC12MEM1	22h
Conversion memory 2	ADC12MEM2	24h
Conversion memory 3	ADC12MEM3	26h
Conversion memory 4	ADC12MEM4	28h
Conversion memory 5	ADC12MEM5	2Ah
Conversion memory 6	ADC12MEM6	2Ch
Conversion memory 7	ADC12MEM7	2Eh
Conversion memory 8	ADC12MEM8	30h
Conversion memory 9	ADC12MEM9	32h

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表 8-41. ADC12_A Registers (Base Address: 0700h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Conversion memory 10	ADC12MEM10	34h
Conversion memory 11	ADC12MEM11	36h
Conversion memory 12	ADC12MEM12	38h
Conversion memory 13	ADC12MEM13	3Ah
Conversion memory 14	ADC12MEM14	3Ch
Conversion memory 15	ADC12MEM15	3Eh

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8.9.18 Input/Output Diagrams

8.9.18.1 Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger

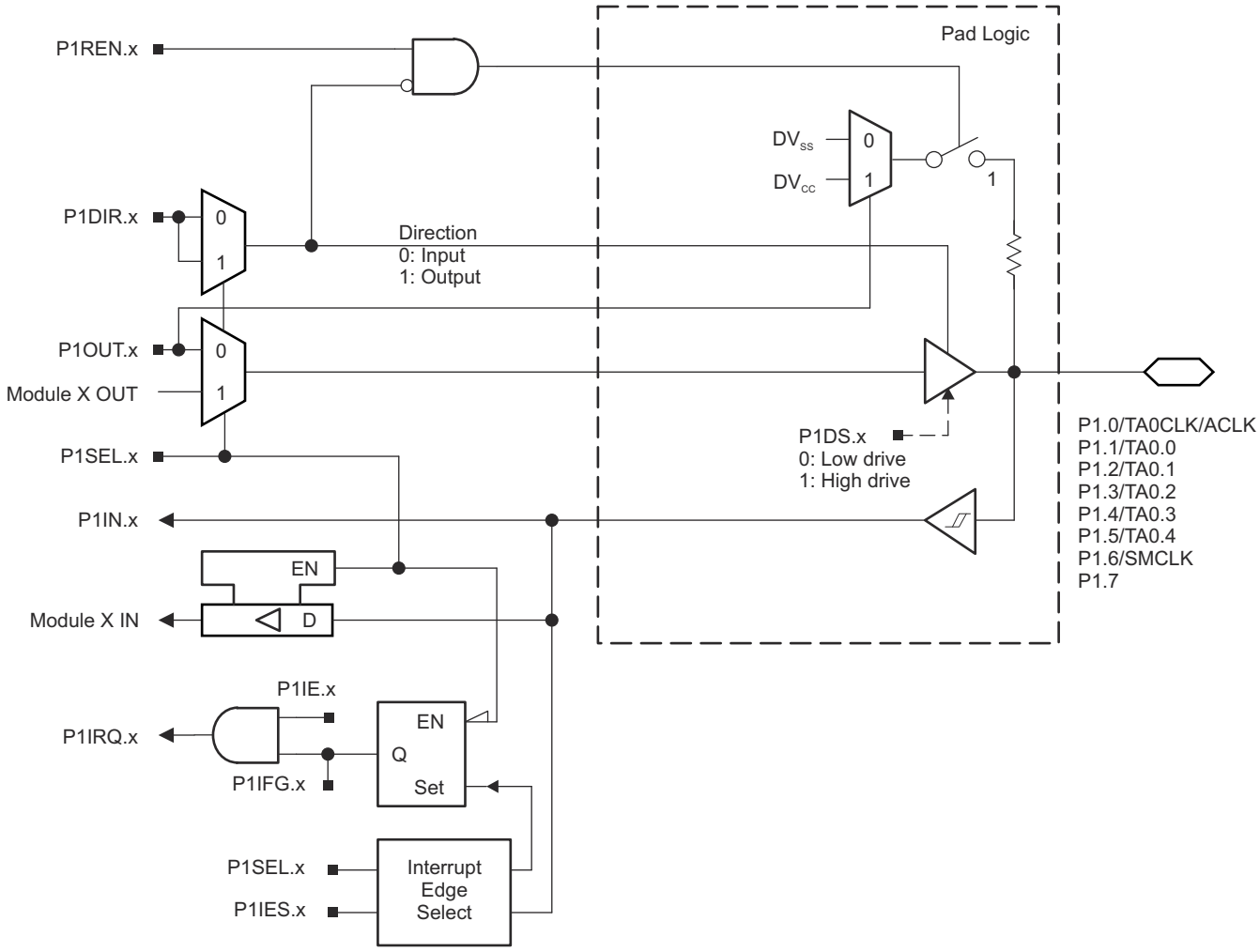

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表 8-42. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		TA0.TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		TA0.CCI2A	0	1
		TA0.2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		TA0.CCI3A	0	1
		TA0.3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		TA0.CCI4A	0	1
		TA0.4	1	1
P1.6/SMCLK	6	P1.6 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P1.7	7	P1.7 (I/O)	I: 0; O: 1	0

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8.9.18.2 Port P2, P2.0 to P2.7, Input/Output With Schmitt Trigger

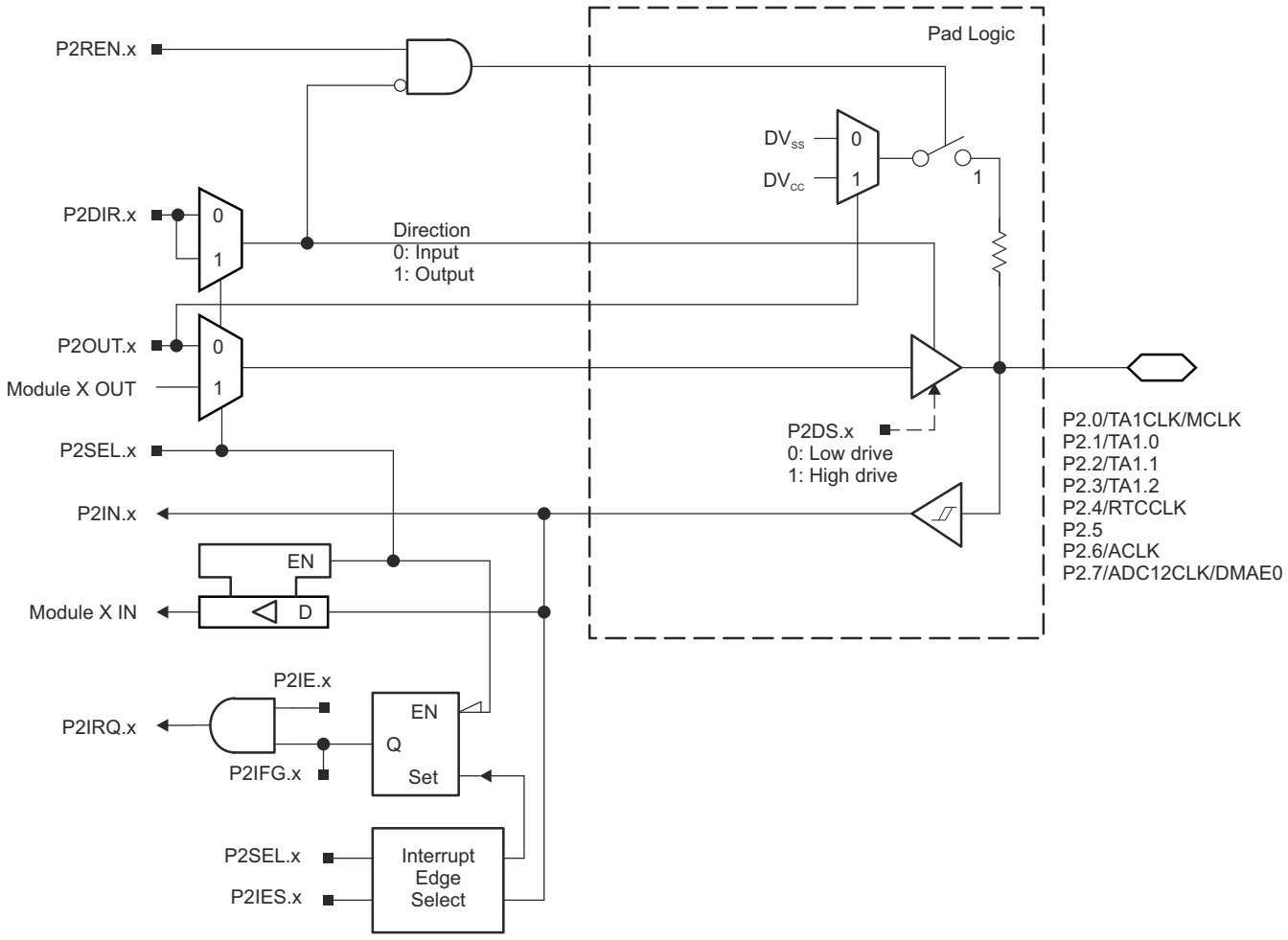

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表 8-43. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P2DIR.x	P2SEL.x
P2.0/TA1CLK/MCLK	0	P2.0 (I/O)	I: 0; O: 1	0
		TA1CLK	0	1
		MCLK	1	1
P2.1/TA1.0	1	P2.1 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.0	1	1
P2.2/TA1.1	2	P2.2 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.1	1	1
P2.3/TA1.2	3	P2.3 (I/O)	I: 0; O: 1	0
		TA1.CCI2A	0	1
		TA1.2	1	1
P2.4/RTCCLK	4	P2.4 (I/O)	I: 0; O: 1	0
		RTCCLK	1	1
P2.5	5	P2.5 (I/O)	I: 0; O: 1	0
P2.6/ACLK	6	P2.6 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P2.7/ADC12CLK/DMAE0	7	P2.7 (I/O)	I: 0; O: 1	0
		DMAE0	0	1
		ADC12CLK	1	1

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8.9.18.3 Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger

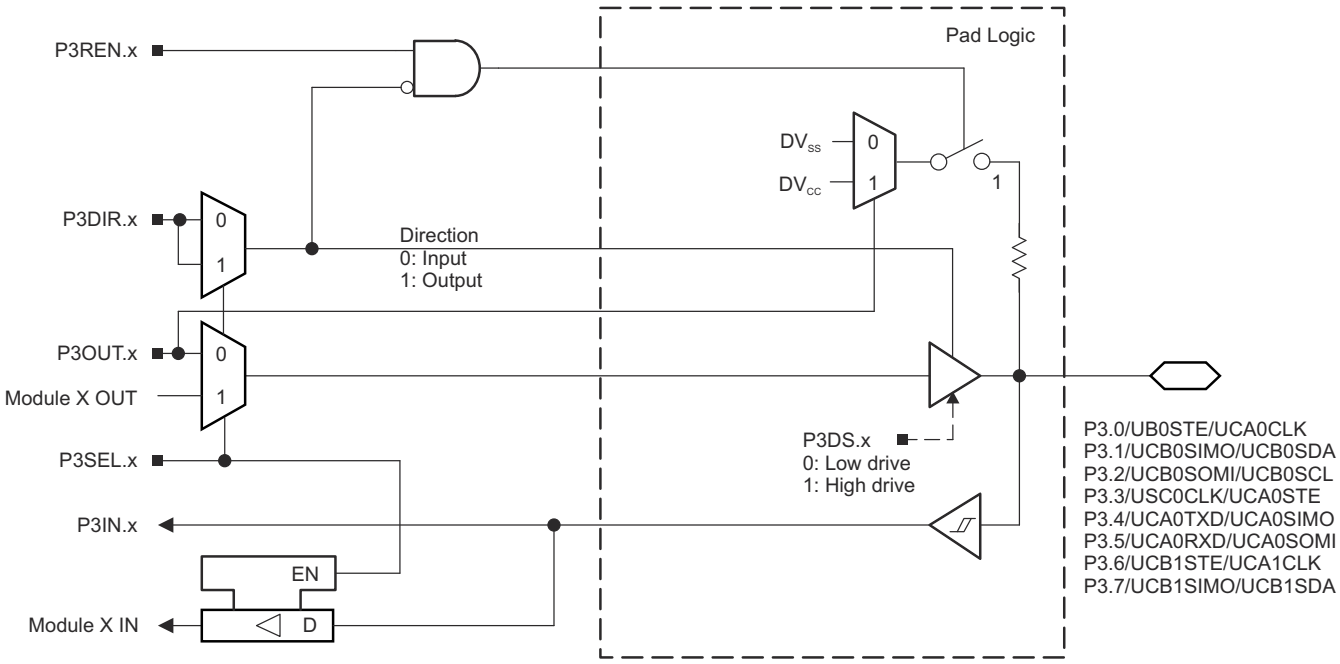

表 8-44. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/UCA0CLK	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK (2) (3)	X	1
P3.1/UCB0SIMO/UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA (2) (4)	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL (2) (4)	X	1
P3.3/UCB0CLK/UCA0STE	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE (2) (5)	X	1
P3.4/UCA0TXD/UCA0SIMO	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO (2)	X	1
P3.5/UCA0RXD/UCA0SOMI	5	P3.5 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI (2)	X	1
P3.6/UCB1STE/UCA1CLK	6	P3.6 (I/O)	I: 0; O: 1	0
		UCB1STE/UCA1CLK (2) (6)	X	1
P3.7/UCB1SIMO/UCB1SDA	7	P3.7 (I/O)	I: 0; O: 1	0
		UCB1SIMO/UCB1SDA (2) (4)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(4) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(5) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(6) UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output, USCI B1 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

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8.9.18.4 Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger

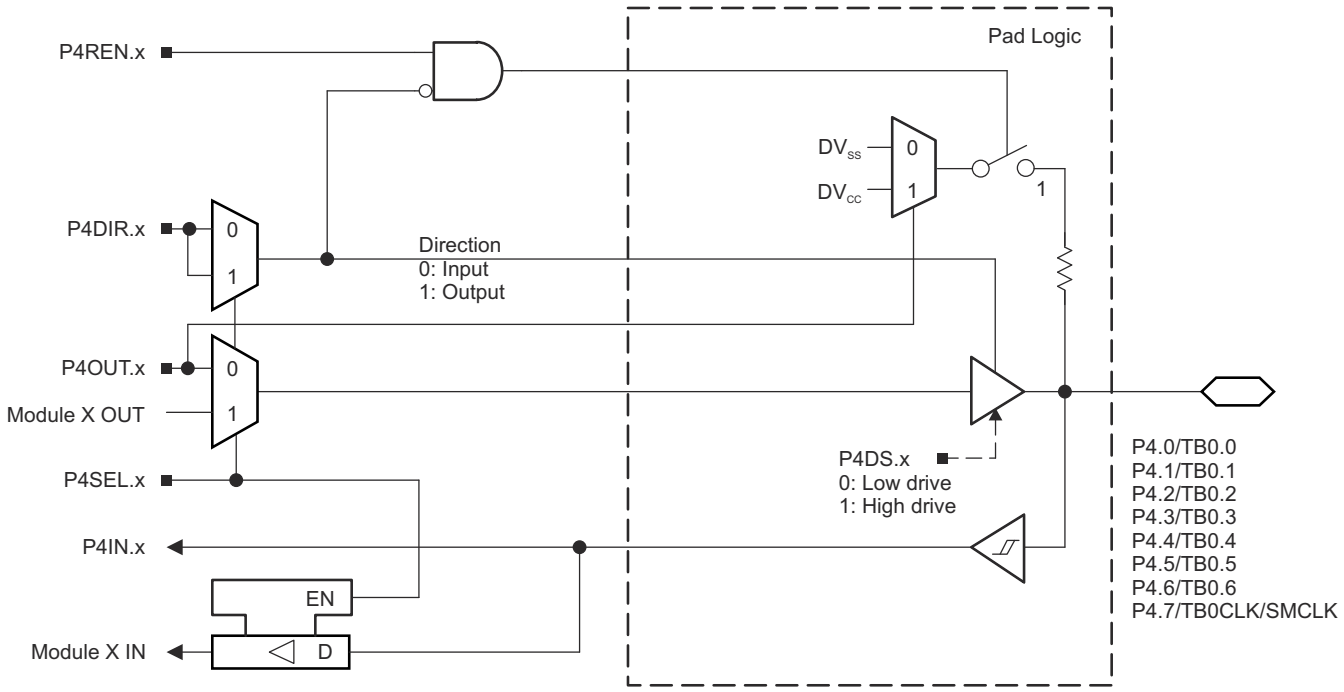

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表 8-45. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0.0	0	4.0 (I/O)	I: 0; O: 1	0
		TB0.CCI0A and TB0.CCI0B	0	1
		TB0.0 (1)	1	1
P4.1/TB0.1	1	4.1 (I/O)	I: 0; O: 1	0
		TB0.CCI1A and TB0.CCI1B	0	1
		TB0.1 (1)	1	1
P4.2/TB0.2	2	4.2 (I/O)	I: 0; O: 1	0
		TB0.CCI2A and TB0.CCI2B	0	1
		TB0.2 (1)	1	1
P4.3/TB0.3	3	4.3 (I/O)	I: 0; O: 1	0
		TB0.CCI3A and TB0.CCI3B	0	1
		TB0.3 (1)	1	1
P4.4/TB0.5	4	4.4 (I/O)	I: 0; O: 1	0
		TB0.CCI4A and TB0.CCI4B	0	1
		TB0.4 (1)	1	1
P4.5/TB0.5	5	4.5 (I/O)	I: 0; O: 1	0
		TB0.CCI5A and TB0.CCI5B	0	1
		TB0.5 (1)	1	1
P4.6/TB0.6	6	4.6 (I/O)	I: 0; O: 1	0
		TB0.CCI6A and TB0.CCI6B	0	1
		TB0.6 (1)	1	1
P4.7/TB0CLK/SMCLK	7	4.7 (I/O)	I: 0; O: 1	0
		TB0CLK	0	1
		SMCLK	1	1

(1) Setting TBOUTH causes all Timer_B configured outputs to be set to high impedance.

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8.9.18.5 Port P5, P5.0 and P5.1, Input/Output With Schmitt Trigger

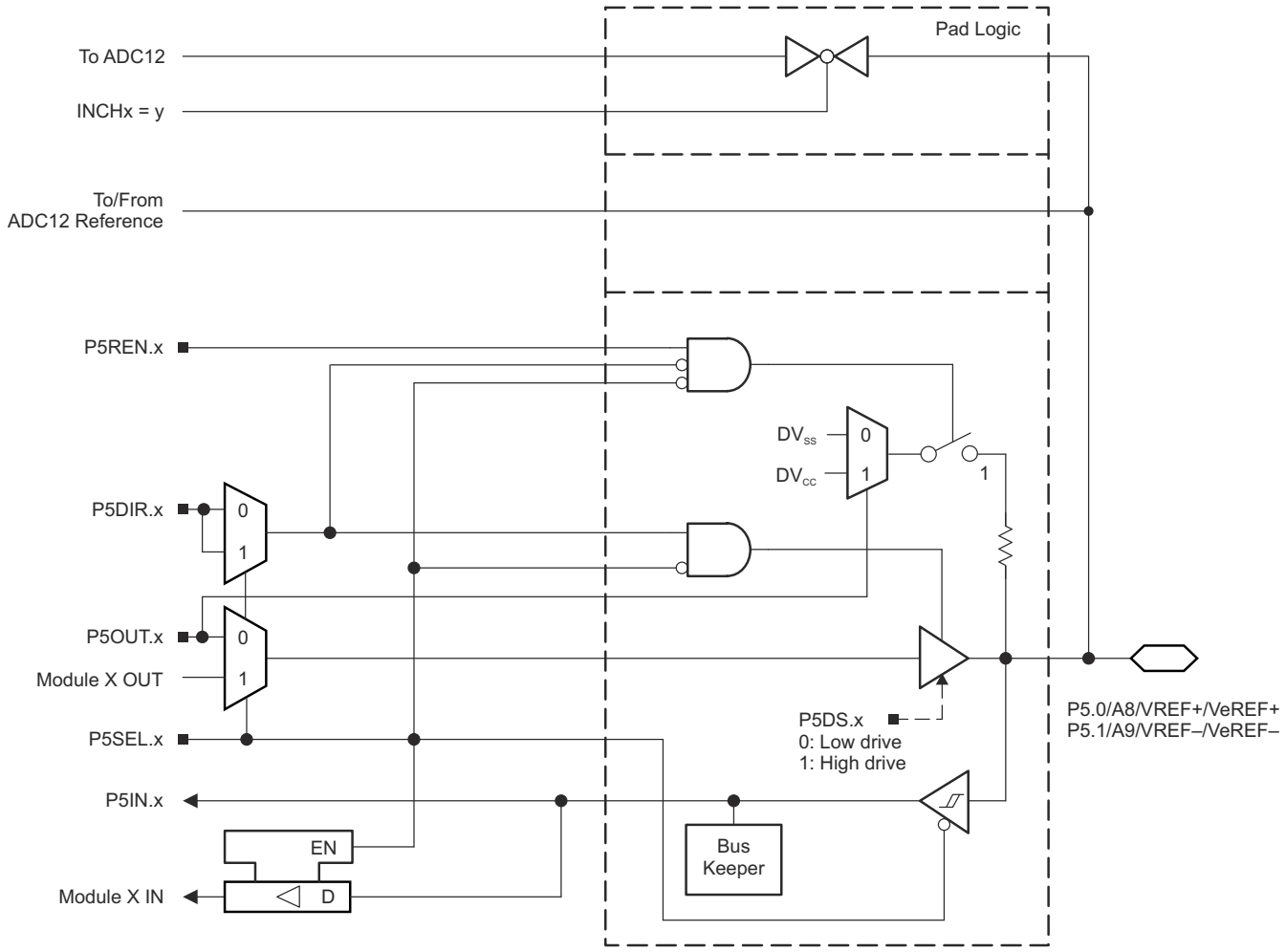

表 8-46. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)		
			P5DIR.x	P5SEL.x	REFOUT
P5.0/A8/VREF+/VeREF+	0	P5.0 (I/O) (2)	I: 0; O: 1	0	X
		A8/VeREF+ (3)	X	1	0
		A8/VREF+ (4)	X	1	1
P5.1/A9/VREF –/VeREF –	1	P5.1 (I/O) (2)	I: 0; O: 1	0	X
		A9/VeREF – (5)	X	1	0
		A9/VREF – (6)	X	1	1

(1) X = Don't care.
(2) Default condition.
(3) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12_A. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.
(4) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF+ reference is available at the pin. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.
(5) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12_A. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.
(6) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF – reference is available at the pin. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.

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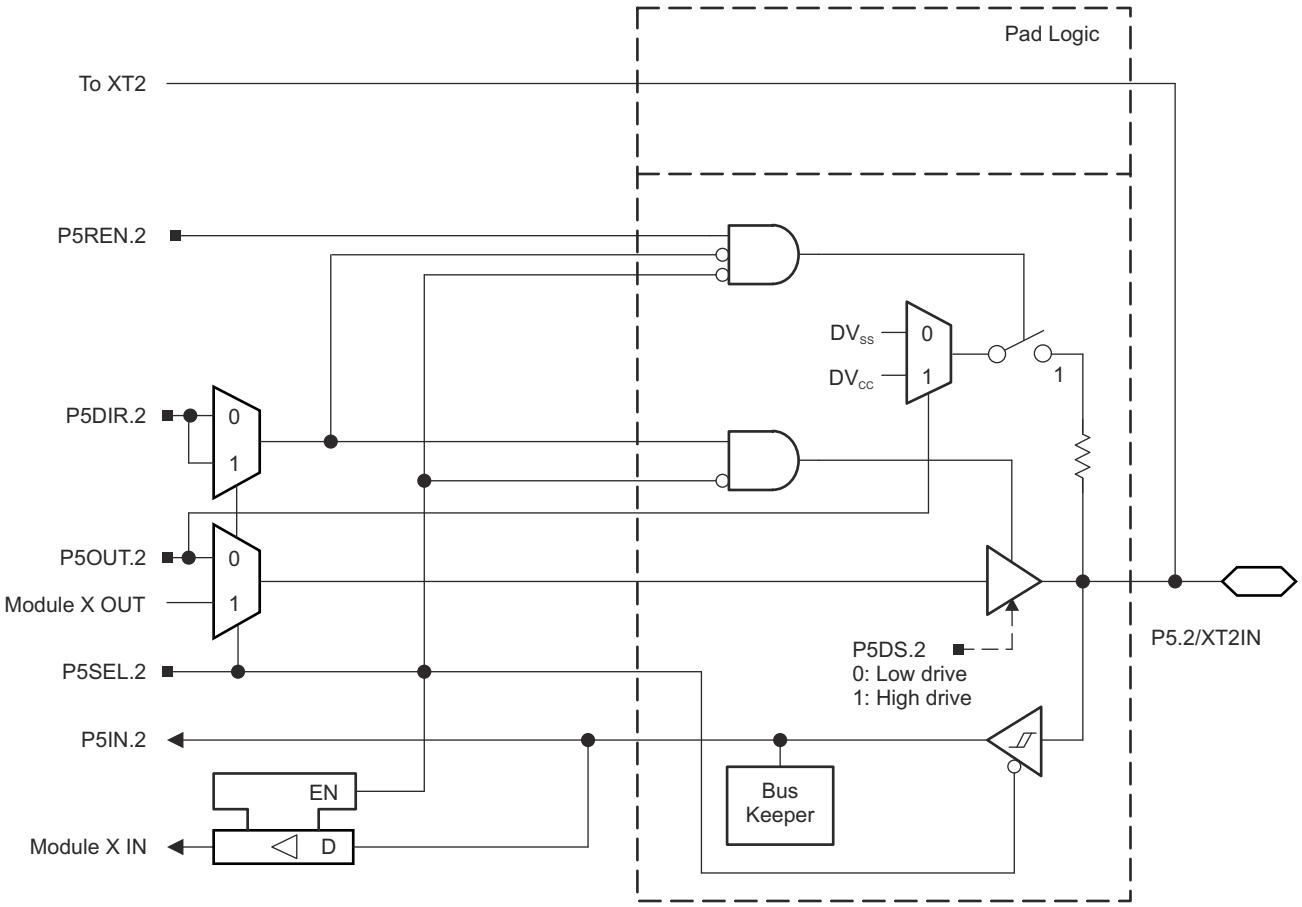
8.9.18.6 Port P5, P5.2, Input/Output With Schmitt Trigger



8.9.18.7 Port P5, P5.3, Input/Output With Schmitt Trigger

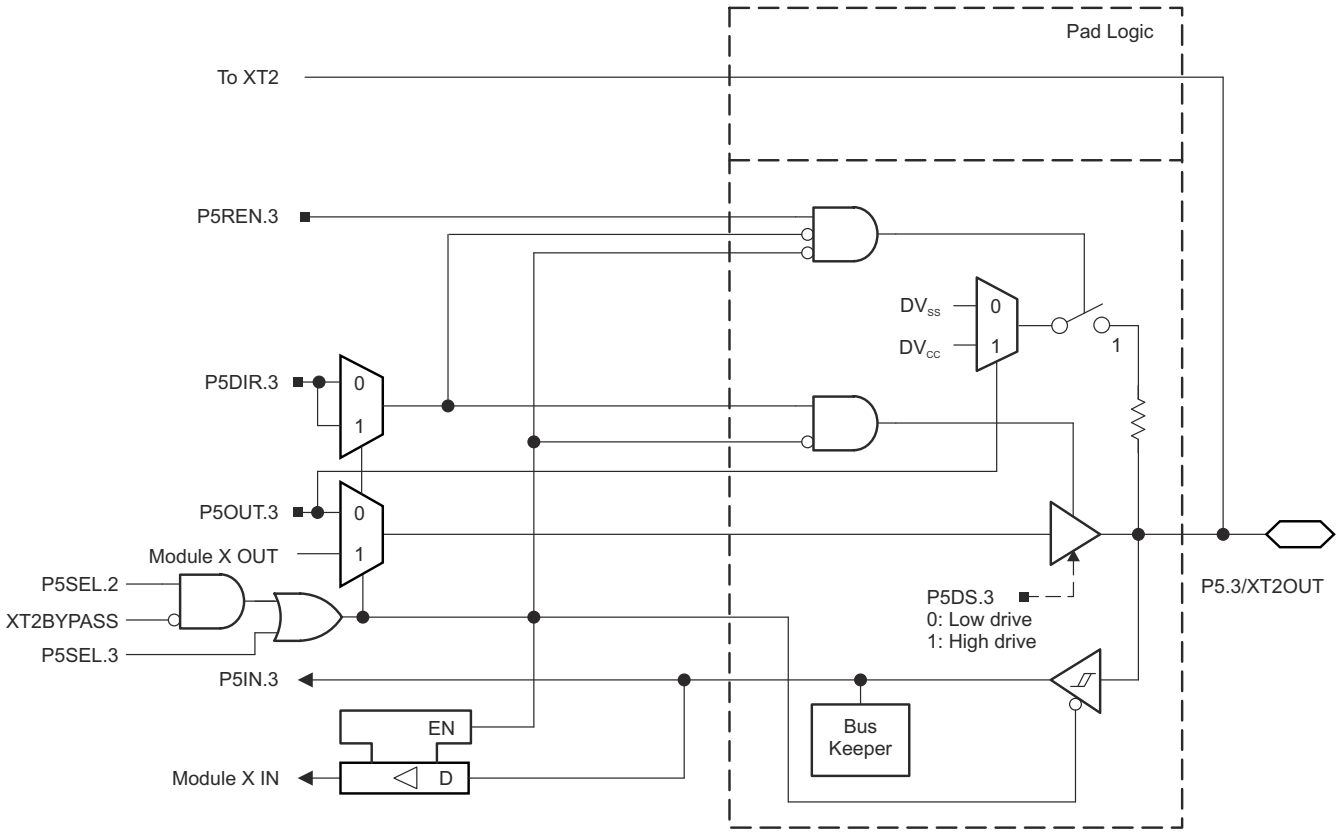


表 8-47. Port P5 (P5.2 and P5.3) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)			
			P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode (2)	X	1	X	0
		XT2IN bypass mode (2)	X	1	X	1
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	X	X
		XT2OUT crystal mode (3)	X	1	X	0
		P5.3 (I/O) (3)	X	1	X	1

(1) X = Don't care
(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

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8.9.18.8 Port P5, P5.4 to P5.7, Input/Output With Schmitt Trigger

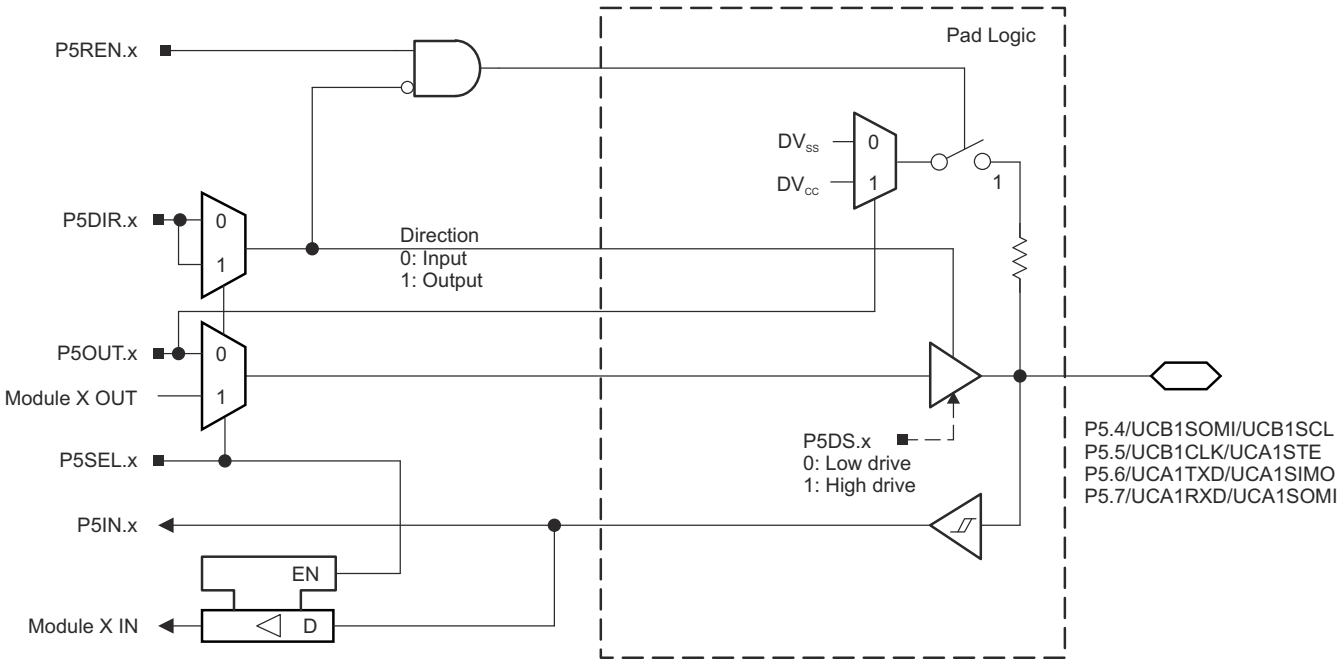

表 8-48. Port P5 (P5.4 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)	
			P5DIR.x	P5SEL.x
P5.4/UCB1SOMI/UCB1SCL	4	P5.4 (I/O)	I: 0; O: 1	0
		UCB1SOMI/UCB1SCL (2) (3)	X	1
P5.5/UCB1CLK/UCA1STE	5	P5.5 (I/O)	I: 0; O: 1	0
		UCB1CLK/UCA1STE (2) (4)	X	1
P5.6/UCA1TXD/UCA1SIMO	6	P5.6 (I/O)	I: 0; O: 1	0
		UCA1TXD/UCA1SIMO (2)	X	1
P5.7/UCA1RXD/UCA1SOMI	7	P5.7 (I/O)	I: 0; O: 1	0
		UCA1RXD/UCA1SOMI (2)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(4) UCB1CLK function takes precedence over UCA1STE function. If the pin is required as UCB1CLK input or output, USCI A1 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

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8.9.18.9 Port P6, P6.0 to P6.7, Input/Output With Schmitt Trigger

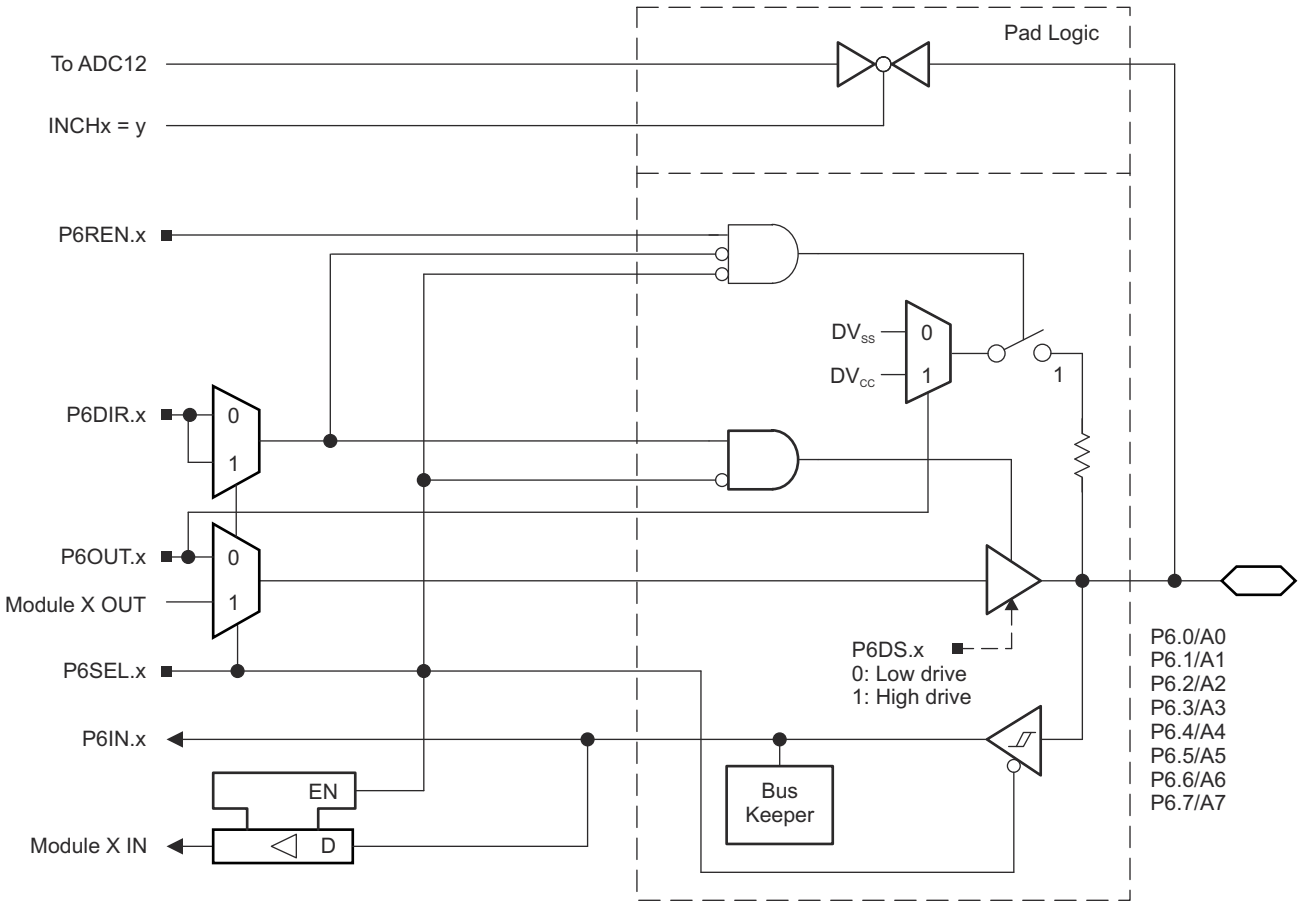

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表 8-49. Port P6 (P6.0 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)		
			P6DIR.x	P6SEL.x	INCHx
P6.0/A0	0	P6.0 (I/O)	I: 0; O: 1	0	X
		A0 (2) (3)	X	X	0
P6.1/A1	1	P6.1 (I/O)	I: 0; O: 1	0	X
		A1 (2) (3)	X	X	1
P6.2/A2	2	P6.2 (I/O)	I: 0; O: 1	0	X
		A2 (2) (3)	X	X	2
P6.3/A3	3	P6.3 (I/O)	I: 0; O: 1	0	X
		A3 (2) (3)	X	X	3
P6.4/A4	4	P6.4 (I/O)	I: 0; O: 1	0	X
		A4 (1) (2) (3)	X	X	4
P6.5/A5	5	P6.5 (I/O)	I: 0; O: 1	0	X
		A5 (2) (3)	X	X	5
P6.6/A6	6	P6.6 (I/O)	I: 0; O: 1	0	X
		A6 (2) (3)	X	X	6
P6.7/A7	7	P6.7 (I/O)	I: 0; O: 1	0	X
		A7 (2) (3)	X	X	7

(1) X = Don't care
(2) Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected via the respective INCHx bits.

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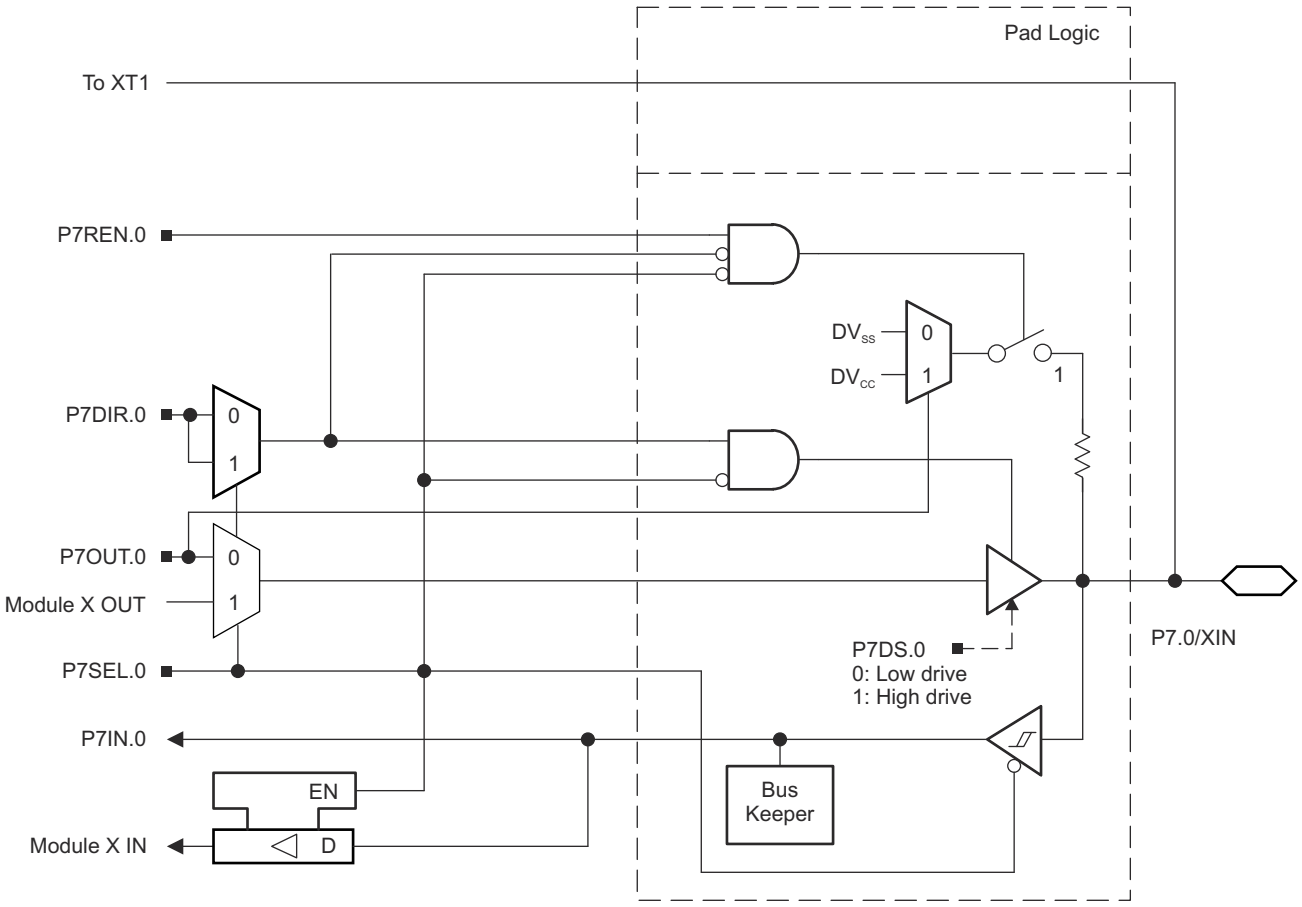
8.9.18.10 Port P7, P7.0, Input/Output With Schmitt Trigger



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8.9.18.11 Port P7, P7.1, Input/Output With Schmitt Trigger

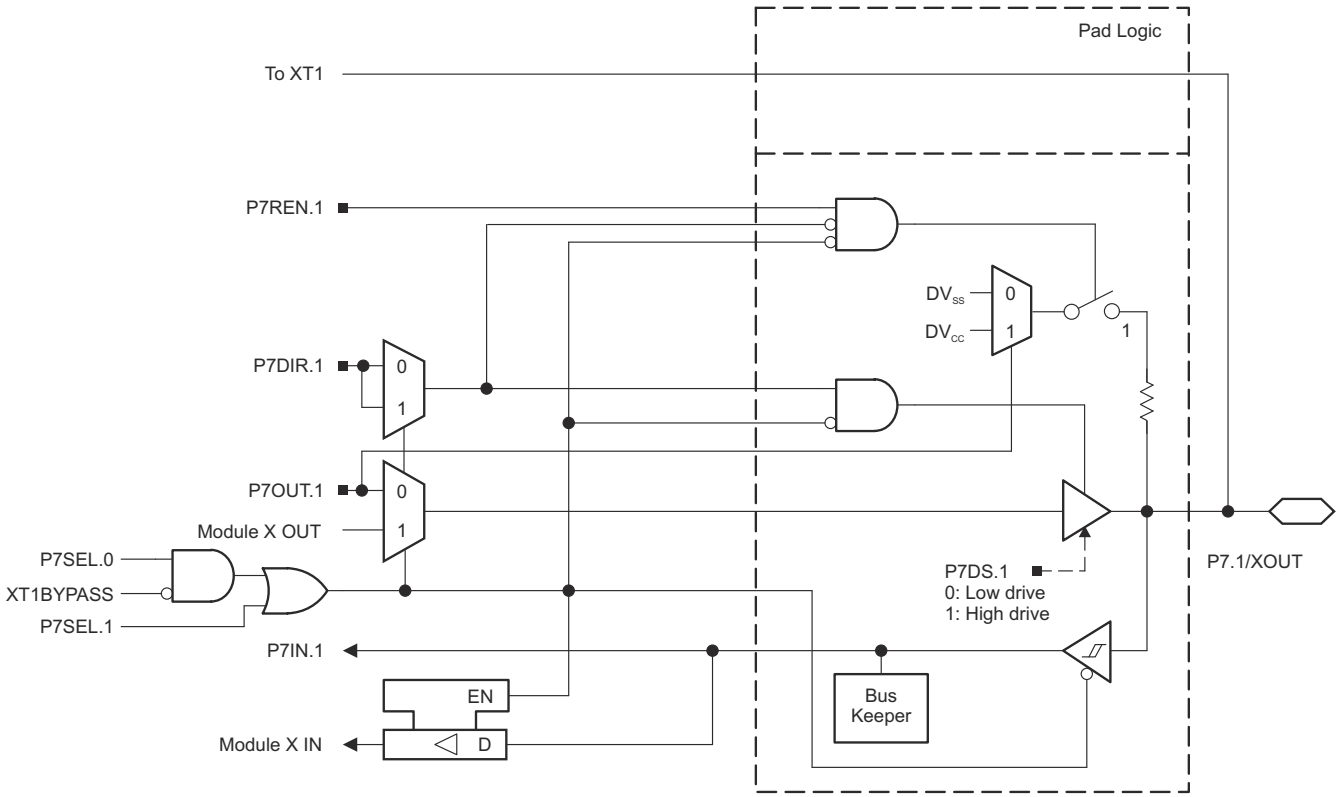

表 8-50. Port P7 (P7.0 and P7.1) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)			
			P7DIR.x	P7SEL.0	P7SEL.1	XT1BYPASS
P7.0/XIN	0	P7.0 (I/O)	I: 0; O: 1	0	X	X
		XIN crystal mode (2)	X	1	X	0
		XIN bypass mode (2)	X	1	X	1
P7.1/XOUT	1	P7.1 (I/O)	I: 0; O: 1	0	X	X
		XOUT crystal mode (3)	X	1	X	0
		P7.1 (I/O) (3)	X	1	X	1

(1) X = Don't care
(2) Setting P7SEL.0 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P7.0 is configured for crystal mode or bypass mode.
(3) Setting P7SEL.0 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P7.1 can be used as general-purpose I/O.

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8.9.18.12 Port P7, P7.2 and P7.3, Input/Output With Schmitt Trigger

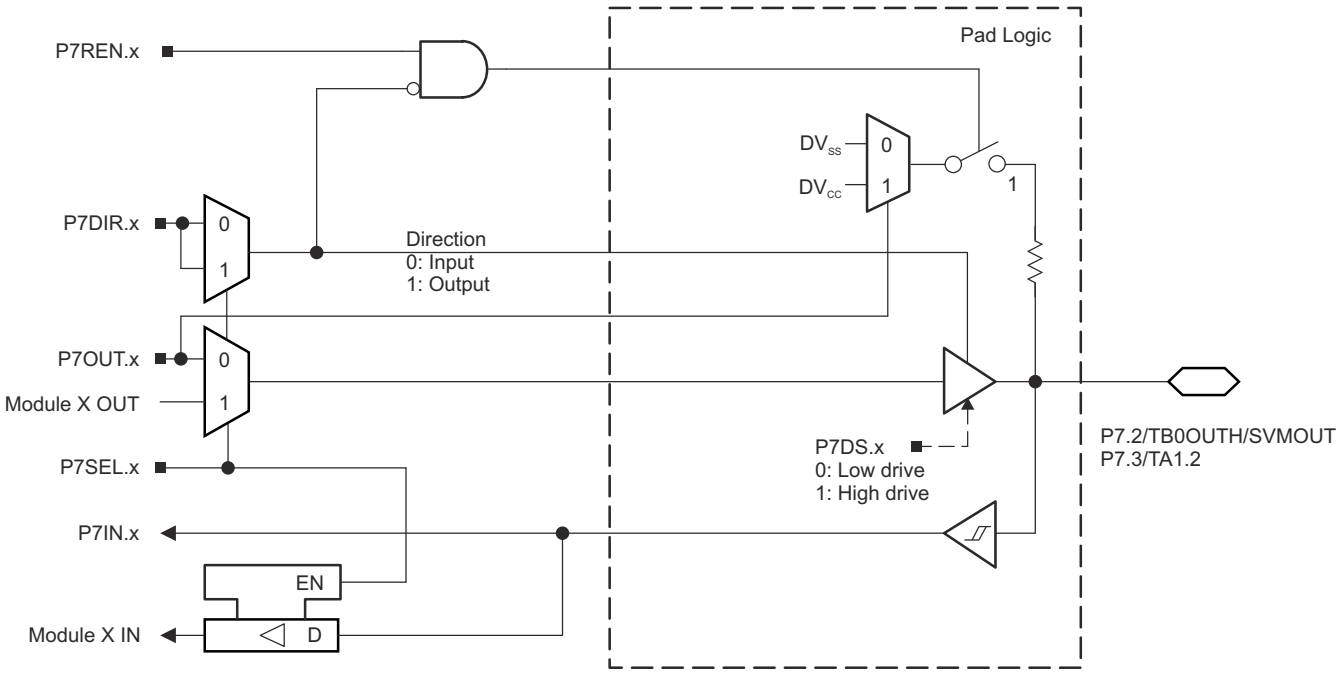

表 8-51. Port P7 (P7.2 and P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P7DIR.x	P7SEL.x
P7.2/TB0OUTH/SVMOUT	2	P7.2 (I/O)	I: 0; O: 1	0
		TB0OUTH	0	1
		SVMOUT	1	1
P7.3/TA1.2	3	P7.3 (I/O)	I: 0; O: 1	0
		TA1.CCI2B	0	1
		TA1.2	1	1

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8.9.18.13 Port P7, P7.4 to P7.7, Input/Output With Schmitt Trigger

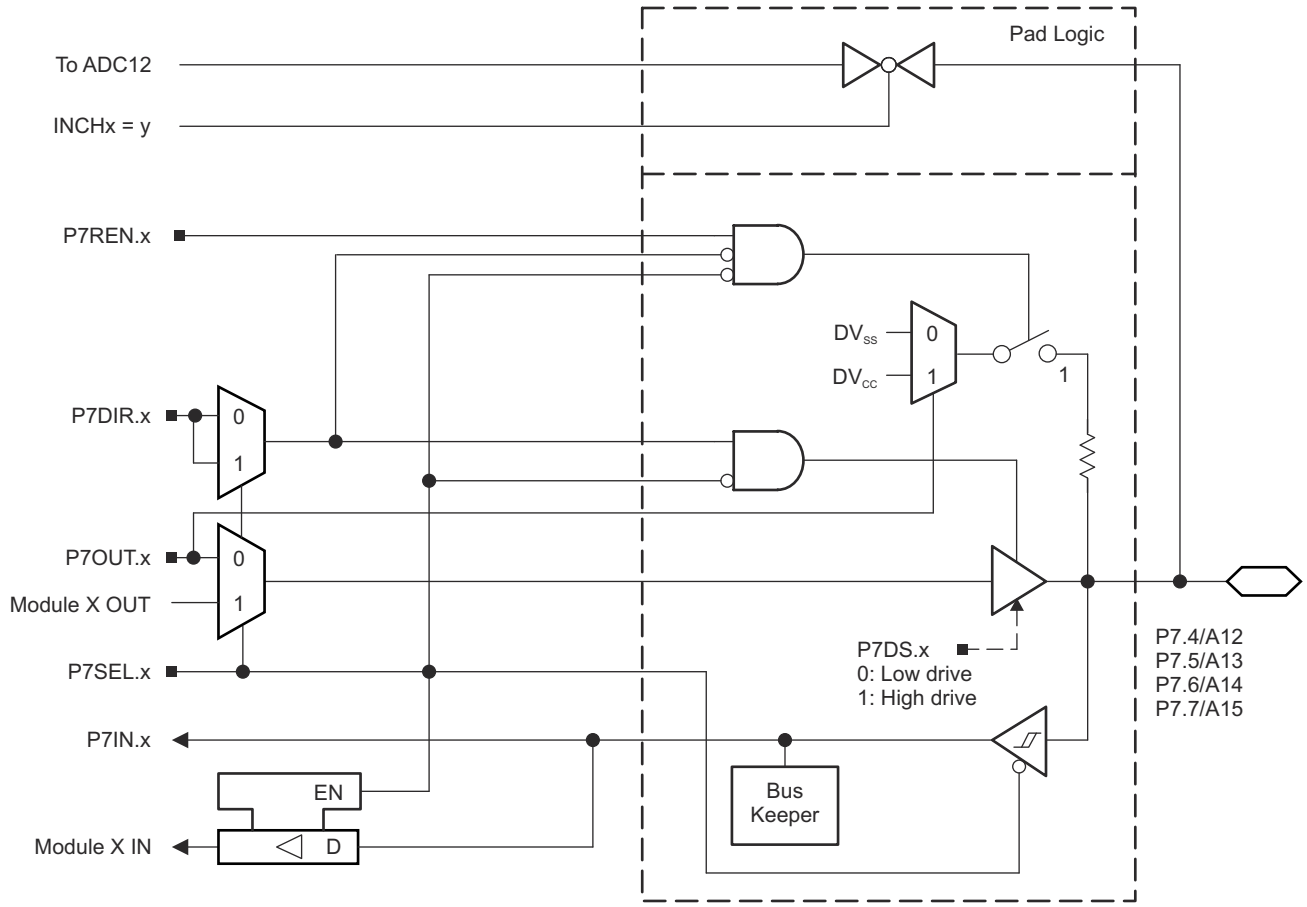

表 8-52. Port P7 (P7.4 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)		
			P7DIR.x	P7SEL.x	INCHx
P7.4/A12	4	P7.4 (I/O)	I: 0; O: 1	0	X
		A12 (2) (3)	X	X	12
P7.5/A13	5	P7.5 (I/O)	I: 0; O: 1	0	X
		A13 (2) (3)	X	X	13
P7.6/A14	6	P7.6 (I/O)	I: 0; O: 1	0	X
		A14 (2) (3)	X	X	14
P7.7/A15	7	P7.7 (I/O)	I: 0; O: 1	0	X
		A15 (2) (3)	X	X	15

(1) X = Don't care
(2) Setting the P7SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected via the respective INCHx bits.

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8.9.18.14 Port P8, P8.0 to P8.7, Input/Output With Schmitt Trigger

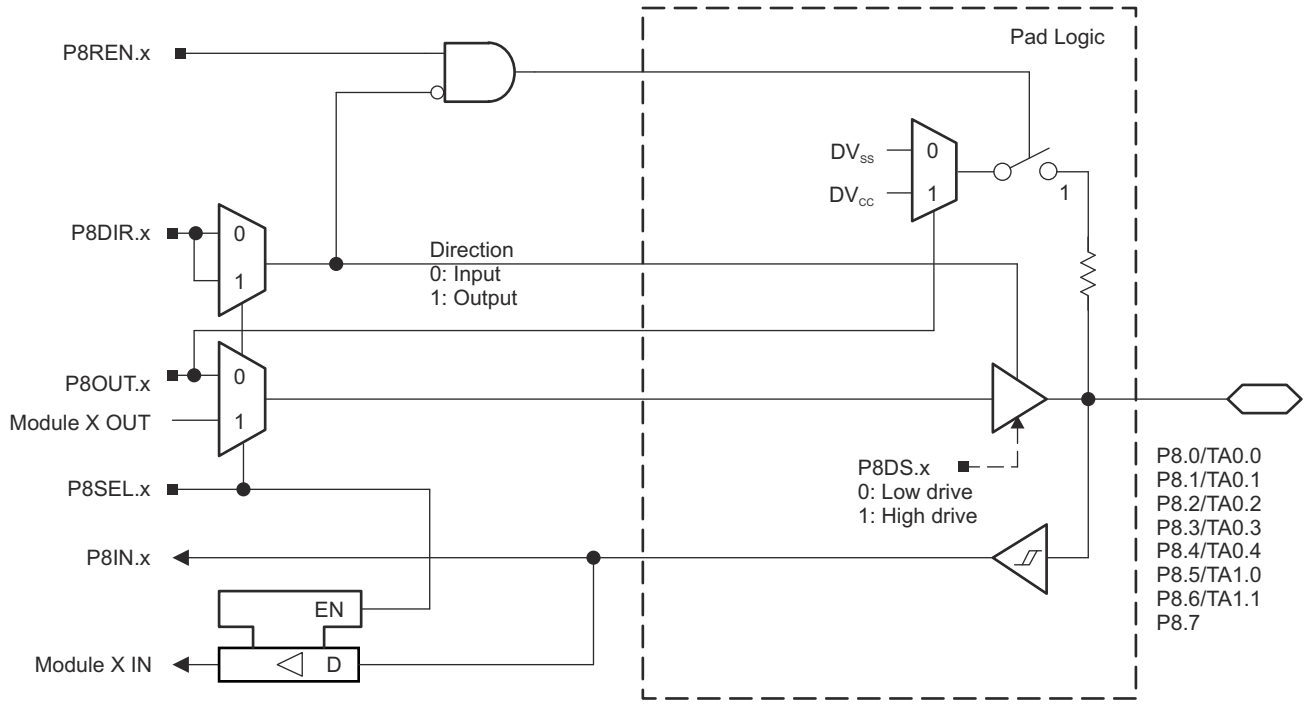

表 8-53. Port P8 (P8.0 to P8.7) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P8DIR.x	P8SEL.x
P8.0/TA0.0	0	P8.0 (I/O)	I: 0; O: 1	0
		TA0.CCI0B	0	1
		TA0.0	1	1
P8.1/TA0.1	1	P8.1 (I/O)	I: 0; O: 1	0
		TA0.CCI1B	0	1
		TA0.1	1	1
P8.2/TA0.2	2	P8.2 (I/O)	I: 0; O: 1	0
		TA0.CCI2B	0	1
		TA0.2	1	1
P8.3/TA0.3	3	P8.3 (I/O)	I: 0; O: 1	0
		TA0.CCI3B	0	1
		TA0.3	1	1
P8.4/TA0.4	4	P8.4 (I/O)	I: 0; O: 1	0
		TA0.CCI4B	0	1
		TA0.4	1	1
P8.5/TA1.0	5	P8.5 (I/O)	I: 0; O: 1	0
		TA1.CCI0B	0	1
		TA1.0	1	1
P8.6/TA1.1	6	P8.6 (I/O)	I: 0; O: 1	0
		TA1.CCI1B	0	1
		TA1.1	1	1
P8.7	7	P8.7 (I/O)	I: 0; O: 1	0

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8.9.18.15 Port P9, P9.0 to P9.7, Input/Output With Schmitt Trigger

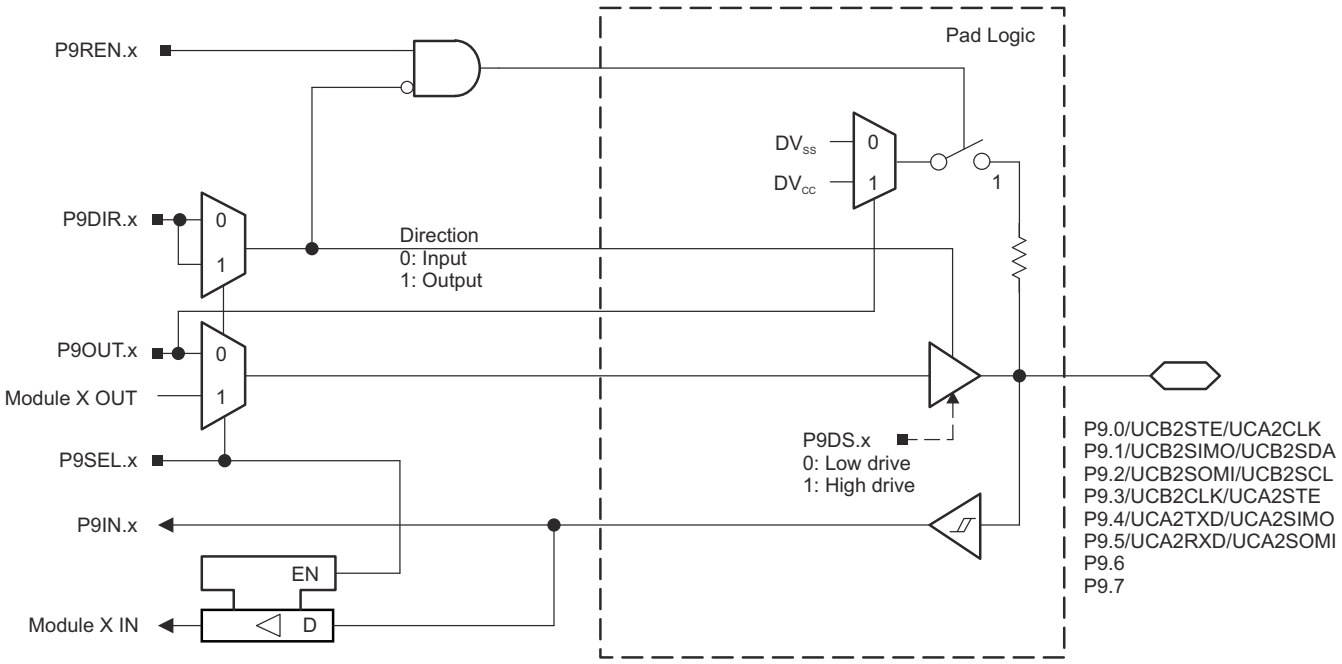

表 8-54. Port P9 (P9.0 to P9.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)	
			P9DIR.x	P9SEL.x
P9.0/UCB2STE/UCA2CLK	0	P9.0 (I/O)	I: 0; O: 1	0
		UCB2STE/UCA2CLK (2) (3)	X	1
P9.1/UCB2SIMO/UCB2SDA	1	P9.1 (I/O)	I: 0; O: 1	0
		UCB2SIMO/UCB2SDA (2) (4)	X	1
P9.2/UCB2SOMI/UCB2SCL	2	P9.2 (I/O)	I: 0; O: 1	0
		UCB2SOMI/UCB2SCL (2) (4)	X	1
P9.3/UCB2CLK/UCA2STE	3	P9.3 (I/O)	I: 0; O: 1	0
		UCB2CLK/UCA2STE (2) (5)	X	1
P9.4/UCA2TXD/UCA2SIMO	4	P9.4 (I/O)	I: 0; O: 1	0
		UCA2TXD/UCA2SIMO (2)	X	1
P9.5/UCA2RXD/UCA2SOMI	5	P9.5 (I/O)	I: 0; O: 1	0
		UCA2RXD/UCA2SOMI (2)	X	1
P9.6	6	P9.6 (I/O)	I: 0; O: 1	0
P9.7	7	P9.7 (I/O)	I: 0; O: 1	0

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA2CLK function takes precedence over UCB2STE function. If the pin is required as UCA2CLK input or output, USCI B2 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(5) UCB2CLK function takes precedence over UCA2STE function. If the pin is required as UCB2CLK input or output, USCI A2 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

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8.9.18.16 Port P10, P10.0 to P10.7, Input/Output With Schmitt Trigger

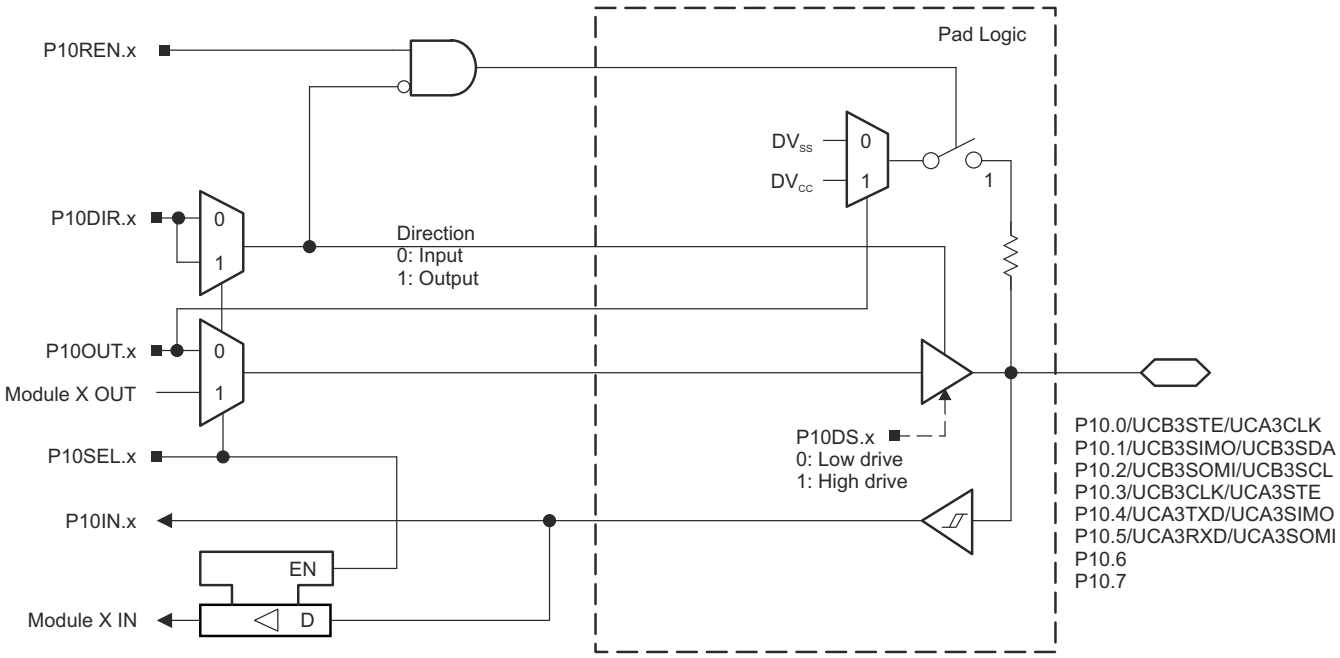

表 8-55. Port P10 (P10.0 to P10.7) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)	
			P10DIR.x	P10SEL.x
P10.0/UCB3STE/UCA3CLK	0	P10.0 (I/O)	I: 0; O: 1	0
		UCB3STE/UCA3CLK (2) (3)	X	1
P10.1/UCB3SIMO/UCB3SDA	1	P10.1 (I/O)	I: 0; O: 1	0
		UCB3SIMO/UCB3SDA (2) (4)	X	1
P10.2/UCB3SOMI/UCB3SCL	2	P10.2 (I/O)	I: 0; O: 1	0
		UCB3SOMI/UCB3SCL (2) (4)	X	1
P10.3/UCB3CLK/UCA3STE	3	P10.3 (I/O)	I: 0; O: 1	0
		UCB3CLK/UCA3STE (2) (5)	X	1
P10.4/UCA3TXD/UCA3SIMO	4	P10.4 (I/O)	I: 0; O: 1	0
		UCA3TXD/UCA3SIMO (2)	X	1
P10.5/UCA3RXD/UCA3SOMI	5	P10.5 (I/O)	I: 0; O: 1	0
		UCA3RXD/UCA3SOMI (2)	X	1
P10.6	6	P10.6 (I/O)	I: 0; O: 1	0
		Reserved (6)	X	1
P10.7	7	P10.7 (I/O)	I: 0; O: 1	0
		Reserved (6)	x	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA3CLK function takes precedence over UCB3STE function. If the pin is required as UCA3CLK input or output, USCI B3 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(5) UCB3CLK function takes precedence over UCA3STE function. If the pin is required as UCB3CLK input or output, USCI A3 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(6) The secondary function on these pins are reserved for factory test purposes. Application should keep the P10SEL.x of these ports cleared to prevent potential conflicts with the application.

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8.9.18.17 Port P11, P11.0 to P11.2, Input/Output With Schmitt Trigger

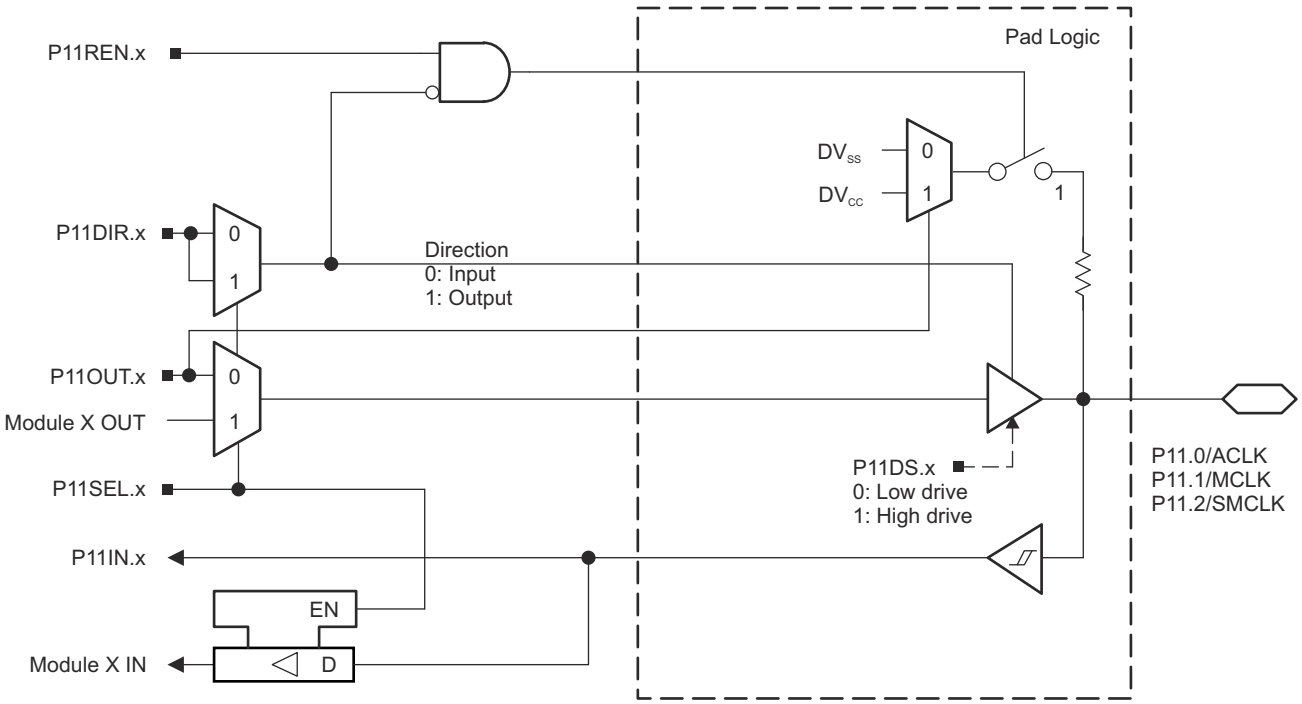

表 8-56. Port P11 (P11.0 to P11.2) Pin Functions

PIN NAME (P11.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P11DIR.x	P11SEL.x
P11.0/ACLK	0	P11.0 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P11.1/MCLK	1	P11.1 (I/O)	I: 0; O: 1	0
		MCLK	1	1
P11.2/SMCLK	2	P11.2 (I/O)	I: 0; O: 1	0
		SMCLK	1	1

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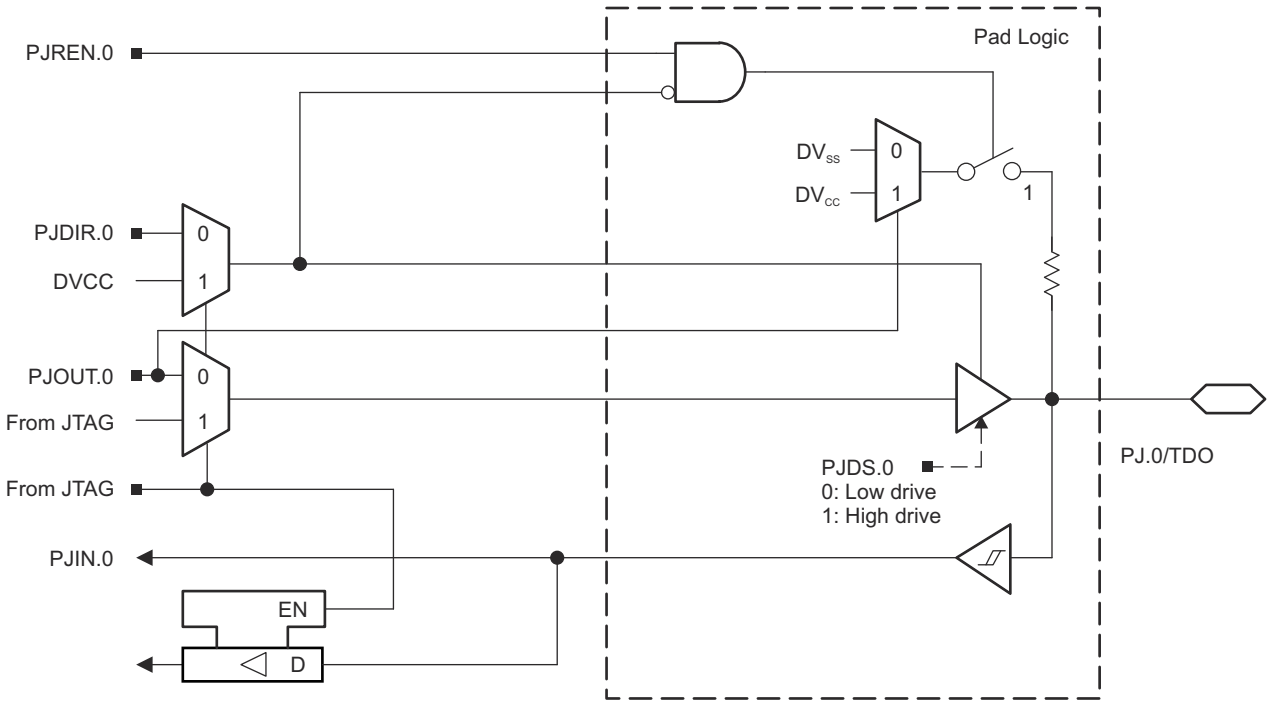
8.9.18.18 Port J, J.0 JTAG Pin TDO, Input/Output With Schmitt Trigger or Output



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8.9.18.19 Port J, J.1 to J.3 JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

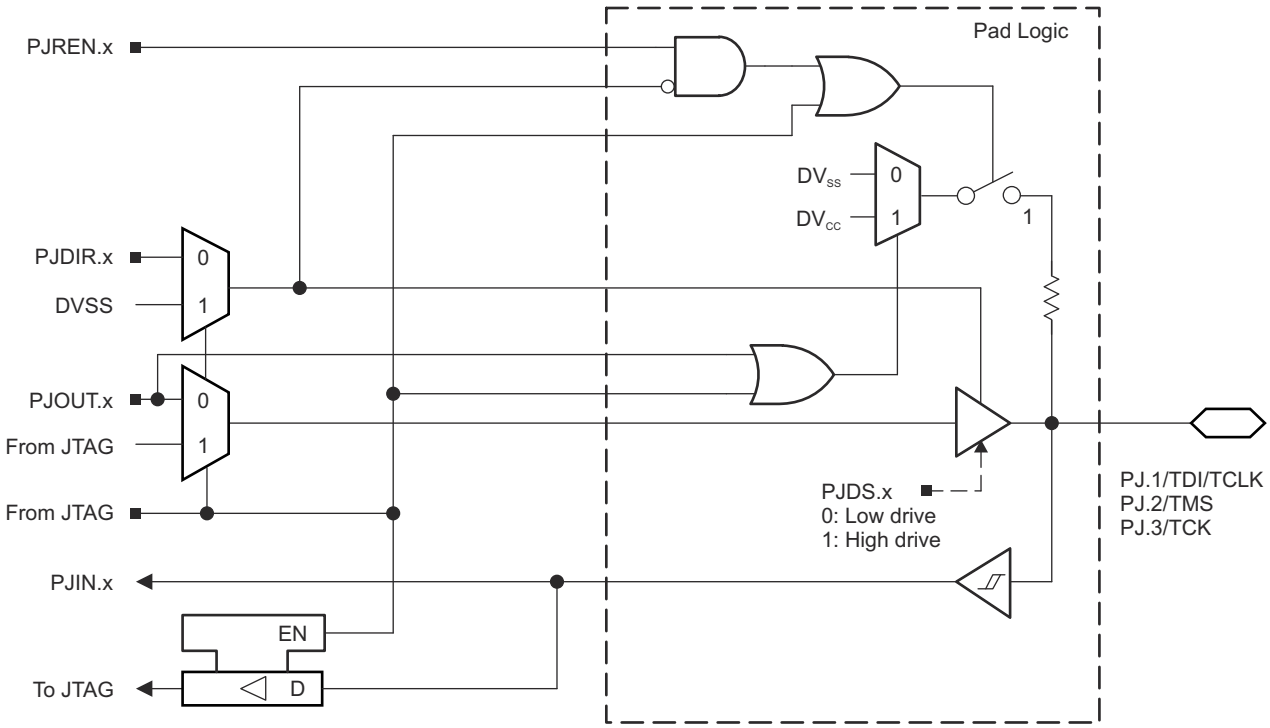

表 8-57. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS (1)
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O) (2)	I: 0; O: 1
		TDO (3)	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O) (2)	I: 0; O: 1
		TDI/TCLK (3) (4)	X
PJ.2/TMS	2	PJ.2 (I/O)(2)	I: 0; O: 1
		TMS (3) (4)	X
PJ.3/TCK	3	PJ.3 (I/O) (2)	I: 0; O: 1
		TCK (3) (4)	X

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

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8.10 Device Descriptors (TLV)

表 8-58 lists the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

表 8-58. Device Descriptors(1)

	DESCRIPTION	ADDRESS	SIZE (bytes)	VALUE
Info Block	Info length	01A00h	1	06h
	CRC length	01A01h	1	06h
	CRC value	01A02h	2	per unit
	Device ID	01A04h	1	05h
	Device ID	01A05h	1	80h
	Hardware revision	01A06h	1	per unit
	Firmware revision	01A07h	1	per unit
Die Record	Die Record Tag	01A08h	1	08h
	Die Record length	01A09h	1	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit
	Die X position	01A0Eh	2	per unit
	Die Y position	01A10h	2	per unit
	Test results	01A12h	2	per unit
ADC12 Calibration	ADC12 Calibration Tag	01A14h	1	11h
	ADC12 Calibration length	01A15h	1	10h
	ADC Gain Factor	01A16h	2	per unit
	ADC Offset	01A18h	2	per unit
	ADC 1.5-V ReferenceTemp. Sensor 30°C	01A1Ah	2	per unit
	ADC 1.5-V ReferenceTemp. Sensor 85°C	01A1Ch	2	per unit
	ADC 2.0-V ReferenceTemp. Sensor 30°C	01A1Eh	2	per unit
	ADC 2.0-V ReferenceTemp. Sensor 85°C	01A20h	2	per unit
	ADC 2.5-V ReferenceTemp. Sensor 30°C	01A22h	2	per unit
	ADC 2.5-V ReferenceTemp. Sensor 85°C	01A24h	2	per unit
REF Calibration	REF Calibration Tag	01A26h	1	12h
	REF Calibration length	01A27h	1	06h
	REF 1.5-V Reference	01A28h	2	per unit
	REF 2.0-V Reference	01A2Ah	2	per unit
	REF 2.5-V Reference	01A2Ch	2	per unit

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表 8-58. Device Descriptors[1] (continued)

	DESCRIPTION	ADDRESS	SIZE (bytes)	VALUE
Peripheral Descriptor	Peripheral Descriptor Tag	01A2Eh	1	02h
	Peripheral Descriptor Length	01A2Fh	1	61h
	Memory 1		2	08h8Ah
	Memory 2		2	0Ch86h
	Memory 3		2	0Eh30h
	Memory 4		2	2Eh98h
	Memory 5		0/1	NA
	delimiter		1	00h
	Peripheral count		1	21h
	MSP430CPUXV2		2	00h23h
	SBW		2	00h0Fh
	EEM-8		2	00h05h
	TI BSL		2	00hFCh
	Package		2	00h1Fh
	SFR		2	10h41h
	PMM		2	02h30h
	FCTL		2	02h38h
	CRC16-straight		2	01h3Ch
	CRC16-bit reversed		2	00h3Dh
	RAMCTL		2	00h44h
	WDT_A		2	00h40h
	UCS		2	01h48h
	SYS		2	02h42h
	REF		2	03hA0h
	Port 1/2		2	05h51h
	Port 3/4		2	02h52h
	Port 5/6		2	02h53h
	Port 7/8		2	02h54h
	Port 9/10		2	02h55h
	Port 11/12		2	02h56h
	JTAG		2	08h5Fh
	TA0		2	02h62h
	TA1		2	04h61h
	TB0		2	04h67h
	RTC		2	0Eh68h
	MPY32		2	02h85h
	DMA-3		2	04h47h
	USCI_A/B		2	0Ch90h
	USCI_A/B		2	04h90h
	USCI_A/B		2	04h90h
	USCI_A/B		2	04h90h
	ADC12_A		2	08hD1h

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表 8-58. Device Descriptors(1) (continued)

	DESCRIPTION	ADDRESS	SIZE (bytes)	VALUE
Interrupts	TB0.CCIFG0		1	64h
	TB0.CCIFG1..6		1	65h
	WDTIFG		1	40h
	USCI_A0		1	90h
	USCI_B0		1	91h
	ADC12_A		1	D0h
	TA0.CCIFG0		1	60h
	TA0.CCIFG1..4		1	61h
	USCI_A2		1	94h
	USCI_B2		1	95h
	DMA		1	46h
	TA1.CCIFG0		1	62h
	TA1.CCIFG1..2		1	63h
	P1		1	50h
	USCI_A1		1	92h
	USCI_B1		1	93h
	USCI_A3		1	96h
	USCI_B3		1	97h
	P2		1	51h
	RTC_A		1	68h
	delimiter		1	00h

(1) NA = Not applicable.

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所有商标均为其各自所有者的财产。

9.2 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M430F5438AMGCARET	Active	Production	NFBGA (GCA) | 113	2500 | LARGE T&R	No	Call TI	Call TI	-55 to 125	MF5438AMET
M430F5438AMGCARET.A	Active	Production	NFBGA (GCA) | 113	2500 | LARGE T&R	No	Call TI	Call TI	-55 to 125	MF5438AMET
M430F5438AMZCARET	Active	Production	NFBGA (ZCA) | 113	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-55 to 125	MF5438AQET
M430F5438AMZCARET.A	Active	Production	NFBGA (ZCA) | 113	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-55 to 125	MF5438AQET
M430F5438AQGCARET	Active	Production	NFBGA (GCA) | 113	2500 | LARGE T&R	No	Call TI	Call TI	-40 to 125	MF5438AQET
M430F5438AQGCARET.A	Active	Production	NFBGA (GCA) | 113	2500 | LARGE T&R	No	Call TI	Call TI	-40 to 125	MF5438AQET
M430F5438AQZCARET	Active	Production	NFBGA (ZCA) | 113	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	MF5438AQET
M430F5438AQZCARET.A	Active	Production	NFBGA (ZCA) | 113	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	MF5438AQET

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430F5438A-ET :

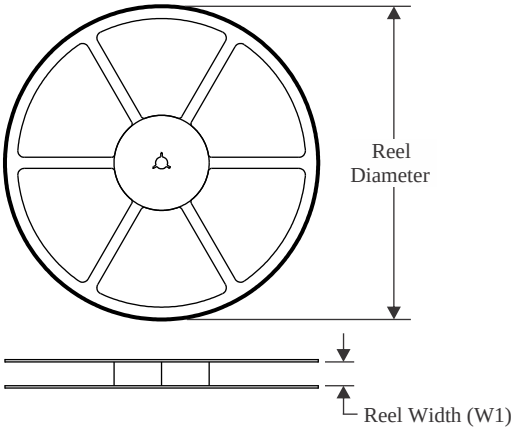
- Enhanced Product : MSP430F5438A-EP

NOTE: Qualified Version Definitions:

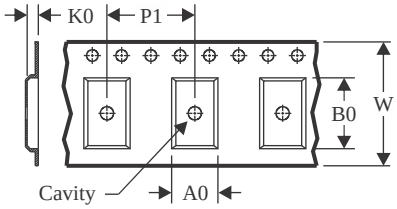
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

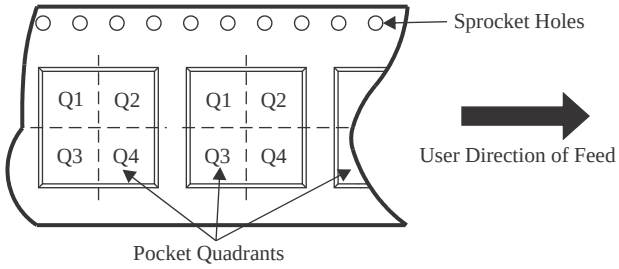


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

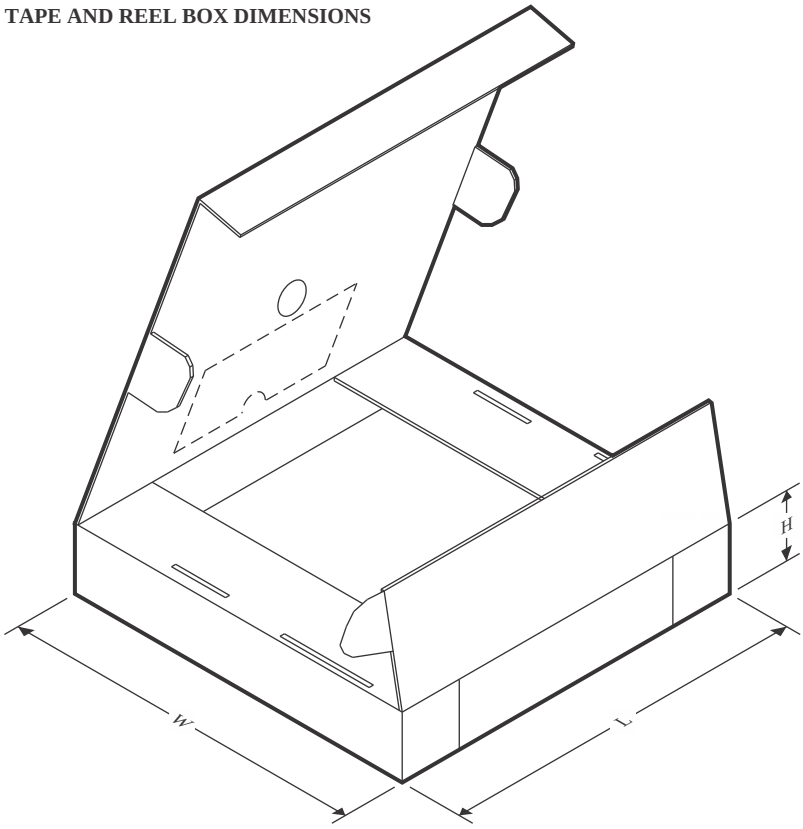
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
M430F5438AMGCARET	NFBGA	GCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
M430F5438AQGCARET	NFBGA	GCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

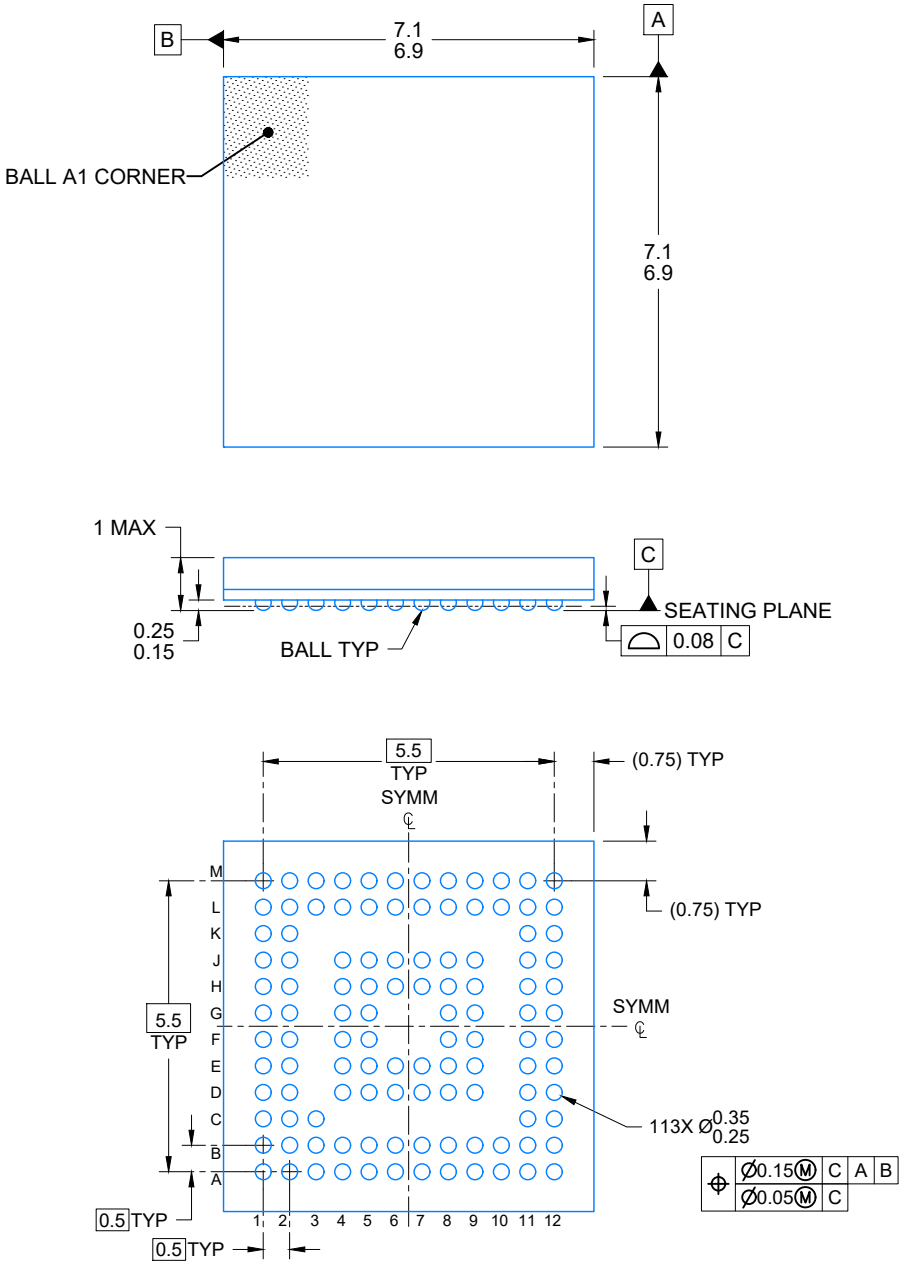
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
M430F5438AMGCARET	NFBGA	GCA	113	2500	350.0	350.0	43.0
M430F5438AQGCARET	NFBGA	GCA	113	2500	350.0	350.0	43.0

PACKAGE OUTLINE

GCA0113A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY

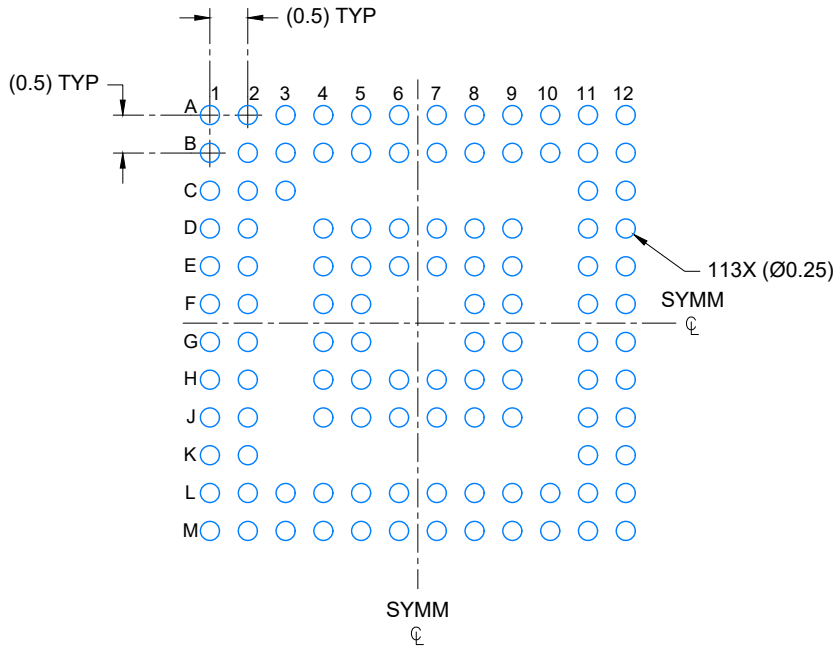


4225769/A 03/2020

NOTES:

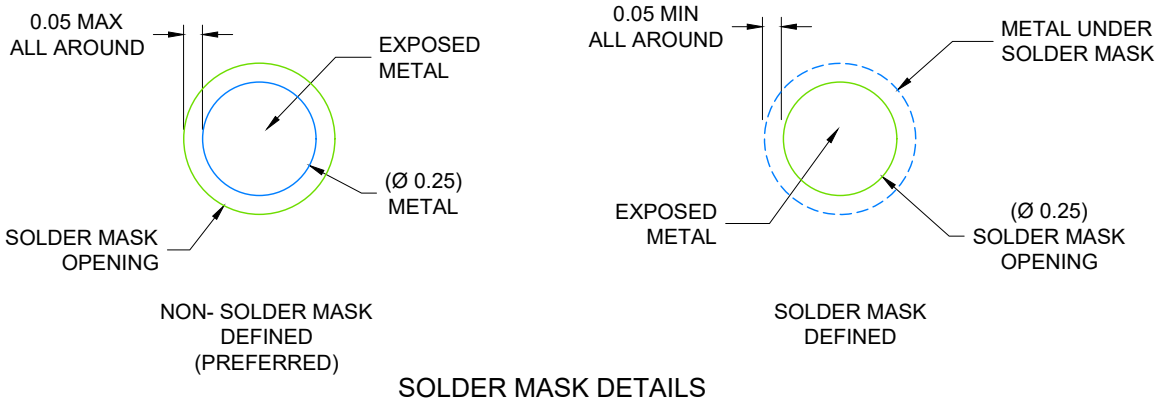
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 10X



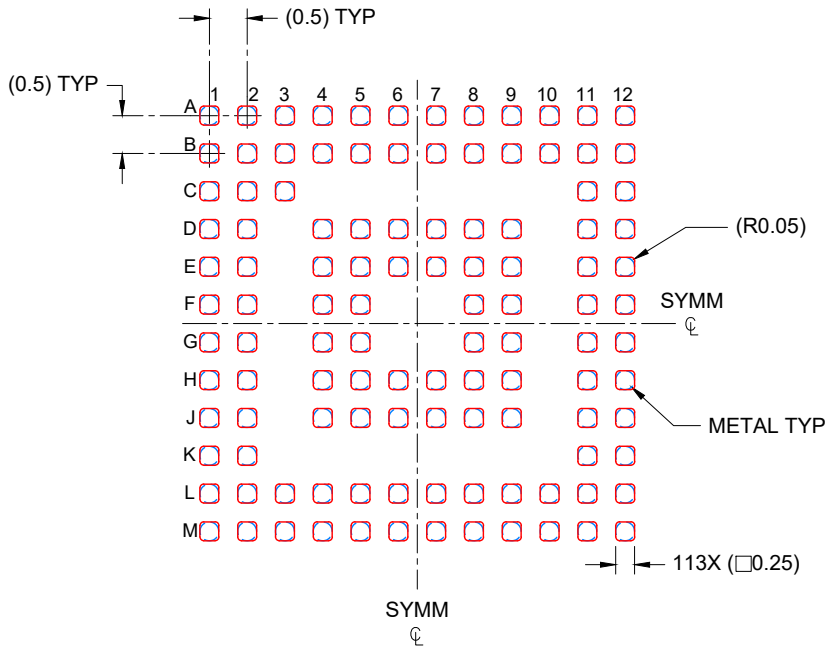
SOLDER MASK DETAILS

NOT TO SCALE

4225769/A 03/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 10X

4225769/A 03/2020

NOTES: (continued)

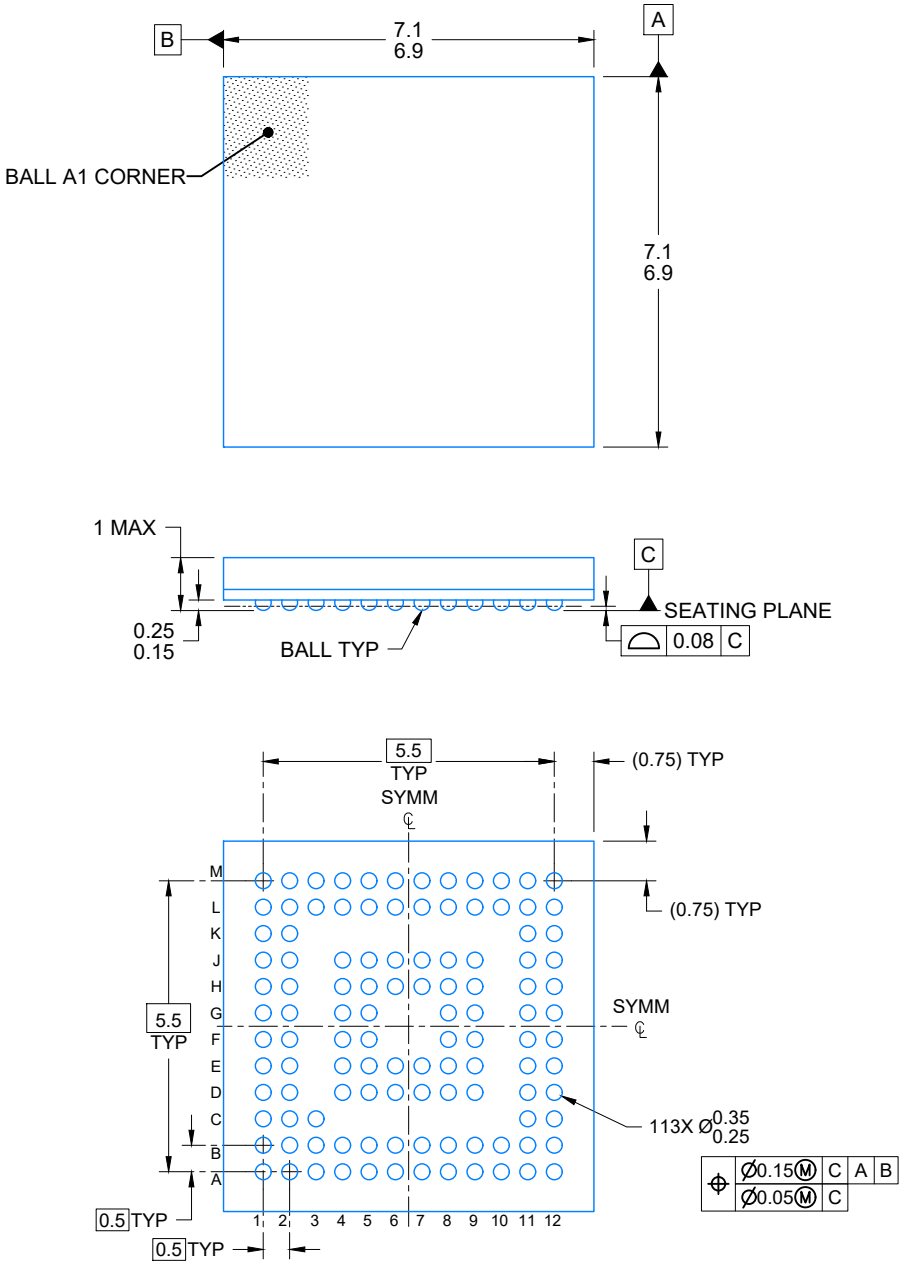
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ZCA0113A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY

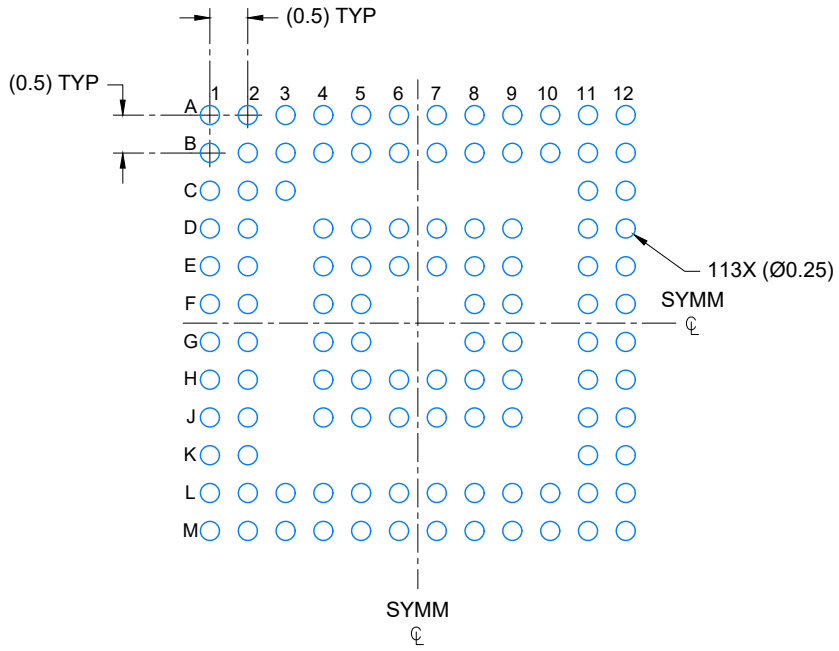


4225149/A 08/2019

NOTES:

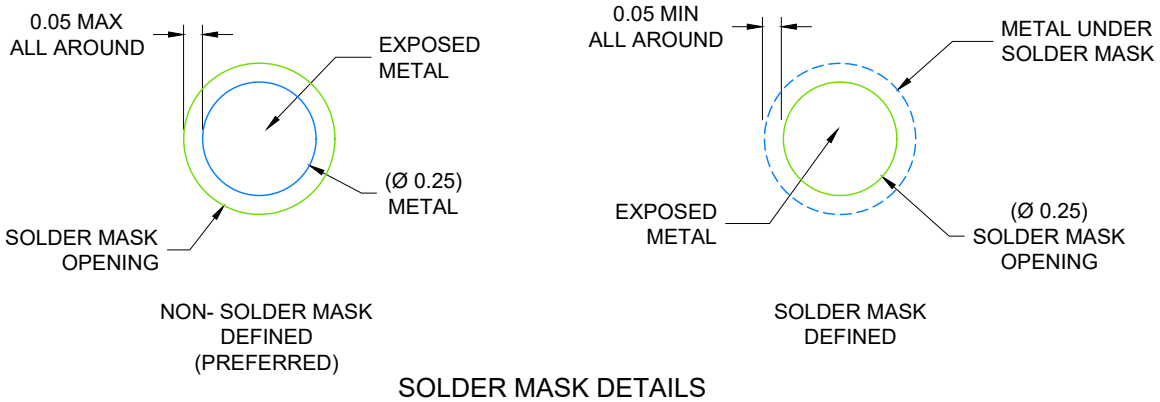
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 10X



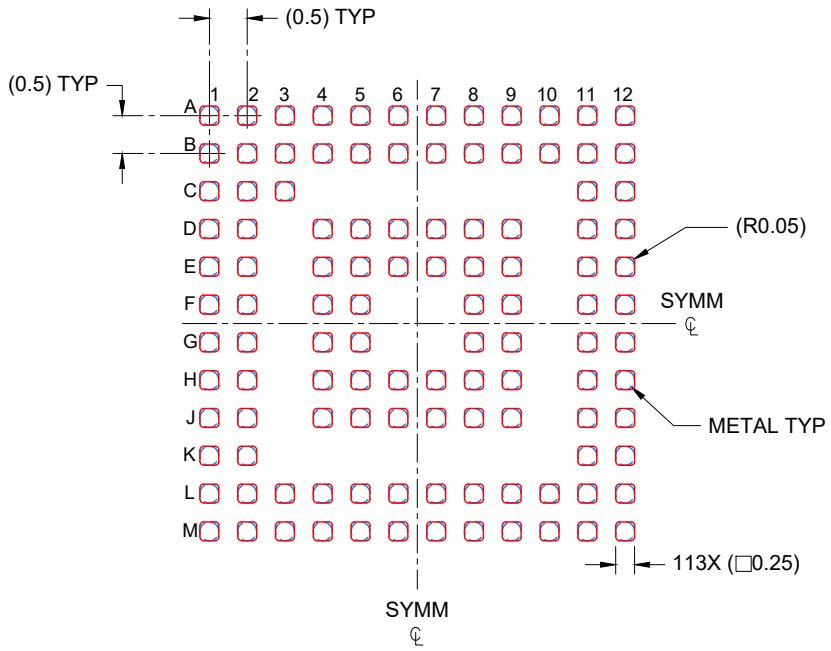
SOLDER MASK DETAILS

NOT TO SCALE

4225149/A 08/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 10X

4225149/A 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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