MAX232E 具有 IEC61000-4-2 保护的双路 RS-232 驱动器和接收器

1 特性

- 符合或超出 TIA/RS-232-F 和 ITU 建议 V.28 的要求
- 为 RS-232 总线引脚提供 ESD 保护
  - ±15kV 人体放电模型 (HBM)
  - ±8kV IEC61000-4-2，接触放电
  - ±15kV IEC61000-4-2，气隙放电
- 通过带 1μF 电荷泵电容器的单个 5V 电源供电
- 速率高达 250kbit/s
- 两个驱动器和两个接收器
- 低电源电流：8mA（典型值）

2 应用

- TIA/RS-232-F
- 电池供电型系统
- 端子
- 调制解调器
- 计算机

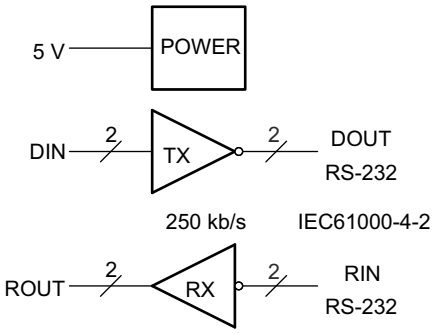
3 说明

MAX232E 是一款双路驱动器和接收器，它包含一个电容式电压发生器，可通过单个 5V 电源提供符合 RS-232-F 标准的电压电平。每个接收器都将 RS-232 输入转换为 5V TTL/CMOS 电平。该接收器的典型阈值为 1.3V，典型迟滞为 0.5V，可接受 ±30V 输入。每个驱动器都将 TTL/CMOS 输入电平转换为 TIA/RS-232-F 电平。

封装信息

器件型号	封装(1)	封装尺寸(2)
MAX232	SOIC (16)	9.9mm x 6mm
	SOIC (16)	10.4mm x 10.3mm
	PDIP (16)	19.3mm x 9mm
	SOP (16)	10.2mm x 7.8 mm

(1) 如需更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



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逻辑图（正逻辑）

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Pin Configuration and Functions 3
5 Specifications 4
5.1 Absolute Maximum Ratings 4
5.2 ESD Ratings 4
5.3 Recommended Operating Conditions 4
5.4 Thermal Information 5
5.5 Electrical Characteristics 5
5.6 Electrical Characteristics: Driver 5
5.7 Electrical Characteristics: Receiver 5
5.8 Switching Characteristics: Driver 6
5.9 Switching Characteristics: Receiver 6
5.10 Typical Characteristics 7
6 Detailed Description 10
6.1 Overview 10
6.2 Functional Block Diagram 10
6.3 Feature Description 10
6.4 Device Functional Modes 11
7 Applications and Implementation 12
7.1 Application Information 12
7.2 Typical Application 12
7.3 Power Supply Recommendations 13
7.4 Layout 14
8 Device and Documentation Support 15
8.1 接收文档更新通知 15
8.2 支持资源 15
8.3 Trademarks 15
8.4 静电放电警告 15
8.5 术语表 15
9 Revision History 15
10 Mechanical, Packaging, and Orderable Information 15

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4 Pin Configuration and Functions

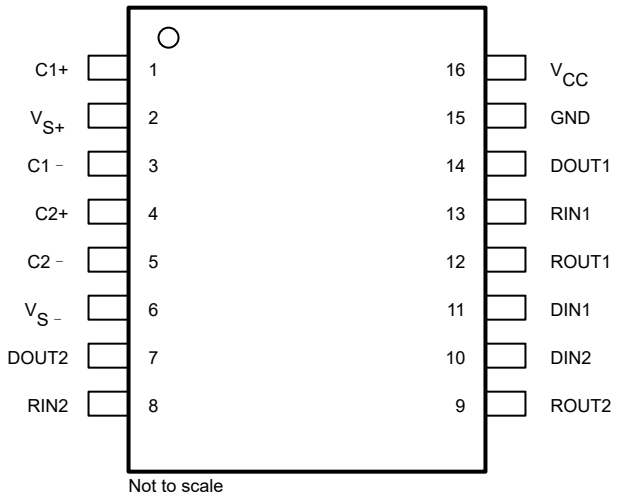

图 4-1. D (SOIC) , DW (SOIC), N (PDIP), or PW (TSSOP) 16-Pin Package (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C1+	—	Positive lead of C1 capacitor
2	V_{S+}	O	Positive charge pump output for storage capacitor only
3	C1 –	—	Negative lead of C1 capacitor
4	C2+	—	Positive lead of C2 capacitor
5	C2 –	—	Negative lead of C2 capacitor
6	V_{S-}	O	Negative charge pump output for storage capacitor only
7	DOUT2	O	RS-232 line data output (to remote RS-232 system)
8	RIN2	I	RS-232 line data input (from remote RS-232 system)
9	ROUT2	O	Logic data output (to UART)
10	DIN2	I	Logic data input (from UART)
11	DIN1	I	Logic data input (from UART)
12	ROUT1	O	Logic data output (to UART)
13	RIN1	I	RS-232 line data input (from remote RS-232 system)
14	DOUT1	O	RS-232 line data output (to remote RS-232 system)
15	GND	—	Ground
16	V_{CC}	—	Supply voltage, connect to external 5V power supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Input supply voltage (2)		–0.3	6	V
V_{S+}	Positive output supply voltage		V_{CC} – 0.3	15	V
V_{S-}	Negative output supply voltage		–0.3	–15	V
V_I	Input voltage	Driver	–0.3	V_{CC} + 0.3	V
		Receiver		±30	
V_O	Output voltage	DOUT	V_{S-} – 0.3	V_{S+} + 0.3	V
		ROUT	–0.3	V_{CC} + 0.3	
	Short-circuit duration	DOUT	Unlimited		
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 7, 8, 13, and 14	±15000	V
			Other pins	±3000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1500	
		IEC61000-4-2, air-gap discharge	Pins 7, 8, 13, and 14	±15000	
		IEC61000-4-2, contact discharge		±8000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (DIN1, DIN2)		2			V
V_{IL}	Low-level input voltage (DIN1, DIN2)				0.8	V
	Receiver input voltage (RIN1, RIN2)		±3		±30	V
T_A	Operating free-air temperature	MAX232EC	0		70	°C
		MAX232EI	–40		85	

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5.4 Thermal Information

THERMAL METRIC(1) (2) (3)		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	73.4	60.6	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	35.1	48.1	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	38.3	40.6	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	9.4	27.5	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	37.7	40.3	53.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Maximum power dissipation is a function of $T_J(max)$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 7-1)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5 V	All outputs open, T_A = 25°C		8	10	mA

(1) Test conditions are C1 – C4 = 1μF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.6 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER			TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	R_L = 3 kΩ to GND		5	7		V
V_{OL}	Low-level output voltage(3)	DOUT	R_L = 3 kΩ to GND			–7	–5	V
r_o	Output resistance	DOUT	$V_{S+} = V_{S-}$ = 0,	V_O = ±2 V	300			Ω
I_{OS} (4)	Short-circuit output current	DOUT	V_{CC} = 5.5 V,	V_O = 0		±10		mA
I_{IS}	Short-circuit input current	DIN	V_I = 0				200	μA

(1) Test conditions are C1 – C4 = 1μF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.
(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(4) Not more than one output should be shorted at a time.

5.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER			TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	ROUT	I_{OH} = –1mA		3.5			V
V_{OL}	Low-level output voltage	ROUT	I_{OL} = 3.2mA				0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	RIN	V_{CC} = 5V	T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	RIN	V_{CC} = 5V	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	RIN	V_{CC} = 5V		0.2	0.5	1	V
r_i	Receiver input resistance	RIN	V_{CC} = 5V	T_A = 25°C	3	5	7	kΩ

(1) Test conditions are C1 – C4 = 1μF at V_{CC} = 5V ± 0.5V.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.

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5.8 Switching Characteristics: Driver

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3kΩ to 7kΩ, See 图 6-2			30	V/µs
SR(t)	Driver transition region slew rate	R_L = 3kΩ, C_L = 2.5nF See 图 6-3		3		V/µs
	Data rate	One DOUT switching		250		kbit/s

(1) Test conditions are C1 – C4 = 1µF at V_{CC} = 5V ± 0.5V.

5.9 Switching Characteristics: Receiver

V_{CC} = 5V, T_A = 25°C (see 图 6-1)

PARAMETER		TEST CONDITIONS(1)	TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	C_L = 50pF	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	C_L = 50pF	500	ns

(1) Test conditions are C1 – C4 = 1µF at V_{CC} = 5V ± 0.5V.

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5.10 Typical Characteristics

T_A = 25 °C

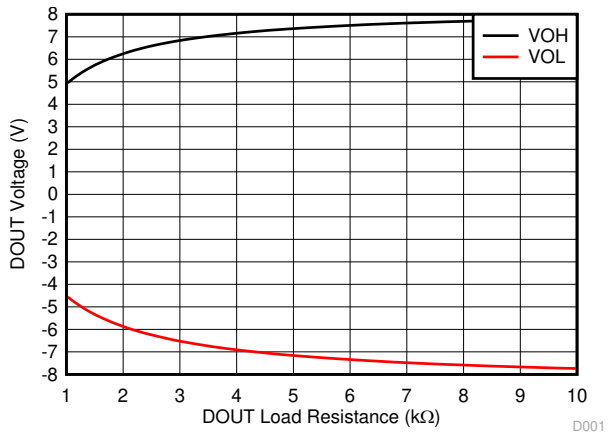

图 5-1. Driver Output Voltage vs Load Resistance

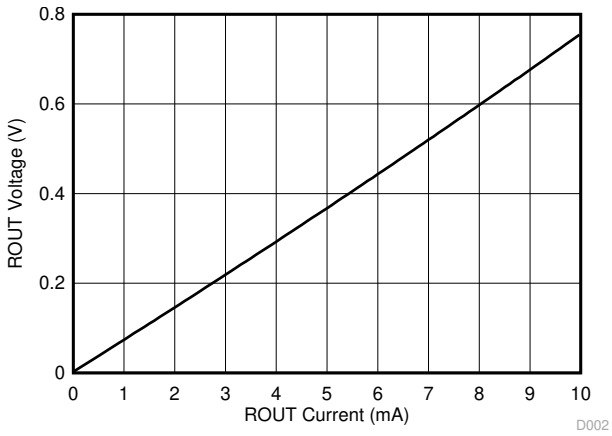

图 5-2. Receiver Low Output Voltage vs Load Current

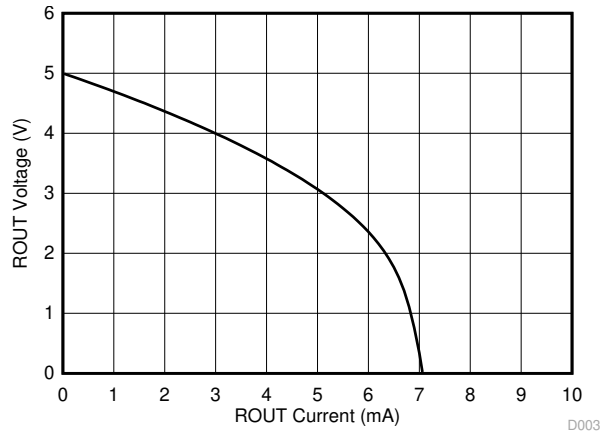

图 5-3. Receiver High Output Voltage vs Load Current

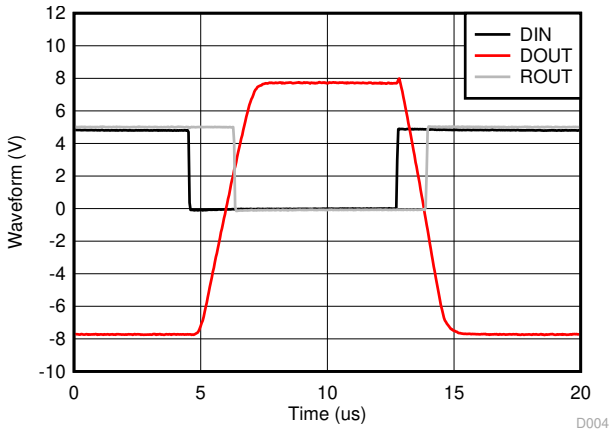

图 5-4. Loopback Waveforms Data Rate 120 kbit/s

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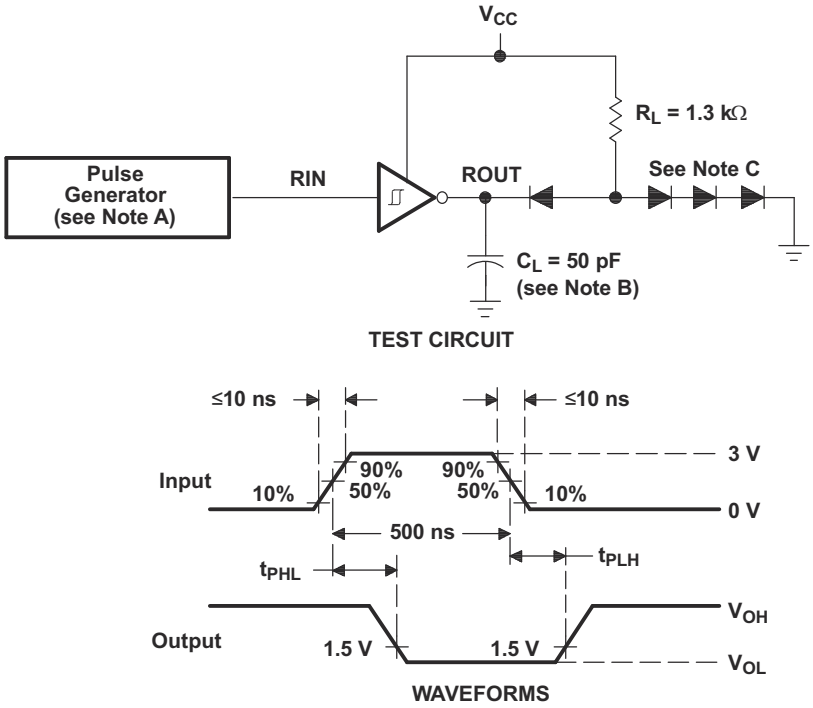

A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

图 6-1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

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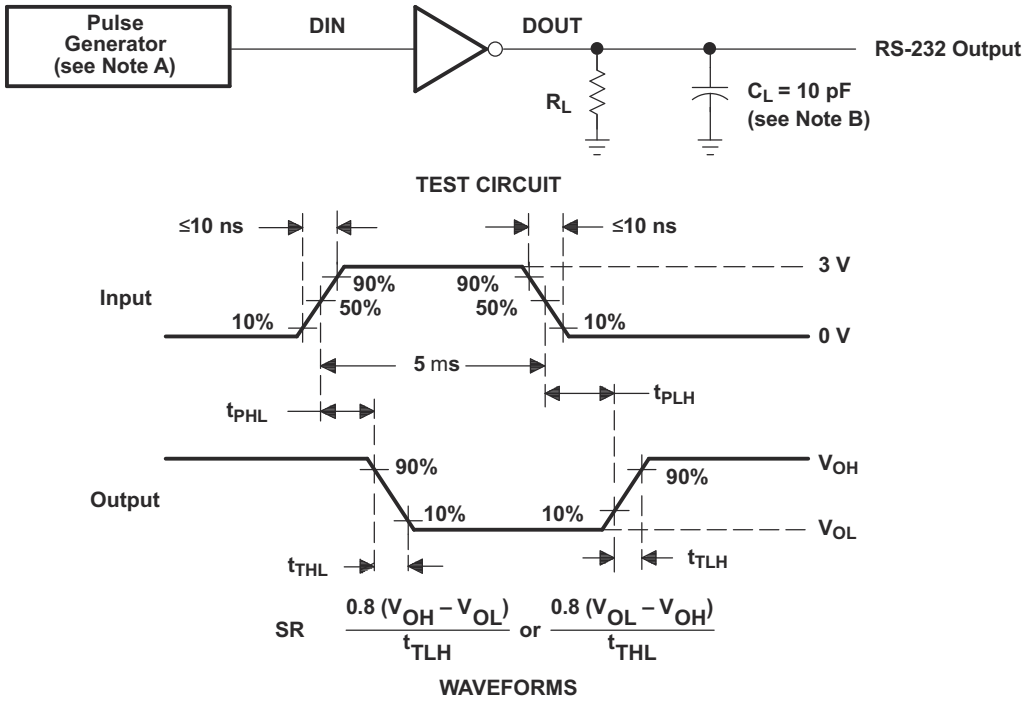
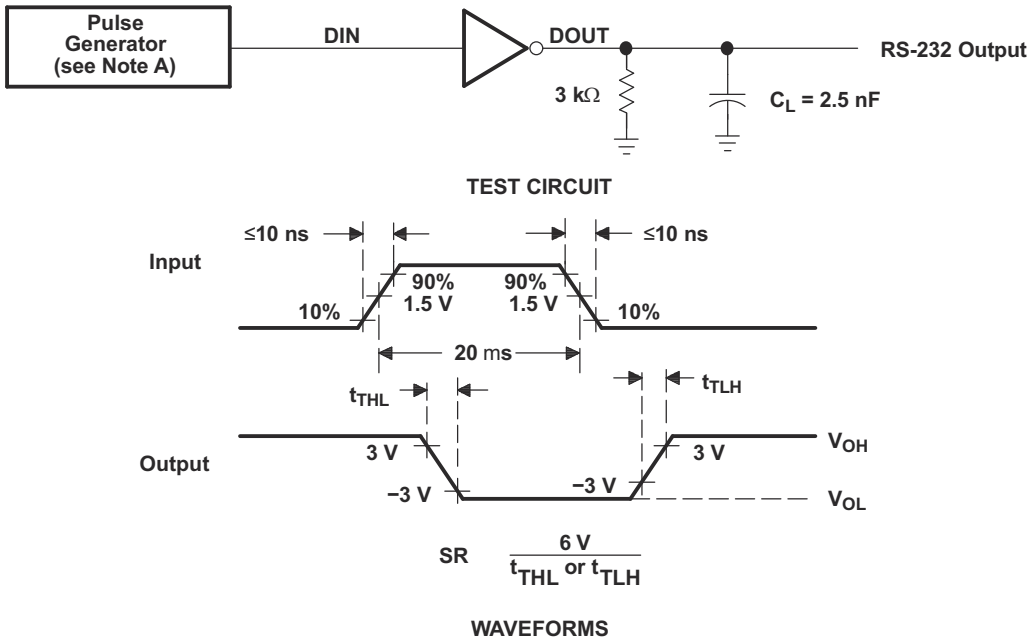


A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

图 6-2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-µs Input)



A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

图 6-3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-µs Input)

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6 Detailed Description

6.1 Overview

The MAX232E is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5V supply. All RS-232 pins have 15kV HBM and IEC61000-4-2 Air-Gap discharge protection. RS-232 pins also have 8kV IEC61000-4-2 contact discharge protection. Each receiver converts TIA/EIA-232-F inputs to 5V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to ±30V inputs and decode inputs as low as ±3 V. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

6.2 Functional Block Diagram

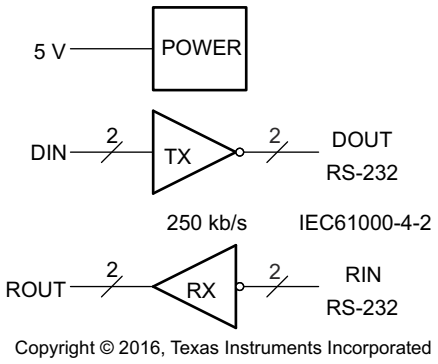

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图 6-1. Logic Diagram (Positive Logic)

6.3 Feature Description

6.3.1 Power

The power block increases and inverts the 5V supply for the RS-232 driver using a charge pump that requires four 1µF external capacitors.

6.3.2 RS-232 Driver

Two drivers interface standard logic level to RS-232 levels. Internal pullup resistors on DIN inputs ensures a high input when the line is high impedance.

6.3.3 RS-232 Receiver

Two receivers interface RS-232 levels to standard logic levels. An open or shorted to ground input results in a high output on ROUT.

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6.4 Device Functional Modes

6.4.1 V_{CC} Powered by 5V

The device is in normal operation.

6.4.2 V_{CC} Unpowered

When MAX232E is unpowered, it can be safely connected to an active remote RS-232 device.

6.4.3 Truth Tables

表 6-1 and 表 6-2 list the functions of this device.

表 6-1. Function Table for Each Driver

INPUT DIN(1)	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

表 6-2. Function Table for Each Receiver

INPUT RIN(1)	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

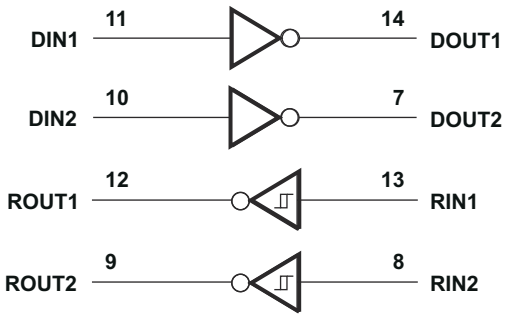


图 6-2. Logic Diagram (Positive Logic)

7 Applications and Implementation

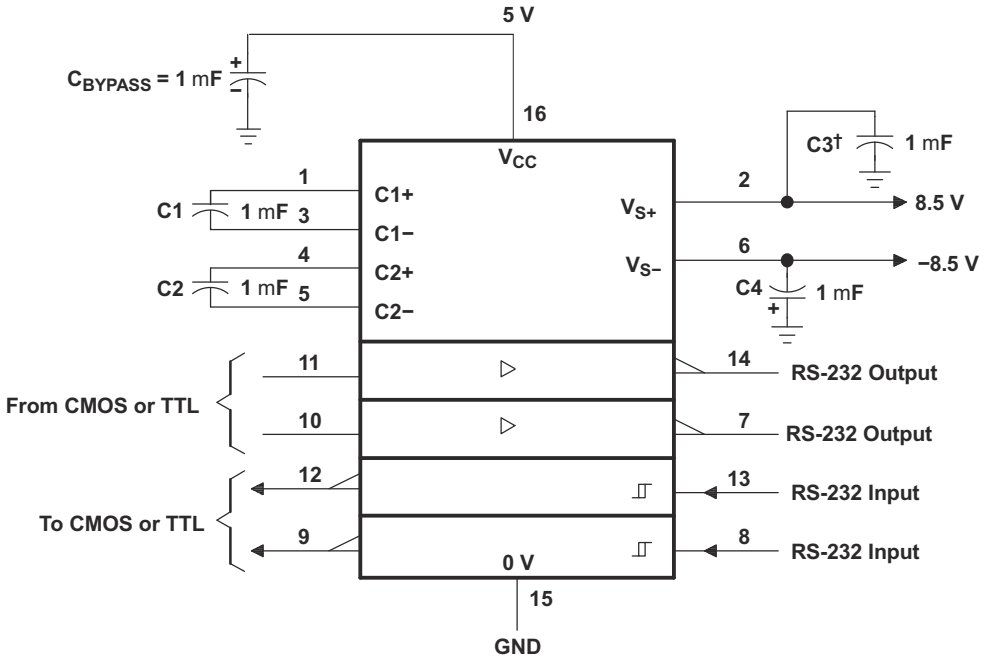
备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

For proper operation add capacitors as shown in 图 7-1. Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

7.2 Typical Application



† C3 can be connected to V_{CC} or GND.

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Resistor values shown are nominal.

Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

图 7-1. Typical Operating Circuit

7.2.1 Design Requirements

- V_{CC} minimum is 4.5V and maximum is 5.5V.
- Maximum recommended bit rate is 250kbit/s.

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7.2.2 Detailed Design Procedure

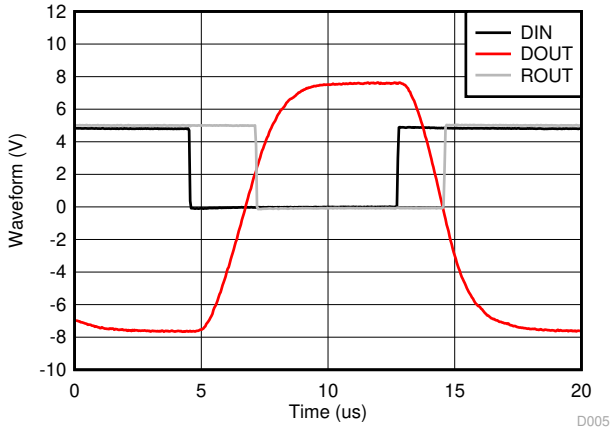
The capacitor type used for C1 – C4 is not critical for proper operation. The MAX232E requires 1µF capacitors, although capacitors up to 10µF can be used without harm. Ceramic dielectrics are suggested for capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V – .

Use larger capacitors (up to 10µF) to reduce the output impedance at V_{S+} and V_{S-}.

Bypass V_{CC} to ground with at least 1 µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 – C4).

7.2.3 Application Curve

Loopback waveform connects DOUT to RIN.



Date Rate = 120 kbit/s, C_L = 1 nF

图 7-2. Loopback Waveforms

7.3 Power Supply Recommendations

The V_{CC} voltage should be connected to the same power source used for logic device connected to DIN and ROUT pins. V_{CC} should be between 4.5V and 5.5V.

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7.4 Layout

7.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from MAX232E ground pin and circuit board ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin.

7.4.2 Layout Example

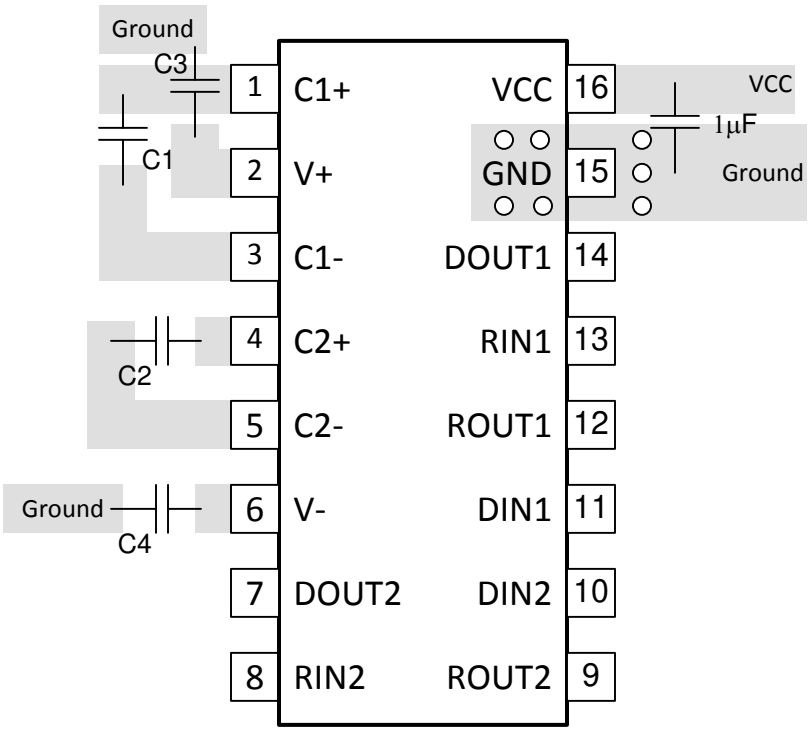

图 7-3. MAX232E Layout

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8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (August 2016) to Revision D (February 2024) — **Page**

- 将“器件信息”表更改为*封装信息* 表 1
- Changed the *Thermal Information* table 5

Changes from Revision B (November 2009) to Revision C (August 2016) — **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实现* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 删除了*特性* 中的“±30V 输入电平” 1
- 删除了*订购信息* 表；请参阅数据表末尾的 POA 1
- Added MIN value ±3 to "Receiver input voltage (RIN1, RIN2) row in *Recommended Operating Conditions* ... 4
- Changed $R_{\theta JA}$ values in *Thermal Information* 5
- Deleted table note 3 from *Receiver Section Electrical Characteristics* 5
- Added a new row to the *Function Table for Each Receiver* 11

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX232ECD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	MAX232EC
MAX232ECDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC
MAX232ECDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC
MAX232ECDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	MAX232EC
MAX232ECDWR	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	MAX232EC
MAX232ECDWRG4	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	
MAX232ECN	Obsolete	Production	PDIP (N) | 16	-	-	Call TI	Call TI	0 to 70	MAX232ECN
MAX232ECPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	0 to 70	MA232EC
MAX232ECPWR	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	0 to 70	MA232EC
MAX232ECPWRG4	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	0 to 70	MA232EC
MAX232EID	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	MAX232EI
MAX232EIDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI
MAX232EIDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI
MAX232EIDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI
MAX232EIDRG4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI
MAX232EIDW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 85	MAX232EI
MAX232EIDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI
MAX232EIDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI
MAX232EIN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	MAX232EIN
MAX232EIN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	MAX232EIN
MAX232EINE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	MAX232EIN
MAX232EIPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	MB232EI
MAX232EIPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB232EI
MAX232EIPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB232EI
MAX232EIPWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB232EI

(1) **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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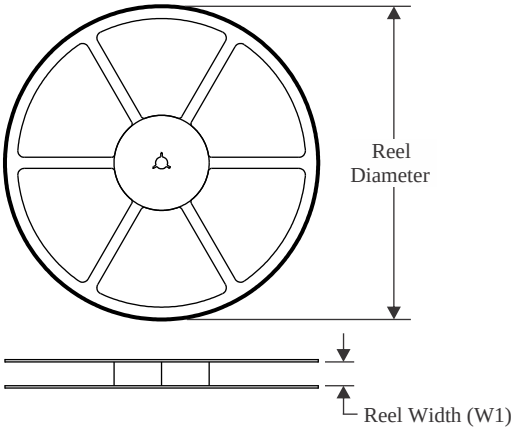
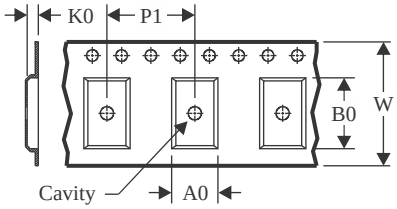
TAPE AND REEL INFORMATION

REEL DIMENSIONS

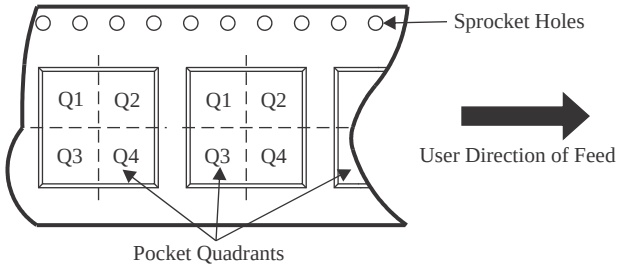


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

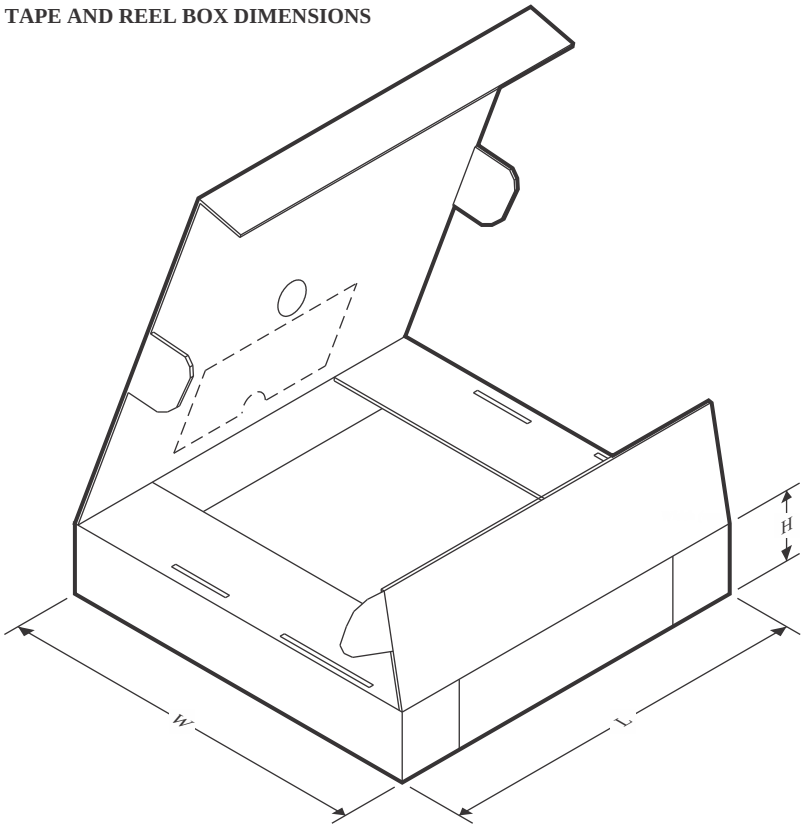
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232EIDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX232EIPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

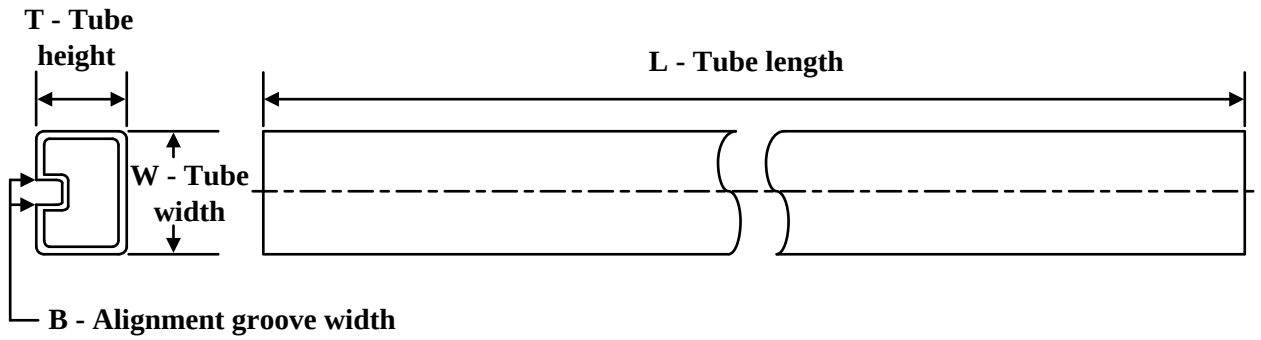
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX232ECDR	SOIC	D	16	2500	333.2	345.9	28.6
MAX232ECDR	SOIC	D	16	2500	340.5	336.1	32.0
MAX232EIDR	SOIC	D	16	2500	353.0	353.0	32.0
MAX232EIDRG4	SOIC	D	16	2500	353.0	353.0	32.0
MAX232EIDWR	SOIC	DW	16	2000	350.0	350.0	43.0
MAX232EIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
MAX232EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX232EIPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0

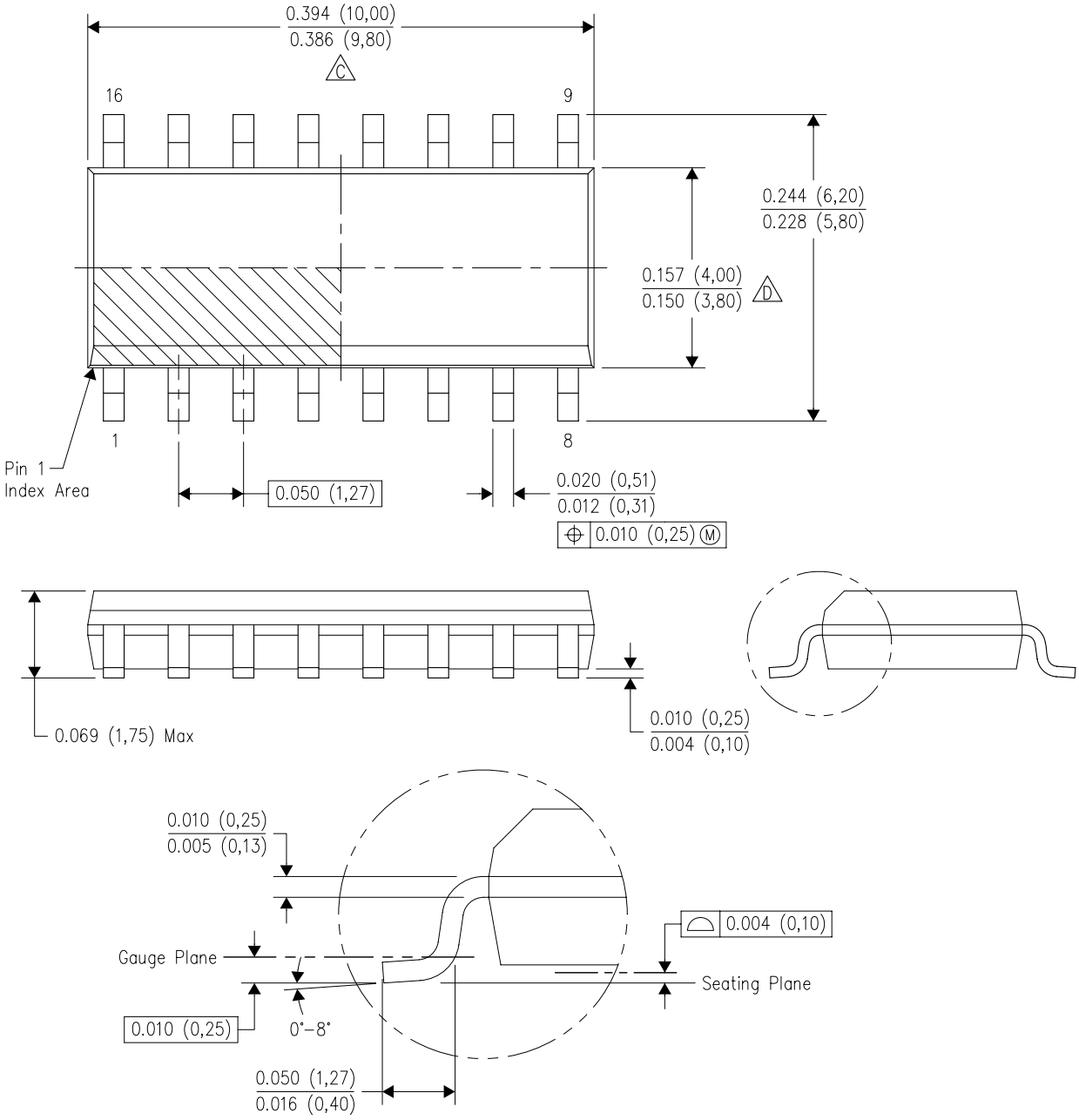
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MAX232EIN	N	PDIP	16	25	506	13.97	11230	4.32
MAX232EIN.A	N	PDIP	16	25	506	13.97	11230	4.32
MAX232EINE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

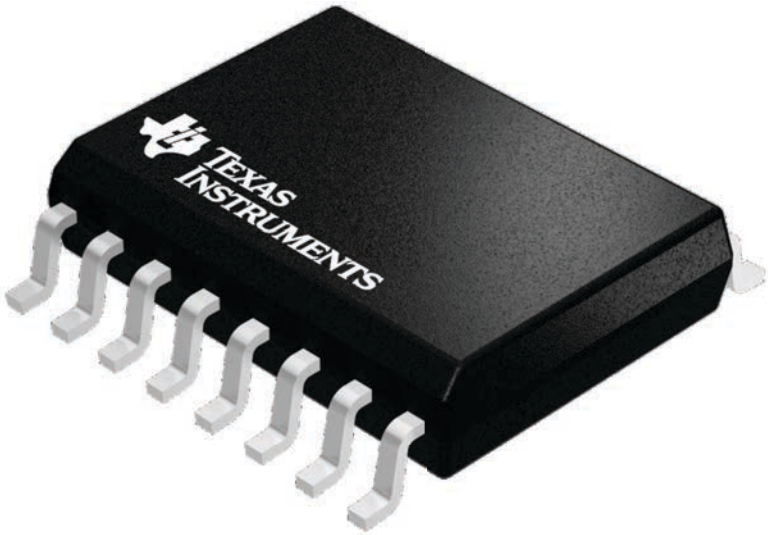
DW 16

SOIC - 2.65 mm max height

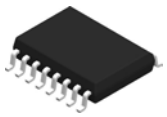
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

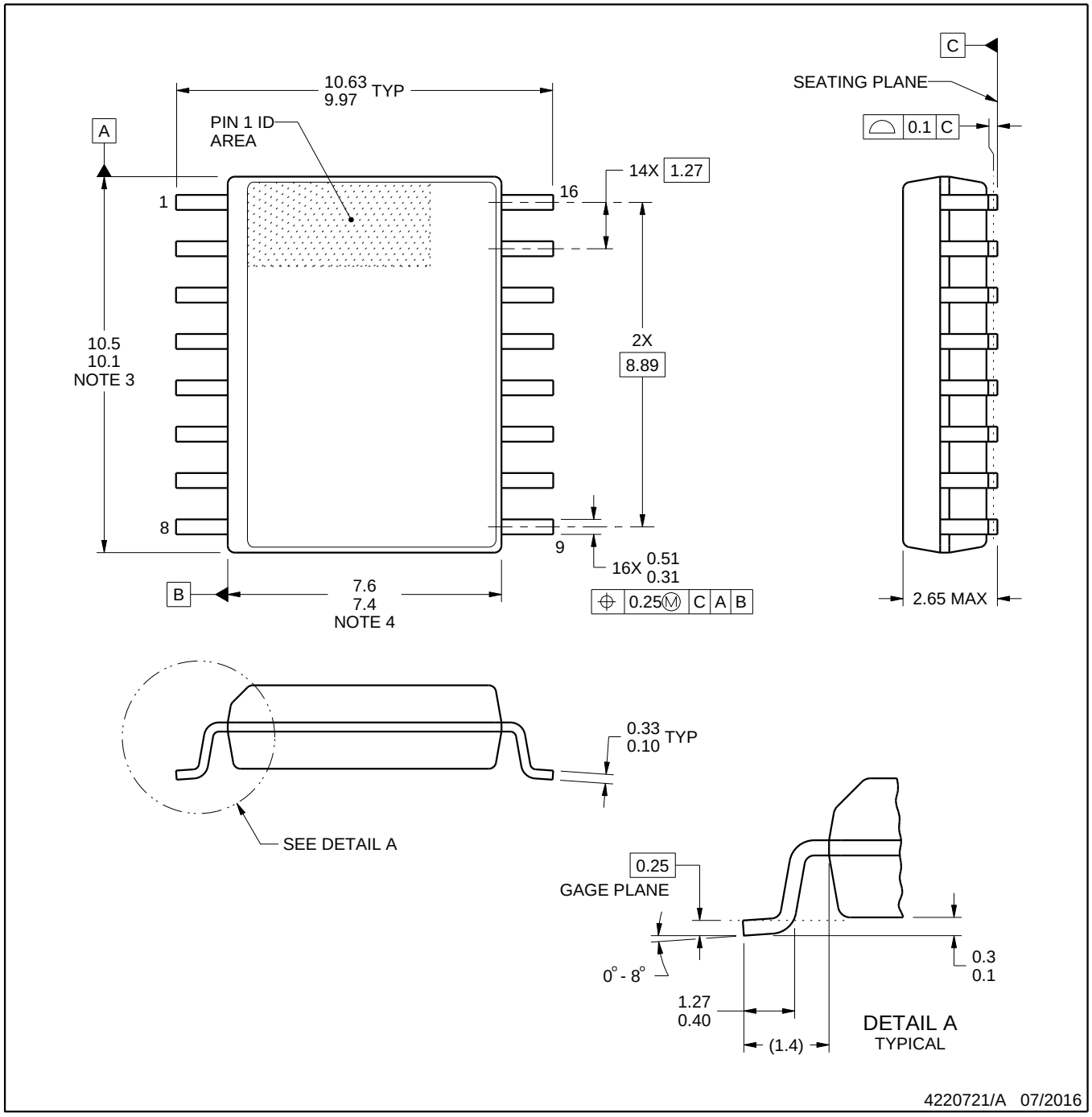


PACKAGE OUTLINE

DW0016A

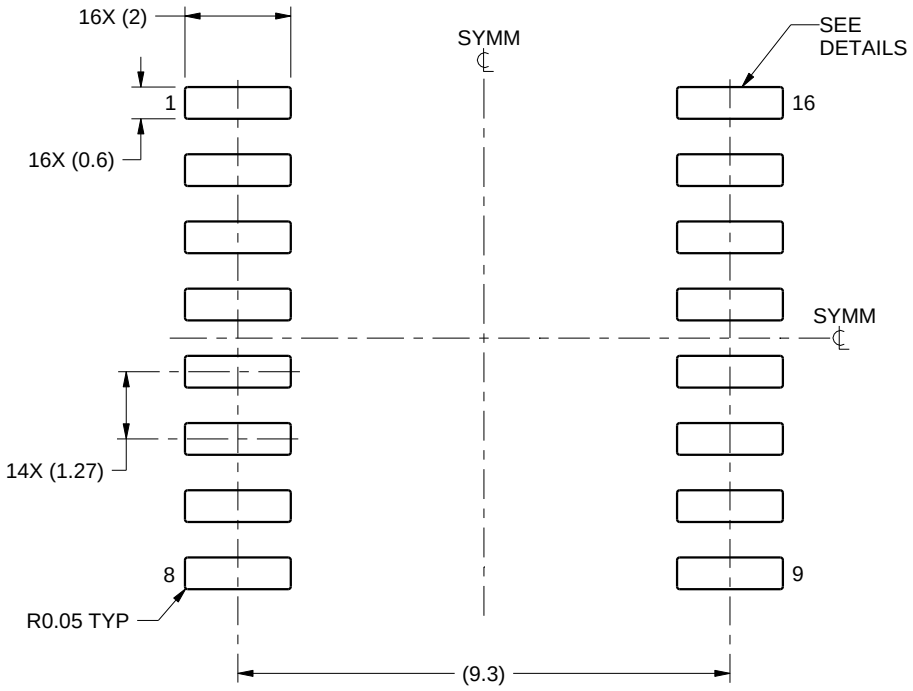
SOIC - 2.65 mm max height

SOIC

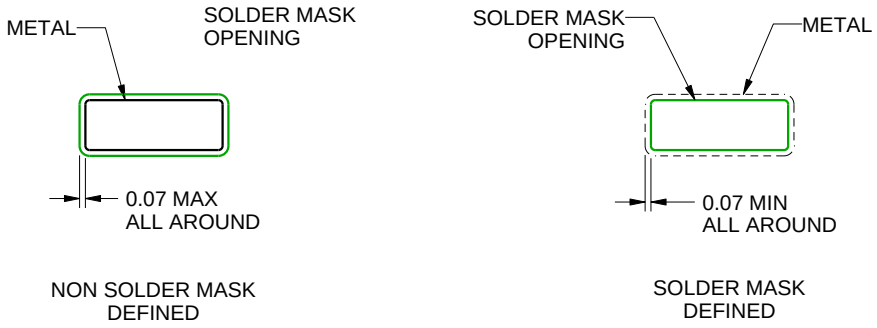


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

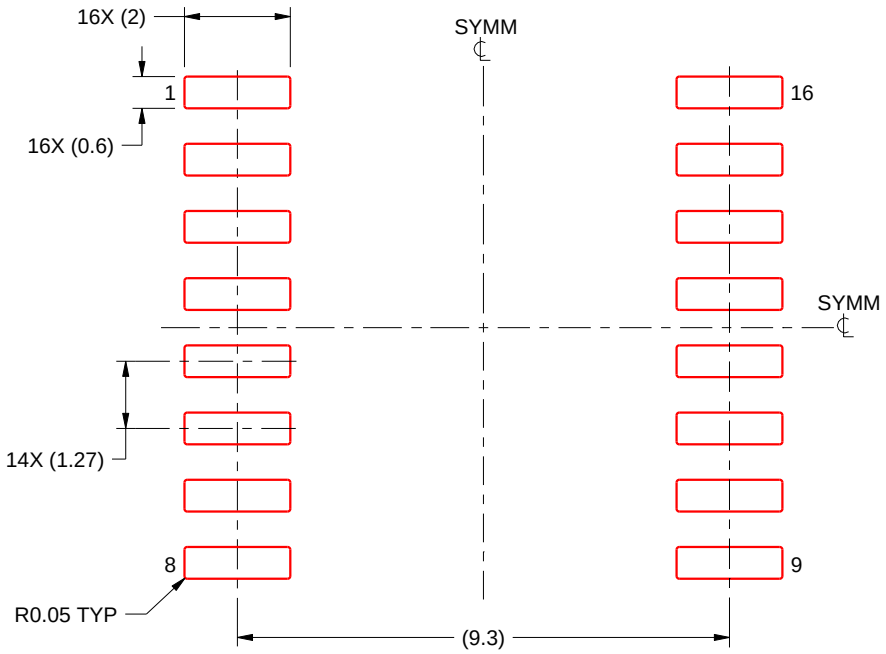


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

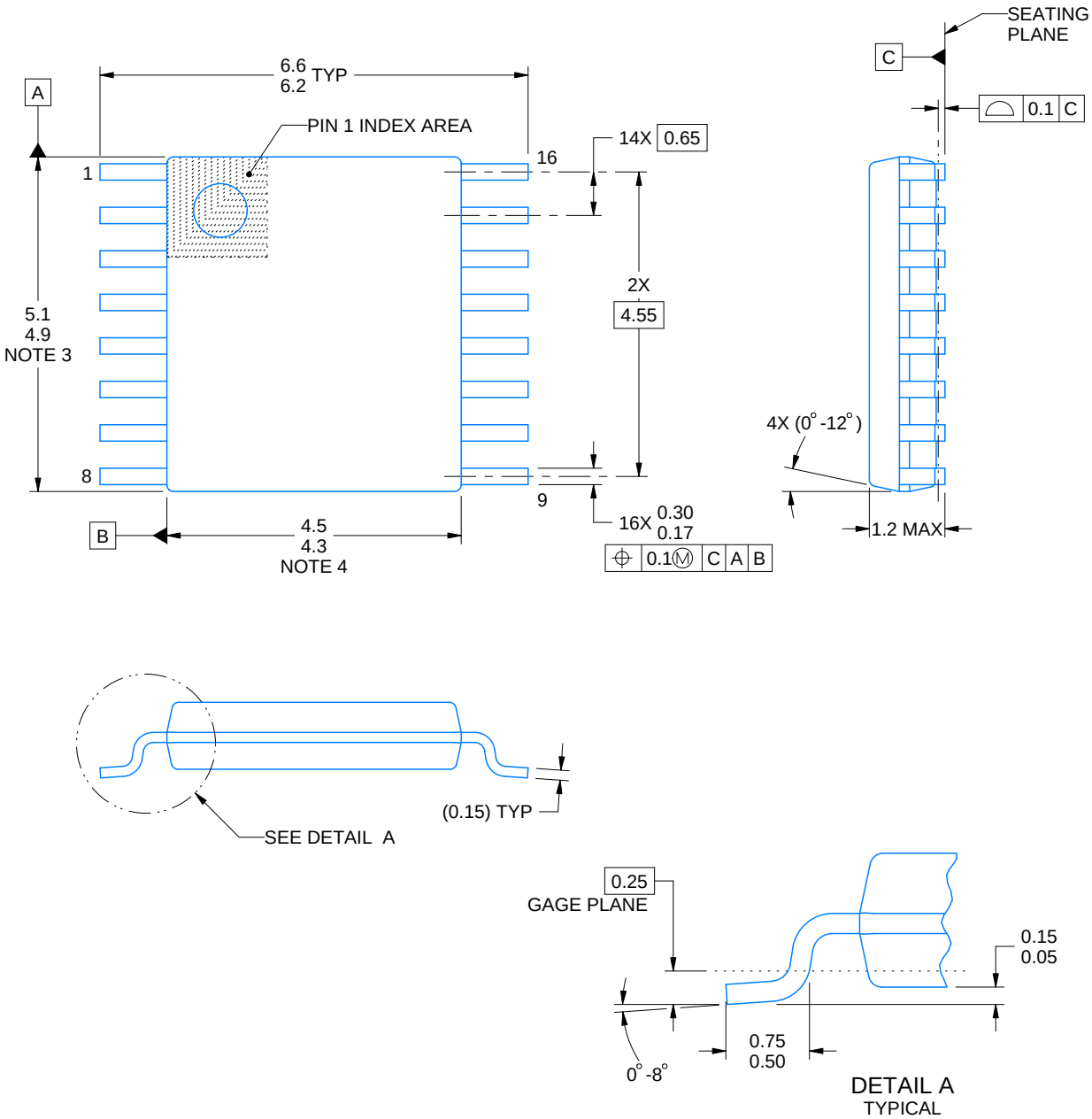
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

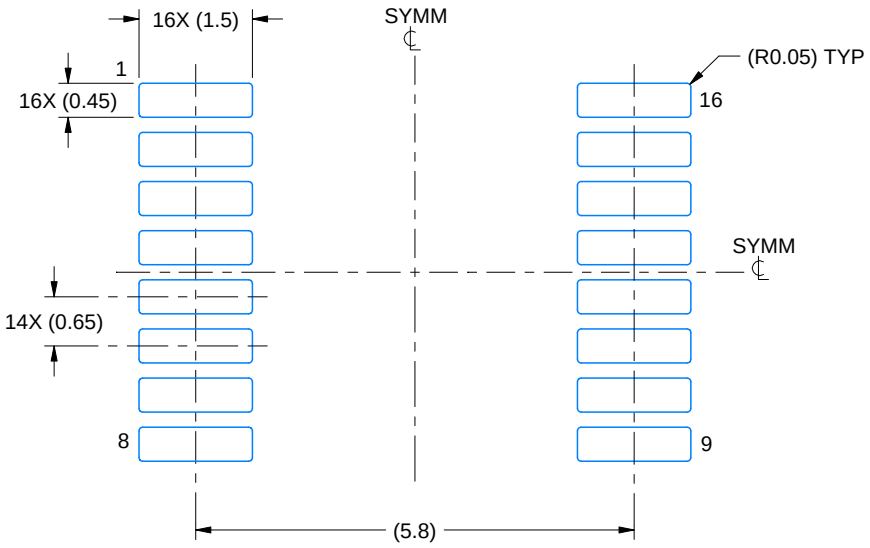
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

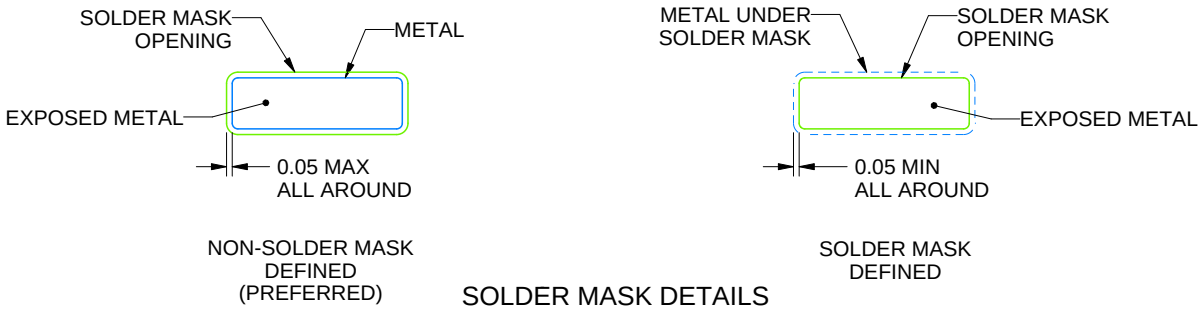


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

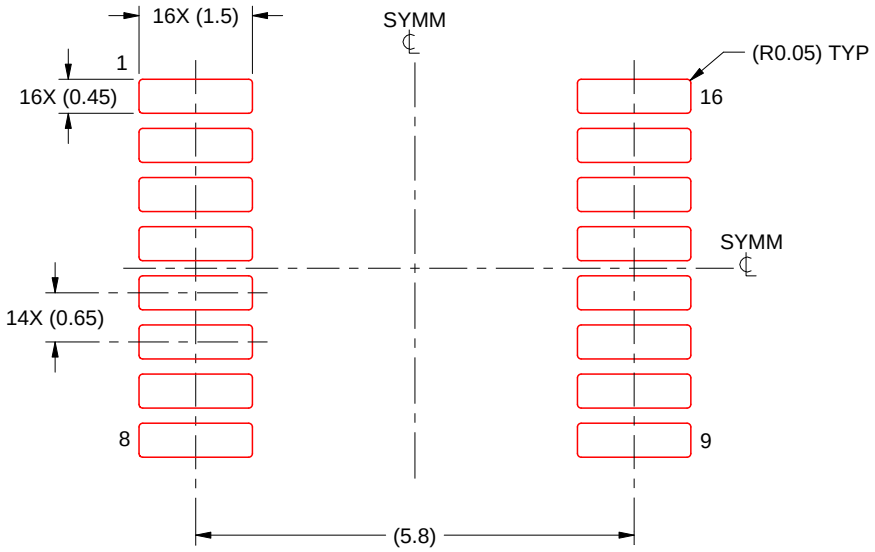


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

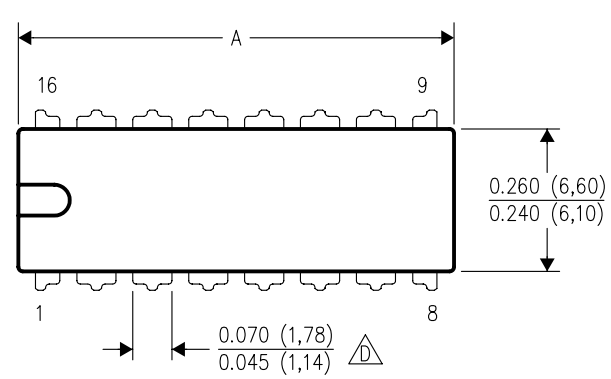
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

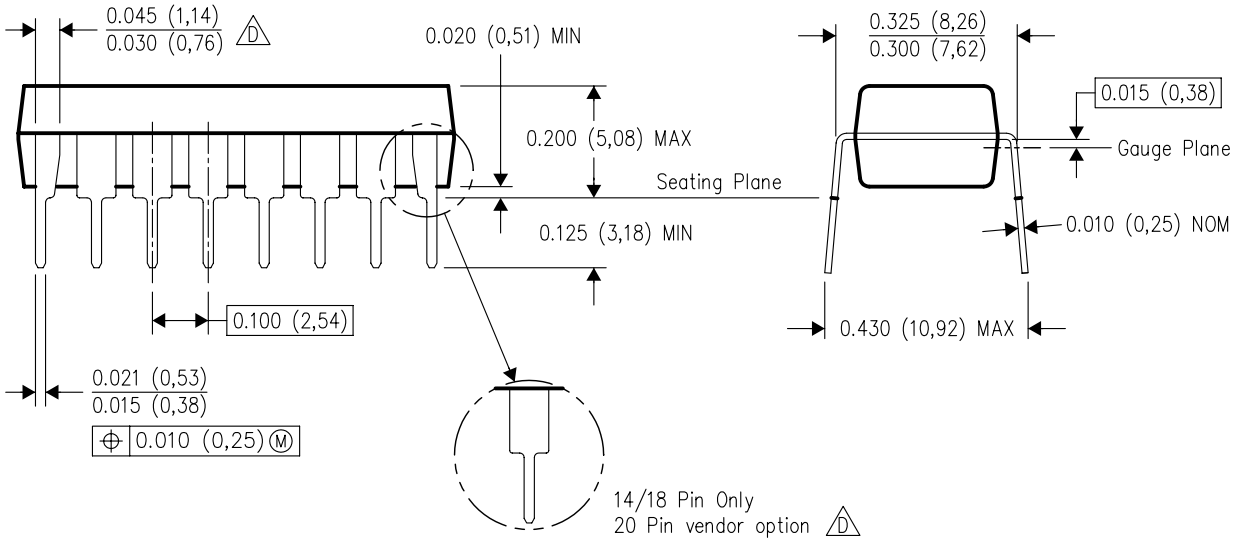
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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最后更新日期：2025 年 10 月