

# LP50xx 9/12 通道、12 位 PWM 超低静态电流 I<sup>2</sup>C RGB LED 驱动器

## 1 特性

- 工作电压范围：
  - V<sub>CC</sub> 范围：2.7V 至 5.5V
  - EN、SDA 和 SCL 引脚，兼容 1.8V、3.3V 和 5V 电源轨
  - 最大输出电压：6V
- 12 路高精度恒定电流阱
  - 在整个 V<sub>CC</sub> 范围内，每个通道的最大电流为 25.5mA
  - 当 V<sub>CC</sub> ≥ 3.3V 时，每个通道的最大电流为 35mA
  - 器件间误差：±5%；通道间误差：±5%
- 超低静态电流：
  - 关断模式：1μA (最大值)，EN 处于低电平
  - 节能模式：10μA (典型值)，EN 处于高电平，且所有 LED 均在超过 30ms 后关闭
- 每个通道都具有集成式 12 位、29kHz PWM 发生器：
  - 每个通道都具有独立的色彩混合寄存器
  - 每个 RGB LED 模块都具有独立的亮度控制寄存器
  - 可选的对数或线性标度亮度控制
  - 集成三相 PWM 相移方案
- 3 个可编程组 (R、G、B)，可轻松对每种颜色进行软件控制
- 2 个外部硬件地址引脚允许连接多达 4 个器件
- 广播从地址允许同时配置多个器件
- 自动递增允许在一次传输期间写入或读取多个连续的寄存器
- 高达 400kHz 的快速模式 I<sup>2</sup>C 速度

## 2 应用

用于以下设备的 LED 照明、指示灯和闪烁光：

- 智能扬声器 (带语音助理)
- 智能家用电器
- 可视门铃
- 电子智能锁
- 烟雾和热量探测器
- STB 和 DVR
- 智能路由器
- 手持设备

## 3 说明

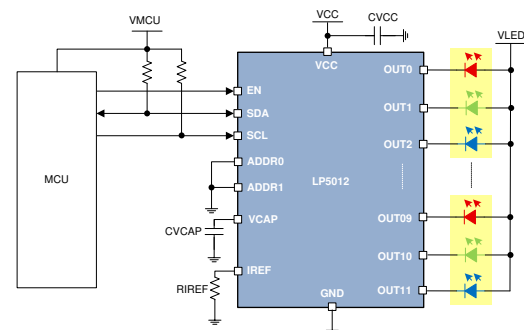
智能家居和其他采用人机交互的应用都需要高性能 RGB LED 驱动器。LED 动画效果 (如闪烁、呼吸以及追逐) 可极大地改善用户体验，同时最大限度地降低系统噪声也至关重要。

LP50xx 器件是一款 9/12 通道恒定电流阱 LED 驱动器。LP50xx 器件包含集成式色彩混合和亮度控制，并且预配置特性可简化软件编码过程。为每个通道配备的集成式 12 位、29kHz PWM 发生器可使 LED 色彩流畅、生动，并消除可闻噪声。

### 器件信息

器件型号 <sup>(1)</sup>	封装	封装尺寸 (标称值)
LP5009	WQFN (20)	3.00mm × 3.00mm
LP5012		
LP5009	TSSOP (24)	7.80mm × 4.40mm
LP5012		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision A (July 2019) to Revision B (August 2020)</b>	<b>Page</b>
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 向数据表中添加了 PW 封装选项.....	1

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<b>Changes from Revision * (May 2019) to Revision A (July 2019)</b>	<b>Page</b>
• 将“预告信息”更改为“量产数据”.....	1

## 5 Description (continued)

The LP50xx device controls each LED output with a 12-bit PWM resolution at 29-kHz switching frequency, which helps achieve a smooth dimming effect and eliminates audible noise. The independent color mixing and intensity control registers make the software coding straightforward. When targeting a fade-in, fade-out type breathing effect, the global R, G, B bank control reduces the microcontroller loading significantly. The LP50xx device also implements a PWM phase-shifting function to help reduce the input power budget when LEDs turn on simultaneously.

The LP50xx device implements an automatic power-saving mode to achieve ultra-low quiescent current. When channels are all off for 30 ms, the device total power consumption is down to 10  $\mu$ A, which makes the LP50xx device a potential choice for battery-powered end equipment.

## 6 Pin Configuration and Functions

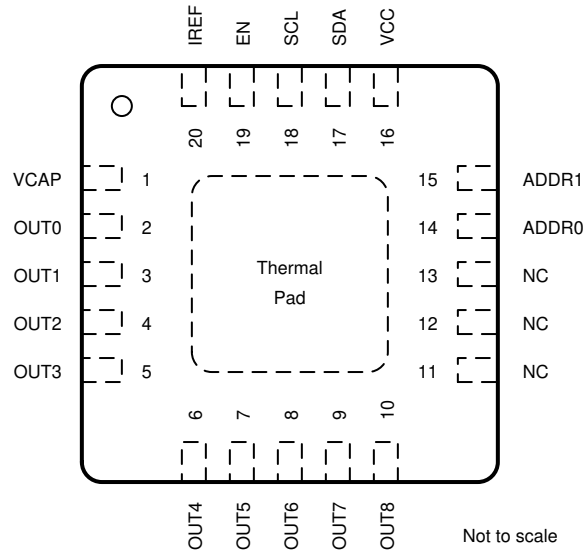


图 6-1. LP5009 RUK Package 20-Pin WQFN With Exposed Thermal Pad Top View

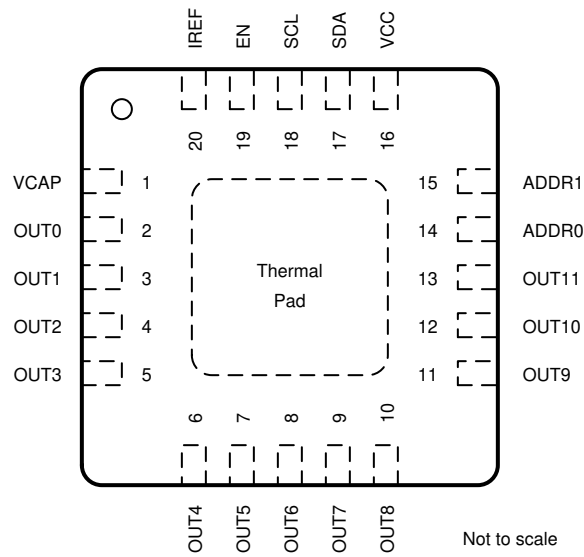


图 6-2. LP5012 RUK Package 20-Pin WQFN With Exposed Thermal Pad Top View

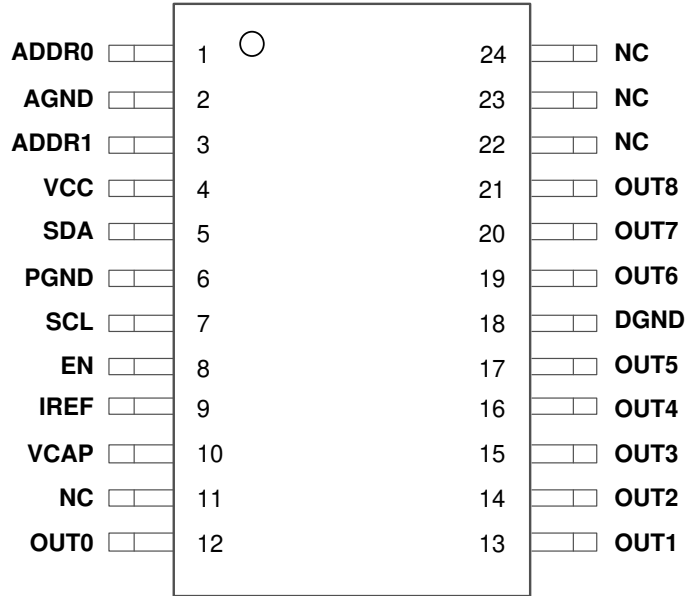


图 6-3. LP5009 PW Package 24-Pin TSSOP Top View

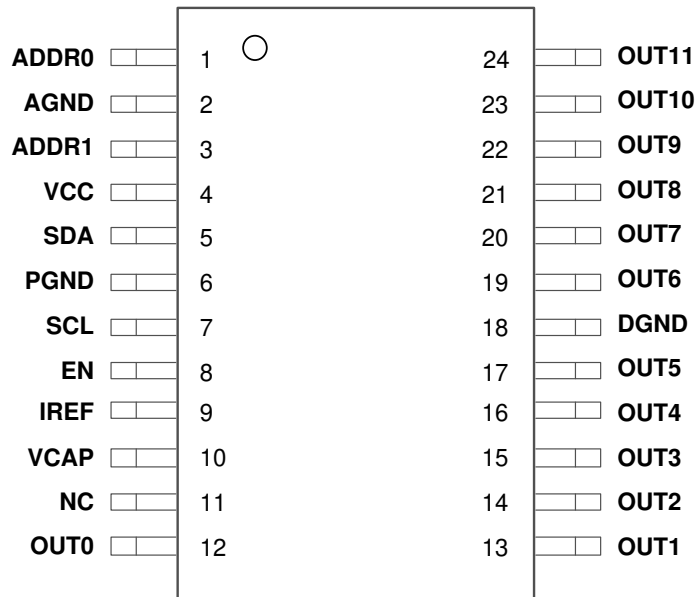


图 6-4. LP5012 PW Package 24-Pin TSSOP Top View

## Pin Functions

NAME	PIN				I/O	DESCRIPTION
	RUK NO.		PW NO.			
	LP5009	LP5012	LP5009	LP5012		
ADDR0	14	14	1	1	—	I <sup>2</sup> C slave-address selection pin. This pin must not be left floating.
ADDR1	15	15	3	3	—	I <sup>2</sup> C slave-address selection pin. This pin must not be left floating.
EN	19	19	8	8	I	Chip enable input pin.
IREF	20	20	9	9	—	Output current-reference global-setting pin.
NC	11, 12, 13	—	22, 23, 24	—	—	No internal connection.
OUT0	2	2	12	12	O	Current sink output 0. If not used, this pin can be left floating.
OUT1	3	3	13	13	O	Current sink output 1. If not used, this pin can be left floating.
OUT2	4	4	14	14	O	Current sink output 2. If not used, this pin can be left floating.
OUT3	5	5	15	15	O	Current sink output 3. If not used, this pin can be left floating.
OUT4	6	6	16	16	O	Current sink output 4. If not used, this pin can be left floating.
OUT5	7	7	17	17	O	Current sink output 5. If not used, this pin can be left floating.
OUT6	8	8	19	19	O	Current sink output 6. If not used, this pin can be left floating.
OUT7	9	9	20	20	O	Current sink output 7. If not used, this pin can be left floating.
OUT8	10	10	21	21	O	Current sink output 8. If not used, this pin can be left floating.
OUT9	—	11	—	22	O	Current sink output 9. If not used, this pin can be left floating.
OUT10	—	12	—	23	O	Current sink output 10. If not used, this pin can be left floating.
OUT11	—	13	—	24	O	Current sink output 11. If not used, this pin can be left floating.
SCL	18	18	7	7	I	I <sup>2</sup> C bus clock line. If not used, this pin must be connected to GND or VCC.
SDA	17	17	5	5	I/O	I <sup>2</sup> C bus data line. If not used, this pin must be connected to GND or VCC.
VCAP	1	1	10	10	—	Internal LDO output pin, this pin must be connected to a 1-μF capacitor to GND. Place the capacitor as close to the device as possible.
VCC	16	16	4	4	—	Power supply.
GND	Thermal pad	Thermal pad	—	—	—	Exposed thermal pad also serves the ground pin for the WQFN package.
AGND	—	—	2	2	—	Analog circuits ground. AGND, PGND and DGND must be connected together.
PGND	—	—	6	6	—	Power ground. AGND, PGND and DGND must be connected together.
DGND	—	—	18	18	—	Digital circuits ground. AGND, PGND and DGND must be connected together.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Voltage on EN, IREF, OUTx, SCL, SDA, VCC	- 0.3	6	V
Voltage on ADDRx	- 0.3	VCC + 0.3	V
Voltage on VCAP	- 0.3	2	V
Continuous power dissipation	Internally limited		
Junction temperature, T <sub>J-MAX</sub>	- 40	125	°C
Storage temperature, T <sub>stg</sub>	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage on VCC	2.7	5.5	V
Voltage on OUTx	0	5.5	V
Voltage on ADDRx, EN, SDA, SCL	0	5.5	V
Operating ambient temperature, T <sub>A</sub>	- 40	85	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LP5009 or LP5012		UNIT
		RUK (QFN)	PW (TSSOP)	
		20 PINS	24 Pins	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	53.7	98.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	55.3	41.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	27.4	53.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.9	5.0	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	27.4	53.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	12.9	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

over operating ambient temperature range ( - 40°C < T<sub>A</sub> < 85°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES (VCC)</b>						
V <sub>VCC</sub>	Supply voltage		2.7		5.5	V
I <sub>VCC</sub>	Shutdown supply current	V <sub>EN</sub> = 0 V		0.2	1	μA
	Standby supply current	V <sub>EN</sub> = 3.3 V, Chip_EN = 0 (bit)		6	10	μA
	Normal-mode supply current	With 10-mA LED current per OUTx		4	6	mA
	Power-save mode supply current	V <sub>EN</sub> = 3.3 V, Chip_EN = 1 (bit), Power_Save_EN = 1 (bit), all the LEDs off duration > t <sub>PSM</sub>		6	10	μA
V <sub>UVR</sub>	Undervoltage restart	V <sub>VCC</sub> rising			2.5	V
V <sub>UVF</sub>	Undervoltage shutdown	V <sub>VCC</sub> falling	2			V
V <sub>UV_HYS</sub>	Undervoltage shutdown hysteresis			0.2		V
<b>OUTPUT STAGE (OUTx)</b>						
I <sub>MAX</sub>	Maximum sink current (OUT0 - OUTx) (For LP5012, x = 11. For LP5009, x = 8.)	V <sub>VCC</sub> in full range, Max_Current_Option = 0 (bit), PWM = 100%			25.5	mA
	Maximum sink current (OUT0 - OUTx) (For LP5012, x = 11. For LP5009, x = 8.)	V <sub>VCC</sub> ≥ 3.3 V, Max_Current_Option = 1 (bit), PWM = 100%			35	
I <sub>LIM</sub>	Internal sink current limit (OUT0 - OUTx) (For LP5012, x = 11. For LP5009, x = 8.)	V <sub>VCC</sub> in full range, Max_Current_Option = 0 (bit), V <sub>IREF</sub> = 0 V	35	55	85	mA
	Internal sink current limit (OUT0 - OUTx) (For LP5012, x = 11. For LP5009, x = 8.)	V <sub>VCC</sub> ≥ 3.3V, Max_Current_Option=1 (bit), V <sub>IREF</sub> = 0 V	40	75	120	
I <sub>lkg</sub>	Leakage current (OUT0 - OUTx) (For LP5012, x = 11. For LP5009, x = 8.)	PWM = 0%		0.1	1	μA
I <sub>ERR_DD</sub>	Device to device current error, I <sub>ERR_DD</sub> = (I <sub>AVE</sub> - I <sub>SET</sub> )/I <sub>SET</sub> × 100%	Channels' current are set to 10 mA. PWM = 100% at 25°C. Already includes the V <sub>IREF</sub> and K <sub>IREF</sub> tolerance	- 5%		5%	
I <sub>ERR_CC</sub>	Channel to channel current error, I <sub>ERR_CC</sub> = (I <sub>OUTX</sub> - I <sub>AVE</sub> )/I <sub>AVE</sub> × 100%	Channels' current are set to 10 mA. PWM = 100% at 25°C. Already includes the V <sub>IREF</sub> and K <sub>IREF</sub> tolerance	- 5%		5%	
V <sub>IREF</sub>	IREF voltage			0.7		V
K <sub>IREF</sub>	IREF ratio			105		
f <sub>PWM</sub>	PWM switching frequency		21	29		kHz
V <sub>SAT</sub>	Output saturation voltage	V <sub>VCC</sub> in full range, Max_Current_Option = 0 (bit), output current set to 20 mA, the voltage when the LED current has dropped 5%		0.25	0.35	V
		V <sub>VCC</sub> ≥ 3.3 V, Max_Current_Option = 1 (bit), output current set to 20 mA, the voltage when the LED current has dropped 5%		0.3	0.4	

## 7.5 Electrical Characteristics (continued)

over operating ambient temperature range ( $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ ) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LOGIC INPUTS (EN, SCL, SDA, ADDR<sub>x</sub>)</b>						
V <sub>IL</sub>	Low level input voltage				0.4	V
V <sub>IH</sub>	High level input voltage		1.4			V
I <sub>LOGIC</sub>	Input current		-1		1	μA
V <sub>SDA</sub>	SDA output low level	I <sub>PULLUP</sub> = 5 mA			0.4	V
<b>PROTECTION CIRCUITS</b>						
T <sub>(TSD)</sub>	Thermal-shutdown junction temperature			160		°C
T <sub>(HYS)</sub>	Thermal shutdown temperature hysteresis			15		°C

## 7.6 Timing Characteristics

over operating ambient temperature range ( $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ ) (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f <sub>OSC</sub>	Internal oscillator frequency		15		MHz
t <sub>PSM</sub>	Power save mode deglitch time	20	30	40	ms
t <sub>EN_H</sub>	EN first rising edge until first I <sup>2</sup> C access			500	μs
t <sub>EN_L</sub>	EN first falling edge until first I <sup>2</sup> C reset			3	μs
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency			400	kHz
1	Hold time (repeated) START condition	0.6			μs
2	Clock low time	1.3			μs
3	Clock high time	600			ns
4	Setup time for a repeated START condition	600			ns
5	Data hold time	0			ns
6	Data setup time	100			ns
7	Rise time of SDA and SCL	20 + 0.1 C <sub>b</sub>		300	ns
8	Fall time of SDA and SCL	15 + 0.1 C <sub>b</sub>		300	ns
9	Setup time for STOP condition	600			ns
10	Bus free time between a STOP and a START condition	1.3			μs
C <sub>b</sub>	Capacitive load parameter for each bus line Load of 1 pF corresponds to one nanosecond.	10		200	pF

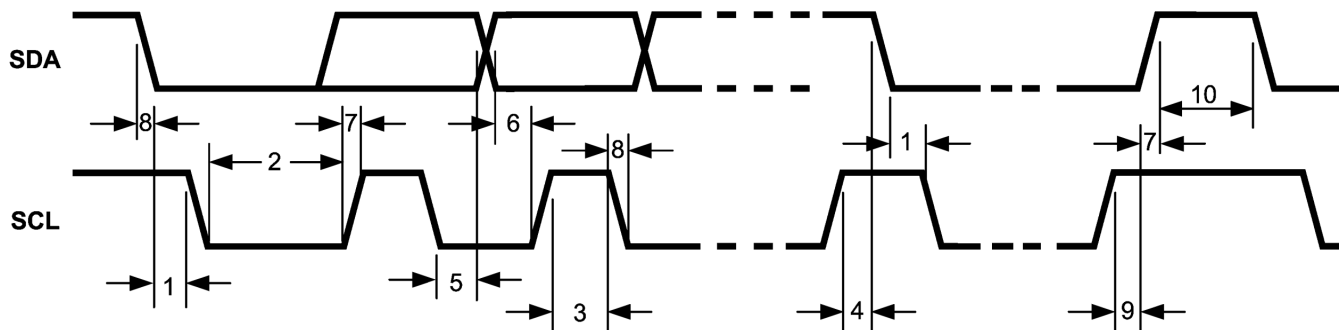


图 7-1. I<sup>2</sup>C Timing Parameters

### 7.7 Typical Characteristics

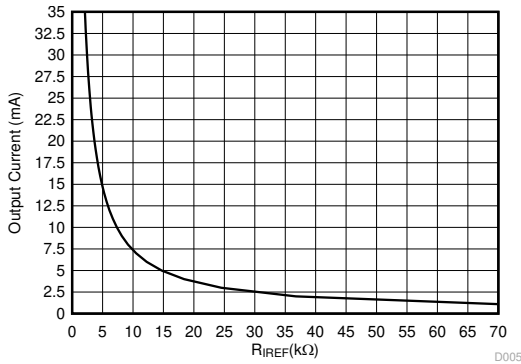
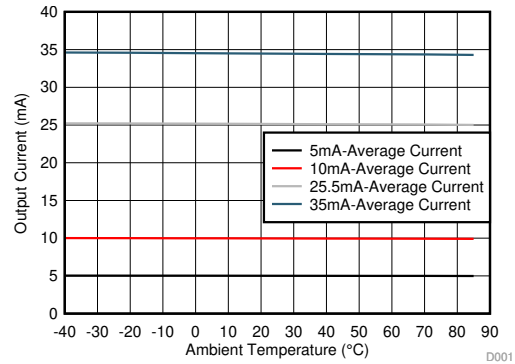
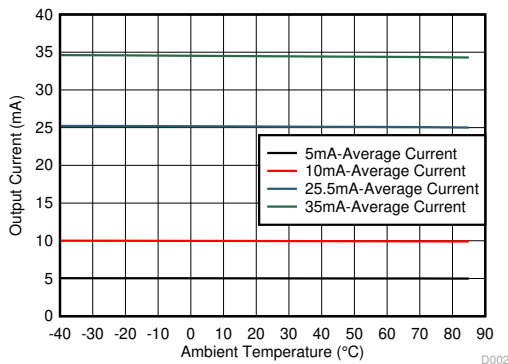


图 7-2. I<sub>OUT</sub> Target vs R<sub>REF</sub>



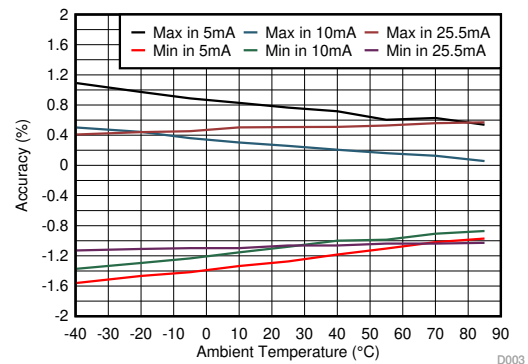
VCC = 3.3 V

图 7-3. Output Current vs Temperature



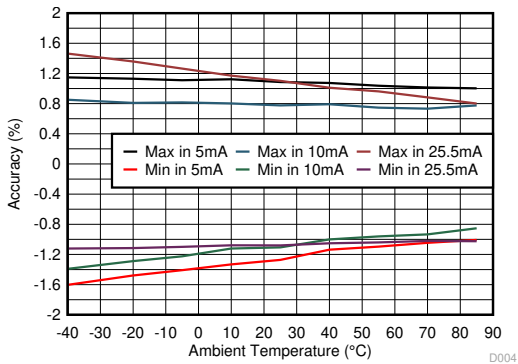
VCC = 5 V

图 7-4. Output Current vs Temperature



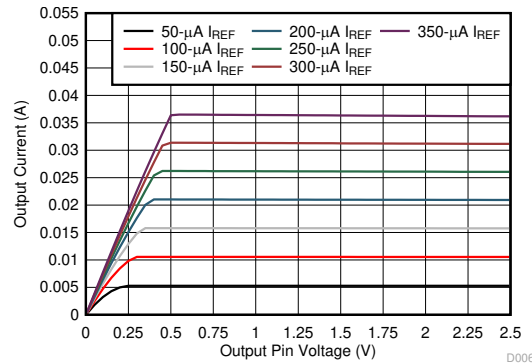
VCC = 3.3 V

图 7-5. Channel-to-Channel Current Accuracy



VCC = 5 V

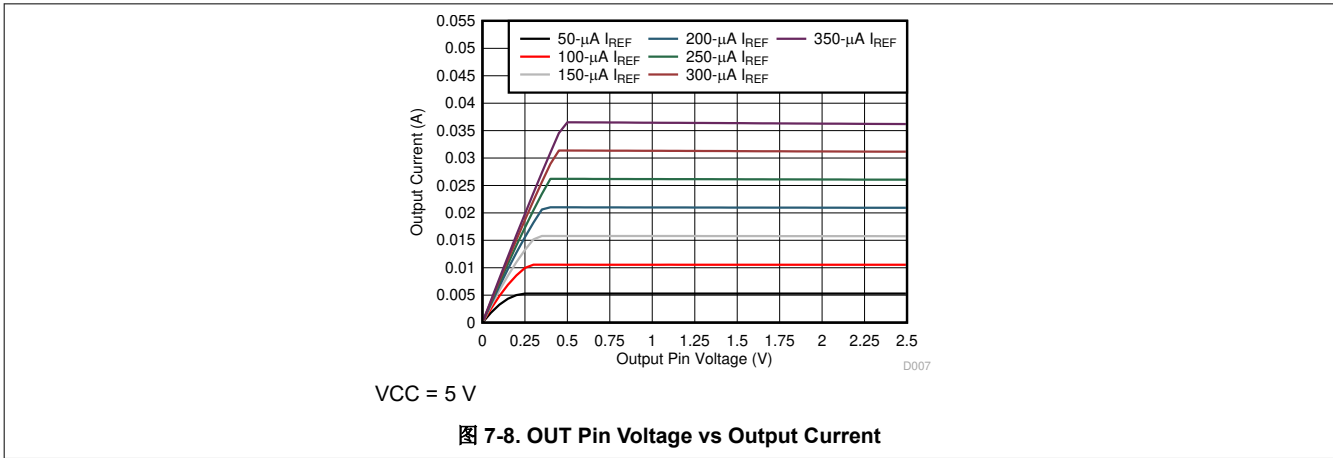
图 7-6. Channel-to-Channel Current Accuracy vs Temperature



VCC = 3.3 V

图 7-7. OUT Pin Voltage vs Current

### 7.7 Typical Characteristics (continued)



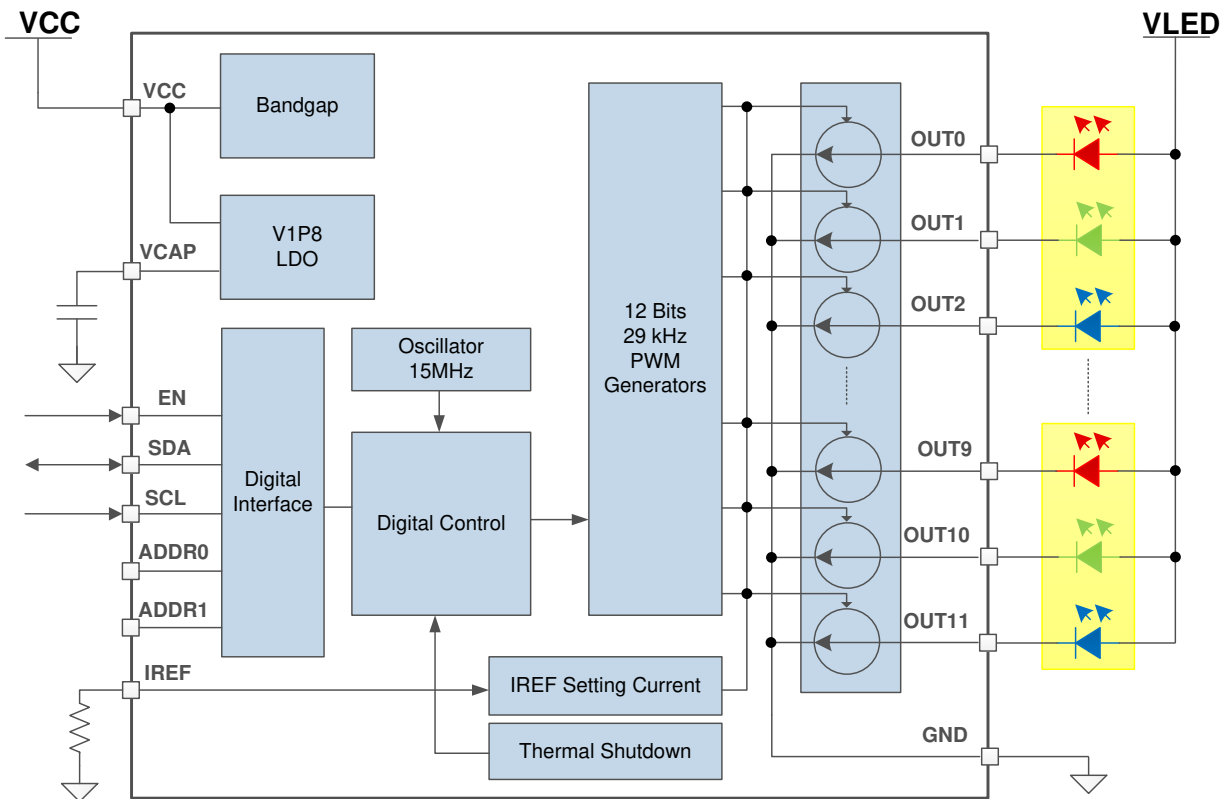
## 8 Detailed Description

### 8.1 Overview

The LP50xx device is an 9- or 12-channel constant-current-sink LED driver. The LP50xx device includes all necessary power rails, an on-chip oscillator, and a two-wire serial I<sup>2</sup>C interface. The maximum constant-current value of all channels is set by a single external resistor. Two hardware address pins allow up to four devices on the same bus. An automatic power-saving mode is implemented to keep the total current consumption under 10  $\mu$ A, which makes the LP50xx device a potential choice for battery-powered end equipment.

The LP50xx device is optimized for RGB LEDs regarding both live effects and software efforts. The LP50xx device controls each LED output with 12-bit PWM resolution at 29-kHz switching frequency, which helps achieve a smooth dimming effect and eliminates audible noise. The independent color-mixing and intensity-control registers make the software coding straightforward. When targeting a fade-in, fade-out type breathing effect, the global RGB bank control reduces the microcontroller loading significantly. The LP50xx device also implements a PWM phase-shifting function to help reduce the input power budget when LEDs turn on simultaneously.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 PWM Control for Each Channel

Most traditional LED drivers are designed for the single-color LEDs, in which the high-resolution PWM generator is used for intensity control only. However, for RGB LEDs, both the color mixing and intensity control must be addressed to achieve the target effect. With the traditional solution, the users must handle the color mixing and intensity control simultaneously with a single PWM register. Several undesired effects occur: the limited dimming steps, the complex software design and the color distortion when using a logarithmic scale control.

The LP50xx device is designed with independent color mixing and intensity control, which makes the RGB LED effects fancy and the control experience straightforward. With the inputs of the color-mixing register and the intensity-control register, the final PWM generator output for each channel is 12-bit resolution and 29-kHz dimming frequency, which helps achieve a smooth dimming effect and eliminates audible noise. See [图 8-1](#).

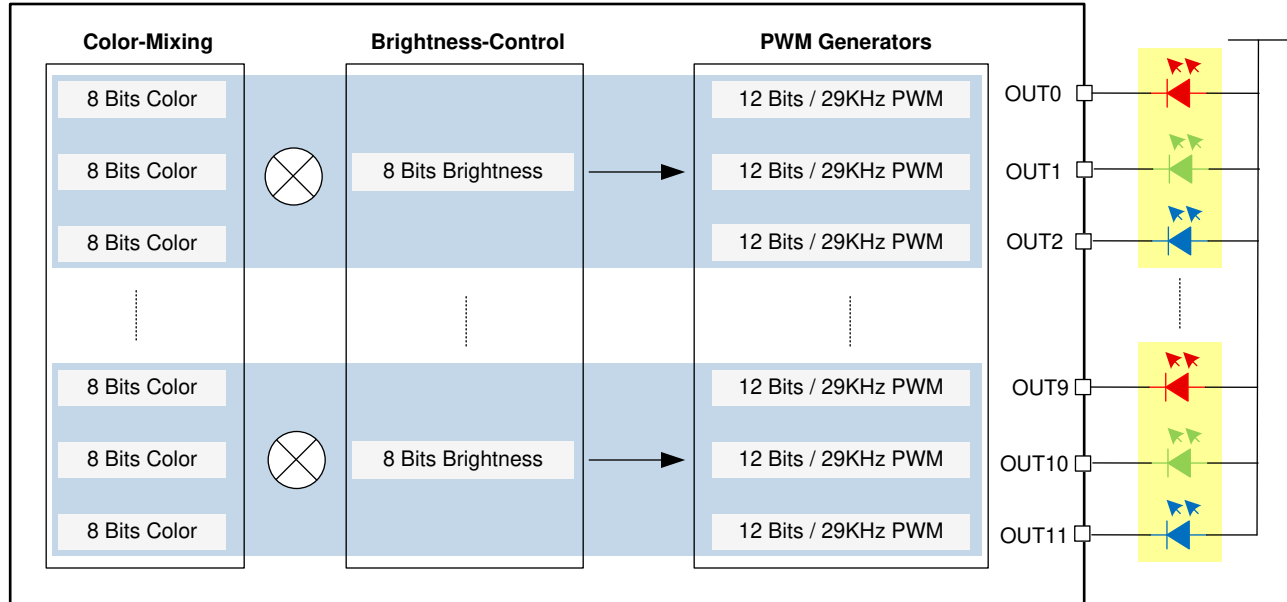


图 8-1. PWM Control Scheme for Each Channel

### 8.3.1.1 Independent Color Mixing Per RGB LED Module

Each output channel has its own individual 8-bit color-setting register (OUTx\_COLOR). The device allows every RGB LED module to achieve >16 million ( $256 \times 256 \times 256$ ) color-mixing.

### 8.3.1.2 Independent Intensity Control Per RGB LED Module

When color is fixed, the independent intensity-control is used to achieve accurate and flexible dimming control for every RGB LED module.

#### 8.3.1.2.1 Intensity-Control Register Configuration

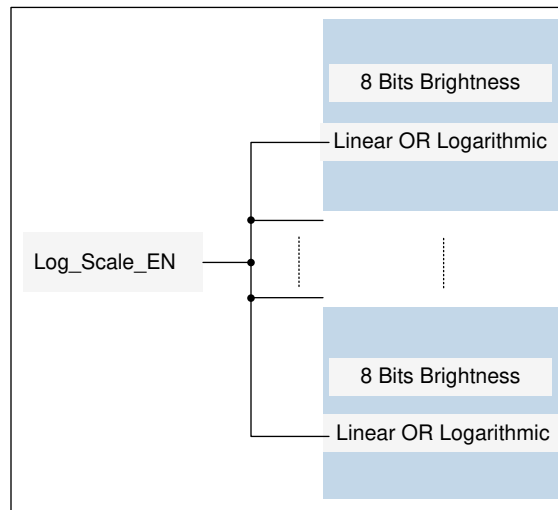
Every three consecutive output channels are assigned to their respective intensity-control register (LEDx\_BRIGHTNESS). For example, OUT0, OUT1, and OUT2 are assigned to LED0\_BRIGHTNESS, so it is recommended to connect the RGB LEDs in the sequence as shown in 表 8-1. The LP50xx device allows 256-step intensity control for each RGB LED module, which helps achieve a smooth dimming effect.

Keeping FFh (default value) in the LED0\_BRIGHTNESS register results in 100% dimming duty cycle. With this setting, users can just configure the color mixing register by channel to achieve the target dimming effect in a single-color LED application.

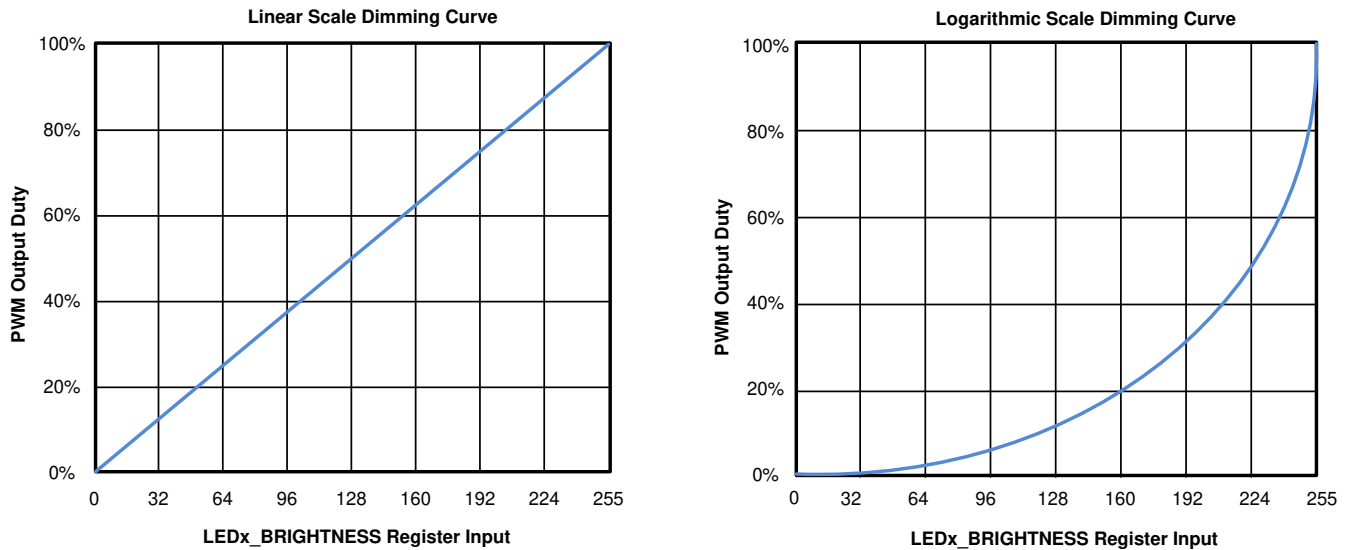
#### 8.3.1.2.2 Logarithmic- or Linear-Scale Intensity Control

For human-eye-friendly visual performance, a logarithmic-scale dimming curve is usually implemented in LED drivers. However, for RGB LEDs, if using a single register to achieve both color mixing and intensity control, color distortion can be observed easily when using a logarithmic scale. The LP50xx device, with independent color-mixing and intensity-control registers, implements the logarithmic scale dimming control inside the intensity control function, which solves the color distortion issue effectively. See 图 8-2. Also, the LP50xx device allows users to configure the dimming scale either logarithmically or linearly through the global Log\_Scale\_EN register. If a special dimming curve is desired, using the linear scale with software correction is the most flexible approach. See 图 8-3.

**Brightness Control**



**图 8-2. Logarithmic- or Linear-Scale Intensity Control**



**图 8-3. Logarithmic vs Linear Dimming Curve**

**8.3.1.3 12-Bit, 29-kHz PWM Generator Per Channel**

**8.3.1.3.1 PWM Generator**

With the inputs of the color mixing and the intensity control, the final output PWM duty cycle is defined as the product obtained by multiplying the color-mixing register value by the related intensity-control register value. The final output PWM duty cycle has 12 bits of control accuracy, which is achieved by a 9 bits of pure PWM resolution and 3 bits of digital dithering control. For 3-bit dithering, every eighth pulse is made 1 LSB longer to increase the average value by 1 / 8th. The LP50xx device allows users to enable or disable the dithering function through the PWM\_Dithering\_EN register. When enabled (default), the output PWM duty-cycle accuracy is 12 bits. When disabled, the output PWM duty-cycle accuracy is 9 bits.

To eliminate the audible noise due to the PWM switching, the LP50xx device sets the PWM switching frequency at 29 kHz, above the 20-kHz human hearing range.

**8.3.1.4 PWM Phase-Shifting**

A PWM phase-shifting scheme allows delaying the time when each LED driver is active. When the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly

decreased. The scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases.

- Phase 1—the rising edge of the PWM pulse is fixed. The falling edge of the pulse is changed when the duty cycle changes. Phase 1 is applied to LED0, LED3, LED6, LED9.
- Phase 2—the middle point of the PWM pulse is fixed. The pulse spreads in both directions when the PWM duty cycle is increased. Phase 2 is applied to LED1, LED4, LED7, LED10.
- Phase 3—the falling edge of the PWM pulse is fixed. The rising edge of the pulse is changed when the duty cycle changes. Phase 3 is applied to LED2, LED5, LED8, LED11.

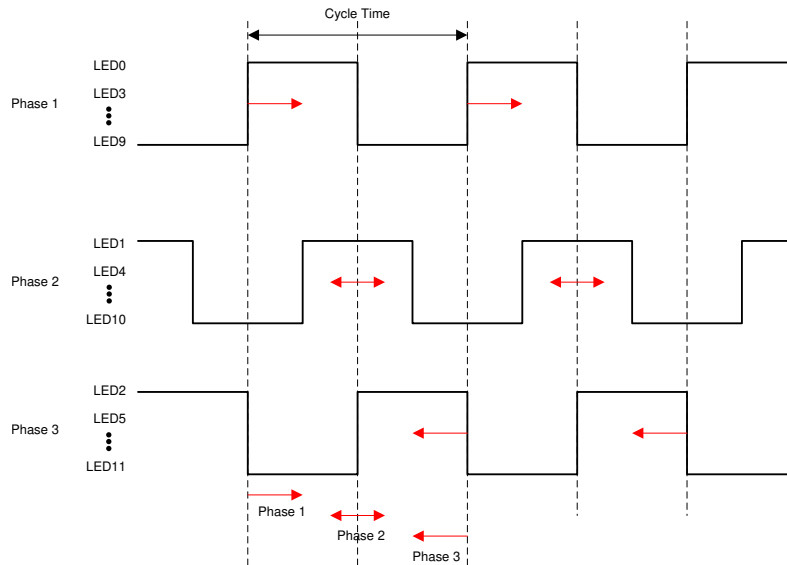


图 8-4. PWM Phase-Shifting

### 8.3.2 LED Bank Control

For most LED-animation effects, like blinking and breathing, all the RGB LEDs have the same lighting pattern. Instead of controlling the individual LED separately, which occupies the microcontroller resources heavily, the LP50xx device provides an easy coding approach, the LED bank control.

Each channel can be configured as either independent control or bank control through the LEDx\_Bank\_EN register. When LEDx\_Bank\_EN = 0 (default), the LED is controlled independently by the related color-mixing and intensity-control registers. When LEDx\_Bank\_EN = 1, the LP50xx device drives the LEDs in LED bank-control mode. The LED bank has its own independent PWM control scheme, which is the same structure as the PWM scheme of each channel. See [PWM Control for Each Channel](#) for more details. When a channel is configured in LED bank-control mode, the related color mixing and intensity control is governed by the bank control registers (BANK\_A\_COLOR, BANK\_B\_COLOR, BANK\_C\_COLOR, and BANK\_BRIGHTNESS) regardless of the inputs on its own color-mixing and intensity-control registers.

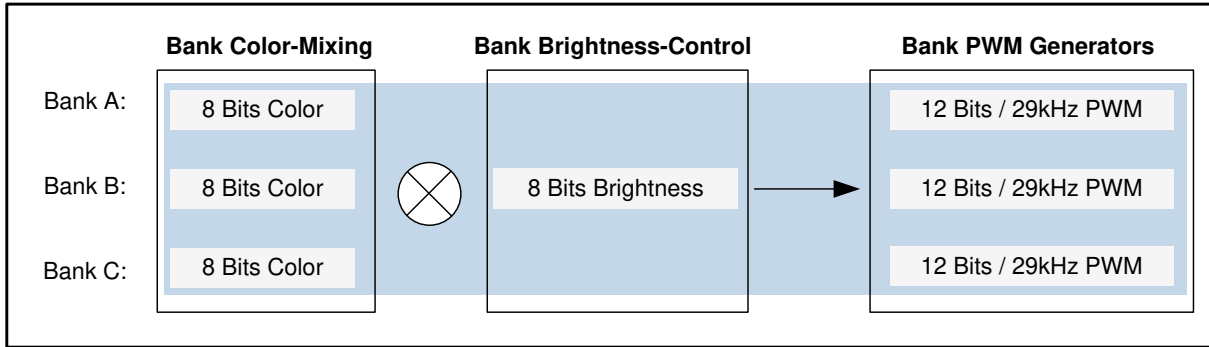


图 8-5. Bank PWM Control Scheme

表 8-1. Bank Number and LED Number Assignment

OUT NUMBER	BANK NUMBER	RGB LED MODULE NUMBER
OUT0	Bank A	LED0
OUT1	Bank B	
OUT2	Bank C	
OUT3	Bank A	LED1
OUT4	Bank B	
OUT5	Bank C	
OUT6	Bank A	LED2
OUT7	Bank B	
OUT8	Bank C	
OUT9 (LP5012 only)	Bank A	LED3
OUT10 (LP5012 only)	Bank B	
OUT11 (LP5012 only)	Bank C	

With the bank control configuration, the LP50xx device enables users to achieve smooth and live LED effects globally with an ultrasimple software effort. 图 8-6 shows an example using LED0 as an independent RGB indicator and others with group breathing effect.

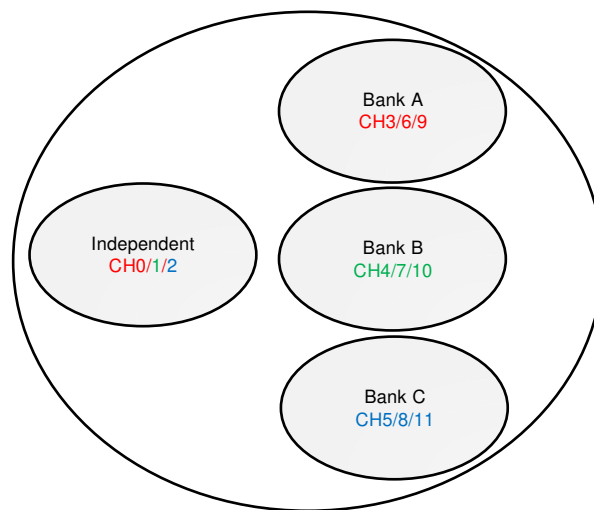


图 8-6. Bank PWM Control Example

### 8.3.3 Current Range Setting

The constant-current value ( $I_{SET}$ ) of all 12 channels is set by a single external resistor,  $R_{IREF}$ . The value of  $R_{IREF}$  can be calculated by [方程式 1](#).

$$R_{IREF} = K_{IREF} \times \frac{V_{IREF}}{I_{SET}} \quad (1)$$

where:

- $K_{IREF} = 105$
- $V_{IREF} = 0.7 \text{ V}$

With the IREF pin floating, the output current is close to zero. With the IREF pin shorted to GND, the LP50xx device provides internal current-limit protection, and the output-channel maximum current is limited to  $I_{LIM}$ .

The LP50xx device supports two levels of maximum output current,  $I_{MAX}$ .

- When  $V_{CC}$  is in the range from 2.7 V to 5.5 V, and the Max\_Current\_Option (bit) = 0,  $I_{MAX} = 25.5 \text{ mA}$ .
- When  $V_{CC}$  is in the range from 3.3 V to 5.5 V, and the Max\_Current\_Option (bit) = 1,  $I_{MAX} = 35 \text{ mA}$ .

### 8.3.4 Automatic Power-Save Mode

When all the LED outputs are inactive, the LP50xx device is able to enter power-save mode automatically, thus lowering idle-current consumption down to  $10 \mu\text{A}$  (typical). Automatic power-save mode is enabled when register bit Power\_Save\_EN = 1 (default) and all the LEDs are off for a duration of > 30 ms. Almost all analog blocks are powered down in power-save mode. If any I<sup>2</sup>C command to the device occurs, the LP50xx device returns to NORMAL mode.

### 8.3.5 Protection Features

#### 8.3.5.1 Thermal Shutdown

The LP50xx device implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to  $160^\circ\text{C}$  (typical), the device switches into shutdown mode. The LP50xx device releases thermal shutdown when the junction temperature of the device is reduced to  $145^\circ\text{C}$  (typical).

#### 8.3.5.2 UVLO

The LP50xx device has an internal comparator that monitors the voltage at  $V_{CC}$ . When  $V_{CC}$  is below  $V_{UVF}$ , reset is active and the LP50xx device is in the INITIALIZATION state.

## 8.4 Device Functional Modes

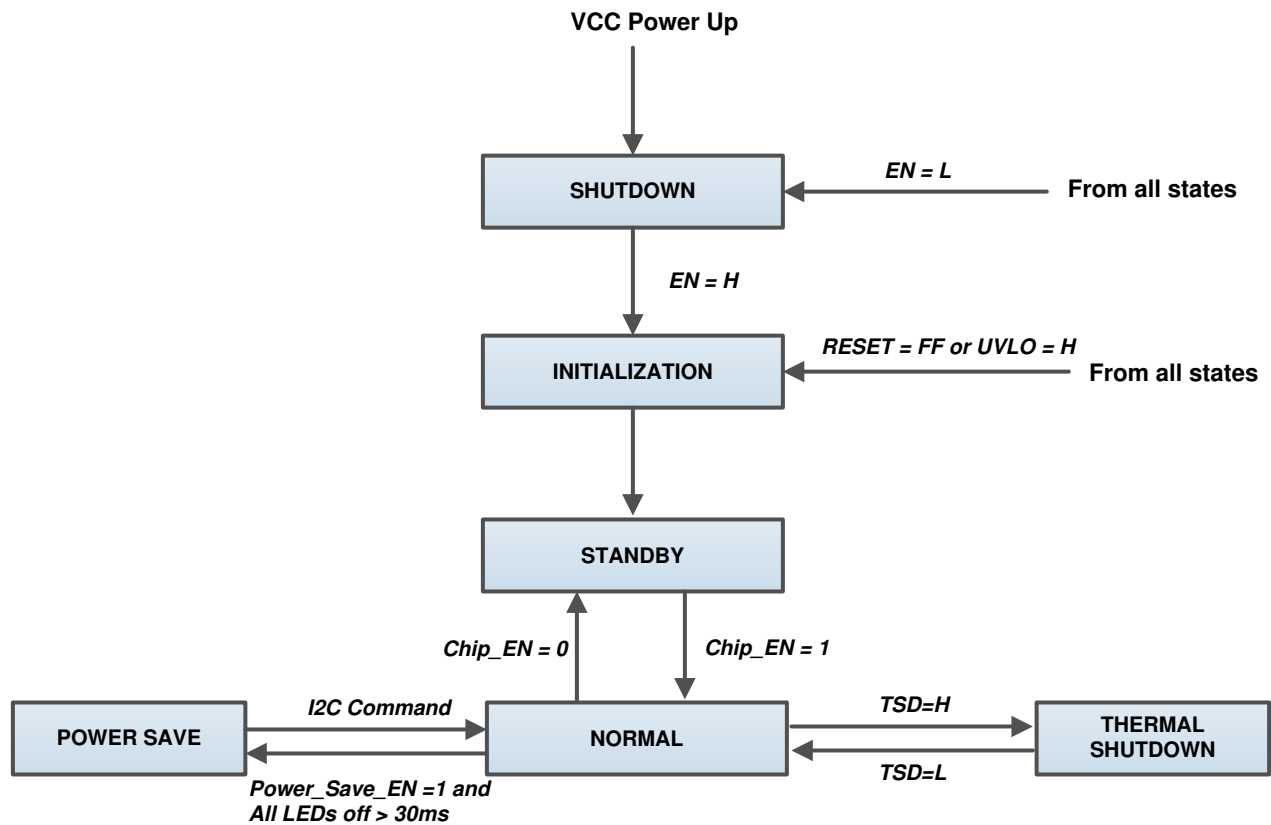


图 8-7. Functional Modes

- **INITIALIZATION:** The device enters into INITIALIZATION mode when EN = H. In this mode, all the registers are reset. Entry can also be from any state, if the RESET (register) = FFh or UVLO is active.
- **NORMAL:** The device enters the NORMAL mode when Chip\_EN (register) = 1.  $I_{CC}$  is 10 mA (typical).
- **POWER SAVE:** The device automatically enters the POWER SAVE mode when Power\_Save\_EN (register) = 1 and all the LEDs are off for a duration of > 30 ms. In POWER SAVE mode, analog blocks are disabled to minimize power consumption, but the registers retain the data and keep it available via I<sup>2</sup>C.  $I_{CC}$  is 10  $\mu$ A (typical). In case of any I<sup>2</sup>C command to this device, it returns to the NORMAL mode.
- **SHUTDOWN:** The device enters into SHUTDOWN mode from all states on V<sub>CC</sub> power up or when EN = L.  $I_{CC}$  is < 1  $\mu$ A (maximum).
- **STANDBY:** The device enters the STANDBY mode when Chip\_EN (register) = 0. In this mode, all the OUTx pins are shut down, but the registers retain the data and keep it available via I<sup>2</sup>C. STANDBY is the low-power-consumption mode, when all circuit functions are disabled.  $I_{CC}$  is 10  $\mu$ A (typical).
- **THERMAL SHUTDOWN:** The device automatically enters the THERMAL SHUTDOWN mode when the junction temperature exceeds 160°C (typical). In this mode, all the OUTx outputs are shut down. If the junction temperature decreases below 145°C (typical), the device returns to the NORMAL mode.

## 8.5 Programming

### 8.5.1 I<sup>2</sup>C Interface

The I<sup>2</sup>C-compatible two-wire serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA) and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock, SCL. The SCL and SDA lines must each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle.

#### 8.5.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when the clock signal is LOW.

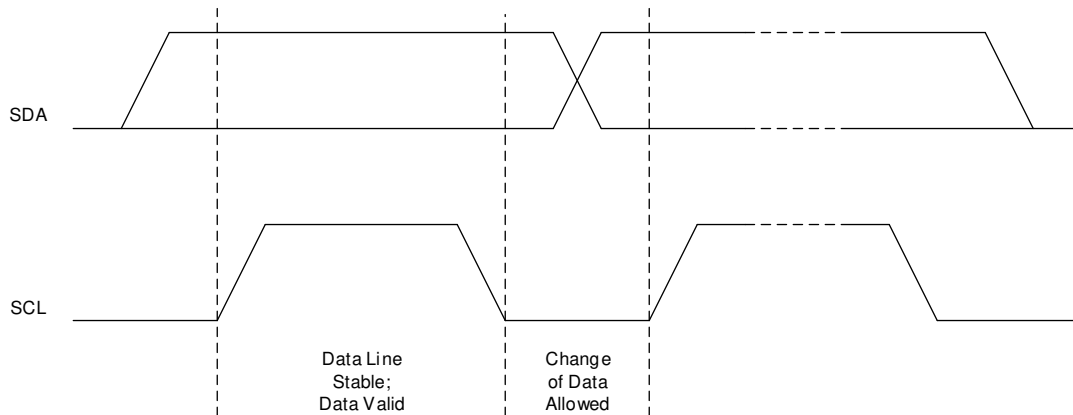


图 8-8. Data Validity

#### 8.5.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus master always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus master can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

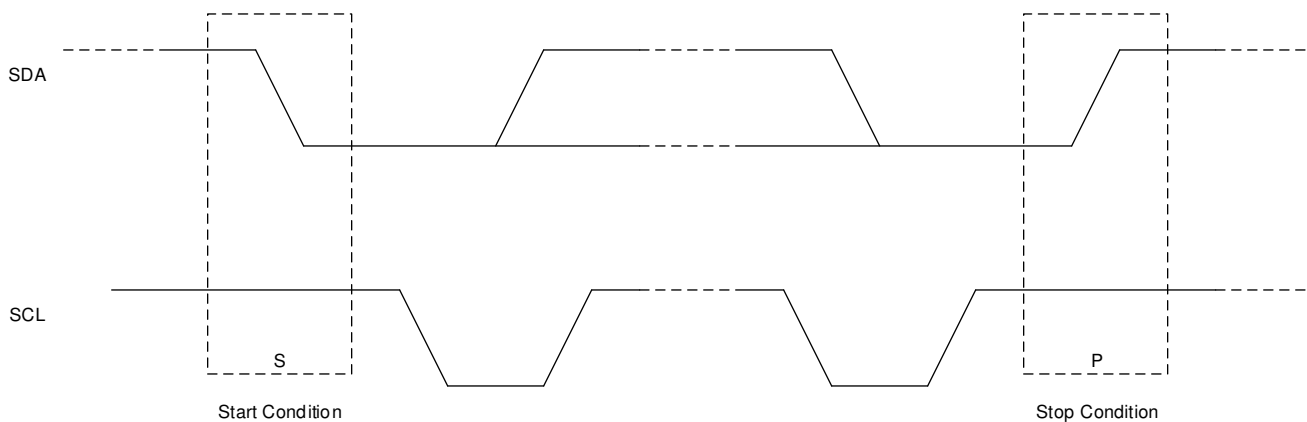


图 8-9. Start and Stop Conditions

### 8.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most-significant bit (MSB) being transferred first. Each byte of data must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the ninth clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge-after-every-byte rule. When the master is the receiver, it must indicate to the transmitter an end of data by not acknowledging (negative acknowledge) the last byte clocked out of the slave. This negative acknowledge still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE, and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

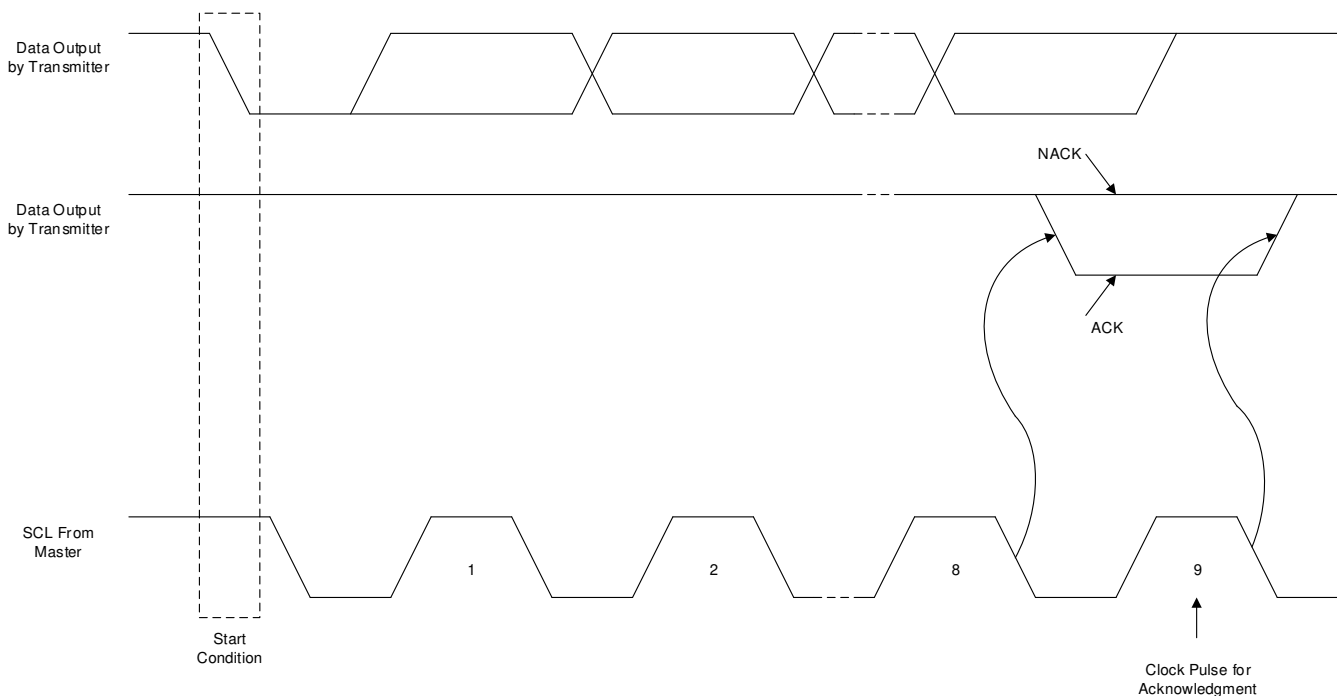


图 8-10. Acknowledge and Not Acknowledge on I<sup>2</sup>C Bus

#### 8.5.1.4 I<sup>2</sup>C Slave Addressing

The device slave address is defined by connecting GND or VCC to the ADDR0 and ADDR1 pins. A total of four independent slave addresses can be realized by combinations when GND or VCC is connected to the ADDR0 and ADDR1 pins (see 表 8-2 and 表 8-3).

The device responds to a broadcast slave address regardless of the setting of the ADDR0 and ADDR1 pins. Global writes to the broadcast address can be used for configuring all devices simultaneously. The device supports global read using a broadcast address; however, the data read is only valid if all devices on the I<sup>2</sup>C bus contain the same value in the addressed register.

表 8-2. Slave-Address Combinations

ADDR1	ADDR0	SLAVE ADDRESS	
		INDEPENDENT	BROADCAST
GND	GND	0010100	0001100
GND	VCC	0010101	
VCC	GND	0010110	
VCC	VCC	0010111	

表 8-3. Chip Address

	SLAVE ADDRESS							R/ $\bar{W}$
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Independent	0	0	1	0	1	ADDR1	ADDR0	1 or 0
Broadcast	0	0	0	1	1	0	0	1 or 0

### 8.5.1.5 Control-Register Write Cycle

- The master device generates a start condition.
- The master device sends the slave address (7 bits) and the data direction bit ( $R/\bar{W} = 0$ ).
- The slave device sends an acknowledge signal if the slave address is correct.
- The master device sends the control register address (8 bits).
- The slave device sends an acknowledge signal.
- The master device sends the data byte to be written to the addressed register.
- The slave device sends an acknowledge signal.
- If the master device sends further data bytes, the control register address of the slave is incremented by 1 after the acknowledge signal. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The write cycle ends when the master device creates a stop condition.

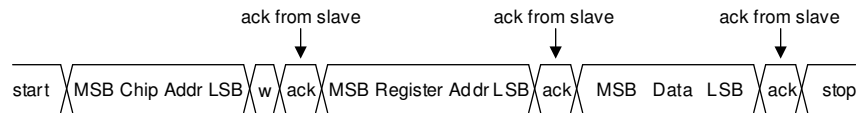


图 8-11. Write Cycle

### 8.5.1.6 Control-Register Read Cycle

- The master device generates a start condition.
- The master device sends the slave address (7 bits) and the data direction bit ( $R/\bar{W} = 0$ ).
- The slave device sends an acknowledge signal if the slave address is correct.
- The master device sends the control register address (8 bits).
- The slave device sends an acknowledge signal.
- The master device generates a repeated-start condition.
- The master device sends the slave address (7 bits) and the data direction bit ( $R/\bar{W} = 1$ ).
- The slave device sends an acknowledge signal if the slave address is correct.
- The slave device sends the data byte from the addressed register.
- If the master device sends an acknowledge signal, the control-register address is incremented by 1. The slave device sends the data byte from the addressed register. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The read cycle ends when the master device does not generate an acknowledge signal after a data byte and generates a stop condition.

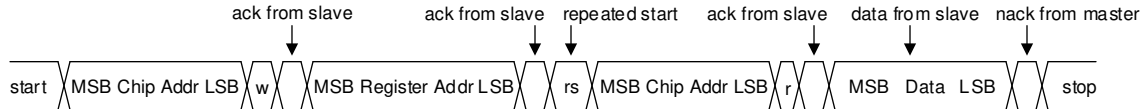


图 8-12. Read Cycle

### 8.5.1.7 Auto-Increment Feature

The auto-increment feature allows writing or reading several consecutive registers within one transmission. For example, when an 8-bit word is sent to the device, the internal address index counter is incremented by 1, and the next register is written. The auto-increment feature is enabled by default and can be disabled by setting the Auto\_Incr\_EN bit = 0 in the DEVICE\_CONFIG1 register. The auto-increment feature is applied for the full register address from 0h to FFh.

## 8.6 Register Maps

表 8-4 lists the memory-mapped registers of the device.

**表 8-4. Register Maps**

REGISTER NAME	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	DEF-AULT	
DEVICE_CONFIG0	00h	R/ W	RESERVED	Chip_EN	RESERVED						00h	
DEVICE_CONFIG1	01h	R/ W	RESERVED		Log_Scale_EN	Power_Save_EN	Auto_Incr_EN	PWM_Dithering_EN	Max_Current_Option	LED_Global Off	3Ch	
LED_CONFIG0	02h	R/ W	RESERVED				LED3_Bank_EN (Only for LP5012)	LED2_Bank_EN	LED1_Bank_EN	LED0_Bank_EN	00h	
BANK_BRIGHTNESS	03h	R/ W	Bank_Brightness									FFh
BANK_A_COLOR	04h	R/ W	Bank_A_Color									00h
BANK_B_COLOR	05h	R/ W	Bank_B_Color									00h
BANK_C_COLOR	06h	R/ W	Bank_C_Color									00h
LED0_BRIGHTNESS	07h	R/ W	LED0_Brightness									FFh
LED1_BRIGHTNESS	08h	R/ W	LED1_Brightness									FFh
LED2_BRIGHTNESS	09h	R/ W	LED2_Brightness									FFh
LED3_BRIGHTNESS	0Ah	R/ W	LED3_Brightness (Only for LP5012)									FFh
OUT0_COLOR	0Bh	R/ W	OUT0_Color									00h
OUT1_COLOR	0Ch	R/ W	OUT1_Color									00h
OUT2_COLOR	0Dh	R/ W	OUT2_Color									00h
OUT3_COLOR	0Eh	R/ W	OUT3_Color									00h
OUT4_COLOR	0Fh	R/ W	OUT4_Color									00h
OUT5_COLOR	10h	R/ W	OUT5_Color									00h
OUT6_COLOR	11h	R/ W	OUT6_Color									00h
OUT7_COLOR	12h	R/ W	OUT7_Color									00h
OUT8_COLOR	13h	R/ W	OUT8_Color									00h

表 8-4. Register Maps (continued)

REGISTER NAME	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	DEF-AULT
OUT9_COLOR	14h	R/ $\bar{W}$	OUT9_Color (Only for LP5012)								00h
OUT10_COLOR	15h	R/ $\bar{W}$	OUT10_Color (Only for LP5012)								00h
OUT11_COLOR	16h	R/ $\bar{W}$	OUT11_Color (Only for LP5012)								00h
RESET	17h	W	Reset								00h

表 8-5. Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 8.6.1 DEVICE\_CONFIG0 (Address = 0h) [reset = 0h]

DEVICE\_CONFIG0 is shown in 图 8-13 and described in 表 8-6.

Return to 表 8-4.

图 8-13. DEVICE\_CONFIG0 Register

7	6	5	4	3	2	1	0
RESERVED	Chip_EN	RESERVED					
R/ W-0h	R/ W-0h	R/ W-0h					

表 8-6. DEVICE\_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/ W	0h	Reserved
6	Chip_EN	R/ W	0h	1 = LP50xx enabled 0 = LP50xx not enabled
5 - 0	RESERVED	R/ W	0h	Reserved

### 8.6.2 DEVICE\_CONFIG1 (Address = 1h) [reset = 3Ch]

DEVICE\_CONFIG1 is shown in 图 8-14 and described in 表 8-7.

Return to 表 8-4.

图 8-14. DEVICE\_CONFIG1 Register

7	6	5	4	3	2	1	0
RESERVED	Log_Scale_EN	Power_Save_EN	Auto_Incr_EN	PWM_Dithering_EN	Optional_Headroom	LED_Global Off	
R/ W-0h	R/ W-1h	R/ W-1h	R/ W-1h	R/ W-1h	R/ W-0h	R/ W-0h	

表 8-7. DEVICE\_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 6	RESERVED	R/ W	0h	Reserved
5	Log_Scale_EN	R/ W	1h	1 = Logarithmic scale dimming curve enabled 0 = Linear scale dimming curve enabled
4	Power_Save_EN	R/ W	1h	1 = Automatic power-saving mode enabled 0 = Automatic power-saving mode not enabled
3	Auto_Incr_EN	R/ W	1h	1 = Automatic increment mode enabled 0 = Automatic increment mode not enabled
2	PWM_Dithering_EN	R/ W	1h	1 = PWM dithering mode enabled 0 = PWM dithering mode not enabled
1	Max_Current_Option	R/ W	0h	1 = Output maximum current $I_{MAX} = 35$ mA. 0 = Output maximum current $I_{MAX} = 25.5$ mA.

表 8-7. DEVICE\_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LED_Global Off	R/ W	0h	1 = Shut down all LEDs 0 = Normal operation

### 8.6.3 LED\_CONFIG0 (Address = 2h) [reset = 00h]

LED\_CONFIG0 is shown in 图 8-15 and described in 表 8-8.

Return to 表 8-4.

图 8-15. LED\_CONFIG0 Register

7	6	5	4	3	2	1	0
RESERVED				LED3_Bank_EN	LED2_Bank_EN	LED1_Bank_EN	LED0_Bank_EN
R/ W-0h				R/ W-0h	R/ W-0h	R/ W-0h	R/ W-0h

表 8-8. LED\_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/ W	0h	Reserved
3	LED3_Bank_EN	R/ W	0h	1 = LED3 bank control mode enabled 0 = LED3 independent control mode enabled
2	LED2_Bank_EN	R/ W	0h	1 = LED2 bank control mode enabled 0 = LED2 independent control mode enabled
1	LED1_Bank_EN	R/ W	0h	1 = LED1 bank control mode enabled 0 = LED1 independent control mode enabled
0	LED0_Bank_EN	R/ W	0h	1 = LED0 bank control mode enabled 0 = LED0 independent control mode enabled

### 8.6.4 BANK\_BRIGHTNESS (Address = 3h) [reset = FFh]

BANK\_BRIGHTNESS is shown in 图 8-16 and described in 表 8-9.

Return to 表 8-4.

图 8-16. BANK\_BRIGHTNESS Register

7	6	5	4	3	2	1	0
Bank_Brightness							
R/ W-FFh							

表 8-9. BANK\_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	Bank_Brightness	R/ W	FFh	FFh = 100% of full brightness ... 80h = 50% of full brightness ... 00h = 0% of full brightness

### 8.6.5 BANK\_A\_COLOR (Address = 4h) [reset = 00h]

BANK\_A\_COLOR is shown in 图 8-17 and described in 表 8-10.

Return to 表 8-4.

图 8-17. BANK\_A\_COLOR Register

7	6	5	4	3	2	1	0
Bank_A_Color							

**图 8-17. BANK\_A\_COLOR Register (continued)**

R/  $\bar{W}$ -0h

**表 8-10. BANK\_A\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	Bank_A_Color	R/ $\bar{W}$	0h	FFh = The color mixing percentage is 100%. ... 80h = The color mixing percentage is 50%. ... 00h = The color mixing percentage is 0%.

### 8.6.6 BANK\_B\_COLOR (Address = 5h) [reset = 00h]

BANK\_B\_COLOR is shown in 图 8-18 and described in 表 8-11.

Return to 表 8-4.

图 8-18. BANK\_B\_COLOR Register

7	6	5	4	3	2	1	0
Bank_B_Color							
R/ $\bar{W}$ -0h							

表 8-11. BANK\_B\_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	Bank_B_Color	R/ $\bar{W}$	0h	FFh = The color mixing percentage is 100%. ... 80h = The color mixing percentage is 50%. ... 00h = The color mixing percentage is 0%.

### 8.6.7 BANK\_C\_COLOR (Address = 6h) [reset = 00h]

BANK\_C\_COLOR is shown in 图 8-19 and described in 表 8-12.

Return to 表 8-4.

图 8-19. BANK\_C\_COLOR Register

7	6	5	4	3	2	1	0
Bank_C_Color							
R/ $\bar{W}$ -0h							

表 8-12. BANK\_C\_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	Bank_C_Color	R/ $\bar{W}$	0h	FFh = The color mixing percentage is 100%. ... 80h = The color mixing percentage is 50%. ... 00h = The color mixing percentage is 0%.

### 8.6.8 LED0\_BRIGHTNESS (Address = 7h) [reset = FFh]

LED0\_BRIGHTNESS is shown in 图 8-20 and described in 表 8-13.

Return to 表 8-4.

图 8-20. LED0\_BRIGHTNESS Register

7	6	5	4	3	2	1	0
LED0_Brightness							
R/ $\bar{W}$ -FFh							

表 8-13. LED0\_BRIGHTNESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	LED0_Brightness	R/ $\bar{W}$	FFh	FFh = 100% of full intensity ... 80h = 50% of full intensity ... 00h = 0% of full intensity

### 8.6.9 LED1\_BRIGHTNESS (Address = 8h) [reset = FFh]

LED1\_BRIGHTNESS is shown in [图 8-21](#) and described in [表 8-14](#).

Return to [表 8-4](#).

**图 8-21. LED1\_BRIGHTNESS Register**

7	6	5	4	3	2	1	0
LED1_Brightness							
R/ W-FFh							

**表 8-14. LED1\_BRIGHTNESS Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	LED1_Brightness	R/ W	FFh	FFh = 100% of full intensity ... 80h = 50% of full intensity ... 00h = 0% of full intensity

### 8.6.10 LED2\_BRIGHTNESS (Address = 9h) [reset = FFh]

LED2\_BRIGHTNESS is shown in [图 8-22](#) and described in [表 8-15](#).

Return to [表 8-4](#).

**图 8-22. LED2\_BRIGHTNESS Register**

7	6	5	4	3	2	1	0
LED2_Brightness							
R/ W-FFh							

**表 8-15. LED2\_BRIGHTNESS Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	LED2_Brightness	R/ W	FFh	FFh = 100% of full intensity ... 80h = 50% of full intensity ... 00h = 0% of full intensity

### 8.6.11 LED3\_BRIGHTNESS (Address = 0Ah) [reset = FFh]

LED3\_BRIGHTNESS is shown in [图 8-23](#) and described in [表 8-16](#).

Return to [表 8-4](#).

**图 8-23. LED3\_BRIGHTNESS Register**

7	6	5	4	3	2	1	0
LED3_Brightness							
R/ W-FFh							

**表 8-16. LED3\_BRIGHTNESS Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	LED3_Brightness	R/ W	FFh	FFh = 100% of full intensity ... 80h = 50% of full intensity ... 00h = 0% of full intensity

### 8.6.12 OUT0\_COLOR (Address = 0Bh) [reset = 00h]

OUT0\_COLOR is shown in 图 8-24 and described in 表 8-17.

Return to 表 8-4.

图 8-24. OUT0\_COLOR Register

7	6	5	4	3	2	1	0
OUT0_Color							
R/ W-00h							

表 8-17. OUT0\_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	OUT0_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.13 OUT1\_COLOR (Address = 0Ch) [reset = 00h]

OUT1\_COLOR is shown in 图 8-25 and described in 表 8-18.

Return to 表 8-4.

图 8-25. OUT1\_COLOR Register

7	6	5	4	3	2	1	0
OUT1_Color							
R/ W-00h							

表 8-18. OUT1\_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	OUT1_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.14 OUT2\_COLOR (Address = 0Dh) [reset = 00h]

OUT2\_COLOR is shown in 图 8-26 and described in 表 8-19.

Return to 表 8-4.

图 8-26. OUT2\_COLOR Register

7	6	5	4	3	2	1	0
OUT2_Color							
R/ W-00h							

表 8-19. OUT2\_COLOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	OUT2_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.15 OUT3\_COLOR (Address = 0Eh) [reset = 00h]

OUT3\_COLOR is shown in [图 8-27](#) and described in [表 8-20](#).

Return to [表 8-4](#).

**图 8-27. OUT3\_COLOR Register**

7	6	5	4	3	2	1	0
OUT3_Color							
R/ W-00h							

**表 8-20. OUT3\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	OUT3_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.16 OUT4\_COLOR (Address = 0Fh) [reset = 00h]

OUT4\_COLOR is shown in [图 8-28](#) and described in [表 8-21](#).

Return to [表 8-4](#).

**图 8-28. OUT4\_COLOR Register**

7	6	5	4	3	2	1	0
OUT4_Color							
R/ W-00h							

**表 8-21. OUT4\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	OUT4_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.17 OUT5\_COLOR (Address = 10h) [reset = 00h]

OUT5\_COLOR is shown in [图 8-29](#) and described in [表 8-22](#).

Return to [表 8-4](#).

**图 8-29. OUT5\_COLOR Register**

7	6	5	4	3	2	1	0
OUT5_Color							
R/ W-00h							

**表 8-22. OUT5\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	OUT5_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.18 OUT6\_COLOR (Address = 11h) [reset = 00h]

OUT6\_COLOR is shown in [图 8-30](#) and described in [表 8-23](#).

Return to [表 8-4](#).

**图 8-30. OUT6\_COLOR Register**

7	6	5	4	3	2	1	0
OUT6_Color							
R/ W-00h							

**表 8-23. OUT6\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	OUT6_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.19 OUT7\_COLOR (Address = 12h) [reset = 00h]

OUT7\_COLOR is shown in [图 8-31](#) and described in [表 8-24](#).

Return to [表 8-4](#).

**图 8-31. OUT7\_COLOR Register**

7	6	5	4	3	2	1	0
OUT7_Color							
R/ W-00h							

**表 8-24. OUT7\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	OUT7_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.20 OUT8\_COLOR (Address = 13h) [reset = 00h]

OUT8\_COLOR is shown in [图 8-32](#) and described in [表 8-25](#).

Return to [表 8-4](#).

**图 8-32. OUT8\_COLOR Register**

7	6	5	4	3	2	1	0
OUT8_Color							
R/ W-00h							

**表 8-25. OUT8\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	OUT8_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.21 OUT9\_COLOR (Address = 14h) [reset = 00h]

OUT9\_COLOR is shown in [图 8-33](#) and described in [表 8-26](#).

Return to [表 8-4](#).

**图 8-33. OUT9\_COLOR Register**

7	6	5	4	3	2	1	0
OUT9_Color							
R/ W-00h							

**表 8-26. OUT9\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	OUT9_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.22 OUT10\_COLOR (Address = 15h) [reset = 00h]

OUT10\_COLOR is shown in [图 8-34](#) and described in [表 8-27](#).

Return to [表 8-4](#).

**图 8-34. OUT10\_COLOR Register**

7	6	5	4	3	2	1	0
OUT10_Color							
R/ W-00h							

**表 8-27. OUT10\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	OUT10_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.23 OUT11\_COLOR (Address = 16h) [reset = 00h]

OUT11\_COLOR is shown in [图 8-35](#) and described in [表 8-28](#).

Return to [表 8-4](#).

**图 8-35. OUT11\_COLOR Register**

7	6	5	4	3	2	1	0
OUT11_Color							
R/ W-00h							

**表 8-28. OUT11\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	OUT11_Color	R/ W	00h	FFh = The color mixing percentage is 0%. ... 80h =The color mixing percentage is 50%. ... 00h = The color mixing percentage is 100%.

### 8.6.24 RESET (Address = 17h) [reset = 00h]

RESET is shown in [图 8-36](#) and described in [表 8-29](#).

Return to [表 8-4](#).

**图 8-36. RESET Register**

7	6	5	4	3	2	1	0
Reset							
W-00h							

**表 8-29. OUT14\_COLOR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7 - 0	Reset	W	00h	FFh = Reset all the registers to default value.

## 9 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LP50xx device is a 9- or 12-channel constant-current-sink LED driver. The LP50xx device improves the user experience in color mixing and intensity control, for both live effects and coding effort. The optimized performance for RGB LEDs makes it a good choice for human-machine interaction applications.

### 9.2 Typical Application

The LP50xx design supports up to four devices in parallel with different configurations on the ADDR0 and ADDR1 pins.

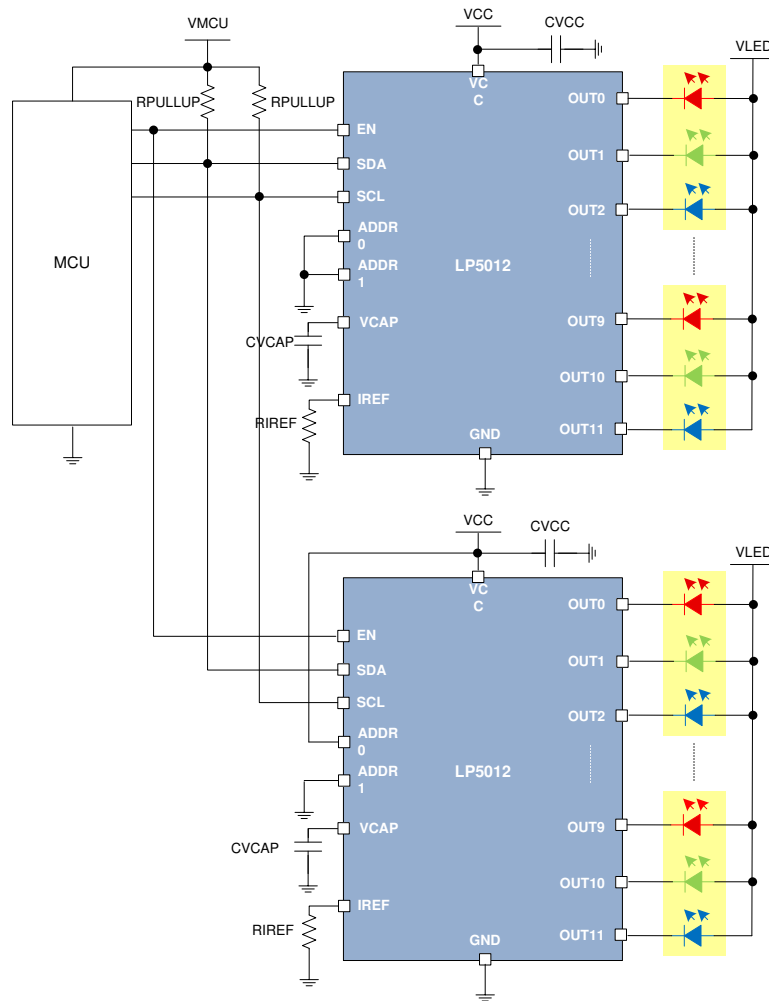


图 9-1. Driving Dual LP5012 Application Example

### 9.2.1 Design Requirements

Set the LED current to 15 mA using the  $R_{IREF}$  resistor. Select the proper value for the other external components, like VCAP pin capacitor and the SCL/SDA pullup resistors.

### 9.2.2 Detailed Design Procedure

LP50xx scales up the reference current ( $I_{REF}$ ) set by the external resistor ( $R_{IREF}$ ) to sink the output current ( $I_{OUT}$ ) at each output port. The following formula can be used to calculate the external resistor ( $R_{IREF}$ ):

$$R_{IREF} = K_{IREF} \times \frac{V_{IREF}}{I_{SET}} \quad (2)$$

The SCL and SDA lines must each have a pullup resistor placed somewhere on the line (the pullup resistors are normally located on the bus master). In typical applications, values of 1.8 k $\Omega$  to 4.7 k $\Omega$  are used.

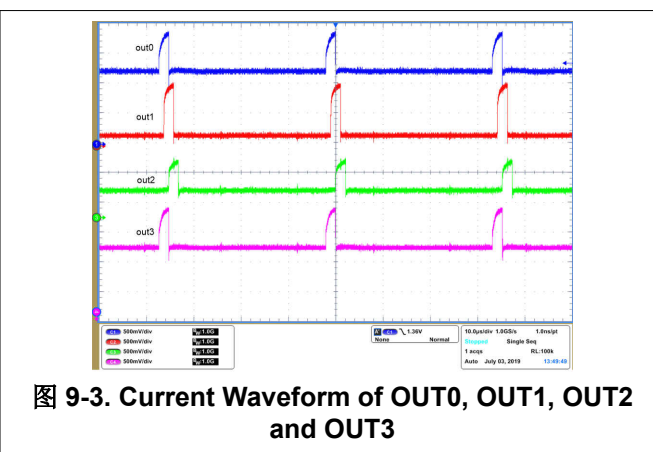
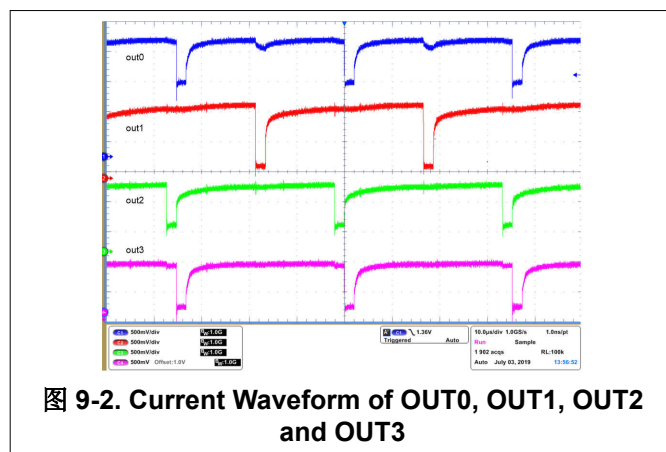
VCAP is internal LDO output pin. This pin must be connected through a 1- $\mu$ F capacitor to GND. Place the capacitor as close to the device as possible.

TI recommends having a 1- $\mu$ F capacitor between VCC and GND to ensure proper operation. Place the capacitor as close to the device as possible.

### 9.2.3 Application Curves

The test condition for [图 9-2](#) is that the testing under bank control, with the register' s (0x04, 0x05, 0x06) value is 0xF0.

The test condition for [图 9-3](#) is that the testing under bank control, with the register' s (0x04, 0x05, 0x06) value is 0x0F.



## 10 Power Supply Recommendations

The device is designed to operate from a  $V_{VCC}$  input-voltage supply range from 2.7 V and 5.5 V. This input supply must be well-regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even in a load-transition condition (start-up or rapid intensity change). The resistance of the input supply rail must be low enough that the input-current transient does not cause a drop below a 2.7-V level in the LP50xx  $V_{VCC}$  supply voltage.

## 11 Layout

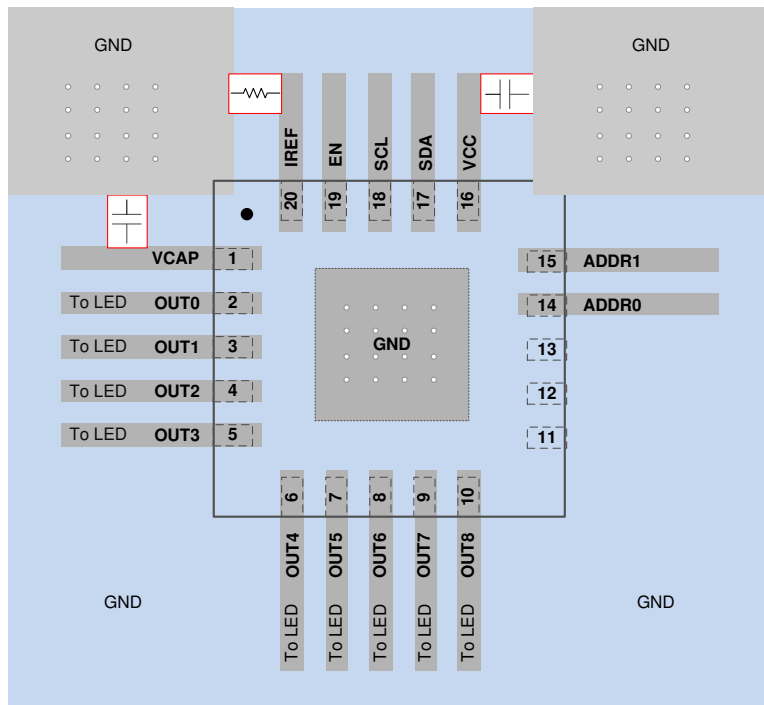
### 11.1 Layout Guidelines

To prevent thermal shutdown, the junction temperature,  $T_J$ , must be less than  $T_{(TSD)}$ . If the voltage drop across the output channels is high, the device power dissipation can be large. The LP50xx device has very good thermal performance because of the thermal pad design; however, the PCB layout is also very important to ensure that the device has good thermal performance. Good PCB design can optimize heat transfer, which is essential for the long-term reliability of the device.

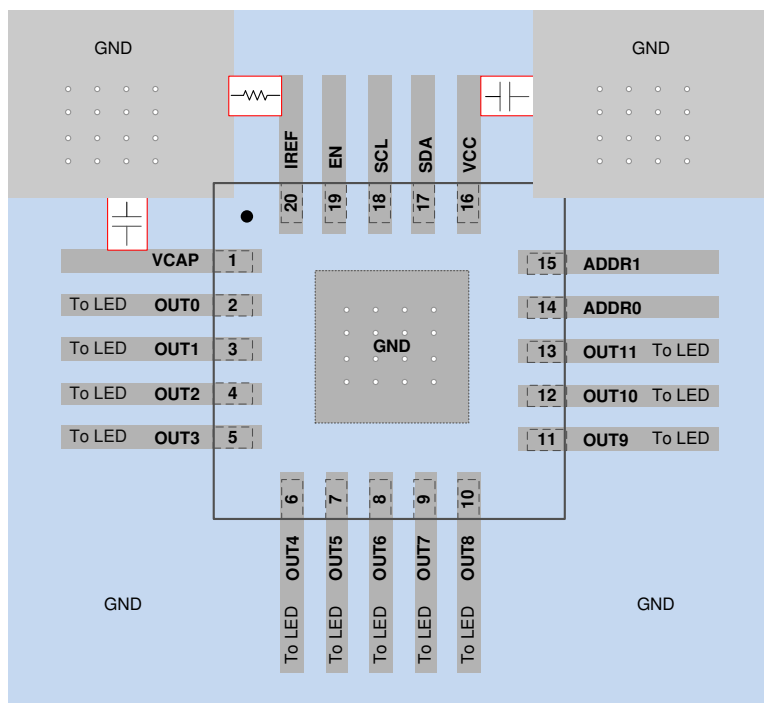
Use the following guidelines when designing the device layout:

- Place the  $C_{V_{CAP}}$ ,  $C_{V_{CC}}$  and  $R_{IREF}$  as close to the device as possible. Also, TI recommends putting the ground plane as [图 11-1](#) and [图 11-2](#).
- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through copper on the PCB. Maximum copper density is extremely important when no heat sinks are attached to the PCB on the other side from the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- Use either plated-shut or plugged and capped vias for all the thermal vias on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage must be at least 85%.

## 11.2 Layout Examples



**图 11-1. LP5009RUK Layout Example**



**图 11-2. LP5012RUK Layout Example**

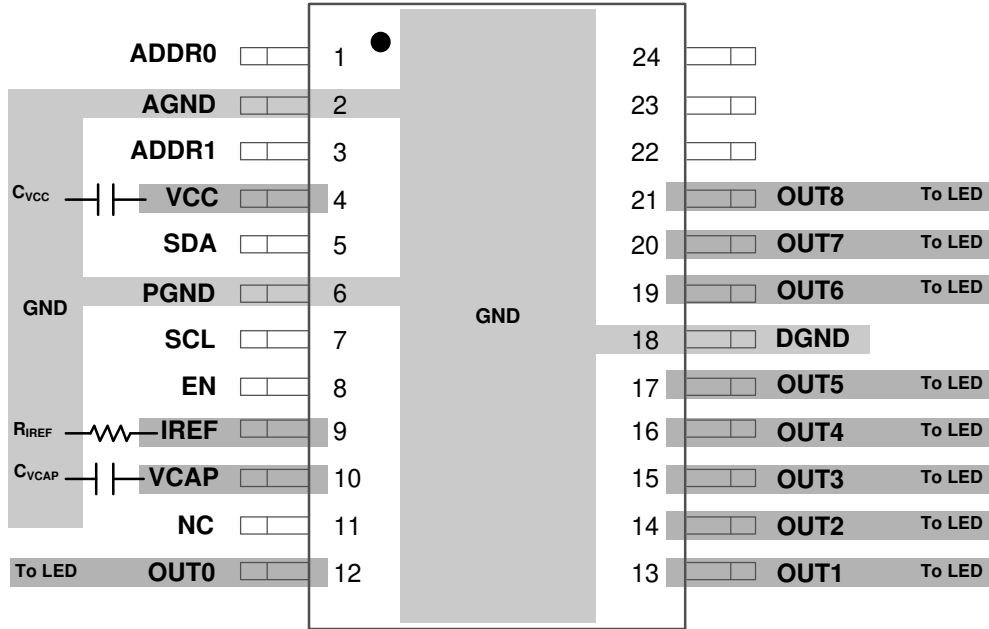


图 11-3. LP5009PW Layout Example

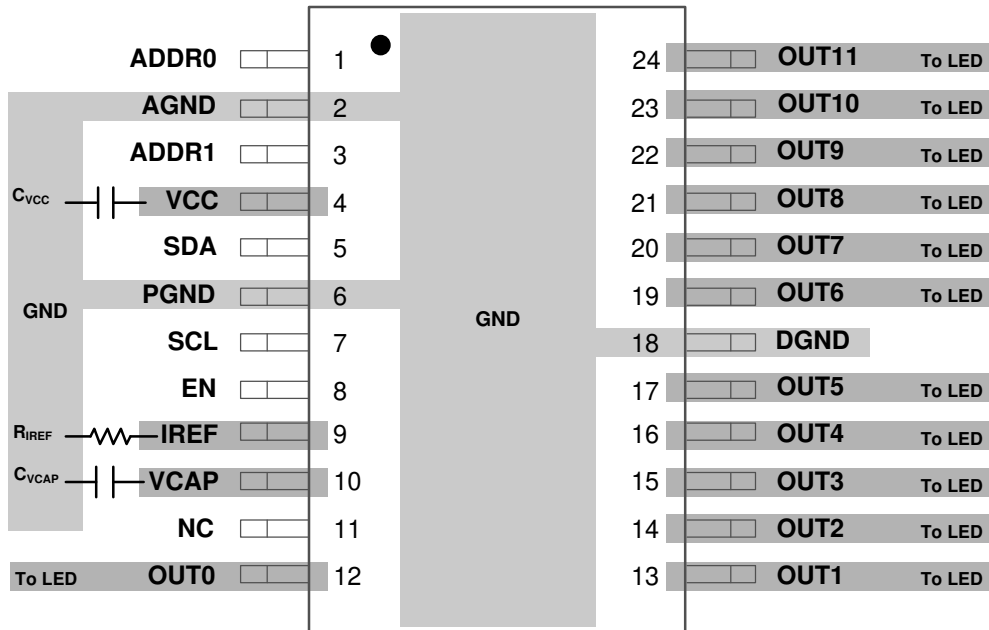


图 11-4. LP5012PW Layout Example

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP5009	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LP5012	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 12.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LP5009PWR</a>	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP5009PWR
LP5009PWR.A	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP5009PWR
<a href="#">LP5009RUKR</a>	Active	Production	WQFN (RUK)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5009
LP5009RUKR.A	Active	Production	WQFN (RUK)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5009
LP5009RUKRG4	Active	Production	WQFN (RUK)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5009
LP5009RUKRG4.A	Active	Production	WQFN (RUK)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5009
<a href="#">LP5012PWR</a>	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP5012PWR
LP5012PWR.A	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP5012PWR
<a href="#">LP5012RUKR</a>	Active	Production	WQFN (RUK)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5012
LP5012RUKR.A	Active	Production	WQFN (RUK)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5012

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

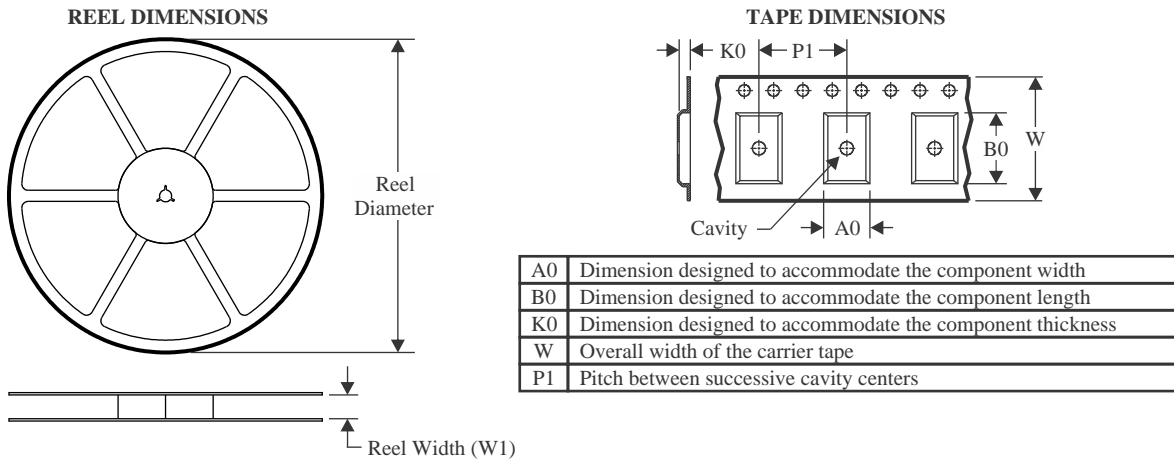
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5009PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
LP5009RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP5009RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP5009RUKRG4	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP5012PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
LP5012RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5009PWR	TSSOP	PW	24	2000	353.0	353.0	32.0
LP5009RUKR	WQFN	RUK	20	3000	356.0	356.0	36.0
LP5009RUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
LP5009RUKRG4	WQFN	RUK	20	3000	367.0	367.0	35.0
LP5012PWR	TSSOP	PW	24	2000	353.0	353.0	32.0
LP5012RUKR	WQFN	RUK	20	3000	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

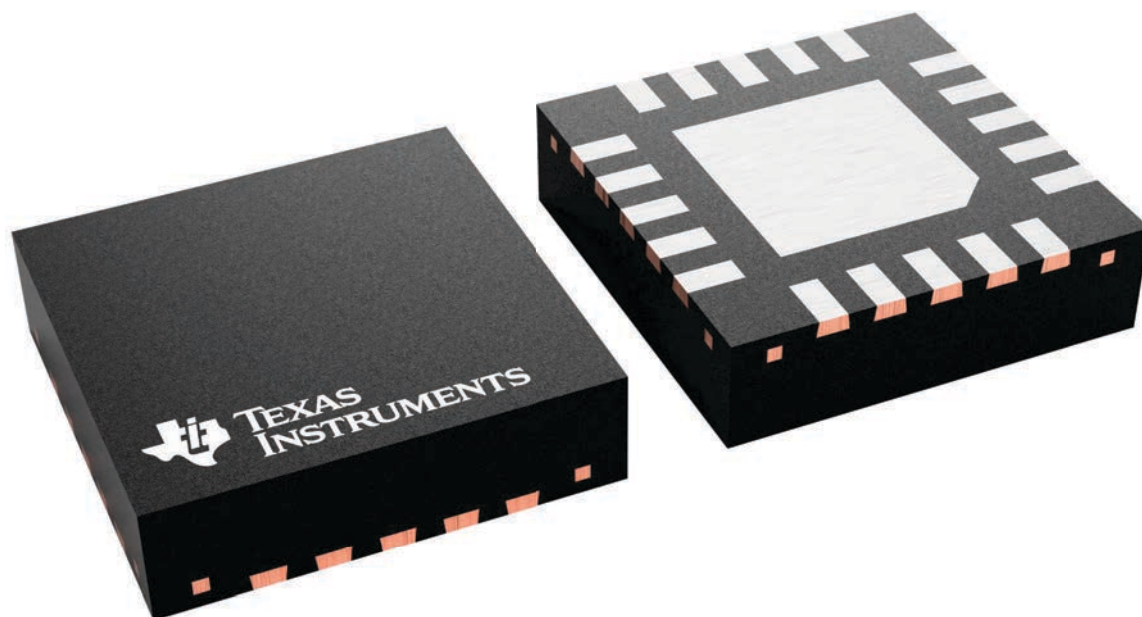
**RUK 20**

**WQFN - 0.8 mm max height**

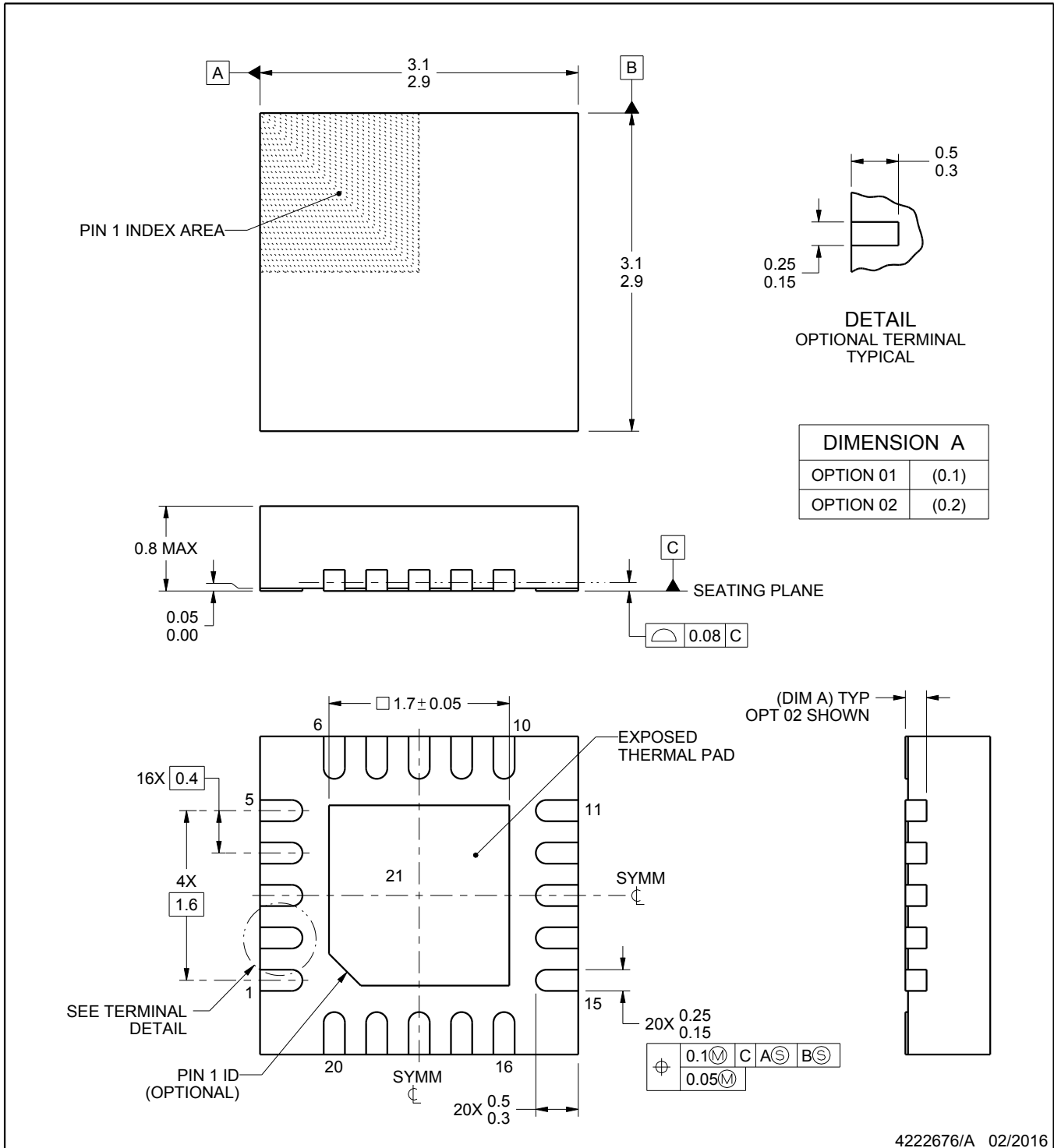
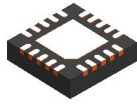
3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229651/A



4222676/A 02/2016

NOTES:

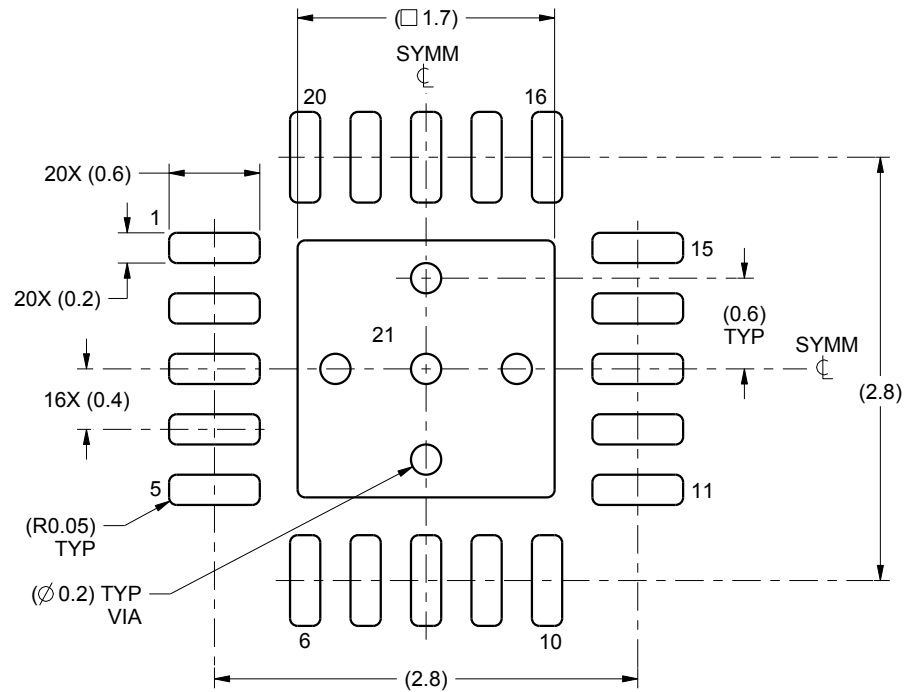
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

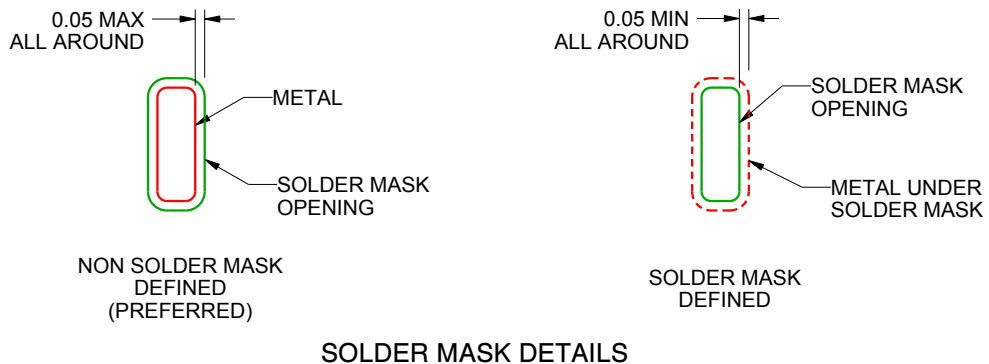
RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4222676/A 02/2016

NOTES: (continued)

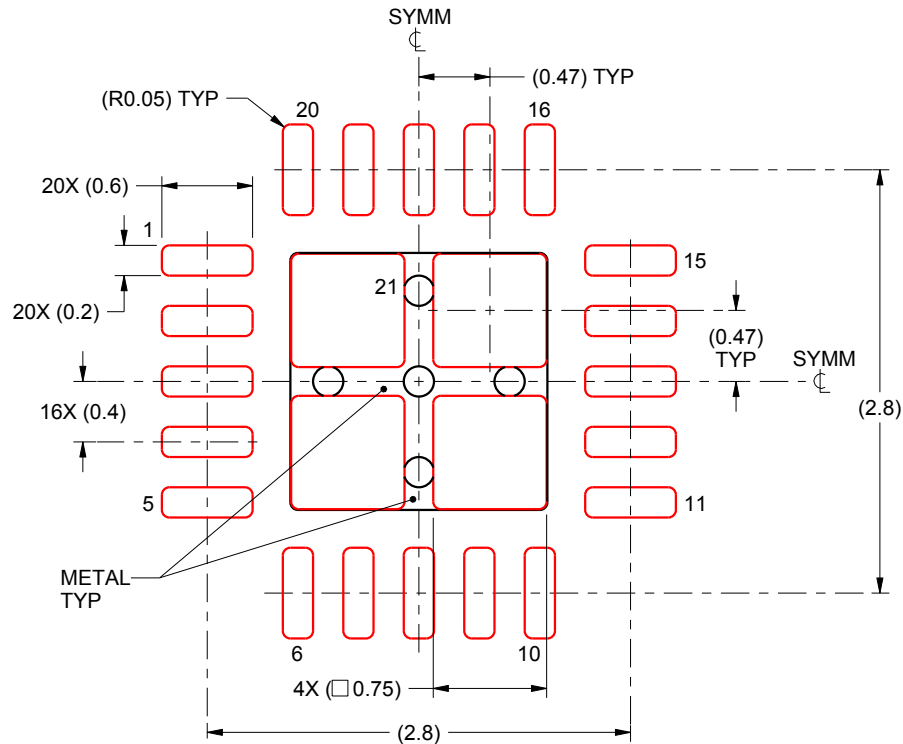
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

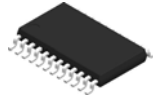
EXPOSED PAD 21:  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

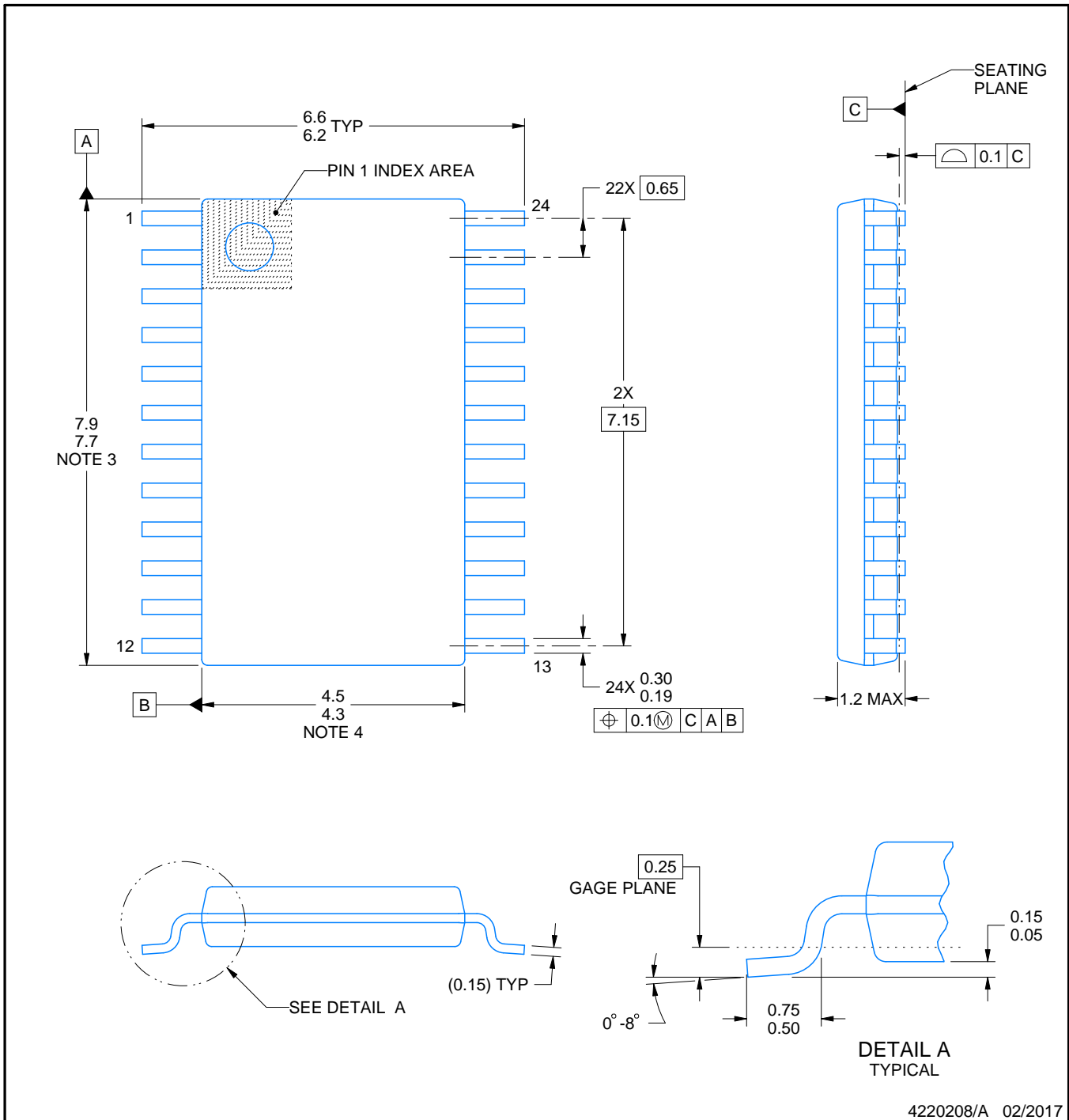
PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

### NOTES:

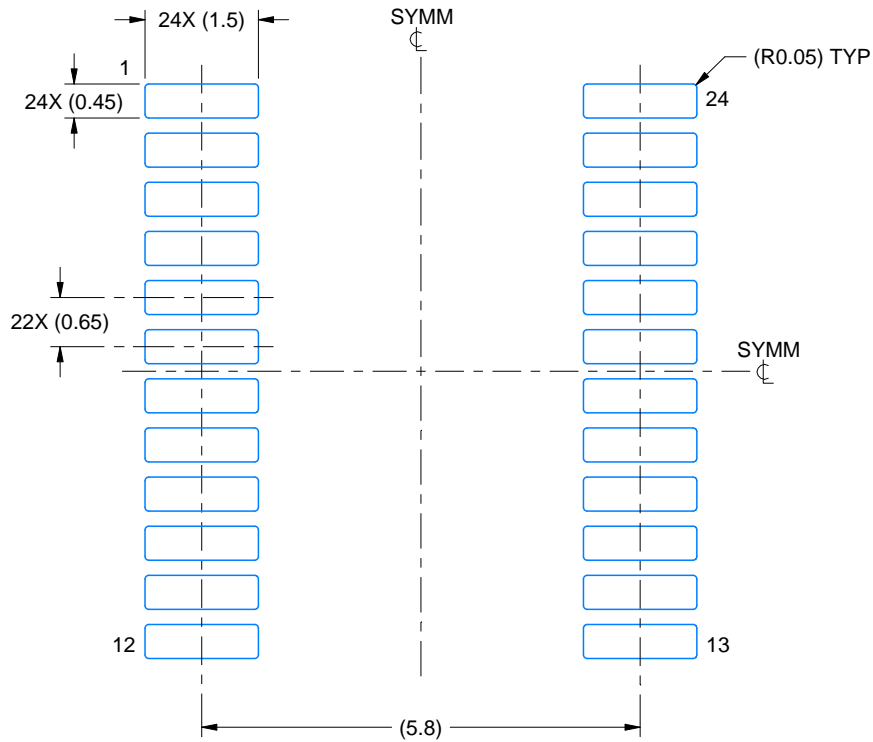
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

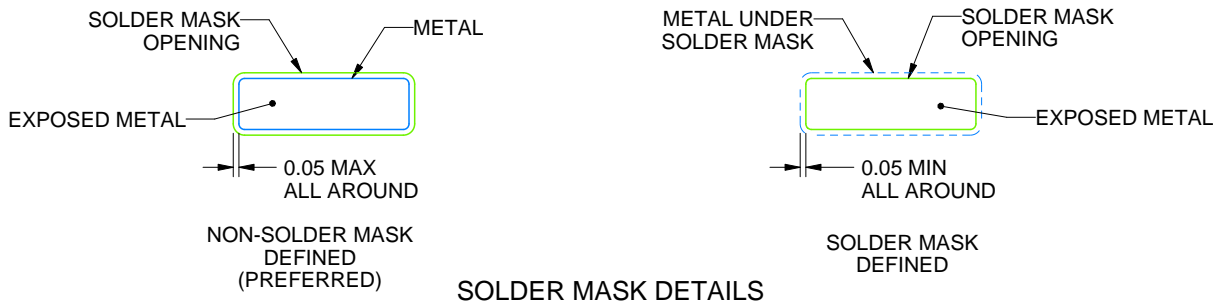
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

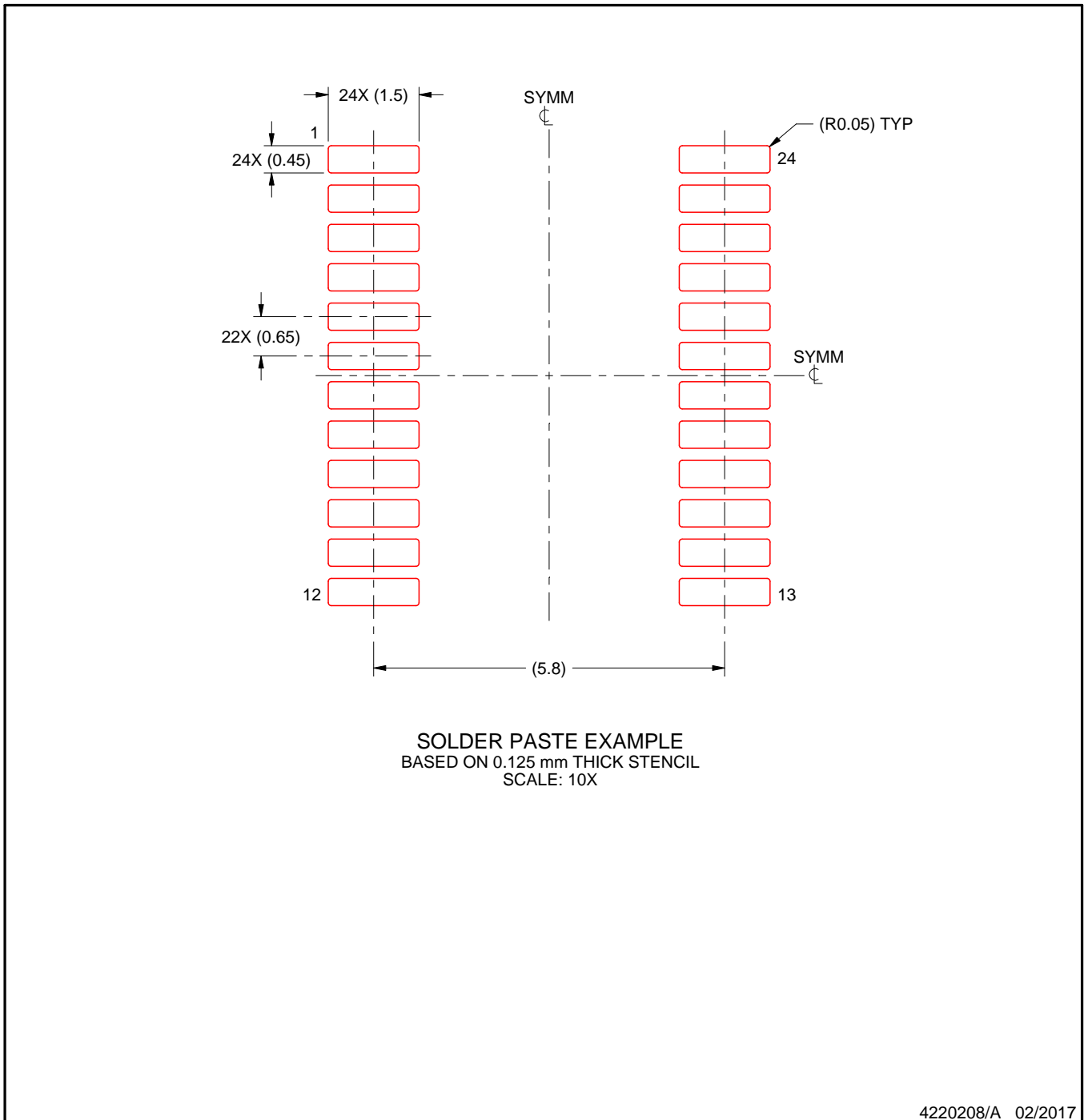
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月