具有 FSK 调制功能的 LMX2571-EP 低功耗、高性能 PLLatinum™ 射频合成器

1 特性

- VID# : V62/21613-01XE
- -55 °C 至 +125 °C 工作温度
- 10MHz 至 1344MHz 范围内的任何频率
- 低相位噪声和毛刺
  - -123dBc/Hz（在 480MHz 且偏移为 12.5kHz 时）
  - -145dBc/Hz（在 480MHz 且偏移为 1MHz 时）
  - 标准 PLL 本底噪声为 –231dBc/Hz
  - 杂散优于 –75dBc/Hz
- 新型 FastLock 技术，缩短了锁定时间
- 新型整数边界毛刺去除技术
- 集成 5V 电荷泵和输出分频器，用于外部 VCO 操作
- 2、4 和 8 电平或者任意电平数直接数字 FSK 调制
- 一个 TX/RX 输出或两个扇出输出
- 低电流消耗
  - 39mA 典型合成器模式（内部 VCO）
  - 9mA 典型 PLL 模式（外部 VCO）
- 24 位分数 N Δ-Σ 调制器
- LMX2571 与 LMX2571-EP 之间的功能差异
  - LMX2571-EP 没有 TrCtl 引脚
  - LMX2571-EP 没有 OSCin* 引脚、差分模式和晶振模式

2 应用

- 导引头前端
- 国防无线电
- 飞行器驾驶舱显示屏
- 飞行控制单元
- 无线基础设施

3 说明

LMX2571-EP 器件是一款低功耗、高性能的宽带 PLLatinum™ 射频合成器，该器件集成了 Δ-Σ 分数 N PLL、多核电压控制振荡器 (VCO)、可编程输出分频器和两个输出缓冲器。VCO 内核的工作频率高达 5.376GHz，持续输出频率范围为 10MHz 至 1344MHz。

该合成器还可搭配外部 VCO 使用。在此配置下，需使用专用的 5V 电荷泵和输出分频器。

该合成器还包含一个独特的可编程乘法器，有助于去除毛刺，即使毛刺落在整数边界，系统也仍能够使用任一通道。

输出具有集成式 SPDT 开关，可用作 FDD 无线电应用中的发送和接收开关。并且可同时导通两个开关，以便同时提供双输出。

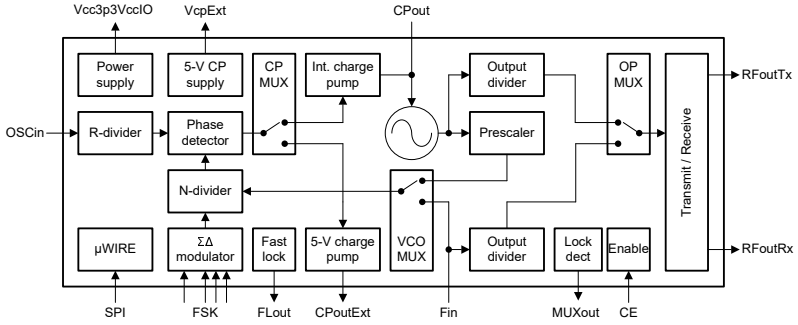
通过编程或引脚，LMX2571-EP 可支持直接数字 FSK 调制。此外，还支持离散电平 FSK、脉冲成形 FSK 以及模拟 FM 调制。

该合成器采用了全新的 FastLock 技术，即使在外部 VCO 与窄带回路滤波器搭配使用时，用户也能够在不到 1.5ms 的时间内从一个频率切换至另一频率。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMX2571-EP V62/21613-01XE	VQFN (36)	6.00mm × 6.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision A (December 2021) to Revision B (June 2022)	Page
• 删除了对 TrCtl 引脚的所有引用	1
• 删除了“差分模式”	1
• 删除了“晶振模式”	1
• Redefined the OSCin* pin to NC	3
• Added the *Differences Between the LMX2571 and LMX2571-EP* section	13

Changes from Revision * (October 2021) to Revision A (December 2021)	Page
• 将数据表状态从“预告信息”更改为：量产数据	1

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5 Pin Configuration and Functions

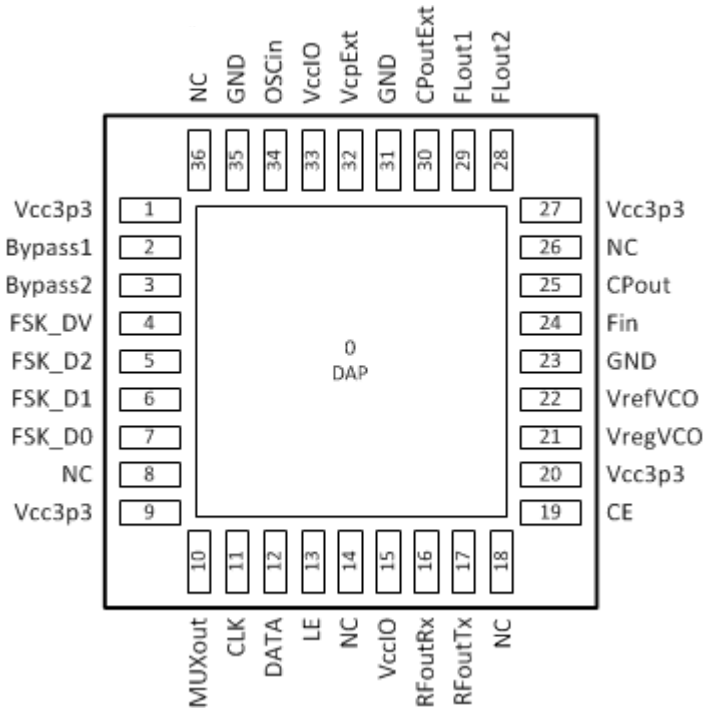


图 5-1. RHH Package 36-Pin VQFN Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Bypass1	2	Bypass	Place a 100-nF capacitor to GND.
Bypass2	3	Bypass	Place a 100-nF capacitor to GND.
CE	19	Input	Chip Enable input. Active HIGH powers on the device.
CLK	11	Input	MICROWIRE clock input.
CPout	25	Output	Internal VCO charge pump access point to connect to a 2nd order loop filter.
CPoutExt	30	Output	5-V charge pump output used in PLL mode (external VCO).
DAP	GND	GND	The DAP should be grounded.
DATA	12	Input	MICROWIRE serial data input.
Fin	24	Input	High-frequency, AC-coupled input pin for an external VCO. Leave it open or AC-coupled to GND if not being used.
FSK_D0	7	Input	FSK data bit 0 (FSK PIN mode) / I2S FS input (FSK I2S mode).
FSK_D1	6	Input	FSK data bit 1 (FSK PIN mode) / I2S DATA input (FSK I2S mode).
FSK_D2	5	Input	FSK data bit 2 (FSK PIN mode).
FSK_DV	4	Input	FSK data valid input (FSK PIN mode) / I2S CLK input (FSK I2S mode).
FLout1	29	Output	FastLock output control 1 for external switch. Output is HIGH when F1 is selected.
FLout2	28	Output	FastLock output control 2 for external switch. Output is HIGH when F2 is selected.
GND	23	GND	VCO ground.
GND	31	GND	Charge pump ground.
GND	35	GND	OSCin ground.
LE	13	Input	MICROWIRE latch enable input.
MUXout	10	Output	Multiplexed output that can be assigned to lock detect or readback serial data output.

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表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
NC	14, 26	NC	Leave floating, do not connect to GND or power supply.
OSCin	34	Input	Reference clock input.
NC	8,18, 36	NC	These pins may be left floating or connected to GND.
RFoutRx	16	Output	RF output used to drive receive mixer. Selectable open-drain or push-pull output.
RFoutTx	17	Output	RF output used to drive transmit signal. Selectable open-drain or push-pull output.
Vcc3p3	1, 9, 20, 27	Supply	Connect to 3.3-V supply.
VccIO	15, 33	Supply	Supply for digital logic interface. Connect to 3.3-V supply.
VcpExt	32	Supply	Supply for 5-V charge pump. Connect to 5-V supply in PLL mode. Connect to either 3.3-V or 5-V supply in synthesizer mode.
VrefVCO	22	Bypass	LDO output. Place a 100-nF capacitor to GND.
VregVCO	21	Bypass	Bias circuitry for the VCO. Place a 2.2-µF capacitor to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	– 0.3	3.6	V
V_{IO}	IO supply voltage	– 0.3	3.6	V
V_{CP}	Charge pump supply voltage		5.25	V
V_{IN}	IO input voltage		V_{CC} + 0.3	V
T_J	Junction temperature	– 55	150	°C
T_{stg}	Storage temperature	– 65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage		3.15	3.3	3.45	V
V_{IO}	IO supply voltage				V_{CC}	V
V_{CP}	Charge pump supply voltage	PLL mode (external VCO)			5	V
		Synthesizer mode (internal VCO)	V_{CC}		5	
T_A	Ambient temperature		– 55		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		LMX2571-EP NJK (WQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

3.15 V ≤ V_{CC} ≤ 3.45 V, V_{IO} = V_{CC}, –55 °C ≤ T_A ≤ 125 °C, except as specified. Typical values are at V_{CC} = V_{IO} = 3.3 V, V_{CP} = 3.3 V or 5 V in synthesizer mode, V_{CP} = 5 V in PLL mode, T_A = 25 °C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION							
I_{CC}	Synthesizer mode	f_{OUT} = 480 MHz, SE OSCIN	Configuration A[1]		39		mA
			Configuration B[2]		44		
			Configuration C[3]		46		
			Configuration D[4]		51		
I_{PLL}	PLL mode		Configuration E[5]		9		
			Configuration F[6]		15		
			Configuration G[7]		21		
I_{PD}	Powerdown	CE = 0 V or POWERDOWN = 1, V_{CC} = 3.3 V, Push-pull output			0.9		mA
OSCIN REFERENCE INPUT							
f_{OSCIN}	Input frequency			10		150	MHz
V_{OSCIN}	Input voltage[8]			0.8		3.3	V
REFERENCE INPUT PROGRAMMABLE MULTIPLIER							
f_{MULTin}	MULT input frequency	MULT > Pre-divider		10		30	MHz
$f_{MULTout}$	MULT output frequency			60		130	
PLL							
f_{PD}	Phase detector frequency			10		130	MHz
K_{PD}	Charge pump current[9]	Programmable minimum value	Internal charge pump		312.5		µA
			5-V charge pump		625		
		Per programmable step	Internal charge pump		312.5		
			5-V charge pump		625		
		Programmable maximum value	Internal charge pump		7187.5		
			5-V charge pump		6875		

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3.15 V ≤ V_{CC} ≤ 3.45 V, V_{IO} = V_{CC}, –55 °C ≤ T_A ≤ 125 °C, except as specified. Typical values are at V_{CC} = V_{IO} = 3.3 V, V_{CP} = 3.3 V or 5 V in synthesizer mode, V_{CP} = 5 V in PLL mode, T_A = 25 °C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$PN_{PLL_1/f}$	Normalized PLL 1/f noise(10)	At maximum charge pump current	Internal charge pump		–124		dBc/Hz
			5-V charge pump		–120		
PN_{PLL_FLAT}	Normalized PLL noise floor(10)		Internal charge pump		–231		
			5-V charge pump		–226		
f_{RFIN}	External VCO input frequency(11)	EXTVCO_CHDIV = 1		100		2000	MHz
		EXTVCO_CHDIV = 8, 10		100		1900	
		EXTVCO_CHDIV = 2, 3, 4, 5, 6, 7, 9		100		1400	
P_{RFIN}	External VCO input power	0.1 GHz ≤ f_{RFIN} < 1 GHz		–10			dBm
		1 GHz ≤ f_{RFIN} ≤ 1.4 GHz		–5			
		1.4 GHz < f_{RFIN} ≤ 2 GHz		0			
VCO							
f_{VCO}	VCO frequency			4300		5376	MHz
K_{VCO}	VCO gain(12)	f_{VCO} = 4800 MHz			56		MHz/V
$\lvert \Delta T_{CL} \rvert$	Allowable temperature drift(13)	VCO not being recalibrated, –40 °C ≤ T_A ≤ 125 °C				165	°C
t_{VCOCAL}	VCO calibration time	f_{OSCIN} = f_{PD} = 100 MHz			140		µs
PNVCO	Open loop VCO phase noise	f_{OUT} = 480 MHz	100 Hz offset		–32.4		dBc/Hz
			1 kHz offset		–62.3		
			10 kHz offset		–92.1		
			100 kHz offset		–121.1		
			1 MHz offset		–144.5		
			10 MHz offset		–156.8		
Outputs							
f_{OUT}	RF output frequency	Synthesizer mode		10		1344	MHz
		PLL mode, RF output from buffer		10		1400	
P_{TX}, P_{RX}	RF output power	f_{OUT} = 480 MHz	Power control bit = 6		0		dBm
$H2_{RFout}$	Second harmonic				–25		dBc
DIGITAL FSK MODULATION							
FSK_{Level}	FSK level(14)	FSK PIN mode		2		8	
FSK_{Baud}	FSK baud rate(15)	Loop bandwidth = 200 kHz			100		kSPs
FSK_{Dev}	FSK deviation	Configuration H(16)			±39		kHz
DIGITAL INTERFACE							
V_{IH}	High-level input voltage			1.4		V_{CC}	V
V_{IL}	Low-Level input voltage					0.4	V
I_{IH}	High-level input current	V_{IH} = 1.75 V		–25		25	µA
I_{IL}	Low-Level input current	V_{IL} = 0 V		–25		25	µA
V_{OH}	High-level output voltage	I_{OH} = 500 µA		2			V
V_{OL}	Low-level input voltage	I_{OL} = –500 µA			0	0.4	V

(1) f_{OSCIN} = 19.44 MHz, MULT = 1, Prescaler = 4, f_{PD} = 19.44 MHz, one RF output, output type = push pull, output power = –3 dBm
(2) f_{OSCIN} = 19.44 MHz, MULT = 1, Prescaler = 2, f_{PD} = 19.44 MHz, one RF output, output type = push pull, output power = –3 dBm
(3) f_{OSCIN} = 19.44 MHz, MULT = 5, Prescaler = 2, f_{PD} = 19.44 MHz, one RF output, output type = push pull, output power = –3 dBm
(4) f_{OSCIN} = 19.44 MHz, MULT = 5, Prescaler = 2, f_{PD} = 97.2 MHz, one RF output, output type = push pull, output power = –3 dBm
(5) f_{OSCIN} = 19.44 MHz, MULT = 1, f_{PD} = 19.44 MHz, output from VCO

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(6) f_{OSCIN} = 19.44 MHz, MULT = 1, f_{PD} = 19.44 MHz, one RF output, output type = push pull, output power = – 3 dBm
(7) f_{OSCIN} = 19.44 MHz, MULT = 1, f_{PD} = 19.44 MHz, two RF outputs, output type = push pull, output power = – 3 dBm
(8) See OSCIN Configuration for definition of OSCIN input voltage.
(9) This is referring to the total base charge pump current. In PLL mode, this is equal to EXTVCO_CP_IDN + EXTVCO_CP_IUP. In synthesizer mode, this is equal to CP_IDN + CP_IUP.
(10) Measured with a clean OSCIN signal with a high slew rate using a wide loop bandwidth. The noise metrics model the PLL noise for an infinite loop bandwidth as:
PLL_Total = 10 * log[$10^{(PLL_Flat / 10)}$ + $10^{(PLL_Flicker / 10)}$]
PLL_Flat = PN1Hz + 20 * log(N) + 10 * log(f_{PD})
PLL_Flicker = PN10kHz – 10 * log(Offset / 10 kHz) + 20 * log(f_{OUT} / 1 GHz)
(11) For external VCO frequencies above 1.4 GHz, there are restrictions on the output divider and register R70 needs to be programmed to 0x046110.
(12) The VCO gain changes as a function of the VCO core and frequency. See Integrated VCO for details.
(13) Not tested in production. Ensured by characterization. Allowable temperature drift refers to programming the device at an initial temperature and allowing this temperature to drift WITHOUT reprogramming the device, and still have the device stay in lock. This change could be up or down in temperature and the specification does not apply to temperatures that go outside the recommended operating temperatures of the device.
(14) The data showed here simply specifies the range of discrete FSK level that is supported in PIN mode. PIN mode supports 2-, 4- and 8-level of FSK modulation. If arbitrary level of FSK modulation is desired, use FSK SPI™ FAST mode or FSK I2S mode. See Direct Digital FSK Modulation for details.
(15) The baud rate is limited by the loop bandwidth of the PLL loop. As a general rule of thumb, it is desirable to have the loop bandwidth at least twice the baud rate.
(16) f_{PD} = 100 MHz, DEN = 224, CHDIV1 = 5, CHDIV2 = 2, Prescaler = 2, FSK step value = 32716, 32819. The maximum achievable frequency deviation depends on the configuration, see Direct Digital FSK Modulation for details.

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6.6 Timing Requirements

3.15 V ⩽ V_{CC} ⩽ 3.45 V, V_{IO} = V_{CC}, – 55 °C ⩽ T_A ⩽ 125 °C, except as specified. Typical values are at V_{CC} = V_{IO} = 3.3 V, T_A = 25 °C.

			MIN	NOM	MAX	UNIT
Timing Requirements						
t_{ES}	CLK to LE low time	See Figure 6-1	5			ns
t_{CS}	DATA to CLK setup time		2			ns
t_{CH}	DATA to CLK hold time		2			ns
t_{CWH}	CLK pulse width high		10			ns
t_{CWL}	CLK pulse width low		10			ns
t_{CES}	LE to CLK setup time		5			ns
t_{EWH}	LE pulse width high		2			ns
t_{OD}	CLK to MUXOUT delay time				8	ns

6.7 Timing Diagrams

There are several other considerations for programming:

- A slew rate of at least 30 V/µs is recommended for the CLK, DATA and LE. The same apply for other digital control signals such as FSK_D[0:2] and FSK_DV signals.
- The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the 24th CLK, the data is transferred from the data field to the selected register bank.
- The LE pin may be held high after programming, causing the LMX2571-EP to ignore clock pulses.
- When CLK or DATA lines are shared between devices, it is recommended to divide down the voltage to the CLK, DATA, and LE pins closer to the minimum voltage. This provides better noise immunity.
- If the CLK and DATA lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during the time of this programming.

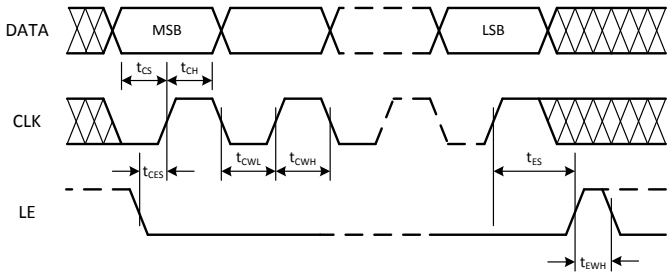
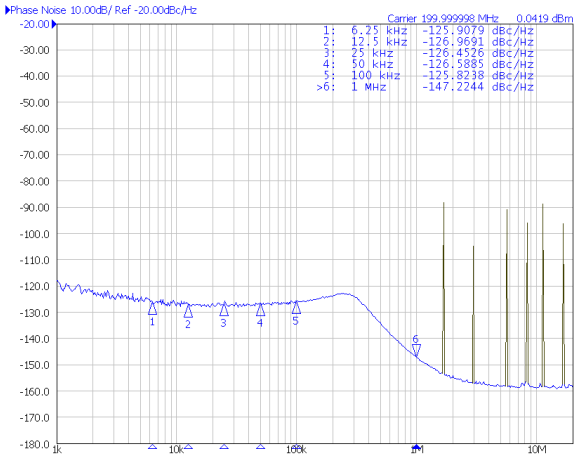


图 6-1. MICROWIRE Timing Diagram

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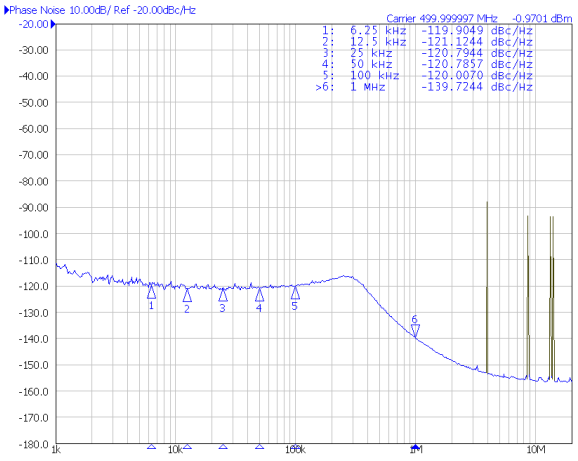
6.8 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



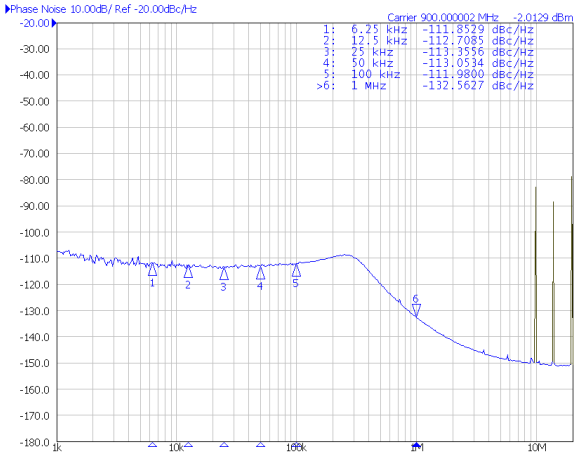
OSCin = 19.44 MHz f_{OUT} = 200 MHz Synthesizer mode

图 6-2. Typical Closed-Loop Phase Noise



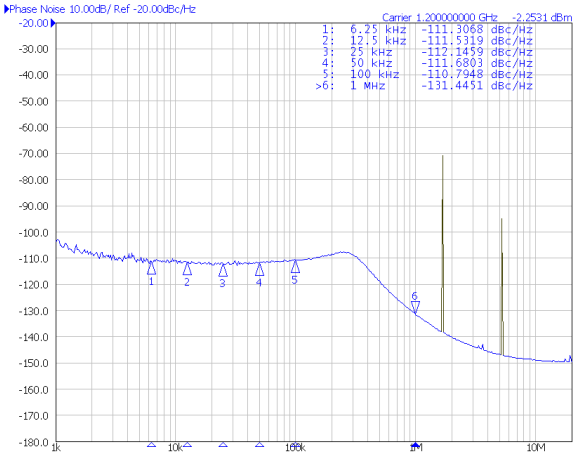
OSCin = 19.44 MHz f_{OUT} = 500 MHz Synthesizer mode

图 6-3. Typical Closed-Loop Phase Noise



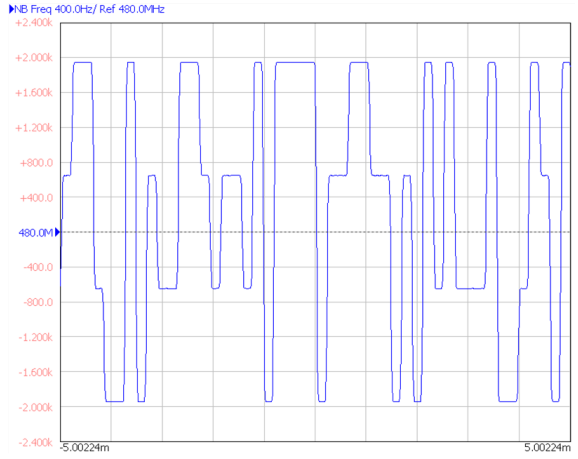
OSCin = 19.44 MHz f_{OUT} = 900 MHz Synthesizer mode

图 6-4. Typical Closed-Loop Phase Noise



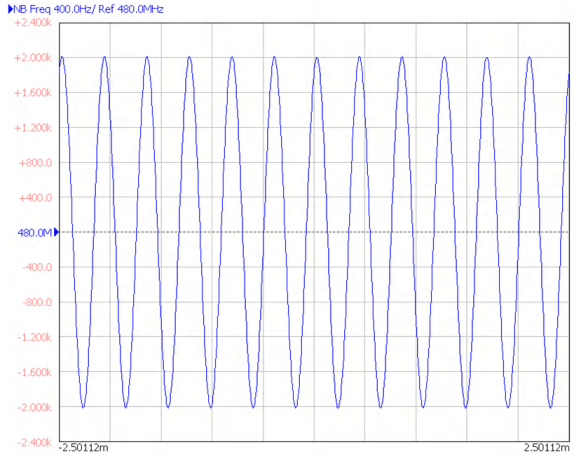
OSCin = 19.44 MHz f_{OUT} = 1200 MHz Synthesizer mode

图 6-5. Typical Closed-Loop Phase Noise



FSK_{Baud} = 4.8 kSPS FSK PIN mode

图 6-6. 4FSK Direct Digital Modulation



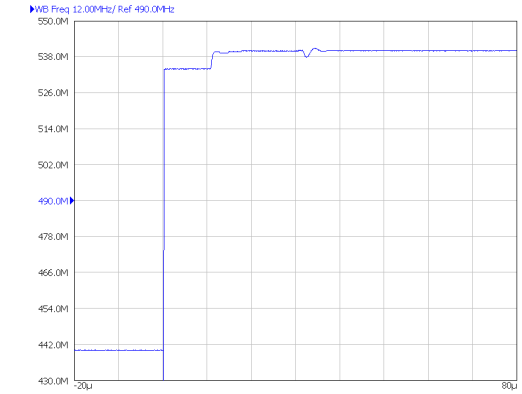
Reference clock is a FM modulated signal with f_{MOD} = 2.4 kHz

图 6-7. FM Modulation Through Reference Clock

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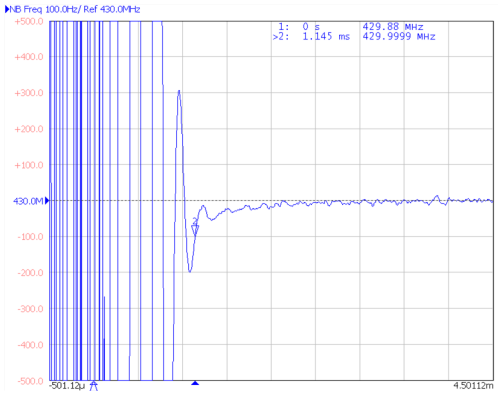
6.8 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



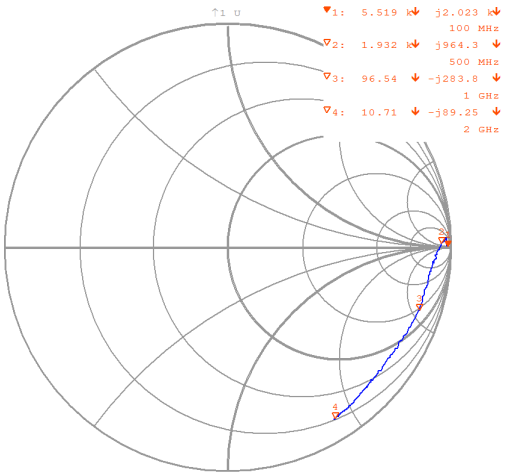
Switching between int. and ext. VCO as well as Tx and Rx port

图 6-8. Output Port and VCO Switching



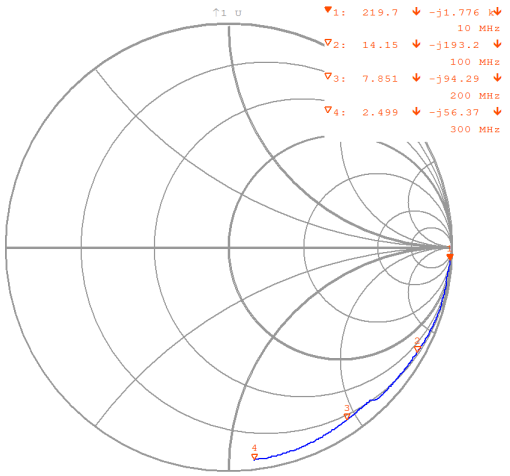
Freq. jump = 50 MHz LBW = 4 kHz PLL mode

图 6-9. FastLock With SPST Switch



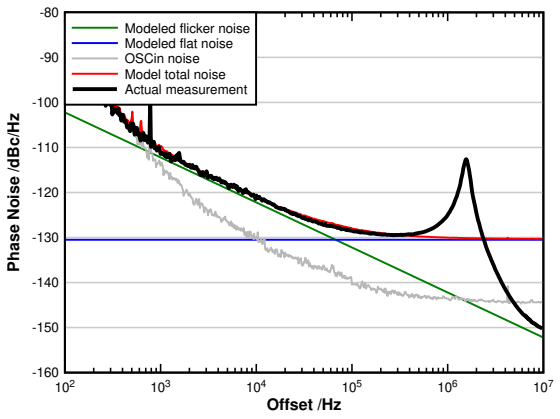
Start: 100 MHz Stop: 2000 MHz

图 6-10. Fin Input Impedance



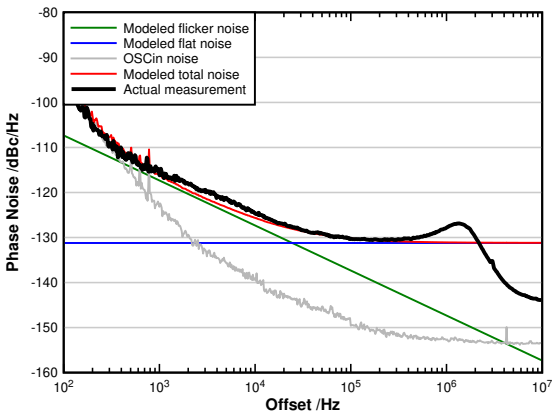
Start: 10 MHz Stop: 300 MHz

图 6-11. OSCin Input Impedance



f_{OUT} = 1228.8 MHz f_{PD} = 122.88 MHz Synthesizer mode

图 6-12. Normalized PLL 1/f Noise and Noise Floor



f_{OUT} = 430.08 MHz f_{PD} = 61.44 MHz PLL mode

图 6-13. Normalized PLL 1/f Noise and Noise Floor

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6.8 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

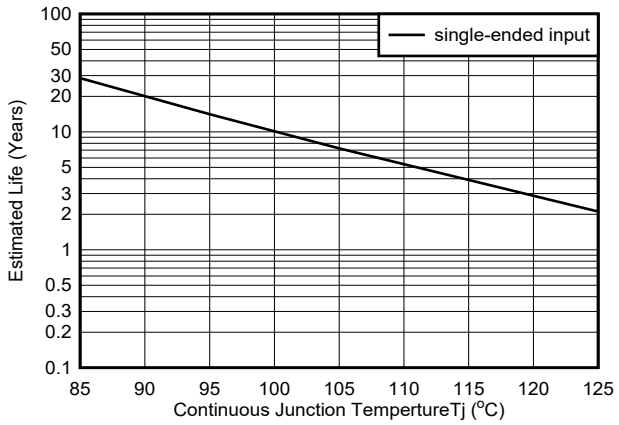


图 6-14. Lifetime vs. Temperature

7 Detailed Description

7.1 Overview

The LMX2571-EP is a frequency synthesizer with low-noise, high-performance integrated VCOs. The 5-GHz VCO cores, together with the output channel dividers, can produce frequencies from 10 MHz to 1344 MHz. The LMX2571-EP supports two operation modes, synthesizer mode and PLL mode. In synthesizer mode, the entire device is used; in PLL mode the internal VCO is bypassed, and an external VCO is required to implement a complete synthesizer.

The PLL is a fractional-N PLL with programmable Delta Sigma modulator (first order to fourth order). The fractional denominator is of variable length and up to 24-bits long, providing a frequency step with very fine resolution.

The internal VCO can be bypassed, allowing the use of an external VCO. A separate 5-V charge pump is dedicated for the external VCO, eliminating the need for an op-amp to support 5-V VCOs. A new advanced FastLock technique is developed to shorten the lock time to less than 1.5 ms, even there is a very narrow loop bandwidth.

A unique programmable multiplier is incorporated in the R-divider. The multiplier is used to avoid and reduce integer boundary spurs or to increase the phase detector frequency for higher performance.

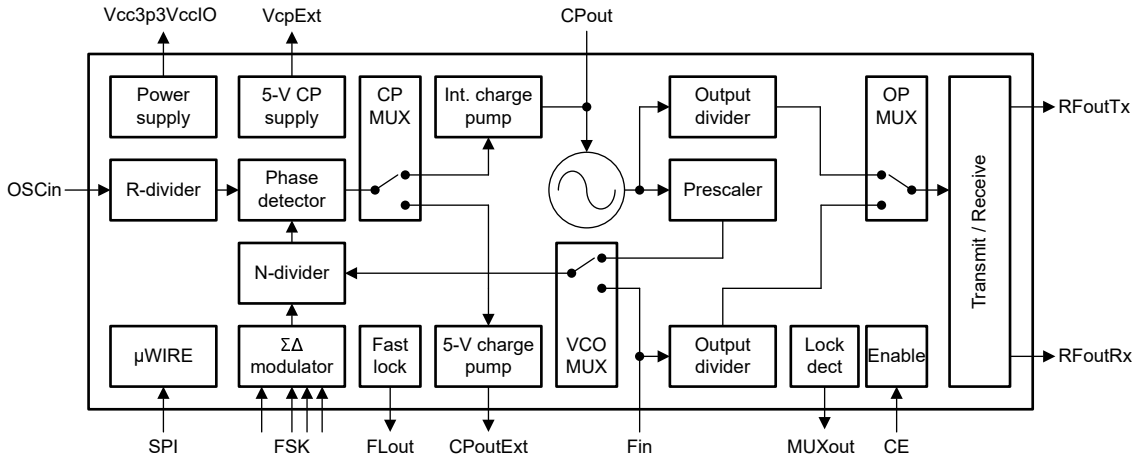
The LMX2571-EP supports direct digital FSK modulation, thus allowing a change in the output frequency by changing the N-divider value. The N-divider value can be programmed through MICROWIRE interface or through pins. Discrete 2-, 4- and 8-level FSK, as well as arbitrary-level FSK, are supported. Arbitrary-level FSK can be used to construct pulse-shaping FSK or analog-FM modulation.

The output has an integrated T/R switch, and the divided-down internal or external VCO signal can be output to either the TX port or the RX port. The switch can also be configured as a 1:2 fanout buffer, providing the signal on both outputs at the same time. In addition to port switching, the output frequency can be switched between two pre-defined frequencies, F1 and F2, simultaneously. This feature is ideal for use in FDD duplex system where the TX frequency is different from RX (LO) frequency.

The LMX2571-EP requires only a single 3.3-V power supply. Digital logic interface is 1.8-V input compatible. The analog blocks power supplies use integrated LDOs, eliminating the need for high performance external LDOs.

Programming of the device is achieved through the MICROWIRE interface. The device can be powered down through a register programming or toggling the Chip Enable (CE) pin.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Differences Between the LMX2571 and LMX2571-EP

For both devices, pin 8 is not connected to the die and pins 14 and 26 are. However, tor the LMX2571-EP, both Pin 36 and Pin 18 are different and are true no connect pins, meaning that this pin is not connected to the die. This impacts some of the functionality of the device.

表 7-1. Differences Between LMX2571 and LMX2571-EP

Aspect	Details	LMX2571	LMX2571-EP
Reference Input	Pin 36	OSCin*	NC. There is no connection to the die.
	Differential Input	Supported R34[14]=IPBUF_SE_DIFF_SEL	Not Supported R34[14]=0 One may drive OSCin and pin 36 with a differential signal, but pin 36 is high impedance (open) and the signal is ignored at this pin.
	Crystal Mode	Supported R34[10]=XTAL_EN R34[11]=XTAL_PWRCTRL	Not Supported R34[10]=0 R34[11]=2
Rx/Tx Switching	Pin 18	TrCtl	NC. There is no connection to the die.
	Pin Switching	Supported R0[8]=F1F2_CTRL R0[10]=RXTX_POL R0[11]=RXTX_CTL	Software Only R0[8]=0 R0[10]=0 R0[11]=0

7.3.2 Reference Oscillator Input

The OSCin pin is used as frequency reference input to the device. The OSCin pin can be driven single-ended with a CMOS clock.

The OSCin signal is used as a clock for VCO calibration, therefore a proper signal must be applied at the OSCin pin at the time of programming the R0 register. A higher slew rate tends to yield the best fractional spurs and phase noise, so a square wave signal is best for the OSCin pin. If using a sine wave, higher frequencies tend to yield better phase noise and fractional spurs due to their higher slew rates.

7.3.3 R-Dividers and Multiplier

The R-divider consists of a Pre-divider, a Multiplier (MULT), and a Post-divider.

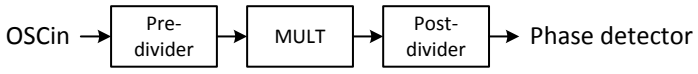


图 7-1. R-Divider

Both the Pre- and Post-dividers divide frequency down while the MULT multiplies frequency up. The purpose of adding a multiplier is to avoid and reduce integer boundary spurs or to increase the phase-detector frequency for higher performance. See *MULT Multiplier* for details. The phase detector frequency, f_{PD}, is therefore equal to

$$f_{PD} = (f_{OSCin} / \text{Pre-divider}) \times (\text{MULT} / \text{Post-divider}) \quad (1)$$

When using the Multiplier (MULT > 1), there are some points to remember:

- The Multiplier must be greater than the Pre-divider.
- Using the multiplier may add noise, especially for multiplier values greater than 6.

7.3.4 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the Post-divider and N-divider and generates a correction current corresponding to the phase error. This charge pump current is programmable to different strengths. The pump

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up and pump down currents are individually programmable, but should always programmed to the same value. The effective charge pump current is the sum of the up and down currents and multiplied by a gain multiplier. In other words, Effective Charge Pump Current = (Base Charge Pump Current) × (Gain Multiplier)

7.3.4.1 CPout Pin Charge Pump Current

When using internal VCO mode, the charge pump output is the CPout pin and the base charge pump current is programmable in 156.25 µA increments set by the CP_IUP and CP_IDN fields (see 表 7-2). This value is doubled and then multiplied by the charge pump gain value specified in 表 7-3.

表 7-2. Base Charge Pump Current When Using Internal VCO

CP_IUP, CP_IDN	BASE CHARGE PUMP CURRENT (µA)
0	Tri-State
1	156.25
2	312.5
3	468.75.
...	...
7	1093.75
8 or 16	1250
9 or 17	1406.25
...	
15 or 23	2343.75
24	2500
25	2656.25
...	
31	3593.75

表 7-3. Charge Pump Gain Multiplier When Using Internal VCO

CP_GAIN	GAIN MULTIPLIER
0	1X
1	2X
2	1.5X
3	2.5X

7.3.4.2 Charge Pump Current When Using External VCO

When using external VCO mode, the charge pump output is the CPoutExt pin and the base charge pump current is programmable in 312.5 µA increments set by the EXTVCO_CP_IUP and EXTVCO_CP_IDN fields as shown in 表 7-4. Odd values for EXTVCO_CP_IUP and EXTVCO_CP_IDN are not valued. This value is doubled and then multiplied by the charge pump gain value specified in 表 7-5.

表 7-4. Base Charge Pump Current in External VCO Mode

EXTVCO_CP_IUP, EXTVCO_CP_IDN	BASE CHARGE PUMP CURRENT (µA)
0	Tri-state
2	312.5
4	625
6	937.5
8 or 16	1250
10 or 18	1562.5
12 or 20	1875
14 or 22	2187.5
24	2500

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表 7-4. Base Charge Pump Current in External VCO Mode (continued)

EXTVCO_CP_IUP, EXTVCO_CP_IDN	BASE CHARGE PUMP CURRENT (µA)
26	2812.5
28	3125
30	3437.5

表 7-5. Charge Pump Gain Multiplier in External VCO Mode

EXTVCO_CP_GAIN	CHARGE PUMP GAIN MULTIPLIER
0	1X
1	2X
2	1.5X
3	2.5X

7.3.5 PLL N-Divider and Fractional Circuitry

The total N-divider value is determined by $N_{integer}$ + NUM / DEN. The N-divider includes fractional compensation and can achieve any fractional denominator (DEN) from 1 to 16,777,215 (2^{24} – 1). The integer portion, $N_{integer}$, is the whole part of the N-divider value and the fractional portion, N_{frac} = NUM / DEN, is the remaining fraction. $N_{integer}$, NUM and DEN are programmable.

The order of the delta sigma modulator is also programmable from integer mode to fourth order. There are several dithering modes that are also programmable. Dithering is used to reduce fractional spurs. In order to make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

7.3.6 Partially Integrated Loop Filter

The LMX2571-EP integrates the third and fourth pole of the loop filter. The values for the resistors can be programmed independently through the MICROWIRE interface. The larger the values of the resistors, the stronger the attenuation of the internal loop filter. This partially integrated loop filter can only be used in synthesizer mode.

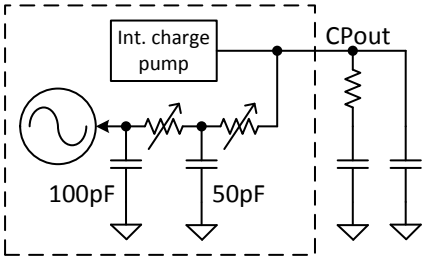


图 7-2. Integrated Loop Filter

7.3.7 Low-Noise, Fully Integrated VCO

The LMX2571-EP includes a fully integrated VCO. The VCO generates a frequency which varies with the tuning voltage from the loop filter. Output of the VCO is fed to a prescaler before going to the N-divider. The prescaler value is selectable between 2 and 4. In general, prescaler equals 2 will result in better phase noise especially when the PLL is operated in fractional-N mode. If the prescaler equals 4, however, the device will consume less current. The VCO frequency is related to the other frequencies and Prescaler as follows:

$$f_{VCO} = f_{PD} \times \text{N-divider} \times \text{Prescaler} \quad (2)$$

To reduce the VCO tuning gain, thus improving the VCO phase noise performance, the VCO frequency range is divided into several different frequency bands. This creates the need for frequency calibration to determine the correct frequency band given a desired output frequency. The VCO is also calibrated for amplitude to optimize phase noise. These calibration routines are activated any time that the R0 register is programmed with the FCAL_EN bit equals one. It is important that a valid OSCin signal must present before VCO calibration begins.

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This device will support a full sweep of the valid temperature range of 125°C (– 40°C to 85°C) without having to recalibrate the VCO. This is important for continuous operation of the synthesizer under the most extreme temperature variation.

7.3.8 External VCO Support

The LMX2571-EP supports an external VCO in PLL mode. In PLL mode, the internal VCO and its associated charge pump are powered down, and a 5-V charge pump is switched in to support external VCO. No extra external low noise op-amp is required to support 5-V tuning range VCO. The external VCO output can be obtained directly from the VCO or from the RF output buffer of the device.

7.3.9 Programmable RF Output Divider

The internal VCO RF output divider consists of two sub-dividers; the total division value is equal to the multiplication of them. As a result, the minimum division is 4 while the maximum division is 448.



图 7-3. VCO Output Divider

There is only one output divider when external VCO is being used. This divider supports even and odd division, and its values are programmable between 1 and 10.

7.3.10 Programmable RF Output Buffer

The RF output buffer type is selectable between push-pull and open-drain. If the open-drain buffer is selected, external pullup to VccIO is required. Regardless of output type, output power can be programmed to various levels. The RF output buffer can be disabled while still keeping the PLL in lock. See *RF Output Buffer Type* for details.

7.3.11 Integrated TX, RX Switch

The LMX2571-EP integrates a T/R switch. The output from the internal VCO or external VCO divider will be routed to either the RFoutTx or RFoutRx ports, depending on the state of the F1F2_SEL bit.

The T/R switch could also be configured as a fanout buffer to output the same signal at both RFoutTx and RFoutRx ports at the same time. All of these features are also programmable, see *Programming* for details.

7.3.12 Power Down

The LMX2571-EP can be powered up and down using the CE pin or the POWERDOWN bit. All registers are preserved in memory and the device may still be programmed when the device is in a powered down state. When the device comes out of the powered down state, do the following:

1. If it was powered-down by CE pin, pull CE pin HIGH
2. If it was powered-down by POWERDOWN bit, set POWERDOWN = 0 and FCAL_EN = 0
3. Wait for 100-µs to have the internal LDOs settled down
4. Program register R0 with FCAL_EN=1

7.3.13 Lock Detect

The MUXout pin of the LMX2571-EP can be configured to output a signal that indicates when the PLL is being locked. If lock detect is enabled while the MUXout pin is configured as a lock-detect output, when the device is locked the MUXout pin output is a logic HIGH voltage. When the device is unlocked, MUXout output is a logic LOW voltage.

7.3.14 FSK Modulation

Direct digital FSK modulation is supported in LMX2571-EP. FSK modulation is achieved by changing the output frequency by changing the N-divider value. The LMX2571-EP supports four different types of FSK operation.

1. FSK PIN mode. LMX2571-EP supports 2-, 4-, and 8-level FSK modulation in PIN mode. In this mode, symbols are directly fed to the FSK_D0, FSK_D1, and FSK_D2 pins. Symbol clock is fed to the FSK_DV pin.

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Symbols are latched into the device on the rising edge of the symbol clock. The maximum supported symbol clock rate is 1 MHz. The device has eight dedicated registers to prestore the desired FSK frequency deviations, with each register corresponding to one of the FSK symbols. The LMX2571-EP will change its output frequency according to the states on the FSK pins; no extra register programming is required.

2. FSK SPI mode. This mode is identical to the FSK PIN mode with the exception that the control for the selected FSK level is not performed with external pins but with register R34. Each time when register R34 is programmed, change only the FSK_DEV_SEL field to select the desired FSK frequency deviation as stored in the dedicated registers.
3. FSK SPI FAST mode. In this mode, instead of selecting one of the prestored FSK level, change the FSK deviation directly by writing to the register R33, FSK_DEV_SPI_FAST field. As a result, this mode supports arbitrary-FSK level, which is useful to construct pulse-shaping or analog-FM modulation.
4. FSK I2S mode. This mode is similar to the FSK SPI FAST mode, but the programming format is an I2S format on dedicated pins instead of SPI. The benefit of using I2S is that this interface could be shared and synchronous to other digital audio interfaces. The same FSK data input pins that are used in FSK PIN mode are reused to support I2S programming. In this mode only the 16 bits of DATA field is required to program. The data is transmitted on the high or low side of the frame sync (programmable in register R34, FSK_I2S_FS_POL). The unused side of the frame sync needs to be at least one clock cycle. In other words, 17 (16 + 1) CLK cycles are required at a minimum for one I2S frame. Maximum I2S clock rate is 100 MHz.

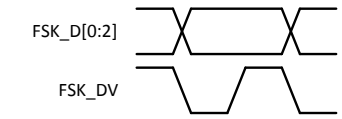


图 7-4. FSK PIN Mode Timing

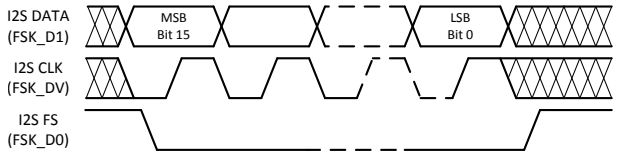


图 7-5. FSK I2S Mode Timing

See *Direct Digital FSK Modulation* for FSK operation details.

7.3.15 FastLock

The LMX2571-EP includes a FastLock feature that can be used to improve the lock times in PLL mode when the loop bandwidth is small. In general, the lock time is approximately equal to 4 divided by the loop bandwidth. If the loop bandwidth is 1 kHz, then the lock time would be 4 ms. However, if the f_{PD} is much higher than the loop bandwidth, cycle slipping may occur, and the actual lock time will be much longer. Traditional fastlock usually reduces lock time by increasing loop bandwidth during frequency switching. However, there is a limitation on the achievable maximum loop bandwidth due to limitation on charge-pump current and loop filter component values. In some cases, this kind of fastlock technique will make cycle slip even worse.

The LMX2571-EP adopts a new FastLock approach that eliminates the cycle slip problem. With an external analog SPST switch in conjunction with FastLock control of the LMX2571-EP, the lock time for a 100-MHz frequency switch could be settled in less than 1.5 ms. See *FastLock With External VCO* for details.

7.3.16 Register Readback

The LMX2571-EP allows any of its registers to be read back. The MUXout pin can be programmed to support either lock-detect output or register-readback serial-data output. To read back a certain register value, follow the following steps:

1. Set the R/W bit to 1; the data field contents are ignored.
2. Send the register to the device; readback serial data outputs starting at the falling edge of the 8th clock cycle.

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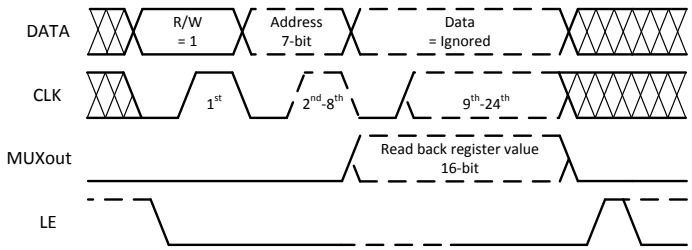


图 7-6. Register Readback Timing Diagram

7.4 Device Functional Modes

7.4.1 Operation Mode

The device can be operated in synthesizer mode or PLL mode.

1. Synthesizer mode. The internal VCO is adopted.
2. PLL mode. The device is operated as a standalone PLL; an external VCO is required to complete the loop.

7.4.2 Duplex Mode

LMX2571-EP supports fast frequency switching between two predefined register sets, F1 and F2. This feature is good for duplex operation. The device supports three duplex modes:

1. Synthesizer duplex mode. Both F1 and F2 are operated in synthesizer mode.
2. PLL duplex mode. Both F1 and F2 are operated in PLL mode.
3. Synthesizer/PLL duplex mode. In this mode, F1 and F2 will be operated in different operation mode.

7.4.3 FSK Mode

LMX2571-EP supports four direct digital FSK modulation modes.

1. FSK PIN mode. 2-, 4-, and 8-level FSK modulation. Modulation data is fed to the device through dedicated pins.
2. FSK SPI mode. 2-, 4-, and 8-level FSK modulation. Pre-defined FSK deviation is selected through SPI programming.
3. FSK SPI FAST mode. This mode supports arbitrary-level FSK modulation. Desired FSK deviation is written to the device through SPI programming.
4. FSK I2S mode. Arbitrary-level FSK modulation is supported. Desired FSK deviation is fed to the device through dedicated pins.

7.5 Programming

The LMX2571-EP is programmed using several 24-bit registers. A 24-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a data field, an address field, and a R/W bit. The MSB is the R/W bit. 0 means register write while 1 means register read. The following 7 bits, ADDR[6:0], form the address field which is used to decode the internal register address. The remaining 16 bits form the data field DATA[15:0]. While LE is low, serial data is clocked into the shift register upon the rising edge of clock. Serial data is shifted MSB first into the shift register when programming. When LE goes high, data is transferred from the data field into the selected active register bank. See 图 6-1 for timing diagram details.

7.5.1 Recommended Initial Power on Programming Sequence

When the device is first powered up, it must to be initialized, and the ordering of this programming is important. The sequence is listed below. After this sequence is completed, the device should be running and locked to the proper frequency.

1. Apply power to the device and ensure the Vcc pins are at the proper levels.
2. If CE is LOW, pull it HIGH.
3. Wait 100 µs for the internal LDOs to become stable.
4. Ensure that a valid reference is applied to the OSCin pin.
5. Program register R0 with RESET=1. This will ensure all the registers are reset to their default values.

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6. Program in sequence registers R60, R58, R53, ⋯, R1 and then R0.

7.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies in different scenarios is as follows:

1. If the N-divider is changing, program the relevant registers, then program R0 with FCAL_EN = 1.
2. In FSK SPI mode, FSK SPI FAST mode, and FSK I2S mode, the fractional numerator is changing; program the relevant registers only.
3. If switching frequency between F1 and F2, program the relevant control registers only toggle the F1F2_SEL bit.

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7.6 Register Maps

REG.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	R/W	ADDRESS[6:0]							DATA[15:0]																
R60	R/W	0	1	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3C4000h
R58	R/W	0	1	1	1	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	3A0C00h
R53	R/W	0	1	1	0	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	352802h
R47	R/W	0	1	0	1	1	1	1	0	DITHERING		0	0	0	0	0	0	0	0	0	0	0	0	0	2F0000h
R46	R/W	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	VCO_SEL_STRT	VCO_SEL		2E001Ah
R42	R/W	0	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	EXTVCO_CP_POL	EXTVCO_CP_IDN					2A0210h
R41	R/W	0	1	0	1	0	0	1	0	0	0	0	EXTVCO_CP_IUP					EXTVCO_CP_GAIN		CP_IDN					290810h
R40	R/W	0	1	0	1	0	0	0	0	0	0	CP_IUP					CP_GAIN		0	1	1	1	0	0	28101Ch
R39	R/W	0	1	0	0	1	1	1	0	0	0	1	0	0	0	1	1	1	1	1	SDO_LD_SEL	0	1	LD_EN	2711F0h
R35	R/W	0	1	0	0	0	1	1	0	0	MULT_WAIT											OUTBUF_AUTO MUTE	OUTBUF_TX_TYPE	OUTBUF_RX_TYPE	230647h
R34	R/W	0	1	0	0	0	1	0	IPBUF DIFF_TERM	0	0	1	0	0	0	FSK_I2S_FS_POL	FSK_I2S_CLK_POL	FSK_LEVEL		FSK_DEV_SEL			FSK_MODE_SEL0	FSK_MODE_SEL1	221000h
R33	R/W	0	1	0	0	0	0	1	FSK_DEV_SPI_FAST																210000h
R32	R/W	0	1	0	0	0	0	0	FSK_DEV7_F2																200000h
R31	R/W	0	0	1	1	1	1	1	FSK_DEV6_F2																1F0000h
R30	R/W	0	0	1	1	1	1	0	FSK_DEV5_F2																1E0000h
R29	R/W	0	0	1	1	1	0	1	FSK_DEV4_F2																1D0000h
R28	R/W	0	0	1	1	1	0	0	FSK_DEV3_F2																1C0000h
R27	R/W	0	0	1	1	0	1	1	FSK_DEV2_F2																1B0000h
R26	R/W	0	0	1	1	0	1	0	FSK_DEV1_F2																1A0000h
R25	R/W	0	0	1	1	0	0	1	FSK_DEV0_F2																190000h
R24	R/W	0	0	1	1	0	0	0	0	0	0	0	0	FSK_EN_F2	EXTVCO_CHDIV_F2				EXTVCO_SEL_F2	OUTBUF_TX_PWR_F2					180010h
R23	R/W	0	0	1	0	1	1	1	0	0	0	OUTBUF_RX_PWR_F2					OUTBUF_TX_EN_F2	OUTBUF_RX_EN_F2	0	0	0	LF_R4_F2			1710A4h
R22	R/W	0	0	1	0	1	1	0	LF_R3_F2			CHDIV2_F2			CHDIV1_F2		PFD_DELAY_F2			MULT_F2					168584h
R21	R/W	0	0	1	0	1	0	1	PLL_R_F2								PLL_R_PRE_F2								150101h
R20	R/W	0	0	1	0	1	0	0	PLL_N_PRE_F2	FRAC_ORDER_F2			PLL_N_F2												140028h
R19	R/W	0	0	1	0	0	1	1	PLL_DEN_F2[15:0]																130000h
R18	R/W	0	0	1	0	0	1	0	PLL_NUM_F2[15:0]																120000h
R17	R/W	0	0	1	0	0	0	1	PLL_DEN_F2[23:16]								PLL_NUM_F2[23:16]								110000h
R16	R/W	0	0	1	0	0	0	0	FSK_DEV7_F1																100000h

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REG.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	R/W	ADDRESS[6:0]							DATA[15:0]																
R15	R/W	0	0	0	1	1	1	1	FSK_DEV6_F1																F0000h
R14	R/W	0	0	0	1	1	1	0	FSK_DEV5_F1																E0000h
R13	R/W	0	0	0	1	1	0	1	FSK_DEV4_F1																D0000h
R12	R/W	0	0	0	1	1	0	0	FSK_DEV3_F1																C0000h
R11	R/W	0	0	0	1	0	1	1	FSK_DEV2_F1																B0000h
R10	R/W	0	0	0	1	0	1	0	FSK_DEV1_F1																A0000h
R9	R/W	0	0	0	1	0	0	1	FSK_DEV0_F1																90000h
R8	R/W	0	0	0	1	0	0	0	0	0	0	0	0	FSK_EN_F1	EXTVCO_CHDIV_F1				EXTVCO_SEL_F1	OUTBUF_TX_PWR_F1					80010h
R7	R/W	0	0	0	0	1	1	1	0	0	0	OUTBUF_RX_PWR_F1					OUTBUF_TX_EN_F1	OUTBUF_RX_EN_F1	0	0	0	LF_R4_F1			710A4h
R6	R/W	0	0	0	0	1	1	0	LF_R3_F1			CHDIV2_F1			CHDIV1_F1		PFD_DELAY_F1			MULT_F1					68584h
R5	R/W	0	0	0	0	1	0	1	PLL_R_F1								PLL_R_PRE_F1								50101h
R4	R/W	0	0	0	0	1	0	0	PLL_N_PRE_F1	FRAC_ORDER_F1			PLL_N_F1												40028h
R3	R/W	0	0	0	0	0	1	1	PLL_DEN_F1[15:0]																30000h
R2	R/W	0	0	0	0	0	1	0	PLL_NUM_F1[15:0]																20000h
R1	R/W	0	0	0	0	0	0	1	PLL_DEN_F1[23:16]								PLL_NUM_F1[23:16]								10000h
R0	R/W	0	0	0	0	0	0	0	0	0	RESET	POWER DOWN	0	0	F1F2_INIT	0	F1F2_MODE	F1F2_SEL	0	0	0	0	1	FCAL_EN	3h

The POR value is the power-on reset value that is assigned when the device is powered up or the RESET bit is asserted. POR is not a default working mode, all registers are required to program properly in order to make the device works as desired.

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7.6.1 R60 Register (offset = 3Ch) [reset = 4000h]

图 7-7. R60 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-4000h															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-6. R60 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0		R/W	4000h	Program A000h to this field.

7.6.2 R58 Register (offset = 3Ah) [reset = C00h]

图 7-8. R58 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
R/W-C00h															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-7. R58 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0		R/W	C00h	Program 8C00h to this field.

7.6.3 R53 Register (offset = 35h) [reset = 2802h]

图 7-9. R53 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0
R/W-2802h															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-8. R53 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0		R/W	2802h	Program 7806h to this field.

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7.6.4 R47 Register (offset = 2Fh) [reset = 0h]

图 7-10. R47 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	DITHERING		0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h		R/W-0h												

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-9. R47 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15		R/W	0h	Program 0h to this field.
14-13	DITHERING	R/W	0h	Set the level of dithering. This feature is used to mitigate spurs level in certain use case by increasing the level of randomness in the Delta Sigma modulator, typically done at the expense of noise at certain offset. 0 = Disabled 1 = Weak 2 = Medium 3 = Strong
12-0		R/W	0h	Program 0h to this field.

7.6.5 R46 Register (offset = 2Eh) [reset = 1Ah]

图 7-11. R46 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	1	VCO_SEL_STRT	VCO_SEL	
R/W-1Ah															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-10. R46 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-3		R/W	3h	Program 3h to this field.
2	VCO_SEL_STRT	R/W	0h	Enables VCO calibration to start with the VCO core being selected in VCO_SEL. Please note that programming to this register is optional. That is, you do not need to program this register, the default POR value of this register will ensure that the right VCO core will be picked up automatically. 0 = Disabled 1 = Enabled
1-0	VCO_SEL	R/W	2h	Set the VCO core to start calibration with. Please note that programming to this register is optional. That is, you do not need to program this register, the default POR value of this register will ensure that the right VCO core will be picked up automatically. 0 = VCOL 1 = VCOM 2 = VCOH

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7.6.6 R42 Register (offset = 2Ah) [reset = 210h]

图 7-12. R42 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	EXTVCO_CP_POL	EXTVCO_CP_IDN				
R/W-8h										R/W-0h	R/W-10h				

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-11. R42 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-6		R/W	8h	Program 8h to this field.
5	EXTVCO_CP_POL	R/W	0h	Sets the phase detector polarity for external VCO in PLL mode operation. Positive means VCO frequency increases directly proportional to Vtune voltage. 0 = Positive 1 = Negative
4-0	EXTVCO_CP_IDN	R/W	10h	Set the base charge pump current for external VCO in PLL mode operation. The total base charge pump current is equal to EXTVCO_CP_IDN + EXTVCO_CP_IUP. EXTVCO_CP_IDN must be equal to EXTVCO_CP_IUP. Only even number values are supported. 0 = Tri-state 2 = 312.5 µA 4 = 625 µA ... 30 = 3437.5 µA

7.6.7 R41 Register (offset = 29h) [reset = 810h]

图 7-13. R41 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	EXTVCO_CP_IUP					EXTVCO_CP_GAIN	CP_IDN					
R/W-0h				R/W-10h					R/W-0h	R/W-10h					

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-12. R41 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12		R/W	0h	Program 0h to this field.
11-7	EXTVCO_CP_IUP	R/W	10h	Set the base charge pump current for external VCO in PLL mode operation. The total base charge pump current is equal to EXTVCO_CP_IDN + EXTVCO_CP_IUP. EXTVCO_CP_IDN must be equal to EXTVCO_CP_IUP. Only even number values are supported. 0 = Tri-state 2 = 312.5 µA 4 = 625 µA ... 30 = 3437.5 µA

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表 7-12. R41 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
6-5	EXTVCO_CP_GAIN	R/W	0h	Set the multiplication factor to the base charge pump current for external VCO in PLL mode operation. For example, if the gain here is 2x and if the total base charge pump current (EXTVCO_CP_IDN + EXTVCO_CP_IUP) is 2.5 mA, then the final charge pump current applied to the loop filter is 5 mA. The gain values are not precise. They are provided as a quick way to boost the total charge pump current for debug purposes or specific applications. 0 = 1x 1 = 2x 2 = 1.5x 3 = 2.5x
4-0	CP_IDN	R/W	10h	Set the base charge pump current for internal VCO in synthesizer mode operation. The total base charge pump current is equal to CP_IDN + CP_IUP. CP_IDN must be equal to CP_IUP. 0 = Tri-state 1 = 156.25 µA 2 = 312.5 µA 3 = 468.75 µA ... 31 = 3593.75 µA

7.6.8 R40 Register (offset = 28h) [reset = 101Ch]

图 7-14. R40 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	CP_IUP					CP_GAIN		0	1	1	1	0	0
R/W-0h			R/W-10h					R/W-0h				R/W-1Ch			

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-13. R40 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-13		R/W	0h	Program 0h to this field.
12-8	CP_IUP	R/W	10h	Set the base charge pump current for internal VCO in synthesizer mode operation. The total base charge pump current is equal to CP_IDN + CP_IUP. CP_IDN must be equal to CP_IUP. 0 = Tri-state 1 = 156.25 µA 2 = 312.5 µA 3 = 468.75 µA ... 31 = 3593.75 µA

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表 7-13. R40 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	CP_GAIN	R/W	0h	Set the multiplication factor to the base charge pump current for internal VCO in synthesizer mode operation. For example, if the gain here is 2x and if the total base charge pump current (CP_IDN + CP_IUP) is 2.5 mA, then the final charge pump current applied to the loop filter is 5 mA. The gain values are not precise. They are provided as a quick way to boost the total charge pump current for debug purposes or specific applications. 0 = 1x 1 = 2x 2 = 1.5x 3 = 2.5x
5-0		R/W	1Ch	Program 1Ch to this field.

7.6.9 R39 Register (offset = 27h) [reset = 11F0h]

图 7-15. R39 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	1	1	1	1	1	SDO_LD_SEL	0	1	LD_EN
R/W-11Fh												R/W-0h	R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-14. R39 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-4		R/W	11Fh	Program 11Fh to this field.
3	SDO_LD_SEL	R/W	0h	Defines the MUXout pin function. 0 = Register readback serial data output 1 = Lock detect output
2-1		R/W	0h	Program 1h to this field.
0	LD_EN	R/W	0h	Enables lock detect function. 0 = Disabled 1 = Enabled

7.6.10 R35 Register (offset = 23h) [reset = 647h]

图 7-16. R35 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	MULT_WAIT											OUTB UF_AU TOMU TE	OUTB UF_TX _TYPE	OUTB UF_RX _TYPE
R/W-0h		R/W-C8h											R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-15. R35 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14		R/W	0h	Program 0h to this field.

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表 7-15. R35 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
13-3	MULT_WAIT	R/W	C8h	A 20-µs settling time is required for MULT, if it is enabled. These bits set the correct settling time according to the OSCin frequency. For example, if OSCin frequency is 100 MHz, set these bits to 2000. No matter if MULT is enabled or not, the configured MULT settling time forms part of the total frequency switching time. 0 = Do not use this setting 1 = 1 OSCin clock cycle ... 2047 = 2047 OSCin clock cycles
2	OUTBUF_AUTOMUTE	R/W	1h	If this bit is set, the output buffers will be muted until PLL is locked. This bit applies to the following events: (a) device initialization (b) manually change VCO frequency, and (c) F1F2 switching. However, if the PLL is unlocked afterward (for example, OSCin is removed), the output buffers will not be muted and will remain active. 0 = Disabled 1 = Enabled
1	OUTBUF_TX_TYPE	R/W	1h	Sets the output buffer type of RFoutTx. If the buffer is open drain output, a pullup to VccIO is required. See *RF Output Buffer Type* for details. 0 = Open drain 1 = Push pull
0	OUTBUF_RX_TYPE	R/W	1h	Sets the output buffer type of RFoutRx. If the buffer is open drain output, a pullup to VccIO is required. See *RF Output Buffer Type* for details. 0 = Open drain 1 = Push pull

7.6.11 R34 Register (offset = 22h) [reset = 1000h]

图 7-17. R34 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPBUFDIFF_TERM	0	0	1	0	0	0	FSK_I2S_FS_POL	FSK_I2S_CLK_POL	FSK_LEVEL		FSK_DEV_SEL			FSK_MODE_SEL0	FSK_MODE_SEL1
R/W-0h	R/W-0h		R/W-2h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-16. R34 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	IPBUFDIFF_TERM	R/W	0h	Enables independent 50 Ω input termination on the OSCin Pin. 0 = Disabled 1 = Enabled
14		R/W	0h	Program 0h to this field.
13-11		R/W	2h	Program 2h to this field.
10		R/W	0h	Program 0h to this field.
9		R/W	0h	Program 0h to this field.

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表 7-16. R34 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
8	FSK_I2S_FS_POL	R/W	0h	Sets the polarity of the I2S Frame Sync input in FSK I2S mode. 0 = Active HIGH 1 = Active LOW
7	FSK_I2S_CLK_POL	R/W	0h	Sets the polarity of the I2S CLK input in FSK I2S mode. 0 = Rising edge strobe 1 = Falling edge strobe
6-5	FSK_LEVEL	R/W	0h	Define the desired FSK level in FSK PIN mode and FSK SPI mode. When this bit is zero, FSK operation in these modes is disabled even if FSK_EN_Fx = 1. 0 = Disabled 1 = 2FSK 2 = 4FSK 3 = 8FSK
4-2	FSK_DEV_SEL	R/W	0h	In FSK SPI mode, these bits select one of the FSK deviations as defined in registers R25-32 or R9-16. 0 = FSK_DEV0_Fx 1 = FSK_DEV1_Fx ... 7 = FSK_DEV7_Fx
1	FSK_MODE_SEL0	R/W	0h	FSK_MODE_SEL0 and FSK_MODE_SEL1 define the FSK operation mode. FSK_MODE_SEL[1:0] = 00 = FSK PIN mode 01 = FSK SPI mode 10 = FSK I2S mode 11 = FSK SPI FAST mode
0	FSK_MODE_SEL1	R/W	0h	Same as above.

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7.6.12 R33 Register (offset = 21h) [reset = 0h]

图 7-18. R33 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV_SPI_FAST															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-17. R33 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	FSK_DEV_SPI_FAST	R/W	0h	Define the desired frequency deviation in FSK SPI FAST mode. See *Direct Digital FSK Modulation* for details.

7.6.13 R25 to R32 Register (offset = 19h to 20h) [reset = 0h]

图 7-19. R25 to R32 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV0_F2 to FSK_DEV7_F2															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-18. R25 to R32 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	FSK_DEV0_F2 to FSK_DEV7_F2	R/W	0h	Define the desired frequency deviation in FSK PIN mode and FSK SPI mode. See *Direct Digital FSK Modulation* for details.

7.6.14 R24 Register (offset = 18h) [reset = 10h]

图 7-20. R24 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	FSK_EN_F2	EXTVCO_CHDIV_F2				EXTVCO_SEL_F2	OUTBUF_TX_PWR_F2				
R/W-0h					R/W-0h	R/W-0h				R/W-0h	R/W-10h				

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-19. R24 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-11		R/W	0h	Program 0h to this field.
10	FSK_EN_F2	R/W	0h	Enables FSK operation in all FSK operation modes. When this bit is set, fractional denominator DEN should be zero. See *Direct Digital FSK Modulation* for details. 0 = Disabled 1 = Enabled

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表 7-19. R24 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
9-6	EXTVCO_CHDIV_F2	R/W	0h	Set the value of the output channel divider, CHDIV3, when using external VCO in PLL mode. 0 = Divide by 1 1 = Reserved 2 = Divide by 2 3 = Divide by 3 ... 10 = Divide by 10 11-15 = Reserved
5	EXTVCO_SEL_F2	R/W	0h	Selects synthesizer mode (internal VCO) or PLL mode (external VCO) operation. 0 = Synthesizer mode 1 = PLL mode
4-0	OUTBUF_TX_PWR_F2	R/W	10h	Set the output power at RFoutTx port. See *RF Output Buffer Power Control* for details.

7.6.15 R23 Register (offset = 17h) [reset = 10A4h]

图 7-21. R23 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OUTBUF_RX_PWR_F2					OUTBUF_TX_EN_F2	OUTBUF_RX_EN_F2	0	0	0	LF_R4_F2		
R/W-0h			R/W-10h					R/W-1h	R/W-0h	R/W-4h			R/W-4h		

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-20. R23 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-13		R/W	0h	Program 0h to this field.
12-8	OUTBUF_RX_PWR_F2	R/W	10h	Set the output power at RFoutRx port. See *RF Output Buffer Power Control* for details.
7	OUTBUF_TX_EN_F2	R/W	1h	Enables RFoutTx port. 0 = Disabled 1 = Enabled
6	OUTBUF_RX_EN_F2	R/W	0h	Enables RFoutRx port. 0 = Disabled 1 = Enabled
5-3		R/W	4h	Program 0h to this field.

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表 7-20. R23 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
2-0	LF_R4_F2	R/W	4h	Set the resistor value for the 4th pole of the internal loop filter. The shunt capacitor of that pole is 100 pF. 0 = Bypass 1 = 3.2 kΩ 2 = 1.6 kΩ 3 = 1.1 kΩ 4 = 800 Ω 5 = 640 Ω 6 = 533 Ω 7 = 457 Ω

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7.6.16 R22 Register (offset = 16h) [reset = 8584h]

图 7-22. R22 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LF_R3_F2			CHDIV2_F2			CHDIV1_F2		PFD_DELAY_F2			MULT_F2				
R/W-4h			R/W-1h			R/W-1h		R/W-4h			R/W-4h				

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-21. R22 Register Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-13	LF_R3_F2	R/W	4h	Set the resistor value for the 3rd pole of the internal loop filter. The shunt capacitor of that pole is 50 pF. 0 = Bypass 1 = 3.2 kΩ 2 = 1.6 kΩ 3 = 1.1 kΩ 4 = 800 Ω 5 = 640 Ω 6 = 533 Ω 7 = 457 Ω
12-10	CHDIV2_F2	R/W	1h	Set the value of the output channel divider, CHDIV2, when using internal VCO in synthesizer mode. 0 = Divide by 1 1 = Divide by 2 2 = Divide by 4 3 = Divide by 8 4 = Divide by 16 5 = Divide by 32 6 = Divide by 64
9-8	CHDIV1_F2	R/W	1h	Set the value of the output channel divider, CHDIV1, when using internal VCO in synthesizer mode. 0 = Divide by 4 1 = Divide by 5 2 = Divide by 6 3 = Divide by 7
7-5	PFD_DELAY_F2	R/W	4h	Used to optimize spurs and phase noise. Suggested values are: Integer mode (NUM = 0): use PFD_DELAY ⩽ 5 Fractional mode with N-divider < 22: use PFD_DELAY ⩽ 4 Fractional mode with N-divider ⩾ 22: use PFD_DELAY ⩾ 3
4-0	MULT_F2	R/W	4h	Set the MULT multiplier value. MULT value must be greater than Pre-divider value. See *MULT Multiplier* for details. 0 = Reserved 1 = Bypass 2 = 2x ... 13 = 13x 14-31 = Reserved

7.6.17 R21 Register (offset = 15h) [reset = 101h]

图 7-23. R21 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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图 7-23. R21 Register (continued)

PLL_R_F2	PLL_R_PRE_F2
R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-22. R21 Register Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	PLL_R_F2	R/W	1h	Set the OSCin buffer Post-divider value.
7-0	PLL_R_PRE_F2	R/W	1h	Set the OSCin buffer Pre-divider value. This value must be smaller than MULT value.

7.6.18 R20 Register (offset = 14h) [reset = 28h]

图 7-24. R20 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_N_PRE_F2	FRAC_ORDER_F2			PLL_N_F2											
R/W-0h	R/W-0h			R/W-28h											

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-23. R20 Register Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	PLL_N_PRE_F2	R/W	0h	Sets the Prescaler value. 0 = Divide by 2 1 = Divide by 4
14-12	FRAC_ORDER_F2	R/W	0h	Select the order of the Delta Sigma modulator. 0 = Integer mode 1 = 1st order 2 = 2nd order 3 = 3rd order 4-7 = 4th order
11-0	PLL_N_F2	R/W	28h	Set the integer portion of the N-divider value. Maximum value is 1023.

7.6.19 R19 Register (offset = 13h) [reset = 0h]

图 7-25. R19 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN_F2[15:0]															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-24. R19 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	PLL_DEN_F2[15:0]	R/W	0h	Set the LSB bits of the fractional denominator of the N-divider.

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7.6.20 R18 Register (offset = 12h) [reset = 0h]

图 7-26. R18 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_NUM_F2[15:0]															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-25. R18 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	PLL_NUM_F2[15:0]	R/W	0h	Set the LSB bits of the fractional numerator of the N-divider.

7.6.21 R17 Register (offset = 11h) [reset = 0h]

图 7-27. R17 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN_F2[23:16]								PLL_NUM_F2[23:16]							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-26. R17 Register Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	PLL_DEN_F2[23:16]	R/W	0h	Set the MSB bits of the fractional denominator of the N-divider.
7-0	PLL_NUM_F2[23:16]	R/W	0h	Set the MSB bits of the fractional numerator of the N-divider.

7.6.22 R9 to R16 Register (offset = 9h to 10h) [reset = 0h]

图 7-28. R9 to R16 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV0_F1 to FSK_DEV7_F1															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-27. R9 to R16 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	FSK_DEV0_F1 to FSK_DEV7_F1	R/W	0h	See 表 7-18.

7.6.23 R8 Register (offset = 8h) [reset = 10h]

图 7-29. R8 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	FSK_EN_F1	EXTVCO_CHDIV_F1				EXTVCO_SEL_F1	OUTBUF_TX_PWR_F1				
R/W-0h					R/W-0h	R/W-0h				R/W-0h	R/W-10h				

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

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表 7-28. R8 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-11		R/W	0h	Program 0h to this field.
10	FSK_EN_F1	R/W	0h	See 表 7-19.
9-6	EXTVCO_CHDIV_F1	R/W	0h	See 表 7-19.
5	EXTVCO_SEL_F1	R/W	0h	See 表 7-19.
4-0	OUTBUF_TX_PWR_F1	R/W	10h	See 表 7-19.

7.6.24 R7 Register (offset = 7h) [reset = 10A4h]

图 7-30. R7 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OUTBUF_RX_PWR_F1					OUTBUF_TX_EN_F1	OUTBUF_RX_EN_F1	0	0	0	LF_R4_F1		
R/W-0h			R/W-10h					R/W-1h	R/W-0h	R/W-4h			R/W-4h		

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-29. R7 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-13		R/W	0h	Program 0h to this field.
12-8	OUTBUF_RX_PWR_F1	R/W	10h	See 表 7-20.
7	OUTBUF_TX_EN_F1	R/W	1h	See 表 7-20.
6	OUTBUF_RX_EN_F1	R/W	0h	See 表 7-20.
5-3		R/W	4h	Program 0h to this field.
2-0	LF_R4_F1	R/W	4h	See 表 7-20.

7.6.25 R6 Register (offset = 6h) [reset = 8584h]

图 7-31. R6 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LF_R3_F1			CHDIV2_F1			CHDIV1_F1		PFD_DELAY_F1			MULT_F1				
R/W-4h			R/W-1h			R/W-1h		R/W-4h			R/W-4h				

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-30. R6 Register Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-13	LF_R3_F1	R/W	4h	See 表 7-21.
12-10	CHDIV2_F1	R/W	1h	See 表 7-21.
9-8	CHDIV1_F1	R/W	1h	See 表 7-21.
7-5	PFD_DELAY_F1	R/W	4h	See 表 7-21.
4-0	MULT_F1	R/W	4h	See 表 7-21.

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7.6.26 R5 Register (offset = 5h) [reset = 101h]

图 7-32. R5 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_R_F1								PLL_R_PRE_F1							
R/W-1h								R/W-1h							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-31. R5 Register Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	PLL_R_F1	R/W	1h	See 表 7-22.
7-0	PLL_R_PRE_F1	R/W	1h	See 表 7-22.

7.6.27 R4 Register (offset = 4h) [reset = 28h]

图 7-33. R4 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_N_PRE_F1	FRAC_ORDER_F1			PLL_N_F1											
R/W-0h	R/W-0h			R/W-28h											

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-32. R4 Register Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	PLL_N_PRE_F1	R/W	0h	See 表 7-23.
14-12	FRAC_ORDER_F1	R/W	0h	See 表 7-23.
11-0	PLL_N_F1	R/W	28h	See 表 7-23.

7.6.28 R3 Register (offset = 3h) [reset = 0h]

图 7-34. R3 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN_F1[15:0]															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-33. R3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	PLL_DEN_F1[15:0]	R/W	0h	See 表 7-24.

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7.6.29 R2 Register (offset = 2h) [reset = 0h]

图 7-35. R2 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_NUM_F1[15:0]															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-34. R2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	PLL_NUM_F1[15:0]	R/W	0h	See 表 7-25.

7.6.30 R1 Register (offset = 1h) [reset = 0h]

图 7-36. R1 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN_F1[23:16]								PLL_NUM_F1[23:16]							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-35. R1 Register Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	PLL_DEN_F1[23:16]	R/W	0h	See 表 7-26.
7-0	PLL_NUM_F1[23:16]	R/W	0h	See 表 7-26.

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7.6.31 R0 Register (offset = 0h) [reset = 3h]

图 7-37. R0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	RESET	POWERDOWN	0	0	F1F2_INIT	0	F1F2_MODE	F1F2_SEL	0	0	0	0	1	FCAL_EN
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h					R/W-1h

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 7-36. R0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14		R/W	0h	Program 0h to this field.
13	RESET	R/W	0h	Resets all the registers to the default values. This bit is self-clearing. 0 = Normal operation 1 = Reset
12	POWERDOWN	R/W	0h	Powers down the device. When the device comes out of the powered down state, either by resuming this bit to zero or by pulling back CE pin HIGH (if it was powered down by CE pin), it is required that register R0 with FCAL_EN = 1 be programmed again to re-calibrate the device. A 100-µs wait-time is recommended before programming R0. 0 = Normal operation 1 = Power down
11		R/W	0h	Program this field to 0h.
10		R/W	0h	Program this field to 0h.
9	F1F2_INIT	R/W	0h	Toggling this bit re-calibrates F1F2 if F1, F2 are modified after calibration. This bit is not self-clear, so it is required to clear the bit value after use. See *Register R0 F1F2_INIT, F1F2_MODE Usage* for details. 0 = Clear bit value 1 = Re-calibrate
8		R/W	0h	Program this field to 0h.
7	F1F2_MODE	R/W	0h	Calibrates F1 and F2 during device initialization (initial power on programming). Even if this bit is not set, F1-F2 switching is still possible but the first switching time will not be optimized because either F1 or F2 will only be calibrated. If F1-F2 switching is not required, set this bit to zero. See *Register R0 F1F2_INIT, F1F2_MODE Usage* for details. 0 = Disable F1F2 calibration 1 = Enable F1F2 calibration
6	F1F2_SEL	R/W	0h	Selects F1 or F2 configuration registers. 0 = F1 registers 1 = F2 registers
5-1		R/W	1h	Program 1h to this field.
0	FCAL_EN	R/W	1h	Activates all kinds of calibrations, suggest keep it enabled all the time. If it is desired that the R0 register be programmed without activating this calibration, then this bit can be set to zero. 0 = Disabled 1 = Enabled

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8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Direct Digital FSK Modulation

In fractional mode, the finest delta frequency difference between two programmable output frequencies is equal to:

$$f_1 - f_2 = \Delta f_{min} = f_{PD} \times \{[(N + 1) / DEN] - (N / DEN)\} = f_{PD} / DEN \quad (3)$$

In other words, when the fractional numerator is incremented by 1 (one step), the output frequency will change by Δf_{min}. A two steps increment will therefore change the frequency by $2 \times \Delta f_{min}$.

In FSK operation, the instantaneous carrier frequency is kept changing among some pre-defined frequencies. In general, the instantaneous carrier frequency is defined as a certain frequency deviation from the nominal carrier frequency. The frequency deviation could be positive and negative.

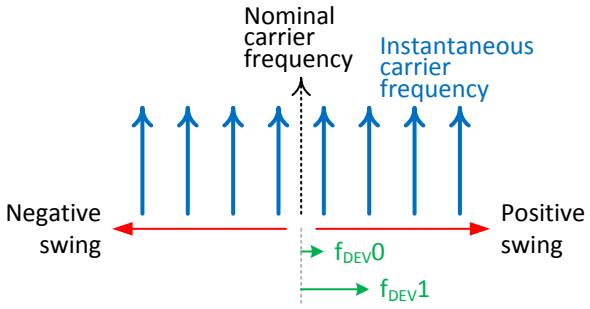


图 8-1. General FSK Definition

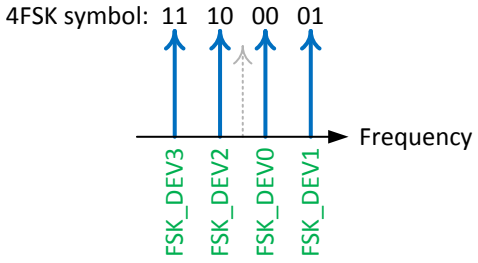


图 8-2. Typical 4FSK Definition

The following equations define the number of steps required for the desired frequency deviation with respect to the nominal carrier frequency output at the RFoutTx or RFoutRx port.

表 8-1. FSK Step Equations

POLARITY	SYNTHESIZER MODE	PLL MODE
POSITIVE SWING	$\text{Round}\left(\frac{f_{DEV} * DEN}{f_{PD}} * \frac{CHDIV1 * CHDIV2}{Prescaler}\right)$ (4)	$\text{Round}\left(\frac{f_{DEV} * DEN}{f_{PD}} * CHDIV3\right)$ (5)
NEGATIVE SWING	2's complement of Equation 4 (6)	2's complement of Equation 5 (7)

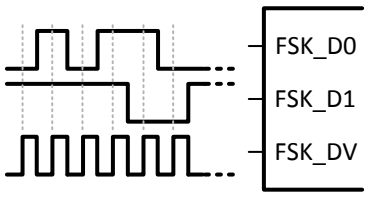
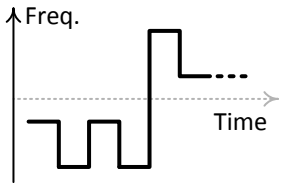
In FSK PIN mode and FSK SPI mode, register R25-32 and R9-16 are used to store the desired FSK frequency deviations in term of the number of step as defined in the above equations. The order of the registers, 0 to 7, depends on the application system. 图 8-2 shows a typical 4FSK definition. In this case, FSK_DEV0_Fx and FSK_DEV1_Fx shall be calculated using 方程式 4 or 方程式 5 while FSK_DEV2_Fx and FSK_DEV3_Fx shall be calculated using 方程式 6 or 方程式 7.

For example, if FSK PIN mode is enabled in F1 to support 4FSK modulation, set FSK_MODE_SEL1 = 0

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FSK_MODE_SEL0 = 0
FSK_LEVEL = 2
FSK_EN_F1 = 1

表 8-2. FSK PIN Mode Example

RAW FSK DATA STREAM INPUT	EQUIVALENT SYMBOL INPUT	REGISTER SELECTED	RF OUTPUT
	10	FSK_DEV2_F1	
	11	FSK_DEV3_F1	
	10	FSK_DEV2_F1	
	11	FSK_DEV3_F1	
	01	FSK_DEV1_F1	
	00	FSK_DEV0_F1	
	...	...	

FSK SPI mode assumes the user knows which symbol to send; user can directly write to register R34, FSK_DEV_SEL to select the desired frequency deviation.

For example, to enable the device to support 4FSK modulation at F1 using FSK SPI mode, set
FSK_MODE_SEL1 = 0
FSK_MODE_SEL0 = 1
FSK_LEVEL = 2
FSK_EN_F1 = 1

表 8-3. FSK SPI Mode Example

DESIRED SYMBOL	WRITE REGISTER FSK_DEV_SEL	REGISTER SELECTED
10	2	FSK_DEV2_F1
11	3	FSK_DEV3_F1
10	2	FSK_DEV2_F1
11	3	FSK_DEV3_F1
01	1	FSK_DEV1_F1
00	0	FSK_DEV0_F1
...	...	...

Both the FSK PIN mode and FSK SPI mode support up to 8 levels of FSK. To support an arbitrary-level FSK, use FSK SPI FAST mode or FSK I2S mode. Constructing pulse-shaping FSK modulation by over-sampling the FSK modulation waveform is one of the use cases of these modes.

Analog-FM modulation can also be produced in these modes. For example, with a 1-kHz sine wave modulation signal with peak frequency deviation of ±2 kHz, the signal can be over-sampled, say 10 times. Each sample point corresponding to a scaled frequency deviation.

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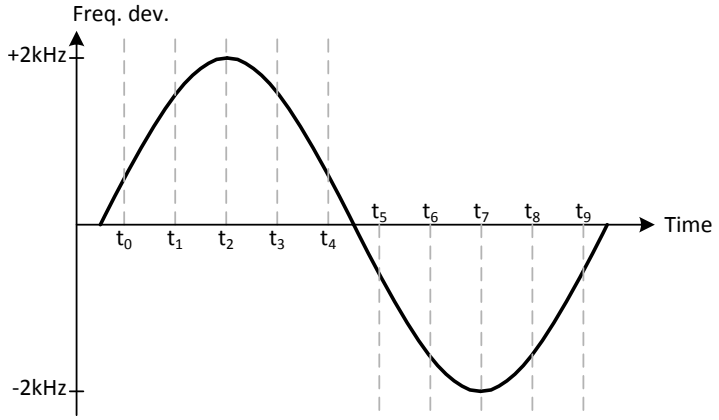


图 8-3. Over-Sampling Modulation Signal

In FSK SPI FAST mode, write the desired FSK steps directly to register R33, FSK_DEV_SPI_FAST. To enable this mode, set
FSK_MODE_SEL1 = 1
FSK_MODE_SEL0 = 1
FSK_EN_F1 = 1

表 8-4. FSK SPI FAST Mode Example

TIME	FREQUENCY DEVIATION	CORRESPONDING FSK STEPS(1)	BINARY EQUIVALENT	WRITE TO FSK_DEV_SPI_FAST
t_0	618.034 Hz	518	0000 0010 0000 0110	518
t_1	1618.034 Hz	1357	0000 0101 0100 1101	1357
t_2	2000 Hz	1678	0000 0110 1000 1110	1678
…	…	…	…	…
t_6	– 1618.034 Hz	64178	1111 1010 1011 0010	64178
t_7	– 2000 Hz	63857	1111 1001 0111 0001	63857
…	…	…	…	…

(1) Synthesizer mode, f_{VCO} = 4800 MHz, f_{OUT} = 480 MHz, f_{PD} = 100 MHz, Prescaler = 2, DEN = 2^{24}, Use 方程式 4 and 方程式 6 to calculate the step value.

In FSK I2S mode, clock in the desired binary format FSK steps in the FSK_D1 pin.

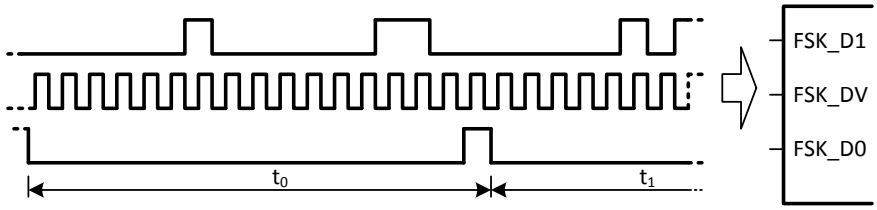


图 8-4. FSK I2S Mode Example

To enable FSK I2S mode, set
FSK_MODE_SEL1 = 1
FSK_MODE_SEL0 = 0
FSK_EN_F1 =1

8.1.2 Frequency and Output Port Switching

The F1F2_SEL bit controls the output switching.

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8.1.3 OSCin Configuration

The OSCin only supports a single-ended clock. The impedance can be programmed as high impedance or 50 Ω.

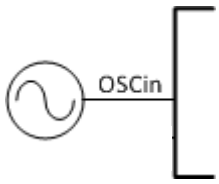


图 8-5. OSCin Configuration

8.1.4 Register R0 F1F2_INIT, F1F2_MODE Usage

These register bits are used to define the calibration behavior. Correct setting is important to ensure that every F1-F2 switching time is optimized. 图 8-6 illustrates the usage of these register bits.

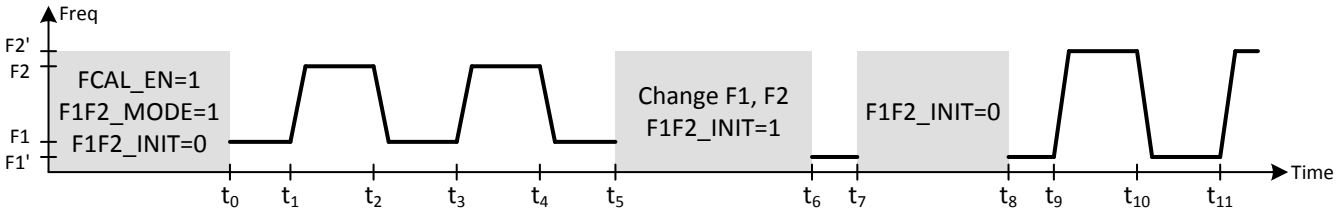


图 8-6. F1F2_INIT, F1F2_MODE Usage

Before t_0: Device initialization

- Power up the device.
- Write all registers to the device.
  - Ensure FCAL_EN = 1 to enable calibration.
  - Only the output frequency (F1 in this example) will be calibrated, F2 will not be calibrated.
  - Set F1F2_INIT = 0. Although the setting of this bit is irrelevant and not important here but if F1F2_INIT = 1, change it back to zero before attempting to change the frequency from F1 to F2.

At t_0: Locked to F1
After initialization, both F1 and F2 are calibrated. The calibration data is stored in the internal memory.

At t_1: Switch to F2.
Because FCAL_EN = 1, calibration will start over again when the output is switching from F1 to F2. F2 calibration begins based on the last calibration data, which is the calibration data obtained at t_0. If the environment (for example, temperature) does not change much, the new calibration data will be similar to the old data. As a result, the calibration time is minimal and therefore, the switching time will be short.

At t_2: Switch back to F1
Again, F1 calibration starts over and begins with the last calibration data as obtained at t_0. Calibration time is again very short, as is the switching time.

At t_3: Switch again to F2
This time, the calibration begins with the calibration data obtained at t_1, which is the last calibration data.

At t_4: Switch back to F1
Calibration begins with the calibration data obtained at t_2, which is the last calibration data.

At t_5: Set new F1, F2 frequency

- Write to the relevant registers to set the new F1 and F2 frequency (for example, change the N-divider values)
- Initiate calibration by rewriting register R0
  - Set F1F2_INIT=1. Both F1' and F2' will be calibrated

At t_6: Locked to F1'

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F1' and F2' calibration completed and their calibration data are ready.

At t_7: Release F1F2_INIT bit
This bit has to be reset to zero or otherwise both F1' and F2' will be calibrated every time they are toggling.

At t_8: F1' calibration data is updated
Since F1F2_INIT is located in register R0, when writing F1F2_INIT = 0 to the device, calibration is once again triggered. However, only F1' will be recalibrated, the calibration data of F2' remains unchanged.

At t_9: Switch to F2'
F2' calibration begins with the calibration data obtained at t_6, which is the last calibration data. Calibration time is again very short, as is the switching time.

At t_{10}: Switch back to F1'
F1' calibration starts over and begins with the last calibration data as obtained at t_8.

At t_{11}: Switch again to F2'
The calibration begins with the calibration data obtained at t_9, which is the last calibration data.

As illustrated above, register F1F2_INIT must be used properly in order to ensure that every F1-F2 switching time is optimized.

8.1.5 FastLock With External VCO

Fastlock may be required in PLL mode where an external VCO with a narrow loop bandwidth is desired. The LMX2571-EP adopts a new FastLock approach to support the very fast switching time requirement in PLL mode.

There are two control pins in the chip, FLout1 and FLout2. Each pin is used to control a SPST analog switch, S1 and S2. The loop filter value with or without FastLock is the same, except that with FastLock, one more C2 and two SPST switches are needed.

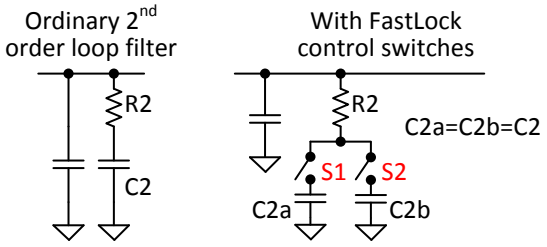


图 8-7. FastLock With SPST Switches

When LMX2571-EP is locked to F1, FLout1 will close the switch S1. When the LMX2571-EP is locked to F2, the user can program the F1F2_SEL bit in the R0 register to release the switch S1 while the FLout2 closes the S2. Although S1 is released, the charge stored in C2a remains unchanged. Thus, when the output is switched back to F1, the Vtune voltage is almost correct, no (or little) charging or discharging to C2a is required which speeds up the switching time. For example, if Vtune for F1 and F2 are 1 V and 2 V, respectively, without FastLock, when the switching frequency shifts from F1 to F2, C2 will have to be re-charged from 1 V to 2 V — this is a big voltage jump. With FastLock, when S2 is closed, Vtune is almost equal to 2 V because C2b maintains the charge. Only a tiny voltage jump (re-charge) is required to make it reach the final Vtune voltage.

图 8-8 and 图 8-9 compare the frequency switching time using different switching methods. In both cases, the loop bandwidth is 4 kHz while f_{PD} is 28 MHz. 图 8-8 shows the switching time for a frequency jump from 430 MHz to 480 MHz with SPST switches. Frequency switching is toggled by the F1F2_SEL bit. Switching time is approximately 1 ms. Frequency switching in 图 8-9 is done in the traditional way. That is, change the output frequency by writing to the relevant registers such as N-divider values. In this case, because f_{PD} is very much bigger than the loop bandwidth, cycle slipping jeopardizes the switching time to more than 20 ms.

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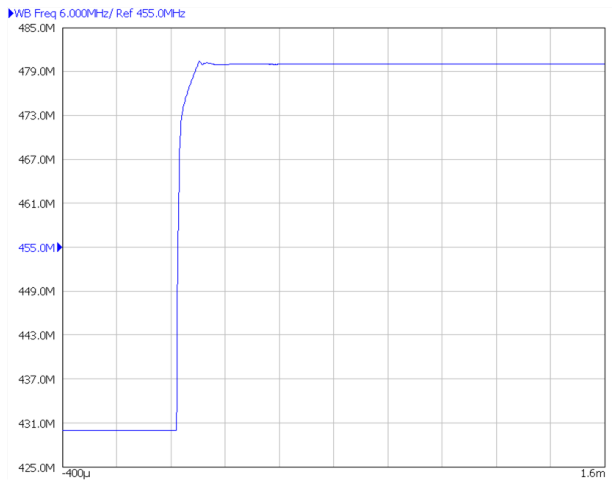


图 8-8. F1F2 Switching With SPST Switches

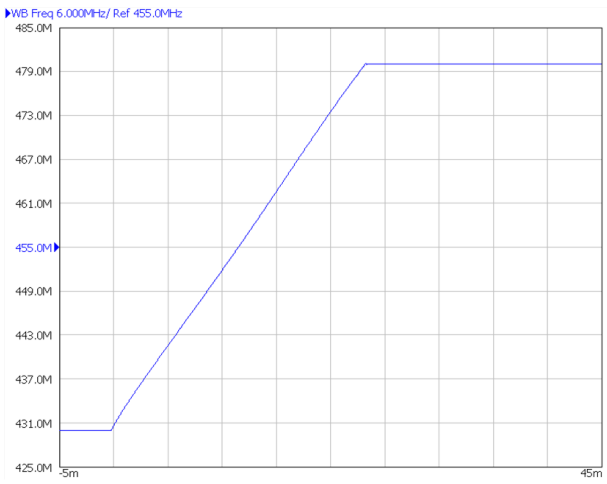


图 8-9. Change F1 Frequency Through SPI Programming

8.1.6 OSCin Slew Rate

A phase-lock loop consists of a clean reference clock, a PLL, and a VCO. Each of these contributes to the total phase noise. The LMX2571-EP is a high-performance PLL with integrated VCO. Both PLL noise and VCO noise are very good. Typical PLL 1/f noise and noise floor are –124 dBc/Hz and –231 dBc/Hz, respectively. To get the best possible phase-noise performance from the device the quality of the reference clock is very important because it may add noise to the loop. First of all, the phase noise of the reference clock must be good so that the final performance of the system is not degraded. Furthermore, using reference clock with a rather high slew rate (such as a square wave) is highly preferred. Driving the device input with a lower slew rate clock will degrade the device phase noise.

For a given frequency, a sine wave clock has the slowest slew rate, especially when the frequency is low. A CMOS clock or differential clock have much faster slew rates and are recommended. 图 8-10 shows a phase-noise comparison with different types of reference clocks. Output frequency is 480 MHz while the input clock frequency is 26 MHz. As one can see, there is a 5-dB difference in phase noise when using a clipped sine wave TCXO compared to a differential LVPECL clock. Note that the crystal option is not available in the LMX2571-EP, but is included in the LMX2571 for comparison purposes.

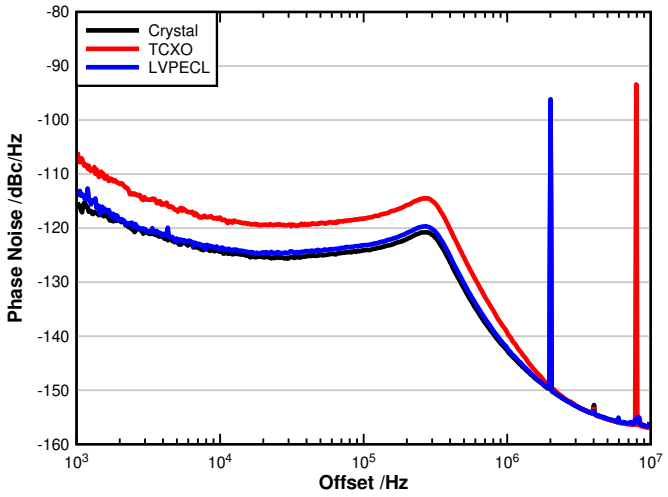


图 8-10. Phase Noise vs. Input Clock

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8.1.7 RF Output Buffer Power Control

Registers OUTBUF_TX_PWR_Fx and OUTBUF_RX_PWR_Fx are used to set the output power at the RFoutTx and RFoutRx ports. 图 8-11 shows a typical output power vs. power control bit plot in synthesizer mode. VCO frequency was 4800 MHz, and channel dividers were set to produce the shown output frequencies.

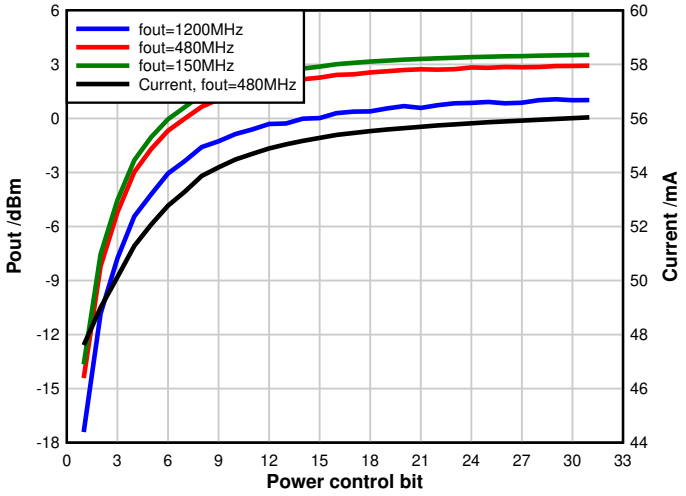
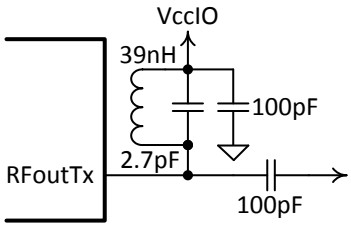
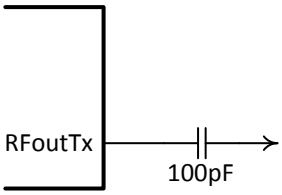


图 8-11. Configurable RF Output Power

8.1.8 RF Output Buffer Type

Registers R35, OUTBUF_TX_TYPE, OUTBUF_RX_TYPE are used to configure the RF output buffer type between open drain and push-pull. Push-pull is easy to use; all that is required is a DC-blocking capacitor at the output. The output waveform is square wave and therefore, harmonics rich. Open-drain output provides an option to reduce the harmonics using an LC resonant pullup network at its output. 表 8-5 summarizes an example an open-drain vs. push-pull application.

表 8-5. RF Output Buffer Type

BUFFER TYPE	OPEN-DRAIN			PUSH-PULL		
Connection Diagram						
Output Power	470 MHz	480 MHz	490 MHz	470 MHz	480 MHz	490 MHz
f_o	2.7 dBm	2.8 dBm	2.8 dBm	– 0.1 dBm	0 dBm	0.1 dBm
$2f_o$	– 31 dBc	– 30.7 dBc	– 30.5 dBc	– 30.4 dBc	– 30.2 dBc	– 30 dBc
$3f_o$	– 17.3 dBc	– 17.9 dBc	– 18.1 dBc	– 11.9 dBc	– 12.1 dBc	– 12.4 dBc
$4f_o$	– 39 dBc	– 40.4 dBc	– 41.6 dBc	– 28.5 dBc	– 28.4 dBc	– 28.1 dBc
$5f_o$	– 18.1 dBc	– 17.8 dBc	– 17.6 dBc	– 15.6 dBc	– 15.6 dBc	– 15.7 dBc
$6f_o$	– 27.6 dBc	– 27.2 dBc	– 28.5 dBc	– 29.5 dBc	– 29.8 dBc	– 29.3 dBc

Clearly, with a proper LC pull up in open-drain architecture, the 3rd to 5th harmonics could be reduced.

8.1.9 MULT Multiplier

The main purpose of the multiplier, MULT, in the R – divider is to push the in-band fractional spurs far away from the carrier such that the spurs could be filtered out by the loop filter. In a fractional engine, the fractional spurs

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appear at a multiple of f_{PD} × N_{frac}. In cases where both f_{PD} and N_{frac} are small, the fractional spurs will appear very close to the carrier. These kinds of spurs are called in-band spurs.

表 8-6. MULT Application Example

USE CASE	OSCin /MHz	PRE-DIVIDER	MULT	POST-DIVIDER	f_{PD} /MHz	VCO /MHz	$N_{integer}$	N_{frac}	SPURS / MHz
I	19.2	1	1	1	19.2	460.8	24	0	0
II	19.2	1	1	1	19.2	461	24	0.0104167	0.2
III	19.2	1	5	4	24	461	19	0.2083333	5

In Case I, the VCO frequency is an integer multiple of the f_{PD}, so N_{frac} is zero and there are no spurs. However, in Case II, the spur appears at an offset of 200 kHz. If this spur cannot be reduced by other typical spur-reduction techniques such as dithering, user can enable the MULT to overcome this problem. If the MULT is enabled as depicted in Case III, the spurs can be pushed to an offset of 5 MHz. In this case, the MULT together with the Post-divider changes the phase detector to a little bit higher frequency. As a consequence, the spurs are pushed further away from the carrier and are reduced more by the loop filter.

Another use case of MULT is to make higher phase-detector frequency. For example, if OSCin is 20 MHz, user can set MULT to 5 to make f_{PD} go to 100 MHz. As a result, the N-divider value will be reduced by 5 times; therefore, the PLL phase noise is reduced. A wide loop bandwidth can then be used to reduce the VCO noise. Consequently, the synthesizer close-in phase noise would be very good.

The MULT multiplier is an active device in nature, whenever it is enabled, it will add noise to the loop. For best phase noise performance, TI recommends setting the MULT not greater than 6.

To use the MULT, beware of the restriction as indicated in the *Electrical Characteristics* table and 表 7-21.

8.1.10 Integrated VCO

The integrated VCO is composed of 3 VCO cores. The approximate frequency ranges for the three VCO cores with their gains is as follows:

表 8-7. Approximate VCO Ranges and VCO Gain

VCO CORE	TYPICAL FREQUENCY RANGE (MHz)		TYPICAL VCO GAIN (MHz/V)		
	LOW	HIGH	LOW	MID	HIGH
VCOL	4200	4700	46	52	61
VCOM	4560	5100	50	56	65
VCOH	4920	5520	55	63	73

8.2 Typical Applications

8.2.1 Synthesizer Duplex Mode

In this example, the internal VCO is being used. The PLL will be put in fractional mode to support 4FSK direct digital modulation using FSK PIN mode. Both frequency (F1, F2) switching as well as RF output port switching is toggled by the F1F2_SEL bit. MULT multiplier in the R-divider will be used to reduce spurs.

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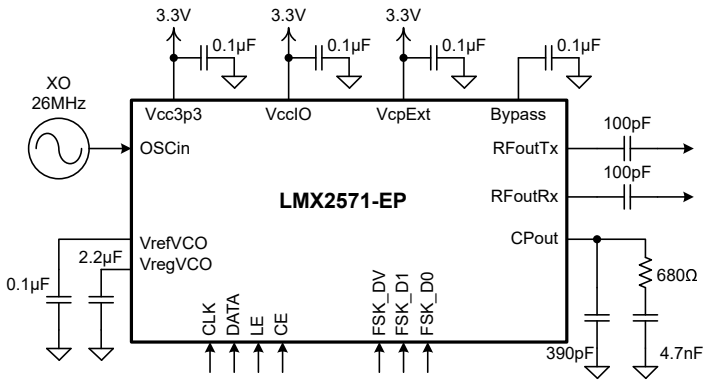


图 8-12. Typical Synthesizer Duplex Mode Application Schematic

8.2.1.1 Design Requirements

OSCin frequency = 26 MHz, LVCMOS
RFoutTx frequency = 902 MHz
RFoutRx frequency = 928 MHz
Frequency switching time ⩽ 500 µs
4FSK modulation on TX, baud rate = 20 kSPs
Frequency deviation = ±10 kHz and ±30 kHz
FSK error ⩽ 1 %
Spurs ⩽ –72 dBc
Lock detect is required to indicate lock status
Output power < 1 dBm

8.2.1.2 Detailed Design Procedure

First of all, calculate all the frequencies in each functional block.

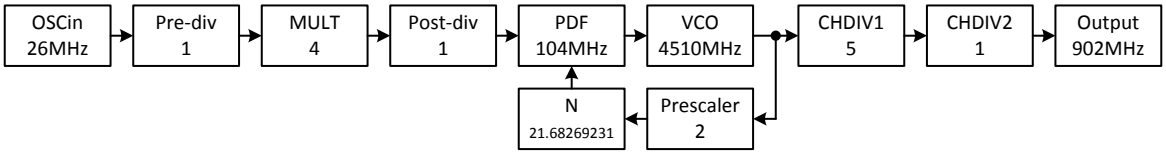


图 8-13. F1 Frequency Plan

Assign F1 frequency to be 902 MHz. With CHDIV1 = 5 and CHDIV2 = 1, the total division is 5. As a result, the VCO frequency will be 902 × 5 = 4510 MHz, which is within the VCO tuning range.

OSCin is 26 MHz, put Pre-divider = 1 to meet the MULT input frequency range requirement.

To meet the maximum MULT output frequency requirement, possible MULT values are 3 to 5. Play around the allowable MULT values and Post-divider values to get the optimum phase noise and spurs performance. Assuming MULT = 4 and Post-divider = 1 returns the best performance, then f_{PD} = 104 MHz.

N-divider = 21.68269231, that means $N_{integer}$ = 21 while N_{frac} = 0.68269231. To use the direct digital modulation feature, put fractional denominator, DEN = 0. The actual DEN value is, in fact, equal to 2^{24} = 16777216. So the fractional numerator, NUM, is equal to N_{frac} × DEN = 11453676.

Use 方程式 4 and 方程式 6 to calculate the required FSK steps. For +10-kHz frequency deviation, the FSK step value is equal to [10000 × 16777216 / (104 × 10^6)] × (5 × 1 / 2) = 4033. For –10-kHz frequency deviation, the FSK step value is equal to 2's complement of 4033 = 61502. Similarly, the FSK step values for ±30-kHz frequency deviation are 12099 and 53436.

All the required configuration values for F2, 928 MHz can be calculated in the similar fashion and are summarized as follows:

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表 8-8. Frequency Plan Summary

CONFIGURATION PARAMETER	F1 (902 MHz)	F2 (928 MHz)
Pre-divider	1	1
MULT	4	4
Post-divider	1	1
PDF	104 MHz	104 MHz
VCO	4510 MHz	4640 MHz
N-divider	21.68269231	22.30769231
$N_{integer}$	21	22
DEN	0	0
NUM	11453676	5162220
CHDIV1	5	5
CHDIV2	1	1
FSK_DEV0	4033	
FSK_DEV1	12099	
FSK_DEV2	61502	
FSK_DEV3	53436	

Assume here that the base charge pump current = 1250 µA, CP Gain = 1x and 3rd order Delta Sigma Modulator without dithering is adopted in both frequency sets. The register settings are summarized as follows:

表 8-9. Register Settings Summary

CONFIGURATION PARAMETERS	REGISTER BIT	COMMON SETTING	F1 SPECIFIC SETTING	F2 SPECIFIC SETTING
VCO calibration	FCAL_EN	1 = Enabled		
Lock detect	SDO_LE_SEL	1 = Lock detect output		
	LD_EN	1 = Enabled		
Dithering	DITHERING	0 = Disabled		
Charge pump gain	CP_GAIN	1 = 1x		
Base charge pump current	CP_IUP	8 = 1250 µA		
	CP_IDN	8 = 1250 µA		
MULT settling time	MULT_WAIT	520 = 20 µs		
Output buffer type	OUTBUF_RX_TYPE	1 = Push pull		
	OUTBUF_TX_TYPE	1 = Push pull		
Output buffer auto mute	OUTBUF_AUTOMUTE	0 = Disabled		
Enable F1 F2 initialization	F1F2_MODE	1 = Enabled		
Pre-divider	PLL_R_PRE_F1		1	
	PLL_R_PRE_F2			1
MULT multiplier	MULT_F1		4	
	MULT_F2			4
Post-divider	PLL_R_F1		1	
	PLL_R_F2			1
ΔΣ modulator order	FRAC_ORDER_F1		3 = 3rd order	
	FRAC_ORDER_F2			3 = 3rd order
PFD delay	PFD_DELAY_F1		5 = 8 clock cycles	
	PFD_DELAY_F2			5 = 8 clock cycles
CHDIV1 divider	CHDIV1_F1		1 = Divide by 5	
	CHDIV1_F2			1 = Divide by 5
CHDIV2 divider	CHDIV2_F1		0 = Divide by 1	
	CHDIV2_F2			0 = Divide by 1

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表 8-9. Register Settings Summary (continued)

CONFIGURATION PARAMETERS	REGISTER BIT	COMMON SETTING	F1 SPECIFIC SETTING	F2 SPECIFIC SETTING
Internal 3rd pole loop filter	LF_R3_F1		4 = 800 Ω	
	LF_R3_F2			4 = 800 Ω
Internal 4th pole loop filter	LF_R4_F1		4 = 800 Ω	
	LF_R4_F2			4 = 800 Ω
Output port selection	OUTBUF_TX_EN_F1		1 = TX port enabled	
	OUTBUF_RX_EN_F2			1 = RX port enabled
Output power control	OUTBUF_TX_PWR_F1		6	
	OUTBUF_RX_PWR_F2			6
FSK mode	FSK_MODE_SEL1 FSK_MODE_SEL0	00 = FSK PIN mode		
FSK level	FSK_LEVEL	2 = 4FSK		
Enable FSK modulation	FSK_EN_F1		1 = Enabled	
FSK deviation at 00	FSK_DEV0_F1		4033 = +10 kHz	
FSK deviation at 01	FSK_DEV1_F1		12099 = +30 kHz	
FSK deviation at 10	FSK_DEV2_F1		61502 = -10 kHz	
FSK deviation at 11	FSK_DEV3_F1		53436 = -30 kHz	
Fractional denominator	PLL_DEN_F1[23:16]		0	
	PLL_DEN_F1[15:0]		0	
	PLL_DEN_F2[23:16]			0
	PLL_DEN_F2[15:0]			0
Fractional numerator	PLL_NUM_F1[23:16]		174	
	PLL_NUM_F1[15:0]		50412	
	PLL_NUM_F2[23:16]			78
	PLL_NUM_F2[15:0]			50412
$N_{integer}$	PLL_N_F1		21	
	PLL_N_F2			22
Prescaler	PLL_N_PRE_F1		0 = Divide by 2	
	PLL_N_PRE_F2			0 = Divide by 2

8.2.1.3 Synthesizer Duplex Mode Application Curves

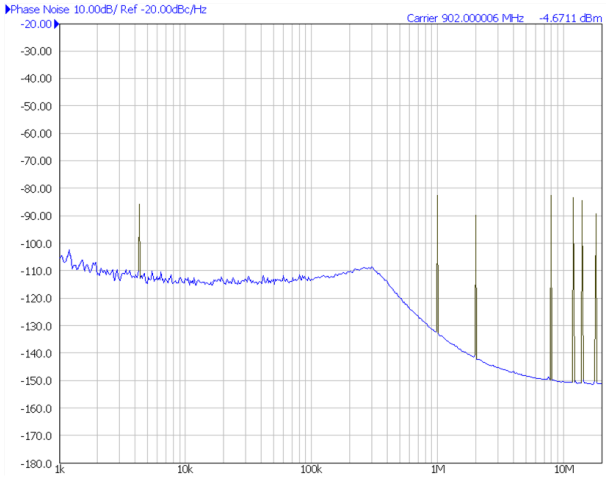


图 8-14. F1 (TX) Phase Noise and Spurs

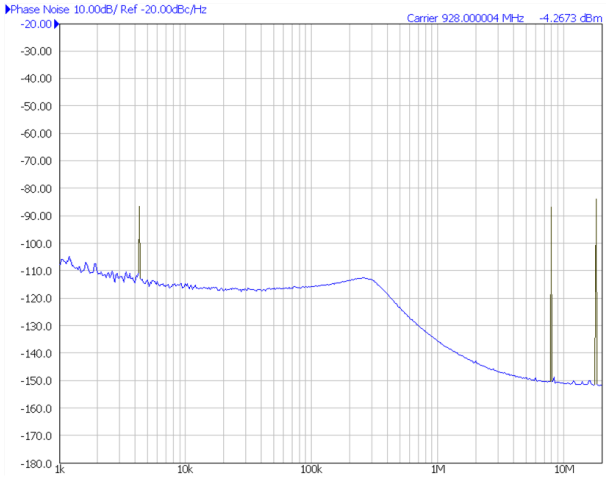


图 8-15. F2 (RX) Phase Noise and Spurs

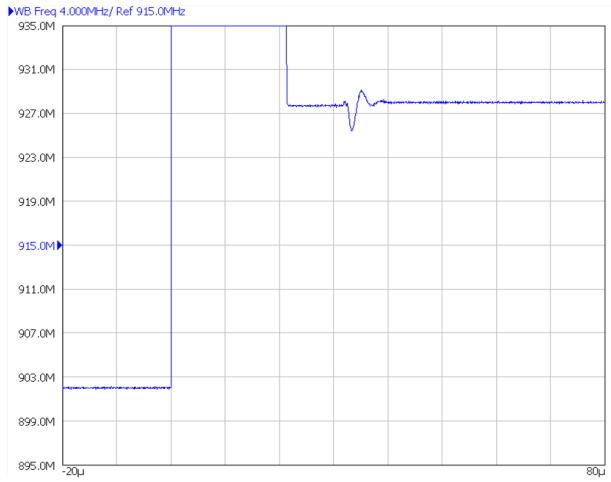


图 8-16. F1 (TX) to F2 (RX) Switching

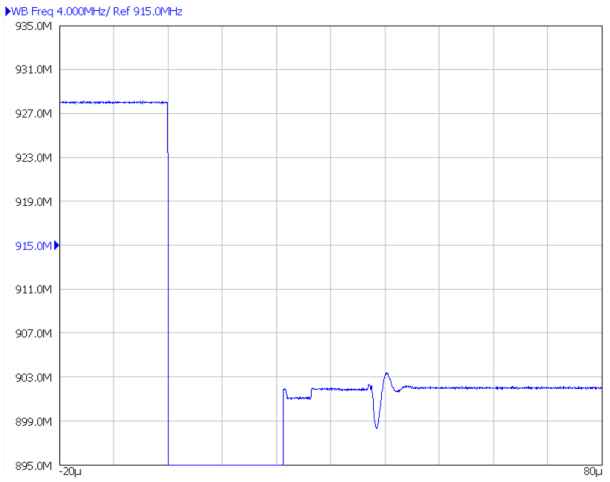


图 8-17. F2 (RX) to F1 (TX) Switching

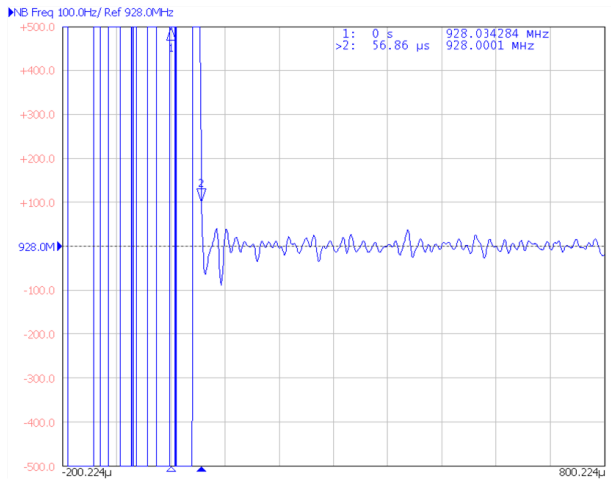


图 8-18. F1 to F2 Switching Time

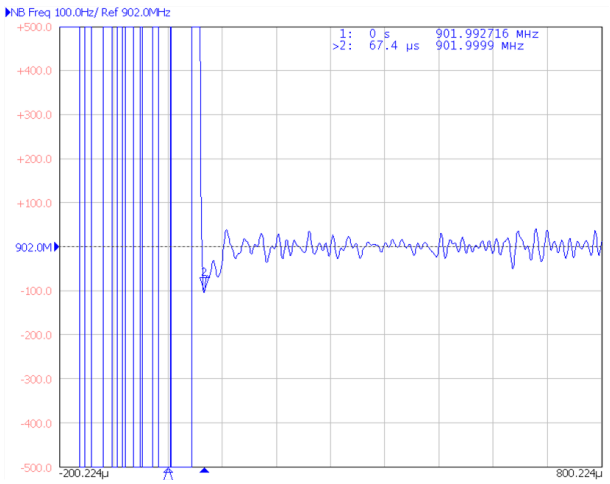


图 8-19. F2 to F1 Switching Time

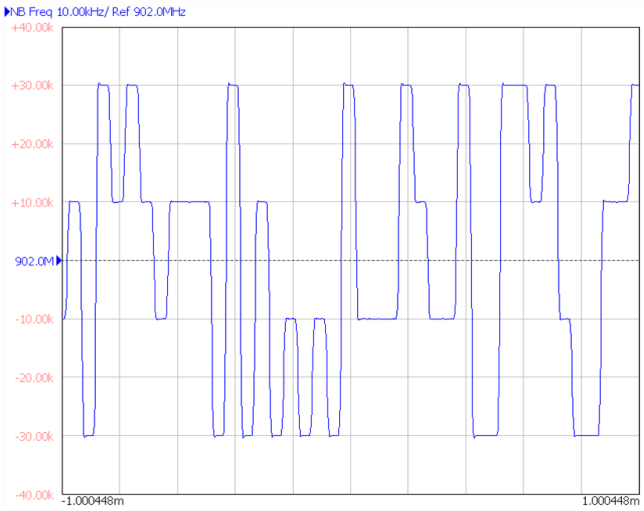


图 8-20. 4FSK Modulation

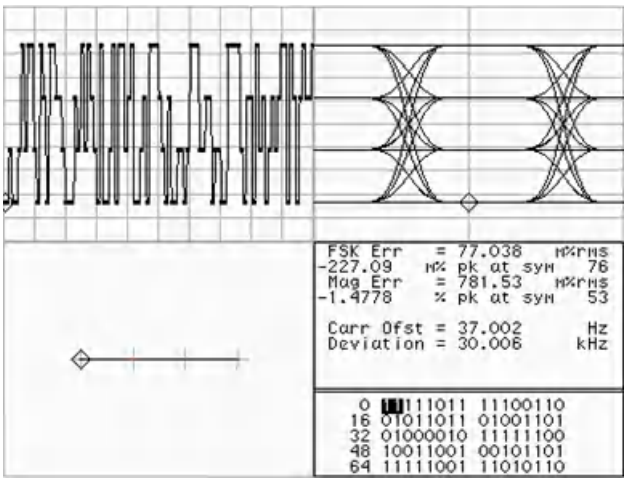


图 8-21. 4FSK Modulation Quality

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8.2.2 PLL Duplex Mode

In this example, the internal VCO is bypassed, and the device is used to lock to an external VCO. TI’s dual SPST analog switch, TS5A21366 is used to facilitate FastLock between two frequencies.

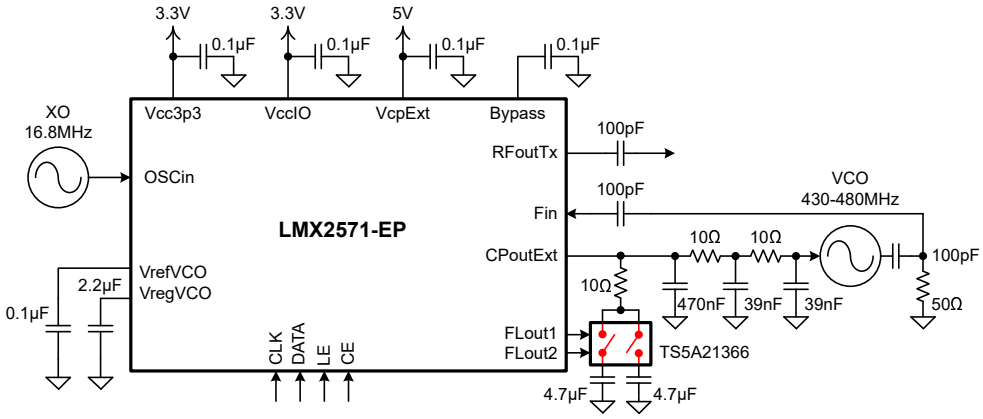


图 8-22. Typical PLL Duplex Mode Application Schematic

8.2.2.1 Design Requirements

OSCin frequency = 16.8 MHz, LVCMOS
F1 frequency = 430 MHz
F2 frequency = 480 MHz
Frequency switching time ⩽ 1.5 ms within 100-Hz frequency tolerance

8.2.2.2 Detailed Design Procedure

Again, we need to figure out all the frequencies in each functional block first.

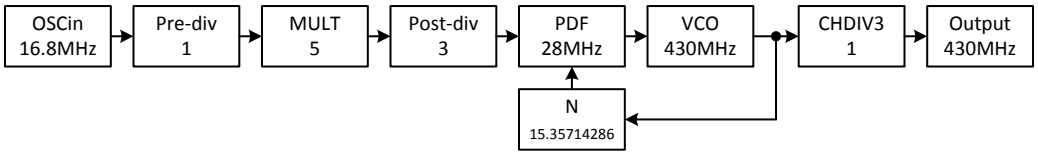


图 8-23. Frequency Plan in PLL Duplex Mode

Follow the previous example to determine all the necessary configurations. 表 8-10 is the summary in this example.

表 8-10. PLL Duplex Mode Frequency Plan Summary

CONFIGURATION PARAMETER	F1 (430 MHz)	F2 (480 MHz)
Pre-divider	1	1
MULT	5	5
Post-divider	3	3
PDF	28 MHz	28 MHz
VCO	430 MHz	480 MHz
N-divider	15.35714286	17.14285714
$N_{integer}$	15	17
DEN	1234567	1234567
NUM	440917	176367

To enable external VCO operation, set the following bits:

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表 8-11. PLL Duplex Mode Register Settings Summary

CONFIGURATION PARAMETER	REGISTER BITS	SETTING
Charge pump polarity	EXTVCO_CP_POL	0 = Positive
External VCO charge pump gain	EXTVCO_CP_GAIN	1 = 1x
Base charge pump current	EXTVCO_CP_IUP	8 = 1250 µA
	EXTVCO_CP_IDN	8 = 1250 µA
Select PLL mode operation	EXTVCO_SEL_F1, EXTVCO_SEL_F2	1 = External VCO
CHDIV3 divider	EXTVCO_CHDIV_F1, EXTVCO_CHDIV_F2	0 = Bypass

Make sure that register R0, FCAL_EN is set so that FastLock is enabled.

The loop bandwidth had been design to be around 4 kHz, while phase margin is about 40 degrees.

8.2.2.3 PLL Duplex Mode Application Curves

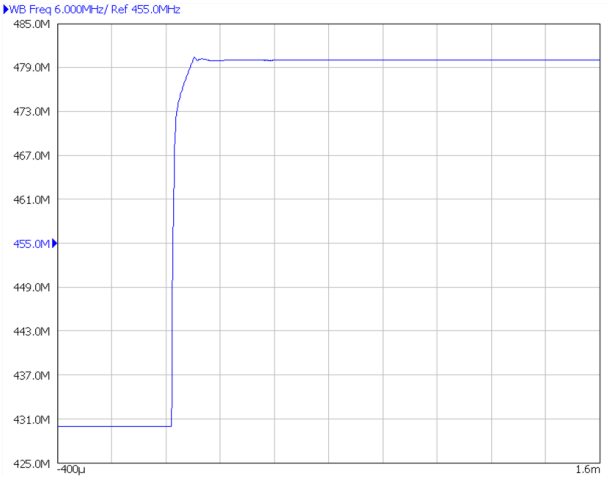


图 8-24. F1 to F2 Switching

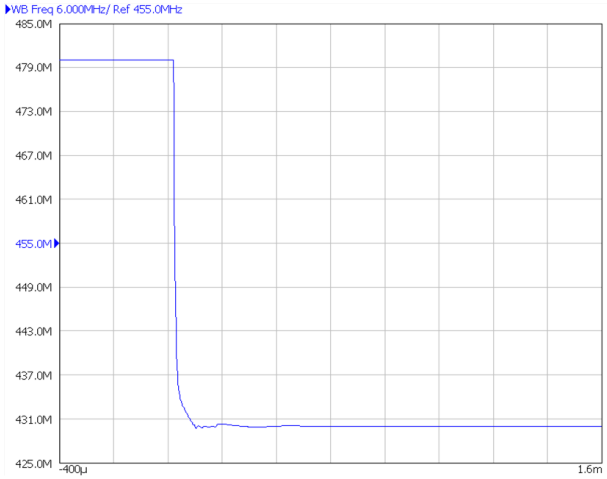


图 8-25. F2 to F1 Switching

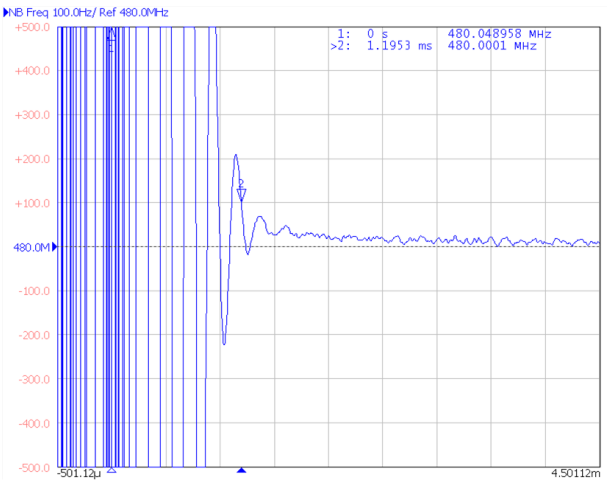


图 8-26. F1 to F2 Switching Time

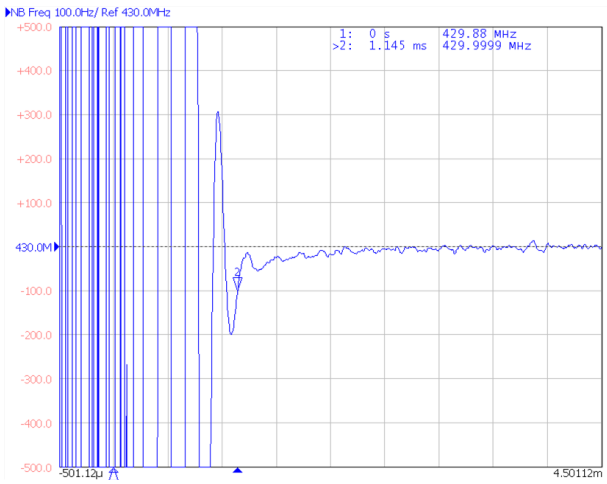


图 8-27. F2 to F1 Switching Time

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8.2.3 Synthesizer/PLL Duplex Mode

This example will demonstrate the device's capability in switching two frequencies using internal and external VCO. VCO switching is toggled by F1F2_SEL bit. Direct digital FSK modulation is enabled in TX using FSK I2S mode.

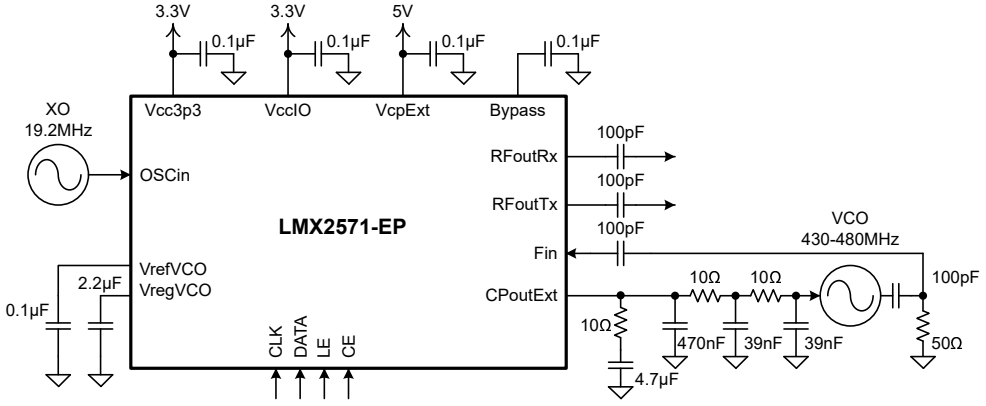


图 8-28. Typical Synthesizer/PLL Duplex Mode Application Schematic

8.2.3.1 Design Requirements

OSCin frequency = 19.2 MHz, LVCMOS
RFoutRX frequency = 440 MHz, external VCO = F1
RFoutTx frequency = 540 MHz, internal VCO = F2
Frequency switching time ⩽ 1.5 ms within 100-Hz frequency tolerance
Arbitrary FSK modulation to simulate analog FM modulation (10 times and 20 times over-sampling rate)
FM modulation frequency = 1 kHz
Frequency deviation = ±2000 Hz
Spurs ⩽ –72 dBc

8.2.3.2 Detailed Design Procedure

Frequency plans in TX and RX paths are as follows:

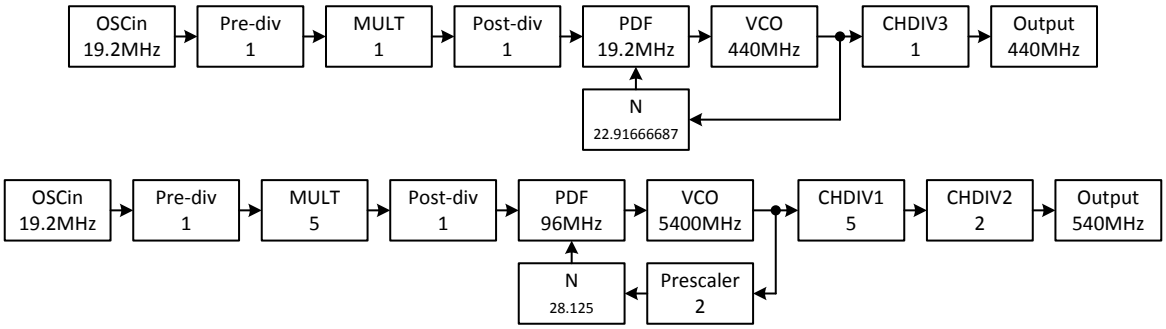


图 8-29. TX and RX Frequency Plans

Follow the previous examples to determine all the necessary configurations. To enable FSK I2S mode, set

FSK_MODE_SEL1=1
FSK_MODE_SEL=0
FSK_EN_F2=1

8.2.3.3 Synthesizer/PLL Duplex Mode Application Curves

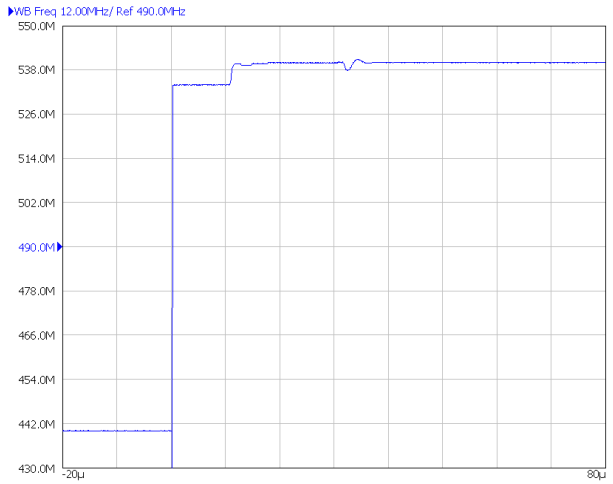


图 8-30. External VCO to Internal VCO Switching

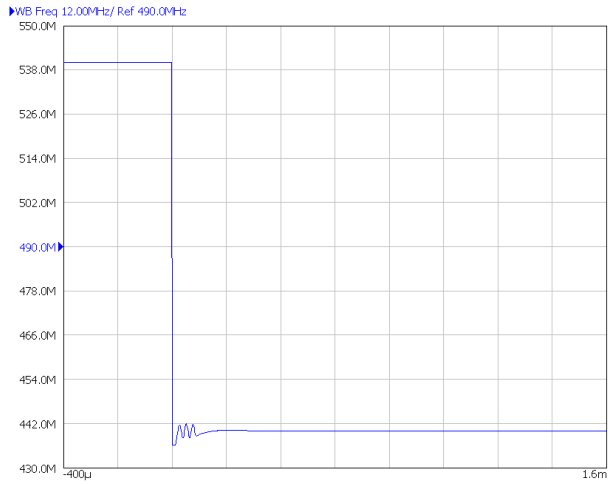


图 8-31. Internal VCO to External VCO Switching

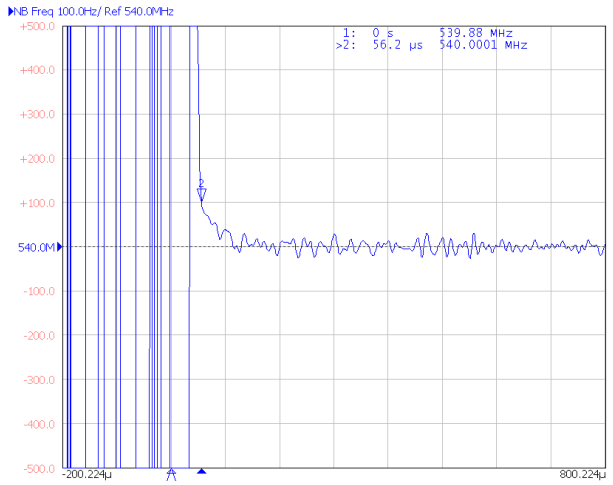


图 8-32. External VCO to Internal VCO Switching Time

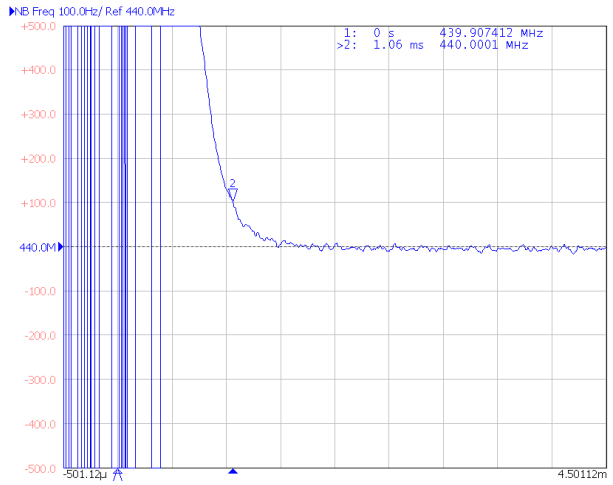


图 8-33. Internal VCO to External VCO Switching Time

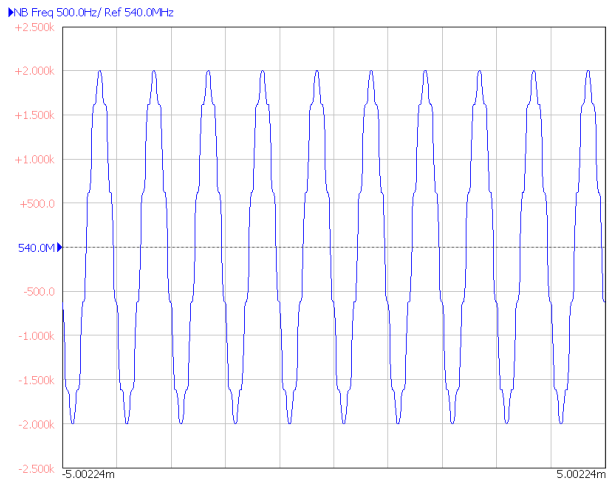


图 8-34. Simulated FM Modulation (10 Times Over-Sampling)

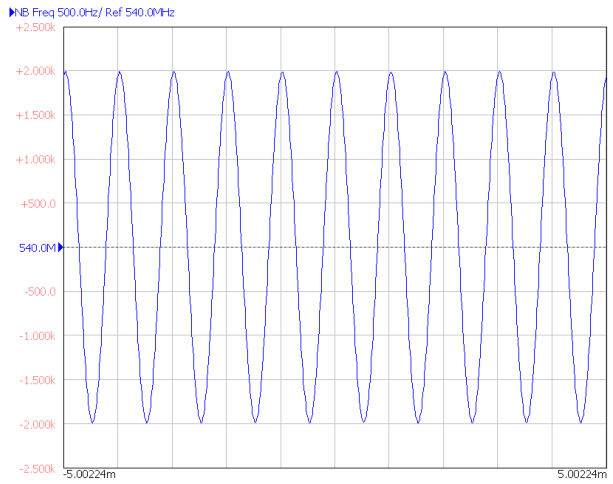


图 8-35. Simulated FM Modulation (20 Times Over-Sampling)

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8.3 Do's and Don'ts

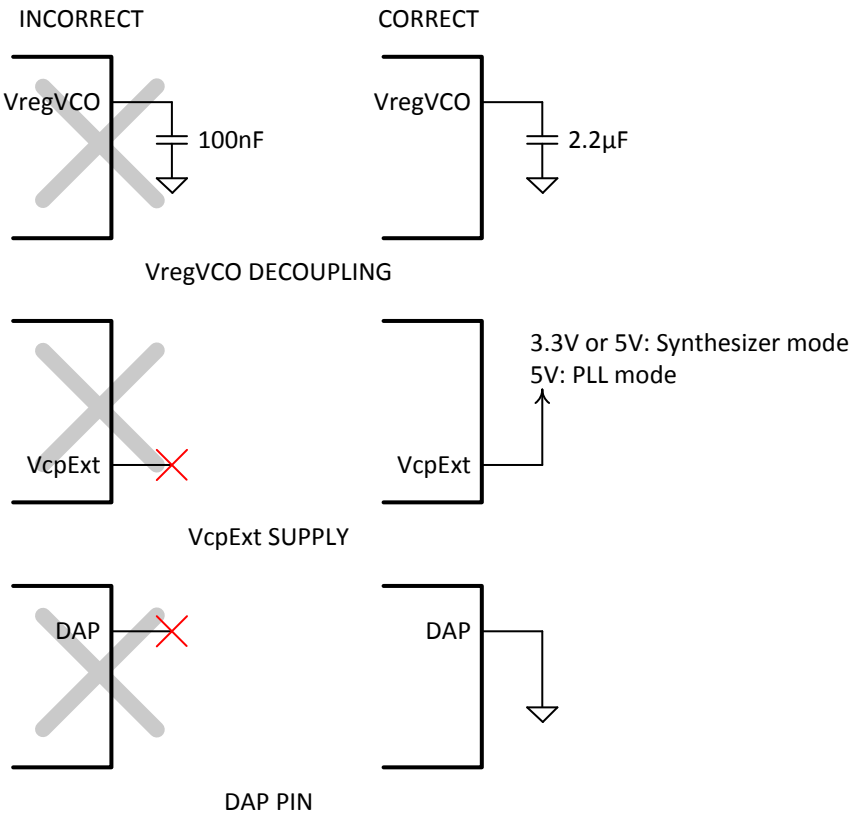


图 8-36. Do's and Don'ts

9 Power Supply Recommendations

TI recommends placing a 100-nF capacitor close to each of the power supply pins. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins may reduce spurs to a small degree.

VcpExt is the power supply pin for the 5-V charge pump. In PLL mode, the 5-V charge pump is active and a 5 V is required at VcpExt pin. **In synthesizer mode, although the 5-V charge pump is not active, either a 3.3-V or 5-V supply is still needed at this pin.**

Because LMX2571-EP has integrated LDOs, the requirement to external power supply is relaxed. In addition to LDO, LMX2571-EP is able to operate with DC-DC converter. The switching noise from the DC-DC converter would not affect performance of the LMX2571-EP. 表 9-1 lists some of the suggested DC-DC converters.

表 9-1. Recommended DC-DC Converters

PART NUMBER	TOPOLOGY	V_{IN}	V_{OUT}	I_{OUT}	SWITCHING FREQUENCY
TPS560200	Buck	4.5 V to 17 V	0.8 V to 6.5 V	500 mA	600 kHz
TPS62050	Buck	2.7 V to 10 V	0.7 V to 6 V	800 mA	1 MHz
TPS62160	Buck	3 V to 17 V	0.9 V to 6 V	1000 mA	2.25 MHz
TPS562200	Buck	4.5 V to 17 V	0.76 V to 7 V	2000 mA	650 kHz
TPS63050	Buck Boost	2.5 V to 5.5 V	2.5 V to 5.5 V	500 mA to 1 A	2.5 MHz

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10 Layout

10.1 Layout Guidelines

See *EVM instructions* (SNAU182) for details. In general, the layout guidelines are similar to most other PLL devices. The followings are some guidelines specific to the device.

- It may be beneficial to separate main ground and OSCin ground, crosstalk spurs might be reduced.
- Don't route any traces that carry switching signal close to the charge pump traces and external VCO.
- When using FSK I2S mode on this device, take care to avoid coupling between the I2S clock and any of the PLL circuit.

10.2 Layout Example

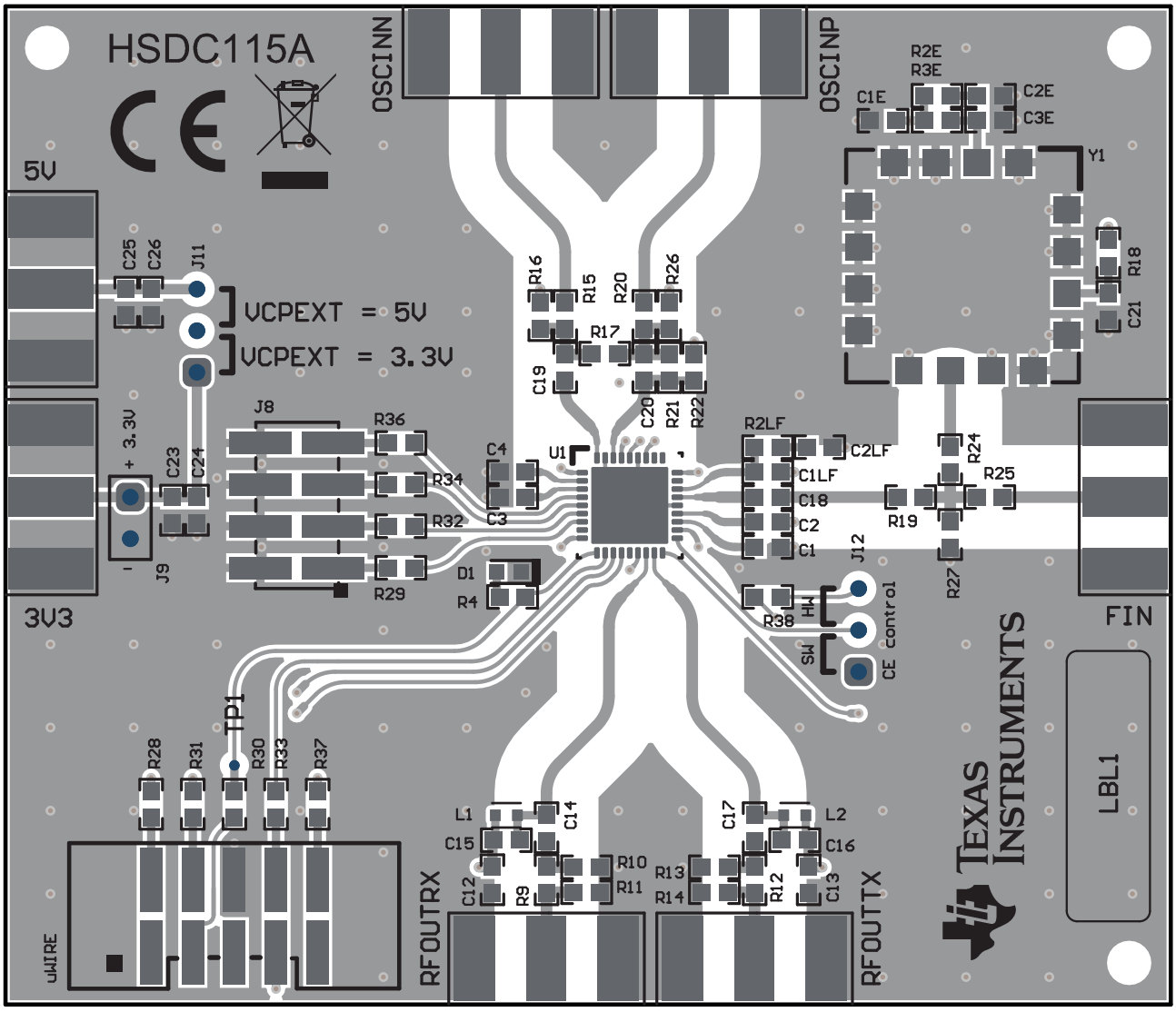


图 10-1. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

Texas Instruments has three main tools to assist with this product. The Clock Tree Architect assists as a solution finder, the PLLatinum Sim tool is used to design and simulate the loop filter (including filter design, bode plot, phase noise, spurs, and lock time), and the TICS Pro software is used to program the device. All these tools are available at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TS5A21366 0.75-Ω Dual SPST Analog Switch With 1.8-V Compatible Input Logic* data sheet
- Texas Instruments, *TPS560200 4.5-V to 17-V Input, 500-mA Synchronous Step-Down SWIFT™ Converter* data sheet
- Texas Instruments, *TPS62050 800-mA Synchronous Step-Down Converter* data sheet
- Texas Instruments, *TPS62160 3-V to 17-V, 1-A Step-Down Converters With DCS-Control* data sheet
- Texas Instruments, *TPS562200 4.5-V to 17-V Input, 2-A Synchronous Step-Down Voltage Regulator in SOT-23* data sheet
- Texas Instruments, *TPS63050 Tiny Single Inductor Buck Boost Converter* data sheet

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMX2571SRHHTEP	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	LMX2571 EP
LMX2571SRHHTEP.A	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	LMX2571 EP
V62/21613-01XE	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	LMX2571 EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LMX2571-EP :

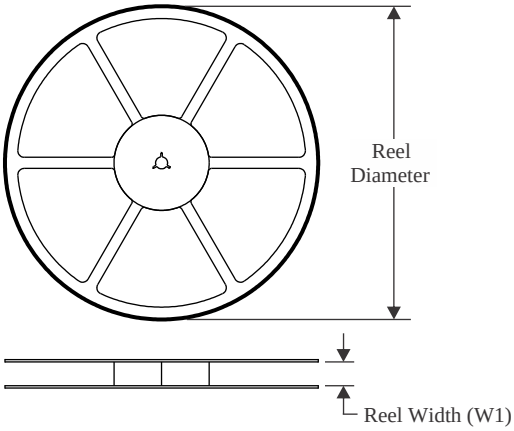
- Catalog : LMX2571

NOTE: Qualified Version Definitions:

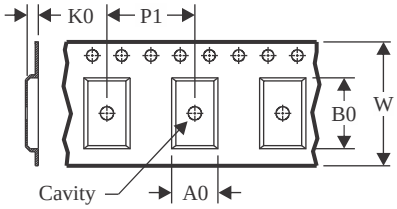
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

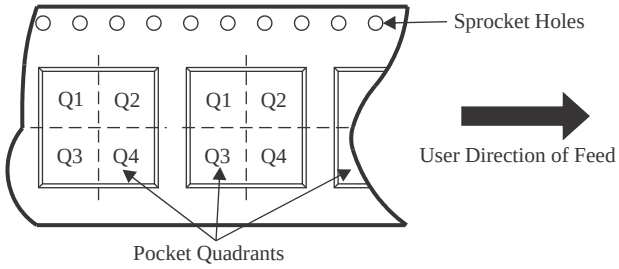


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

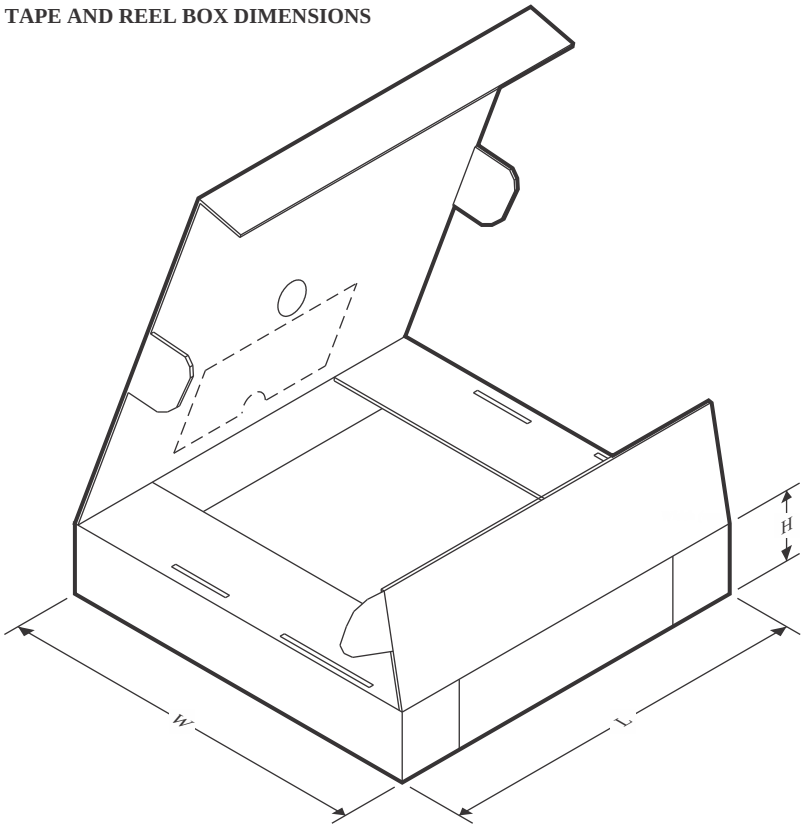
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2571SRHHTEP	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2571SRHHTEP	VQFN	RHH	36	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

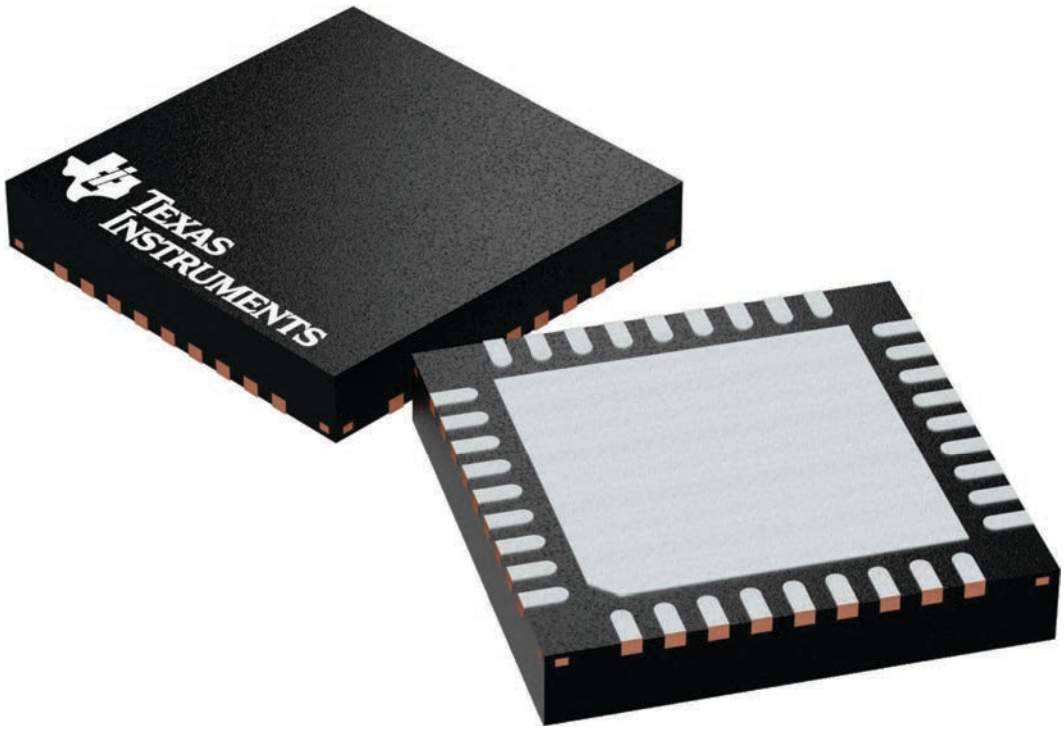
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



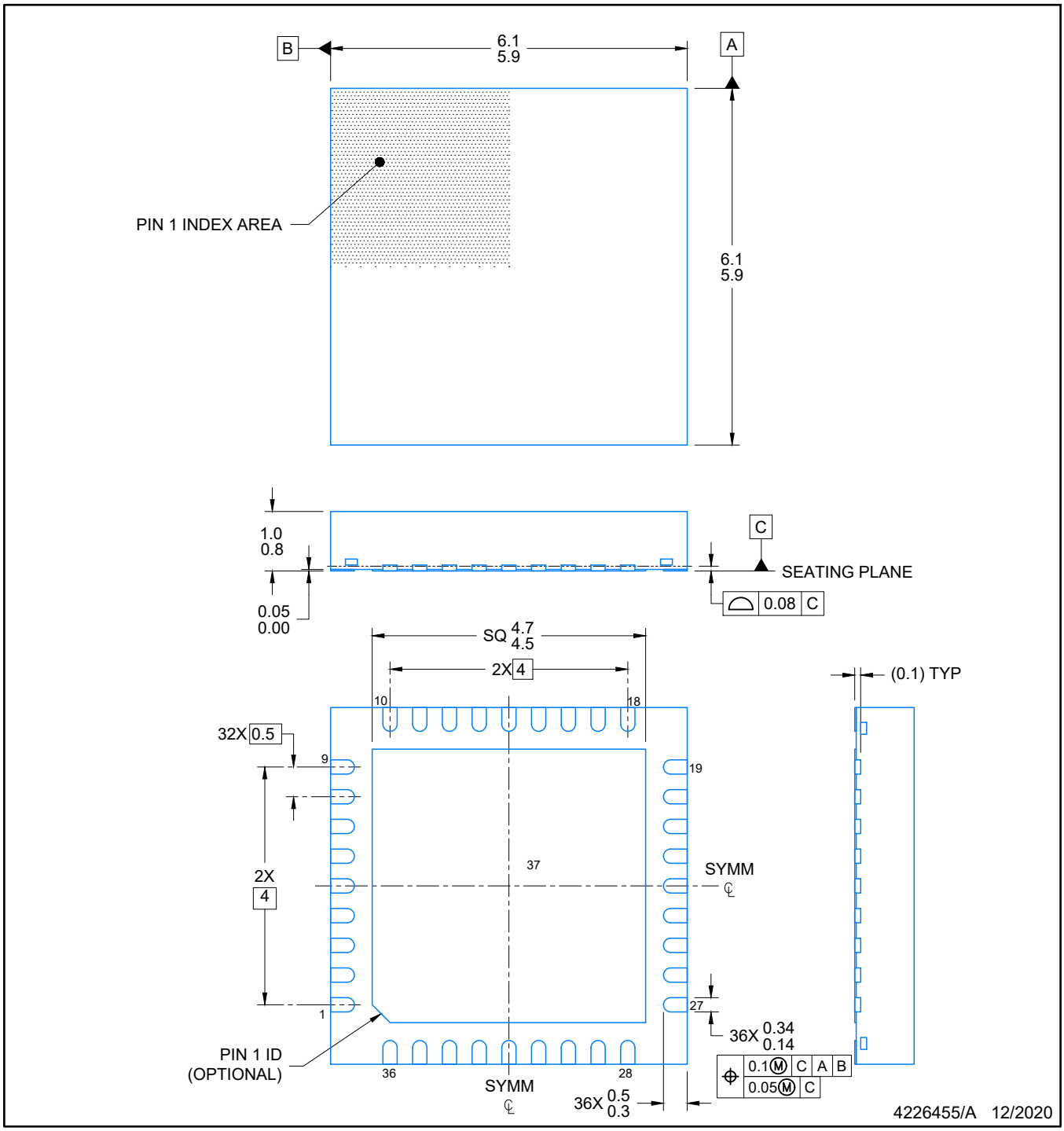
4225440/A

PACKAGE OUTLINE

RHH0036G

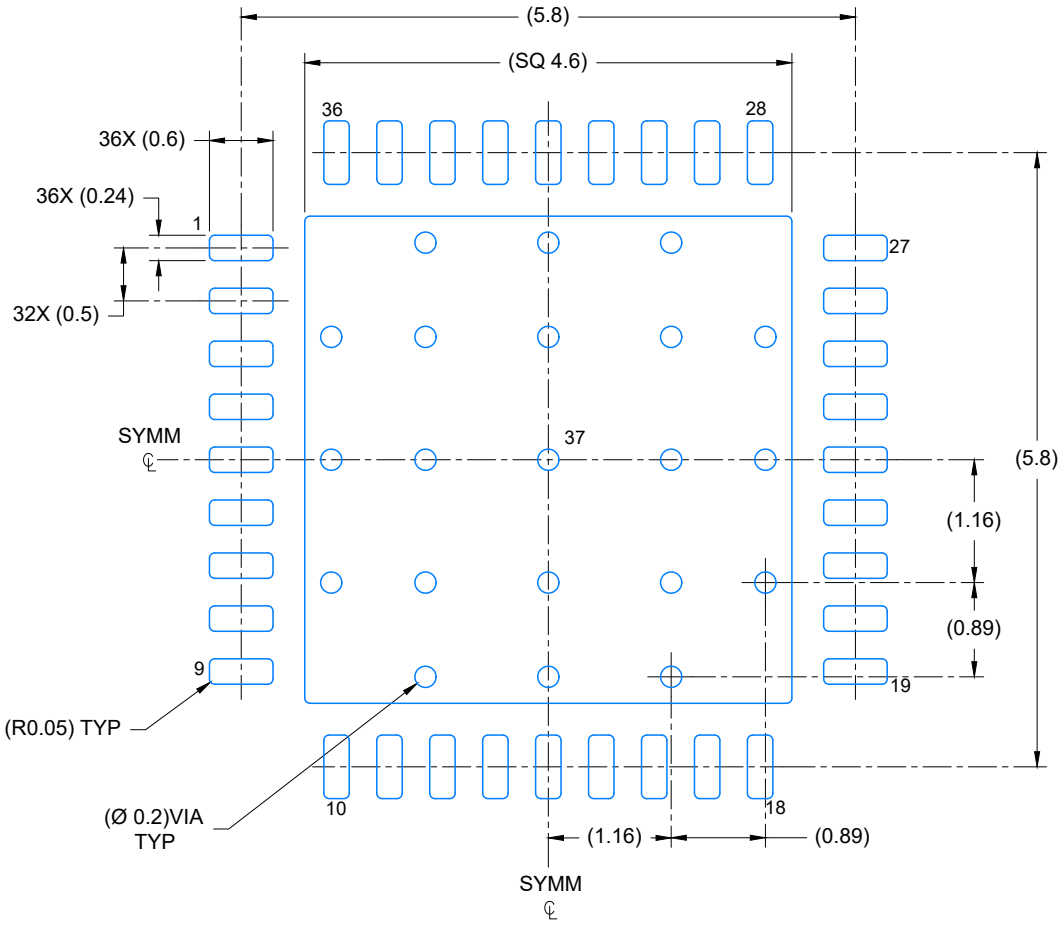
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

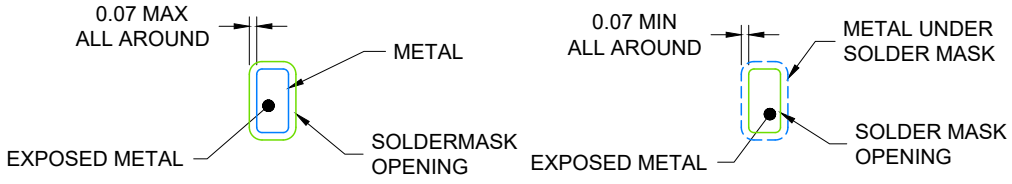


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 14X



NON- SOLDER MASK DEFINED (PREFERRED)

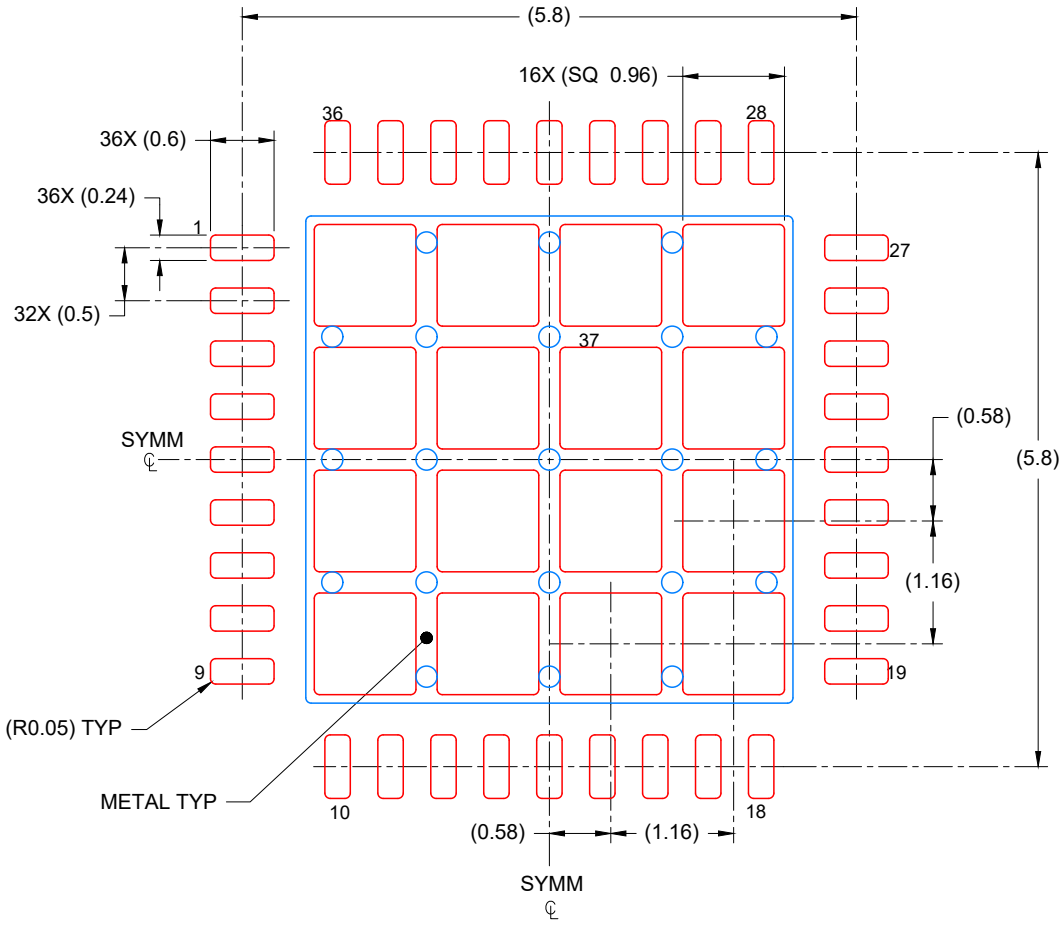
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4226455/A 12/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED COVERAGE BY AREA
SCALE: 14X

4226455/A 12/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月