LMH6702QML-SP 1.7GHz、超低失真、宽带运算放大器

1 特性

- V_S = ±5V，T_A = 25°C，A_V = +2V/V，R_L = 100Ω，V_{OUT} = $2V_{PP}$（典型值，除非另有说明）
- 具有辐射保证
  - 高剂量率 300krad(Si)
  - 在 300krad(Si) 条件下无 ELDRS
- −3dB 带宽 (V_{OUT} = $0.2V_{PP}$)：720MHz
- 低噪声：1.83nV/√Hz
- 快速稳定至 0.1% 的时间：13.4ns
- 快速压摆率：3100V/μs
- 电源电流：12.5mA
- 输出电流：80mA
- 低互调失真 (75MHz)：−67dBc
- 经改进可替代 CLC409 和 CLC449

2 应用

- Flash A/D 驱动器
- D/A 跨阻缓冲器
- 宽动态范围中频放大器
- 雷达和通信接收器
- 线路驱动器
- 高分辨率视频

3 说明

LMH6702QML-SP 是一款超宽带、直流耦合、单片运算放大器，专为需要出色信号保真度的宽动态范围系统而设计。得益于采用 TI 的电流反馈架构，LMH6702QML-SP 可以出色的速度提供单位增益稳定性，无需外部补偿。

LMH6702QML-SP 具有 720MHz 带宽（A_V = 2V/V，V_O = $2V_{PP}$）、60MHz 范围内的 10 位失真水平 (R_L = 100Ω)、1.83nV/√Hz 输入基准噪声和 12.5mA 电源电流，是适用于高速 Flash 模数 (A/D) 和数模 (D/A) 转换器的出色驱动器或缓冲器。

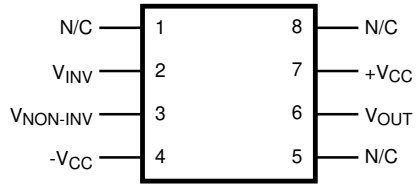
LMH6702QML-SP 对于需要宽带放大器提供出色信号纯度的宽动态范围系统（例如雷达和通信接收器）颇有益处。低输入基准噪声以及低谐波和互调失真使得该器件非常适合高速应用。

LMH6702QML-SP 采用 TI 的 VIP10 互补双极工艺和 TI 成熟的电流反馈架构构建而成。

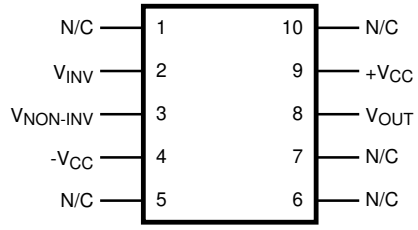
封装信息

器件型号	封装(1)	封装尺寸(2)
LMH6702QML-SP	NAB（CDIP，8）	10.16mm × 7.87mm
	NAC（CFP，10）	9.91mm × 6.45mm

(1) 有关更多信息，请参阅节 9。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



NAB 封装，8 引脚 CDIP（顶视图）



NAC 封装，10 引脚 CLGA（顶视图）

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

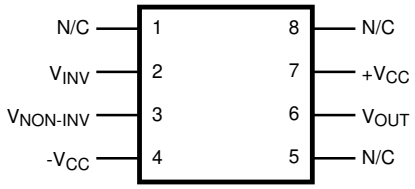


图 4-1. NAB Package, 8-Pin CDIP (Top View)

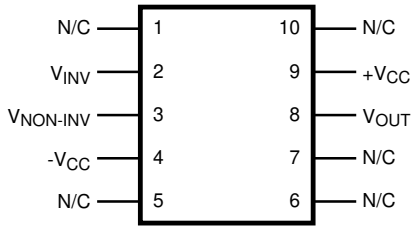


图 4-2. NAC Package, 10-Pin CLGA (Top View)

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	VALUE
Supply voltage (V_{CC})	±6.75V_{DC}
Common-mode input voltage (V_{CM})	V^- to V^+
Power dissipation (P_D) (2)	1W
Junction temperature (T_J)	175°C
Lead temperature (soldering, 10 seconds)	300°C
Storage temperature	−65°C ≤ T_A ≤ +150°C
Thermal resistance	
θ_{JA}	
CDIP (still air)	170°C/W
CDIP (500LF/min air flow)	100°C/W
CLGA (still air)	220°C/W
CLGA (500LF/min air flow)	150°C/W
θ_{JC}	
CDIP	35°C/W
CLGA	37°C/W
Package weight (typical)	
CDIP	1078mg
CLGA	227mg
ESD tolerance (3)	1000V

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower.

(3) Human body model, 1.5kΩ in series with 100pF.

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5.2 Recommended Operating Conditions

	VALUE
Supply voltage (V_{CC})	±5V_{DC} to ±6V_{DC}
Gain	±1 to ±10
Ambient operating temperature (T_A)	– 55°C to +125°C

5.3 Quality Conformance Inspection

MIL-STD-883, Method 5005, Group A

SUBGROUP	DESCRIPTION	TEMPERATURE (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	– 55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	– 55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	– 55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	– 55

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5.4 Electrical Characteristics: DC Parameters

The following conditions apply (unless otherwise specified)(1) (2):
R_L = 100Ω, V_{CC} = ±5V_{DC}, A_V = +2 feedback resistor (R_F) = 250Ω, gain resistor (R_G) = 250Ω

PARAMETER		TEST CONDITIONS	NOTES	MIN	MAX	UNIT	SUB-GROUPS
I_{BN}	Input bias current, noninverting			– 15	15	µA	1, 2
				– 21	21	µA	3
I_{BI}	Input bias current, inverting			– 30	30	µA	1, 2
				– 34	34	µA	3
V_{IO}	Input offset voltage			– 4.5	4.5	mV	1, 3
				– 6.0	6.0	mV	2
I_{CC}	Supply current, no load	R_L = ∞			15	mA	1, 2, 3
PSSR	Power supply rejection ratio	– V_{CC} = – 4.5V to – 5.0V, +V_{CC} = 4.5V to 5.0V		45		dB	1, 2, 3

(1) The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
(2) Pre- and post-irradiation limits are identical to those listed under the dc parameter tables. Post-irradiation testing is conducted at room temperature, 25°C, only. Testing is performed as specified in MIL-STD-883 Test Method 1019 Condition A. The ELDRS-Free part is also tested per Test Method 1019 Conditions D.

5.5 Electrical Characteristics: AC Parameters

The following conditions apply (unless otherwise specified)(1) (2):
R_L = 100Ω, V_{CC} = ±5V_{DC}, A_V = +2 feedback resistor (R_F) = 250Ω, gain resistor (R_G) = 250Ω

PARAMETER		TEST CONDITIONS	NOTES	MIN	MAX	UNIT	SUB-GROUPS
HD_3	3rd harmonic distortion	2V_{PP} at 20MHz			– 62	dBc	4
GFPL	Gain flatness peaking	0.1MHz to 75MHz, V_O < 0.5V_{PP}			0.4	dB	4
GFPH	Gain flatness peaking	> 75MHz, V_O < 0.5V_{PP}			2.0	dB	4
GFRH	Gain flatness rolloff	75MHz to 125MHz, V_O < 0.5V_{PP}			0.2	dB	4
HD_2	2nd harmonic distortion	2V_{PP} at 20MHz			– 52	dBc	4

(1) The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
(2) These parameters are not post irradiation tested.

5.6 Electrical Characteristics: Drift Values Parameters

The following conditions apply (unless otherwise specified)(1):
R_L = 100Ω, V_{CC} = ±5V_{DC}, A_V = +2 feedback resistor (R_F) = 250Ω, gain resistor (R_G) = 250Ω
Delta not required on B level product. Delta required for S-level product at Group B5 only, or as specified on the internal processing instruction (IPI).

PARAMETER		TEST CONDITIONS	PACKAGE	MIN	MAX	UNIT	SUB-GROUPS
I_{BN}	Input bias current noninverting		NAB	– 0.3	0.3	µA	1
			NAC	– 0.75	0.75		
I_{BI}	Input bias current inverting			– 3.0	3.0	µA	1
V_{IO}	Input offset voltage		NAB	– 0.3	0.3	mV	1
			NAC	– 1.0	1.0		

(1) The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

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5.7 Typical Characteristics

at T_A = 25°C, V_S = ±5V, R_L = 100Ω, and R_F = 237Ω (unless otherwise noted)

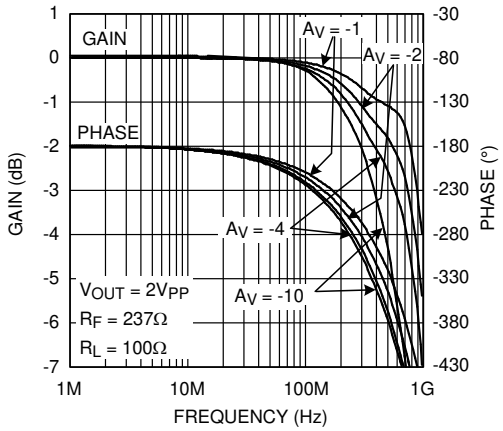


图 5-1. Inverting Frequency Response

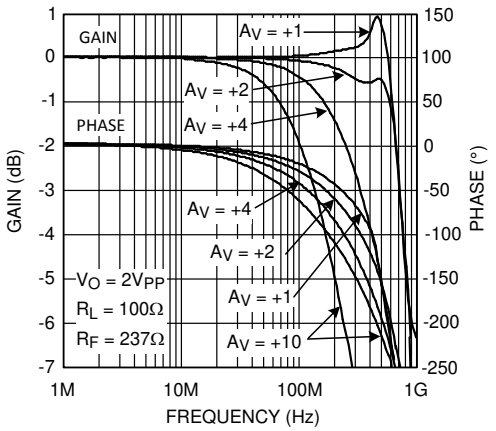


图 5-2. Noninverting Frequency Response

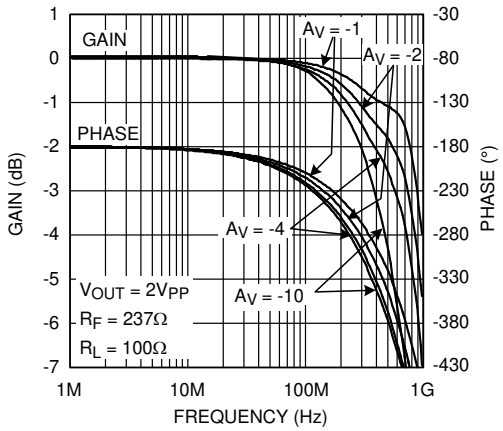


图 5-3. Inverting Frequency Response

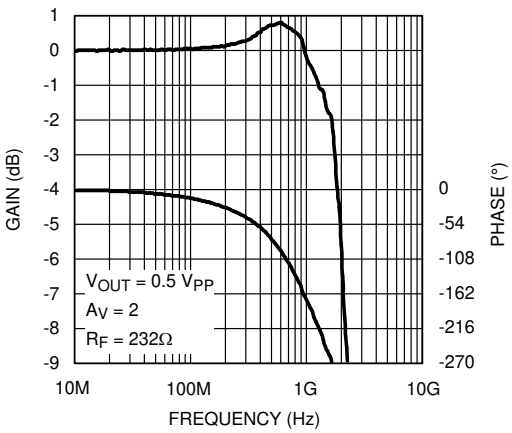


图 5-4. Small-Signal Bandwidth

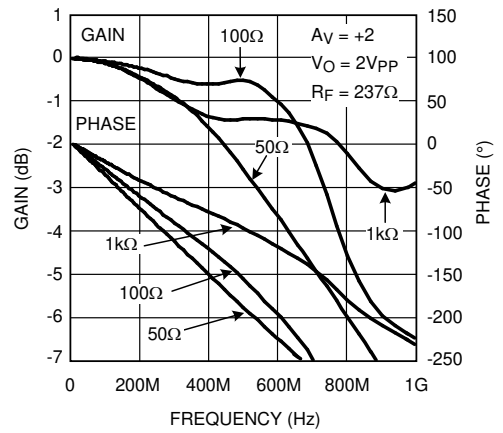


图 5-5. Frequency Response for Various R_L, A_V = +2

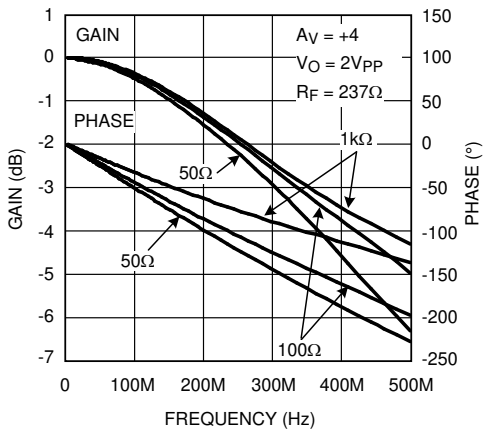


图 5-6. Frequency Response for Various R_L, A_V = +4

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5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±5V, R_L = 100Ω, and R_F = 237Ω (unless otherwise noted)

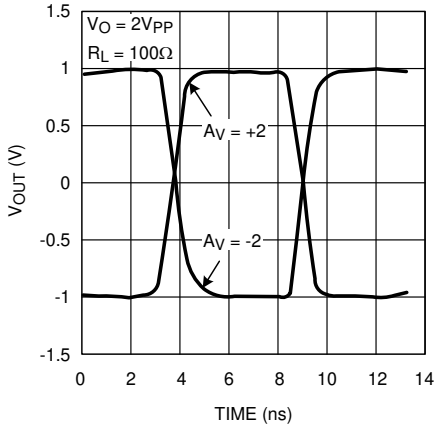


图 5-7. Step Response, $2V_{PP}$

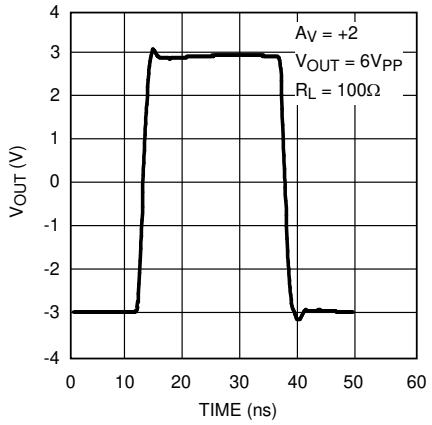


图 5-8. Step Response, $6V_{PP}$

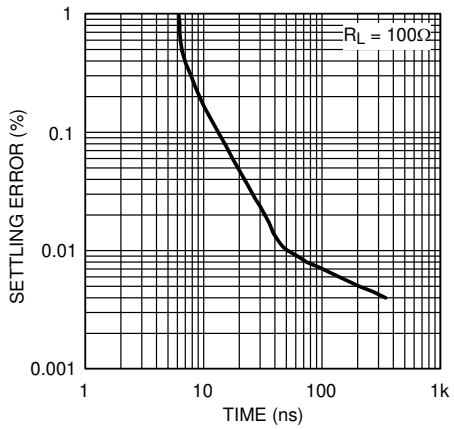


图 5-9. Percent Settling vs Time

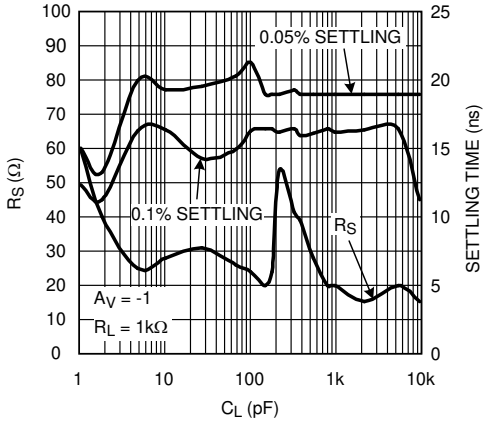


图 5-10. R_S and Settling Time vs C_L

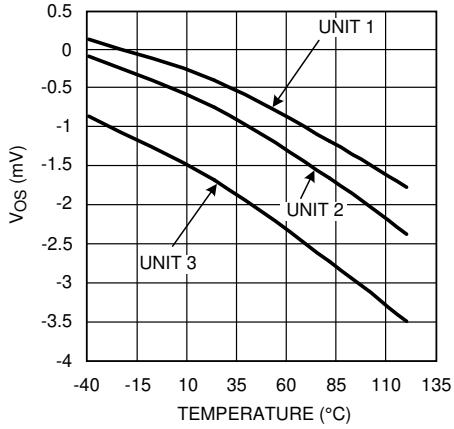


图 5-11. Input Offset for Three Representative Units

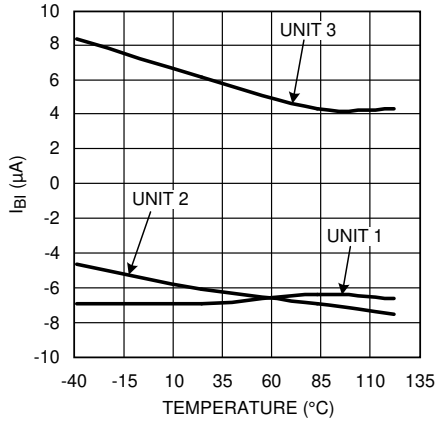


图 5-12. Inverting Input Bias for Three Representative Units

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5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±5V, R_L = 100Ω, and R_F = 237Ω (unless otherwise noted)

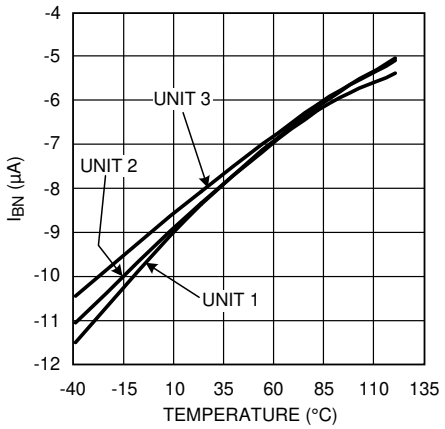


图 5-13. Noninverting Input Bias for Three Representative Units

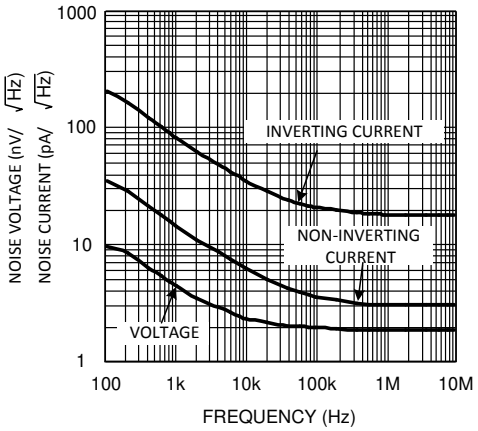


图 5-14. Noise

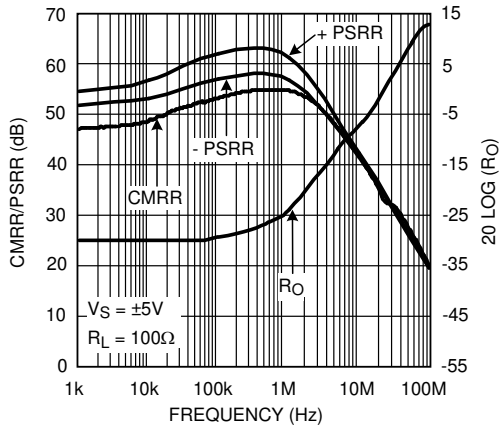


图 5-15. CMRR, PSRR, R_{OUT}

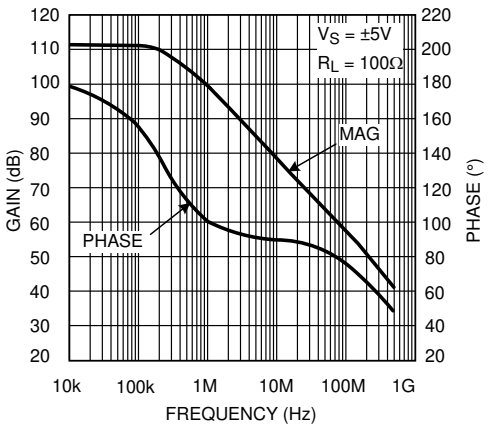


图 5-16. Transimpedance

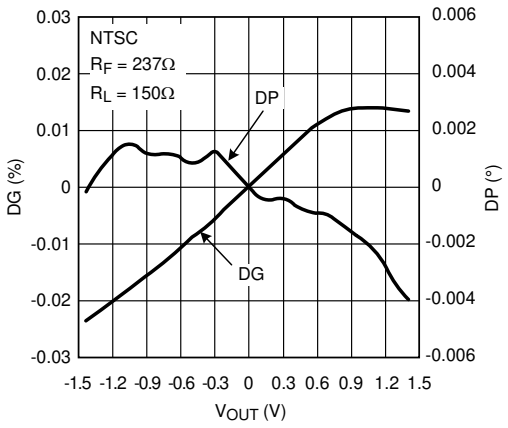


图 5-17. DG/DP (NTSC)

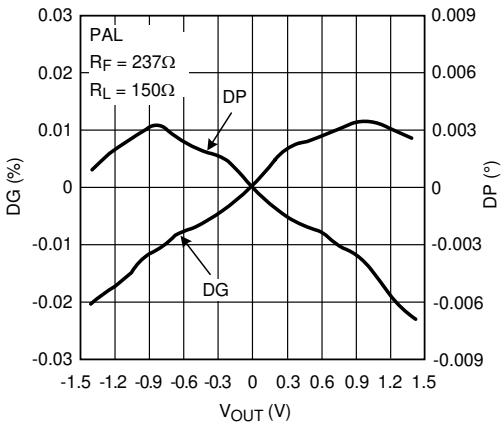


图 5-18. DG/DP (PAL)

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6 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

6.1 Application Information

6.1.1 Feedback Resistor

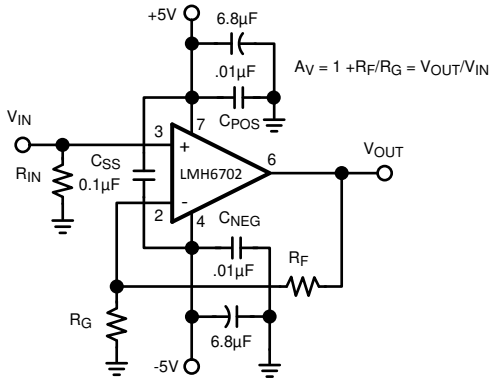


图 6-1. Recommended Noninverting Gain Circuit

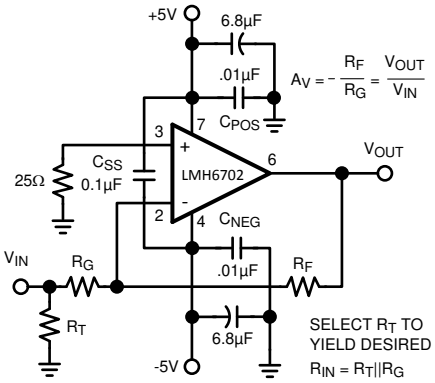


图 6-2. Recommended Inverting Gain Circuit

The LMH6702 achieves excellent pulse and distortion performance by using current feedback topology. The loop gain for a current-feedback op amp, and thus the frequency response, is predominantly set by the feedback-resistor value. The LMH6702 is optimized for use with a 237Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value limits the bandwidth. Application Note OA-13 SNOA366 discusses this configuration in detail along with the occasions where a different R_F can be advantageous.

6.1.2 Harmonic Distortion

The LMH6702 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high-speed flash ADCs, the distortions introduced by the converter dominate over the low LMH6702 distortions. Capacitor C_{SS}, shown across the supplies in 图 6-1 and 图 6-2, is critical to achieving the lowest 2nd harmonic distortion. For absolute minimum distortion levels, keep the supply decoupling currents (ground connections to C_{POS}, and C_{NEG} in 图 6-1

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and 图 6-2) separate from the ground connections to sensitive input circuitry (such as R_G, R_T, and R_{IN} ground connections). Splitting the ground plane in this manner, and separately routing the high frequency current spikes on the decoupling caps back to the power supply (similar to a *star connection* layout technique) provides minimum coupling back to the input circuitry and results in best harmonic distortion response (especially 2nd-order distortion).

If this layout technique has not been observed on a particular application board, the supply decoupling capacitors can adversely affect HD2 performance by increasing the coupling phenomenon already mentioned. 图 6-3 shows actual HD2 data on a board where the ground plane is shared between the supply decoupling capacitors and the rest of the circuit. After these capacitors are removed, the HD2 distortion levels reduce significantly, especially between 10MHz to 20MHz, as shown in 图 6-3.

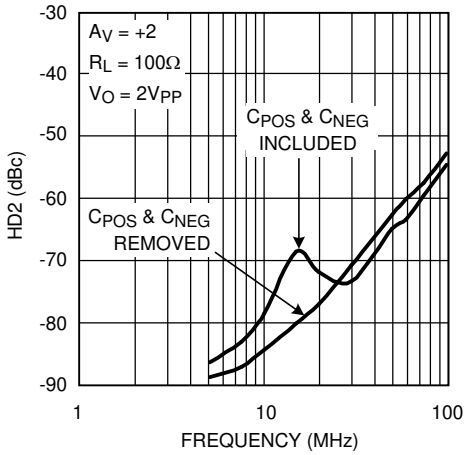


图 6-3. Decoupling Current Adverse Effect on a Board With Shared Ground Plane

At these extremely low distortion levels, the high-frequency behavior of decoupling capacitors themselves can be significant. In general, lower-value decoupling capacitors tend to have higher resonance frequencies, making lower-value decoupling capacitors more effective for higher-frequency regions. A particular application board that has been laid out correctly with ground returns split to minimize coupling benefits the most by having low-value and higher-value capacitors paralleled to take advantage of the effective bandwidth of each, and extend the low-distortion frequency range.

6.1.3 Capacitive Load Drive

图 6-4 shows a typical application using the LMH6702 to drive an ADC.

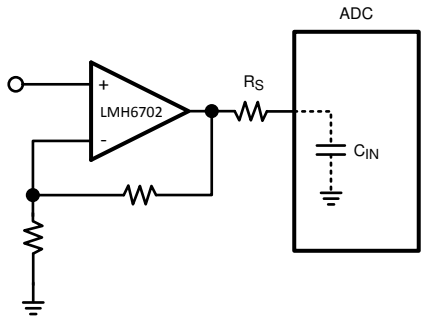


图 6-4. Input Amplifier to ADC

The series resistor, R_S, between the amplifier output and the ADC input is critical to achieving best system performance. This load capacitance, if applied directly to the output pin, can quickly lead to unacceptable levels of ringing in the pulse response. The plot of *R_S and Settling Time vs C_L* in the *Typical Characteristics* is an

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excellent starting point for selecting R_S. The value derived in that plot minimizes the step settling time into a fixed discrete capacitive load with the output driving a very light resistive load (1kΩ). Sensitivity to capacitive loading is greatly reduced after the output is loaded more heavily. Therefore, for cases where the output is heavily loaded, R_S value can be reduced. The exact value can best be determined experimentally for these cases.

In applications where the LMH6702 is replacing the CLC409, take care when the device is lightly loaded and some capacitance is present at the output. As a result of the much higher frequency response of the LMH6702 compared to the CLC409, increased susceptibility to low value output capacitance (parasitic or inherent to the board layout or otherwise being part of the output load) is possible. As previously mentioned, this susceptibility is most noticeable when the LMH6702 resistive load is light. Parasitic capacitance can be minimized by careful layout. Addition of an output snubber R-C network also helps by increasing the high-frequency resistive loading.

Referring back to 图 6-4, consider several additional constraints in driving the capacitive input of an ADC. There is an option to increase R_S, band-limiting at the ADC input for either noise or Nyquist band-limiting purposes. However, increasing R_S too much can induce an unacceptably large input glitch due to switching transients coupling through from the convert signal. Also, C_{IN} is often a voltage-dependent capacitance. This input impedance nonlinearity induces distortion terms that increase as R_S is increased. Therefore, attempt only slight adjustments up or down from the recommended R_S value in optimizing system performance.

6.1.4 DC Accuracy and Noise

Example below shows the output offset computation equation for the noninverting configuration using the typical bias current and offset specifications for A_V = +2:

Output Offset: $V_O = (\pm I_{BN} \times R_{IN} \pm V_{IO}) (1 + R_F/R_G) \pm I_{BI} \times R_F$

Where R_{IN} is the equivalent input impedance on the noninverting input.

Example computation for A_V = +2, R_F = 237Ω, R_{IN} = 25Ω:

$V_O = (\pm 6\ \mu A \times 25\Omega \pm 1mV) (1 + 237/237) \pm 8\ \mu A \times 237 = \pm 4.20mV$

A good design, however, includes a worst-case calculation using minimum and maximum numbers in the data sheet tables to provide worst-case operation.

Further improvement in the output offset voltage and drift is possible using composite amplifiers. The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. Therefore, to cancel the effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices) is not possible.

The total output noise is computed in a similar fashion to the output offset voltage. Using the input noise voltage and the two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See the *OA-12 Noise Analysis for Comlinear Amplifiers* application report for a full discussion of noise calculations for current-feedback amplifiers.

6.2 Layout

6.2.1 Layout Guidelines

Generally, a good high frequency layout keeps power supply and ground traces away from the inverting input and output pins. Parasitic capacitance on these nodes to ground cause frequency-response peaking and possible circuit oscillations (see the *OA-15 Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers* application report for more information). Texas Instruments suggests the following evaluation boards as a guide for high-frequency layout and as an aid in device testing and characterization:

DEVICE	PACKAGE	EVALUATION BOARD PART NUMBER
LMH6702QMLMF	SOT-23-5	CLC730216
LMH6702QMLMA	Plastic SOIC	CLC730227

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7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (March 2013) to Revision F (August 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Changed input bias current noninverting limits from ±0.3 µA to ±0.75 µA for NAC package type in *LMH6702 Electrical Characteristics Drift Values Parameters*	5
• Changed input offset voltage limits from ±0.3mA to ±1mV for NAC package type in *LMH6702 Electrical Characteristics Drift Values Parameters*	5

Changes from Revision D (October 2011) to Revision E (March 2013)	Page
• 将美国国家半导体数据表的布局更改为 TI 格式	1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-0254601VPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702J-QV 5962-02546 01VPA Q ACO 01VPA Q >T
5962-0254601VZA	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702 WGQMLV Q 5962-02546 01VZA ACO 01VZA >T
5962F0254601VPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702JFQV 5962F02546 01VPA Q ACO 01VPA Q >T
5962F0254601VZA	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702 WGFQMLV Q 5962F02546 01VZA ACO 01VZA >T
5962F0254602VPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702JFLQV 5962F02546 02VPA Q ACO 02VPA Q >T
LMH6702J-QMLV	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702J-QV 5962-02546 01VPA Q ACO 01VPA Q >T
LMH6702J-QMLV.A	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702J-QV 5962-02546 01VPA Q ACO 01VPA Q >T
LMH6702JFLQMLV	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702JFLQV 5962F02546 02VPA Q ACO 02VPA Q >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6702JFQMLV	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702JFQV 5962F02546 01VPA Q ACO 01VPA Q >T
LMH6702JFQMLV.A	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702JFQV 5962F02546 01VPA Q ACO 01VPA Q >T
LMH6702WG-QMLV	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702 WGQMLV Q 5962-02546 01VZA ACO 01VZA >T
LMH6702WG-QMLV.A	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702 WGQMLV Q 5962-02546 01VZA ACO 01VZA >T
LMH6702WGFQMLV	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702 WGFQMLV Q 5962F02546 01VZA ACO 01VZA >T
LMH6702WGFQMLV.A	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMH6702 WGFQMLV Q 5962F02546 01VZA ACO 01VZA >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

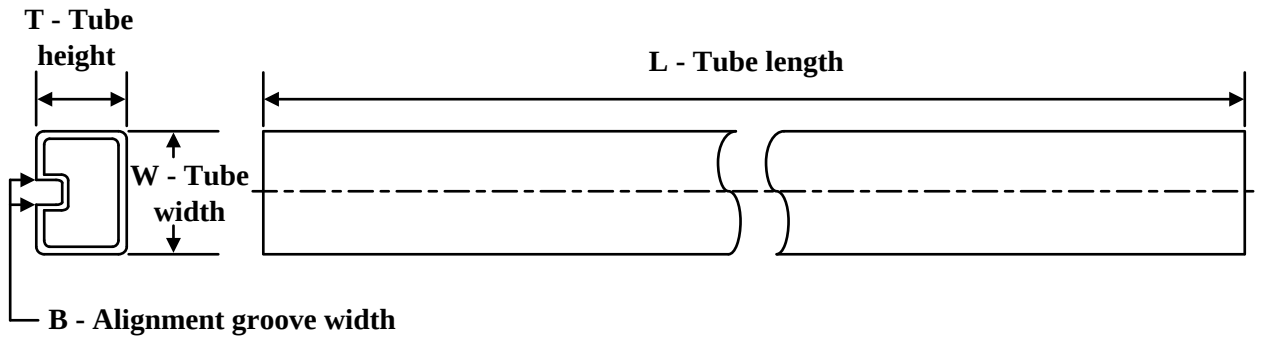
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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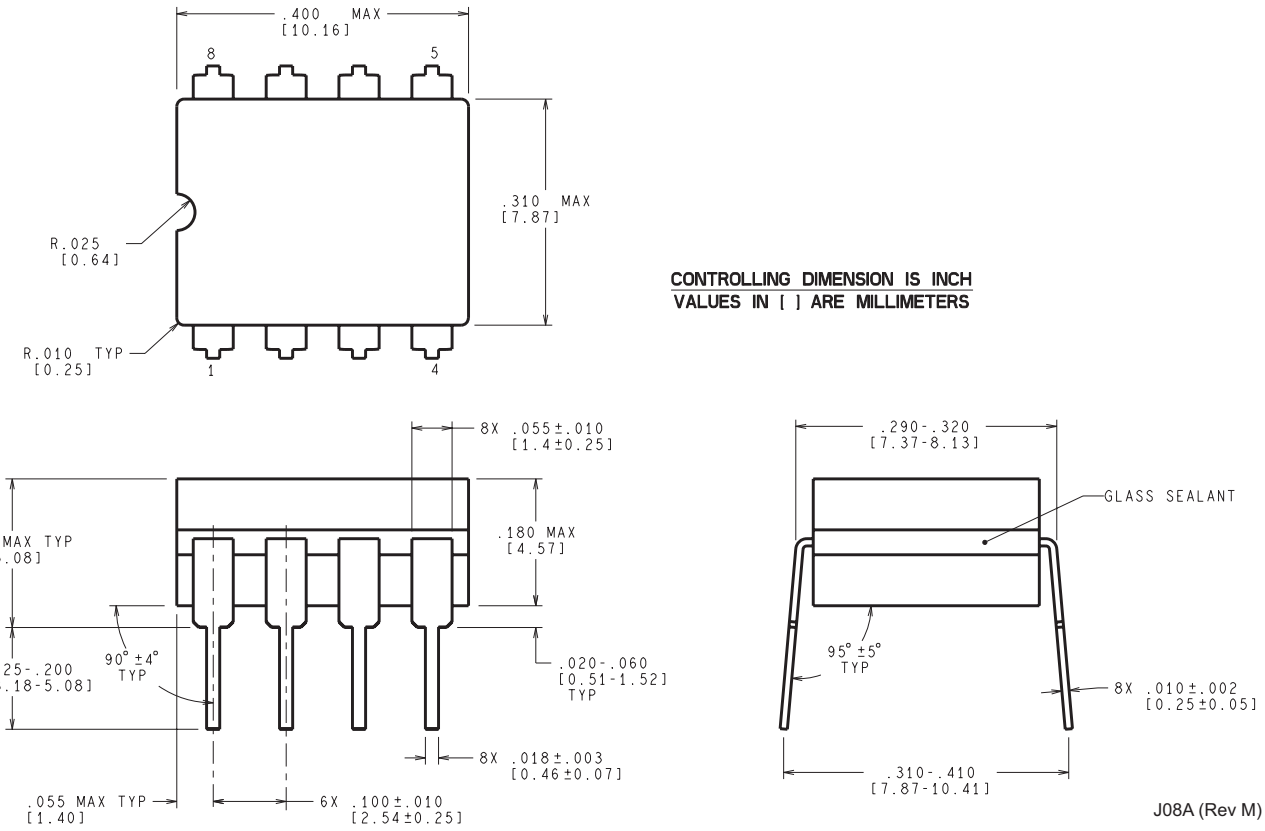
TUBE

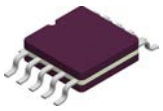


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-0254601VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
5962F0254601VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
LMH6702J-QMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA
LMH6702J-QMLV.A	NAB	CDIP	8	40	506.98	15.24	13440	NA
LMH6702JFQMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA
LMH6702JFQMLV.A	NAB	CDIP	8	40	506.98	15.24	13440	NA

NAB0008A


.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

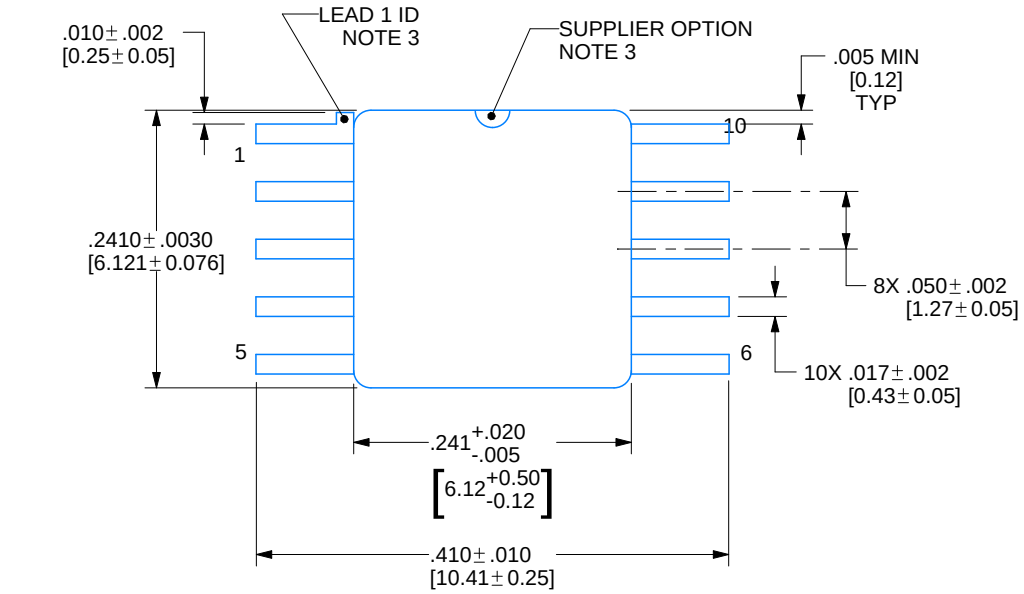


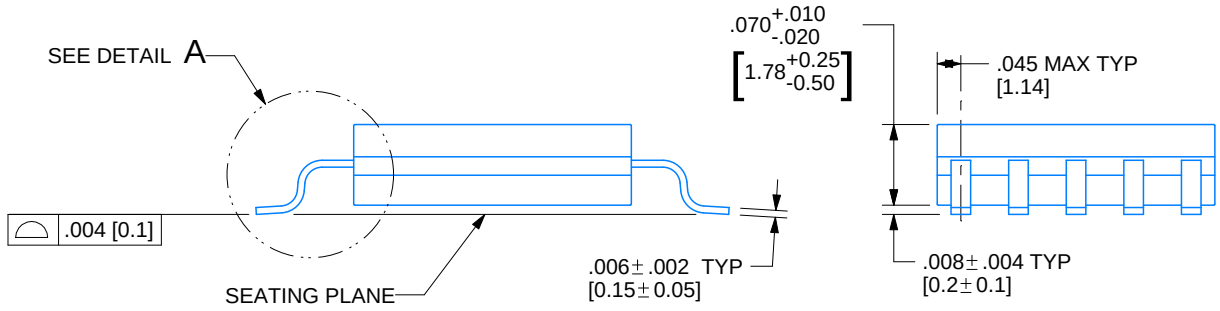
PACKAGE OUTLINE

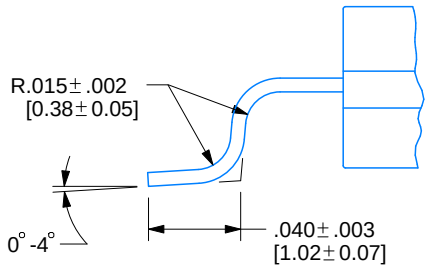
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK







DETAIL A
TYPICAL

4215196/D 08/2022

NOTES:

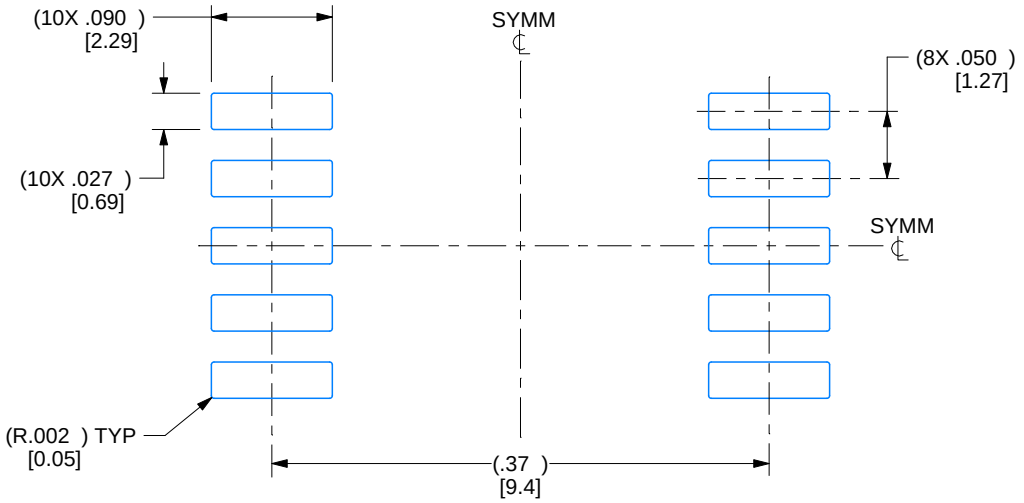
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

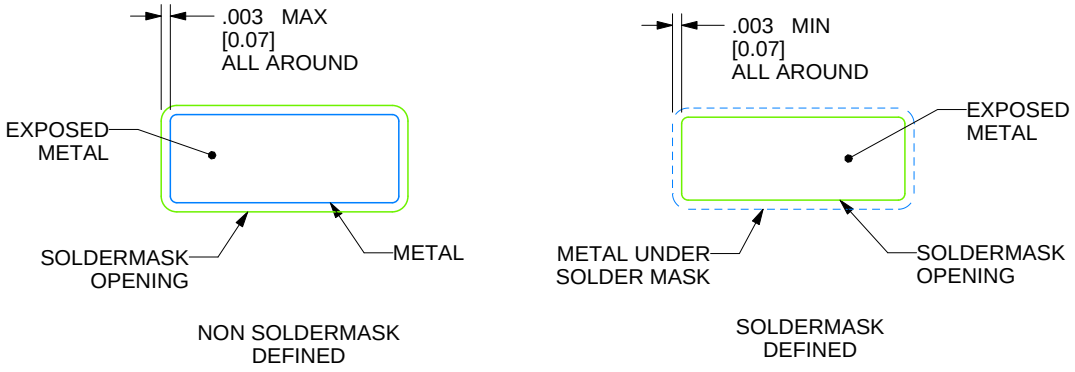
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



4215196/D 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197877	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198820	02/14/2022	K. SINCERBOX
C	CHANGE PIN 1 ID LOCATION ON PIN	2198845	02/18/2022	D. CHIN / K. SINCERBOX
D	.2410± .0030 WAS .2700 +.0012/-.0002;	2200915	08/08/2022	D. CHIN / K. SINCERBOX

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最后更新日期：2025 年 10 月