# LMG210xR0xx 100V GaN 半桥功率级，集成保护功能和智能开关特性

ADVANCE INFORMATION

## 1 特性

- 集成驱动器的 GaN 半桥功率级 100V（GaN FET 选项：2.2mΩ 和 4.4mΩ）
- 高效率、高密度的功率转换
  - 超低传播延迟 (20ns) 和匹配 (2ns)
  - 两个 GaN FET 的导通和关断压摆率可独立控制
  - 用于优化死区时间的零电压检测 (ZVD) 报告
  - 支持理想二极管模式 (IDM)，降低软开关应用下的第三象限损耗
- 输入控制灵活多样
  - 独立输入模式 (IIM) 控制
  - 单路 PWM 输入，电阻可编程死区时间，适配 IO 受限的控制器
- 强大的保护
  - IIM 模式下的互锁保护 (LMG2104)
  - 内部自举电源电压调节，可防止 GaN FET 过驱动
  - 基于 $V_{DS}$ 监测的逐周期短路保护
  - 过热、欠压和短路事件的故障指示
- 外置辅助供电电源：5V
  - 支持 3.3V 和 5V 输入逻辑电平
- 寄生优化 QFN 封装，顶部设有外露焊盘，支持顶面散热

## 2 应用

- 服务器 PSU 和 BBU
- 电信电源
- 能源基础设施
- 电机驱动器
- D 类音频放大器

## 3 说明

LMG210xR0xx 器件是一个 100V 半桥功率级系列，具有集成栅极驱动器和增强模式氮化镓 (GaN) FET。该器件由采用半桥配置的高频 GaN FET 驱动器构成，可驱动两个 100V GaN FET。

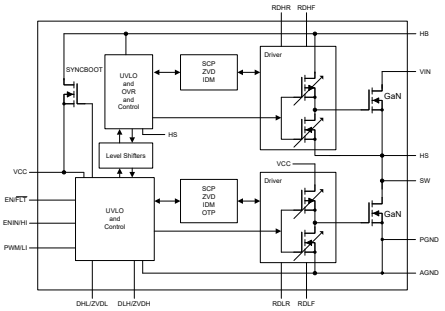
由于 GaN FET 的反向恢复为零，而且输入电容 ($C_{ISS}$) 和输出电容 ($C_{OSS}$) 都极小，所以 GaN FET 在功率转换方面优势极为显著。所有器件均安装在一个完全无键合线的封装平台上，最大限度减少封装寄生元件，便于在 PCB 板上安装使用。

无论 VCC 电压如何，TTL 逻辑兼容输入均可支持 3.3V 和 5V 逻辑电平。专有自举电压调节技术可将增强模式 GaN FET 的栅极电压调控至安全工作范围内。该器件配有用户友好型接口且更为出色，进一步提升了分立式 GaN FET 的优势。对于需要小尺寸、高频率、高效率运行的应用，该器件是理想之选。

**器件信息**

| 器件型号(3) | 封装(1) | 封装尺寸(2) |
|---|---|---|
| LMG210xR022 | VBN（VQFN-FCRLF，18） | 7mm × 4.5mm |
| LMG210xR044 | RAR（VQFN-FCRLF，17） | 5.5mm × 4.5mm |

(1) 有关更多信息，请参阅 节 7。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 请参阅 *器件比较表*。




简化版方框图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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# 4 器件比较

表 4-1. 器件比较

| 器件 | | $R_{DS\ (ON)}$(mΩ) | 封装尺寸(2) |
|---|---|---|---|
| LMG2105R022VBNR | LMG2104R022VBNR | 2.2 | 7.00mm × 4.50mm |
| LMG2105R044RARR | LMG2104R044RARR | 4.4 | 5.50mm × 4.50mm |

表 4-2. 特性比较

| 器件型号 | IIM 模式下的互锁 |
|---|---|
| LMG2104Rxxx | 启用 |
| LMG2105Rxxx | 禁用 |

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# 5 器件和文档支持

## 5.1 文档支持

### *5.1.1 相关文档*

- 德州仪器 (TI)，*LMG5200 GaN 功率级布局设计要点* 应用手册
- 德州仪器 (TI)，*使用 LMG5200：GaN 半桥功率级 EVM* 用户指南

## 5.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。点击右上角的*提醒我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 5.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

## 5.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 5.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 5.6 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |

# 6 修订历史记录

| 日期 | 修订版本 | 注释 |
|---|---|---|
| May 2026 | * | 初始发行版 |

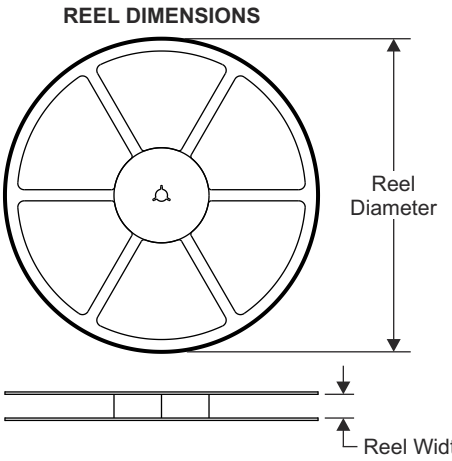
ADVANCE INFORMATION

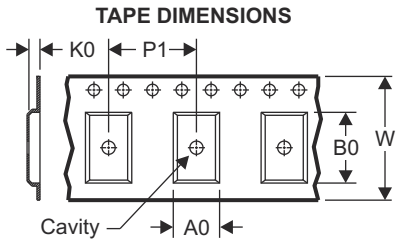

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# 7 机械、封装和可订购信息

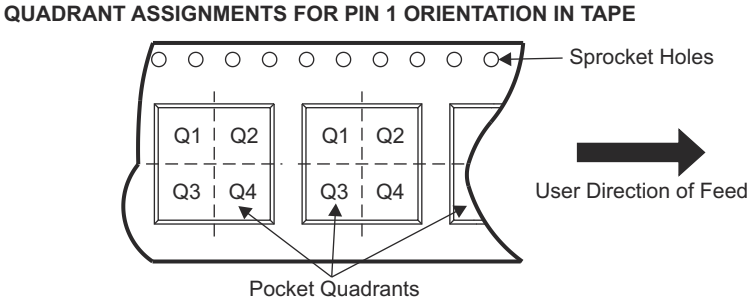
以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

## 7.1 卷带包装信息




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |



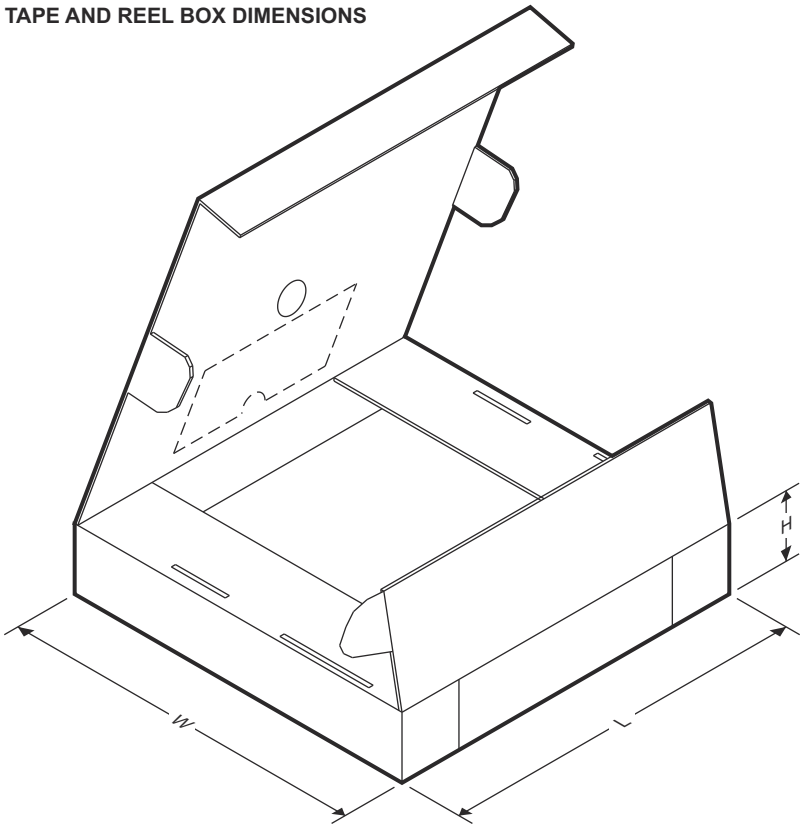

| 器件 | 封装类型 | 封装图 | 引脚 | SPQ | 卷带直径 (mm) | 卷带宽度 W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1象限 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMG2104R022VBNR | VQFN-FCRLF | VBN | 18 | 2000 | 330 | 16.4 | 5.3 | 7.8 | 1.2 | 8 | 16.0 | Q1 |
| LMG2104R044RARR | VQFN-FCRLF | RAR | 17 | 2000 | 330 | 16.4 | 4.8 | 5.8 | 1.15 | 8 | 16.0 | Q1 |
| LMG2105R022VBNR | VQFN-FCRLF | VBN | 18 | 2000 | 330 | 16.4 | 5.3 | 7.8 | 1.2 | 8 | 16.0 | Q1 |
| LMG2105R044RARR | VQFN-FCRLF | RAR | 17 | 2000 | 330 | 16.4 | 4.8 | 5.8 | 1.15 | 8 | 16.0 | Q1 |

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TAPE AND REEL BOX DIMENSIONS




| 器件 | 封装类型 | 封装图 | 引脚 | SPQ | 长度 (mm) | 宽度 (mm) | 高度 (mm) |
|---|---|---|---|---|---|---|---|
| LMG2104R022VBNR | VQFN-FCRLF | VBN | 18 | 2000 | 336.6 | 336.6 | 28.6 |
| LMG2104R044RARR | VQFN-FCRLF | RAR | 17 | 2000 | 336.6 | 336.6 | 28.6 |
| LMG2105R022VBNR | VQFN-FCRLF | VBN | 18 | 2000 | 336.6 | 336.6 | 28.6 |
| LMG2105R044RARR | VQFN-FCRLF | RAR | 17 | 2000 | 336.6 | 336.6 | 28.6 |

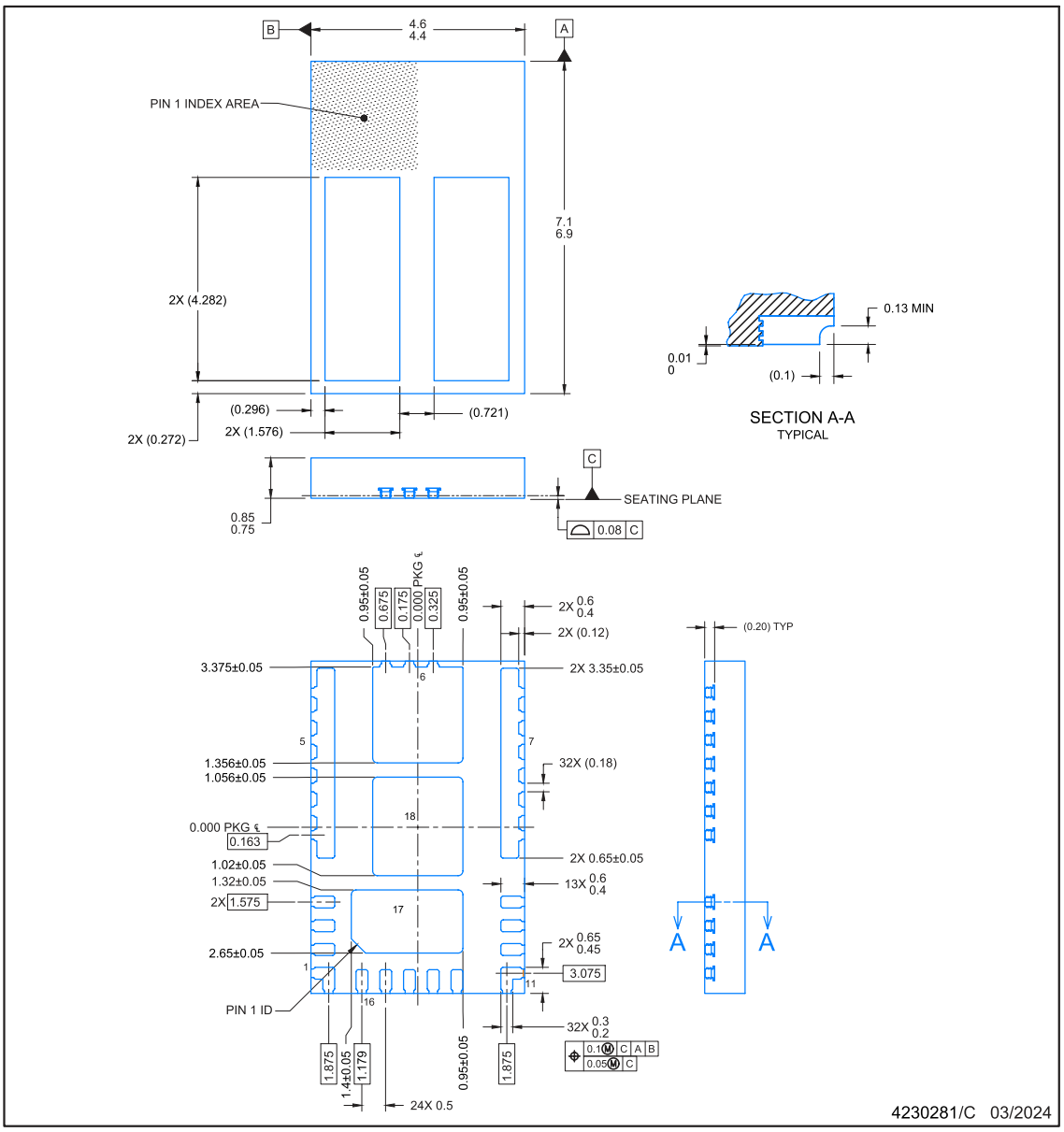

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## 7.2 机械数据

**PACKAGE OUTLINE**

**VBN0018A** — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

ADVANCE INFORMATION

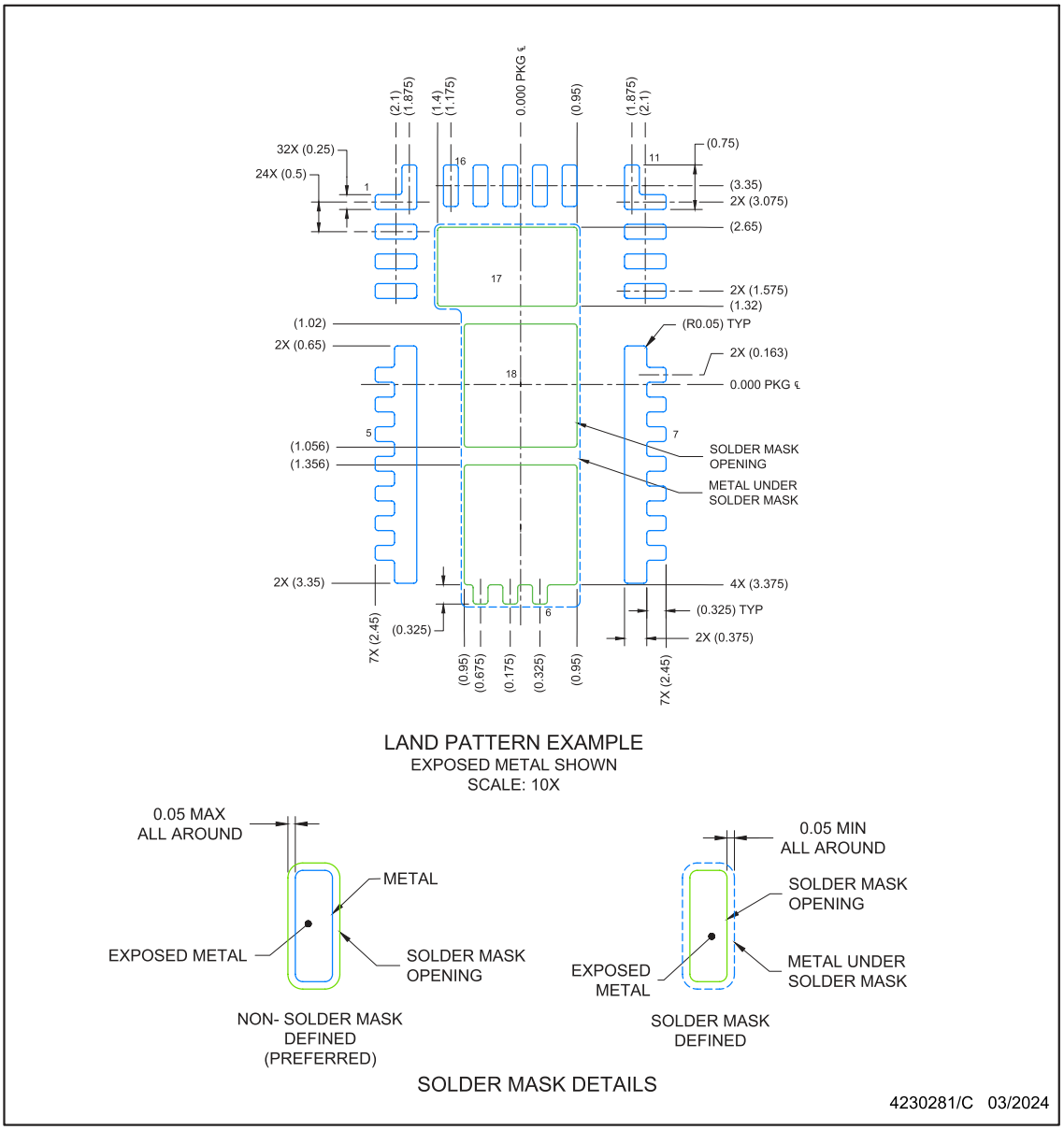

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## EXAMPLE BOARD LAYOUT

**VBN0018A** — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD




NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

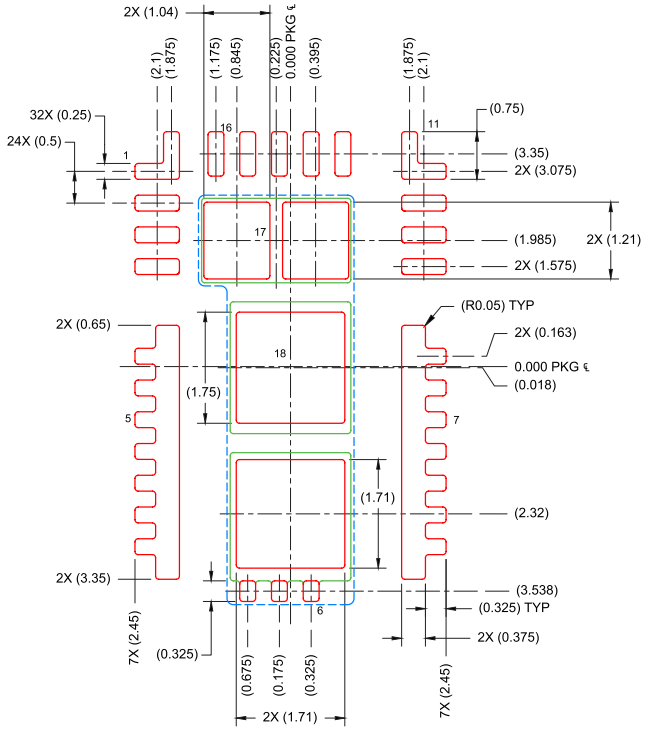

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# EXAMPLE STENCIL DESIGN

## VBN0018A

### VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 6: 78%
PAD 17: 81%
PAD 18: 76%

4230281/C 03/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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ADVANCE INFORMATION

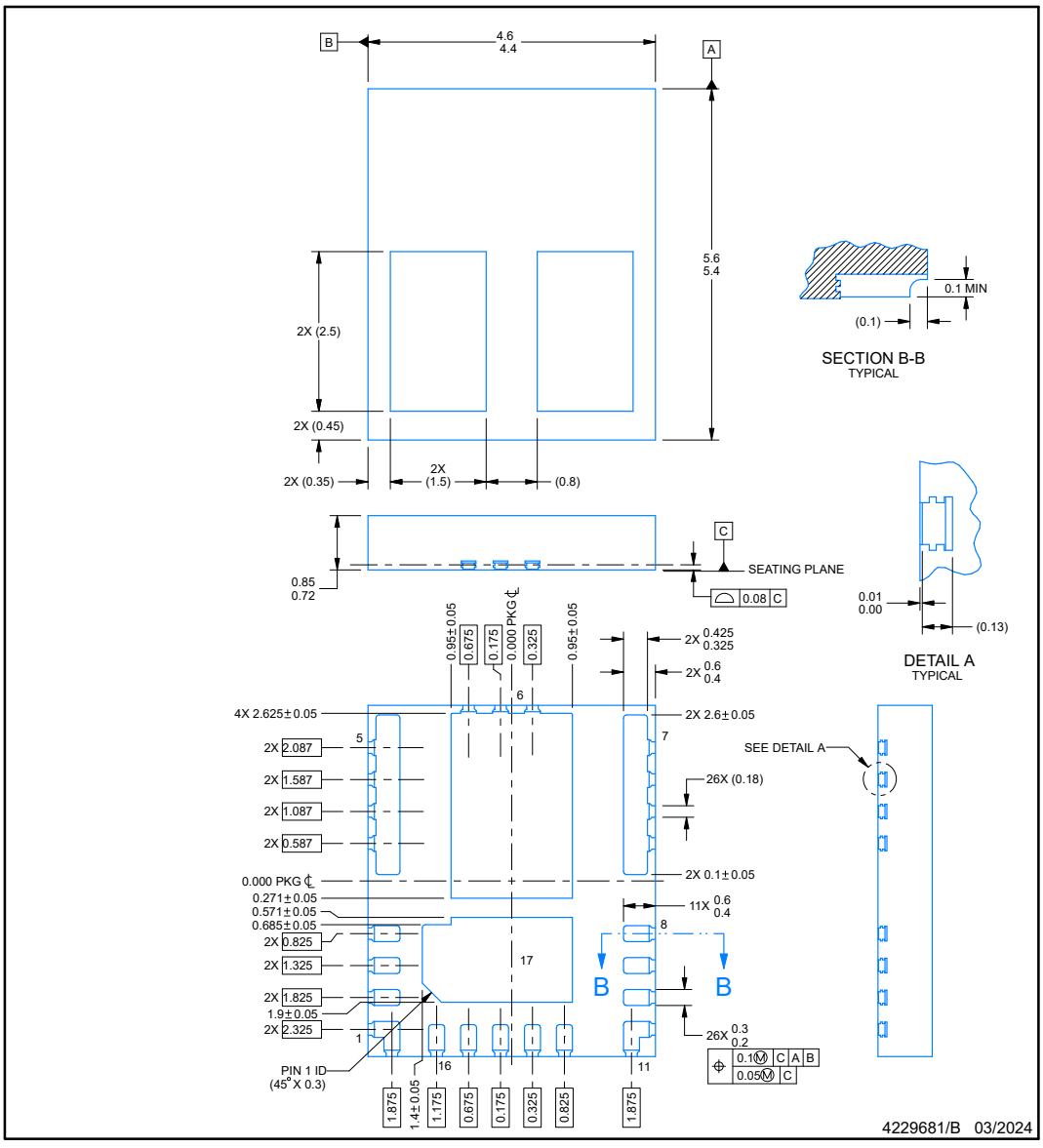
# PACKAGE OUTLINE

## RAR0017B



## VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

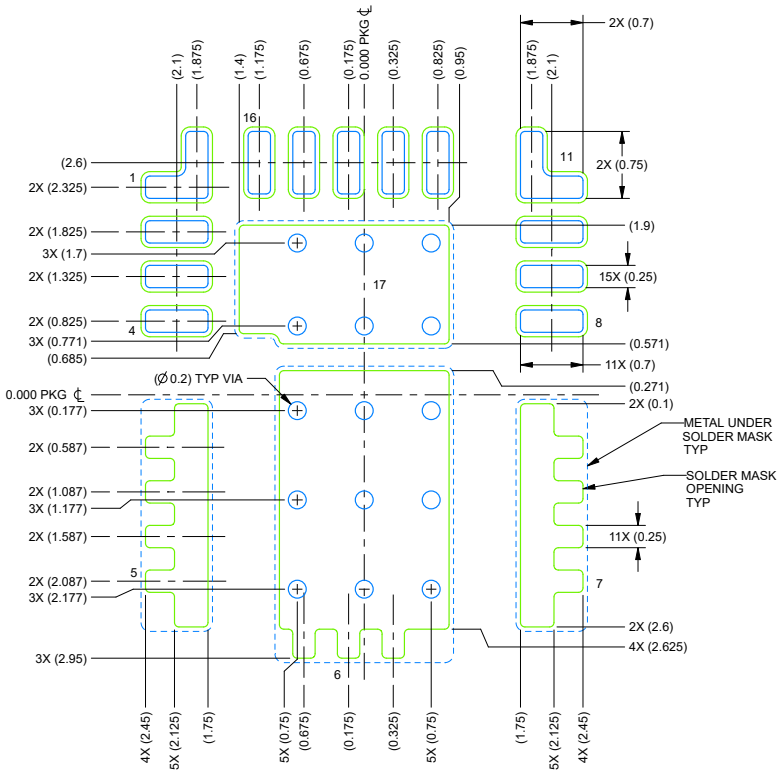
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.


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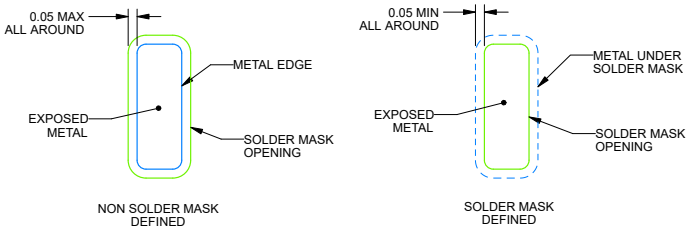
## EXAMPLE BOARD LAYOUT

**RAR0017B** — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD




LAND PATTERN EXAMPLE
SCALE: 15X




SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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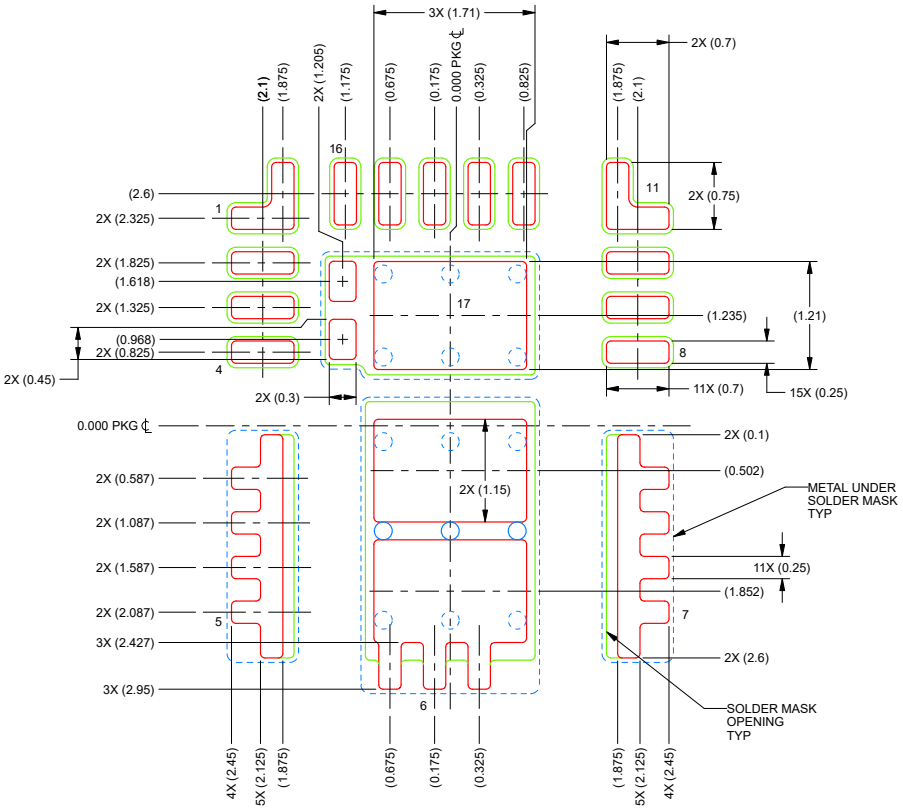
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## EXAMPLE STENCIL DESIGN

**RAR0017B** — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 5, 6 & 7: 75%
PAD 17: 76%

4229681/B 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| XLMG2104R022VBNR | Active | Preproduction | VQFN-FCRLF (VBN) \| 18 | 2500 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| XLMG2104R044RARR | Active | Preproduction | VQFN-FCRLF (RAR) \| 17 | 2500 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| XLMG2105R022VBNR | Active | Preproduction | VQFN-FCRLF (VBN) \| 18 | 2500 \| LARGE T&R | - | Call TI | Call TI | - | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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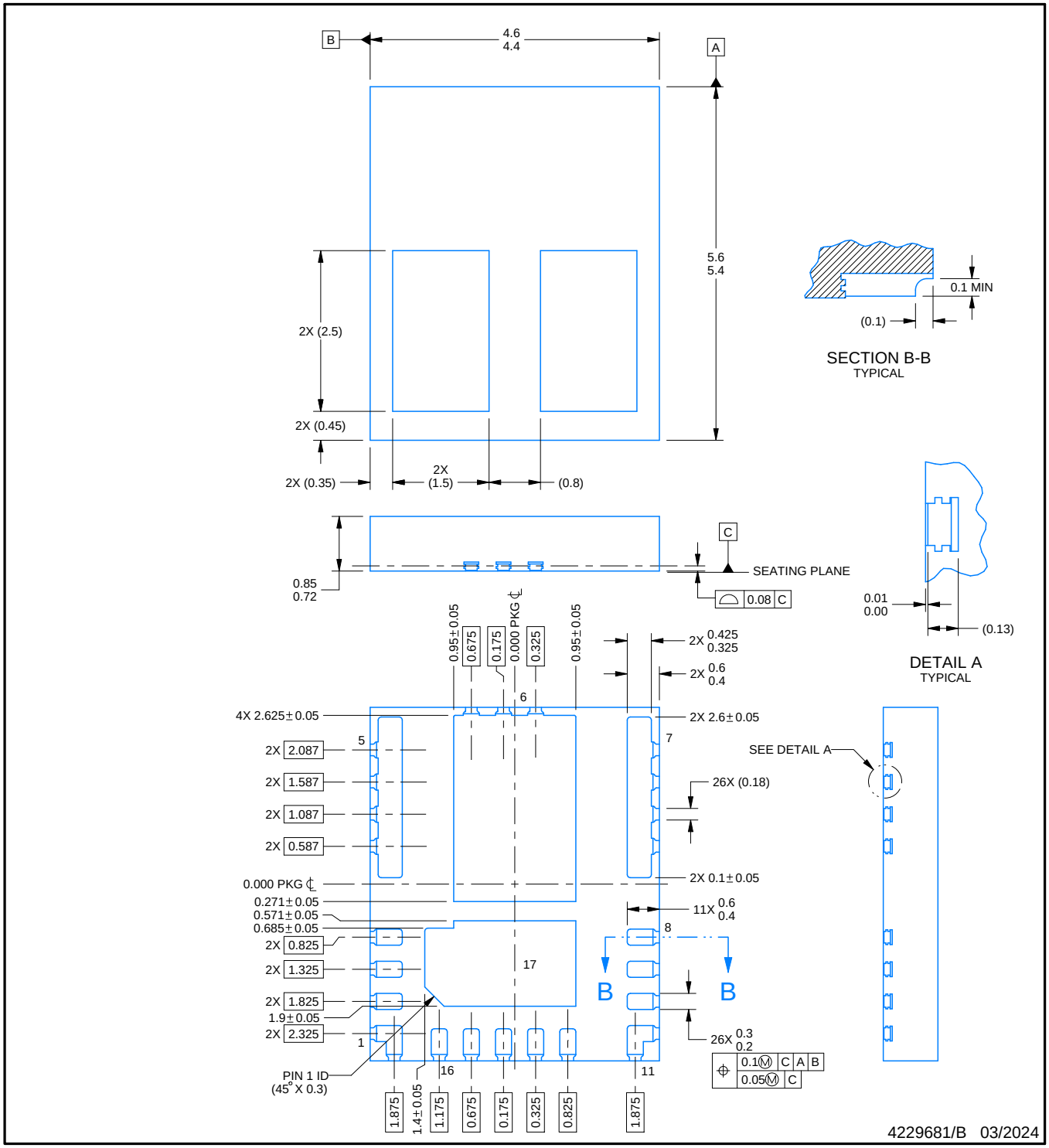
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE OUTLINE

## RAR0017B

## VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

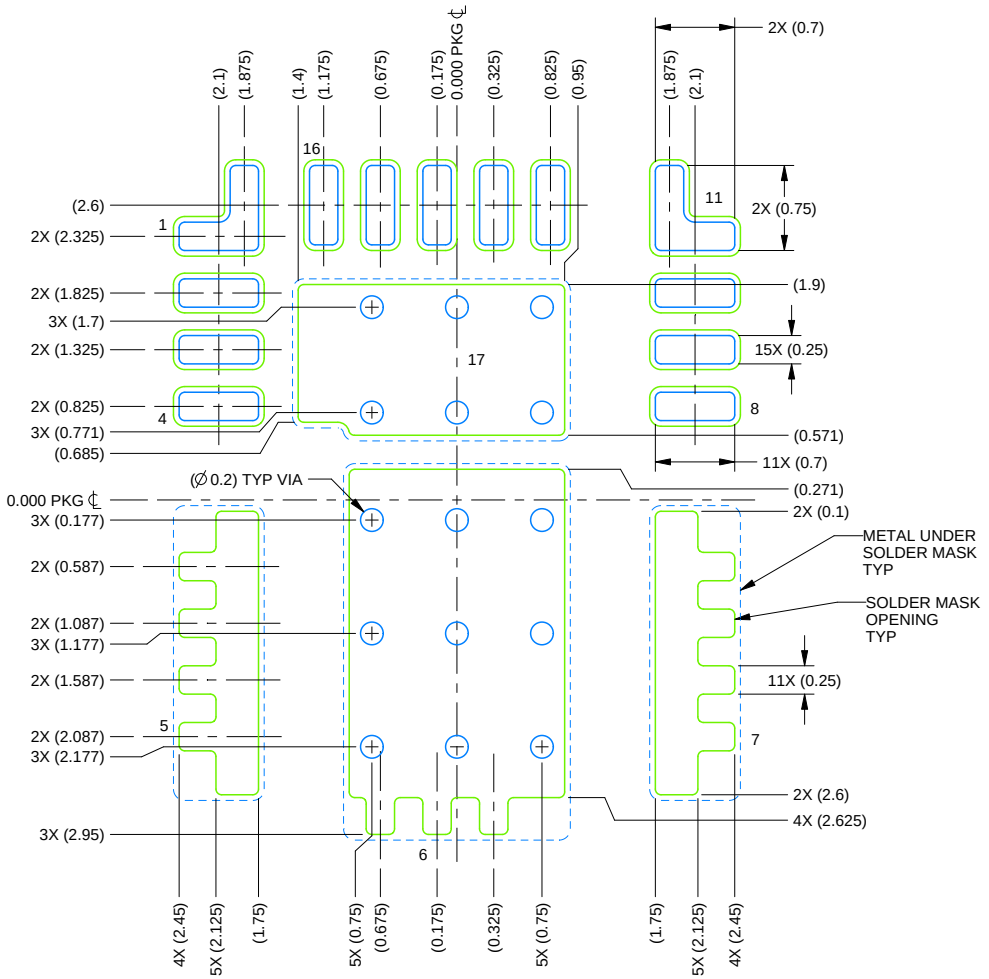
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

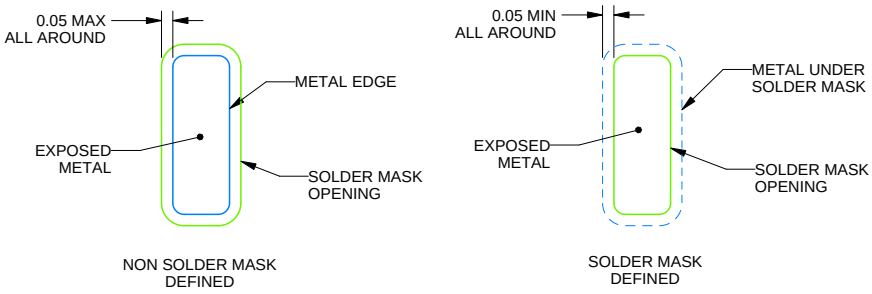
## RAR0017B

## VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




LAND PATTERN EXAMPLE
SCALE: 15X

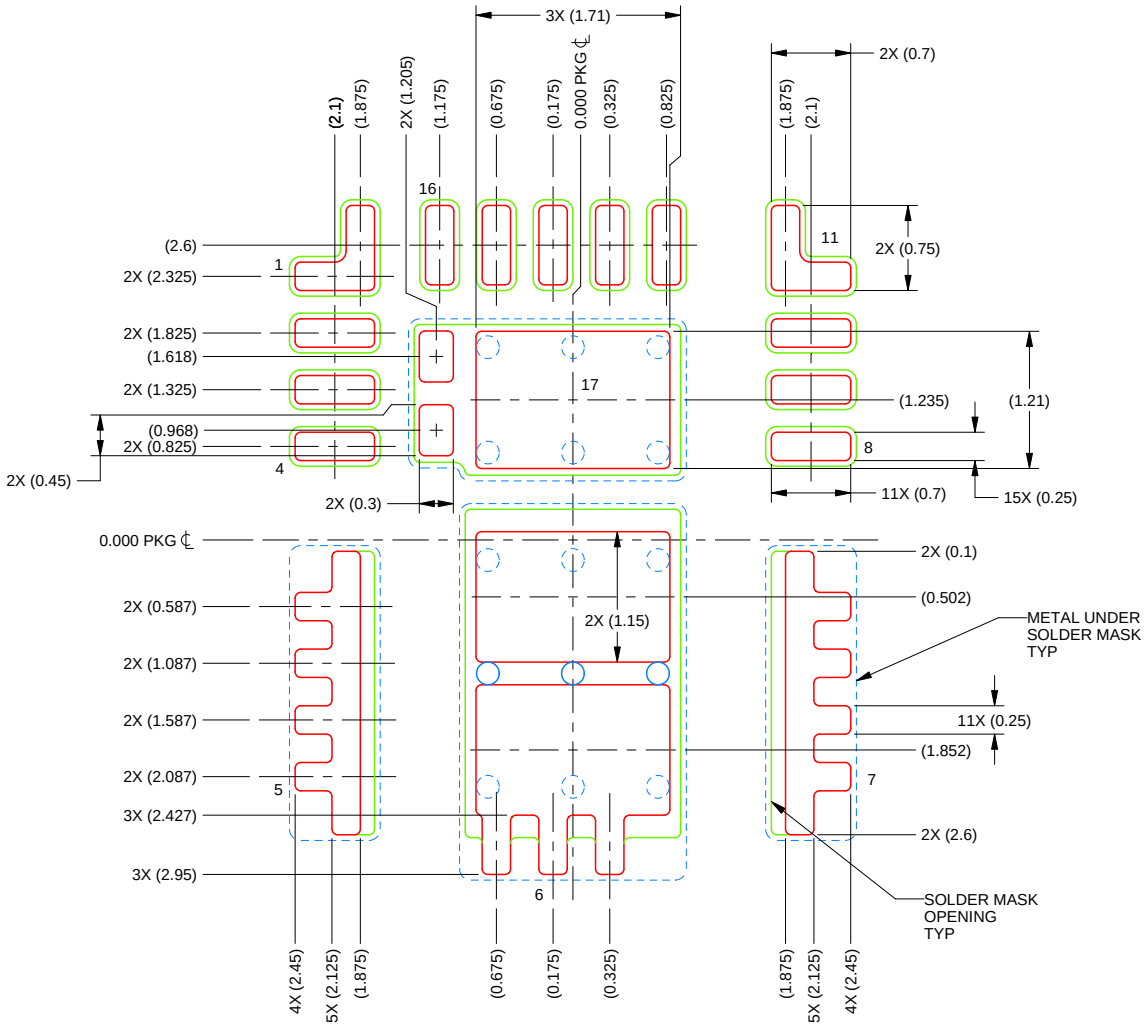



SOLDER MASK DETAILS

4229681/B 03/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 5, 6 & 7: 75%
PAD 17: 76%

4229681/B 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# GENERIC PACKAGE VIEW

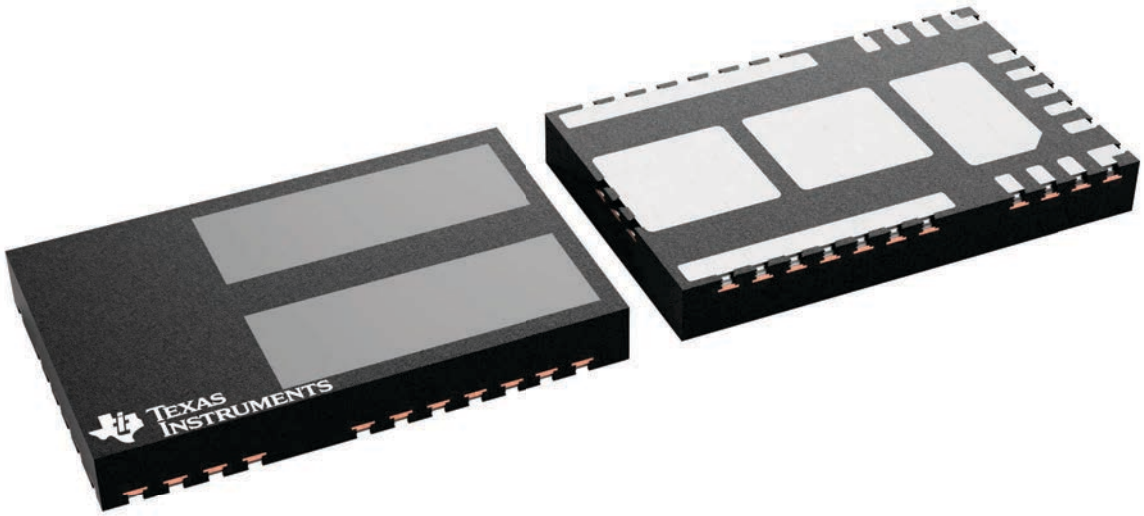
## VBN 18

## VQFN-FCRLF - 0.85 mm max height

**4.5 x 7, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



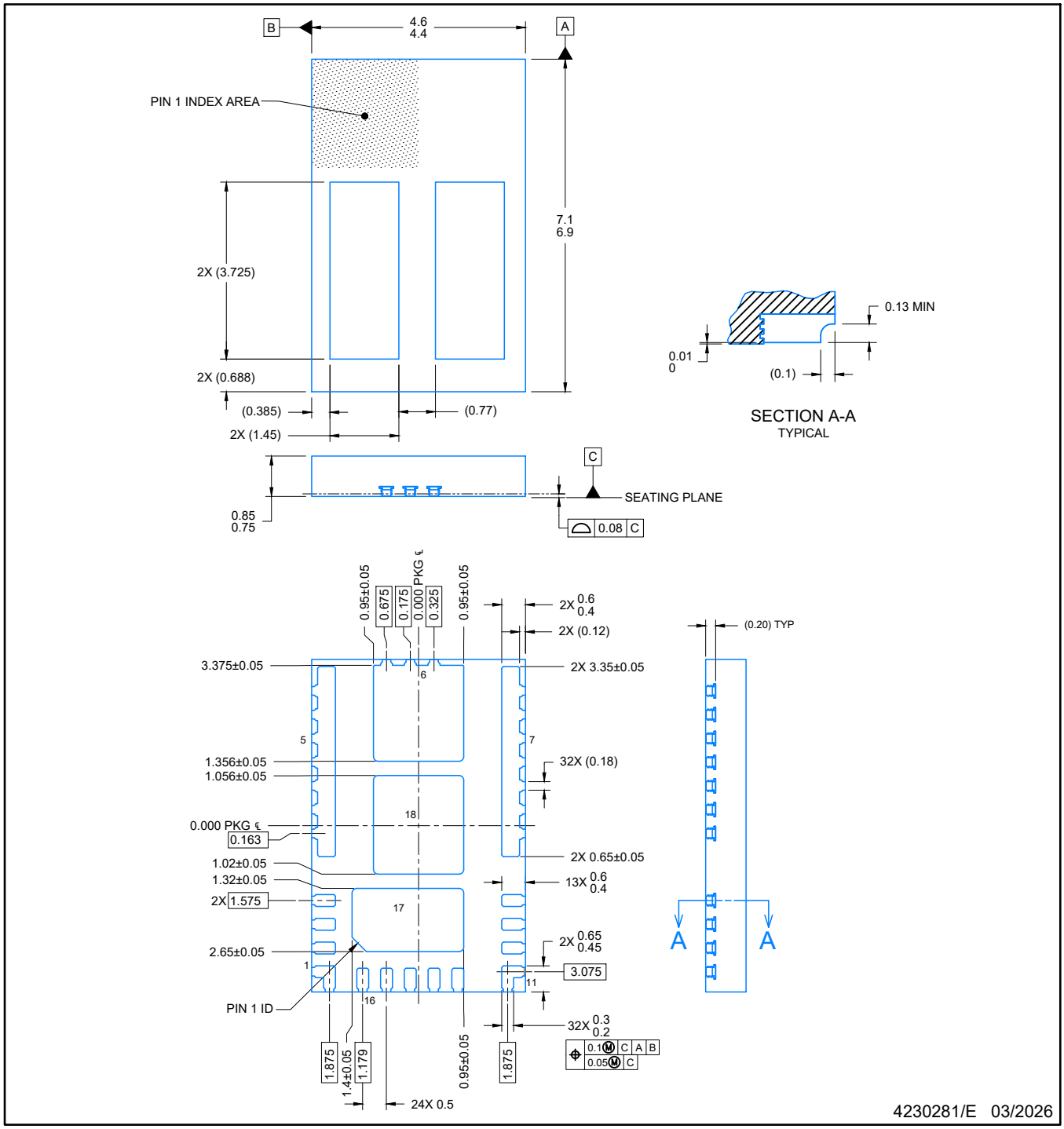

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# PACKAGE OUTLINE

## VBN0018A

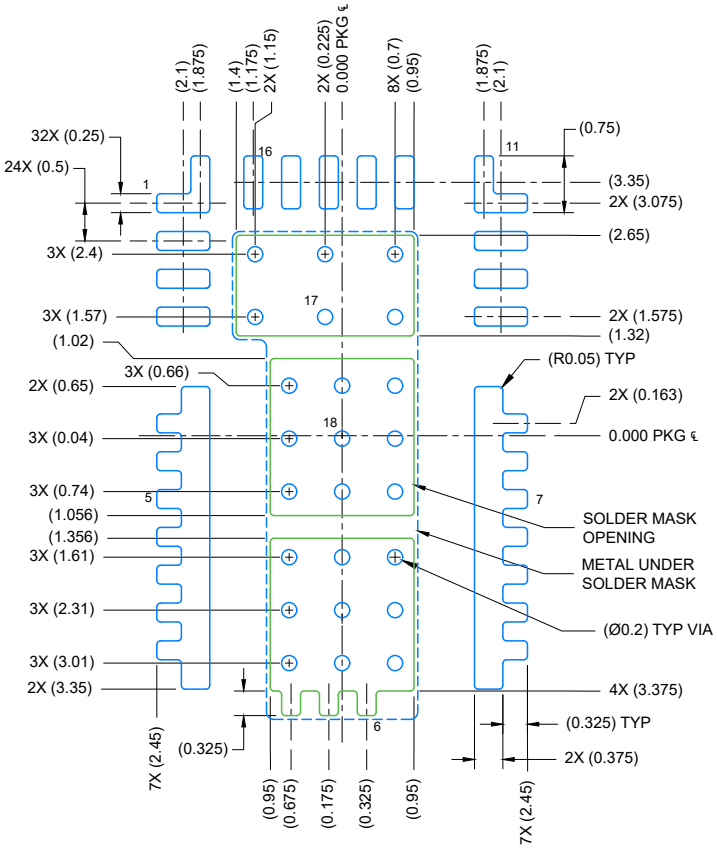
## VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD




NOTES:

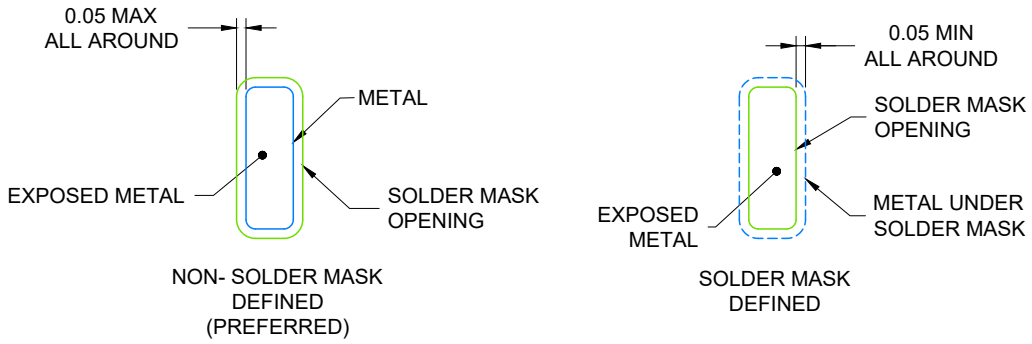
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 10X

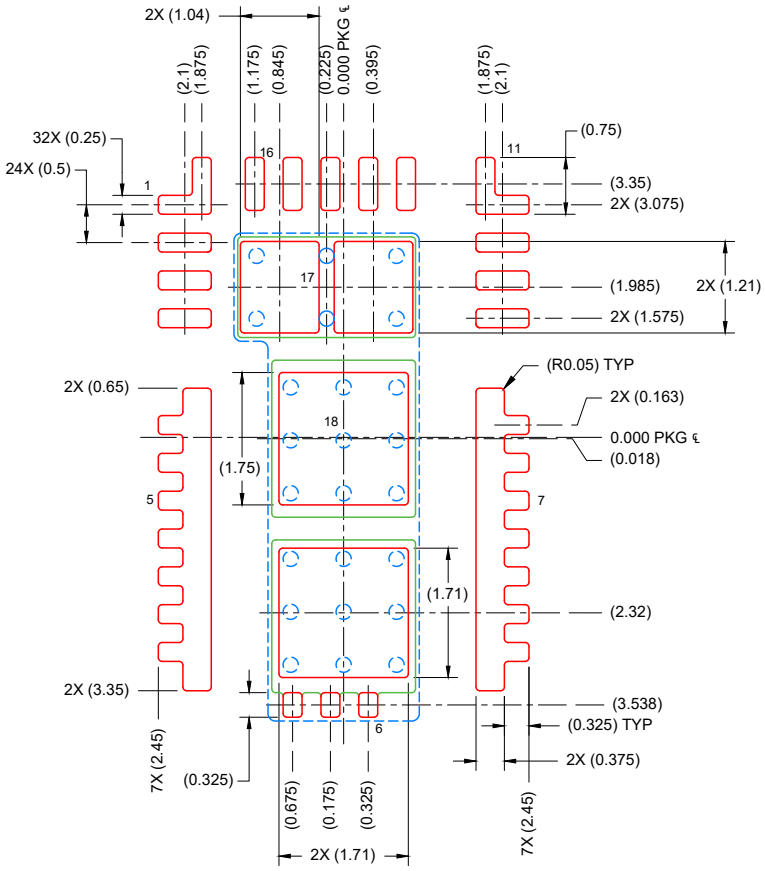



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 6: 78%
PAD 17: 81%
PAD 18: 76%

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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