# LM723JAN Voltage Regulator

**Check for Samples: LM723JAN**

## FEATURES

- **150 mA Output Current without External Pass Transistor**
- **Output Currents in Excess of 10A Possible by Adding External Transistors**
- **Input Voltage 40V Max**
- **Output Voltage Adjustable from 2V to 37V**
- **Can be Used as Either a Linear or a Switching Regulator**

## DESCRIPTION

The LM723 is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The LM723 is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

## Connection Diagram

NOTE: Pin 5 connected to case.

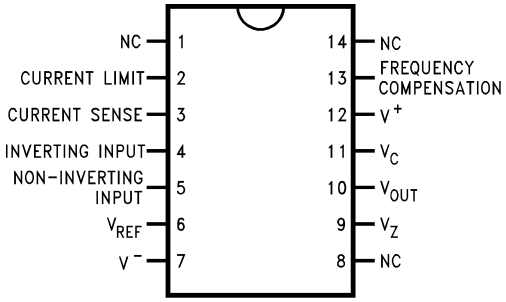



**Figure 1. CDIP Package**
**Top View**
**See Package J0014A**

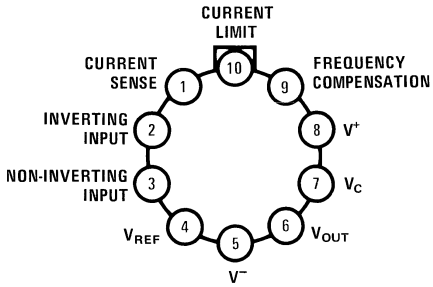
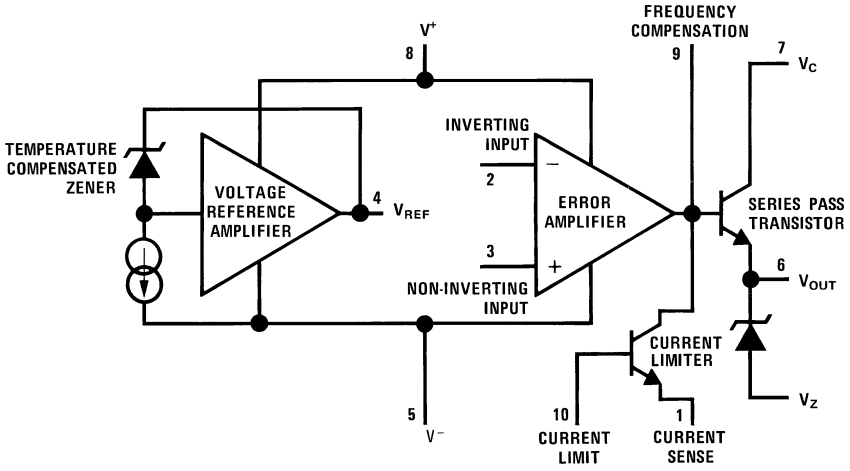


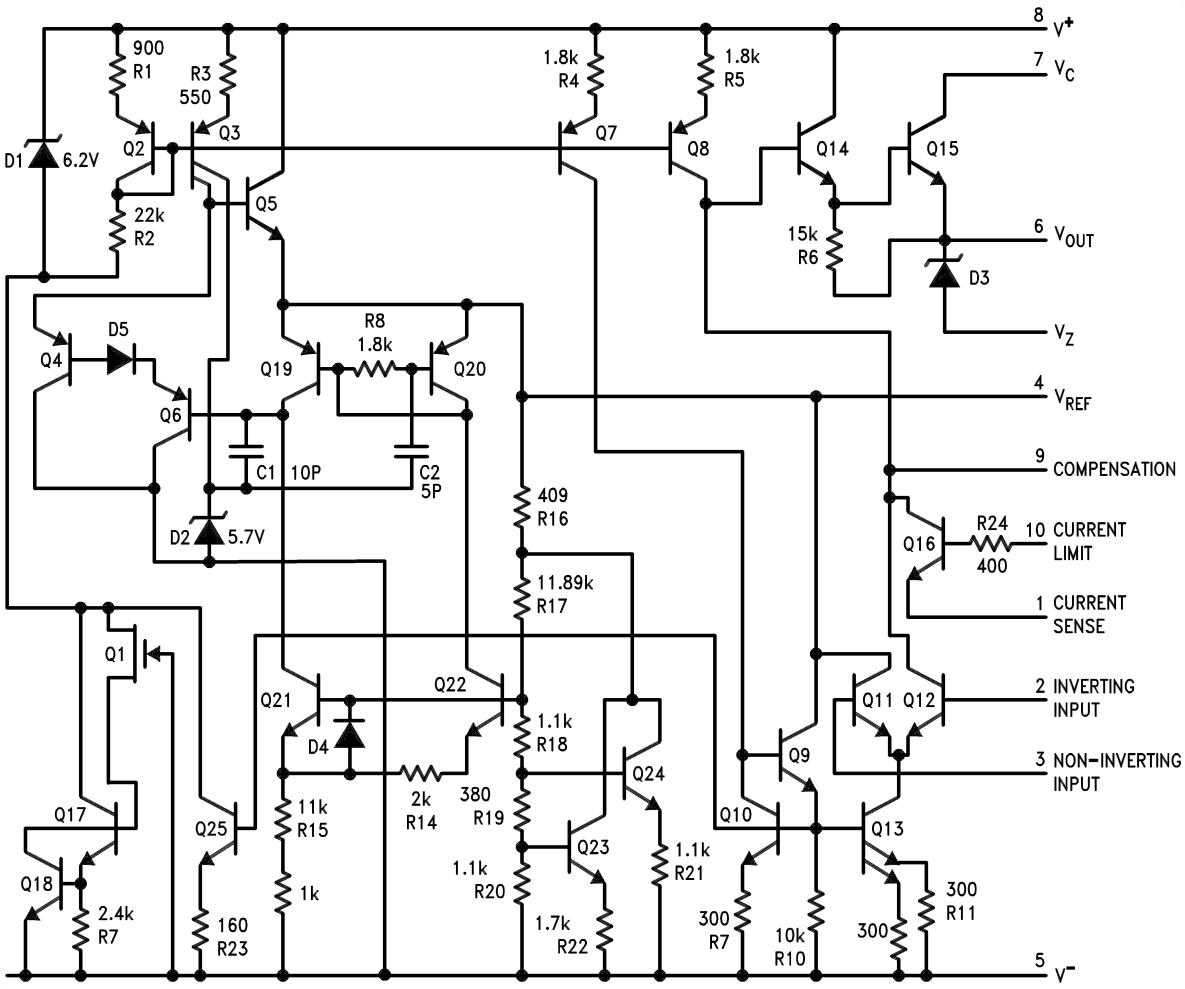

**Figure 2. Metal Can Package**
**Top View**
**See Package LME0010C**

## Equivalent Circuit




Pin numbers refer to metal can package.

## Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)

| | | |
|---|---|---|
| Pulse Voltage from $V^+$ to $V^-$ (50 ms) | | 50V |
| Continuous Voltage from $V^+$ to $V^-$ | | 40V |
| Input-Output Voltage Differential | | 40V |
| Differential Input Voltage | | ±5V |
| Voltage between non-inverting input and $V^-$ | | +8V |
| Current from $V_Z$ | | 25 mA |
| Current from $V_{REF}$ | | 15 mA |
| Internal Power Dissipation ($T_A$ = 125°C) | Metal Can (2) | 300 mW |
| | CDIP (2) | 400 mW |
| Maximum $T_J$ | | +175°C |
| Storage Temperature Range | | −65°C ≤ $T_A$ ≤ +150°C |
| Lead Temperature (Soldering, 4 sec. max.) | | 300°C |
| Thermal Resistance | | |
| $\theta_{JA}$ | CDIP (Still Air) | 100°C/W |
| | CDIP (500LF/ Min Air flow) | 61°C/W |
| | Metal Can (Still Air) | 156°C/W |
| | Metal Can (500LF/ Min Air flow) | 89°C/W |
| $\theta_{JC}$ | CDIP | 22°C/W |
| | Metal Can | 37°C/W |
| ESD Tolerance (3) | | 1200V |

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is less. See derating curves for maximum power rating above 25°C.
(3) Human body model, 1.5 kΩ in series with 100 pF.

## Recommended Operating Conditions

| | |
|---|---|
| Input Voltage Range | 9.5V to 40V $_{DC}$ |
| Output Voltage Range | 2V to 37V $_{DC}$ |
| Input-Output Voltage Differential | 2.5 V to 38V $_{DC}$ |
| Ambient Operating Temperature Range | −55°C ≤ $T_A$ ≤ +125°C |

## Quality Conformance Inspection

MIL-STD-883, Method 5004 and Method 5005

| Subgroup | Description | Temp ( °C) |
|---|---|---|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |

| Subgroup | Description | Temp ( °C) |
|---|---|---|
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |

## Electrical Characteristics

DC Parameters (1)

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $V_{Rline}$ | Line Regulation | 12V ≤ $V_{IN}$ ≤ 15V, $V_{OUT}$ = 5V, $I_L$ = 1mA | | −0.1 | 0.1 | %$V_{OUT}$ | 1 |
| | | | | −0.2 | 0.2 | %$V_{OUT}$ | 2 |
| | | | | −0.3 | 0.3 | %$V_{OUT}$ | 3 |
| | | 12V ≤ $V_{IN}$ ≤ 40V, $V_{OUT}$ = 2V, $I_L$ = 1mA | | −0.2 | 0.2 | %$V_{OUT}$ | 1 |
| | | 9.5V ≤ $V_{IN}$ ≤ 40V, $V_{OUT}$ = 5V, $I_L$ = 1mA | | −0.3 | 0.3 | %$V_{OUT}$ | 1 |
| | | 12V ≤ $V_{IN}$ ≤ 15V, $V_{OUT}$ = 5V, $I_L$ = 1mA | | −10.0 | +10.0 | mV | 1 |
| | | | | −20.0 | +20.0 | mV | 2 |
| | | | | −30.0 | +30.0 | mV | 3 |
| $V_{Rload}$ | Load Regulation | 1mA ≤ $I_L$ ≤ 50mA, $V_{IN}$ = 12V, $V_{OUT}$ = 5V | | −0.15 | 0.15 | %$V_{OUT}$ | 1 |
| | | | | −0.4 | 0.4 | %$V_{OUT}$ | 2 |
| | | | | −0.6 | 0.6 | %$V_{OUT}$ | 3 |
| | | 1mA ≤ $I_L$ ≤ 10mA, $V_{IN}$ = 40V, $V_{OUT}$ = 37V | | −0.5 | 0.5 | %$V_{OUT}$ | 1 |
| | | 6mA ≤ $I_L$ ≤ 12mA, $V_{IN}$ = 10V, $V_{OUT}$ = 7.5V | | −0.2 | 0.2 | %$V_{OUT}$ | 1 |
| | | 1mA ≤ $I_L$ ≤ 50mA, $V_{IN}$ = 12V, $V_{OUT}$ = 5V | | −15.0 | +15.0 | mV | 1 |
| | | | | −40.0 | +40.0 | mV | 2 |
| | | | | −60.0 | +60.0 | mV | 3 |
| $V_{REF}$ | Voltage Reference | $I_{REF}$ = 1mA, $V_{IN}$ = 12V | | 6.95 | 7.35 | V | 1 |
| | | | | 6.9 | 7.4 | V | 2, 3 |
| $I_{SCD}$ | Standby Current | $V_{IN}$ = 30V, $I_L$ = $I_{REF}$ = 0, $V_{OUT}$ = $V_{REF}$ | | 0.5 | 3 | mA | 1 |
| | | | | 0.5 | 2.4 | mA | 2 |
| | | | | 0.5 | 3.5 | mA | 3 |
| $I_{OS}$ | Short Circuit Current | $V_{OUT}$ = 5V, $V_{IN}$ =12V, $R_{SC}$ = 10Ω, $R_L$ = 0 | | 45 | 85 | mA | 1 |
| $V_Z$ | Zener Voltage | $I_Z$ = 1mA | | (2)(3) 5.58 | 6.82 | V | 1 |
| $V_{OUT}$ | Output Voltage | $V_{IN}$ = 12V, $V_{OUT}$ = 5V, $I_L$ = 1mA | (4) | 4.5 | 5.5 | V | 1, 2, 3 |

(1) Unless otherwise specified, $T_A$ = 25°C, $V_{IN}$ = $V^+$ = $V_C$ = 12V, $V^-$ = 0, $V_{OUT}$ = 5V, $I_L$ = 1 mA, $R_{SC}$ = 0, $C_1$ = 100 pF, $C_{REF}$ = 0 and divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in Figure 14. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.
(2) For metal can applications where $V_Z$ is required, an external 6.2V zener diode should be connected in series with $V_{OUT}$.
(3) Tested for 14 – lead DIP only.
(4) Setup test for Temp. Coeff.

## Electrical Characteristics (continued)

DC Parameters (1)

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| Delta $V_{OUT}$ / Delta T | Average Temperature Coefficient of Output Voltage | 25°C ≤ $T_A$ ≤ +125°C, $V_{IN}$ = 12V, $V_{OUT}$ = 5V, $I_L$ = 1mA | (5) | −0.01 | 0.01 | %/°C | 8A |
| | | −55°C ≤ $T_A$ ≤ +25°C, $V_{IN}$ = 12V, $V_{OUT}$ = 5V, $I_L$ = 1mA | (5) | −0.015 | 0.015 | %/°C | 8B |
| Delta $V_{OUT}$ / Delta $V_{IN}$ | Ripple Rejection | f = 10KHz, $C_{REF}$ = 0F, $V_{INS}$ = $2V_{RMS}$ | | 64 | | dB | 4 |
| | | f = 10KHz, $C_{REF}$ = 5µF, $V_{INS}$ = $2V_{RMS}$ | | 76 | | dB | 4 |
| $N_O$ | Output Noise Voltage | 100Hz ≤ f ≤ 10KHz, $V_{INS}$ = $0V_{RMS}$, $C_{REF}$ = 0µF | | | 120 | $\mu V_{RMS}$ | 4 |
| | | 100Hz ≤ f ≤ 10KHz, $V_{INS}$ = $0V_{RMS}$, $C_{REF}$ = 5µF | | | 7 | $\mu V_{RMS}$ | 4 |
| Delta $V_{OUT}$ / Delta $V_{IN}$ | Line Transient Response | $V_{IN}$ = 12V, $V_{OUT}$ = 5V, $I_L$ = 1mA, $C_{REF}$ = 5µF, $R_{SC}$ = 0Ω, Delta $V_{IN}$ = 3V for 25µsec | | 0 | 10 | mV/V | 4 |
| Delta $V_{OUT}$ / Delta $I_L$ | Load Transient Response | $V_{IN}$ = 12V, $V_{OUT}$ = 5V, $I_L$ = 40mA, $C_{REF}$ = 5µF, $R_{SC}$ = 0Ω, Delta $I_L$ = 10mA for 25µsec | | −1.5 | 0 | mV/mA | 4 |

(5) Calculated parameter

## DC Parameters: Drift Values

Delta calculations performed on JAN S and QMLV devices at Group B, Subgroup 5, only.

| Symbol | Parameters | Conditions | Notes | Min | Max | Unit | Sub-groups |
|---|---|---|---|---|---|---|---|
| $V_{Rline}$ | Line Regulation | 12V ≤ $V_{IN}$ ≤ 15V, $V_{OUT}$ = 5V, $I_L$ = 1mA, ±1mV, or ±15% (whichever is greater) | | −1.0 | 1.0 | mV | 1 |
| $V_{Rload}$ | Load Regulation | 1mA ≤ $I_L$ ≤ 50mA, $V_{IN}$ = 12V, $V_{OUT}$ = 5V, ±1mV, or ±20% (whichever is greater) | | −1.0 | 1.0 | mV | 1 |
| $V_{REF}$ | Reference Voltage | $I_{REF}$ = 1mA, $V_{IN}$ = 12V | | −15 | 15 | mV | 1 |
| $I_{SCD}$ | Standby Current Drain | $V_{IN}$ = 30V, $I_L$ = $I_{REF}$ =0, $V_{OUT}$ = $V_{REF}$ | | −10 | 10 | % | 1 |

## Typical Performance Characteristics

**Load Regulation Characteristics with Current Limiting**

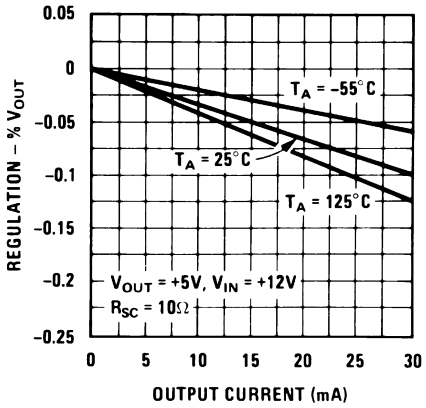



Figure 3.

**Load Regulation Characteristics with Current Limiting**

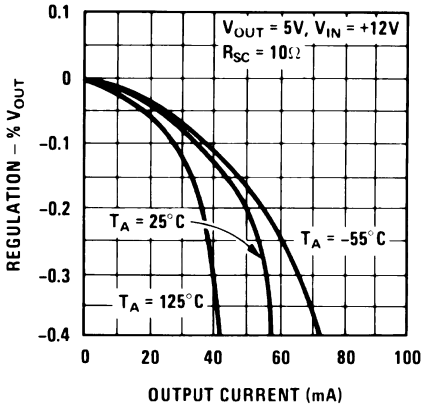



Figure 4.

**Load & Line Regulation vs Input-Output Voltage Differential**

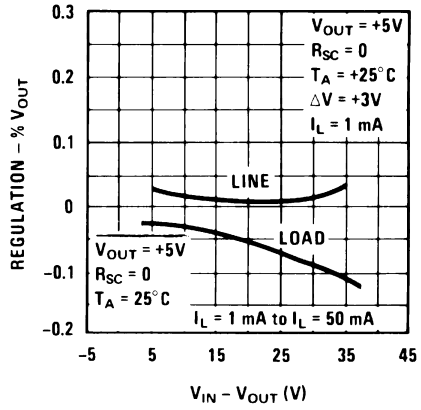



Figure 5.

**Current Limiting Characteristics**

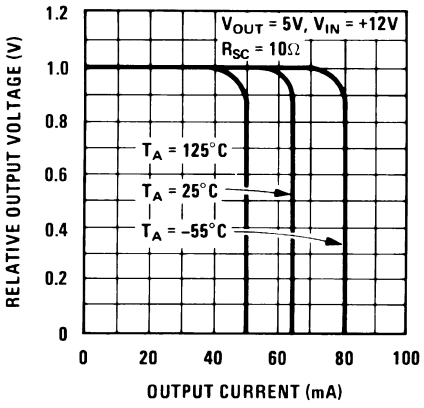



Figure 6.

**Current Limiting Characteristics vs Junction Temperature**

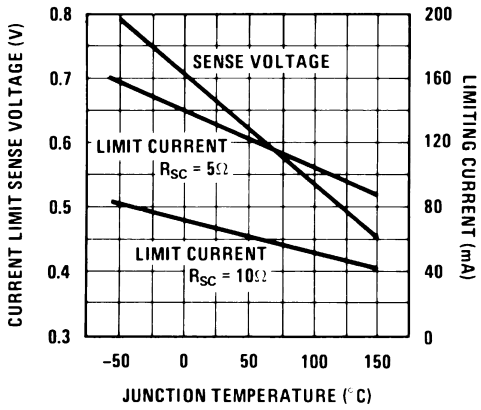



Figure 7.

**Standby Current Drain vs Input Voltage**

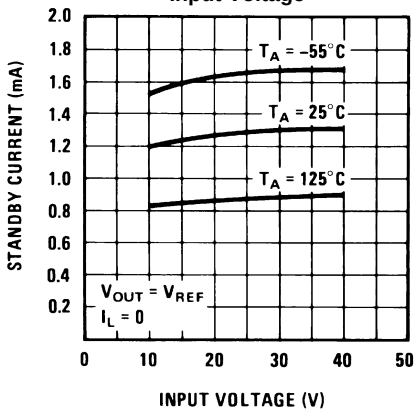



Figure 8.

## Typical Performance Characteristics (continued)

**Line Transient Response**

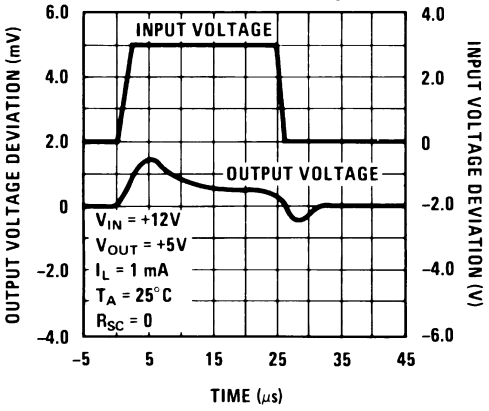



Figure 9.

**Load Transient Response**

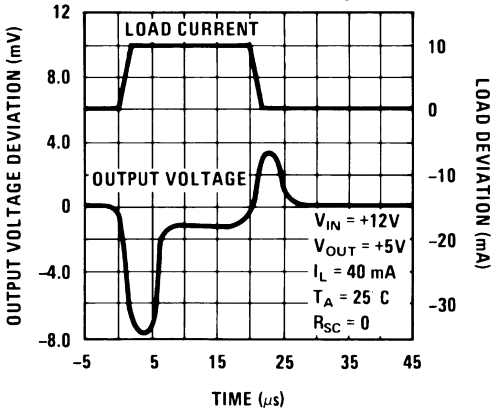



Figure 10.

**Output Impedence vs Frequency**

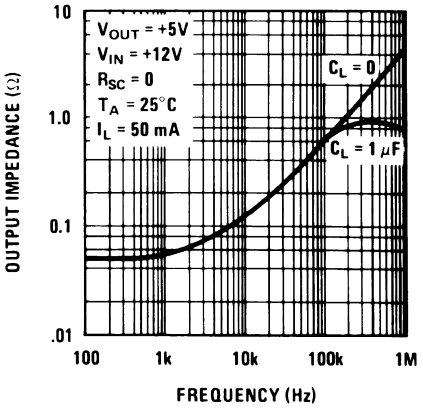



Figure 11.

## Maximum Power Ratings

**Noise vs Filter Capacitor ($C_{REF}$ in Circuit of Figure 14) (Bandwidth 100 Hz to 10 kHz)**

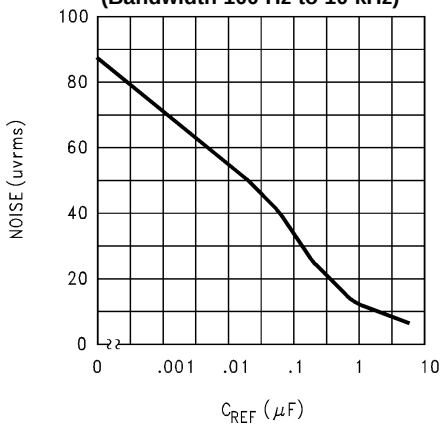



Figure 12.

**LM723 Power Dissipation vs Ambient Temperature**

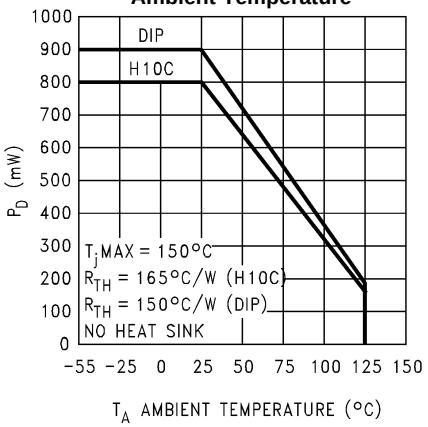



Figure 13.

## Table 1. Resistor Values (kΩ) for Standard Output Voltage

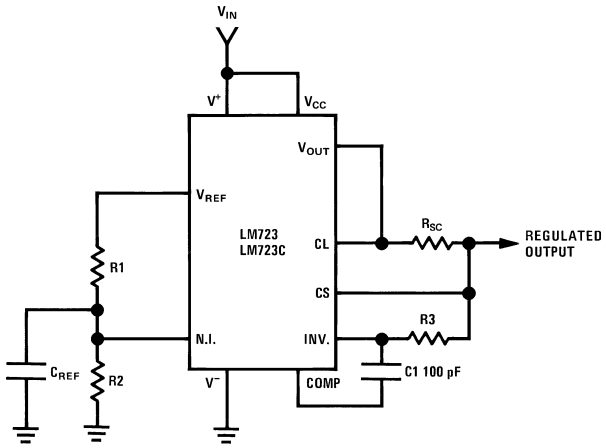
| Positive Output Voltage | Applicable Figures (1) | Fixed Output ±5% | | Output Adjustable ±10% (2) | | | Negative Output Voltage | Applicable Figures | Fixed Output ±5% | | 5% Output Adjustable ±10% | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | R1 | R2 | R1 | P1 | R2 | | | R1 | R2 | R1 | P1 | R2 |
| +3.0 | Figure 14, Figure 18, Figure 19, Figure 22, Figure 25 (Figure 17) | 4.12 | 3.01 | 1.8 | 0.5 | 1.2 | +100 | Figure 20 | 3.57 | 102 | 2.2 | 10 | 91 |
| +3.6 | Figure 14, Figure 18, Figure 19, Figure 22, Figure 25 (Figure 17) | 3.57 | 3.65 | 1.5 | 0.5 | 1.5 | +250 | Figure 20 | 3.57 | 255 | 2.2 | 10 | 240 |
| +5.0 | Figure 14, Figure 18, Figure 19, Figure 22, Figure 25 (Figure 17) | 2.15 | 4.99 | 0.75 | 0.5 | 2.2 | −6 (3) | Figure 16, (Figure 23) | 3.57 | 2.43 | 1.2 | 0.5 | 0.75 |
| +6.0 | Figure 14, Figure 18, Figure 19, Figure 22, Figure 25 (Figure 17) | 1.15 | 6.04 | 0.5 | 0.5 | 2.7 | −9 | Figure 16, Figure 23 | 3.48 | 5.36 | 1.2 | 0.5 | 2.0 |
| +9.0 | Figure 15, Figure 17, (Figure 18, Figure 19, Figure 22, Figure 25) | 1.87 | 7.15 | 0.75 | 1.0 | 2.7 | −12 | Figure 16, Figure 23 | 3.57 | 8.45 | 1.2 | 0.5 | 3.3 |
| +12 | Figure 15, Figure 17, (Figure 18, Figure 19, Figure 22, Figure 25) | 4.87 | 7.15 | 2.0 | 1.0 | 3.0 | −15 | Figure 16, Figure 23 | 3.65 | 11.5 | 1.2 | 0.5 | 4.3 |
| +15 | Figure 15, Figure 17, (Figure 18, Figure 19, Figure 22, Figure 25) | 7.87 | 7.15 | 3.3 | 1.0 | 3.0 | −28 | Figure 16, Figure 23 | 3.57 | 24.3 | 1.2 | 0.5 | 10 |
| +28 | Figure 15, Figure 17, (Figure 18, Figure 19, Figure 22, Figure 25) | 21.0 | 7.15 | 5.6 | 1.0 | 2.0 | −45 | Figure 21 | 3.57 | 41.2 | 2.2 | 10 | 33 |
| +45 | Figure 20 | 3.57 | 48.7 | 2.2 | 10 | 39 | −100 | Figure 21 | 3.57 | 97.6 | 2.2 | 10 | 91 |
| +75 | Figure 20 | 3.57 | 78.7 | 2.2 | 10 | 68 | −250 | Figure 21 | 3.57 | 249 | 2.2 | 10 | 240 |

(1) Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.
(2) Replace R1/R2 in figures with divider shown in Figure 26.
(3) $V^+$ and $V_{CC}$ must be connected to a +3V or greater supply.

## Table 2. Formulae for Intermediate Output Voltages

| Outputs from +2 to +7 volts | Outputs from +4 to +250 volts | Current Limiting |
|---|---|---|
| (Figure 14, Figure 17, Figure 18, Figure 19, Figure 22, Figure 25) | (Figure 20) | |
| $V_{OUT} = \left(V_{REF} \times \frac{R2}{R1 + R2}\right)$ | $V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R2 - R1}{R1}\right)$; R3 = R4 | $I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$ |
| **Outputs from +7 to +37 volts** | **Outputs from −6 to −250 volts** | **Foldback Current Limiting** |
| (Figure 15, Figure 17, Figure 18, Figure 19, Figure 22, Figure 25) | (Figure 16, Figure 21, Figure 23) | $I_{KNEE} = \left(\frac{V_{OUT}\,R3}{R_{SC}\,R4} + \frac{V_{SENSE}\,(R3 + R4)}{R_{SC}\,R4}\right)$ |
| $V_{OUT} = \left(V_{REF} \times \frac{R1 + R2}{R2}\right)$ | $V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R1 + R2}{R1}\right)$; R3 = R4 | $I_{SHORT\ CKT} = \left(\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4}\right)$ |

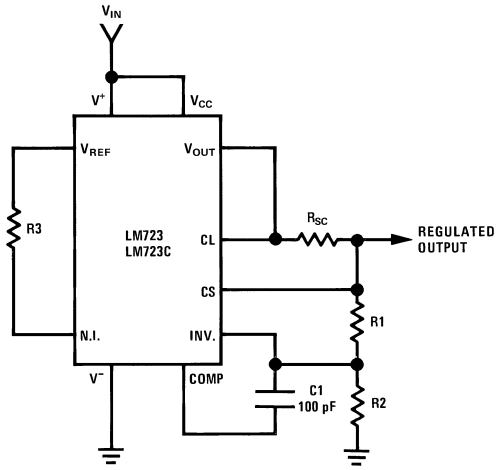
## TYPICAL APPLICATIONS




Note: R3 = $\frac{R1\,R2}{R1 + R2}$ for minimum temperature drift

**Figure 14. Basic Low Voltage Regulator ($V_{OUT}$ = 2 to 7 Volts)**

| Typical Performance | |
|---|---|
| Regulated Output Voltage | 5V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 0.5mV |
| Load Regulation ($\Delta I_L$ = 50 mA) | 1.5mV |




Note: R3 = $\frac{R1\,R2}{R1 + R2}$ for minimum temperature drift.
R3 may be eliminated for minimum component count.

**Figure 15. Basic High Voltage Regulator ($V_{OUT}$ = 7 to 37 Volts)**

| Typical Performance | |
|---|---|
| Regulated Output Voltage | 15V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 1.5 mV |
| Load Regulation ($\Delta I_L$ = 50 mA) | 4.5 mV |

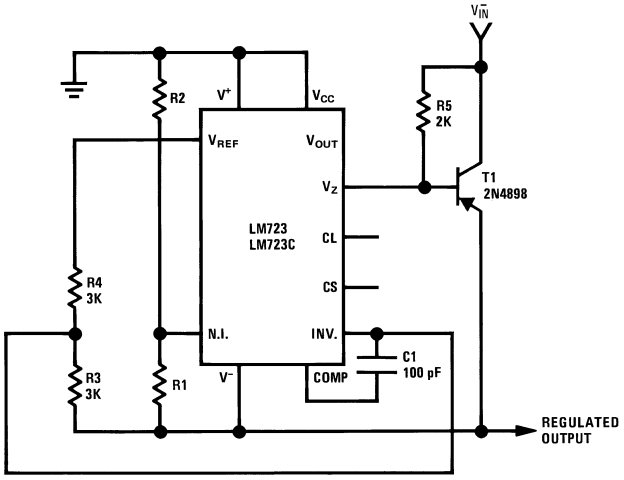



**Figure 16. Negative Voltage Regulator**

| Typical Performance | |
|---|---|
| Regulated Output Voltage | −15V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 1 mV |
| Load Regulation ($\Delta I_L$ = 100 mA) | 2 mV |

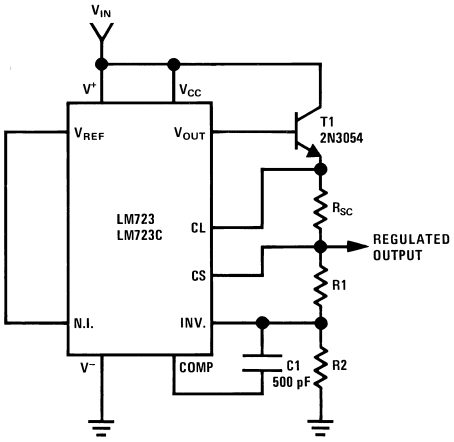



**Figure 17. Positive Voltage Regulator (External NPN Pass Transistor)**

| Typical Performance | |
|---|---|
| Regulated Output Voltage | +15V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 1.5 mV |
| Load Regulation ($\Delta I_L$ = 1A) | 15 mV |

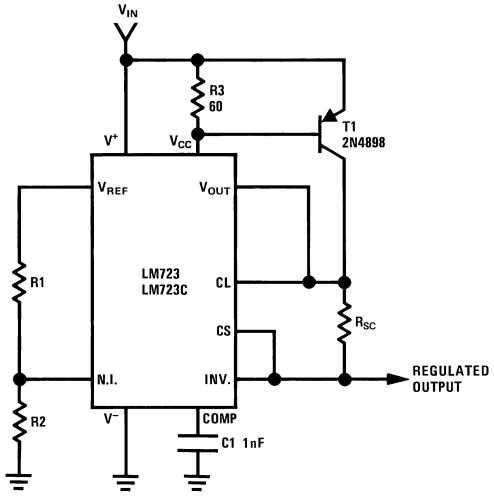



**Figure 18. Positive Voltage Regulator (External PNP Pass Transistor)**

| Typical Performance | |
|---|---|
| Regulated Output Voltage | +5V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 0.5 mV |
| Load Regulation ($\Delta I_L$ = 1A) | 5 mV |

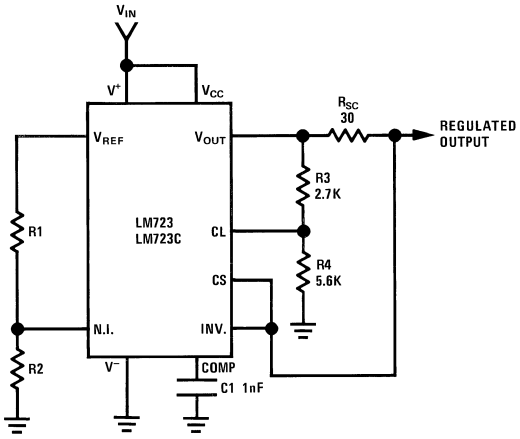



**Figure 19. Foldback Current Limiting**

| Typical Performance | |
|---|---|
| Regulated Output Voltage | +5V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 0.5 mV |
| Load Regulation ($\Delta I_L$ = 10 mA) | 1 mV |
| Short Circuit Current | 20 mA |

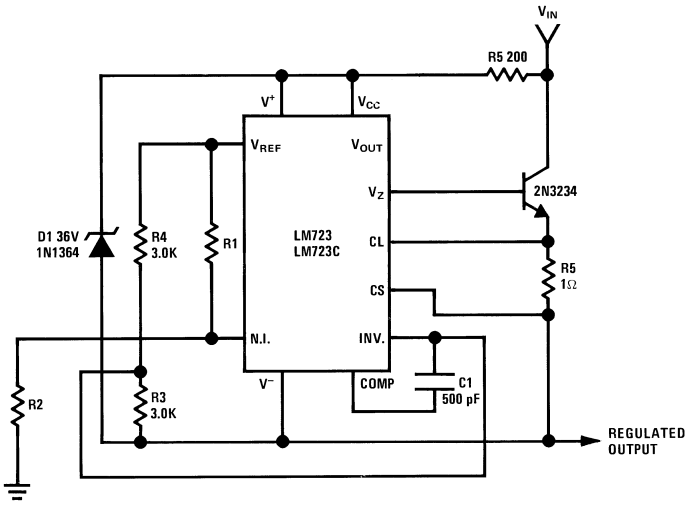



**Figure 20. Positive Floating Regulator**

| Typical Performance | |
|---|---|
| Regulated Output Voltage | +50V |
| Line Regulation ($\Delta V_{IN}$ = 20V) | 15 mV |
| Load Regulation ($\Delta I_L$ = 50 mA) | 20 mV |

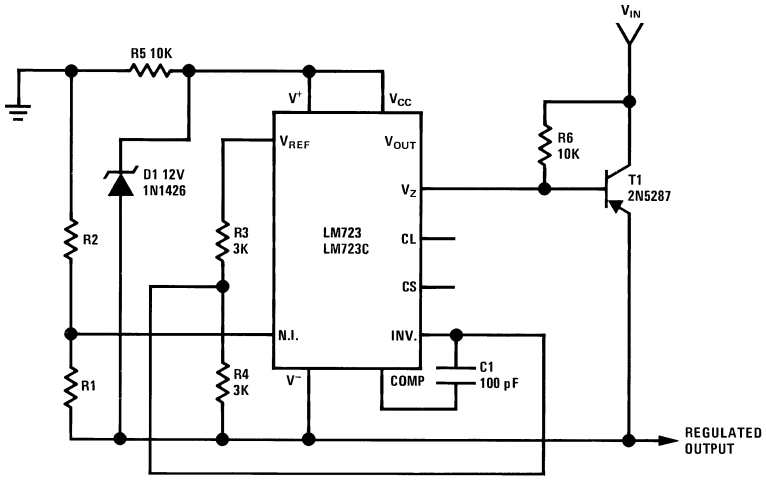
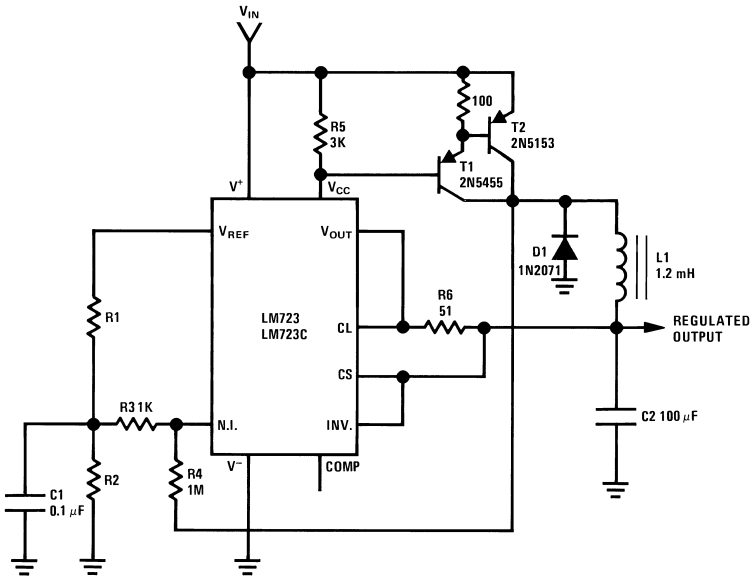



**Figure 21. Negative Floating Regulator**

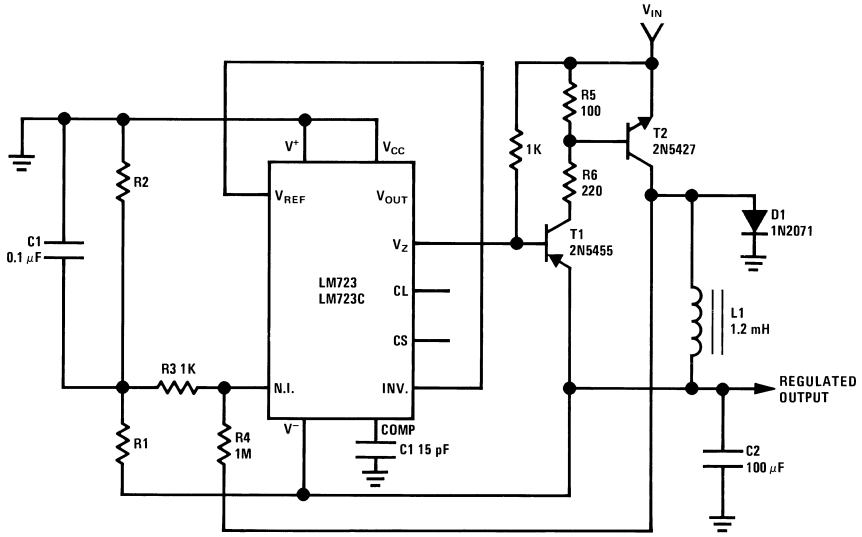
| Typical Performance | |
|---|---|
| Regulated Output Voltage | −100V |
| Line Regulation ($\Delta V_{IN}$ = 20V) | 30 mV |
| Load Regulation ($\Delta I_L$ = 100 mA) | 20 mV |




$L_1$ is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

**Figure 22. Positive Switching Regulator**

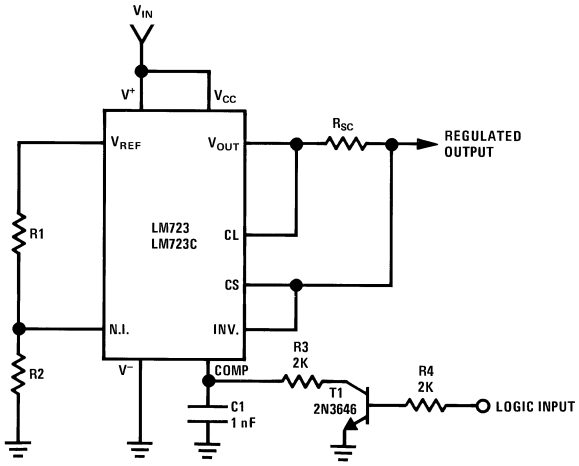
| Typical Performance | |
|---|---|
| Regulated Output Voltage | +5V |
| Line Regulation ($\Delta V_{IN}$ = 30V) | 10 mV |
| Load Regulation ($\Delta I_L$ = 2A) | 80 mV |




$L_1$ is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

**Figure 23. Negative Switching Regulator**

| Typical Performance | |
|---|---|
| Regulated Output Voltage | −15V |
| Line Regulation ($\Delta V_{IN}$ = 20V) | 8 mV |
| Load Regulation ($\Delta I_L$ = 2A) | 6 mV |




**Note:** Current limit transistor may be used for shutdown if current limiting is not required.

**Figure 24. Remote Shutdown Regulator with Current Limiting**

| Typical Performance | |
|---|---|
| Regulated Output Voltage | +5V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 0.5 mV |
| Load Regulation ($\Delta I_L$ = 50 mA) | 1.5 mV |

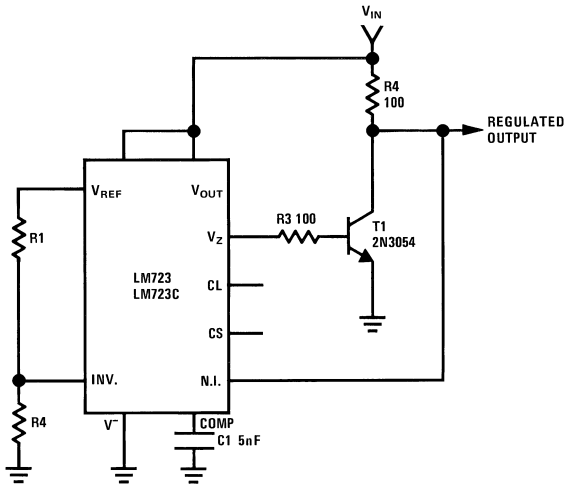
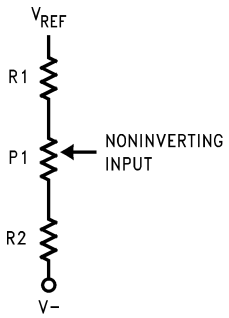



**Figure 25. Shunt Regulator**

| | |
|---|---|
| Regulated Output Voltage | +5V |
| Line Regulation ($\Delta V_{IN}$ = 10V) | 0.5 mV |
| Load Regulation ($\Delta I_L$ = 100 mA) | 1.5 mV |




NOTE: Replace R1/R2 in figures with divider shown in Figure 26

**Figure 26. Output Voltage Adjust**

## REVISION HISTORY SECTION

| Date Released | Revision | Section | Originator | Changes |
|---|---|---|---|---|
| 02/15/05 | A | New Release, Corporate format | L. Lytle | 1 MDS data sheet converted into one Corp. data sheet format. MJLM723-X, Rev. 1A0. MDS data sheet will be archived. |
| 03/25/2013 | A | All Sections | | Changed layout of National Data Sheet to TI format |

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| JL723SCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | JL723SCA JM38510/10201SCA Q |
| JL723SIA | Active | Production | TO-100 (LME) \| 10 | 20 \| TRAY NON-STD | No | Call TI | Level-1-NA-UNLIM | -55 to 125 | JL723SIA JM38510/10201SIA Q ACO JM38510/10201SIA Q >T |
| JM38510/10201SCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | JL723SCA JM38510/10201SCA Q |
| JM38510/10201SIA | Active | Production | TO-100 (LME) \| 10 | 20 \| TRAY NON-STD | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | JL723SIA JM38510/10201SIA Q ACO JM38510/10201SIA Q >T |
| M38510/10201SCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | JL723SCA JM38510/10201SCA Q |
| M38510/10201SIA | Active | Production | TO-100 (LME) \| 10 | 20 \| TRAY NON-STD | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | JL723SIA JM38510/10201SIA Q ACO JM38510/10201SIA Q >T |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

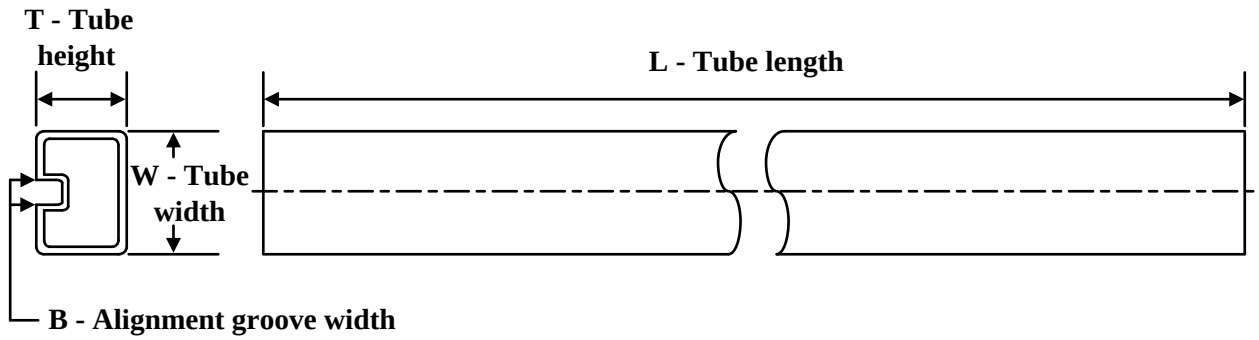
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

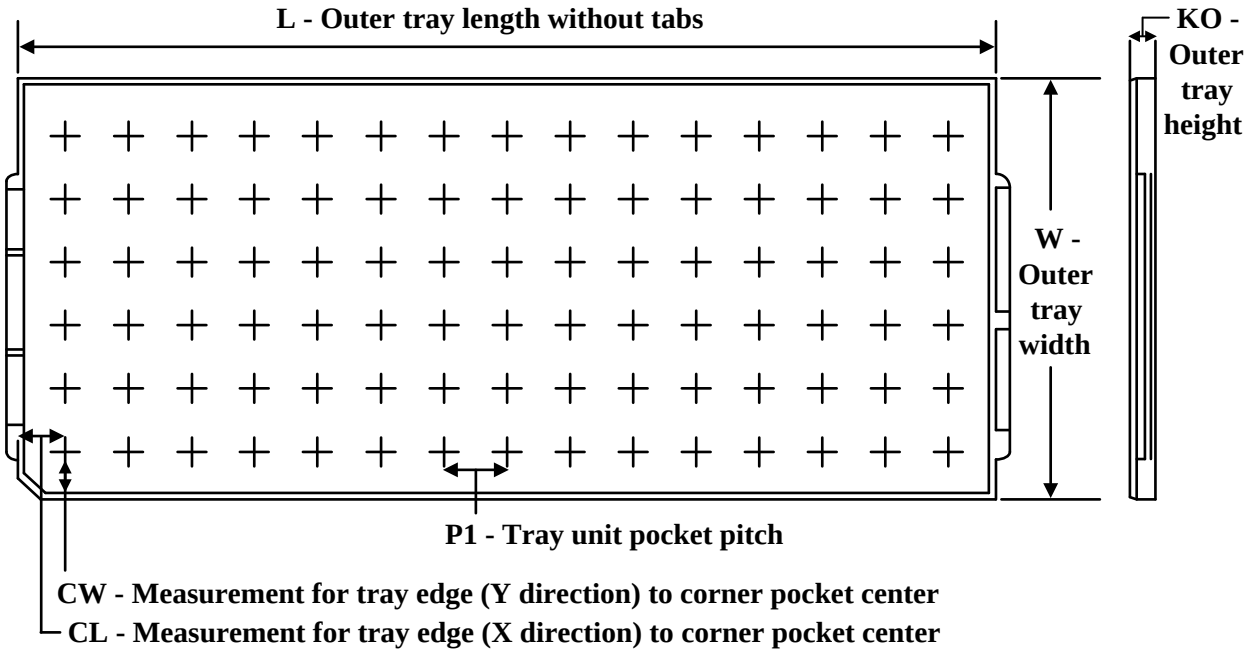
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| JL723SCA | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| JM38510/10201SCA | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| M38510/10201SCA | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

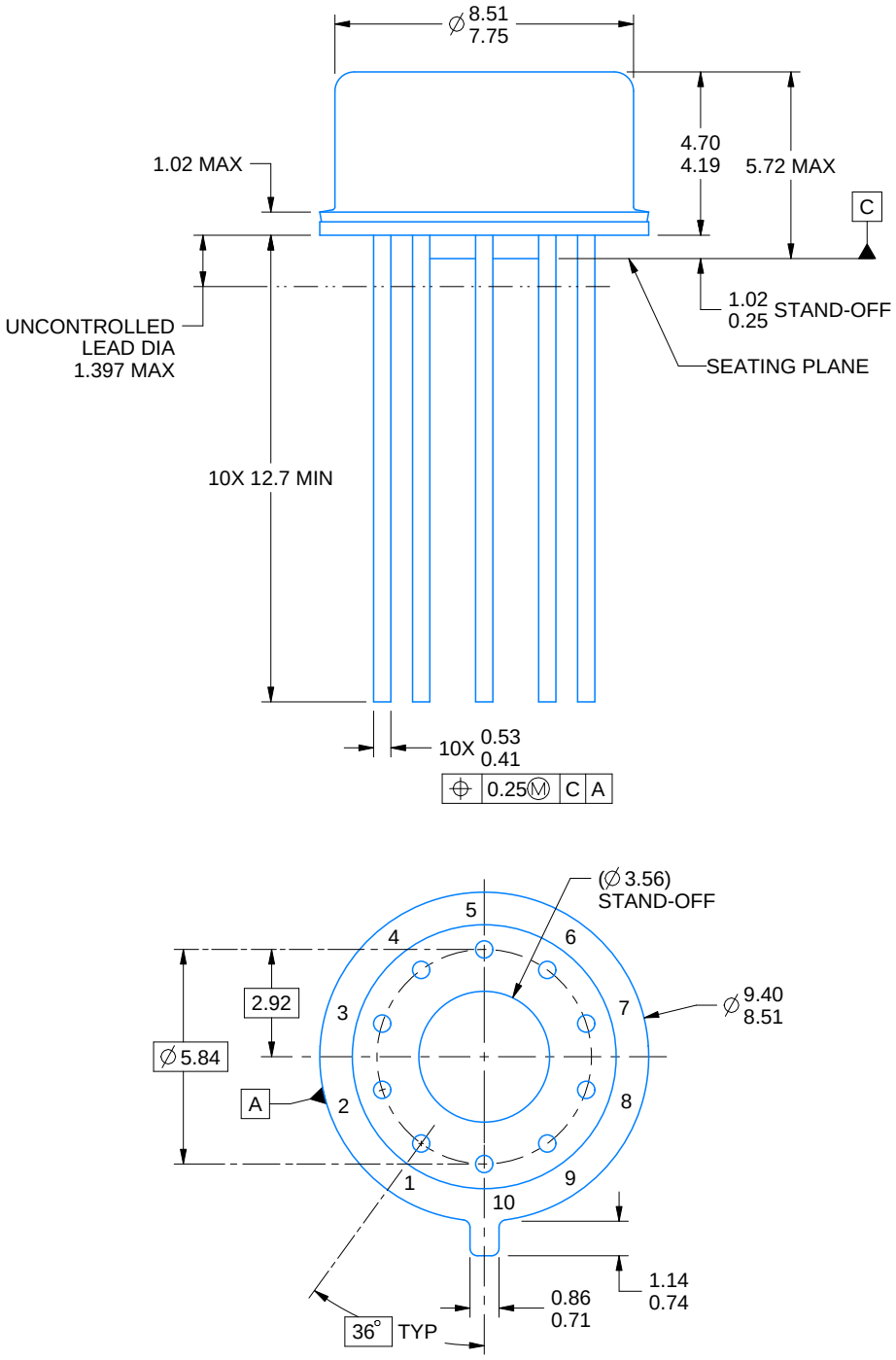
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| JL723SIA | LME | TO-CAN | 10 | 20 | 2 X 10 | 150 | 126.49 | 61.98 | 8890 | 11.18 | 12.95 | 18.54 |
| JM38510/10201SIA | LME | TO-CAN | 10 | 20 | 2 X 10 | 150 | 126.49 | 61.98 | 8890 | 11.18 | 12.95 | 18.54 |
| M38510/10201SIA | LME | TO-CAN | 10 | 20 | 2 X 10 | 150 | 126.49 | 61.98 | 8890 | 11.18 | 12.95 | 18.54 |

# PACKAGE OUTLINE

## LME0010A

## TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE




4220604/B 09/2024

NOTES:

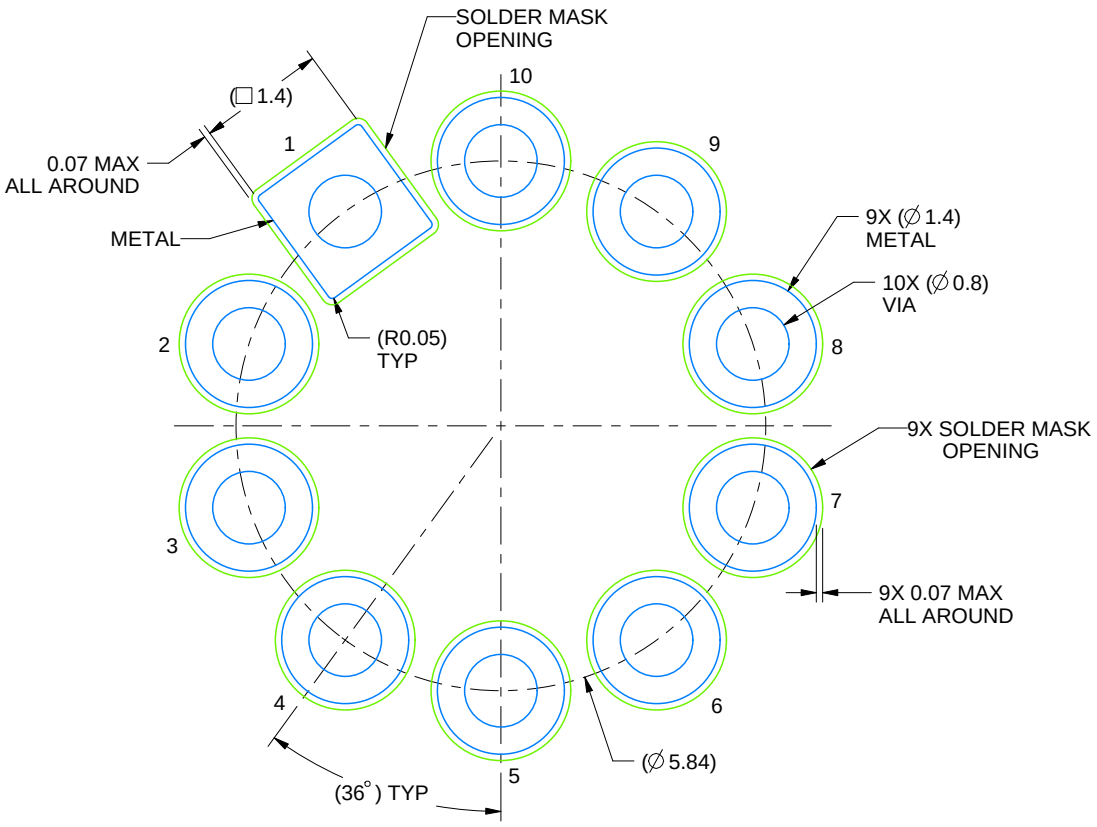
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-006/TO-100.

# EXAMPLE BOARD LAYOUT

## LME0010A

## TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



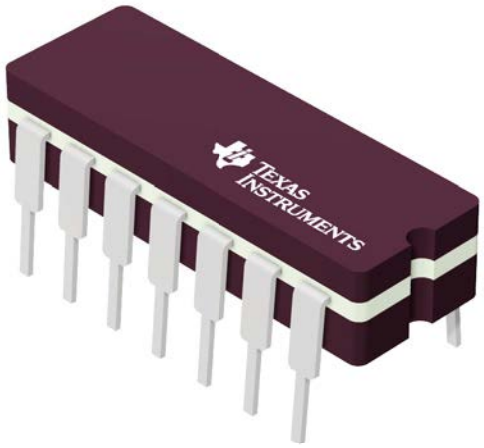

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220604/B 09/2024

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

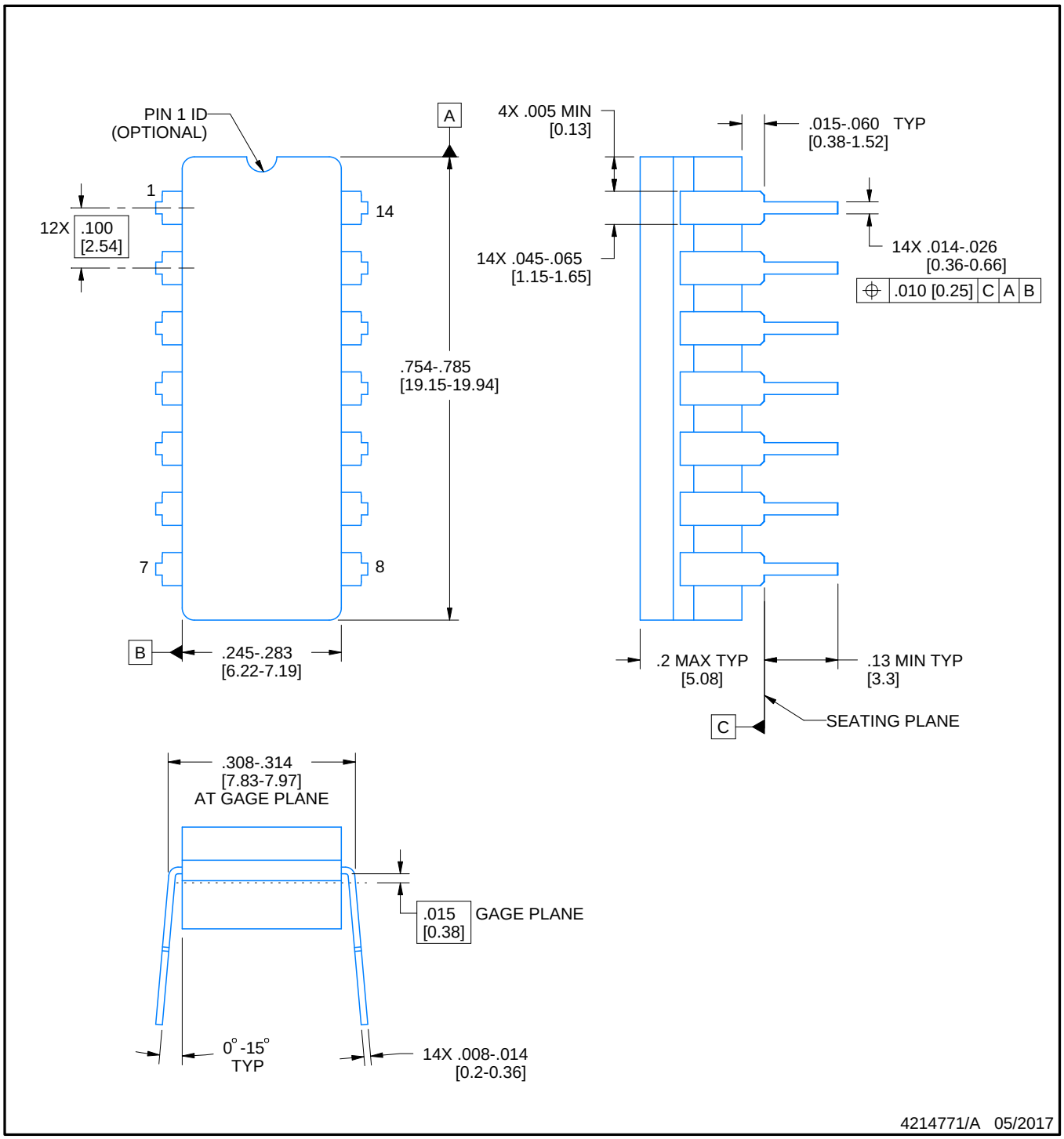
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

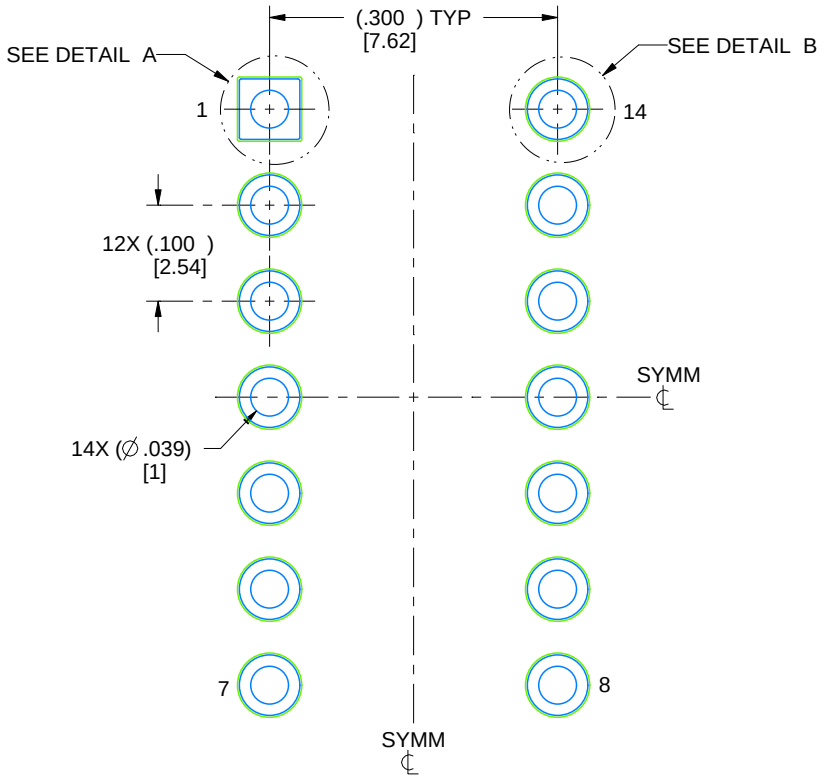
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

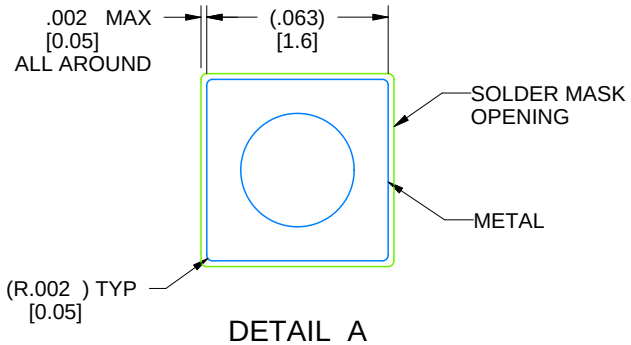
## J0014A

## CDIP - 5.08 mm max height

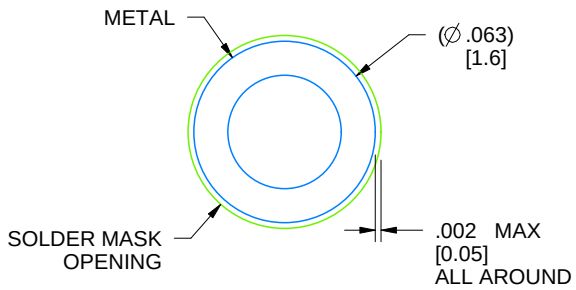
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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