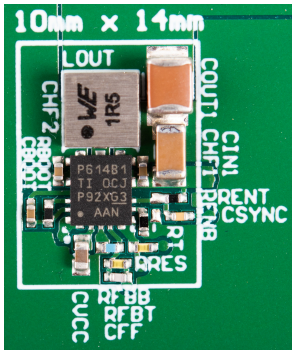
LM61430-Q1 3V 到 36V、3A、低 EMI 同步降压转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C 至 +150°C，T_J
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 针对超低 EMI 要求进行了优化
  - HotRod™ 封装可更大限度地减少开关节点振铃
  - 并行输入路径可更大限度减少寄生电感
  - 可调节 SW 节点上升时间
- 专为汽车应用而设计
  - 支持 42V 的汽车负载突降
  - ±1% 的总输出稳压精度
  - V_{OUT} 可在 1V 至 95% 的 V_{IN} 范围内调节
- 可在所有负载下进行高效电源转换
  - 在 13.5V_{IN}、3.3V_{OUT} 下具有 7µA 的无开关电流
  - 具有用于提升效率的外部偏置选项
- 适用于可扩展电源
  - 与以下器件引脚兼容：
    - LM61435-Q1（36V、3.5A、可调节 f_{sw}）
    - LM61440-Q1（36V、4A、可调节 f_{SW}）
    - LM61460-Q1（36V、6A、可调节 f_{SW}）

2 应用

- 汽车信息娱乐系统与仪表组： 音响主机、 媒体集线器、 USB 充电器、 显示屏
- 汽车 ADAS 和车身电子装置



解决方案总尺寸

3 说明

LM61430-Q1 是一款高性能直流/直流同步降压转换器。该器件具有集成式高侧和低侧 MOSFET，能够在 3.0V 至 36V 的宽输入电压范围内提供高达 3A 的输出电流；可耐受 42V 电压，简化了输入涌流保护设计。LM61430-Q1 可对压降进行软恢复，因此无需对输出进行过冲。

LM61430-Q1 专门设计用于降低 EMI。该器件具有可调节 SW 节点上升时间和低 EMI，并采用具有低开关节点振铃和易于使用、优化型引脚排列的 VQFN-HR 封装。开关频率可在 200kHz 至 2.2MHz 范围内设置或同步，从而避开噪声敏感频段。另外，可以选择频率，从而在低工作频率下提高效率，或在高工作频率下缩小解决方案尺寸。

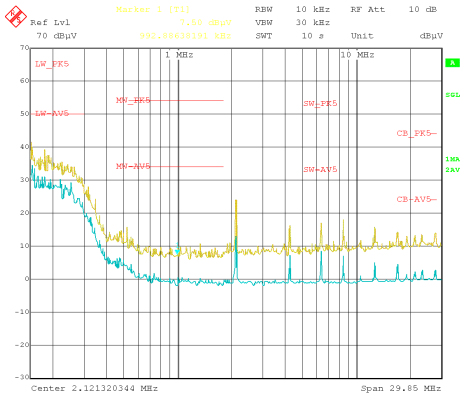
自动模式可在轻负载运行时进行频率折返，实现仅 7µA（典型值）的空载电流消耗和高轻负载效率。PWM 和 PFM 模式之间无缝转换，以及超低的 MOSFET 导通电阻和外部偏置输入，均确保在整个负载范围内实现卓越的效率。

电气特性额定结温范围为 –40°C 至 +150°C。如需其他资源，请参阅*相关文档*。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
LM61430-Q1	VQFN-HR (14)	4.00mm × 3.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



传导 EMI：，V_{OUT} = 5V，F_{SW} = 2100 kHz

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

DATE	REVISION	NOTES
October 2021	*	Initial release

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5 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	REFERENCE PART NUMBER	LIGHT LOAD MODE	Spread Spectrum	OUTPUT VOLTAGE	SWITCHING FREQUENCY
LM61430-Q1	LM61430AASQRJRRQ1	LM61430AAS-Q1	AUTO Mode	Yes	Adjustable	Adjustable
LM61430-Q1	LM61430AFSQRJRRQ1	LM61430AFS-Q1	FPWM	Yes	Adjustable	Adjustable

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6 Pin Configuration and Functions

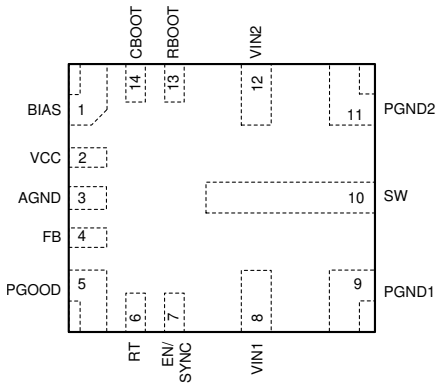


图 6-1. RJR Package 14-Pin VQFN-HR (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BIAS	1	P	Input to internal LDO. Connect to an output voltage point to improve efficiency. Connect an optional high quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity. If output voltage is above 12 V, connect this pin to ground.
VCC	2	O	Internal LDO output. Used as supply to internal control circuits. Do not connect to any external loads. Connect a high-quality 1-µF capacitor from this pin to AGND.
AGND	3	G	Analog ground for internal circuitry. Feedback and VCC are measured with respect to this pin. Must connect AGND to both PGND1 and PGND2 on the PCB.
FB	4	I	Output voltage feedback input to the internal control loop. Connect to the feedback divider tap point for adjustable output voltage. Do not float or connect to ground.
PGOOD	5	O	Open-drain power-good status output. Pull this pin up to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault. PGOOD output goes low when EN = low, V_{IN} > 1 V.
RT	6	I/O	Connect this pin to ground through a resistor with value between 5.76 kΩ and 66.5 kΩ to set switching frequency between 200 kHz and 2200 kHz. Do not float or connect to ground.
EN/SYNC	7	I	Precision enable input. High = on, Low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. See 节 9. Do not float. EN/SYNC also functions as a synchronization input pin. Used to synchronize the device switching frequency to a system clock. Triggers on rising edge of external clock. A capacitor can be used to AC couple the synchronization signal to this pin. When synchronized to an external clock, the device functions in forced PWM and disables the PFM light-load efficiency mode. See 节 8.
VIN1	8	P	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2.
PGND1	9	G	Power ground to the internal low-side MOSFET. Connect to system ground. Low impedance connection should be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
SW	10	O	Switch node of the converter. Connect to the output inductor.
PGND2	11	G	Power ground to the internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
VIN2	12	P	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Low impedance connection must be provided to VIN1.
RBOOT	13	I/O	Connect to CBOOT through a resistor. This resistance must be between 0 Ω and open and determines SW node rise time.
CBOOT	14	I/O	High-side driver upper supply rail. Connect a 100-nF capacitor between SW pin and CBOOT. An internal diode connects to VCC and allows CBOOT to charge while the SW node is low.

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40℃ to +150℃ (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Input voltage	VIN1, VIN2 to AGND, PGND	-0.3	42	V
	RBOOT to SW	-0.3	5.5	V
	CBOOT to SW	-0.3	5.5	V
	BIAS to AGND, PGND	-0.3	16	V
	EN/SYNC to AGND, PGND	-0.3	42	V
	RT to AGND, PGND	-0.3	5.5	V
	FB to AGND, PGND	-0.3	16	V
	PGOOD to AGND, PGND	0	20	V
	PGND to AGND(3)	-1	2	V
Output voltage	SW to AGND, PGND(2)	-0.3	V_{IN}+0.3	V
	VCC to AGND, PGND	-0.3	5.5	V
Current	PGOOD sink current(4)		10	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-40	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) A voltage of 2 V below GND and 2 V above V_{IN} can appear on this pin for ≤ 200 ns with a duty cycle of ≤ 0.01%.
(3) This specification applies to voltage durations of 100 ns or less. The maximum D.C. voltage should not exceed ± 0.3 V.
(4) Do not exceed the voltage rating of the pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) Device HBM Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 Device CDM Classification Level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
Input voltage	Input voltage range after start-up	3		36	V
Output voltage	Output voltage range for adjustable version (2)	1		0.95 × V_{IN}	V
Frequency	Frequency adjustment range	200		2200	kHz
Sync frequency	Synchronization frequency range	200		2200	kHz
Load current	Output DC current range (3)	0		3	A
Temperature	Operating junction temperature T_J range	-40		150	°C

(1) Recommended operating conditions are conditions under the device is intended to be functional. For specifications and test conditions see the *Electrical Characteristics* table.
(2) Under no conditions should the output voltage be allowed to fall below zero volts.
(3) Maximum continuous DC current may be derated when operating with high switching frequency, high ambient temperature, or both. See 节 9 for details.

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7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, with a 4-layer PCB, a $R_{\Theta JA}$ = 25℃/W can be achieved.

THERMAL METRIC (1) (2)		LM61430-Q1 RJR (QFN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is converter output voltage.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
$V_{IN_OPERATE}$	Input operating voltage(2)	Needed to start up	3.95			V
		Once operating	3.0			
$V_{IN_OPERATE_H}$	Hysteresis(2)			1		V
I_{Q_VIN}	Operating quiescent current (not switching)	V_{FB} = +5%, V_{BIAS} = 5 V		9	18	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	EN = 0 V, T_J = 25℃		0.6	6	µA
ENABLE						
V_{EN}	Enable input threshold voltage – rising			1.263		V
$V_{EN\text{-}ACC}$	Enable input threshold voltage – rising deviation from typical		–5%		5%	
$V_{EN\text{-}HYST}$	Enable threshold hysteresis as percentage of V_{EN} (TYP)		24%	28%	32%	
$V_{EN\text{-}WAKE}$	Enable wake-up threshold		0.4			V
I_{EN}	Enable pin input current	V_{IN} = EN = 13.5 V		2.3		µA
V_{EN_SYNC}	Edge height necessary to sync using EN/SYNC pin	Rise/fall time < 30 ns			2.4	V
LDO – VCC						
V_{CC}	Internal V_{CC} voltage	V_{BIAS} > 3.4 V, CCM operation(2)		3.3		V
		V_{BIAS} = 3.1 V, nonswitching		3.1		
V_{CC_UVLO}	Internal V_{CC} input undervoltage lockout	V_{CC} rising undervoltage threshold		3.6		V
$V_{CC_UVLO_HYST}$	Internal V_{CC} input under voltage lockout	Hysteresis below V_{CC_UVLO}		1.1		V

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Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is converter output voltage.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FEEDBACK						
V_{FB_acc}	Initial reference voltage accuracy	V_{IN} = 3.3 V to 36 V, FPWM Mode	–1%		1%	
I_{FB}	Input current from FB to AGND	Adjustable versions only, FB = 1 V		10		nA
OSCILLATOR						
f_{ADJ}	Minimum adjustable frequency by R_T or SYNC	RT = 66.5 kΩ	0.18	0.2	0.22	MHz
	Adjustable frequency by R_T or SYNC with 400-kHz setting	RT = 33.2 kΩ	0.36	0.4	0.44	MHz
	Maximum adjustable frequency by R_T or SYNC	RT = 5.76 kΩ	1.98	2.2	2.42	MHz
MOSFETS						
$R_{DS(ON)_HS}$	Power switch on-resistance	High-side MOSFET $R_{DS(ON)}$		41	82	mΩ
$R_{DS(ON)_LS}$	Power switch on-resistance	Low-side MOSFET $R_{DS(ON)}$		21	45	mΩ
V_{BOOT_UVLO}	Voltage on CBOOT pin compared to SW which will turn off high-side switch			2.1		V
CURRENT LIMITS						
I_{L-HS}	High-side switch current limit(1)	Duty cycle approaches 0%	4.4	5.2	6.05	A
I_{L-LS}	Low-side switch current limit		2.95	3.5	3.95	A
I_{L-ZC}	Zero-cross current limit. Positive current direction is out of SW pin	AUTO Mode, static measurement		0.25		A
I_{L-NEG}	Negative current limit FPWM and SYNC Modes. Positive current direction is out of SW pin.	FPWM operation		-2		A
$I_{PK_MIN_0}$	Minimum peak command in auto mode / device current rating	Pulse duration < 100 ns		25%		
$I_{PK_MIN_100}$	Minimum peak command in auto mode / device current rating	Pulse duration > 1 µs		12.5		%
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage	Not during soft start		40%		
POWER GOOD						
PGD_{OV}	PGOOD upper threshold - rising	% of V_{OUT} setting	105%	107%	110%	
$PGD_{U\ V}$	PGOOD lower threshold - falling	% of V_{OUT} setting	92%	94%	96.5%	
PGD_{HYST}	PGOOD upper threshold (rising and falling)	% of V_{OUT} setting		1.3%		
$V_{IN(PGD_VALID)}$	Input voltage for proper PGOOD function		1.0			V
$V_{PGD(LOW)}$	Low level PGOOD function output voltage	46-µA pullup to PGOOD pin, V_{IN} = 1.0 V, EN = 0 V			0.4	V
		1-mA pullup to PGOOD pin, V_{IN} = 13.5 V, EN = 0 V			0.4	
		2-mA pullup to PGOOD pin, V_{IN} = 13.5 V, EN = 3.3 V			0.4	
R_{PGD}	$R_{DS(ON)}$ of PGOOD output	1-mA pullup to PGOOD pin, EN = 0 V		17	40	Ω
		1-mA pullup to PGOOD pin, EN = 3.3 V		40	90	Ω
I_{OV}	Pulldown current at the SW node under overvoltage condition			0.5		mA

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Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is converter output voltage.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T_{SD_R}	Thermal shutdown rising threshold(2)		158	168	180	℃
T_{SD_HYST}	Thermal shutdown hysteresis(2)			10		℃

(1) High side current limit is a function of duty factor. High side current limit value is highest at small duty factor and less at higher duty factors.
(2) Parameter specified by design, statistical analysis and production testing of correlated parameters.

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7.6 Timing Characteristics

Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SWITCH NODE						
t_{ON_MIN}	Minimum HS switch on time	V_{IN} = 20 V, I_{OUT} = 2 A, RBOOT short to CBOOT		55	70	ns
t_{ON_MAX}	Maximum HS switch on time			9		µs
t_{OFF_MIN}	Minimum LS switch on time	V_{IN} = 4.0 V, I_{OUT} = 1 A, RBOOT short to CBOOT		65	85	ns
t_{SS}	Time from first SW pulse to V_{REF} at 90%	$V_{IN} \geqslant$ 4.2 V	3.5	5	7	ms
t_{SS2}	Time from first SW pulse to release of FPWM lockout if output not in regulation	$V_{IN} \geqslant$ 4.2 V	9.5	13	17	ms
t_W	Short circuit wait time ("Hiccup" time)			80		ms
ENABLE						
t_{EN}	Turn-on delay(1)	C_{VCC} = 1 µF, time from EN high to first SW pulse if output starts at 0 V		0.7		ms
t_B	Blanking of EN after rising or falling edges(1)		4		28	µs
t_{SYNC_EDGE}	Enable sync signal hold time after edge for edge recognition		100			ns
POWER GOOD						
$t_{PGDFLT(rise)}$	Delay time to PGOOD high signal		1.5	2	2.5	ms
$t_{PGDFLT(fall)}$	Glitch filter time constant for PGOOD function			120		µs

(1) Parameter specified using design, statistical analysis and production testing of correlated parameters; not tested in production.

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7.7 Systems Characteristics

The following values are specified by design provided that the component values in the typical application circuit are used. Limits apply over the junction temperature range of -40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are derived using test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is output setting. *These parameters are not tested in production.*

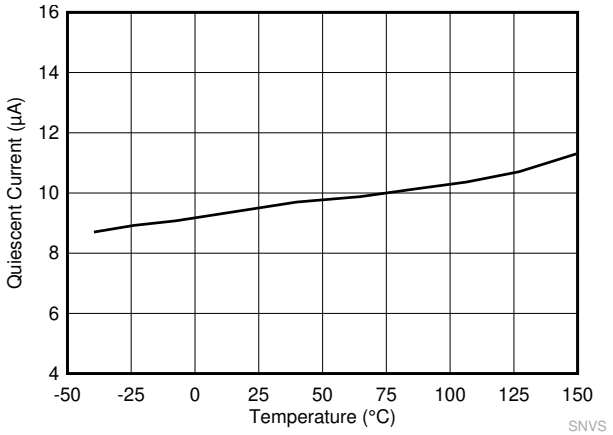
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EFFICIENCY						
η_{5V_2p1MHz}	Typical 2.1-MHz efficiency	V_{OUT} = 5 V, I_{OUT} = 3 A, R_{BOOT} = 0 Ω		93%		
		V_{OUT} = 5 V, I_{OUT} = 100 µA, R_{BOOT} = 0 Ω, R_{FBT} = 1 MΩ		73%		
RANGE OF OPERATION						
V_{VIN_MIN1}	V_{IN} for full functionality at reduced load, after start-up.	V_{OUT} set to 3.3 V	3.0			V
V_{VIN_MIN2}	V_{IN} for full functionality at 100% of maximum rated load, after start-up.	V_{OUT} set to 3.3 V	3.95			V
$I_{Q\text{-}VIN}$	Operating quiescent current(1)	V_{OUT} = 3.3 V, I_{OUT} = 0 A, auto mode, R_{FBT} = 1 MΩ		7		µA
		V_{OUT} = 5 V, I_{OUT} = 0 A, auto mode, R_{FBT} = 1 MΩ		10		
D_{MAX}	Maximum switch duty cycle	f_{SW} =1.85 MHz		87%		
		While in frequency fold back	98%			
RBOOT						
t_{RISE}	SW node rise time	R_{BOOT} = 0 Ω, I_{OUT} = 2 A (10% to 80%)		2.15		ns
		R_{BOOT} = 100 Ω, I_{OUT} = 2 A (10% to 80%)		2.7		ns

(1) See 节 8 for the meaning of this specification and how it can be calculated.

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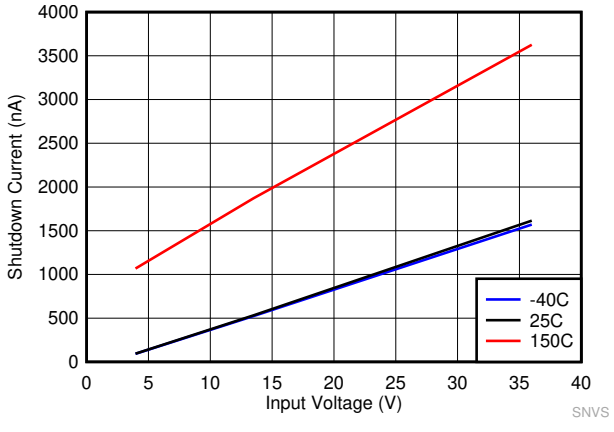
7.8 Typical Characteristics

Unless otherwise specified, V_{IN} = 13.5 V and f_{SW} = 400 kHz.



V_{BIAS} = 5 V

图 7-1. Nonswitching Input Supply Current



V_{EN} = 0 V

图 7-2. Shutdown Supply Current

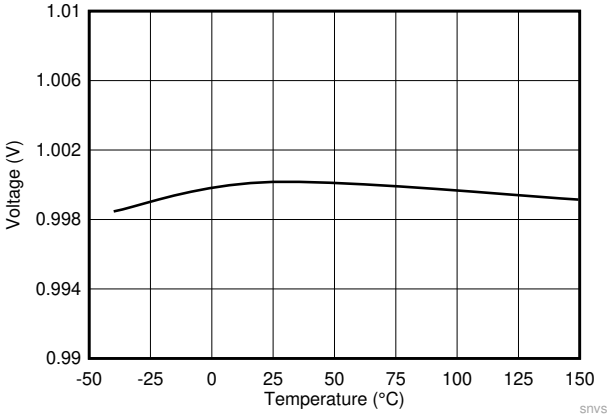


图 7-3. Feedback Voltage

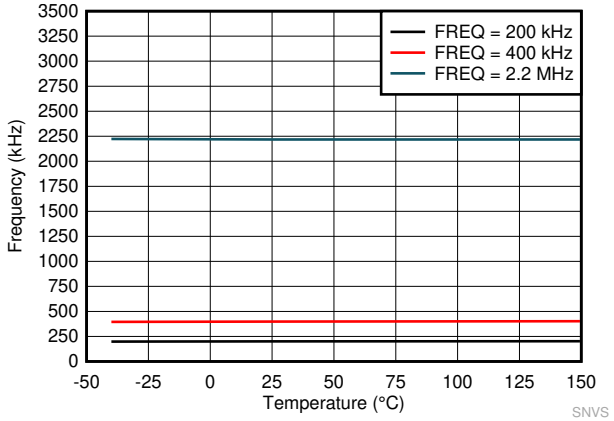


图 7-4. Switching Frequency Set by RT Resistor

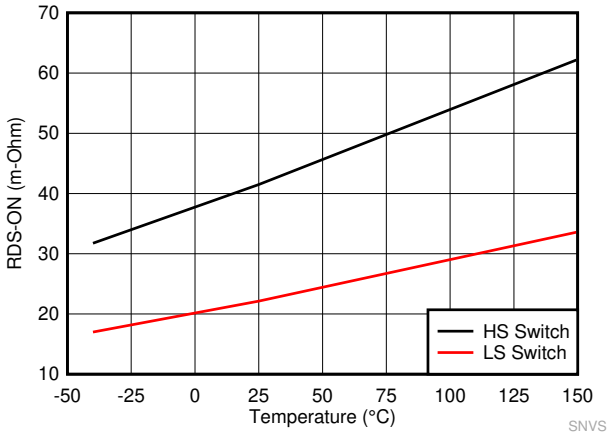


图 7-5. High-Side and Low-Side Switches R_{DS_ON}

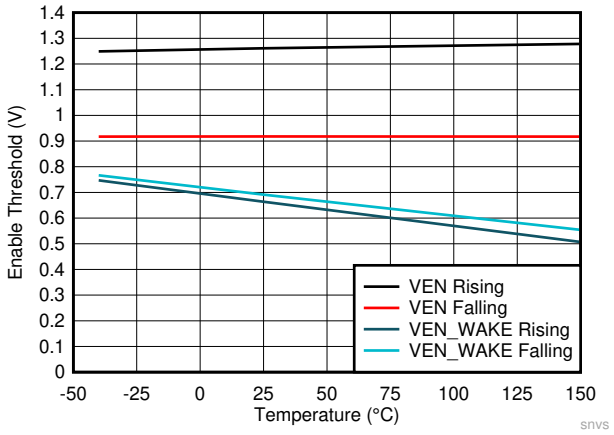


图 7-6. Enable Thresholds

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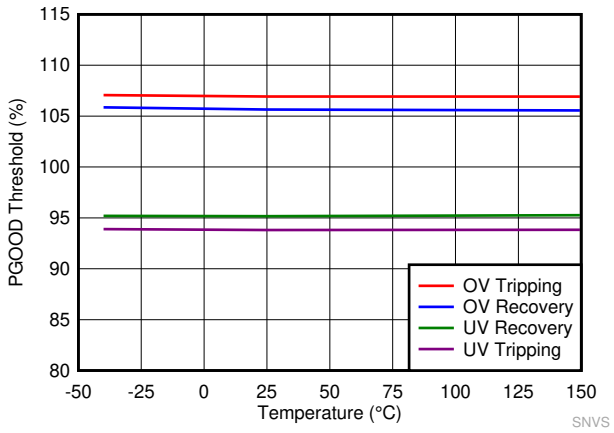


图 7-7. PGOOD Thresholds

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8 Detailed Description

8.1 Overview

The LM61430-Q1 is a wide input, synchronous peak-current mode buck regulator designed for a wide variety of industrial applications. The regulator can operate over a wide range of switching frequencies including sub-AM band at 400 kHz and above the AM band at 2.1 MHz. This device operates over a wide range of conversion ratios. If minimum on time or minimum off time does not support the desired conversion ratio, frequency is reduced automatically, allowing output voltage regulation to be maintained during input voltage transients with a high operating-frequency setting.

The LM61430-Q1 has been designed for low EMI and is optimized for both above and below AM band operation:

- HotRod package minimizes switch node ringing
- Parallel input path minimizes parasitic inductance
- Adjustable SW node rise time

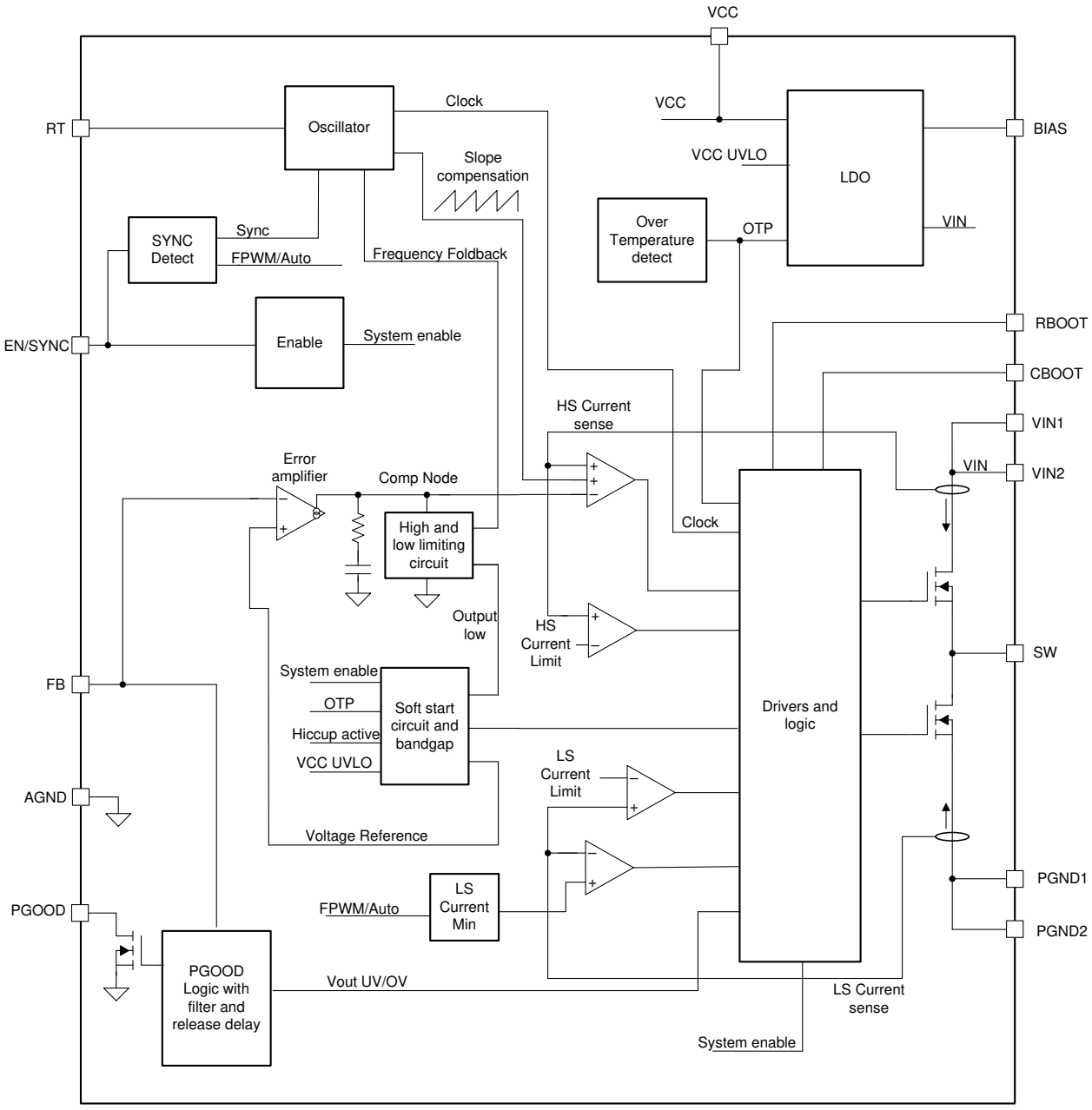
These features together can eliminate shielding and other expensive EMI mitigation measures.

This device is designed to minimize end-product cost and size while operating in demanding high-performance industrial environments. The LM61430-Q1 can be set to operate in the range of 200 kHz through 2.2 MHz using its RT pin. Operation at 2.1 MHz allows for the use of small passive components. The current limit function allows the use of inductors that are optimized for 3-A regulators. In addition, this device has low unloaded current consumption, desirable for off-battery, always on applications. The low shutdown current and high maximum operating voltage also allows for the elimination of an external load switch and input transient protection. To further reduce system cost, an advanced PGOOD output is provided, which can often eliminate the use of an external reset or supervisory device.

The LM61430-Q1 devices are AEC-Q100 qualified and have electrical characteristics specified up to a maximum junction temperature of 150°C.

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8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 EN/SYNC Uses for Enable and V_{IN} UVLO

Start-up and shutdown are controlled by the EN/SYNC input and V_{IN} UVLO. For the device to remain in shutdown mode, apply a voltage below V_{EN_WAKE} (0.4 V) to the EN/SYNC pin. In shutdown mode, the quiescent current drops to 0.6 µA (typical). At a voltage above V_{EN_WAKE} and below V_{EN}, VCC is active and the SW node is inactive. Once the EN voltage is above V_{EN}, the chip begins to switch normally provided the input voltage is above 3 V.

The EN/SYNC pin cannot be left floating. The simplest way to enable the operation is to connect the EN/SYNC pin to V_{IN}, which allows self-start-up of the LM61430-Q1 when V_{IN} drives the internal VCC above its UVLO level. However, many applications benefit from the employment of an enable divider network as shown in 图 8-1, which establishes a precision input undervoltage lockout (UVLO). This can be used for sequencing, to prevent re-triggering the device when used with long input cables, or to reduce the occurrence of deep discharge of a battery power source. Note that the precision enable threshold V_{EN} has a 5% tolerance. Hysteresis must be enough to prevent re-triggering. External logic output of another IC can also be used to drive the EN/SYNC pin, allowing system power sequencing.

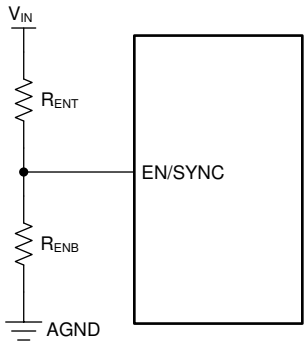


图 8-1. VIN UVLO Using the EN pin

Resistor values can be calculated using 方程式 1. See 节 9.2.2.11 for additional information.

$$R_{ENB} = R_{ENT} \cdot \frac{V_{EN}}{V_{ON} - V_{EN}} \tag{1}$$

where

- V_{ON} = Desired typical start-up input voltage for the circuit being designed

Note that since the EN/SYNC pin can also be used as an external synchronization clock input. A blanking time, t_B, is applied to the enable logic after a clock edge is detected. Any logic change within the blanking time is ignored. Blanking time is not applied when the device is in shutdown mode. The blanking time ranges from 4 µs to 28 µs. To effectively disable the output, the EN/SYNC input must stay low for longer than 28 µs.

8.3.2 EN/SYNC Pin Uses for Synchronization

The LM61430-Q1 EN/SYNC pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive clock edge into the EN pin, as shown in 图 8-2. It is recommended to keep the parallel combination value of R_{ENT} and R_{ENB} in the 100-kΩ range. R_{ENT} is required for synchronization, but R_{ENB} can be left unmounted. Switching action can be synchronized to an external clock ranging from 200 kHz to 2.2 MHz. The external clock must be off before start-up to allow proper start-up sequencing.

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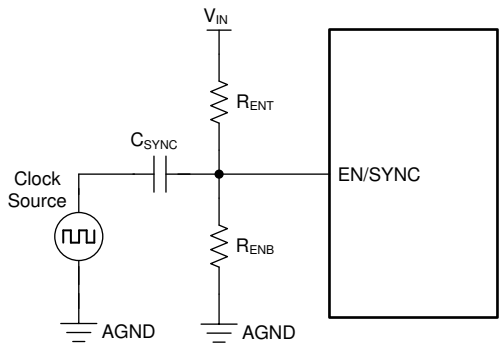


图 8-2. Typical Implementation Allowing Synchronization Using the EN Pin

Referring to 图 8-3, the AC-coupled voltage edge at the EN pin must exceed the SYNC amplitude threshold, $V_{EN_SYNC_MIN}$, to trip the internal synchronization pulse detector. In addition, the minimum EN/SYNC rising pulse and falling pulse durations must be longer than $t_{SYNC_EDGE(MIN)}$ and shorter than the blanking time t_B. A 3.3-V or higher amplitude pulse signal coupled through a 1-nF capacitor, C_{SYNC}, is suggested.

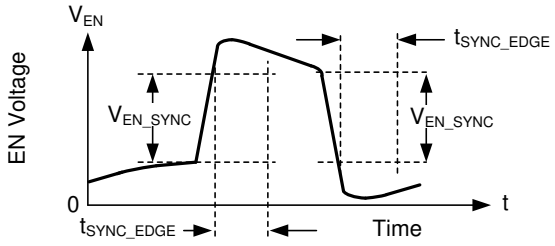


图 8-3. Typical SYNC/EN Waveform

After a valid synchronization signal is applied for 2048 cycles, the clock frequency abruptly changes to that of the applied signal.

8.3.3 Clock Locking

Once a valid synchronization signal is detected, a clock locking procedure is initiated. LM61430-Q1 devices receive this signal over the EN/SYNC pin. After approximately 2048 pulses, the clock frequency changes to the frequency of the synchronization signal. Note that while the frequency is adjusted suddenly, phase is maintained so the clock cycle that lies between operation at the default frequency and at the synchronization frequency is of intermediate length. This eliminates very long or very short pulses. Once frequency is adjusted, phase is adjusted over a few tens of cycles so that rising synchronization edges correspond to rising SW node pulses. See 图 8-4.

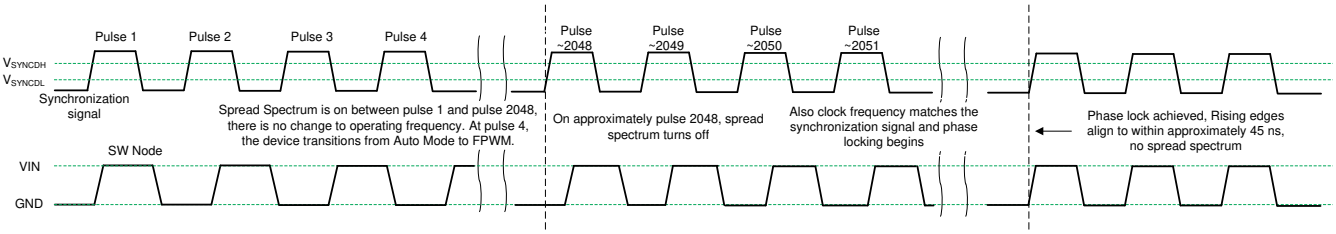


图 8-4. Synchronization Process

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8.3.4 Adjustable Switching Frequency

A resistor tied from the device RT pin to AGND is used to set operating frequency. Use 方程式 2 or refer to 图 8-5 for resistor values. Note that a resistor value outside of the recommended range can cause the device to shut down. This prevents unintended operation if RT pin is shorted to ground or left open. Do not apply a pulsed signal to this pin to force synchronization. If synchronization is needed, refer to 节 8.3.2.

$$R_{RT}(k\Omega) = (1 / f_{SW}(kHz) - 3.3 \times 10^{-5}) \times 1.346 \times 10^{4} \quad (2)$$

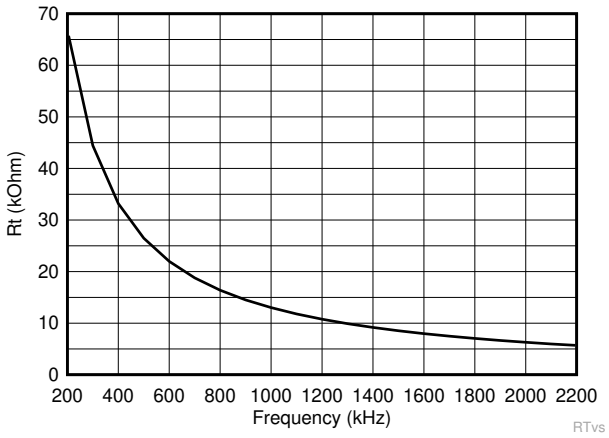


图 8-5. Setting Clock Frequency

8.3.5 PGOOD Output Operation

The PGOOD function is implemented to replace a discrete reset device, reducing BOM count and cost. The PGOOD pin voltage goes low when the feedback voltage is outside of the specified PGOOD thresholds (see 图 7-7). This can occur in current limit and thermal shutdown, as well as while disabled and during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. Output voltage excursions that are shorter than t_{PGDFLT_FALL} do not trip the power-good flag. Power-good operation can be best understood by referring to 图 8-6.

The power-good output consists of an open-drain NMOS; requiring an external pullup resistor to a suitable logic supply or V_{OUT}. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ⩾ 1 V (typical).

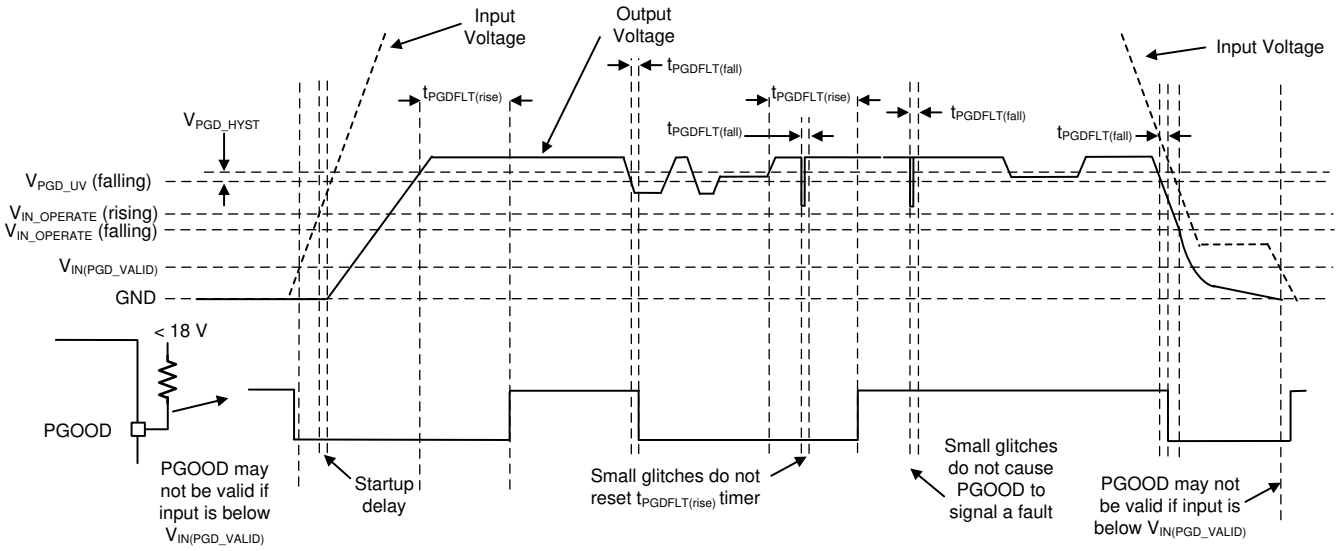


图 8-6. PGOOD Timing Diagram (Excludes OV Events)

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表 8-1. Conditions That Cause PGOOD to Signal a Fault (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH $t_{PGDFLT(rise)}$ MUST PASS BEFORE PGOOD OUTPUT IS RELEASED)(1)
$V_{OUT} < V_{OUT-target} \times PGD_{UV}$ AND $t > t_{PGDFLT(fall)}$	Output voltage in regulation: $V_{OUT-target} \times (PGD_{UV} + PGD_{HYST}) < V_{OUT} < V_{OUT-target} \times (PGD_{OV} - PGD_{HYST})$ (See 图 7-7.)
$V_{OUT} > V_{OUT-target} \times PGD_{OV}$ AND $t > t_{PGDFLT(fall)}$	Output voltage in regulation
$T_J > T_{SD_R}$	$T_J < T_{SD_F}$ AND output voltage in regulation
EN < V_{EN} falling	EN > V_{EN} Rising AND output voltage in regulation
$V_{CC} < V_{CC_UVLO} - V_{CC_UVLO_HYST}$	$V_{CC} > V_{CC_UVLO}$ AND output voltage in regulation

(1) As an additional operational check, PGOOD remains low during soft start, defined as until the lesser of either full output voltage reached or t_{SS2} has passed since initiation.

8.3.6 Internal LDO, VCC UVLO, and BIAS Input

The VCC pin is the output of the internal LDO used to supply the control circuits of the LM61430-Q1. The nominal output is 3 V to 3.3 V. The BIAS pin is the input to the internal LDO. This input can be connected to V_{OUT} to provide the lowest possible input supply current. If the BIAS voltage is less than 3.1 V, VIN1 and VIN2 directly powers the internal LDO.

To prevent unsafe operation, VCC has a UVLO that prevents switching if the internal voltage is too low. See V_{CC_UVLO} and $V_{CC_UVLO_HYST}$ in the *Electrical Characteristics*. Note that these UVLO values and the dropout of the LDO are used to derive minimum $V_{IN_OPERATE}$ and $V_{IN_OPERATE_H}$ values.

8.3.7 Bootstrap Voltage and $V_{CBOOT-UVLO}$ (CBOOT Pin)

The driver of the high-side (HS) switch requires bias higher than V_{IN}. The capacitor, CBOOT, connected between CBOOT and SW works as a charge pump to boost voltage on the CBOOT pin to SW+VCC. A boot diode is integrated on the LM61430-Q1 die to minimize external component count. It is recommended that a 100-nF capacitor rated for 10-V or higher is used. The V_{BOOT_UVLO} threshold (2.1-V typical) is designed to maintain proper HS switch operation. If the CBOOT capacitor voltage drops below V_{BOOT_UVLO}, then the device initiates a charging sequence turning on the low-side switch before attempting to turn on the HS switch.

8.3.8 Adjustable SW Node Slew Rate

To allow optimization of EMI with respect to efficiency, the LM61430-Q1 is designed to allow a resistor to select the strength of the driver of the high-side FET during turn on. See 图 8-7. The current drawn through the RBOOT pin (the dotted loop) is magnified and drawn through from CBOOT (the dashed line). This current is used to turn on the high-side power MOSEFT.

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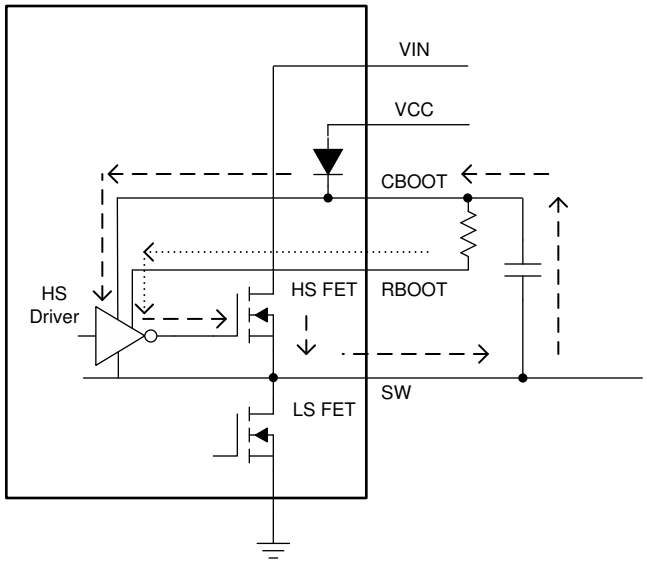


图 8-7. Simplified Circuit Showing How RBOOT Functions

With RBOOT short circuited to CBOOT, rise time is very fast. As a result, SW node harmonics do not "roll off" until above 150 MHz. A boot resistor of 100 Ω corresponds to approximately 2.7-ns SW node rise, and this 100-Ω boot resistor virtually eliminates SW node overshoot. The slower rise time allows energy in SW node harmonics to roll off near 100 MHz under most conditions. Rolling off harmonics eliminates the need for shielding and common mode chokes in many applications. Note that rise time increases with increasing input voltage. Noise due to stored charge is also greatly reduced with higher RBOOT resistance. Switching with slower slew rate also decreases the efficiency.

8.3.9 Spread Spectrum

Spread spectrum is a factory option. To find which devices have spread spectrum enabled, see 节 5. The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these emissions across a wider range of frequencies rather than a part with fixed frequency operation. In most systems containing the LM61430-Q1, low frequency-conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is the reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The LM61430-Q1 uses a ±2% spread of frequencies, which can spread energy smoothly across the FM and TV bands, but is small enough to limit subharmonic emissions below the device switching frequency. Peak emissions at the switching frequency of the part are only reduced slightly, by less than 1 dB, while peaks in the FM band are typically reduced by more than 6 dB.

The LM61430-Q1 uses a cycle-to-cycle frequency hopping method based on a linear feedback shift register (LFSR). This intelligent pseudo-random generator limits cycle-to-cycle frequency changes to limit output ripple. The pseudo-random pattern repeats at less than 1.5 Hz, which is below the audio band.

The spread spectrum is only available while the clock of the LM61430-Q1 devices are free running at their natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- The clock is slowed during dropout.
- The clock is slowed at light load in AUTO mode. In FPWM mode, spread spectrum is active even if there is no load.
- At high input voltage/low output voltage ratio when the device operates at minimum on time the internal clock is slowed disabling spread spectrum. See the *Timing Characteristics*.
- The clock is synchronized with an external clock.

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8.3.10 Soft Start and Recovery From Dropout

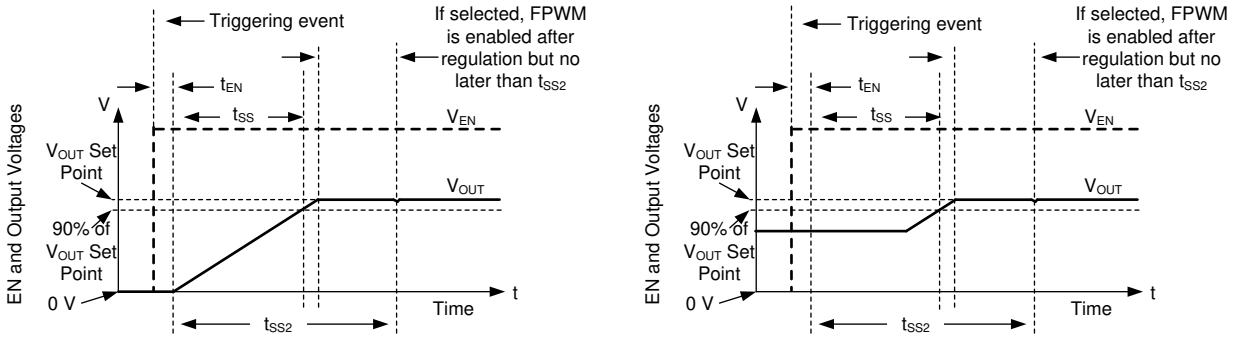
The LM61430-Q1 uses a reference-based soft start that prevents output voltage overshoots and large inrush currents during start up. Soft start is triggered by any of the following conditions:

- Power is applied to the VIN pin of the IC, releasing UVLO.
- EN is used to turn on the device.
- Recovery from a hiccup waiting period.
- Recovery from shutdown due to overtemperature protection.

Once soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped. The net result is that output voltage takes t_{SS} to reach 90% of its desired value.
- Operating mode is set to AUTO, activating diode emulation. This allows start-up without pulling output low if there is a voltage already present on output.

These actions together provide start-up with limited inrush currents and also allow the use of larger output capacitors and higher loading conditions that cause current to border on current limit during start-up without triggering hiccup. See 图 8-8.



Soft start works with both output voltage starting from 0 V on the left curves, or if there is already voltage on the output, as shown on right. In either case, output voltage must reach within 10% of the desired value t_{SS} after soft start is initiated. During soft start, FPWM and hiccup are disabled. Both hiccup and FPWM are enabled once output reaches regulation or t_{SS2}, whichever happens first.

图 8-8. Soft-Start Operation

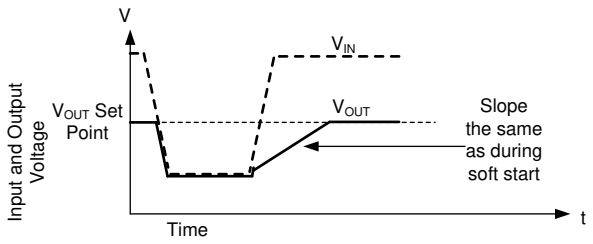
Any time the output voltage falls more than a few percent, the output voltage ramps up slowly. This condition is called recovery from dropout and differs from soft start in three important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.
- Hiccup is allowed if output voltage is less than 0.4 times its set point. Note that during dropout regulation itself, hiccup is inhibited.
- FPWM mode is allowed during recovery from dropout. If the output voltage were to suddenly be pulled up by an external supply, the LM61430-Q1 can pull down on the output.

Despite being called recovery from dropout, this feature is active whenever output voltage drops to a few percent lower than the set point. This primarily occurs under the following conditions:

- Dropout: When there is insufficient input voltage for the desired output voltage to be generated
- Overcurrent: When there is an overcurrent event that is not severe enough to trigger hiccup

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Whether output voltage falls due to high load or low input voltage, once the condition that causes output to fall below its set point is removed, the output climbs at the same speed as during start-up. Even though hiccup does not trigger due to dropout, it can in principle be triggered during recovery if output voltage is below 0.4 times the output set point for more than 128 clock cycles.

图 8-9. Recovery From Dropout

8.3.11 Output Voltage Setting

A feedback resistor divider network between the output voltage and the FB pin is used to set output voltage level. See 图 8-10.

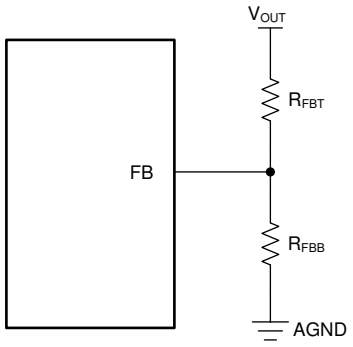


图 8-10. Setting Output Voltage of Adjustable Versions

The LM61430-Q1 uses a 1-V reference voltage for the feedback (FB) pin. The FB pin voltage is regulated by the internal controller to be the same as the reference voltage. The output voltage level is then set by the ratio of the resistor divider. 方程式 3 can be used to determine R_{FBB} for a desired output voltage and a given R_{FBT}. Usually R_{FBT} is between 10 kΩ and 1 MΩ. 100 kΩ is recommended for R_{FBT} for improved noise immunity compared to 1 MΩ and reduced current consumption compared to lower resistance values.

$$R_{FBB} = \frac{R_{FBT}}{V_{OUT} - 1} \tag{3}$$

In addition, a feedforward capacitor, C_{FF}, connected in parallel with R_{FBT} can be required to optimize the transient response.

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8.3.12 Overcurrent and Short Circuit Protection

The LM61430-Q1 is protected from overcurrent conditions with cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the nature of the peak-current mode control. The HS switch current is sensed when the HS is turned on after a short blanking time. Every switching cycle, the HS switch current is compared to either the minimum of a fixed current set point or the output of the voltage regulation loop minus slope compensation. Because the voltage loop has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty cycle when duty cycle is above 35%.

When the LS switch is turned on, the switch current is also sensed and monitored. Like the high-side device, the low-side device turns off as commanded by the voltage control loop, low-side current limit. If the LS switch current is higher than I_{LS_Limit} at the end of a switching cycle, the switching cycle is extended until the LS current reduces below the limit. The LS switch is turned off once the LS current falls below its limit, and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

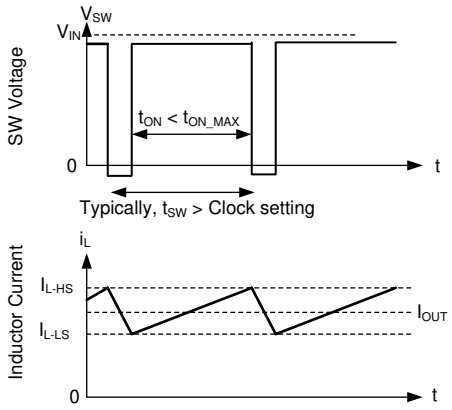


图 8-11. Current Limit Waveforms

Since the current waveform assumes values between I_{L-HS} and I_{L-LS}, the maximum output current is very close to the average of these two values. Hysteretic control is used and current does not increase as output voltage approaches zero.

The LM61430-Q1 employs hiccup overcurrent protection if there is an extreme overload, and the following conditions are met for 128 consecutive switching cycles:

- Output voltage is below approximately 0.4 times the output voltage set point.
- Greater than t_{SS2} has passed since soft start has started; see 节 8.3.10.
- The part is not operating in dropout, which is defined as having minimum off time controlled duty cycle.

In hiccup mode, the device shuts itself down and attempts to soft start after t_W. Hiccup mode helps reduce the device power dissipation under severe overcurrent conditions and short circuits.See 图 8-12.

Once the overload is removed, the device recovers as though in soft start. See 图 8-13.

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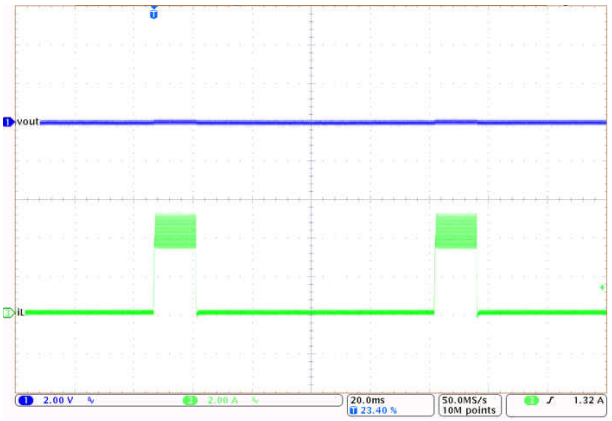


图 8-12. Inductor Current Bursts During Hiccup

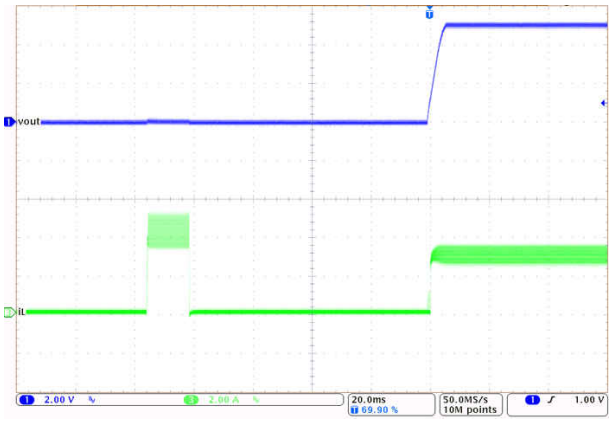


图 8-13. Short-Circuit Recovery

8.3.13 Thermal Shutdown

Thermal shutdown prevents the device from extreme junction temperatures by turning off the internal switches when the IC junction temperature exceeds 165°C (typical). Thermal shutdown does not trigger below 158°C. After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 155°C. When the junction temperature falls below 155°C (typical), the LM61430-Q1 attempts to soft start.

While the LM61430-Q1 is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The VCC current limit is reduced to a few milliamperes during thermal shutdown.

8.3.14 Input Supply Current

The LM61430-Q1 is designed to have very low input supply current when regulating light loads. This is achieved by powering much of the internal circuitry from the output. The BIAS pin is the input to the LDO that powers the majority of the control circuits. By connecting the BIAS input pin to the output of the regulator, a small amount of current drawn from the output. This current is reduced at the input by the ratio of V_{OUT} / V_{IN}.

$$I_{Q_VIN\,(SW)} = I_{EN} + I_{Q_VIN} \times \left(\frac{1}{\eta_{eff}} \right) + I_{div} \times \left(\frac{\text{Output Voltage}}{\text{Input Voltage} \times \eta_{eff}} \right) \quad (4)$$

where

- $I_{Q_VIN(SW)}$ = Current consumed by the operating (switching) buck converter while unloaded
- I_{Q_VIN} = Nonswitching input current. See I_{Q_VIN} in the *Electrical Characteristics*.
- I_{EN} = Current drawn by the EN terminal. Include this current if EN is connected to VIN. See I_{EN} in the *Electrical Characteristics*. Note that this current drops to a very low value if connected to a voltage less than 5 V.
- I_{div} = Current drawn by the feedback voltage divider used to set output voltage
- η_{eff} Light-load efficiency of the buck converter with I_{Q_VIN} removed from the input current of the buck converter. η_{eff} = 0.8 is a conservative value that can be used under normal operating conditions.

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8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage is below 0.4 V, both the converter and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to typically 0.6 µA.

8.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the converter. When the EN pin voltage is above 1.1 V (maximum) and below the precision enable threshold for the output voltage, the internal LDO regulates the VCC voltage at 3.3 V typical. The precision enable circuitry is ON once VCC is above its UVLO. The internal power MOSFETs of the SW node remain off unless the voltage on EN pin goes above its precision enable threshold. The LM61430-Q1 also employs UVLO protection. If the VCC voltage is below its UVLO level, the output of the converter is turned off.

8.4.3 Active Mode

The LM61430-Q1 is in active mode whenever the EN pin is above V_{EN}, V_{IN} is high enough to satisfy $V_{IN_OPERATE}$, and no other fault conditions are present. The simplest way to enable the operation is to connect the EN pin to V_{IN} which allows self start-up when the applied input voltage exceeds the minimum $V_{IN_OPERATE}$.

In active mode, depending on the load current, input voltage, and output voltage, the LM61430-Q1 is in one of four modes:

- AUTO Mode - Light-Load Operation: Discontinuous conduction mode (DCM) when the load current is lower than half of the inductor current ripple. PFM when switching frequency is decreased at very light load.
- FPWM Mode - Light-Load Operation: Continuous conduction mode (CCM) with fixed switching frequency when load current is below half of the inductor current ripple.
- Minimum on time: At high input voltage, low output voltages the switching frequency is reduced to maintain regulation.
- Dropout mode: When switching frequency is reduced to minimize voltage dropout.

8.4.3.1 Auto Mode - Light-Load Operation

The LM61430-Q1 can have two behaviors while lightly loaded. One behavior, called AUTO mode operation, allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light load operation. The other behavior, called FPWM Mode, maintains full frequency even when unloaded. Which mode the LM61430-Q1 operates in depends on which factory option is employed; see 节 5. Note that all parts operate in FPWM mode when synchronizing frequency to an external signal.

In auto mode, light load operation is employed in the LM61430-Q1 at load lower than approximately a tenth of the rated maximum output current. Light-load operation employs two techniques to improve efficiency:

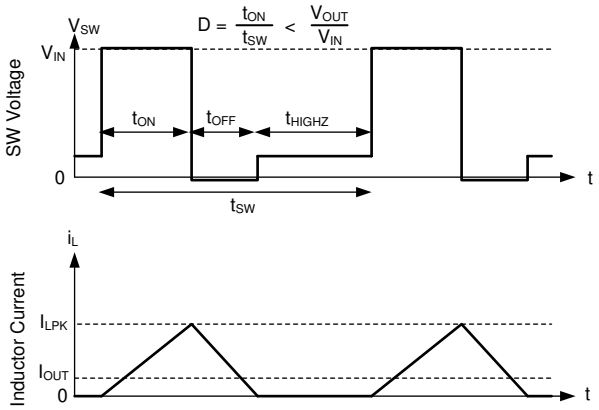
- Diode emulation, which allows DCM operation
- Frequency reduction

Note that while these two features operate together to create excellent light load behavior, they operate independently of each other.

8.4.3.1.1 Diode Emulation

Diode emulation prevents reverse current though the inductor, which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.

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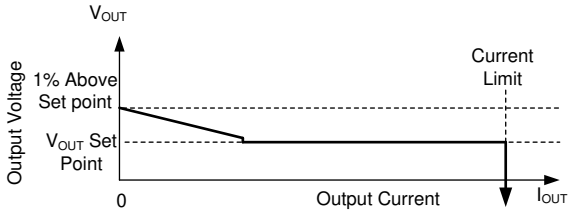
In auto mode, the low-side device is turned off once SW node current is near zero. As a result, once output current is less than half of what inductor ripple would be in CCM, the part operates in DCM which is equivalent to the statement that diode emulation is active.

图 8-14. PFM Operation

The LM61430-Q1 has a minimum peak inductor current setting while in auto mode. Once current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

8.4.3.1.2 Frequency Reduction

The LM61430-Q1 reduces frequency whenever output voltage is high. This function is enabled whenever Comp, an internal signal, is low and there is an offset between the regulation set point of FB and the voltage applied to FB. The net effect is that there is larger output impedance while lightly loaded in AUTO mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.



In auto mode, once output current drops below approximately 1/10th the rated current of the part, output resistance increases so that output voltage is 1% high while the buck is completely unloaded.

图 8-15. Steady State Output Voltage Versus Output Current in Auto Mode

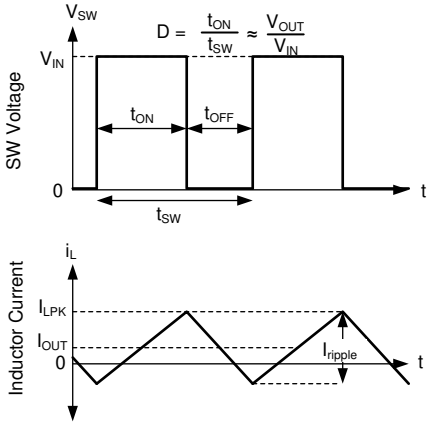
In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on V_{OUT}. If the DC offset on V_{OUT} is not acceptable, a dummy load at V_{OUT} or FPWM Mode can be used to reduce or eliminate this offset.

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8.4.3.2 FPWM Mode - Light-Load Operation

Like auto mode operation, FPWM mode operation during light load operation is selected as a factory option.

In FPWM mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry, see the *Electrical Characteristics* for reverse current limit values.



In FPWM mode, Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple}.

图 8-16. FPWM Mode Operation

For all devices in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on time even while lightly loaded, allowing good behavior during faults which involve output being pulled up.

8.4.3.2.1 CCM Mode

In continuous conduction mode (CCM), the LM61430-Q1 supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During the HS switch on-time, the SW pin voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic as shown in 节 8.2. During the HS switch off time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. Refer to the waveforms in 图 8-17. The converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on time of the HS switch over the switching period:

$$D = T_{ON} / T_{SW} \quad (5)$$

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \quad (6)$$

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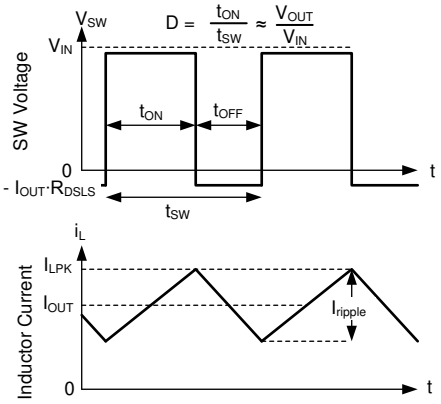
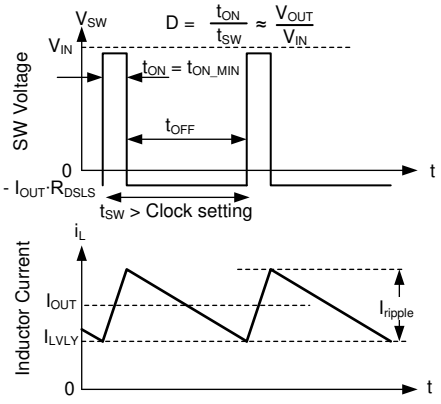


图 8-17. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

8.4.3.3 Minimum On Time (High Input Voltage) Operation

The LM61430-Q1 continues to regulate output voltage even if the input-to-output voltage ratio requires an on time less than the minimum on time of the chip with a given clock setting. This is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the converter is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input voltage to output voltage ratio is too high, even though current exceeds the peak value dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. Once a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Since on-time is fixed at its minimum value, this type of operation resembles that of a device using a COT control scheme; see 图 8-18.



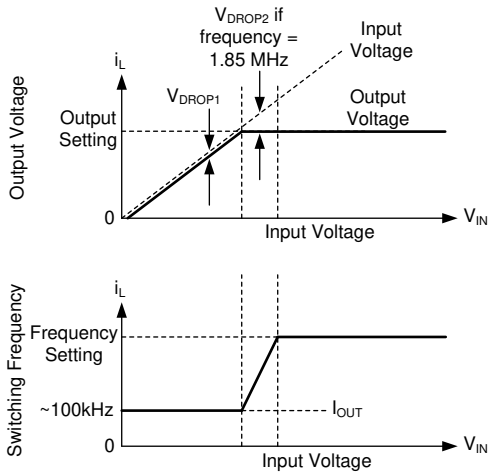
In valley control mode, minimum inductor current is regulated, not peak inductor current.

图 8-18. Valley Current Mode Operation

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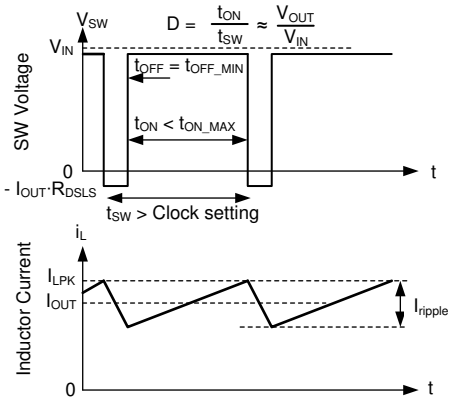
8.4.3.4 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency, duty cycle is limited by minimum off time. Once this limit is reached, if clock frequency were maintained, output voltage would fall. Instead of allowing the output voltage to drop, the LM61430-Q1 extends on time past the end of the clock cycle until needed peak inductor current is achieved. The clock is allowed to start a new cycle once peak inductor current is achieved or once a pre-determined maximum on-time, t_{ON_MAX}, of approximately 9 µs passes. As a result, once the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off-time, frequency drops to maintain regulation. If input voltage is low enough so that output voltage cannot be regulated even with an on time of t_{ON_MAX}, output voltage drops to slightly below input voltage, V_{DROP1}. For additional information on recovery from dropout, reference 图 8-9.



Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110 kHz, input voltage tracks output voltage.

图 8-19. Frequency and Output Voltage in Dropout



Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON_MAX}.

图 8-20. Dropout Waveforms

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9 Application and Implementation

Note

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9.1 Application Information

The LM61430-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3 A. The following design procedure can be used to select components for the LM61430-Q1.

9.2 Typical Application

图 9-1 shows a typical application circuit for the LM61430-Q1. This device is designed to function with a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, 表 9-2 provides typical component values for some of the common configurations.

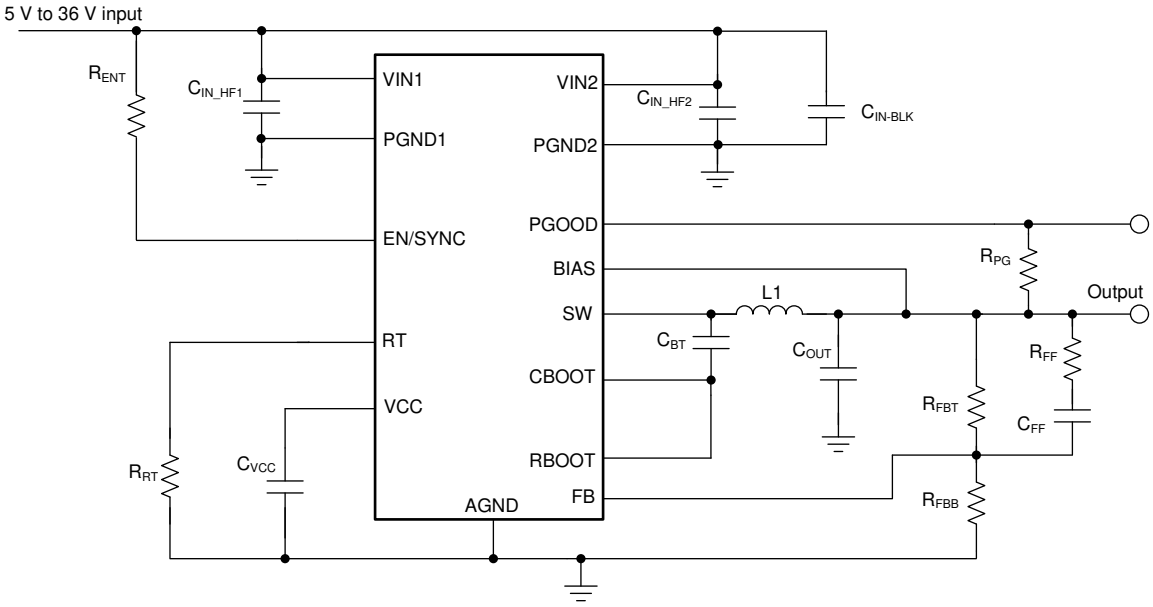


图 9-1. Example Application Circuit

9.2.1 Design Requirements

表 9-1 provides the parameters for our detailed design procedure example:

表 9-1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	13.5 V (5 V to 36 V)
Input voltage for constant f_{SW}	8 V to 18 V
Output voltage	5 V
Maximum output current	0 A to 3 A
Switching frequency	2100 kHz

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表 9-2. Typical External Component Values

f_{SW} (kHz)	V_{OUT} (V)	L1 (µH)	C_{OUT} (RATED)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{BOOT} (µF)	R_{BOOT} (Ω)	C_{VCC} (µF)	C_{FF} (pF)	R_{FF} (kΩ)
400	3.3	10	44 µF ceramic	100	43.2	0.1	0	1	22	1
2100	3.3	1.5	37 µF ceramic	100	43.2	0.1	0	1	22	1
400	5	10	44 µF ceramic	100	24.9	0.1	0	1	22	1
2100	5	1.5	37 µF ceramic	100	24.9	0.1	0	1	22	1

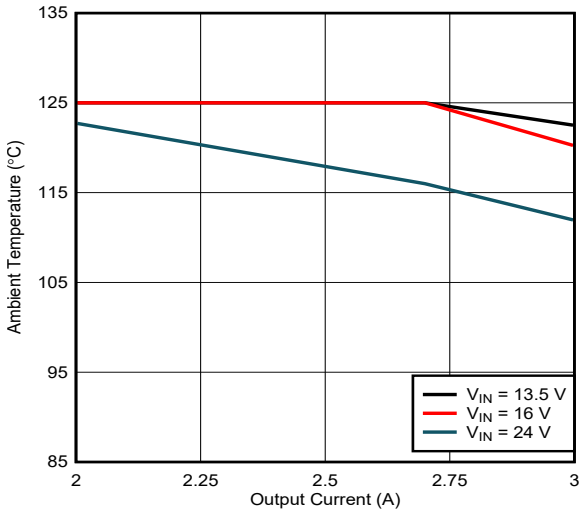
9.2.2 Detailed Design Procedure

The following design procedure applies to 图 9-1 and 表 9-1.

9.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows for the use of smaller inductors and output capacitors, hence, a more compact design.

When choosing operating frequency, the most important consideration is thermal limitations. This constraint typically dominates frequency selection. See 图 9-2 for circuits running at 2.1 MHz. This curves shows how much output current can be supported at a given ambient temperature given a 2.1 MHz. Note that power dissipation is layout dependent so while these curves are a good starting point, thermal resistance in any design will be different from the estimates used to generate 图 9-2. The maximum temperature ratings are based on a 100-mm × 80-mm, 4-layer EVM PCB design.



f_{SW} = 2100 kHz PCB $R_{\theta JA}$ = 25°C/W V_{OUT} = 5 V

图 9-2. Maximum Ambient Temperature versus Output Current

Two other considerations are what maximum and minimum input voltage the part must maintain its frequency setting. Since the LM61430-Q1 adjusts its frequency under conditions in which regulation would normally be prevented by minimum on-time or minimum off time, these constraints are only important for input voltages requiring constant frequency operation.

If foldback is undesirable at high input voltage, then use 方程式 7:

$$f_{SW} \leq \frac{V_{OUT}}{V_{IN}(MAX2) \cdot t_{ON_MIN}(MAX)} \quad (7)$$

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If foldback at low input voltage is a concern, use 方程式 8:

$$f_{SW} \leq \frac{V_{INeff}(MIN2) - V_{OUT}}{V_{INeff}(MIN2) \cdot t_{OFF_MIN}(MAX)} \quad (8)$$

where:

- $V_{INeff}(MIN2) = V_{IN}(MIN2) - I_{OUT}(MAX) \cdot (R_{DS(ON)_HS}(MAX) + DCR(MAX))$
- DCR(MAX) = Maximum DCR of the inductor
- $t_{OFF_MIN}(MAX)$ = See the *Electrical Characteristics*.
- $R_{DS(ON)_HS}(MAX)$ = See the *Electrical Characteristics*.

The fourth constraint is the rated frequency range of the IC. See f_{ADJ} in the *Electrical Characteristics*. All previously stated constraints (thermal, $V_{IN}(MAX2)$, $V_{IN}(MIN2)$, and device-specified frequency range) must be considered when selecting frequency.

Many applications require that the AM band can be avoided. These applications tend to operate at either 400 kHz below the AM band or 2.1 MHz above the AM band. In this example, 400 kHz is chosen.

9.2.2.2 Setting the Output Voltage

The output voltage of LM61430-Q1 is externally adjustable using a resistor divider network. The range of recommended output voltage is found in the *Recommended Operating Conditions*. The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100 kΩ with a maximum value of 1 MΩ. If 1 MΩ is selected for R_{FBT}, then a feedforward capacitor must be used across this resistor to provide adequate loop phase margin (see 节 9.2.2.10). Once R_{FBT} is selected, 方程式 3 is used to select R_{FBB}. V_{REF} is nominally 1 V. For this 5-V example, R_{FBT} = 100 kΩ and R_{FBB} = 24.9 kΩ are chosen.

9.2.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current for systems with a fixed input voltage and 25% for systems with a variable input voltage such as the 12-V battery in a car. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current must still be used. 方程式 9 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, K = 0.25 was chosen and an inductance of approximately 1.85 µH was found. The next standard value of 1.5 µH was selected.

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \cdot K \cdot I_{OUT}(MAX)} \cdot \frac{V_{OUT}}{V_{IN}} \quad (9)$$

The saturation current rating of the inductor must be at least as large as the high-side switch current limit, $I_{L\text{-}HS}$ (see the *Electrical Characteristics*). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, $I_{L\text{-}LS}$, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage; do not allow the inductor to saturate. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powdered iron cores

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exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies typically above 1 MHz. In any case, the inductor saturation current must not be less than the device high-side current limit, $I_{L\text{-}HS}$ (see the *Electrical Characteristics*). To avoid subharmonic oscillation, the inductance value must not be less than that given in 方程式 10. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L \geq 0.32 \cdot \frac{V_{OUT}}{f_{SW}} \tag{10}$$

方程式 10 assumes that this design must operate with input voltage near or in dropout. If minimum operating voltage for this design is high enough to limit duty factor to below 50%, 方程式 9 can be used in place of 方程式 10.

Note that choosing an inductor that is larger than the minimum inductance calculated using 方程式 9 through 方程式 10 results in less output capacitance being needed to limit output ripple but more output capacitance being needed to manage large load transients. See 节 9.2.2.4.

9.2.2.4 Output Capacitor Selection

The value of the output capacitor and its ESR determine the output voltage ripple and load transient performance. The output capacitor is usually determined by the load transient requirements rather than the output voltage ripple. 表 9-3 can be used to find the output capacitor and C_{FF} selection for a few common applications. Note that a 1-kΩ R_{FF} must be used in series with C_{FF}. In this example, the component selection is 2 × 47 µF ceramic as the output capacitor and 22 pF as C_{FF}.

表 9-3. Recommended Output Ceramic Capacitors and C_{FF} Values

FREQUENCY	TRANSIENT PERFORMANCE	3.3-V OUTPUT		5-V OUTPUT	
		CERAMIC OUTPUT CAPACITANCE	C_{FF}	CERAMIC OUTPUT CAPACITANCE	C_{FF}
2.1 MHz	Minimum	37 µF	22 pF	37 µF	22 pF
2.1 MHz	Better Transient	47 µF	22 pF	47 µF	22 pF
400 kHz	Minimum	44 µF	22 pF	44 µF	22 pF
400 kHz	Better Transient	66 µF	22 pF	66 µF	22 pF

To minimize ceramic capacitance, a low-ESR electrolytic capacitor can be used in parallel with minimal ceramic capacitance.

Most ceramic capacitors deliver far less capacitance than the rating of the capacitor indicates. Be sure to check any capacitor selected for initial accuracy, temperature derating, and voltage derating. 表 9-3 has been generated assuming typical derating for 16-V, X7R, automotive grade capacitors. If lower voltage, non-automotive grade, or lower temperature rated capacitors are used, more capacitors than listed are likely to be needed.

9.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the converter in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10 µF of ceramic capacitance is required on the input of the device. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100-nF ceramic capacitor must be used at each input/ground pin pair, VIN1/PGND1 and VIN2/PGND2, immediately adjacent to the converter. This provides a high-frequency bypass for the control circuits internal to the device. These capacitors also suppress SW node ringing, which reduces the maximum voltage present on the SW node and EMI. The two 100 nF must also be rated at 50 V with an X7R or better dielectric. The VQFN-HR (RJR)

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package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split, and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. In this example, two 4.7-µF and two 100-nF ceramic capacitors are used, one at each VIN/PGND location. A single 10-µF can also be used on one side of the package.

Many times, it is desirable and necessary to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the converter. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitors. The approximate worst case RMS value of this current can be calculated from 方程式 11 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \approx \frac{I_{OUT}}{2} \tag{11}$$

9.2.2.6 BOOT Capacitor

The LM61430-Q1 requires a bootstrap capacitor connected between the CBOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the high side power MOSFET. A high-quality (X7R) ceramic capacitor of 100 nF and at least 10 V is required.

9.2.2.7 BOOT Resistor

A BOOT resistor can be connected between the CBOOT and RBOOT pins. Unless EMI for the application being designed is critical, these two pins can be shorted. A 100-Ω resistor between these pins eliminates overshoot. Even with 0 Ω, overshoot and ringing are minimal, less than 2 V if input capacitors are placed correctly. A boot resistor of 100 Ω, which corresponds to approximately 2.7 ns SW node rise time and decreases efficiency by approximately 0.5% at 2 MHz. To maximize efficiency, 0 Ω is chosen for this example. Under most circumstances, selecting an RBOOT resistor value above 100 Ω is undesirable since the resulting small improvement in EMI is not enough to justify further decreased efficiency.

9.2.2.8 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the converter. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to AGND for proper operation. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see 节 8.3.5). A pullup resistor with a value of 100 kΩ is a good choice in this case. Note, VCC remains high when V_{EN_WAKE}< EN < V_{EN}. The nominal output voltage on VCC is 3.3 V. Do not short this output to ground or any other external voltage.

9.2.2.9 BIAS

Because V_{OUT} = 5 V in this design, the BIAS pin is tied to V_{OUT} to reduce LDO power loss. The output voltage is supplying the LDO current instead of the input voltage. The power saving is I_{LDO} × (V_{IN} – V_{OUT}). The power saving is more significant when V_{IN} >> V_{OUT} and with higher frequency operation. To prevent V_{OUT} noise and transients from coupling to BIAS, a series resistor, 1 Ω to 10 Ω, can be added between V_{OUT} and BIAS. A bypass capacitor with a value of 1 µF or higher can be added close to the BIAS pin to filter noise. Note, the maximum allowed voltage on the BIAS pin is 16 V.

9.2.2.10 C_{FF} and R_{FF} Selection

A feedforward capacitor, C_{ff}, is used to improve phase margin and transient response of circuits which have output capacitors with low ESR. Since this capacitor can conduct noise from the output of the circuit directly to

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the FB node of the IC, a 1-kΩ resistor, R_{ff}, can be placed in series with Cff. If the ESR zero of the output capacitor is below 200 kHz, no C_{ff} should be used.

If output voltage is less than 2.5 V, C_{ff} has little effect so can be omitted. If output voltage is greater than 14 V, C_{ff} must not be used since it will introduce too much gain at higher frequencies.

9.2.2.11 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 图 9-3. The input voltage at which the device turns on is designated V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then 方程式 13 is used to calculate R_{ENT} and V_{OFF}. R_{ENB} is typically set based on how much current this voltage divider should consume. R_{ENB} can be calculated using 方程式 12.

$$R_{ENB} = \frac{V_{EN} \cdot V_{IN}}{I_{DIVIDER} \cdot V_{ON}} \tag{12}$$

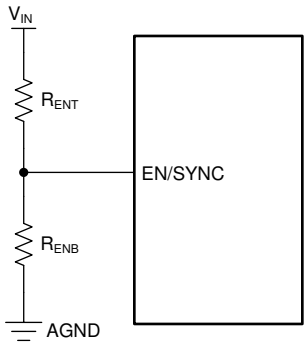


图 9-3. UVLO Using EN

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN}} - 1\right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot (1 - V_{EN\text{-}HYST}) \tag{13}$$

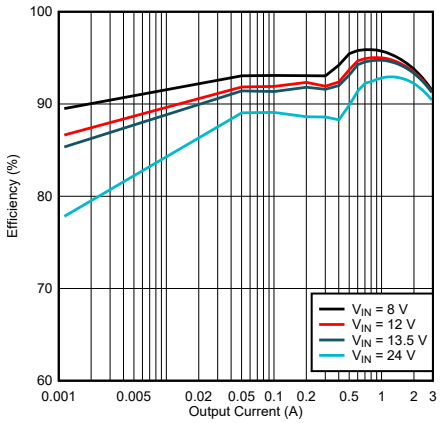
where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage
- $I_{DIVIDER}$ = Voltage divider current

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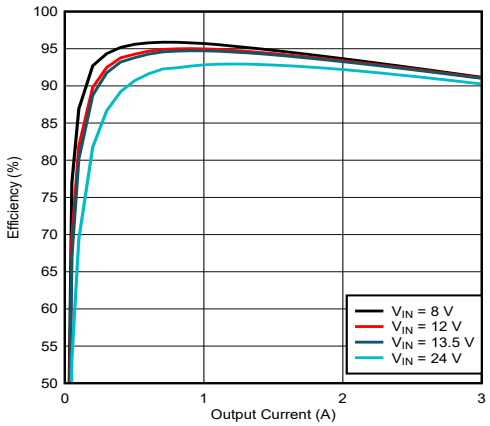
9.2.3 Application Curves

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. The circuit is shown in 图 9-1, with the appropriate BOM from 表 9-4.



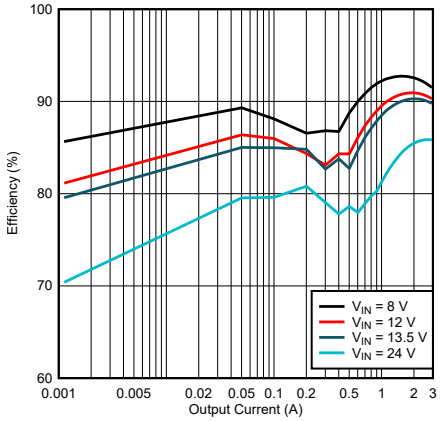
V_{OUT} = 3.3 V F_{SW} = 400 kHz Auto mode

图 9-4. LM61430-Q1 Efficiency



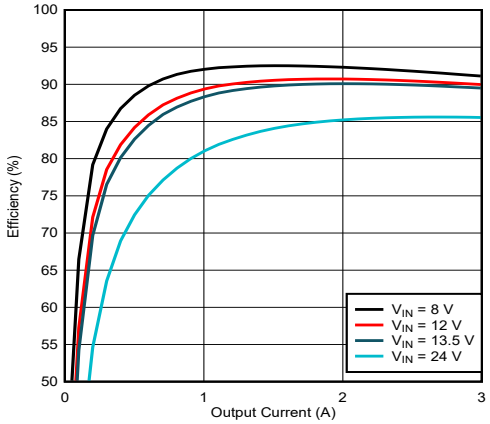
V_{OUT} = 3.3 V F_{SW} = 400 kHz FPWM mode

图 9-5. LM61430-Q1 Efficiency



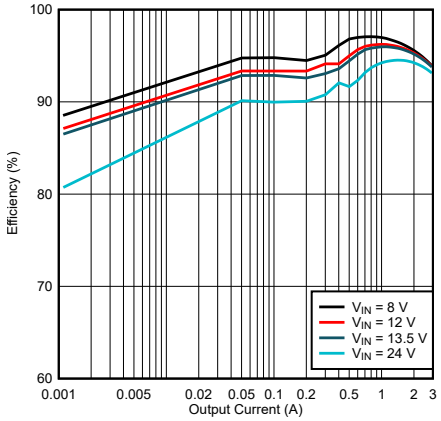
V_{OUT} = 3.3 V F_{SW} = 2100 kHz Auto mode

图 9-6. LM61430-Q1 Efficiency



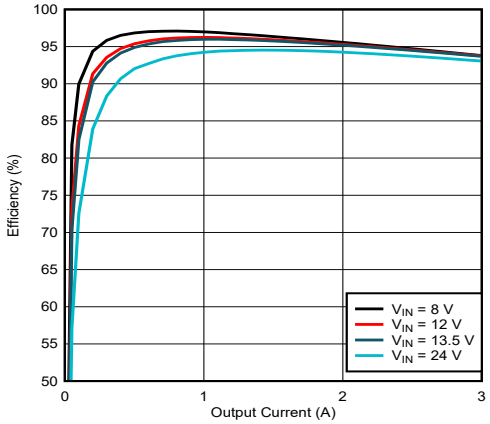
V_{OUT} = 3.3 V F_{SW} = 2100 kHz FPWM mode

图 9-7. LM61430-Q1 Efficiency



V_{OUT} = 5 V F_{SW} = 400 kHz Auto mode

图 9-8. LM61430-Q1 Efficiency



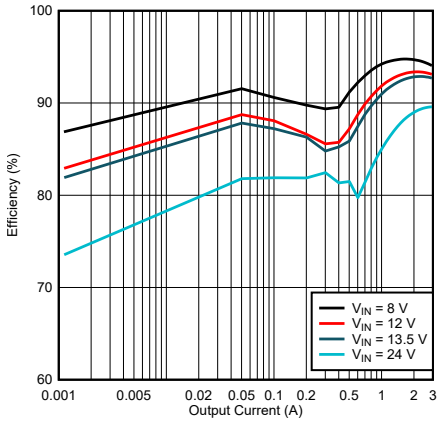
V_{OUT} = 5 V F_{SW} = 400 kHz FPWM mode

图 9-9. LM61430-Q1 Efficiency

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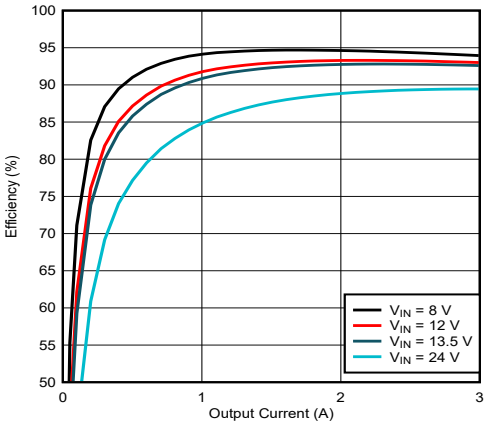
9.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. The circuit is shown in 图 9-1, with the appropriate BOM from 表 9-4.



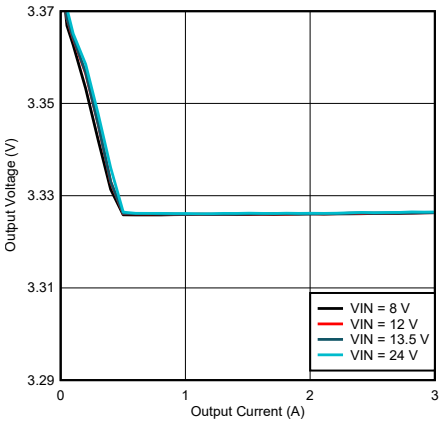
V_{OUT} = 5 V F_{SW} = 2100 kHz Auto mode

图 9-10. LM61430-Q1 Efficiency



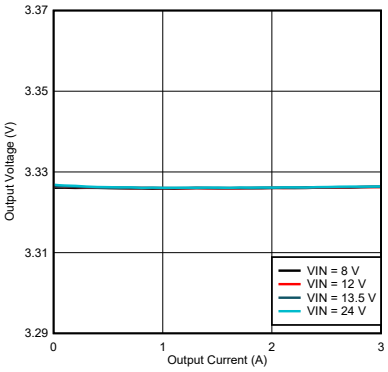
V_{OUT} = 5 V F_{SW} = 2100 kHz FPWM mode

图 9-11. LM61430-Q1 Efficiency



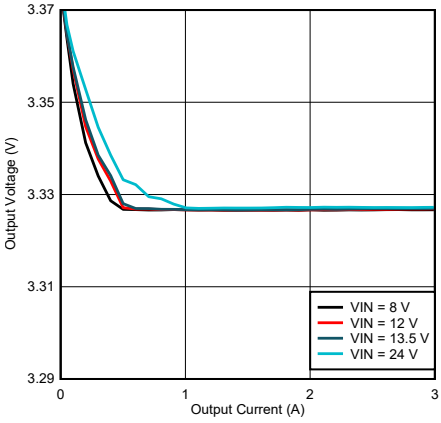
V_{OUT} = 3.3 V F_{SW} = 400 kHz Auto mode

图 9-12. LM61430-Q1 Load and Line Regulation



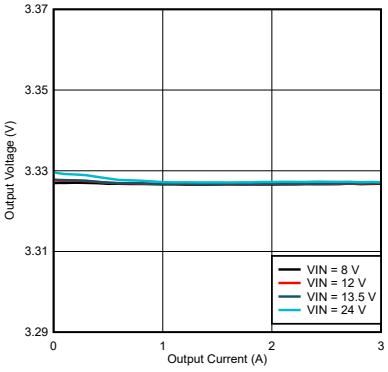
V_{OUT} = 3.3 V F_{SW} = 400 kHz FPWM mode

图 9-13. LM61430-Q1 Load and Line Regulation



V_{OUT} = 3.3 V F_{SW} = 2100 kHz Auto mode

图 9-14. LM614630-Q1 Load and Line Regulation



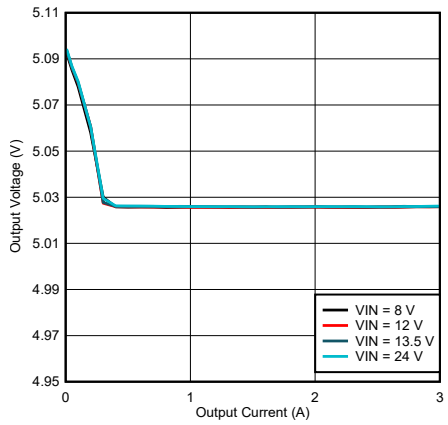
V_{OUT} = 3.3 V F_{SW} = 2100 kHz FPWM mode

图 9-15. LM61430-Q1 Load and Line Regulation

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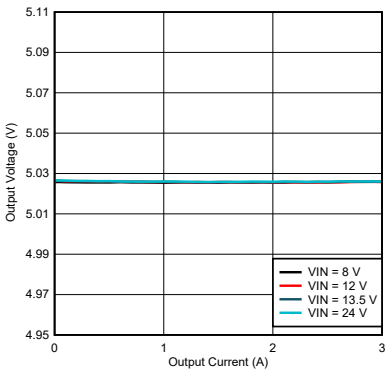
9.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. The circuit is shown in 图 9-1, with the appropriate BOM from 表 9-4.



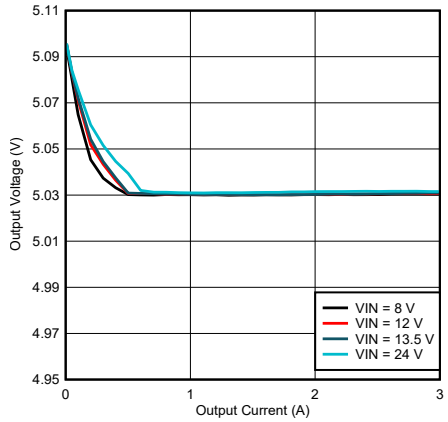
V_{OUT} = 5 V F_{SW} = 400 kHz Auto mode

图 9-16. LM61430-Q1 Load and Line Regulation



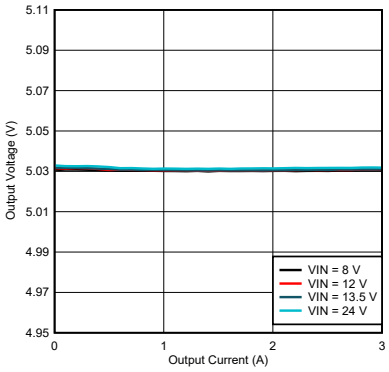
V_{OUT} = 5 V F_{SW} = 400 kHz FPWM mode

图 9-17. LM61430-Q1 Efficiency



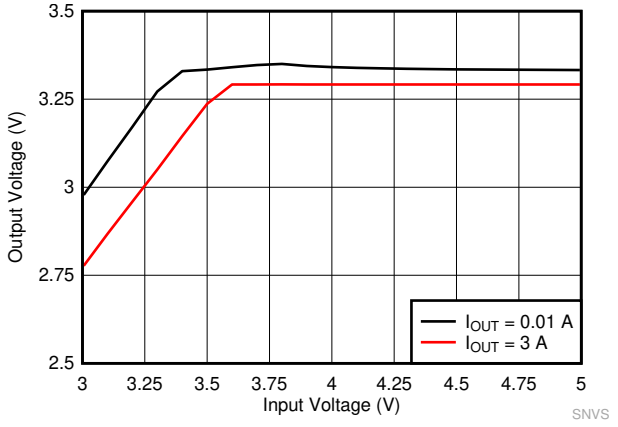
V_{OUT} = 5 V F_{SW} = 2100 kHz Auto mode

图 9-18. LM61430-Q1 Load and Line Regulation



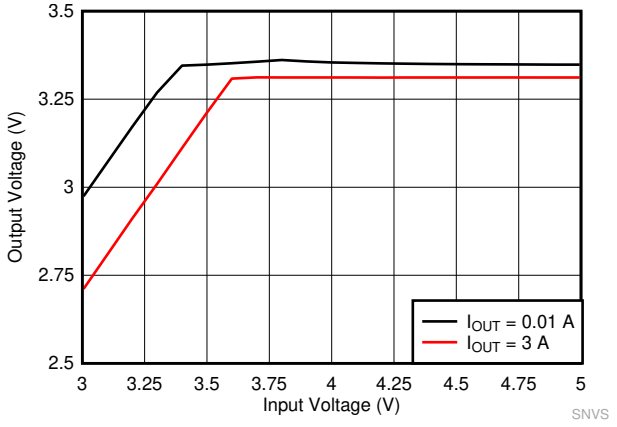
V_{OUT} = 5 V F_{SW} = 2100 kHz FPWM mode

图 9-19. LM61430-Q1 Load and Line Regulation



V_{OUT} = 3.3 V F_{SW} = 400 kHz Auto mode

图 9-20. LM61430-Q1 Dropout Curve



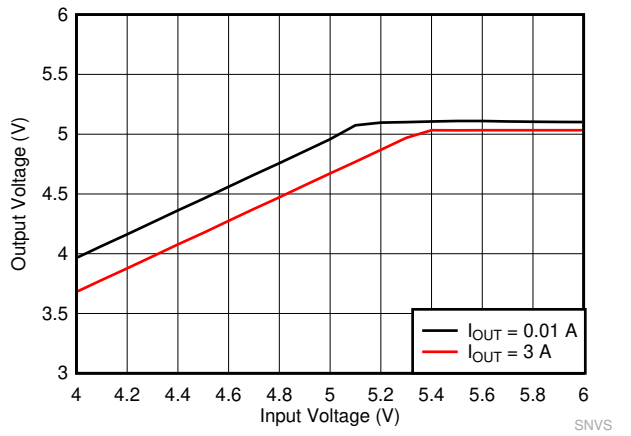
V_{OUT} = 3.3 V F_{SW} = 2100 kHz Auto mode

图 9-21. LM61430-Q1 Dropout Curve

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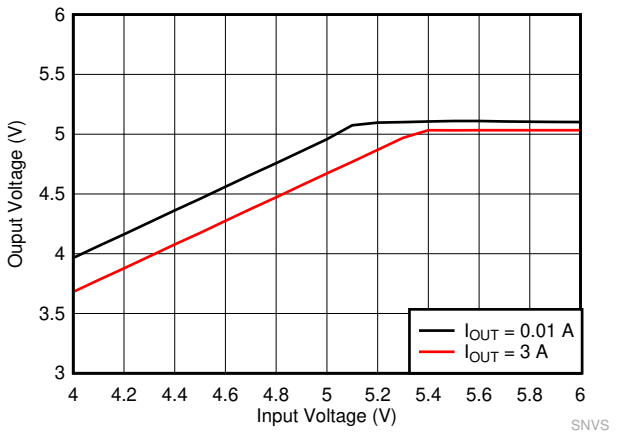
9.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. The circuit is shown in 图 9-1, with the appropriate BOM from 表 9-4.



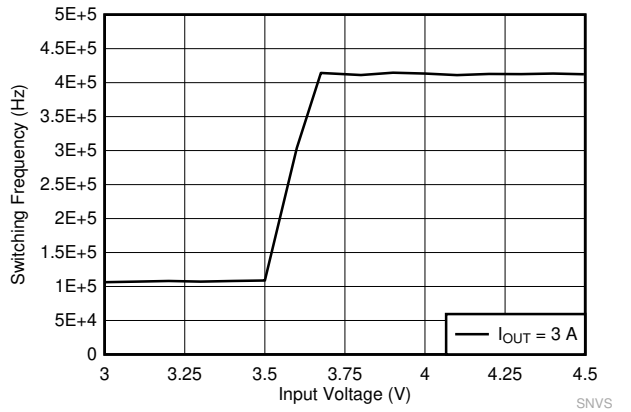
V_{OUT} = 5 V F_{SW} = 400 kHz Auto mode

图 9-22. LM61430-Q1 Dropout Curve



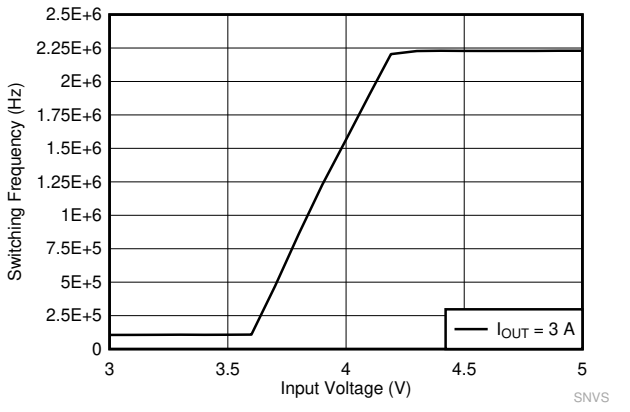
V_{OUT} = 5 V F_{SW} = 2100 kHz Auto mode

图 9-23. LM61430-Q1 Dropout Curve



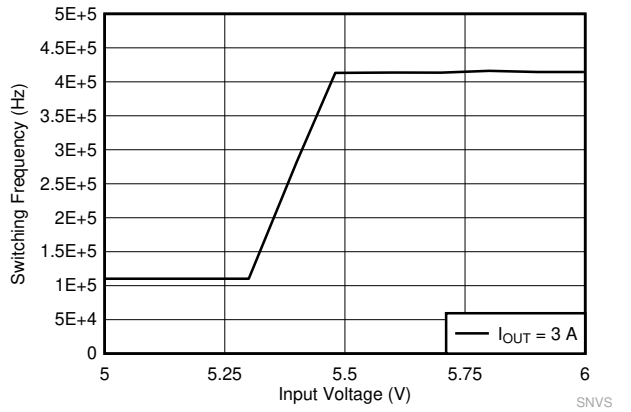
V_{OUT} = 3.3 V F_{SW} = 400 kHz Auto mode

图 9-24. LM61430-Q1 Frequency Dropout Curve



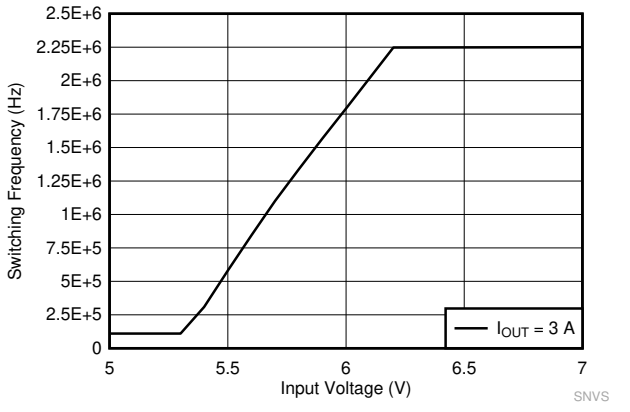
V_{OUT} = 3.3 V F_{SW} = 2100 kHz Auto mode

图 9-25. LM61430-Q1 Frequency Dropout Curve



V_{OUT} = 5 V F_{SW} = 400 kHz Auto mode

图 9-26. LM61430-Q1 Frequency Dropout Curve



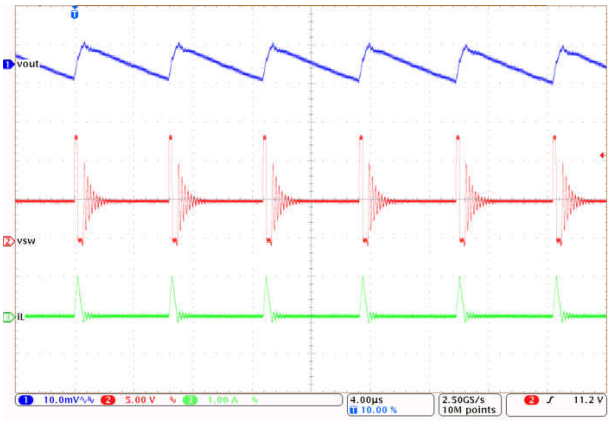
V_{OUT} = 5 V F_{SW} = 2100 kHz Auto mode

图 9-27. LM61430-Q1 Frequency Dropout Curve

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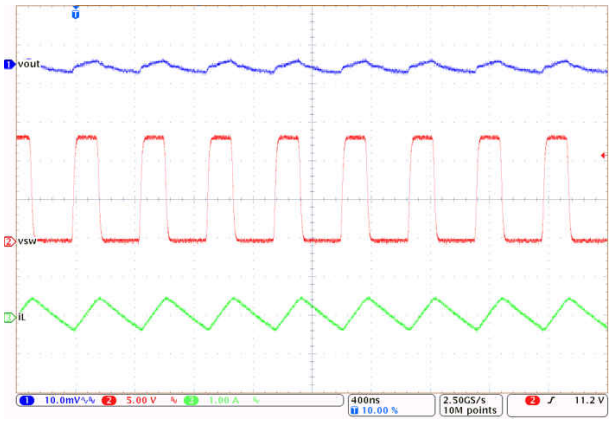
9.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. The circuit is shown in 图 9-1, with the appropriate BOM from 表 9-4.



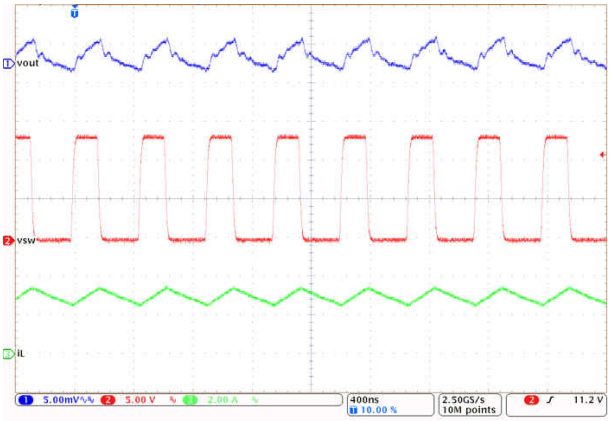
V_{OUT} = 5 V F_{SW} = 2100 kHz Auto mode
I_{OUT} = 100 mA V_{IN} = 13.5 V

图 9-28. LM61430-Q1 Switching Waveform and V_{OUT} Ripple



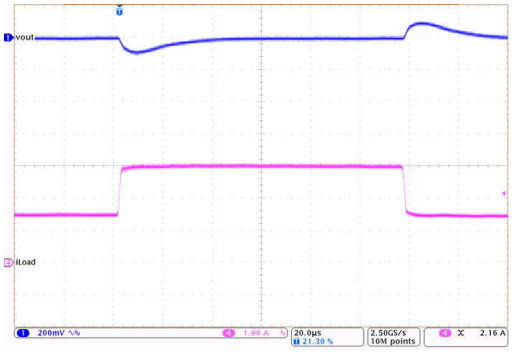
V_{OUT} = 5 V F_{SW} = 2100 kHz FPWM mode
I_{OUT} = 100 mA V_{IN} = 13.5 V

图 9-29. LM61430-Q1 Switching Waveform and V_{OUT} Ripple



V_{OUT} = 5 V F_{SW} = 2100 kHz Auto mode
I_{OUT} = 3 A V_{IN} = 13.5 V

图 9-30. LM61430-Q1 Switching Waveform and V_{OUT} ripple

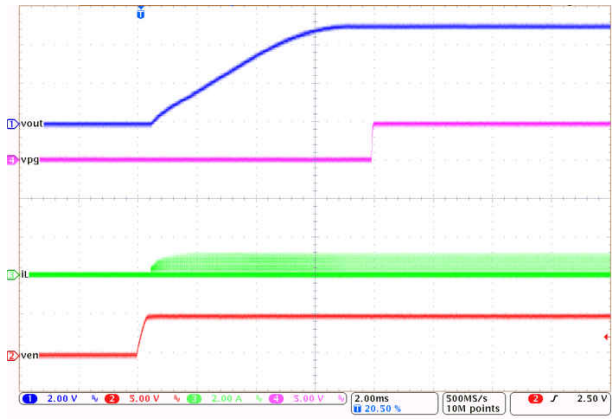


V_{OUT} = 5 V F_{SW} = 2100 kHz FPWM mode
I_{OUT} = 1.5 A to 3 A to 0 A V_{IN} = 13.5 V $T_R = T_F$ = 6 µs

图 9-31. LM61430-Q1 Load Transient

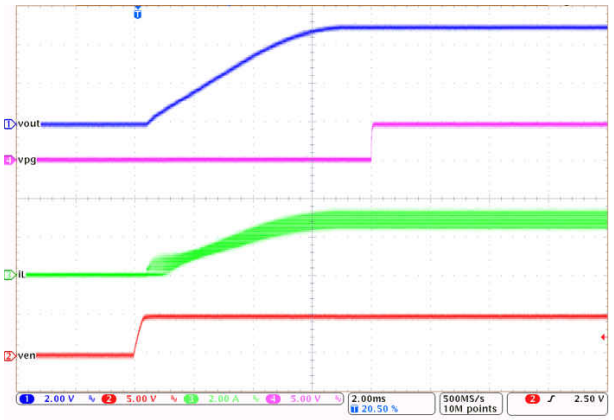
9.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. The circuit is shown in 图 9-1, with the appropriate BOM from 表 9-4.



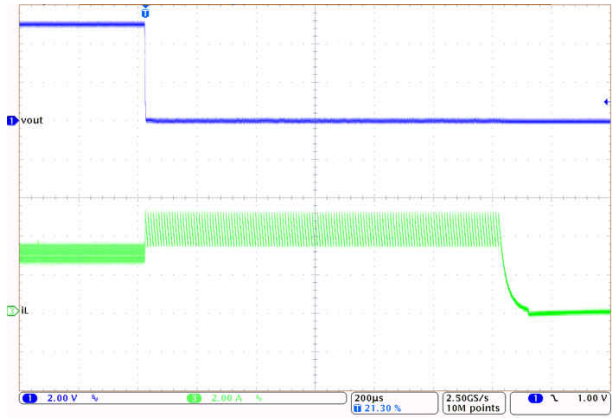
V_{OUT} = 5 V F_{SW} = 2100 kHz Auto mode
I_{OUT} = 100 mA V_{IN} = 13.5 V

图 9-32. LM61430-Q1 Start-up with 100-mA Load



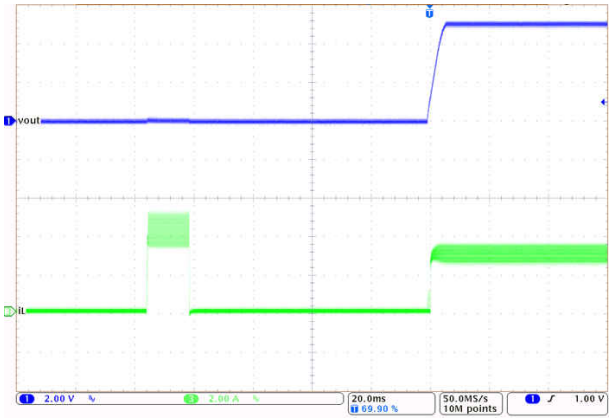
V_{OUT} = 5 V F_{SW} = 2100 kHz FPWM mode
I_{OUT} = 3 A V_{IN} = 13.5 V

图 9-33. LM61430-Q1 Start-up with 3 A



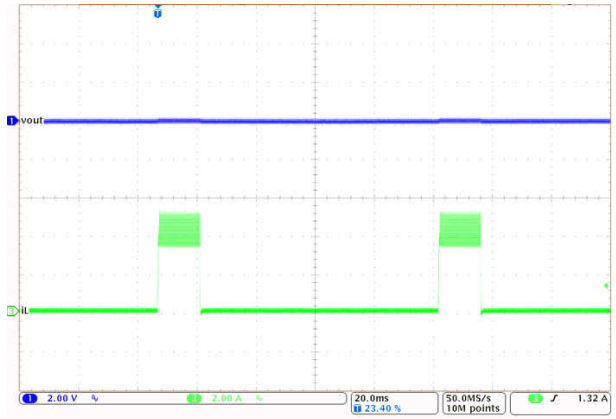
V_{OUT} = 5 V F_{SW} = 2100 kHz FPWM mode
I_{OUT} = 3 A to Short Circuit V_{IN} = 13.5 V

图 9-34. LM61430-Q1 Short Circuit Protection



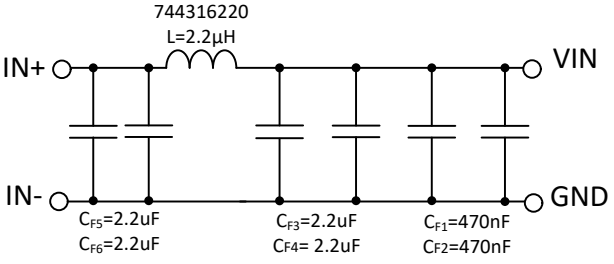
V_{OUT} = 5 V F_{SW} = 2100 kHz FPWM mode
I_{OUT} = Short Circuit to 3 A V_{IN} = 13.5 V

图 9-35. LM61430-Q1 Short Circuit Recovery



V_{OUT} = 5 V F_{SW} = 2100 kHz FPWM mode
I_{OUT} = Short Circuit V_{IN} = 13.5 V

图 9-36. LM61430-Q1 Short Circuit Performance



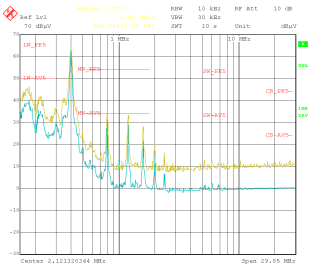
F_{SW} = 400 kHz

图 9-37. Recommended Input EMI Filter

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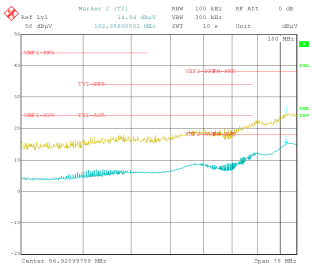
9.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. The circuit is shown in 图 9-1, with the appropriate BOM from 表 9-4.



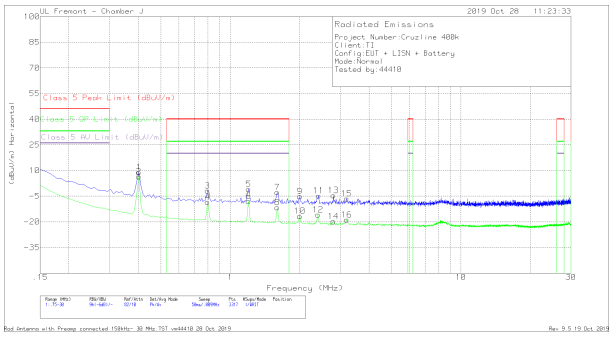
F_{SW} = 400 kHz V_{OUT} = 5 V I_{OUT} = 5 A
Frequency tested: 150 kHz to 30 MHz
Tested on 6-A variant with LM61460EVM

图 9-38. Conducted EMI Versus CISPR25 Limits (Yellow: Peak Signal, Blue: Average Signal)



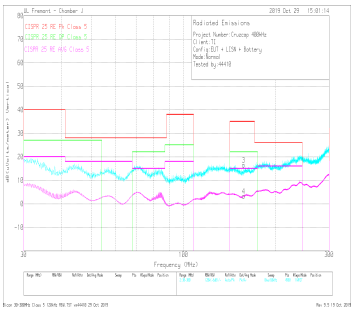
V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 5 A
Frequency tested: 30 MHz to 108 MHz
Tested on 6-A variant with LM61460EVM

图 9-39. Conducted EMI Versus CISPR25 Limits (Yellow: Peak Signal, Blue: Average Signal)



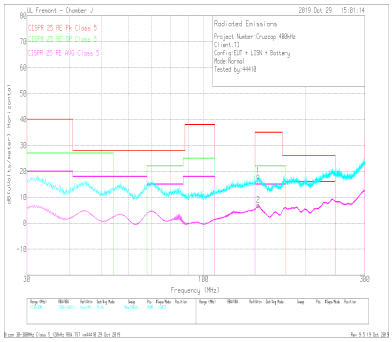
V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 5 A
Frequency tested: 150 kHz to 30 MHz
Tested on 6-A variant with LM61460EVM

图 9-40. Radiated EMI Rod Versus CISPR25 Limits



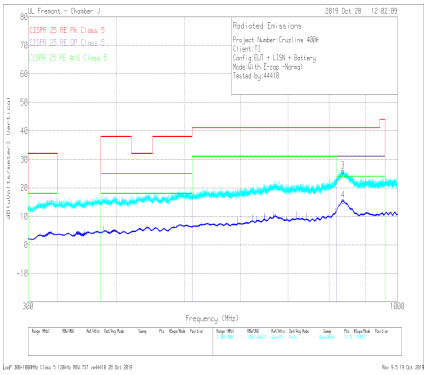
V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 5 A
Frequency tested: 30 MHz to 300 MHz
Tested on 6-A variant with LM61460EVM

图 9-41. Radiated EMI Bicon Vertical Versus CISPR25 Limits



V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 5 A
Frequency tested: 30 MHz to 300 MHz
Tested on 6-A variant with LM61460EVM

图 9-42. Radiated EMI Bicon Horizontal Versus CISPR25 Limits



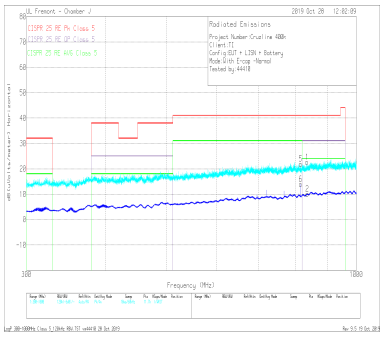
V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 5 A
Frequency tested: 300 MHz to 1 GHz
Tested on 6-A variant with LM61460EVM

图 9-43. Radiated EMI Log Vertical Versus CISPR25 Limits

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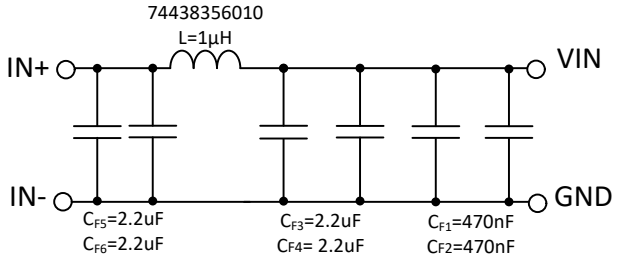
9.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. The circuit is shown in 图 9-1, with the appropriate BOM from 表 9-4.



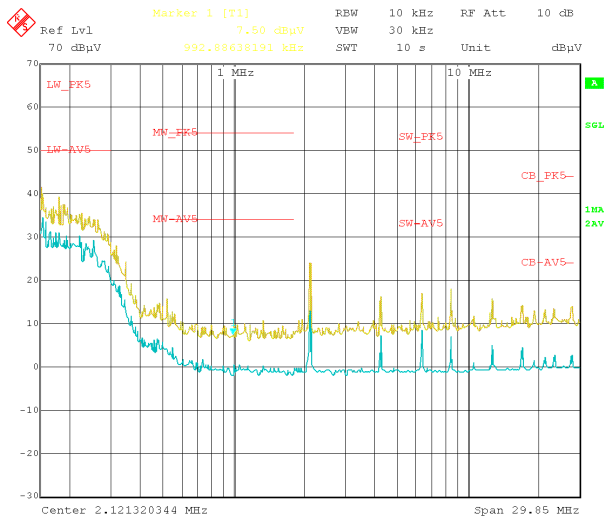
V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 5 A
Frequency tested: 300 MHz to 1 GHz
Tested on 6-A variant with LM61460EVM

图 9-44. Radiated EMI Log Horizontal Versus CISPR25 Limits



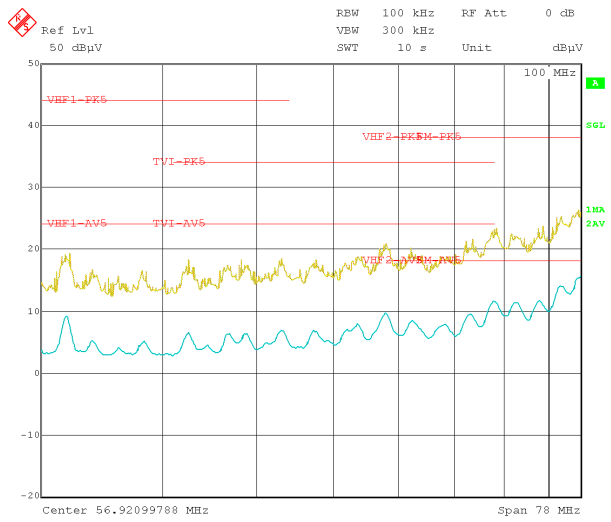
F_{SW} = 2100 kHz Note: Measurements taken with LM61460EVM

图 9-45. Recommended Input EMI Filter



F_{SW} = 2100 kHz V_{OUT} = 5 V I_{OUT} = 5 A
Frequency tested: 150 kHz to 30 MHz
Tested on 6-A variant with LM61460EVM

图 9-46. Conducted EMI Versus CISPR25 Limits (Yellow: Peak Signal, Blue: Average Signal)



F_{SW} = 2100 kHz V_{OUT} = 5 V I_{OUT} = 5 A
Frequency tested: 30 MHz to 108 MHz
Tested on 6-A variant with LM61460EVM

图 9-47. Conducted EMI Versus CISPR25 Limits (Yellow: Peak Signal, Blue: Average Signal)

表 9-4. BOM for Typical Application Curves

V_{OUT}	FREQUENCY	R_{FBB}	R_T	C_{OUT}	C_{IN} + C_{HF}	L
3.3 V	400 kHz	100 kΩ	43.2 kΩ	**6 x 22 µF**	**2 x 4.7 µF + 2 x 100 nF**	10 µH **(XHMI6060)**
3.3 V	2100 kHz	100 kΩ	43.2 kΩ	**3 x 22 µF**	**2 x 4.7 µF + 2 x 100 nF**	1.5 µH **(XEL5030)**
5 V	400 kHz	100 kΩ	24.9 kΩ	**4 x 22 µF**	**2 x 4.7 µF + 2 x 100 nF**	10 µH (XHMI6060)
5 V	2100 kHz	100 kΩ	24.9 kΩ	**3 x 22 µF**	**2 x 4.7 µF + 2 x 100 nF**	1.5 µH (74438356015)

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10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded converter. The average input current can be estimated with 方程式 14.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{14}$$

where

- η = efficiency

If the converter is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the converter. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under-damped resonant circuit, resulting in overvoltage transients at the input to the converter or tripping UVLO. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the converter to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the converter and use an aluminum input capacitor in parallel with the ceramics. The moderate ESR of this type of capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

In some cases, a transient voltage suppressor (TVS) is used on the input of converters. One class of this device has a snap-back characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the converter, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the TVS and cause large input transients.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then a Schottky diode between the input supply and the output must be used.

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11 Layout

11.1 Layout Guidelines

The PCB layout of any DC-DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the converter is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in 图 11-1. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance.

- *Place the input capacitor or capacitors as close as possible input pin pairs*: VIN1 to PGND1 and VIN2 to PGND2. Each pair of pins are adjacent, simplifying the input capacitor placement. With the VQFN-HR package, there are two VIN/PGND pairs on either side of the package. This provides for a symmetrical layout and helps minimize switching noise and EMI generation. Use a wide VIN plane on a lower layer to connect both of the VIN pairs together to the input supply.
- *Place bypass capacitor for VCC close to the VCC pin and AGND pins*: This capacitor must routed with short, wide traces to the VCC and AGND pins.
- *Use wide traces for the CBOOT capacitor*: Place the CBOOT capacitor as close to the device with short, wide traces to the CBOOT and SW pins. It is important to route the SW connection under the device through the gap between VIN2 and RBOOT pins, reducing exposed SW node area. If an RBOOT resistor is used, place as close as possible to CBOOT and RBOOT pins. If high efficiency is desired, RBOOT and CBOOT pins can be shorted. This short must be placed as close as possible to RBOOT and CBOOT pins as possible.
- *Place the feedback divider as close as possible to the FB pin of the device*: Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and AGND through R_{FBB} must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the converter.
- *Layer 2 of the PCB must be a ground plane*: This plane acts as a noise shield and a heat dissipation path. Using layer 2 reduces the inclosed area in the input circulating current in the input loop, reducing inductance.
- *Provide wide paths for V_{IN}, V_{OUT}, and GND*: These paths must be wide and direct as possible to reduce any voltage drops on the input or output paths of the converter and maximizes efficiency.
- *Provide enough PCB area for proper heat sinking*: Enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces must be used for all pins except where noise considerations dictate minimization of area.
- *Keep switch area small*: Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

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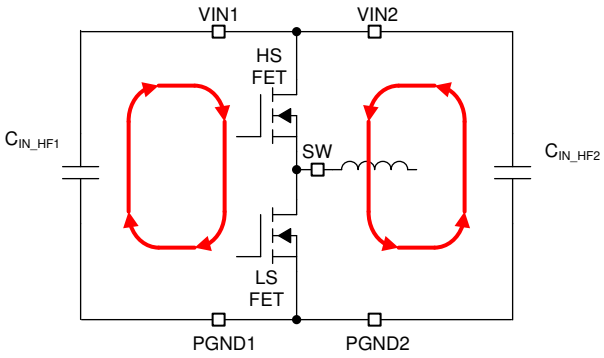


图 11-1. Input Current Loop

11.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low-side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by using vias near ground and V_{IN} to connect to the system ground plane or V_{IN} strap, both of which dissipate heat. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness and proper layout, provides low current conduction impedance, proper shielding, and lower thermal resistance.

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11.2 Layout Example

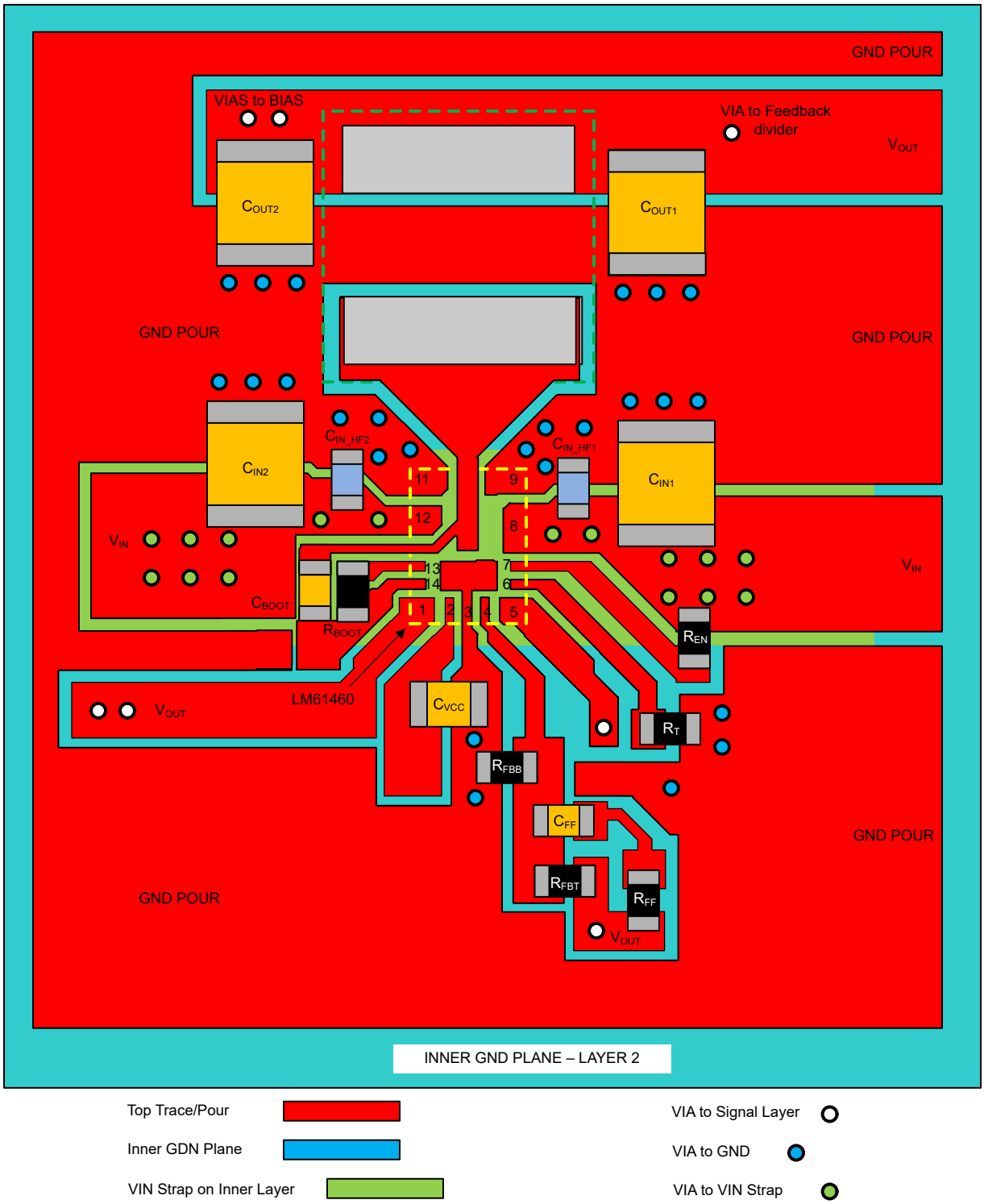


图 11-2. Layout Example

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12 Device and Documentation Support

12.1 Device Support

12.1.1 第三方产品免责声明

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Designing High Performance, Low-EMI, Automotive Power Supplies Application Report*
- Texas Instruments, *LM61460-Q1 EVM User's Guide*
- Texas Instruments, *30 W Power for Automotive Dual USB Type-C Charge Port Reference Design*
- Texas Instruments, *EMI Filter Components and Their Nonidealities for Automotive DC/DC Regulators Technical Brief*
- Texas Instruments, *AN-2020 Thermal Design by Insight, Not Hindsight Application Report*
- Texas Instruments*Optimizing the Layout for the TPS54424/TPS54824 HotRod QFN Package for Thermal Performance Application Report*
- Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC-DC Converters Application Report*
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules Application Report*

12.3 接收文档更新通知

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12.4 支持资源

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM61430AASQRJRRQ1	Active	Production	VQFN-HR (RJR) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6143Q1 AAS
LM61430AASQRJRRQ1.A	Active	Production	VQFN-HR (RJR) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6143Q1 AAS
LM61430AFSQRJRRQ1	Active	Production	VQFN-HR (RJR) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6143Q1 AFS
LM61430AFSQRJRRQ1.A	Active	Production	VQFN-HR (RJR) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6143Q1 AFS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

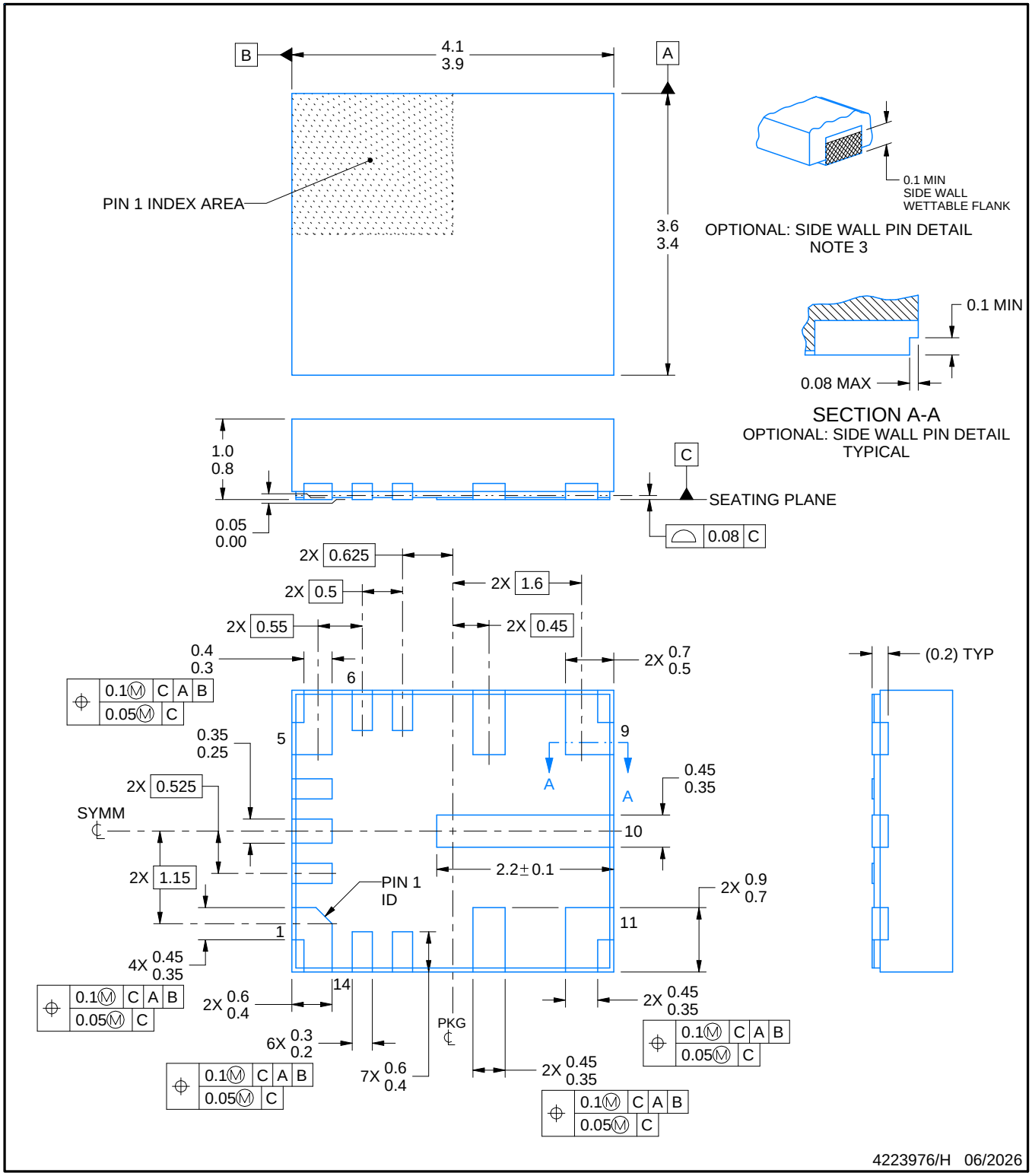
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RJR0014A

PACKAGE OUTLINE

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

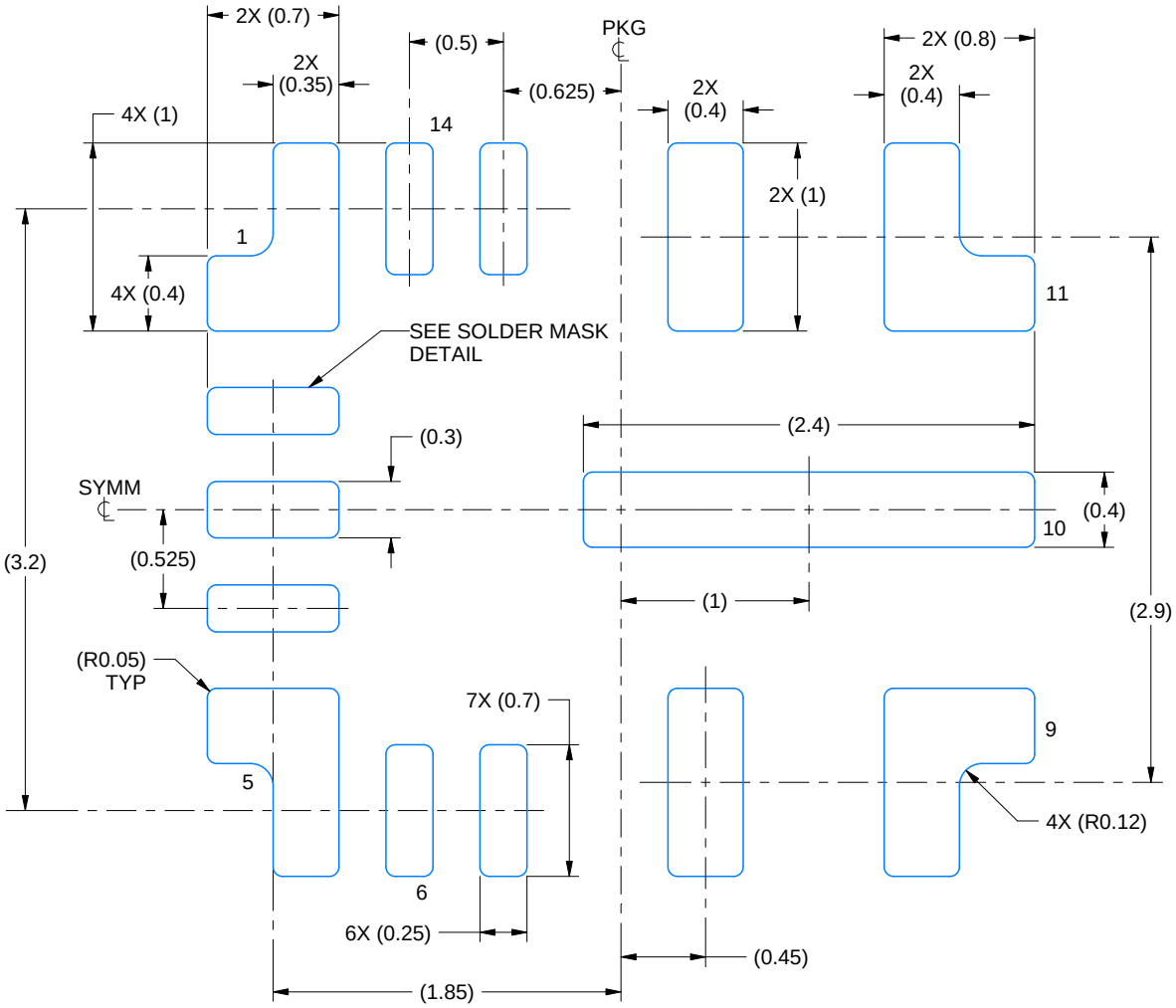
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.

EXAMPLE BOARD LAYOUT

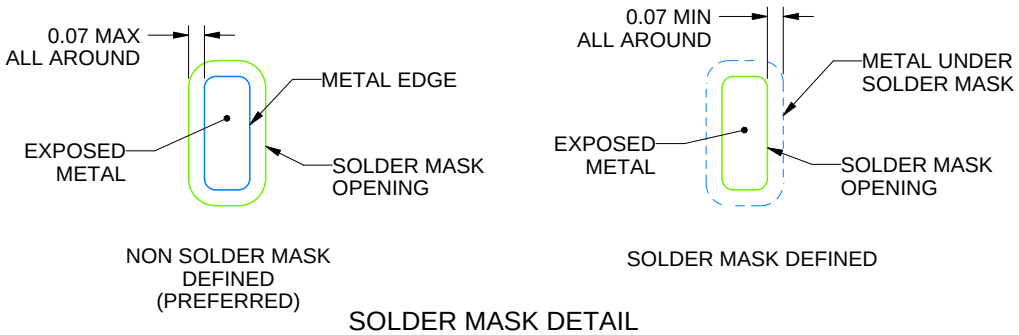
RJR0014A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAIL

4223976/H 06/2026

NOTES: (continued)

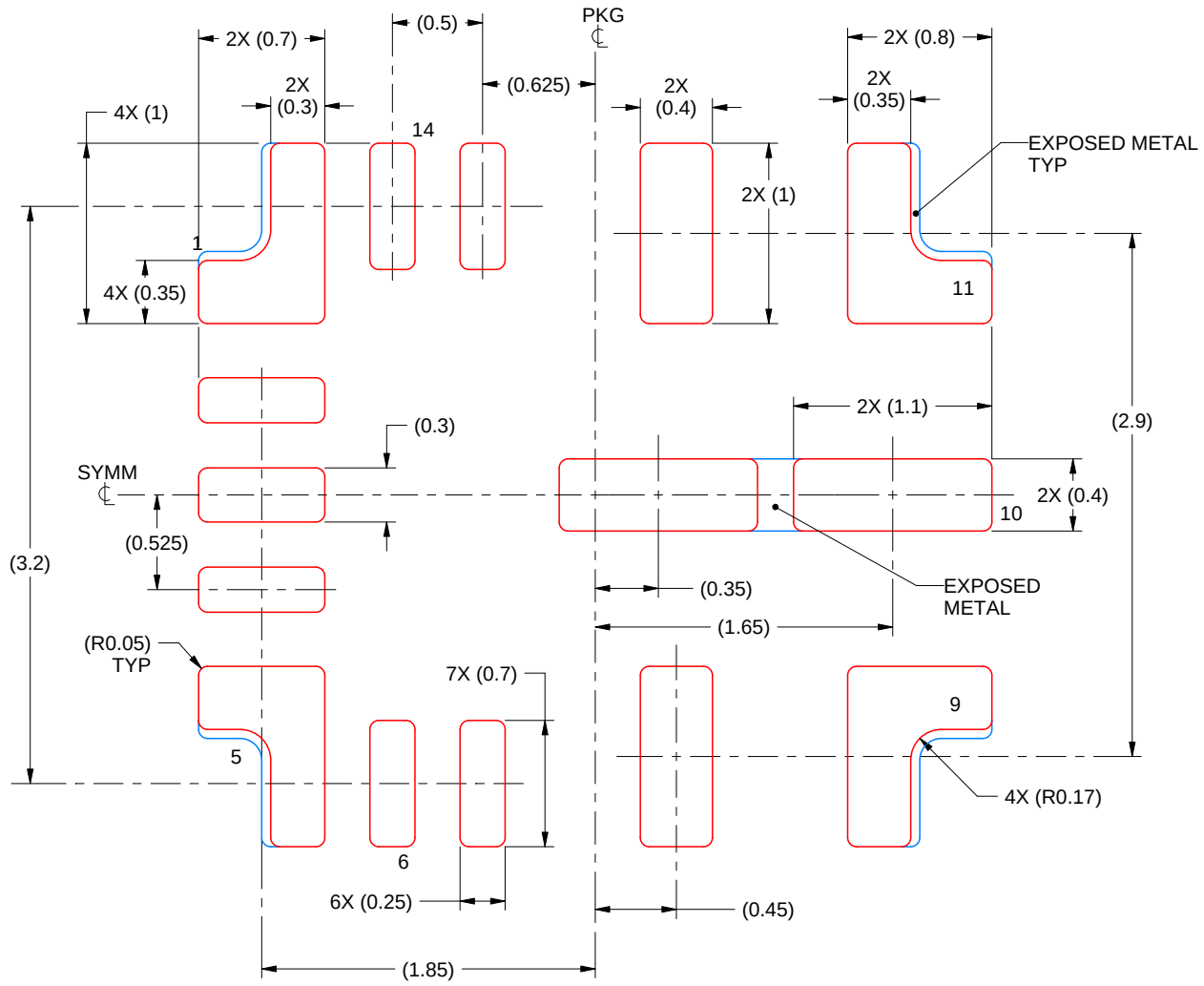
4. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RJR0014A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
PADS 1, 5, 9 & 11:
90% PRINTED SOLDER COVERAGE BY AREA
SCALE: 25X

4223976/H 06/2026

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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