LM604x0-Q1 3.8V 至 36V、 3A 和 4A 超小型同步降压转换器

ADVANCE INFORMATION

1 特性

- 符合面向汽车 应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 +125°C，T_A
- 提供功能安全
  - 可帮助进行功能安全系统设计的可用文档
- 低 EMI 和开关噪声
  - 符合 CISPR25 5 类标准
  - 增强型 QFN 封装最大程度地减少了寄生电感和开关节点振铃
- 专用于条件汽车类 应用
  - 标准 QFN 封装：单个大散热焊盘和所有引脚均分布在封装外围
  - 引脚兼容型号：
    - LM60440-Q1（36V，4A）
    - LM60430-Q1（36V，3A）
  - 结温范围：–40°C 至 +150°C
  - ±1.5% 的总输出稳压精度
  - 频率：400kHz
  - 输出电压范围：1V 至 24V
- 可在所有负载下进行高效电源转换
  - 峰值效率 > 95%
  - 在 10mA、$12V_{IN}$、$5V_{OUT}$ 下，PFM 效率为 90%
  - 低至 25µA 的工作静态电流
- 使用 LM60440-Q1 并借助 WEBENCH® 电源设计器创建定制设计

2 应用

- 信息娱乐系统和仪表组：USB 充电
- 汽车车身电子装置和照明

3 说明

LM604x0-Q1 稳压器符合汽车标准，是一款简单易用的同步降压直流/直流转换器，可提供业界一流的效率，适用于汽车类 应用。LM60430-Q1 可驱动高达 3A 的负载电流，而 LM60440-Q1 是一款业界超小型的 4A 降压转换器。

LM604x0-Q1 采用带有可湿性侧面的超小型 WQFN 封装和带有散热焊盘的标准 QFN 引脚布局以增强热性能。此增强型 QFN 封装 具有 极小的寄生电感和电阻，能够实现非常高的效率，同时可最大程度地减少开关节点振铃并显着降低 EMI。

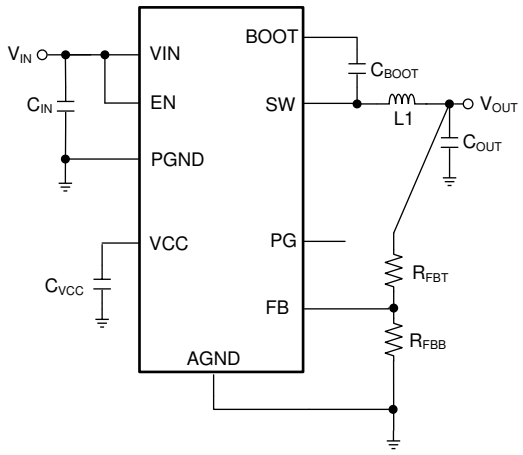
LM604x0-Q1 采用峰值电流模式控制，可在轻负载时自动折返频率，以确保在整个负载范围内具有出色的效率。较低的功率耗散在热性能经优化的 QFN 封装的加持之下，可以较小的尺寸实现具有较高功率密度的解决方案。此外，此器件需要极少外部组件，并且具有可简化 PCB 布局的引脚排列方式。LM604x0-Q1 的小型解决方案尺寸和功能集旨在简化各种终端设备的实现。

器件信息(1)

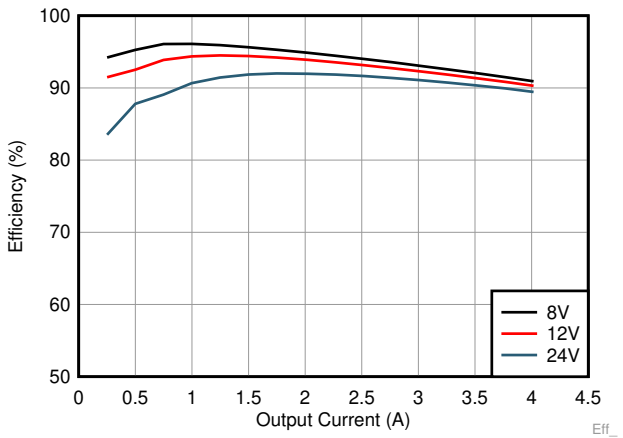
器件型号	封装	封装尺寸（标称值）
LM60440-Q1	WQFN-13	3.00mm × 2.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化原理图



效率与输出电流间的关系
V_{OUT} = 5V，400kHz



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2020 年 2 月	*	初始发行版

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5 Device Comparison Table

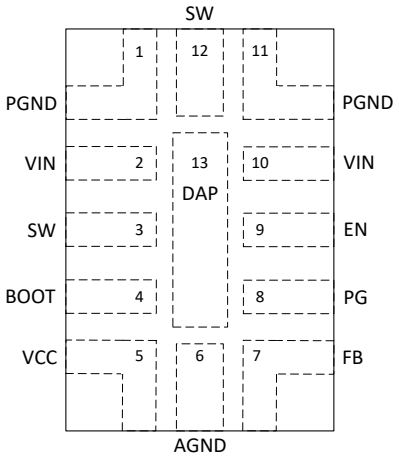
DEVICE OPTION	PACKAGE	FREQUENCY	RATED CURRENT	OUTPUT VOLTAGE
PLM60440AQRPKRQ1	RPK (WQFN-13)	400 kHz	4 A	Adjustable
PLM60430AQRPKRQ1	RPK (WQFN-13)	400 kHz	3 A	Adjustable

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6 Pin Configuration and Functions

RPK Package
WQFN-13 With PowerPAD™
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1, 11	PGND	G	Power ground terminal. Connect to system ground and AGND. Connect to bypass capacitor with short wide traces.
2, 10	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and PGND.
3, 12	SW	P	Regulator switch node. Connect to power inductor. Pin 3 can be used to simplify the connection from the C_{BOOT} capacitor to the SW pin.
4	BOOT	P	Bootstrap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. On the WQFN package, connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin.
5	VCC	P	Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high quality 1-µF capacitor from this pin to GND.
6	AGND	G	Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB.
7	FB	A	Feedback input to regulator. Connect to tap point of feedback voltage divider. *Do not float. Do not ground.*
8	PG	A	Open-drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Flag pulls low when EN = Low. Can be left open when not used.
9	EN	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; *Do not float.*
13	DAP	—	Low impedance connection to PGND. Connect to system ground on PCB. Major heat dissipation path for the die. Must be used for heat sinking by soldering to ground copper on PCB. Thermal vias are preferred.
A = Analog, P = Power, G = Ground			

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to PGND	–0.3	38	V
	EN to AGND(2)	–0.3	V_{IN} + 0.3	
	FB to AGND	–0.3	5.5	
	PG to AGND(2)	0	22	
	AGND to PGND	–0.3	0.3	
	SW to PGND	–0.3	V_{IN} + 0.3	
	SW to PGND less than 100-ns transients	–3.5	38	
	BOOT to SW	–0.3	5.5	
	VCC to AGND(3)	–0.3	5.5	
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V
(3) Under some operating conditions the VCC LDO voltage may increase beyond 5.5 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) (1)	±2500	V
		Charged-device model (CDM) (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating temperature range of –40°C to 150°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	3.8	36	V
	EN (2)	0	V_{IN}	
	PG(2)	0	18	
Adjustable output voltage	V_{OUT}(3)	1	24	V
Output current	I_{OUT}	0	4	A

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see *Electrical Characteristics*.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) The maximum output voltage can be extended to 95% of V_{IN}; contact TI for details. Under no conditions should the output voltage be allowed to fall below zero volts.

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7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature*.

THERMAL METRIC(1)(2)		LM60440/30-Q1 WQFN 13 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	24.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature*.

7.5 Electrical Characteristics

Limits apply over the operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Minimum operating input voltage				3.8	V
I_Q	Non-switching input current; measured at VIN pin (1)	V_{FB} = 1.2 V		24	34	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	EN = 0		5	10	µA
ENABLE						
$V_{EN-VCC-H}$	EN input level required to turn on internal LDO	Rising threshold			1	V
$V_{EN-VCC-L}$	EN input level required to turn off internal LDO	Falling threshold	0.3			V
V_{EN-H}	EN input level required to start switching	Rising threshold	1.2	1.231	1.26	V
V_{EN-HYS}	Hysteresis below V_{EN-H}	Hysteresis below V_{EN-H}; falling		100		mV
INTERNAL SUPPLIES						
VCC	Internal LDO output voltage appearing at the VCC pin	6 V ≤ V_{IN} ≤ 36 V	4.75	5	5.25	V
$V_{BOOT-UVLO}$	Bootstrap voltage undervoltage lock-out threshold(2)			2.2		V
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage; ADJ option		0.985	1	1.015	V
CURRENT LIMITS(3)						
I_{SC}	High-side current limit	LM60440-Q1		5.5		A
I_{SC}	High-side current limit	LM60430-Q1		4.5		A
I_{LIMIT}	Low-side current limit	LM60440-Q1		4.5		A
I_{LIMIT}	Low-side current limit	LM60430-Q1		3.5		A
$I_{PEAK-MIN}$	Minimum peak inductor current	LM60440-Q1		0.86		A

(1) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(2) When the voltage across the C_{BOOT} capacitor falls below this voltage, the low side MOSFET is turned on to recharge C_{BOOT}.
(3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

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Electrical Characteristics (continued)

Limits apply over the operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PEAK-MIN}$	Minimum peak inductor current	LM60430-Q1		0.69		A
I_{ZC}	Zero current detector threshold			-0.106		A
SOFT START						
t_{SS}	Internal soft-start time		2.9	4.4	6	ms
POWER GOOD (PG PIN)						
$V_{PG-HIGH-UP}$	Power-good upper threshold - rising	% of FB voltage	105%	107%	110%	
$V_{PG-HIGH-DN}$	Power-good upper threshold - falling	% of FB voltage	103%	105%	108%	
$V_{PG-LOW-UP}$	Power-good lower threshold - rising	% of FB voltage	92%	94%	97%	
$V_{PG-LOW-DN}$	Power-good lower threshold - falling	% of FB voltage	90%	92%	95%	
t_{PG}	Power-good glitch filter delay(4)		60		170	µs
R_{PG}	Power-good flag R_{DSON}	V_{IN} = 12 V, V_{EN} = 4 V		76	150	Ω
		V_{EN} = 0 V		35	60	
V_{IN-PG}	Minimum input voltage for proper PG function	50-µA, EN = 0 V			2	V
V_{PG}	PG logic low output	50-µA, EN = 0 V, V_{IN} = 2V			0.2	V
OSCILLATOR						
f_{SW}	Switching frequency		340	400	460	kHz
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance			76	146	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance			51	96	mΩ

(4) See *Power-Good Flag Output* for details.

7.6 Timing Characteristics

Limits apply over the operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, V_{EN} = 4 V.

			MIN	NOM	MAX	UNIT
t_{ON-MIN}	Minimum switch on-time			55	80	ns
$t_{OFF-MIN}$	Minimum switch off-time			50	70	ns
t_{ON-MAX}	Maximum switch on-time			7	9	µs

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7.7 System Characteristics

The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. *These specifications are not ensured by production testing.*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range	V_{OUT} = 3.3 V, I_{OUT}= 0 A	3.8		36	V
V_{OUT}	Output voltage regulation for V_{OUT} = 5 V(1)	V_{OUT} = 5 V, V_{IN} = 7 V to 36 V, I_{OUT} = 0 A to 4 A	–1.6%		2.5%	
		V_{OUT} = 5 V, V_{IN} = 7 V to 36 V, I_{OUT} = 1 A to 4 A	–1.6%		1.5%	
	Output voltage regulation for V_{OUT} = 3.3 V(1)	V_{OUT} = 3.3 V, V_{IN} = 3.8 V to 36 V, I_{OUT} = 0 A to 4 A	–1.6%		2.5%	
		V_{OUT} = 3.3 V, V_{IN} = 3.8 V to 36 V, I_{OUT} = 1 A to 4 A	–1.6%		1.5%	
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, R_{FBT} = 1 MΩ		25		µA
V_{DROP}	Dropout voltage; (V_{IN} – V_{OUT})	V_{OUT} = 5 V, I_{OUT} = 1A Dropout at –1% of regulation, f_{SW} = 140 kHz		150		mV
D_{MAX}	Maximum switch duty cycle(2)	V_{IN} = V_{OUT} = 12 V, I_{OUT} = 1 A		98%		
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
t_{HC}	Time between current-limit hiccup burst			94		ms
t_D	Switch voltage dead time			2		ns
T_{SD}	Thermal shutdown temperature	Shutdown temperature		165		°C
		Recovery temperature		148		°C

(1) Deviation is with respect to V_{IN} =12 V, I_{OUT} = 1 A.
(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: f_{MIN} = 1 / ($t_{ON\text{-}MAX}$ + $t_{OFF\text{-}MIN}$). D_{MAX} = $t_{ON\text{-}MAX}$ /($t_{ON\text{-}MAX}$ + $t_{OFF\text{-}MIN}$).

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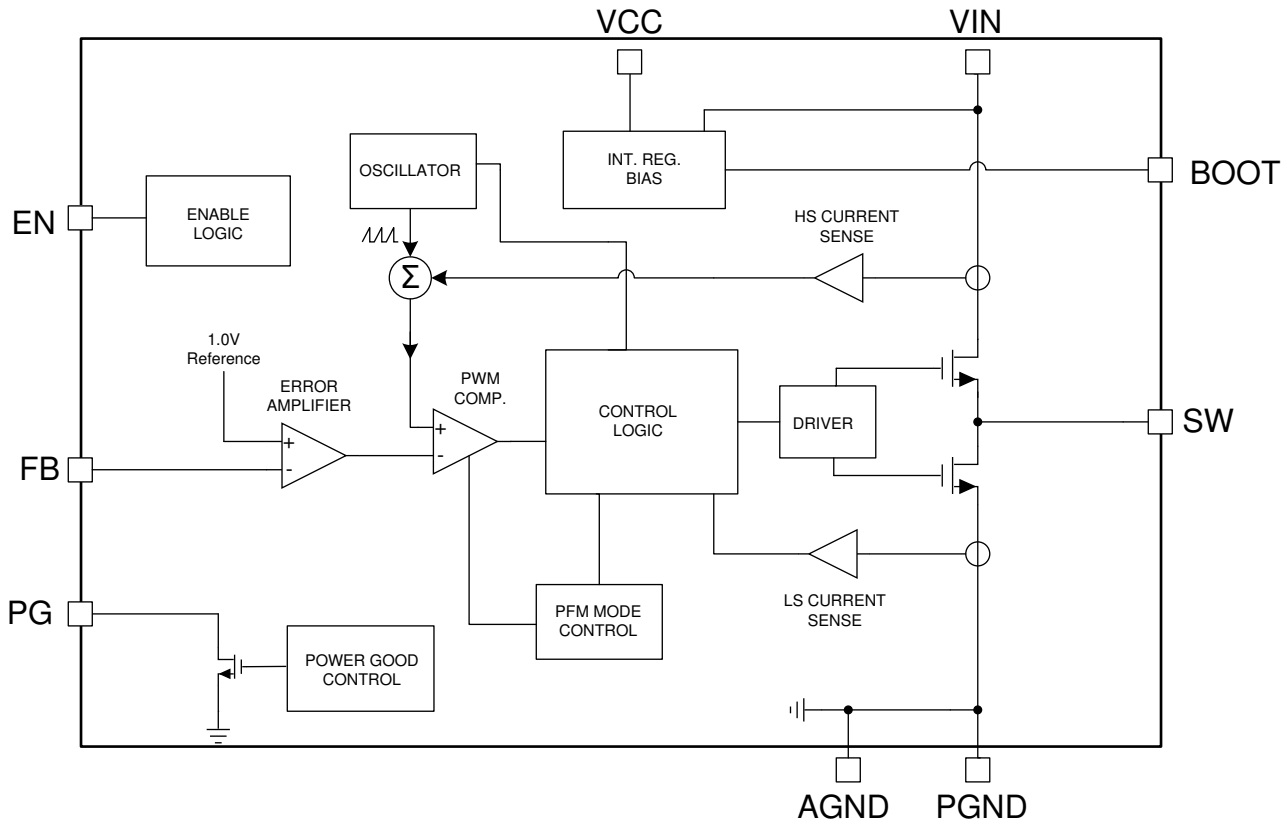
8 Detailed Description

8.1 Overview

The LM604x0-Q1 is a synchronous peak-current-mode buck regulator designed for a wide variety of applications. Advanced high speed circuitry allows the device to regulate from an input voltage of 20 V, while providing an output voltage of 3.3 V. The innovative architecture allows the device to regulate a 3.3-V output from an input of only 3.8 V. The regulator automatically switches modes between PFM and PWM depending on load. At heavy load, the device operates in PWM at a constant switching frequency. At light loads, the mode changes to PFM with diode emulation allowing DCM. This reduces the input supply current and keeps efficiency high. The device features internal loop compensation which reduces design time and requires fewer external components than externally compensated regulators.

The LM604x0-Q1 is available in an ultra-miniature WQFN package with wettable flanks. This enhanced QFN package features extremely small parasitic inductance and resistance, enabling very high efficiency while minimizing switch node ringing and dramatically reducing EMI. The VIN/PGND pin layout is symmetrical on either side of the WQFN package. This allows the input current magnetic fields to partially cancel, resulting in reduce EMI generation.

8.2 Functional Block Diagram



ADVANCE INFORMATION

8.3 Feature Description

8.3.1 Power-Good Flag Output

The power-good flag function (PG output pin) of the LM604x0-Q1 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. The timing parameters of the glitch filter are found in the *Electrical Characteristics* table. Output voltage excursions lasting less than t_{PG} do not trip the power-good flag. Power-good operation can best be understood by reference to 图 1 and 图 2. Note that during initial power up, a delay of about 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

The power-good output consists of an open-drain NMOS, requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either VCC or V_{OUT}, through a 100-kΩ resistor, as desired. If this function is not needed, the PG pin must be left floating. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ≥ 2 V (typical). Limit the current into the power-good flag pin to less than 5 mA D.C. The maximum current is internally limited to about 35 mA when the device is enabled and about 65 mA when the device is disabled. The internal current limit protects the device from any transient currents that can occur when discharging a filter capacitor connected to this output.

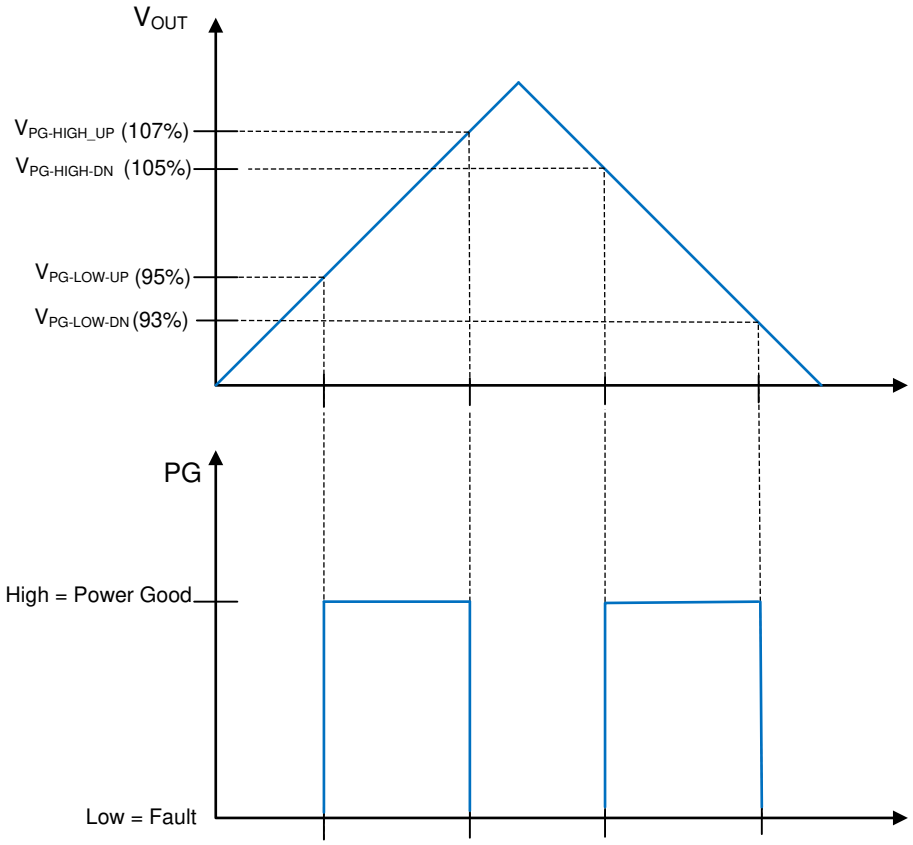


图 1. Static Power-Good Operation

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Feature Description (接下页)

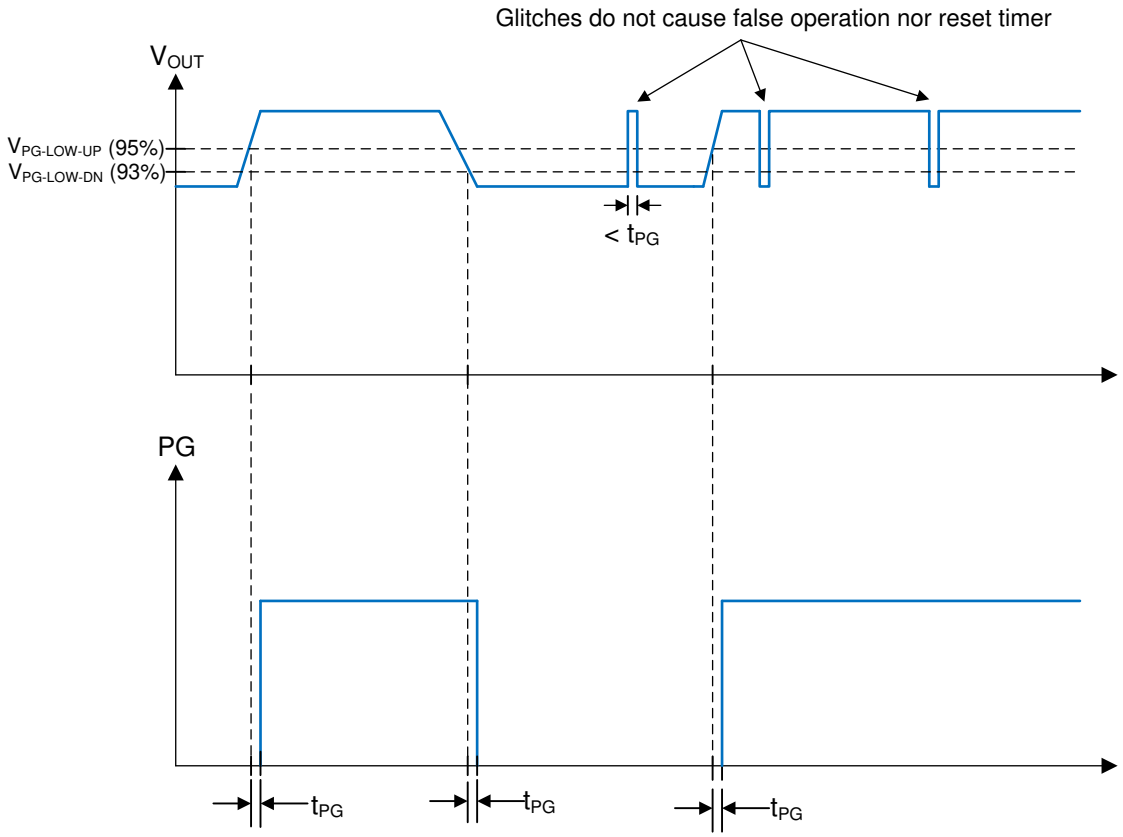


图 2. Power-Good-Timing Behavior

8.3.2 Enable and Start-up

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO (see the *External UVLO* section). Applying a voltage of ≥ V_{EN-VCC_H} causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to V_{EN-H} fully enables the device, allowing it to enter start-up mode and starting the soft-start period. When the EN input is brought below V_{EN-H} by V_{EN-HYS}, the regulator stops running and enters standby mode. Further decrease in the EN voltage to below $V_{EN-VCC-L}$ completely shuts down the device. This behavior is shown in 图 3. The EN input can be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in the *Electrical Characteristics* table.

The LM604x0-Q1 uses a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. A typical start-up waveform is shown in 图 4, indicating typical timings. The rise time of the output voltage is about 4 ms (see the *Electrical Characteristics*).

ADVANCE INFORMATION

Feature Description (接下页)

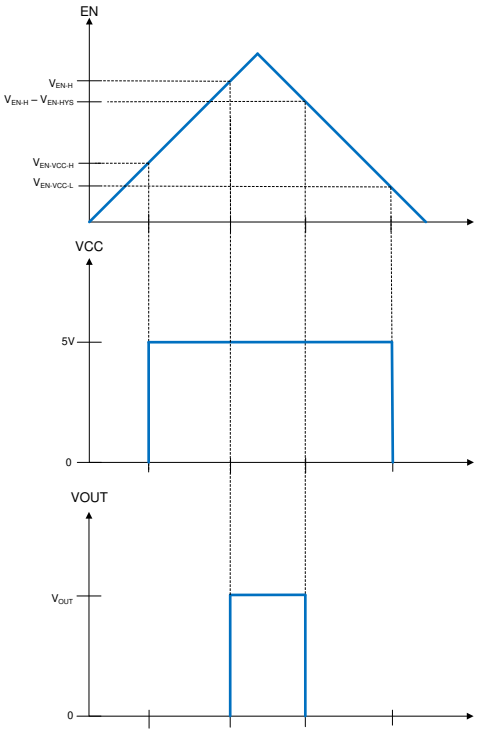


图 3. Precision Enable Behavior

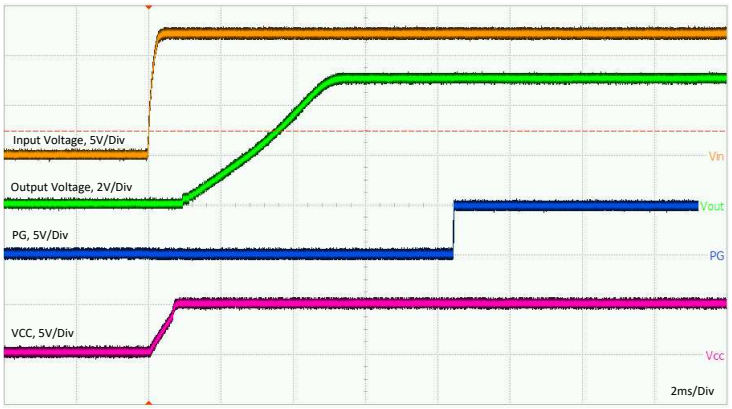


图 4. Typical Start-up Behavior
V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 4 A

8.3.3 Current Limit and Short Circuit

The LM604x0-Q1 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement DEM at light loads (see the *Glossary*). The typical value of this current limit is found under I_{ZC} in the *Electrical Characteristics*.

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Feature Description (接下页)

When the device is overloaded, the valley of the inductor current may not reach below I_{LIMIT} (see the *Electrical Characteristics* table) before the next clock cycle. When this occurs, the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop, and the inductor ripple current to increase. When the peak of the inductor current reaches the high-side current limit, I_{SC} (see the *Electrical Characteristics* table), the switch duty cycle is reduced and the output voltage falls out of regulation. This represents the maximum output current from the converter and is given approximately by 公式 1.

$$I_{OUT}\big|_{max} = \frac{I_{LIMIT} + I_{SC}}{2} \quad (1)$$

If, during current limit, the voltage on the FB input falls below about 0.4 V due to a short circuit, the device enters into hiccup mode. In this mode, the device stops switching for t_{HC} (see the *System Characteristics*), or about 94 ms and then goes through a normal re-start with soft start. If the short-circuit condition remains, the device runs in current limit for about 20 ms (typical) and then shuts down again. This cycle repeats, as shown in 图 5 as long as the short-circuit-condition persists. This mode of operation helps reduce the temperature rise of the device during a hard short on the output. The output current is greatly reduced during hiccup mode. Once the output short is removed and the hiccup delay is passed, the output voltage recovers normally as shown in 图 6.

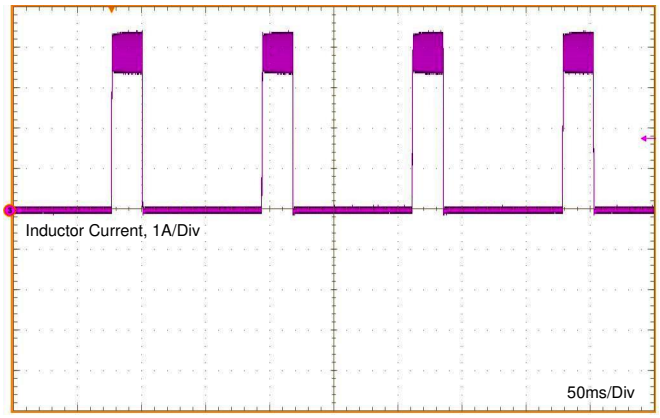


图 5. LM60430-Q1 Inductor Current Burst in Short-Circuit Mode

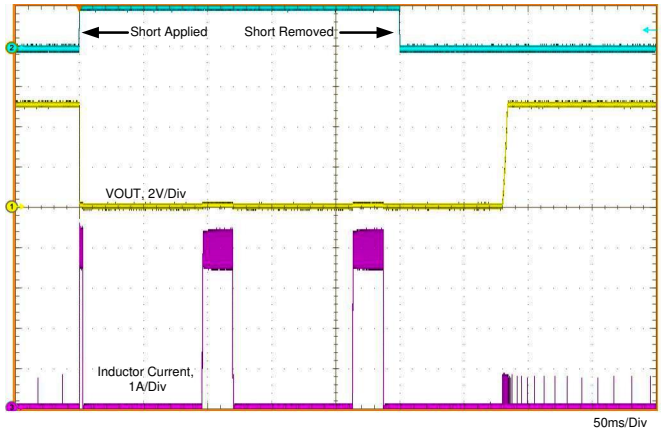


图 6. LM60430-Q1 Short-Circuit Transient and Recovery

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8.3.4 Undervoltage Lockout and Thermal Shutdown

The LM604x0-Q1 incorporates an undervoltage-lockout feature on the output of the internal LDO (at the VCC pin). When VCC reaches about 3.7 V, the device is ready to receive an EN signal and start up. When VCC falls below about 3 V, the device shuts down, regardless of EN status. Because the LDO is in dropout during these transitions, the above values roughly represent the input voltage levels during the transitions.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches about 165°C the device shuts down; re-start occurs when the temperature falls to about 148°C.

8.4 Device Functional Modes

8.4.1 Auto Mode

In auto mode, the device moves between PWM and PFM as the load changes. At light loads, the regulator operates in PFM. At higher loads, the mode changes to PWM. The load current for which the device moves from PFM to PWM can be found in the *Application Curves*. The output current at which the device changes modes depends on the input voltage, inductor value, and the nominal switching frequency. For output currents above the curve, the device is in PWM mode. For currents below the curve, the device is in PFM. The curves apply for a nominal switching frequency of 400 kHz. At higher switching frequencies, the load at which the mode change occurs is greater. For applications where the switching frequency must be known for a given condition, the transition between PFM and PWM must be carefully tested before the design is finalized.

In PWM mode, the regulator operates as a constant frequency converter using PWM to regulate the output voltage. While operating in this mode, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

In PFM, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach $I_{PEAK-MIN}$. The periodicity of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency (see *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at light loads. PFM results in very good light-load efficiency, but also yields larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depends on the input voltage, output voltage, and load. Typical switching waveforms in PFM and PWM are shown in 图 7 and 图 8.

See the *Application Curves* for output voltage variation with load in auto mode.

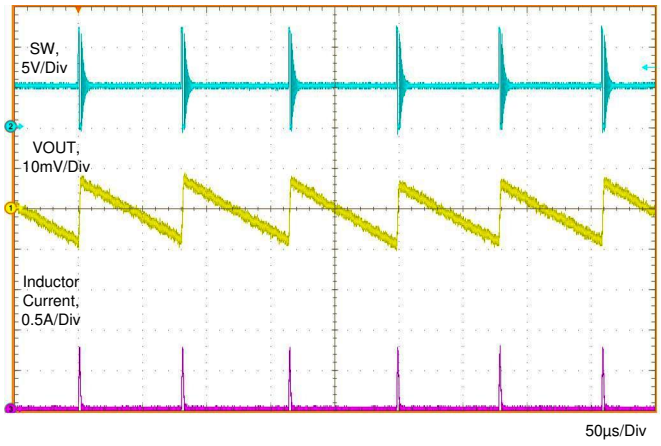


图 7. LM60430-Q1 Typical PFM Switching Waveforms
V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 10 mA

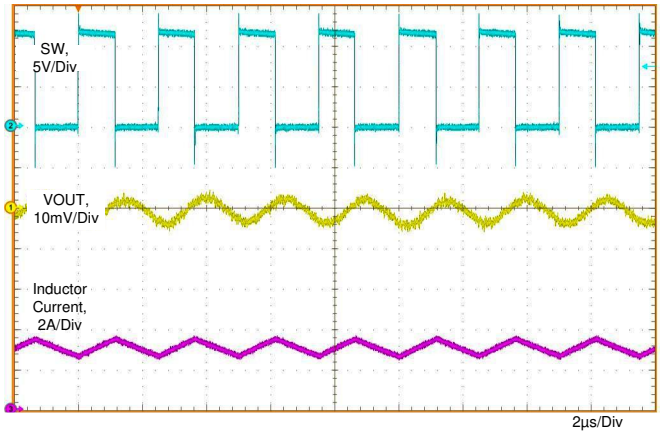


图 8. LM60430-Q1 Typical PWM Switching Waveforms
V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3 A, f_S = 400 kHz

8.4.2 Dropout

The dropout performance of any buck regulator is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor and the maximum duty cycle that the controller can achieve. As the input voltage level approaches the output voltage, the off-time of the high-side MOSFET starts to approach the minimum value (see the *Timing Characteristics*). Beyond this point, the switching can become erratic, and the output voltage falls out of regulation. To avoid this problem, the LM604x0-Q1 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. In this data sheet, the dropout voltage is defined as the difference between the input and output voltage when the output has dropped by 1% of its nominal value. Under this condition, the switching frequency has dropped to its minimum value of about 140 kHz. Note that the 0.4 V short circuit detection threshold is not activated when in dropout mode.

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Device Functional Modes (接下页)

8.4.3 Minimum Switch On-Time

Every switching regulator has a minimum controllable on-time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle and, therefore, a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the LM604x0-Q1 automatically reduces the switching frequency when the minimum on-time limit is reached. This way the converter can regulate the lowest programmable output voltage at the maximum input voltage. An estimate for the approximate input voltage, for a given output voltage, before frequency foldback occurs is found in 公式 2. The values of t_{ON} and f_{SW} can be found in the *Electrical Characteristics* table. As the input voltage is increased, the switch on-time (duty-cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops, while the on-time remains fixed.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \cdot f_{SW}} \tag{2}$$

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM604x0-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 4 A. The following design procedure can be used to select components for the LM604x0-Q1. Alternately, the WEBENCH Design Tool can be used to generate a complete design. This tool utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various options.

注

In this data sheet, the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature; not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias the capacitance drops considerably. Large case sizes and/or higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank should be made in order to ensure that the minimum value of *effective* capacitance is provided.

9.2 Typical Application

图 9 shows a typical application circuit for the LM604x0-Q1. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, 表 2 and 表 3 provide typical component values for a range of the most common output voltages. The values given in the table are typical. Other values can be used to enhance certain performance criterion as required by the application. Note that for the WQFN package, the input capacitors are split and placed on either side of the package; see the *Input Capacitor Selection* section for more details.

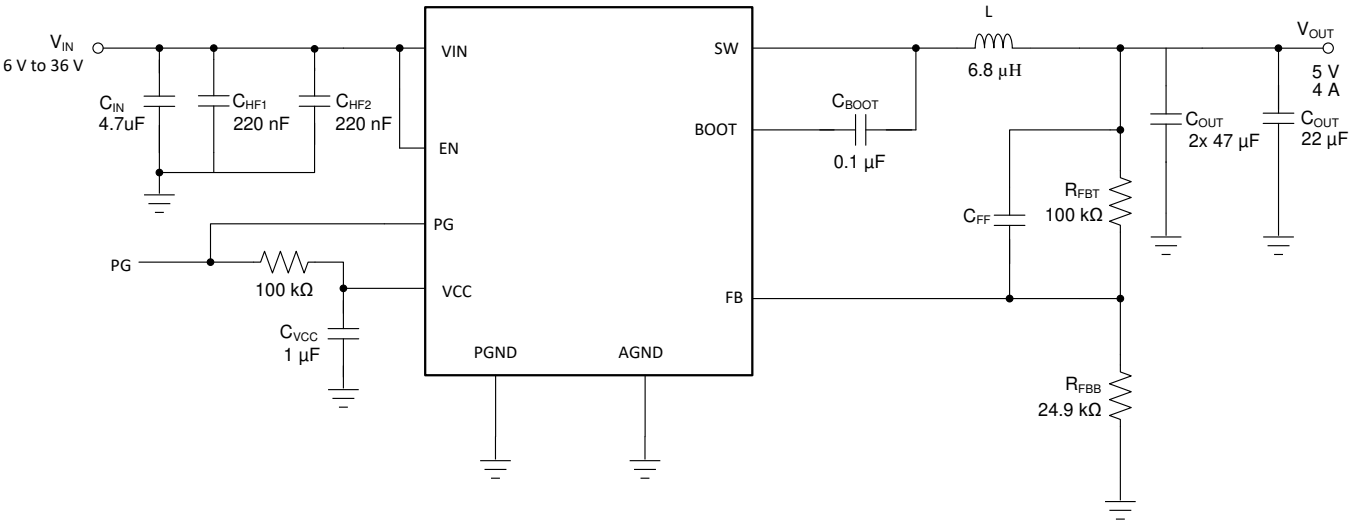


图 9. Example Application Circuit (400 kHz)

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Typical Application (接下页)

9.2.1 Design Requirements

表 1 provides the parameters for our detailed design procedure example:

表 1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V (6 V to 36 V)
Output voltage	5 V
Maximum output current	0 A to 4 A
Switching frequency	400 kHz

表 2. LM60440-Q1 Typical External Component Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (RATED CAPACITANCE)	R_{FBT} (Ω)	R_{FBB} (Ω)	C_{IN} + C_{HF}	C_{BOOT}	C_{VCC}	C_{FF}
400	3.3	4.7	3 × 47 µF	100 k	43.2 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	open
400	5	6.8	2 × 47 µF + 22 µF	100 k	24.9 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	open
400	12	15	2 × 47 µF	100 k	9.09 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	open

表 3. LM60430-Q1 Typical External Component Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (RATED CAPACITANCE)	R_{FBT} (Ω)	R_{FBB} (Ω)	C_{IN} + C_{HF}	C_{BOOT}	C_{VCC}	C_{FF}
400	3.3	5.6	4 × 22 µF	100 k	43.2 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	open
400	5	8.2	4 × 22 µF	100 k	24.9 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	open
400	12	15	4 × 22 µF	100 k	9.09 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	open

9.2.2 Detailed Design Procedure

The following design procedure applies to 图 9 and 表 1.

9.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, and hence a more compact design. For this example, the LM604x0-Q1 fixed 400-kHz switching frequency was chosen.

9.2.2.2 Setting the Output Voltage

The output voltage of the LM604x0-Q1is externally adjustable using a resistor divider network. The range of recommended output voltage is found in the *Recommended Operating Conditions* table. The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The resistance of the divider is a compromise between excessive noise pick-up and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100 kΩ; with a maximum value of 1 MΩ. If a 1 MΩ is selected for R_{FBT}, then a feedforward capacitor must be used across this resistor to provide adequate loop phase margin (see *C_{FF} Selection*). Once R_{FBT} is selected, 公式 3 is used to select R_{FBB}. V_{REF} is nominally 1 V (see the *Electrical Characteristics* for limits).

$$R_{FBB} = \frac{R_{FBT}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]} \quad (3)$$

For this 5-V example, R_{FBT} = 100 kΩ and R_{FBB} = 24.9 kΩ are chosen.

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9.2.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current should be used. 公式 4 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, K = 0.3 was chosen and an inductance was found; the next standard value of 6.8 µH was selected.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUT\,max}} \cdot \frac{V_{OUT}}{V_{IN}} \tag{4}$$

Ideally, the saturation current rating of the inductor must be at least as large as the high-side switch current limit, I_{SC} (see the *Electrical Characteristics*). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage; do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing for some relaxation in the current rating of the inductor. However, they have more core losses at frequencies typically above 1 MHz. In any case, the inductor saturation current must not be less than the device low-side current limit, I_{LIMIT} (see the *Electrical Characteristics*). The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

9.2.2.4 Output Capacitor Selection

The value of the output capacitor and the ESR of the capacitor determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements, rather than the output voltage ripple. 公式 5 can be used to estimate a lower bound on the total output capacitance and an upper bound on the ESR, which is required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[(1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[1 + K + \frac{K^2}{12} \cdot \left(1 + \frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = ripple factor from *Inductor Selection*

(5)

Once the output capacitor and ESR have been calculated, 公式 6 can be used to check the peak-to-peak output voltage ripple; V_r.

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}} \tag{6}$$

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

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For this example, a $\Delta V_{OUT} \leq 300$ mV for an output current step of $\Delta I_{OUT} = 4$ A is required. 公式 5 gives a minimum value of 86 µF and a maximum ESR of 0.022 Ω. Assuming a 20% tolerance and a 10% bias de-rating, you arrive at a minimum capacitance of 111 µF. This can be achieved with 2 × 47-µF and a 22-uF, 16-V ceramic capacitors in the 1210 case size. More output capacitance can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases, an aluminum electrolytic capacitor can be placed in parallel with the ceramics to help build up the required value of capacitance. In general, use a capacitor of at least 10 V for output voltages of 3.3 V or less and a capacitor of 16 V or more for output voltages of 5 V and above.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and Bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing voltage spikes on the output caused by inductor and board parasitics.

The maximum value of total output capacitance must be limited to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

9.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10 µF of ceramic capacitance is required on the input of the LM604x0-Q1. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size, 220-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example a 4.7-µF, 50-V, X7R (or better) ceramic capacitor is chosen. The 220 nF must also be rated at 50 V with an X7R dielectric. The WQFN package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split, and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. In this example, a single 4.7-µF and two 100-nF ceramic capacitors at each VIN/PGND location.

Many times, it is desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate worst case RMS value of this current can be calculated from 公式 7 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{7}$$

9.2.2.6 C_{BOOT}

The LM604x0-Q1 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 10 V is required.

9.2.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see the *Power-Good Flag Output* section). A value of 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 5 V; see the *Electrical Characteristics* for limits. Do not short this output to ground or any other external voltage.

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9.2.2.8 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of R_{FBT}, in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A C_{FF} can help to mitigate this effect. 公式 8 can be used to estimate the value of C_{FF}. The value found with 公式 8 is a starting point; use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor. The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feed-forward Capacitor Application Report* is helpful when experimenting with a feedforward capacitor.

$$C_{FF} < \frac{V_{OUT} \cdot C_{OUT}}{120 \cdot R_{FBT} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{8}$$

9.2.2.9 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 图 10. The input voltage at which the device turns on is designated V_{ON}; while the turnoff voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ and then 公式 9 is used to calculate R_{ENT} and V_{OFF}.

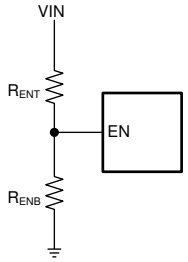


图 10. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left(1 - \frac{V_{EN-HYS}}{V_{EN-H}} \right)$$

where

- $V_{ON} = V_{IN}$ turnon voltage
- $V_{OFF} = V_{IN}$ turnoff voltage

(9)

9.2.2.10 Maximum Ambient Temperature

As with any power conversion device, the LM604x0-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss and the effective thermal resistance, $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LM604x0-Q1 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and therefore the load current. 公式 10 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the value of $R_{\theta JA}$ given in the *Thermal Information* table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

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$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (10)$$

where

- η = efficiency

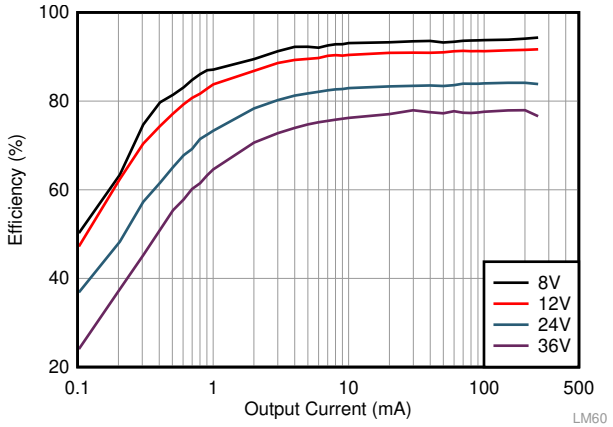
The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as power dissipation, air temperature/flow, PCB area, copper heat-sink area, number of thermal vias under the package, and adjacent component placement; to mention just a few. The copper area given in the graph is for each layer; the top and bottom layers are 2 oz. copper each, while the inner layers are 1 oz. It must be remembered that the data given in these graphs are for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.

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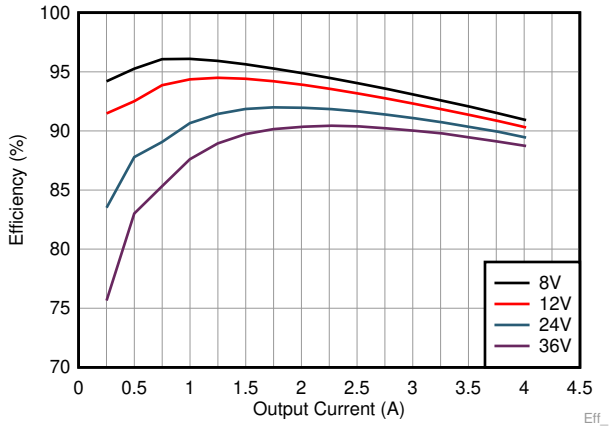
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25°C. The circuit is shown in 图 17, with the appropriate BOM from 表 4.



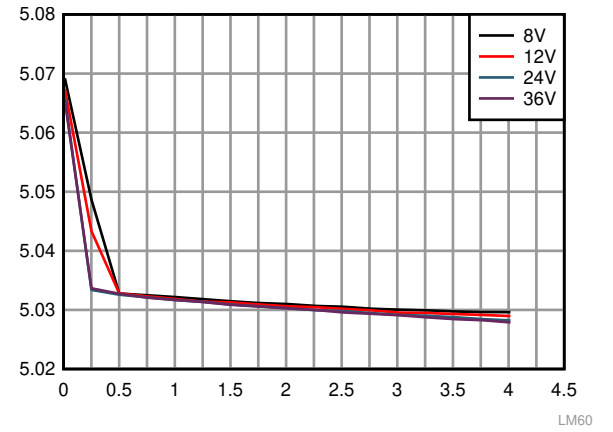
V_{OUT} = 5 V 400 kHz

图 11. Low-Load Efficiency



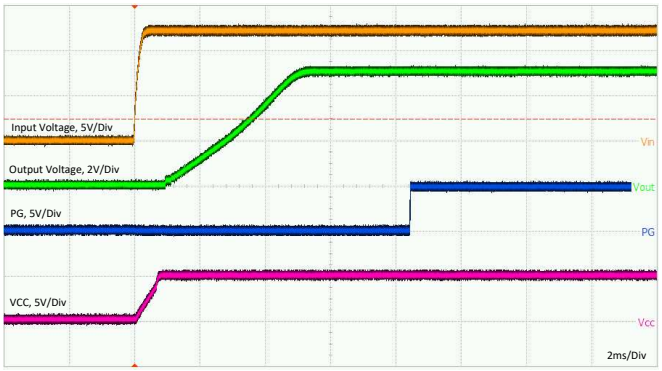
V_{OUT} = 5 V 400 kHz

图 12. High-Load Efficiency



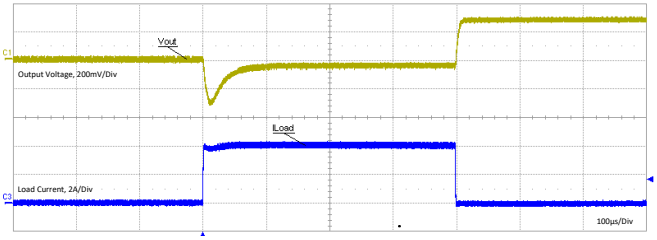
V_{OUT} = 5 V

图 13. Line and Load Regulation



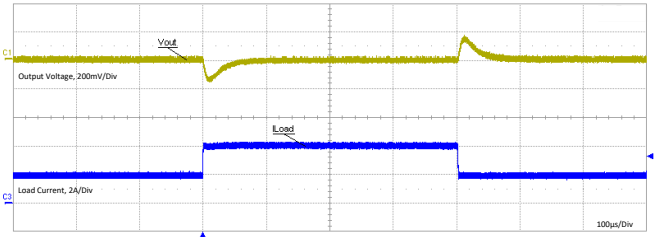
V_{IN} = 13.5 V V_{OUT} = 5 V I_{OUT} = 4 A

图 14. Start-up



V_{IN} = 12 V V_{OUT} = 5 V
I_{OUT} = 0 A to 4 A $t_f = t_r$ = 4 µs

图 15. Load Transient



V_{IN} = 12 V V_{OUT} = 5 V
$t_f = t_r$ = 2 µs I_{OUT} = 2 A to 4 A

图 16. Load Transient

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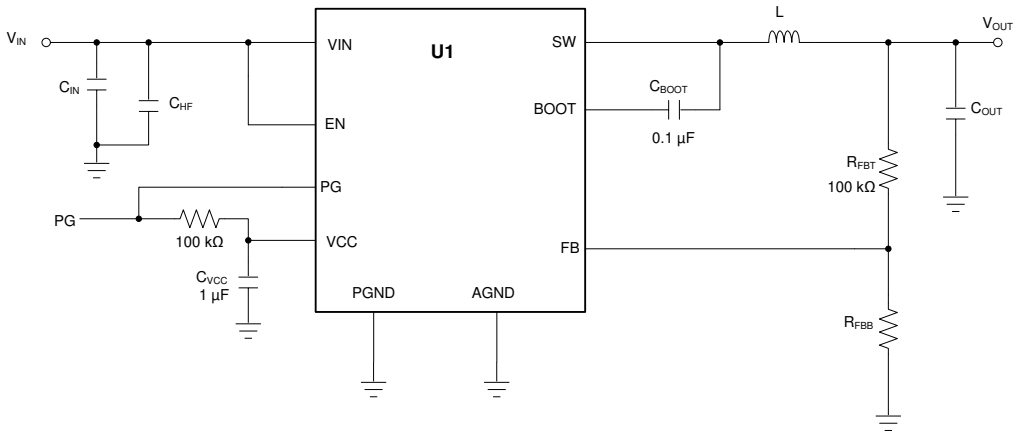


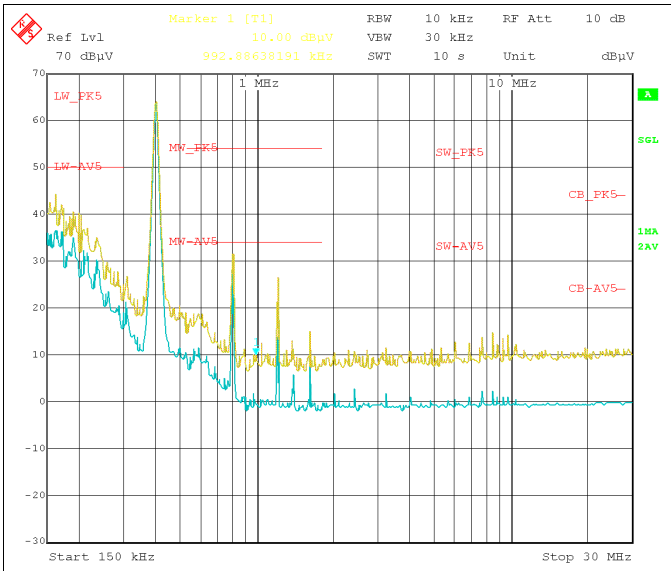
图 17. Circuit for Application Curves

表 4. BOM for Typical Application Curves

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT}	C_{IN} + C_{HF}	L	U1
5 V	400 kHz	24.9 k	2 x 47 µF + 22µF	4.7 µF + 2 × 220 nF	6.8 µH, 20.8 mΩ	LM60440AQRPKRQ1

9.3 EMI

EMI results depend critically on PCB layout and test setup. The results presented here are typical and given for information purposes only. The EMI filter used is shown in 图 20. The limit lines shown refer to CISPR25 class 5.

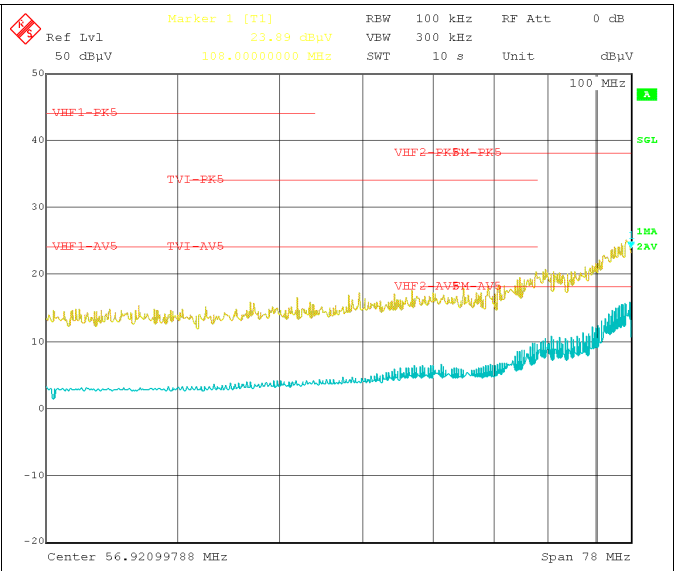


V_{IN} = 13.5 V
f_{SW} = 400 kHz

V_{OUT} = 5 V

I_{OUT} = 4 A
WQFN package

图 18. Low Frequency Conducted EMI



V_{IN} = 12 V
f_{SW} = 400 kHz

V_{OUT} = 5 V

I_{OUT} = A
WQFN package

图 19. High Frequency Conducted EMI

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EMI (接下页)

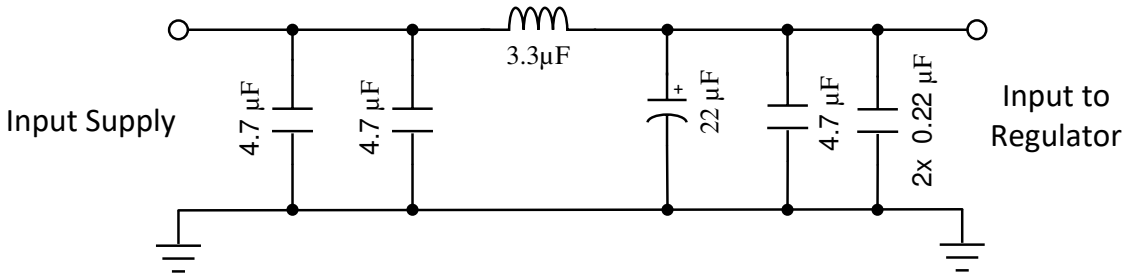


图 20. Typical Input EMI Filter
Filter Used Only for EMI Measurements Found in EMI

9.4 What to Do and What Not to Do

- **Don't:** Exceed the *Absolute Maximum Ratings*.
- **Don't:** Exceed the *ESD Ratings*.
- **Don't:** Exceed the *Recommended Operating Conditions* .
- **Don't:** Allow the EN input to float.
- **Don't:** Allow the output voltage to exceed the input voltage, nor go below ground.
- **Don't:** Use the value of $R_{\theta JA}$ given in the *Thermal Information* table to design your application. Us the information in the *Maximum Ambient Temperature* section.
- **Do:** Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.

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10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 公式 11, where η is the efficiency.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{11}$$

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under damped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help damp the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The user guide *AN-2162 Simple Success With Conducted EMI From DCDC Converters* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharges through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then a Schottky diode between the input supply and the output should be used.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or input capacitors, and power ground, as shown in 图 21. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages will disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance.

1. ***Place the input capacitor or capacitors as close as possible to the VIN and GND terminals.*** VIN and GND pins are adjacent, simplifying the input capacitor placement. With the WQFN package there are two VIN/PGND pairs on either side of the package. This provides for a symmetrical layout and helps minimize switching noise and EMI generation. A wide VIN plane must be used on a lower layer to connect both of the VIN pairs together to the input supply; see 图 22.
2. ***Place bypass capacitor for VCC close to the VCC pin.*** This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. ***Use wide traces for the C_{BOOT} capacitor.*** Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins.
4. ***Place the feedback divider as close as possible to the FB pin of the device.*** Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. ***Use at least one ground plane in one of the middle layers.*** This plane acts as a noise shield and also act as a heat dissipation path.
6. ***Provide wide paths for VIN, VOUT, and GND.*** Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. ***Provide enough PCB area for proper heat sinking.*** As stated in the *Maximum Ambient Temperature* section, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
8. ***Keep switch area small.*** Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time the total area of this node should be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies*
- *Simple Switcher PCB Layout Guidelines*
- *Construction Your Power Supply- Layout Considerations*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x*

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Layout Guidelines (接下页)

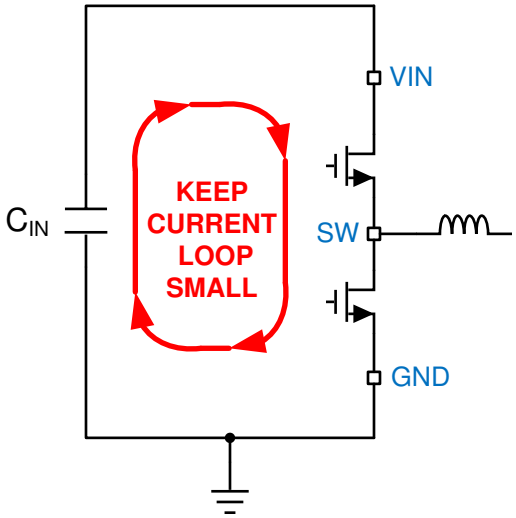


图 21. Current Loops with Fast Edges

11.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding, and lower thermal resistance.

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11.2 Layout Example

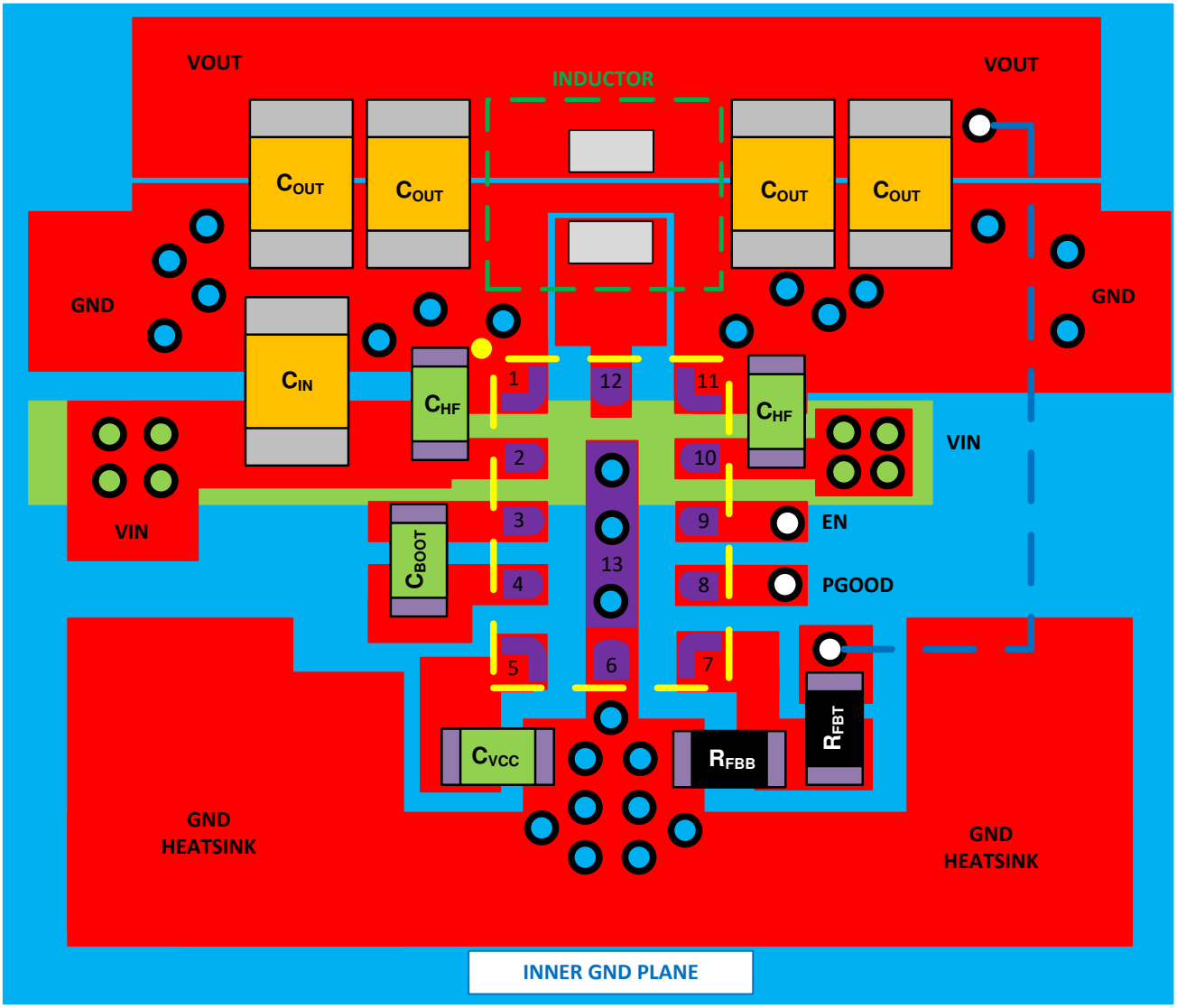


图 22. Example Layout for WQFN Package

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12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 使用 WEBENCH® 工具创建定制设计方案

请单击此处，使用 LM60440-Q1 器件并借助 WEBENCH® 电源设计器创建定制设计。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- *《热设计：学会洞察先机，不做事后诸葛》*
- *《外露焊盘封装实现最佳热阻性的电路板布局指南》*
- *《半导体和 IC 封装热指标》*
- *《使用 LM43603 和 LM43602 简化热设计》*
- *《PowerPAD™ 热增强型封装》*
- *《PowerPAD™ 速成》*
- *《使用新的热指标》*
- *《开关电源布局指南》*
- *《Simple Switcher PCB 布局指南》*
- *《构建电源 - 布局注意事项》*
- *《使用 LM4360x 与 LM4600x 简化低辐射 EMI 布局》*

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.5 商标

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WEBENCH is a registered trademark of Texas Instruments.
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12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM60430AQRPKRQ1	Active	Production	WQFN-HR (RPK) | 13	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6430AQ
LM60430AQRPKRQ1.A	Active	Production	WQFN-HR (RPK) | 13	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6430AQ
LM60440AQRPKRQ1	Active	Production	WQFN-HR (RPK) | 13	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6440AQ
LM60440AQRPKRQ1.A	Active	Production	WQFN-HR (RPK) | 13	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6440AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM60430-Q1, LM60440-Q1 :

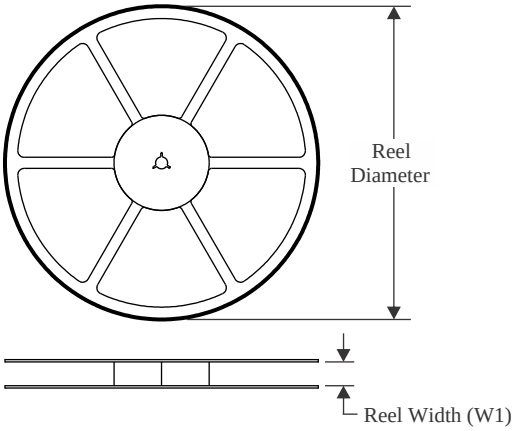
- Catalog : LM60430, LM60440

NOTE: Qualified Version Definitions:

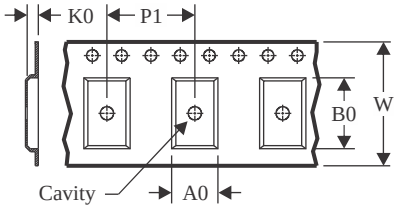
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

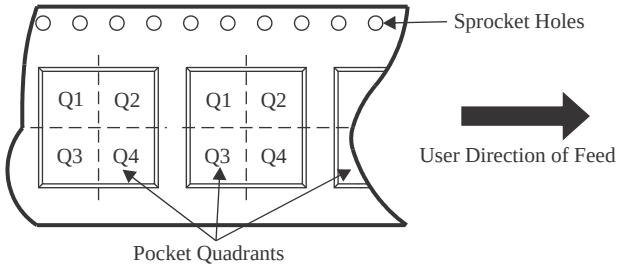


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

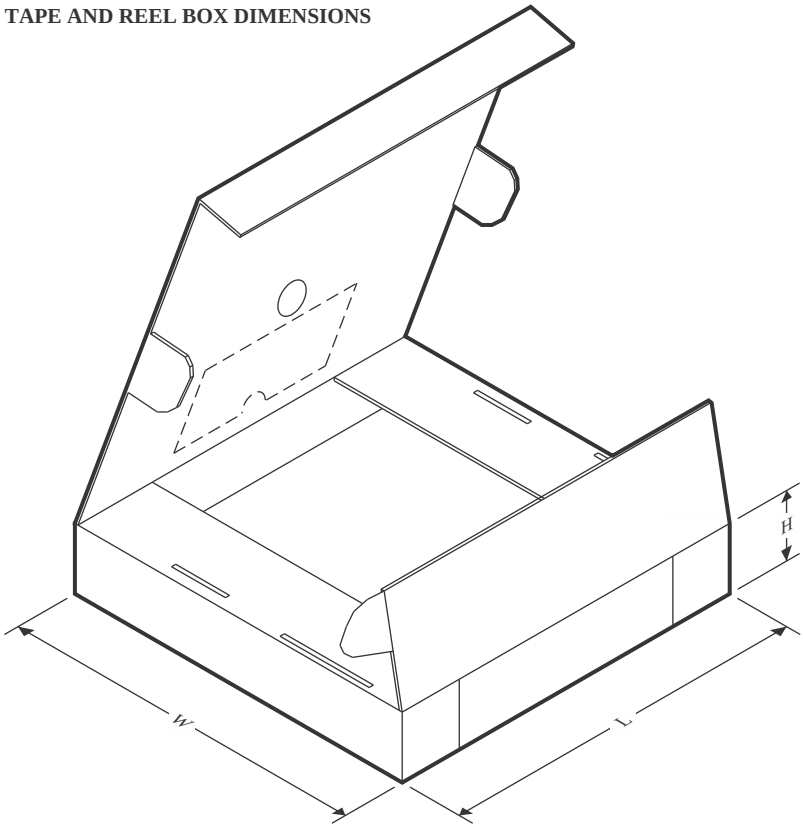
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM60430AQRPKRQ1	WQFN-HR	RPK	13	3000	180.0	12.5	2.2	3.2	0.9	4.0	12.0	Q1
LM60440AQRPKRQ1	WQFN-HR	RPK	13	3000	180.0	12.5	2.2	3.2	0.9	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

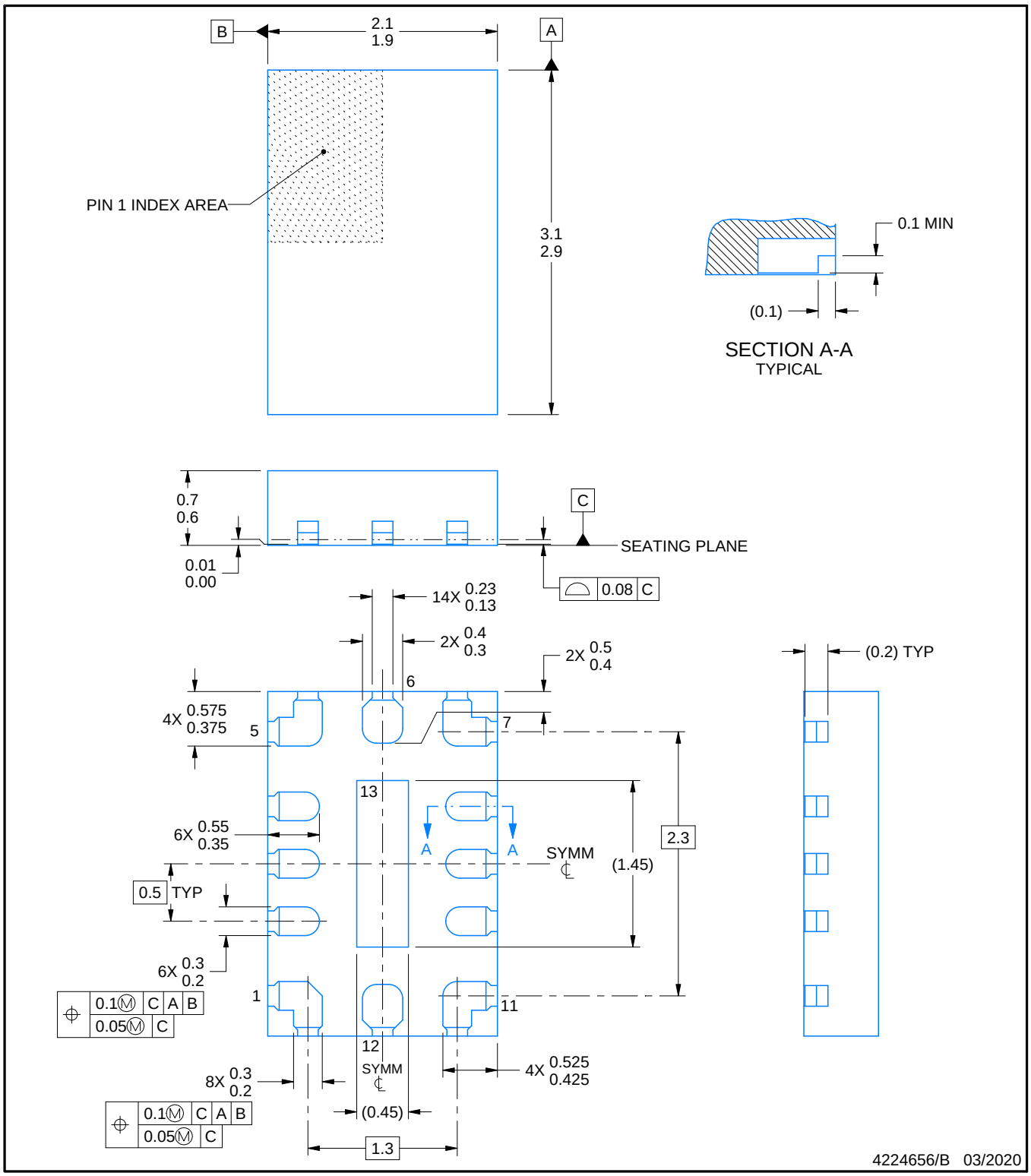
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM60430AQRPKRQ1	WQFN-HR	RPK	13	3000	205.0	200.0	33.0
LM60440AQRPKRQ1	WQFN-HR	RPK	13	3000	205.0	200.0	33.0

PACKAGE OUTLINE

RPK0013A

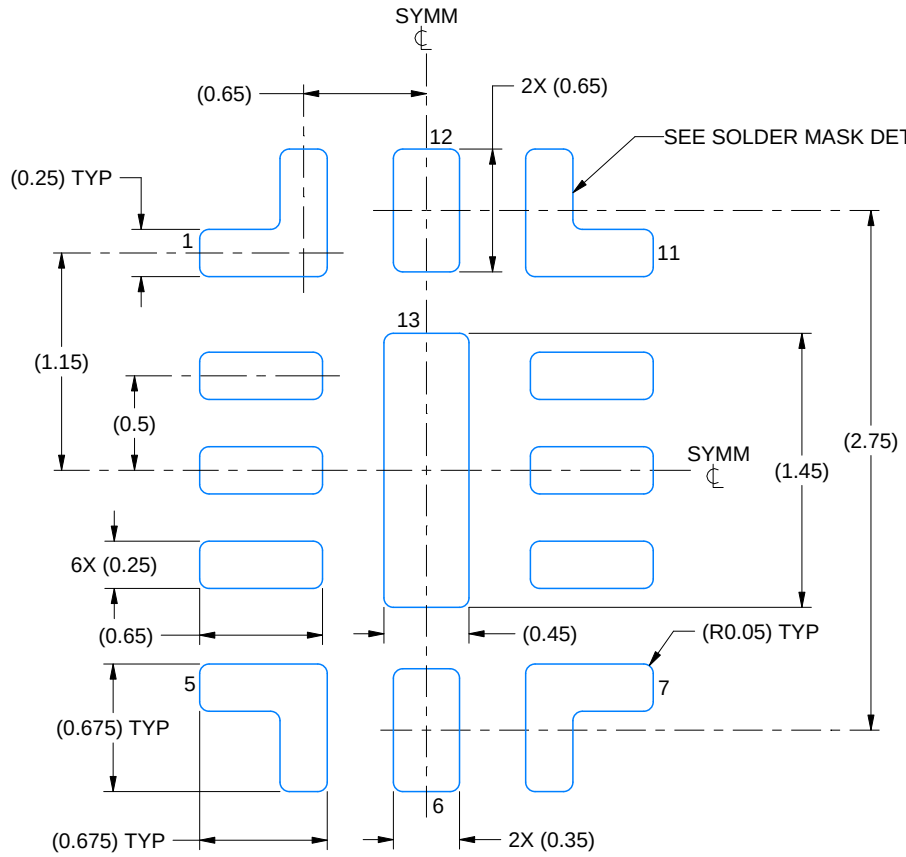
WQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

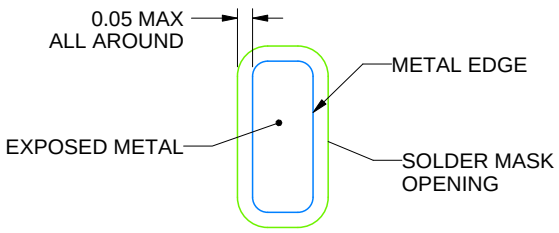


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



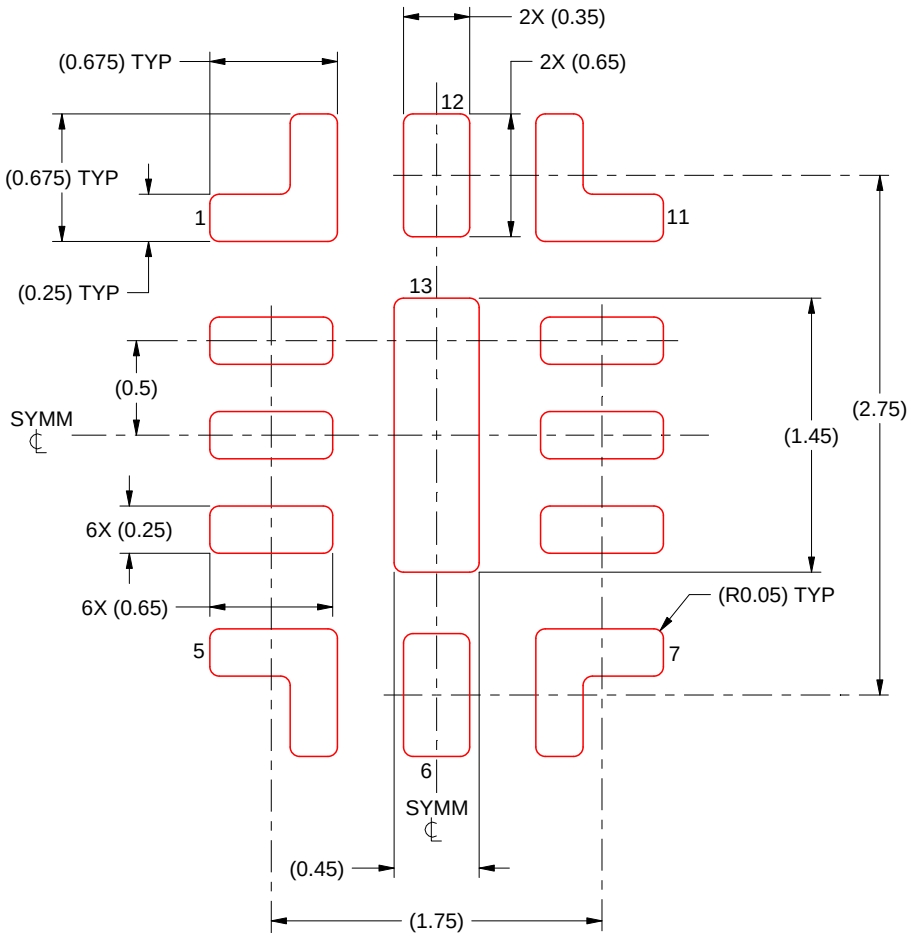
NON SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4224656/B 03/2020

NOTES: (continued)

3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
100% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

4224656/B 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月