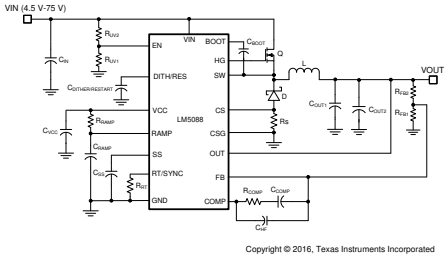
LM5088、LM5088-Q1 宽输入范围非同步降压控制器

1 特性

- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C5
- 仿真电流模式控制
- 驱动外部高侧 N 沟道 MOSFET
- 4.5V 至 75V 的超宽输入电压范围
- 低 I_Q 关断和待机模式
- 高占空比功能可降低压差
- 展频 EMI 降低 (LM5088-1)
- 用于过载保护的断续计时器 (LM5088-2)
- 可调节输出电压从 1.205V 开始，反馈基准精度为 1.5%
- 宽带宽误差放大器
- 单个电阻振荡器频率设置
- 振荡器同步功能
- 可编程软启动
- 高压、低压差偏置稳压器
- 热关断保护
- 16 引脚 HTSSOP 封装

2 应用

- 汽车信息娱乐系统
- 汽车 USB 配件适配器
- 工业直流/直流偏置和电机驱动器



简化版原理图

3 说明

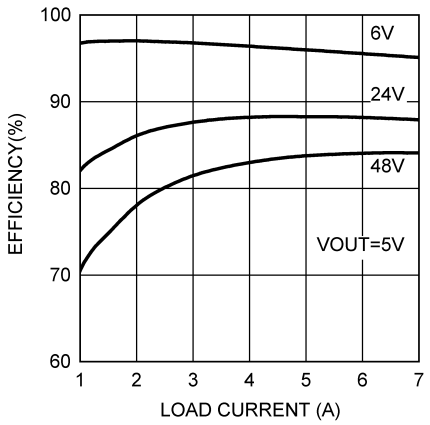
LM5088 高电压非同步降压控制器具有使用尽可能少的外部元件实现高效、高压降压转换器所需的所有功能。LM5088 可配置为在 4.5V 至 75V 的超宽输入电压范围内工作。这款易于使用的控制器包括一个电平转换栅极驱动器，能够控制外部 N 沟道降压开关。此控制方法基于采用仿真电流斜坡的峰值电流模式控制。通过使用仿真电流斜坡可降低脉宽调制电路的噪声灵敏度，从而对高输入电压和低输出电压应用中所需的极小占空比进行可靠控制。LM5088 具有 50kHz 至 1MHz 的可编程开关频率。

LM5088 有两个版本：LM5088-1 提供 ±5% 频率抖动功能以降低传导和辐射 EMI，而 LM5088-2 提供通用重启计时器以提供过载保护。其他特性包括低压差偏置稳压器、用于控制关断和待机模式的三电平使能输入、软启动和振荡器同步能力。此器件采用热增强型 16 引脚 HTSSOP 封装。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
LM5088	HTSSOP (16)	5.00mm × 4.00mm
LM5088-Q1		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用电路频率

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (August 2014) to Revision J (June 2022) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 ... 1
- 将 AEC-Q100 要点更新为新标准 ... 1
- 更正了整个文档中的语法错误 ... 1
- Added EP as pin 17 ... 3
- Changed all instances of legacy terminology to controller ... 3
- Moved storage temperature from *ESD Ratings* to *Absolute Maximum Ratings* ... 5
- Changed unit and value from kV to V in *ESD Ratings* ... 5
- Changed Handling Ratings to ESD Ratings ... 5
- Moved storage temperature to Absolute Maximum Ratings ... 5
- Added new ESD ratings table for LM5088-Q1 ... 5
- Added application and implementation note ... 21

Changes from Revision H (March 2013) to Revision I (March 2013) — **Page**

- 更改了数据表流程和布局，以符合新的 TI 新标准。添加了*器件信息* 表、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- Changed (VIN × V_{OUT}) to (VIN – V_{OUT}) in *Ramp Generator* equation ... 13
- Added unit kΩ to the standard value chosen for the *Timing Resistor* equation ... 21
- Deleted /A from the numerator of the *Current Sense Resistor* equation ... 24

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5 Pin Configuration and Functions

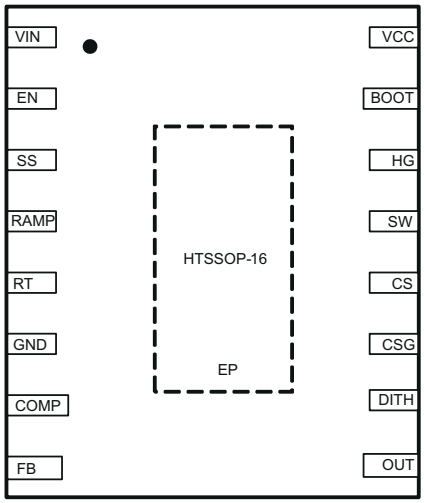


图 5-1. 16-Pin PWP Package (Dither Version) (Top View)

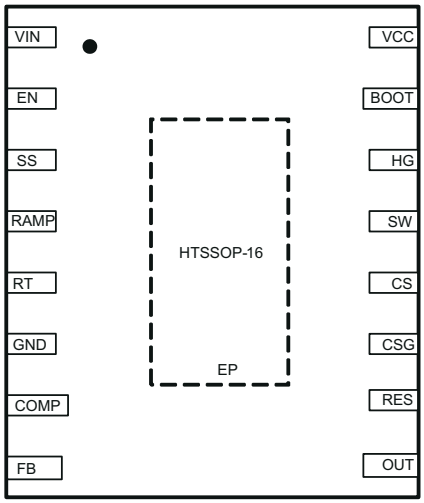


图 5-2. 16-Pin PWP Package (Restart Version) (Top View)

表 5-1. Pin Functions

Pin		Description	Application Information
Number	Name		
1	VIN	Input supply voltage	IC supply voltage. The operating range is 4.5 V to 75 V.
2	EN	Enable input	If the EN pin voltage is below 0.4 V, the regulator is in a low power state. If the EN pin voltage is between 0.4 V and 1.2 V, the controller is in standby mode. If the EN pin voltage is above 1.2 V, the controller is operational. An external voltage divider can be used to set a line undervoltage shutdown threshold. If the EN pin is left open, a 5-µA pullup current forces the pin to the high state and enables the controller.
3	SS	Soft start	When SS is below the internal 1.2-V reference, the SS voltage controls the error amplifier. An internal 11-µA current source charges an external capacitor to set the start-up rate of the controller. The SS pin is held low in the standby, VCC UV, and thermal shutdown states. The SS pin can be used for voltage tracking by connecting this pin to a controller voltage supply less than 1.2 V. The applied voltage acts as the reference for the error amplifier.
4	RAMP	Ramp control signal	An external capacitor connected between this pin and the GND pin sets the ramp slope used for emulated current mode control. The recommended capacitor range 100 pF to 2000 pF. See 节 8 for selection of capacitor value.
5	RT/SYNC	Internal oscillator frequency set input and synchronization input	The internal oscillator is programmed with a single resistor between this pin and the GND pin. The recommended frequency range is 50 kHz to 1 MHz. An external synchronization signal, which is higher in frequency than the programmed frequency, can be applied to this pin through a small coupling capacitor. The RT resistor to ground is required even when using external synchronization.
6	GND	Ground	Ground return
7	COMP	Output of the internal error amplifier	The loop compensation network must be connected between this pin and the FB pin.
8	FB	Feedback signal from the regulated output	This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.205 V.
9	OUT	Output voltage connection	Connect this pin directly to the regulated output voltage.
10	DITH	Frequency Dithering (LM5088-1 Only)	A capacitor connected between DITH pin and GND is charged and discharged by 27-µA current sources. As the voltage on the DITH pin ramps up and down, the oscillator frequency is modulated between –5% to +5% of the nominal frequency set by the RT resistor. Grounding the DITH pin disables the frequency dithering mode.

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表 5-1. Pin Functions (continued)

Pin		Description	Application Information
Number	Name		
10	RES	Hiccup Mode Restart (LM5088-2 Only)	The RES pin is normally connected to an external capacitor that sets the timing for hiccup mode current limiting. In normal operation, a 25-µA current source discharges the RES pin capacitor to ground. If cycle-by-cycle current limit threshold is exceeded during any PWM cycle, the current sink is disabled and RES capacitor is charged by an internal 50-µA current. If the RES voltage reaches 1.2 V, the HG pin gate drive signal is disabled and the RES pin capacitor is discharged by a 1-µA current sink. Normal operation resumes when the RES pin falls below 0.2 V.
11	CSG	Current Sense Ground	Low-side reference for the current sense resistor
12	CS	Current sense	Current measurement connection for the re-circulating diode. An external sense resistor and an internal sample and hold circuit sense the diode current at the conclusion of the buck switch off time. This current measurement provides the DC offset level for the emulated current ramp.
13	SW	Switching node	Connect this pin to the source terminal of the external MOSFET switch.
14	HG	High gate	Connect this pin to the gate terminal of the external MOSFET switch.
15	BOOT	Input for bootstrap capacitor	An external capacitor is required between the BOOT and the SW pins to provide bias to the MOSFET gate driver. The capacitor is charged from VCC via an internal diode during the off-time of the buck switch.
16	VCC	Output of the bias regulator	VCC tracks VIN up to the regulation level (7.8 V typical). A 0.1-µF to 10-µF ceramic decoupling capacitor is required. An external voltage between 8.3 V and 13 V can be applied to this pin to reduce internal power dissipation.
17	EP	Exposed pad	Exposed pad of the package. Electrically isolated. Must be soldered to the ground plane to reduce thermal resistance.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

	MIN	MAX	UNIT
VIN, V_{OUT} to GND		76	V
BOOT to GND		90	V
SW to GND	–2	76	V
VCC to GND	–0.3	16	V
HG to SW	–0.3	BOOT + 0.3	V
EN to GND		14	V
BOOT to SW	–0.3	16	V
CS, CSG to GND	–0.3	0.3	V
All other inputs to GND	–0.3	7	V
Junction temperature		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings: LM5088

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per JESD22- A114 (1)	±2000	V
		Charged Device Model (CDM), per JESD22-C101 (2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LM5088-Q1

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged Device Model (CDM), per AEC Q100-011	All pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN voltage	4.5	75	V
VCC voltage (externally supplied)	8.3	13	V
Operation junction temperature	–40	125	°C

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6.5 Thermal Information

THERMAL METRIC(1)		LM5088/LM5088-Q1 PWP 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

See (2) (4)

PARAMETER		TEST CONDITIONS	T_J = –40°C to +125°C			T_J = 25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IN} SUPPLY									
I_{BIAS}	V_{IN} operating current	V_{FB} = 1.3 V			5.5		3.8		mA
$I_{STANDBY}$	V_{IN} standby current	V_{EN} = 1 V			3.6		2.9		mA
$I_{SHUTDOWN}$	V_{IN} shutdown current	V_{EN} = 0 V			26		15		µA
VCC REGULATOR									
$V_{VCC(Reg)}$	VCC regulation	V_{VCC} = open	7.4		8.2		7.8		V
$V_{VCC(Reg)}$	VCC regulation	V_{VIN} = 4.5 V, V_{VCC} = open	4.3		4.5				V
	VCC sourcing current limit	V_{VCC} = 0	30				35		mA
$V_{VCC(UV)}$	VCC undervoltage lockout threshold	Positive going VVCC	3.7		4.2		4		V
	VCC undervoltage hysteresis						200		mV
ENABLE THRESHOLDS									
	EN shutdown threshold	V_{EN} rising	320		480		400		mV
	EN shutdown hysteresis	V_{EN} falling					100		mV
	EN standby threshold	V_{EN} rising	1.1		1.3		1.2		V
	EN standby hysteresis	V_{EN} falling					120		mV
	EN pullup current source	V_{EN} = 0 V					5		µA
SOFT START									
	SS pullup current source	V_{SS} = 0 V	8		13		11		µA
	FB to SS offset	V_{FB} = 1.3 V					150		mV
ERROR AMPLIFIER									
V_{REF}	FB reference voltage	Measured at FB pin FB = COMP	1.187		1.223		1.205		V
	FB input bias current	V_{FB} = 1.2 V			100		18		nA
	COMP sink and source current		3						mA
AOL	DC gain						60		dB
FBW	Unity gain bandwidth						3		MHz
PWM COMPARATORS									
$t_{HG(OFF)}$	Forced HG off time		185		365		280		ns
$t_{ON(MIN)}$	Minimum HG on time	V_{VIN} = 60 V					55		ns
	COMP to PWM comparator offset						930		mV
OSCILLATOR (RT PIN)									
		LM5088-2 (non-dithering)							

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See (2) (4)

PARAMETER		TEST CONDITIONS	T_J = –40°C to +125°C			T_J = 25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{nom1}	Nominal oscillator frequency	R_{RT} = 31.6 kΩ	180		220		200		kHz
f_{nom2}		R_{RT} = 11.3 kΩ	430		565		500		kHz
		LM5088-1 (dithering)							
f_{min}	Dithering range	Minimum dither frequency					f_{nom} – 5%		kHz
f_{max}		Maximum dither frequency					f_{nom} + 5%		kHz
SYNC									
	SYNC positive threshold						2.3		V
	SYNC pulse width		15		150				ns
CURRENT LIMIT									
$V_{CS(TH)}$	Cycle-by-cycle sense voltage threshold	V_{RAMP} = 0 V	112		136		120		mV
	Cycle-by-cycle current limit delay	V_{RAMP} = 2.5 V					280		ns
	Buck switch VDS protection	VIN to SW					1.5		V
CURRENT LIMIT RESTART (RES Pin)									
V_{resup}	RES threshold upper (rising)	V_{CS} = 0.125	1.1		1.3		1.2		V
$V_{resdown}$	RES threshold lower (falling)		0.1		0.3		0.2		V
I_{charge}	Charge source current	$V_{CS} \geqslant 0.125$	40		65		50		µA
$I_{discharge}$	Discharge sink current	V_{CS} < 0.125	20		34		27		µA
$I_{rampdown}$	Discharge sink current (post fault)		0.8		1.6		1.2		µA
RAMP GENERATOR(1)									
I_{RAMP1}	RAMP current 1	V_{VIN} = 60 V, V_{OUT} = 10 V	235		345		295		µA
I_{RAMP2}	RAMP current 2	V_{VIN} = 10 V, V_{OUT} = 10 V	18		30		25		µA
	V_{OUT} bias current	V_{OUT} = 48 V					250		µA
	RAMP output low voltage	V_{VIN} = 60 V, V_{OUT} = 10 V					200		mV
HIGH SIDE (HG) GATE DRIVER									
V_{OLH}	HG low-state output voltage	I_{HG} = 100 mA			215		115		mV
V_{OHH}	HG high-state output voltage	I_{HG} = – 100 mA, $V_{OHH} = V_{BOOT} - V_{HG}$					240		mV
	HG rise time	C_{load} = 1000 pF					12		ns
	HG fall time	C_{load} = 1000 pF					6		ns
I_{OHH}	Peak HG source current	V_{HG} = 0 V					1.5		A
I_{OLH}	Peak HG sink current	$V_{HG} = V_{VCC}$					2		A
	BOOT UVLO	BOOT to SW					3		V
Pre $R_{DS(ON)}$	Pre-charge switch ON resistance	I_{VCC} = 1 mA					72		Ω
	Pre-charge switch on time						300		ns
THERMAL(3)									
T_{SD}	Thermal shutdown temperature	Junction temperature rising					165		°C
	Thermal shutdown hysteresis	Junction temperature falling					25		°C

(1) RAMP and COMP are output pins. As such they are not specified to have an external voltage applied.
(2) Typical specifications represent the most likely parametric norm at 25°C operation.
(3) For detailed information on soldering plastic HTSSOP packages, visit www.ti.com/packaging.
(4) Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{VIN} = 48 V, V_{VCC} = 8 V, V_{EN} = 5 V, R_{RT} = 31.6 kΩ. No load on HG.

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6.7 Typical Characteristics

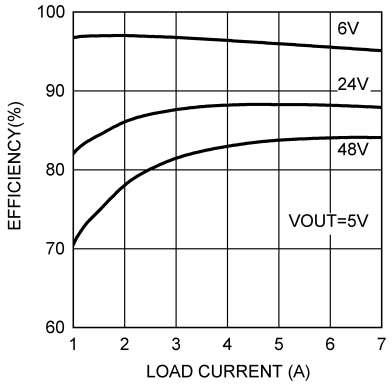


图 6-1. Typical Application Circuit Efficiency

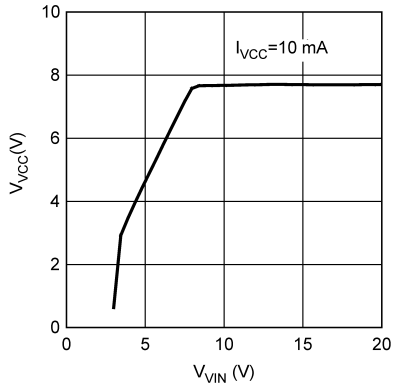


图 6-2. V_{CC} vs V_{IN}

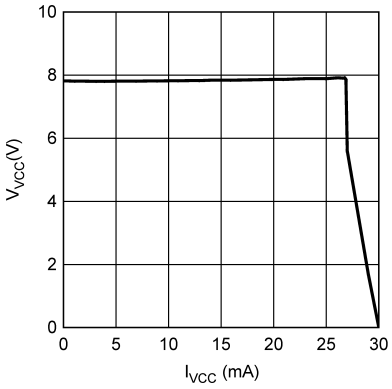


图 6-3. V_{VCC} vs I_{VCC}

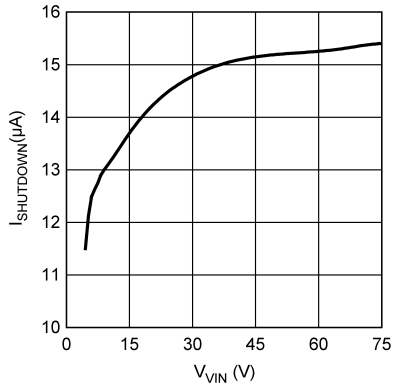


图 6-4. Shutdown Current

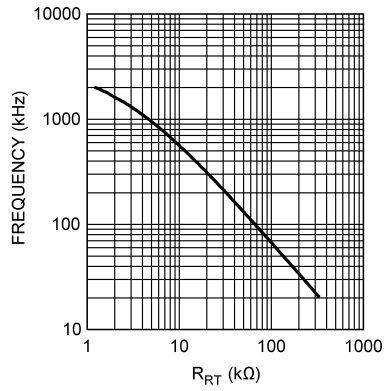


图 6-5. Frequency vs R_{RT}

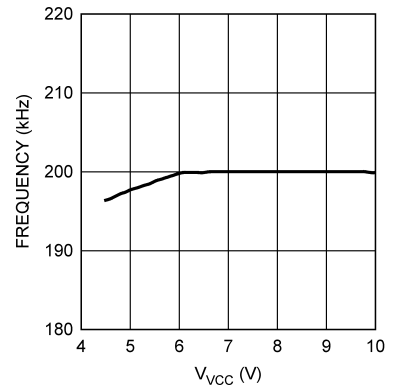


图 6-6. Frequency vs V_{VCC}

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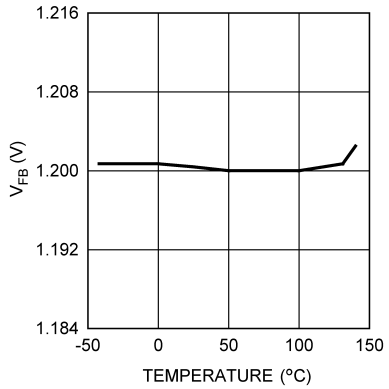


图 6-7. V_{FB} vs Temperature

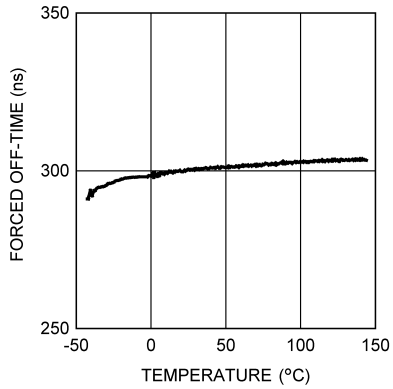


图 6-8. Forced Off Time vs Temperature

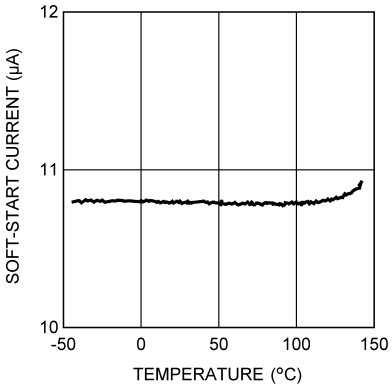


图 6-9. Soft Start vs Temperature

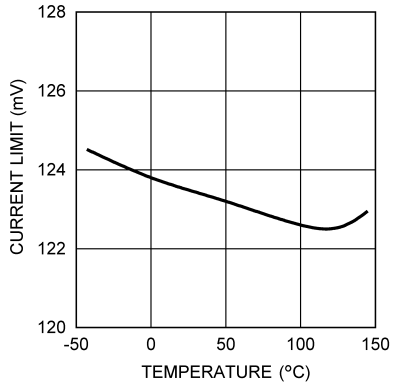


图 6-10. Current Limit vs Temperature

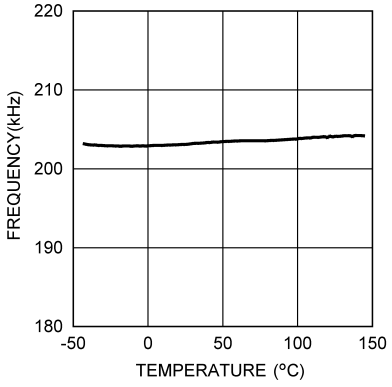


图 6-11. Frequency vs Temperature

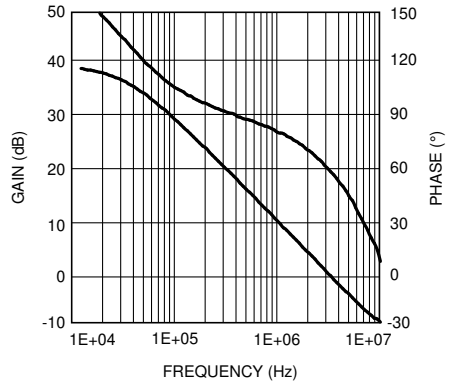


图 6-12. Error Amplifier Gain and Phase

7 Detailed Description

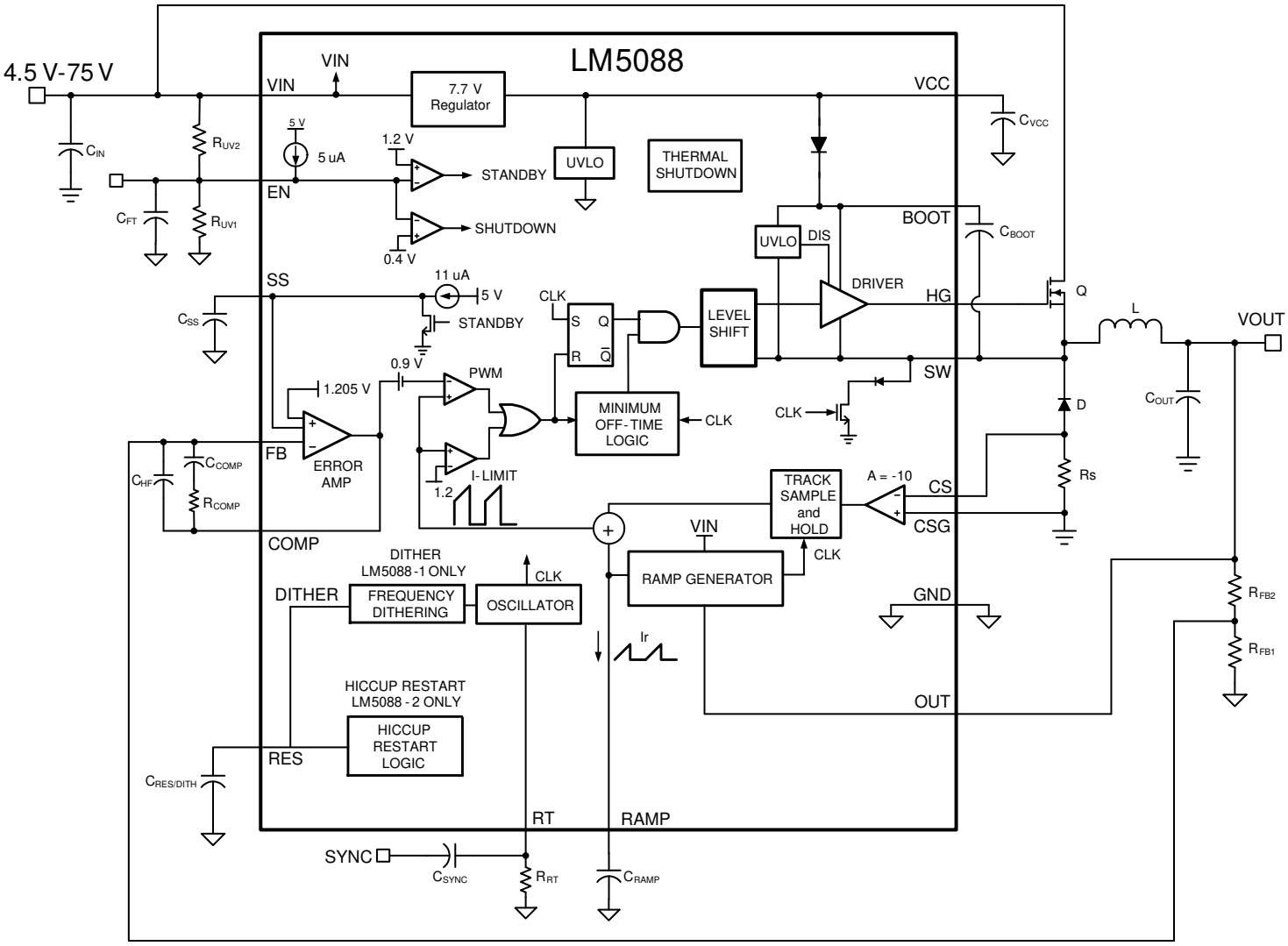
7.1 Overview

The LM5088 wide input range buck controller features all the functions necessary to implement an efficient high voltage step-down converter using a minimum number of external components. The control method is based on peak current mode control utilizing an emulated current ramp. Peak current mode control provides inherent line voltage feedforward, cycle-by-cycle current limiting, and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of very small duty cycles necessary in high input voltage applications. The operating frequency is user programmable from 50 kHz to 1 MHz. The LM5088-1 provides a ±5% frequency dithering function to reduce the conducted and radiated EMI, while the LM5088-2 provides a versatile restart timer for overload protection. Additional features include the low dropout bias regulator, tri-level enable input to control shutdown and standby modes, soft start, and voltage tracking and oscillator synchronization capability. The device is available in a thermally enhanced HTSSOP-16 pin package.

See 图 7-1 and 图 9-1. The LM5088 is well suited for a wide range of applications where efficient step-down of high, unregulated input voltage is required. The typical applications for the LM5088 include telecom, industrial, and automotive.

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7.2 Functional Block Diagram



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图 7-1. LM5088 Functional Block Diagram

7.3 Feature Description

7.3.1 High Voltage Low-Dropout Regulator

The LM5088 contains a high voltage, low-dropout regulator that provides the VCC bias supply for the controller and the bootstrap MOSFET gate driver. The input pin (VIN) can be connected directly to an input voltage as high as 75 V. The output of the VCC regulator (7.8 V) is internally current limited to 30 mA. Upon power up, the regulator sources current into the capacitor connected to the VCC pin. When the voltage at the VCC pin exceeds the upper VCC UV threshold of 4 V and the EN pin is greater than 1.2 V, the output (HG) is enabled and a soft-start sequence begins. The output is terminated if VCC falls below its lower UV threshold (3.8 V) or the EN pin falls below 1.1 V. When VIN is less than VCC regulation point of 7.8 V, then the internal pass device acts as a switch. Thereby, VCC tracks VIN with a voltage drop determined by the $R_{DS(ON)}$ of the internal switch and operating current of the controller. The required VCC capacitor value is dependent on system start-up characteristics with a minimum value no less than 0.1 µF.

An auxiliary supply voltage can be applied to the VCC pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 8.2 V, the internal regulator is disabled. The VCC regulator series pass transistor includes a diode between VCC and VIN that must not be forward biased in normal operation.

In high voltage applications, take care to ensure that the VIN pin does not exceed the absolute maximum voltage rating of 76 V. During line or load transients, voltage ringing on the VIN pin that exceeds the absolute maximum ratings can damage the IC. Both careful PC board layout and the use of high quality bypass capacitors located close to the VIN and GND pins are essential.

7.3.2 Line Undervoltage Detector

The LM5088 contains a dual-level undervoltage lockout (UVLO) circuit. When the EN pin is below 0.4 V, the controller is in a low current shutdown mode. When the EN pin is greater than 0.4 V but less than 1.2 V, the controller is in a standby mode. In standby mode, the VCC regulator is active, but the output switch is disabled and the SS pin is held low. When the EN pin exceeds 1.2 V and VCC exceeds the VCC UV threshold, the SS pin and the output switch is enabled and normal operation begins. An internal 5-µA pullup current source at the EN pin configures the controller to be fully operational if the EN pin is left open.

An external VIN UVLO set-point voltage divider from VIN to GND can be used to set the minimum start-up input voltage of the controller. The divider must be designed such that the voltage at the EN pin exceeds 1.2 V (typical) when VIN is in the desired operating range. The internal 5-µA pullup current source must be included in calculations of the external set-point divider. 100 mV of hysteresis is included for both shutdown and standby thresholds. The EN pin is internally connected to a 1-kΩ resistor and an 8-V zener clamp. If the voltage at the EN pin exceeds 8 V, the bias current for the EN pin increases at the rate of 1 mA/V. The voltage at the EN pin should never exceed 14 V.

7.3.3 Oscillator and Sync Capability

The LM5088 oscillator frequency is set by a single external resistor connected between the RT pin and the GND pin. The R_T resistor must be located very close to the device. To set a desired oscillator frequency (f_{SW}), the necessary value of R_T resistor can be calculated from the following equation:

$$R_{RT} = \frac{\frac{1}{f_{SW}} - 280\ ns}{152\ pF} \quad (1)$$

The RT pin can also be used to synchronize the internal oscillator to an external clock. The internal oscillator is synchronized to an external clock by AC coupling a positive edge into the RT/SYNC pin. The RT/SYNC pin voltage must exceed 3 V to trip the internal clock synchronization pulse detector. The free-running frequency should be set nominally 15% below the external clock frequency and the pulse width applied to the RT/SYNC pin must be less than 150 ns. Synchronization to an external clock more than twice the free-running frequency can produce abnormal behavior of the pulse-width modulator.

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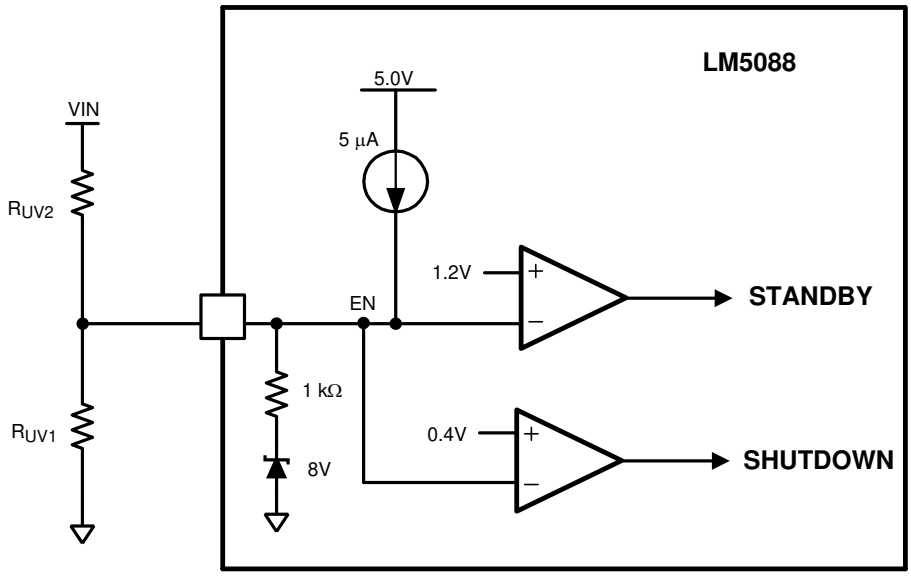


图 7-2. Basic Enable Configuration

7.3.4 Error Amplifier and PWM Comparator

The internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision voltage reference (1.205 V). The output of the error amplifier is connected to the COMP pin, allowing the user to connect loop compensation components. Generally a type II network, as illustrated in 图 7-1, is sufficient. This network creates a pole at DC, a mid-band zero for phase boost and a high frequency pole for noise reduction. The PWM comparator compares the emulated current signal from the RAMP generator to the error amplifier output voltage at the COMP pin. A typical control loop gain and phase plot is shown in 节 6.7.

7.3.5 Ramp Generator

The ramp signal used for the pulse width modulator in current mode control is typically derived directly from the buck switch current. This signal corresponds to the positive slope portion of the buck inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feedforward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics which must be filtered or blanked. Also, the current measurement can introduce significant propagation delays. The filtering time, blanking time, and propagation delay limit the minimum achievable pulse width. In applications where the input voltage can be relatively large in comparison to the output voltage, controlling small pulse widths and duty cycles are necessary for regulation. The LM5088 utilizes a unique ramp generator, which does not actually measure the buck switch current but rather reconstructs or emulates the signal. Emulating the inductor current provides a ramp signal that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements: a sample and hold DC level and an emulated current ramp.

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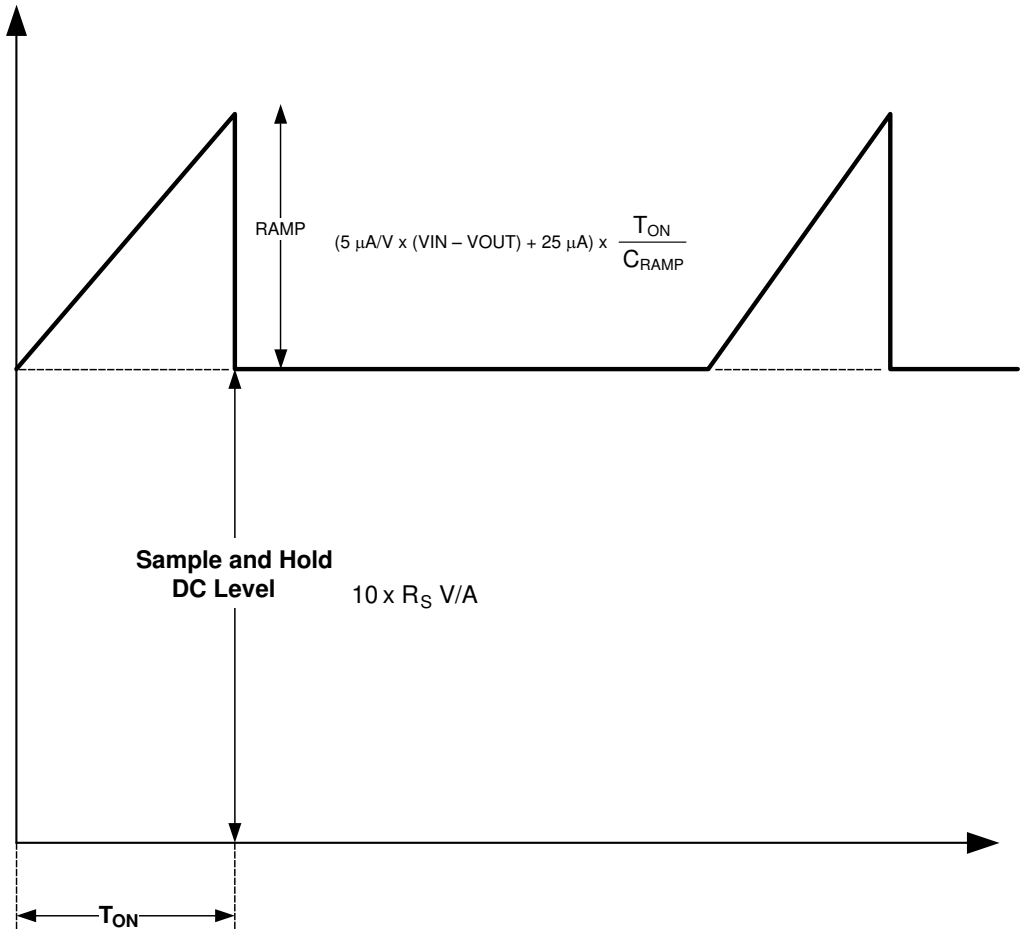


图 7-3. Composition of Current Sense Signal

The sample and hold DC level illustrated in 图 7-3 is derived from a measurement of the re-circulating (or free-wheeling) diode current. The diode current flows through the current sense resistor connected between the CS and CSG pins. The voltage across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The diode current sensing and sample and hold provide the DC level for the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to GND and an internal voltage controlled current source. The ramp current source that emulates the inductor current is a function of the V_{IN} and V_{OUT} voltages per the following equation:

$$I_{RAMP} = 5\ \mu A/V \times (VIN - V_{OUT}) + 25\ \mu A \quad (2)$$

Proper selection of the RAMP capacitor depends upon the selected value of the output inductor and the current sense resistor (R_S). For proper current emulation, the DC sample and hold value and the ramp amplitude must have the same dependence on the load current. That is:

$$C_{RAMP} = \frac{g_m \times L}{R_S \times A} \quad (3)$$

where

- g_m is the ramp current generator transconductance (5 µA/V).
- A is the gain of the current sense amplifier (10 V/V).

The RAMP capacitor must connected directly to the RAMP and GND pins of the IC.

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For duty cycles greater than 50%, peak current mode control circuits are subject to subharmonic oscillation. Subharmonic oscillation is normally characterized by alternating wide and narrow pulses at the SW pin. Adding a fixed slope voltage ramp (slope compensation) to the current sense signal prevents this oscillation. The 25-µA offset current supplied by the emulated current source provides a fixed slope to the ramp signal. In some high output voltage, high duty cycles applications, additional slope compensation can be required. In these applications, a pullup resistor can be added between the RAMP and VCC pins to increase the ramp slope compensation. A formula to configure pullup resistor is shown in 节 8.

7.3.6 Dropout Voltage Reduction

The LM5088 features unique circuitry to reduce the dropout voltage. Dropout voltage is defined as the difference between the minimum input voltage to maintain regulation and the output voltage ($V_{IN(min)}$ – V_{OUT}). Dropout voltage thus determines the lowest input voltage at which the converter maintains regulation. In a buck converter, dropout voltage primarily depends upon the maximum duty cycle. The maximum duty cycle is dependent on the oscillator frequency and minimum off time.

An approximation for the dropout voltage is:

$$\text{Dropout_Voltage} = V_{OUT} \times \frac{T_{OFF(max)}}{T_{OSC} - T_{OFF(max)}} \tag{4}$$

where

- $T_{OSC} = 1 / f_{SW}$.
- $T_{OFF\ (max)}$ is the forced off time (280 ns typical, 365 ns maximum).
- f_{SW} is the oscillator frequency.
- T_{OSC} is the oscillator period.

From the above equation, it can be seen that for a given output voltage, reducing the dropout voltage requires either reducing the forced off time or oscillator frequency ($1/T_{OSC}$). The forced off time is limited by the time required to replenish the bootstrap capacitor and time required to sample the re-circulating diode current. The 365-ns forced off time of the LM5088 controller is a good trade-off between these two requirements. Thus, the LM5088 reduces dropout voltage by dynamically decreasing the operating frequency during dropout. The dynamic frequency control (DFC) is achieved using a dropout monitor, which detects a dropout condition and reduces the operating frequency. The operating frequency continues to decrease with decreasing input voltage until the frequency falls to the minimum value set by the DFC circuitry.

$$f_{SW(minDFC)} \cong 1 / 3 \times f_{SW(nominal)} \tag{5}$$

If the V_{IN} voltage continues to fall below this point, output regulation can no longer be maintained. The oscillator frequency reverts back to the nominal operating frequency set by the RT resistor when the input voltage increases above the dropout range. DFC circuitry does not affect the PWM during normal operating conditions.

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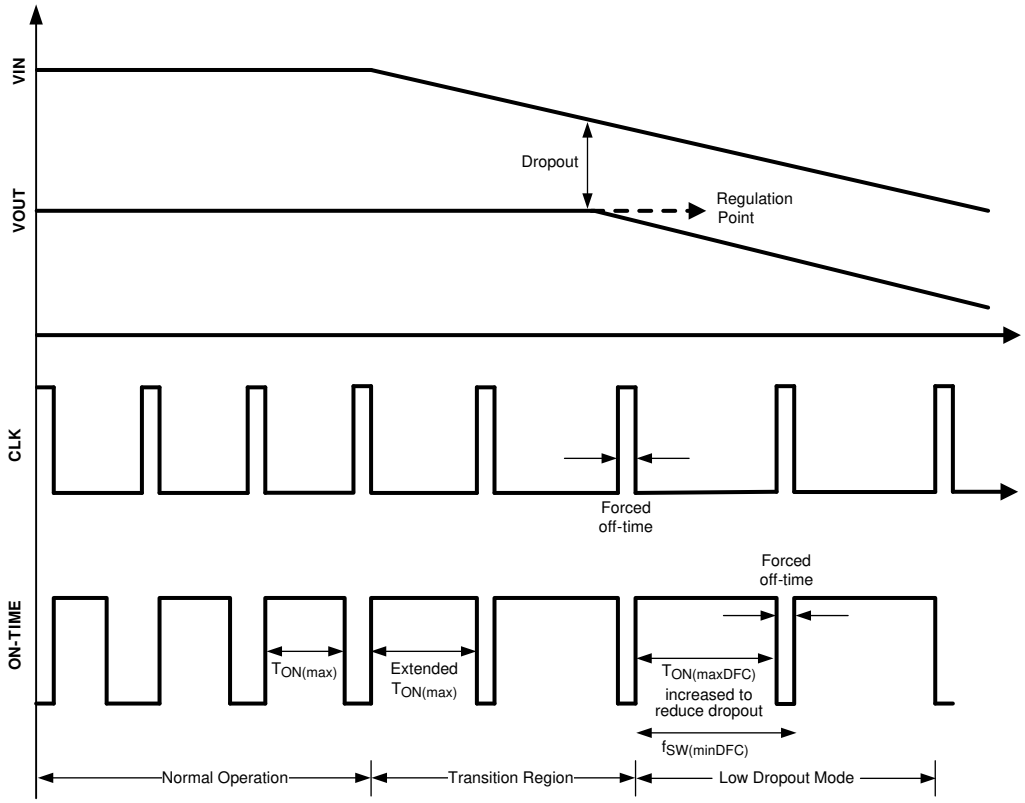


图 7-4. Dropout Voltage Reduction using Dynamic Frequency Control

7.3.7 Frequency Dithering (LM5088-1 Only)

Electromagnetic interference (EMI) emissions are fundamentally associated with switch-mode power supplies due to sharp voltage transitions, diode reverse recovery currents, and the ringing of parasitic L-C circuits. These emissions conduct back to the power source or radiate into the environment and potentially interfere with nearby electronic systems. System designers typically use a combination of shielding, filtering, and layout techniques to reduce the EMI emissions sufficiently to satisfy EMI emission standards established by regulatory bodies. In a typical fixed frequency switching converter, narrowband emissions typically peak at the switching frequency with the successive harmonics having less energy. Dithering the oscillator frequency spreads the EMI energy over a range of frequencies, thus reducing the peak levels. Dithering can also reduce the system cost by reducing the size and quantity of EMI filtering components.

The LM5088-1 provides an optional frequency dithering function, which is enabled by connecting a capacitor from the dither pin (DITH) to GND. Connecting the DITH pin directly to GND disables frequency dithering, causing the oscillator to operate at the frequency established by the RT resistor. As shown in 图 7-5, the C_{dither} capacitor is used to generate a triangular wave centered at 1.2 V. This triangular waveform is used to manipulate the oscillator circuit such that the oscillator frequency modulates from –5% to +5% of the nominal operating frequency set by the RT resistor. The C_{dither} capacitor value sets the rate of the low frequency modulation. For example, a lower value C_{dither} capacitor modulates the oscillator frequency from –5% to +5% at a faster rate than a higher value capacitor. For the dither circuit to work effectively, the modulation rate must be much less than the oscillator frequency (f_{SW}), select C_{dither} such that:

$$C_{dither} \geq \frac{100 \times 25\ \mu A}{f_{SW} \times 0.12V} \quad (6)$$

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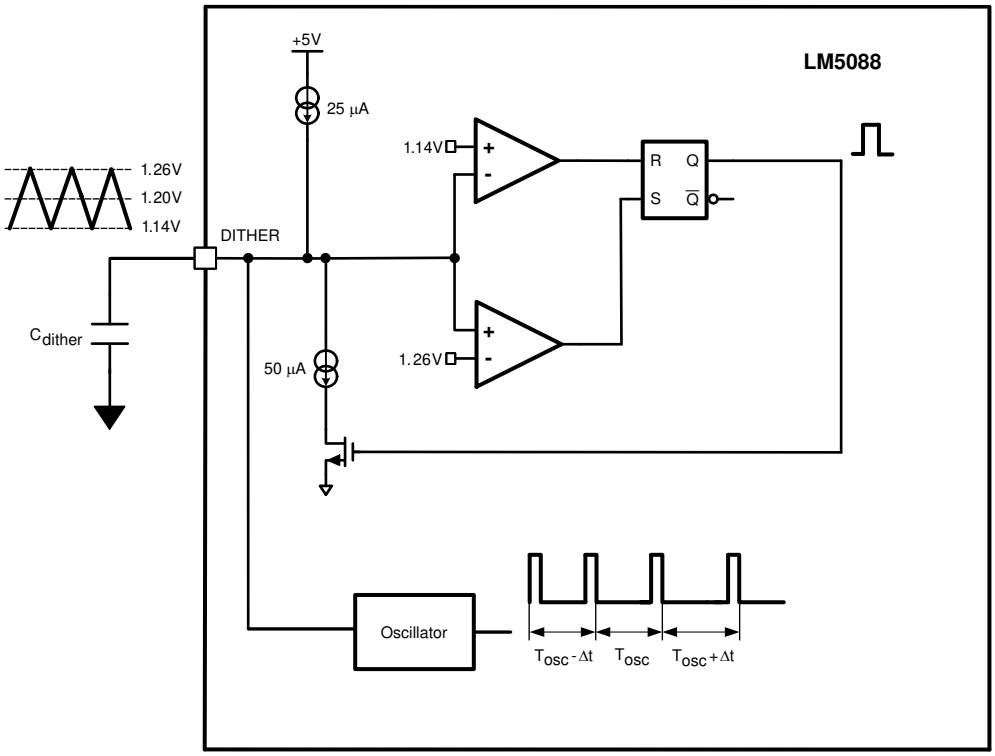


图 7-5. Frequency Dithering Scheme

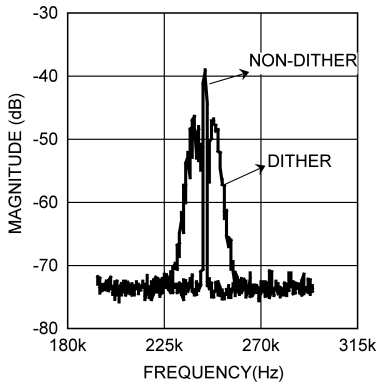


图 7-6. Conducted Emissions Measured at the Input of a LM5088-Based Buck Converter

图 7-6 shows the conducted emissions on the LM5088 evaluation board input power line. It can be seen from the above picture that the peak emissions with non-dithering operation are centered narrowly at the operating frequency of the converter. With dithering operation, the conducted emissions are spread around the operating frequency and the maximum amplitude is reduced by approximately 10 dB. 图 7-6 was captured using a Chroma DC power supply model number 62006P and an Agilent network analyzer model number 4395A.

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7.3.8 Cycle-by-Cycle Current Limit

The LM5088 contains a current limit feature that protects the circuit from extended overcurrent conditions. The emulated current signal is directly proportional to the buck switch current and is applied to the current limit comparator. If the emulated current exceeds 1.2 V, the PWM cycle is terminated. The peak inductor current required to trigger the current limit comparator is given by:

$$I_{PEAK} = \frac{1.2V - 25\ \mu A \times \frac{V_{OUT}}{VIN \times f_{SW} \times C_{RAMP}}}{A \times R_S}$$

$$\text{or} \quad I_{PEAK} \cong \frac{0.12V}{R_S} \tag{7}$$

where

- A is 10 V/V is the current sense amplifier gain.
- C_{RAMP} is the ramp capacitor.
- R_S is the sense resistor.
- $25\ \mu A \times \frac{V_{OUT}}{VIN \times f_{SW} \times C_{RAMP}}$ is the voltage ramp added for slope compensation .
- 1.2 V is the reference of the current limit comparator.

Since the current that charges the RAMP capacitor is proportional to $V_{IN} - V_{OUT}$, if the output is suddenly shorted, the V_{OUT} term is zero and the RAMP charging current increases. The increased RAMP charging current immediately reduces the PWM duty cycle. The LM5088 also includes a buck switch protection scheme. A dedicated comparator monitors the drain-to-source voltage of the buck FET when it is turned on, if the V_{DS} exceeds 1.5 V, the comparator turns off the buck FET immediately. This feature helps protect the buck FET in catastrophic conditions, such as a sudden saturation of the inductor.

7.3.9 Overload Protection Timer (LM5088-2 Only)

To further protect the external circuitry during a prolonged over current condition, the LM5088-2 provides a current limit timer to disable the switching regulator and provide a delay before restarting (hiccup mode). The number of current limit events required to trigger the restart mode is programmed by an external capacitor at the RES pin. During each PWM cycle, as shown in 图 7-8, the LM5088 either sinks current from or sources current into the RES capacitor. If the emulated current ramp exceeds the 1.2-V current limit threshold, the present PWM cycle is terminated and the LM5088 sources 50 µA into the RES pin capacitor during the next PWM clock cycle. If a current limit event is not detected in a given PWM cycle, the LM5088 disables the 50-µA source current and sinks 27 µA from the RES pin capacitor during the next cycle. In an overload condition, the LM5088 protects the converter with cycle-by-cycle current limiting until the voltage at RES pin reaches 1.2 V. When RES reaches 1.2 V, a hiccup mode sequence is initiated as follows:

- The SS capacitor is fully discharged.
- The RES capacitor is discharged with 1.2 µA
- Once the RES capacitor reaches 0.2 V, a normal soft-start sequence begins. This provides a time delay before restart.
- If the overload condition persists after restart, the cycle repeats.
- If the overload condition no longer exists after restart, the RES pin is held at ground by the 27-µA discharge current source and normal operation resumes.

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The overload protection timer is very versatile and can be configured for the following modes of protection:

1. **Cycle-by-Cycle only:** The hiccup mode can be completely disabled by connecting the RES pin to GND. In this configuration, the cycle-by-cycle protection limits the output current indefinitely and no hiccup sequence occurs.
2. **Delayed Hiccup:** Connecting a capacitor to the RES pin provides a programmed number of cycle-by-cycle current limit events before initiating a hiccup mode restart, as previously described. The advantage of this configuration is that a short term overload does not cause a hiccup mode restart but during extended overload conditions, the average dissipation of the power converter is very low.
3. **Externally Controlled Hiccup:** The RES pin can also be used as an input. By externally driving the pin to a level greater than the 1.2-V hiccup threshold, the controller is forced into the delayed restart sequence. For example, the external trigger for a delayed restart sequence could come from an overtemperature protection or an output overvoltage sensor.

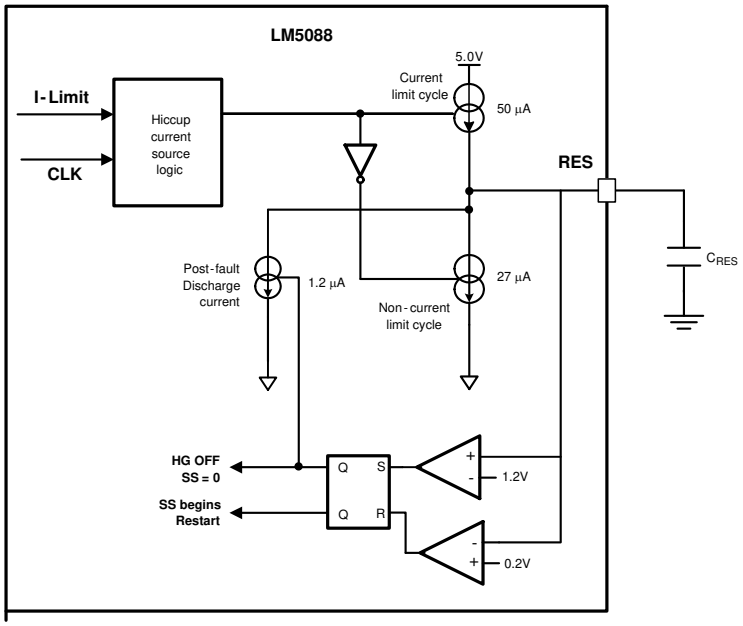


图 7-7. Current Limit Restart Circuit

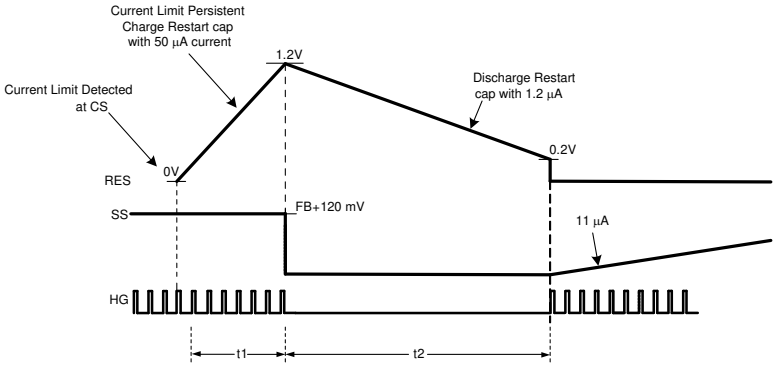


图 7-8. Current Limit Restart Timing Diagram

7.3.10 Soft Start

The soft-start (SS) feature forces the output to rise linearly until it reaches the steady-state operating voltage set by the feedback resistors. The LM5088 regulates the FB pin to the SS pin voltage or the internal 1.205-V reference, whichever is lower. At the beginning of the soft-start sequence, VSS = 0 V and an internal 11-µA current source gradually increases the voltage of the external soft-start capacitor (C_{SS}). An internal amplifier

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clamps the SS pin voltage at 120 mV above the FB voltage. This feature provides soft start-controlled recovery with reduced output overshoot in the event that the output voltage momentarily dips out of regulation.

7.3.11 HG Output

The LM5088 provides a high current, high-side driver and associated level shift circuit to drive an external N-channel MOSFET. The gate driver works in conjunction with an internal diode and external bootstrap capacitor. A ceramic bootstrap capacitor is recommended, and must be connected directly between the BOOT and SW pins. During the off time of the buck switch, the bootstrap capacitor charges from VCC through an internal diode. When operating with a high PWM duty cycle, the HG output is forced-off each cycle for 365 ns (maximum) to make sure that BOOT capacitor is recharged. A *pre-charge* circuit, comprised of a MOSFET between SW and GND, is turned ON during the forced off time to help replenish the BOOT capacitor. The pre-charge circuit provides charge to the BOOT capacitor under light load or pre-biased load conditions when the SW voltage does not remain low during the entire off time.

7.3.12 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum operating temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the output driver and the bias supply of the controller. The feature prevents catastrophic failures from accidental device over-heating.

7.4 Device Functional Modes

7.4.1 EN Pin Modes

If the EN pin voltage is below 0.4 V, the regulator is in a low power state. If the EN pin voltage is between 0.4 V and 1.2 V, the controller is in standby mode. If the EN pin voltage is above 1.2 V, the controller is operational. An external voltage divider can be used to set a line undervoltage shutdown threshold. If the EN pin is left open, a 5-μA pullup current forces the pin to the high state and enables the controller.

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8 Application and Implementation

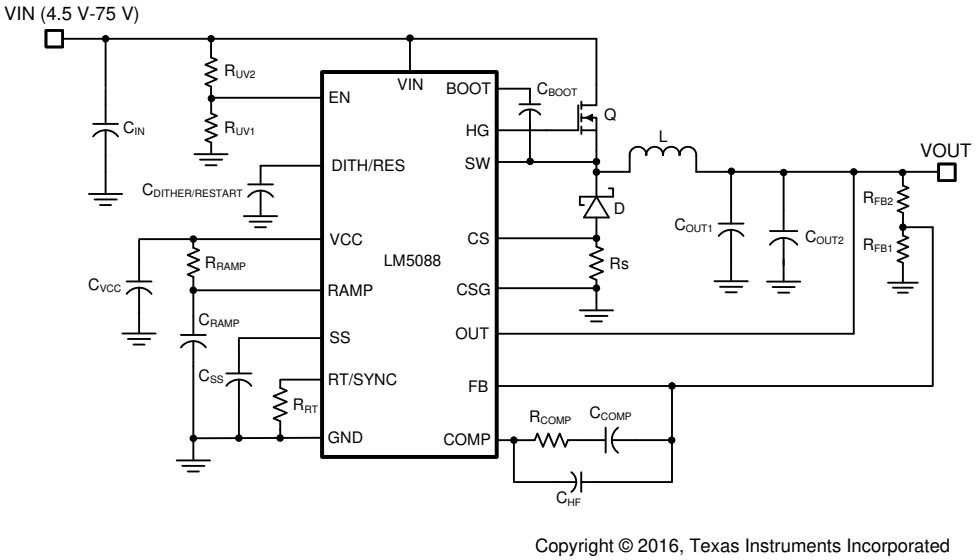
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8.1 Application Information

The LM5088 wide input range buck controller features all the functions necessary to implement an efficient high-voltage step-down converter using a minimum number of external components. The LM5088 is well-suited for a wide range of applications where efficient step-down of high, unregulated input voltage is required.

8.2 Typical Application



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图 8-1. LM5088 Typical Application Schematic

8.2.1 Design Requirements

The procedure for calculating the external components is illustrated with the following design example. The circuit shown in 图 9-1 and 图 9-2 is configured for the following specifications:

- Output voltage = 5 V
- Input voltage = 5.5 V to 36 V
- Maximum load current = 7 A
- Switching frequency = 250 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Timing Resistor

The RT resistor sets the oscillator switching frequency. Higher frequencies result in smaller size components such as the inductor and filter capacitors. However, operating at higher frequencies also results in higher MOSFET and diode switching losses. Operation at 250 kHz was selected for this example as a reasonable compromise between size and efficiency.

The value of RT resistor can be calculated as follows:

$$R_{RT} = \frac{\frac{1}{250\ kHz} - 280\ ns}{152\ pF} = 24.5\ k\Omega \tag{8}$$

The nearest standard value of 24.9 kΩ was chosen for RT.

8.2.2.2 Output Inductor

The inductor value is determined based on the operating frequency, load current, ripple current, and the input and output voltages.

Knowing the switching frequency (f_{SW}), maximum ripple current (I_{PP}), maximum input voltage ($V_{IN(max)}$), and the nominal output voltage (V_{OUT}), the inductor value can be calculated as follows:

$$L = \frac{V_{OUT}}{I_{PP} \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) \tag{9}$$

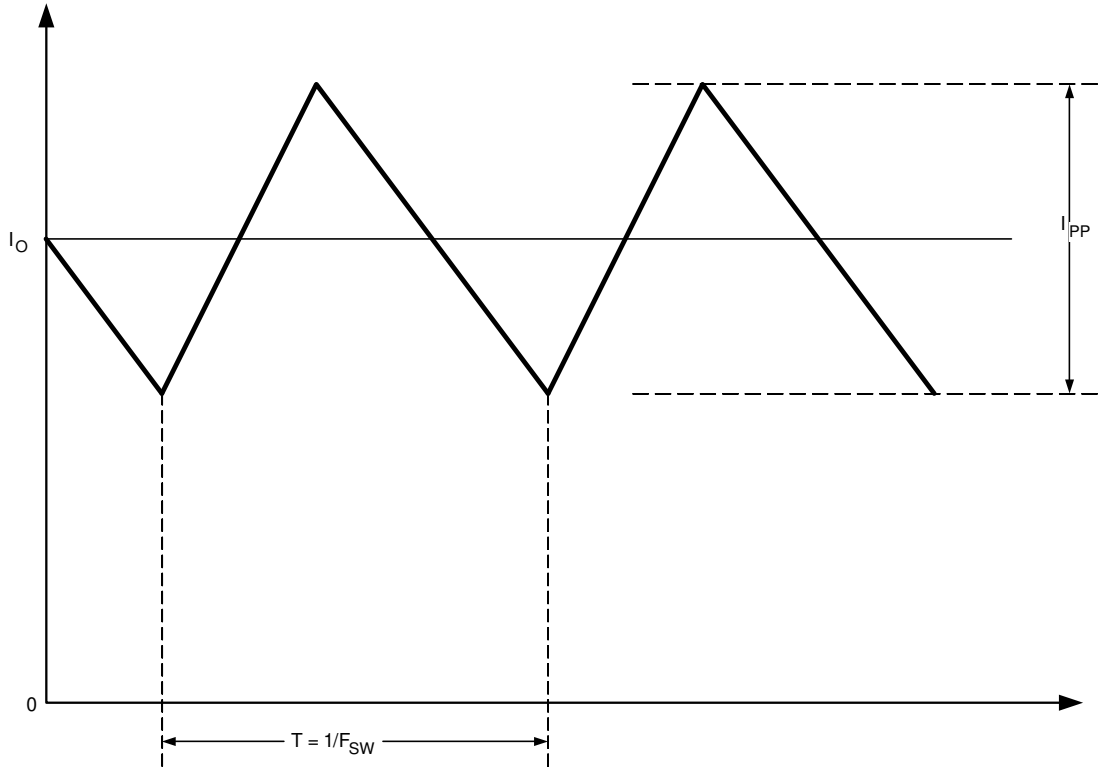


图 8-2. Inductor Current

The maximum ripple current occurs at the maximum input voltage. Typically, I_{PP} is selected between 20% and 40% of the full load current. Higher ripple current results in a smaller inductor. However, it places more burden on the output capacitor to smooth out the ripple current to achieve low output ripple voltage. For this example, 40% ripple was chosen for a smaller sized inductor.

$$L = \frac{5V}{0.4 \times 7A \times 250\ kHz} \times \left(1 - \frac{5V}{55V}\right) = 6.2\ \mu H \tag{10}$$

The nearest standard value of 6.8 µH is used. To prevent saturation, the inductor must be rated for the peak current. During normal operation, the peak current occurs at maximum load current (plus maximum ripple). With

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properly scaled component values, the peak current is limited to $V_{CS(TH)}/R_S$during overload conditions. At the maximum input voltage with a shorted output, the chosen inductor must be evaluated at elevated temperature. Note that the saturation current rating of inductors drops significantly at elevated temperatures.

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8.2.2.3 Current Sense Resistor

The current limit value (I_{LIM}) is set by the current sense resistor (R_S).

R_S can be calculated by

$$R_S = \frac{V_{CS}}{(1 + \text{margin}) \times \left(I_{OUT} + 0.5 \times I_{PP}\right) + \frac{V_{OUT}}{L \times f_{sw}}} = \frac{0.12}{(1 + 0.1) \times \left(7\,A + 0.5 \times 2.8\right) + \frac{5\,V}{6.8\,\mu H \times 250\,kHz}} \cong 10\,m\Omega \quad (11)$$

Some *margin* beyond the maximum load current is recommended for the current limit threshold. In this design example, the current limit is set at 10% above the maximum load current, resulting in a R_S value of 10 mΩ. The CS and CSG pins must be Kelvin connected to the current sense resistor.

8.2.2.4 Ramp Capacitor

With the inductor and sense resistor value selected, the value of the ramp capacitor (C_{RAMP}) necessary for the emulation ramp circuit is given by:

$$C_{RAMP} = \frac{g_m \text{ x } L}{A \text{ x } R_S} \quad (12)$$

where

- L is the value of the output inductor.
- g_m is the ramp generator transconductance (5 µA/V).
- A is the current sense amplifier gain (10 V/V).

For the current design example, the ramp capacitor is calculated as:

$$C_{RAMP} = \frac{5\ \mu A/V \text{ x } 6.8\ \mu H}{10 V/V \text{ x } 10\ m\Omega} = 340\ pF \quad (13)$$

The next lowest standard value, 270 pF, was selected for C_{RAMP}. An NPO capacitor with 5% or better tolerance is recommended. Note that selecting a capacitor value lower than the calculated value increases the slope compensation. Furthermore, selecting a ramp capacitor substantially lower or higher than the calculated value also results in incorrect PWM operation.

For V_{OUT} > 5 V, internal slope compensation provided by the LM5088 may not be adequate for certain operating conditions especially at low input voltages. A pullup resistor may be added from the VCC to RAMP pin to increase the slope compensation. Optimal slope compensation current can be calculated from 方程式 14.

$$I_{OS} = V_{OUT} \times 5\ \mu A/V \quad (14)$$

and R_{RAMP} is given by 方程式 15.

$$R_{RAMP} = \frac{V_{VCC} - V_{RAMP}}{I_{OS} - 25\ \mu A} \quad (15)$$

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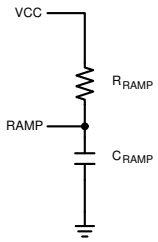


图 8-3. Additional Slope Compensation for V_{OUT} > 5 V

8.2.2.5 Output Capacitors

The output capacitors smooth the inductor current ripple and provide a source of charge for load transient conditions. The output capacitor selection is primarily dictated by the following specifications:

- Steady-state output peak-peak ripple (ΔV_{PK-PK})
- Output voltage deviation during transient condition ($\Delta V_{Transient}$)

For the 5-V output design example, ΔV_{PK-PK} = 50 mV (1% of V_{OUT}) and $\Delta T_{Transient}$ = 100 mV (2% of V_{OUT}) were chosen. The magnitude of output ripple primarily depends on ESR of the capacitors while load transient voltage deviation depends both on the output capacitance and ESR.

When a full load is suddenly removed from the output, the output capacitor must be large enough to prevent the inductor energy to raise the output voltage above the specified maximum voltage. In other words, the output capacitor must be large enough to absorb the maximum stored energy of the inductor. The stored energy equations of both the inductor and the output capacitor can be calculated with:

$$C_O = \frac{L \times \left(I_O + \frac{\Delta I_{PP}}{2}\right)^2}{(\Delta V + V_{OUT})^2 - V_{OUT}^2} \tag{16}$$

Evaluating, the above equation with a ΔV_{OUT} of 100 mV results in an output capacitance of 475 µF. As stated earlier, the maximum peak-to-peak ripple primarily depends on the ESR of the output capacitor and the inductor ripple current. To satisfy the ΔV_{PK-PK} of 50 mV with 40% inductor current ripple, the ESR must be less than 15 mΩ. In this design example, a 470-µF aluminum capacitor with an ESR of 10 mΩ is paralleled with two 47-µF ceramic capacitors to further reduce the ESR.

8.2.2.6 Input Capacitors

The input power supply typically has large source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on time. When the buck switch turns ON, the current into the external FET steps to the valley of the inductor current waveform at turn-on, ramps up to the peak value, and then drops to zero at turn-off. The input capacitors must be selected for RMS current rating and minimum ripple voltage. A good approximation for the ripple current is $I_{RMS} > I_{OUT} / 2$.

Select quality ceramic capacitors with a low ESR for the input filter. To allow for capacitor tolerances and voltage rating, five 2.2-µF, 100-V ceramic capacitors were selected. With ceramic capacitors, the input ripple voltage is triangular and peaks at 50% duty cycle. Taking into account the capacitance change with DC bias, a worst case input peak-to-peak ripple voltage can be approximated with 方程式 17.

$$\Delta V_{IN} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}} = \frac{7A}{4 \times 250\ kHz \times 11\ \mu F} = 636\ mV \tag{17}$$

When the converter is connected to an input power source, a resonant circuit is formed by the line impedance and the input capacitors. This can result in an overshoot at the VIN pin and can result in VIN exceeding its

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absolute maximum rating. Because of those conditions, it is recommended that either an aluminum type capacitor with an ESR or increasing C_{IN} > 10 × L_{IN}. While using aluminum type capacitor, take care to not exceed its maximum ripple current rating. Tantalum capacitors must be avoided at the input as they are prone to shorting.

8.2.2.7 VCC Capacitor

The capacitor at the VCC pin provides noise filtering and stability for the VCC regulator. The recommended value must be no smaller than 0.1 µF, and must be a good-quality, low-ESR, ceramic capacitor. A value of 1 µF was selected for this design.

8.2.2.8 Bootstrap Capacitor

The bootstrap capacitor between HB and SW pins supplies the gate current to charge the high-side MOSFET gate at the turn-on of each cycle as well as supplying the recovery charge for the bootstrap diode (D1).The peak current can be several amperes. The recommended value of the bootstrap capacitor is at least 0.022 µF and must be a good-quality, low-ESR, ceramic capacitor located close to the pins of the IC. The absolute minimum value for the bootstrap capacitor is calculated as:

$$C_{HB} \geq \frac{Q_g}{\Delta V_{HB}} \tag{18}$$

where

- Q_g is the high-side MOSFET gate charge.
- ΔV_{HB} is the tolerable voltage droop on C_{HB}, which is typically less than 5% of the VCC.

.A value of 0.1 µF was selected for this design.

8.2.2.9 Soft-Start Capacitor

The capacitor at the SS capacitor determines the soft-start time, the output voltage to reach the final regulated value. The value of C_{SS} for a given time is determined from:

$$C_{SS} = \frac{t_{SS} \text{ x } 11\ \mu A}{1.205V} \tag{19}$$

For this design example, a value of 0.022 µF was chosen for a soft-start time of approximately 2 ms.

8.2.2.10 Output Voltage Divider

R_{FB1} and R_{FB2} set the output voltage level. The ratio of these resistors can be calculated from:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{VOUT}{1.205V} - 1 \tag{20}$$

1.62 kΩ was chosen for R_{FB1} in this design, which results in a R_{FB2} value of 5.11 kΩ. A reasonable guide is to select the value of R_{FB1} value such that the current through the resistor (1.2 V/ R_{FB1}) is in between 1 mA and 100 µA.

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8.2.2.11 UVLO Divider

A voltage divider can be connected to the EN pin to the set the minimum start-up voltage ($VIN_{(min)}$) of the regulator. If this feature is required, set the value of R_{UV2} between 10 kΩ and 100 kΩ and then calculate R_{UV1} from:

$$R_{UV1} = 1.2V \times \frac{R_{UV2}}{(V_{IN(min)} + (5\ \mu A \times R_{UV2}) - 1.2V)} \quad (21)$$

In this design, for a $V_{IN(min)}$ of 5 V, R_{UV2} was selected to be 54.9 kΩ, resulting in a R_{UV1} value of 16.2 kΩ. Install a capacitor parallel to R_{UV1} for filtering. If the EN pin is left open, the LM5088 begins operation once the upper VCC UV threshold of 4.0 V (typical) is reached.

8.2.2.12 Restart Capacitor (LM5008-2 Only)

The basic operation of hiccup mode current limit is described in 节 7.3.9. In the LM5088-2 application example, the RES pin is configured for delayed hiccup mode. Please refer to 节 7.3.9 to configure this pin in alternate configurations and also refer to 图 7-8. The delay time to initiate a hiccup cycle (t1) is programmed by the selection of RES pin capacitor. In the case of continuous cycle-by-cycle current limit detection at the CS pin, the time required for C_{RES} to reach the 1.2 V is given by:

$$T_{restart_delay} = \frac{C_{RES} \times 1.2V}{50\ \mu A} = C_{RES} \times 24k \quad (22)$$

The cool down time (t2) is set by the time taken to discharge the RES cap with 1.2-µA current source. This feature reduces the input power drawn by the converter during a prolonged overcurrent condition. In this application, a 500-µs delay time was selected. The minimum value of C_{RES} capacitor must be no less than 0.022 µF.

8.2.2.13 MOSFET Selection

Selection of the buck MOSFET is governed by the same trade-offs as the switching frequency. Losses in power MOSFETs can be broken down into conduction losses and switching losses. The conduction loss is given by 方程式 23.

$$P_{DC} = D \times (I_O{}^2 \times R_{DS(ON)} \times 1.3) \quad (23)$$

where

- D is the duty cycle.
- I_O is the maximum load current.

The factor 1.3 accounts for the increase in MOSFET on-resistance due to heating. Alternatively, for a more precise calculation, the factor of 1.3 can be ignored and the on-resistance of the MOSFET can be estimated using the *$R_{DS(ON)}$ vs Temperature* curves in the MOSFET data sheet.

The switching loss occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the MOSFET. The switching loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_O \times (t_R + t_F) \times f_{SW} \quad (24)$$

where

- $t_R$is the rise time of the MOSFET.
- t_F is the fall time of the MOSFET.

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The rise and fall times are usually mentioned in the MOSFET data sheet or can be empirically observed on the scope. There is another loss, which is associated with the buck MOSFET is the *gate-charging loss*. This loss differs from the above two losses in the sense that it is dissipated in the LM5088 and not in the MOSFET itself. Gate charging loss, P_{GC}, results from the drive current charging the gate capacitance of the power MOSFET and is approximated as:

$$P_{GC} = VCC \times Q_g \times f_{SW} \quad (25)$$

For this example with the maximum input voltage of 55 V, the V_{DS} breakdown rating of the selected MOSFET must be greater than 55 V, plus any ringing across drain to source due to parasitics. In order to minimize switching time and gate drive losses, the selected MOSFET must also have low gate charge (Q_g). A good choice of MOSFET for this design example is the SI7148DP which has a total gate charge of 30 nC and rise and fall times of 10 ns and 12 ns, respectively.

8.2.2.14 Diode Selection

A Schottky type re-circulating diode is required for all LM5088 applications. The near ideal reverse recovery current transients and low forward voltage drop are particularly important diode characteristics for high input voltage and low output voltage applications common to LM5088. The diode switching loss is minimized in a Schottky diode because of near ideal reverse recovery. The conduction loss can be approximated by:

$$P_{dc_diode} = (1 - D) \times I_O \times V_F \quad (26)$$

where

- V_F is the forward drop of the diode.

The worst case is to assume a short circuit load condition. In this case, the diode carries the output current almost continuously. The reverse breakdown rating must be selected for the maximum input voltage level, plus some additional safety margin to withstand ringing at the SW node. For this application, a 60-V On Semiconductor Schottky diode (MBRB2060) with a specified forward drop of 0.6 V at 7 A at a junction temperature of 50°C was selected. For output loads of 5 A and greater and high input voltage applications, a diode in a D^2PAK package is recommended to support the worst case power dissipation.

8.2.2.15 Snubber Components Selection

Excessive ringing and spikes can cause erratic operation and couple spikes and noise to the output. Voltage spikes beyond the rating of the LM5088 or the re-circulating diode can damage these devices. A snubber network across the power diode reduces ringing and spikes at the switching node. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure that the lead lengths for the snubber connections are very short. For the current levels typical for the LM5088, a resistor value between 3 Ω and 10 Ω must be adequate. As a rule of thumb, a snubber capacitor, which is four to five times the junction temperature of the Schottky diode reduce spikes adequately. Increasing the value of the snubber capacitor results in more damping but also results in higher losses. The power dissipation of the resistor is independent of the resistance value as the resistor dissipates the energy stored by the snubber capacitor. The power dissipation of the resistor can be approximated as:

$$P_{R_SNUB} = C_{SNUB} \times V_{IN(max)}{}^2 \times f_{SW} \quad (27)$$

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8.2.2.16 Error Amplifier Compensation

R_{COMP}, C_{COMP}, and C_{HF} configure the error amplifier gain characteristics to accomplish a stable voltage loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components, R_{COMP} and C_{COMP}. The voltage loop gain is the product of the modulator gain and the error amplifier gain. For this example, the modulator can be treated as an ideal voltage-to-current (transconductance) converter. The DC modulator gain of the LM5088 can be modeled as:

$$\text{DC Gain}_{(MOD)} = R_{LOAD} / (A \times R_S)$$

The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD}) and the output capacitance (C_{OUT}). The corner frequency of this pole is:

If R_{LOAD} = 5 V/7 A = 0.714 Ω and C_{OUT} = 500 µF (effective), then $FP_{(MOD)}$ = 550 Hz. (28)

$$\text{DC Gain}_{(MOD)} = 0.714 / (10 \times 10\ m\Omega) = 7.14 = 17\ dB \quad (29)$$

For the 5-V design example, the modulator gain versus frequency characteristic was measured as shown in 图 8-4.

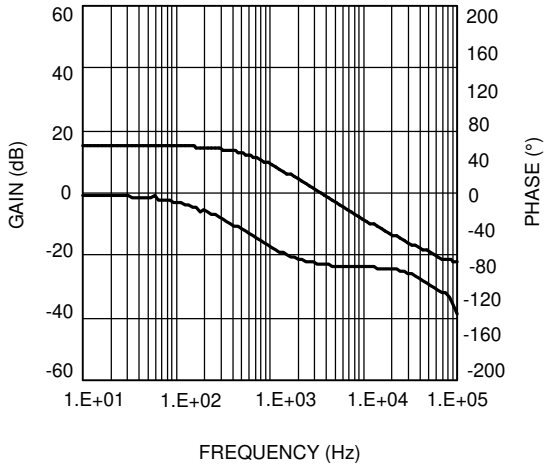


图 8-4. Modular Gain Phase

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Components R_{COMP} and C_{COMP} configure the error amplifier as a type II compensation configuration. The DC gain of the amplifier is 80 dB, which has a pole at low frequency and a zero at $f_{Zero} = 1 / (2 \pi \times R_{COMP} \times C_{COMP})$. The error amplifier zero is set such that it cancels the modulator pole leaving a single pole response at the crossover frequency of the voltage loop. A single pole response at the crossover frequency yields a very stable loop with 90° of phase margin. For the design example, a target loop bandwidth (crossover frequency) of 15 kHz was selected. The compensation network zero (f_{Zero}) must be at least an order of magnitude lower than the target crossover frequency. This constrains the product of R_{COMP} and C_{COMP} for a desired compensation network zero $1/ (2 \pi \times R_{COMP} \times C_{COMP})$ to be less than 1.5 kHz. Increasing R_{COMP}, while proportionally decreasing C_{COMP}, decreases the error amp gain. For the design example, C_{COMP} was selected to be 0.015 µF and R_{COMP} was selected to be 18 kΩ. These values configure the compensation network zero at 0.6 kHz. The error amp gain at frequencies greater than f_{Zero} is R_{COMP} / R_{FB2}, which is approximately 3.56 (11dB).

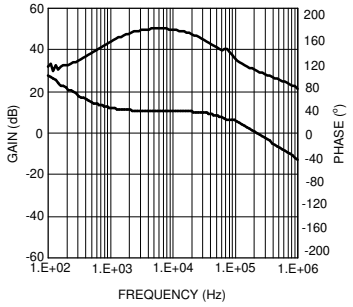


图 8-5. Error Amplifier Gain and Phase

The overall voltage loop gain can be predicted as the sum (in dB) of the modulator gain and the error amp gain. If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If a network analyzer is not available, the error amplifier compensation components can be designed with the suggested guidelines. Step load transient tests can be performed to verify performance. The step load goal is minimum overshoot with a damped response. C_{HF} can be added to the compensation network to decrease noise susceptibility of the error amplifier. The value of C_{HF} must be sufficiently small since the addition of this capacitor adds a pole in the error amplifier transfer function. A good approximation of the location of the pole added by C_{HF} is $f_{P2} = f_{Zero} \times C_{COMP} / C_{HF}$.Using C_{HF} is recommended to minimize coupling of any switching noise into the modulator. The value of C_{HF} was selected as 100 pF for this design example.

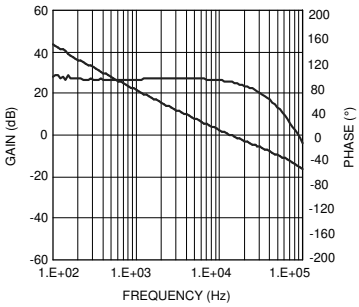


图 8-6. Overall Loop Gain and Phase

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8.2.3 Application Curves

See 图 8-4 through 图 8-6 for Typical Application Curves.

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9 Power Supply Recommendations

9.1 Thermal Considerations

In a buck converter, most of the losses can be attributed to MOSFET conduction and switching loss, re-circulating diode conduction loss, inductor DCR loss, and LM5088 V_{IN} and V_{CC} loss. The other dissipative components in a buck converter produce losses, but these other losses collectively account for about 2% of the total loss. Formulas to calculate all the major losses are described in their respective sections of this data sheet. The easiest method to determine the power dissipated within the LM5088 is to measure the total conversion losses (P_{IN} – P_{OUT}), then subtract the power losses in the Schottky diode, MOSFET, output inductor, and snubber resistor. When operating at 7 A of output current and at 55 V, the power dissipation of the LM5088 is approximately 850 mW. The junction-to-ambient thermal resistance of the LM5088 mounted in the evaluation board is approximately 40°C with no airflow. At 25°C ambient temperature and no airflow, the predicted junction temperature is 25 + 40 × 0.9 = 61°C. The LM5088 has an exposed thermal pad to aid in power dissipation. Adding several vias under the device greatly reduces the controller junction temperature. The junction to ambient thermal resistance varies with application. The most significant variables are the area of copper in the PC board: the number of vias under the IC exposed pad and the amount of forced air cooling. The integrity of solder connection from the IC exposed pad to the PC board is critical. Excessive voids greatly diminish the thermal dissipation capacity.

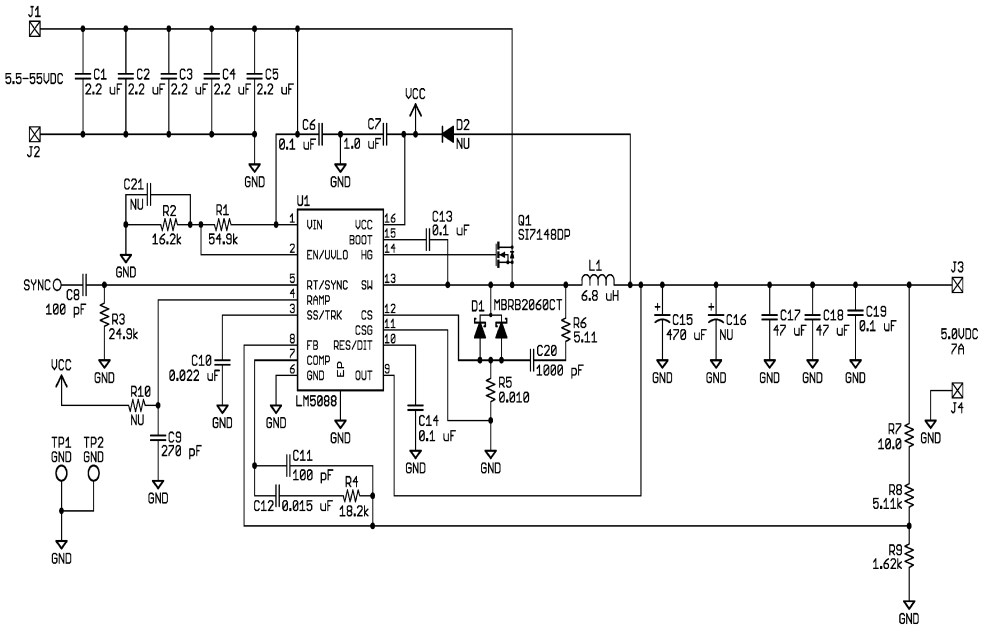


图 9-1. LM5088-1 Application Schematic

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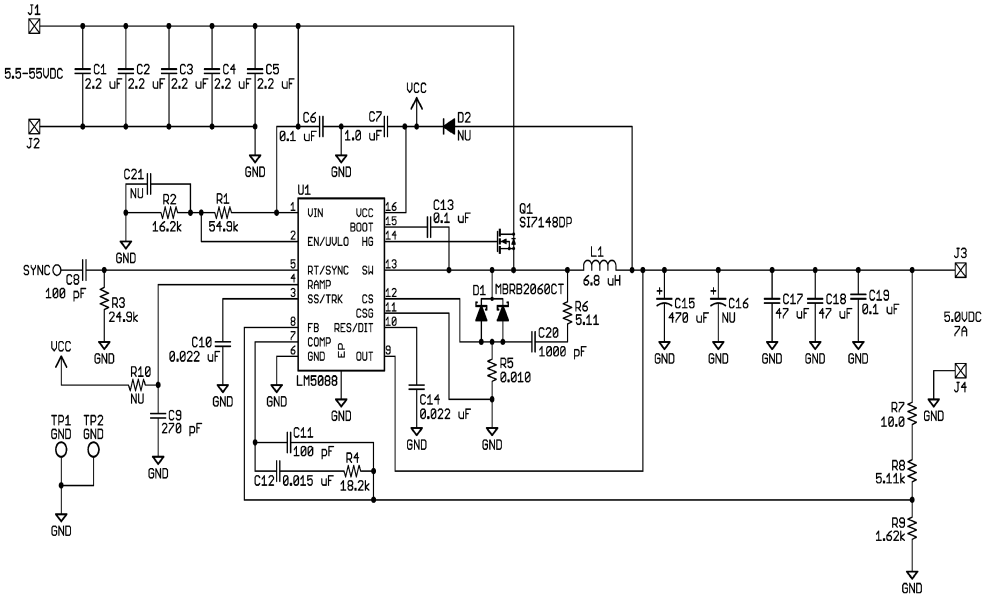


图 9-2. LM5088-2 Application Schematic

10 Layout

10.1 Layout Guidelines

In a buck regulator, there are two loops where currents are switched very fast. The first loop starts from the input capacitors, through the buck MOSFET, to the inductor then out to the load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the current sense resistor, through the Schottky diode, to the inductor and then out to the load. Minimizing the area of these two loops reduces the stray inductance and minimizes noise, which can cause erratic operation. A ground plane is recommended as a means to connect the input filter capacitors of the output filter capacitors and the PGND pin of the regulator. Connect all of the low power ground connections (C_{SS}, R_T, and C_{RAMP}) directly to the regulator GND pin. Connect the GND pin and PGND pins together through to top-side copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane. The input capacitor ground connection must be as close as possible to the current sense ground connection.

10.2 Layout Example

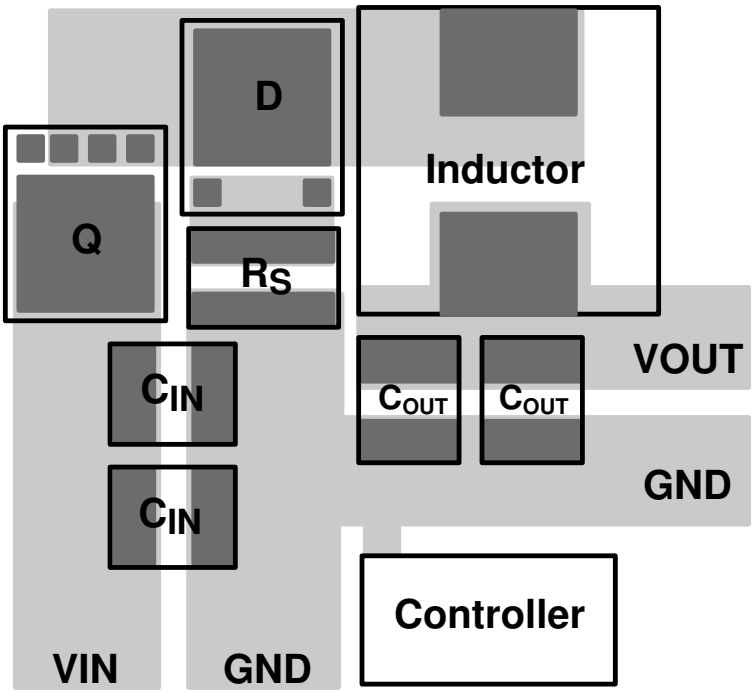


图 10-1. LM5088 Layout Example

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11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5088MH-1/NOPB	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-1
LM5088MH-1/NOPB.A	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-1
LM5088MH-1/NOPB.B	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-1
LM5088MH-2/NOPB	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-2
LM5088MH-2/NOPB.A	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-2
LM5088MH-2/NOPB.B	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-2
LM5088MHX-1/NOPB	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-1
LM5088MHX-1/NOPB.A	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-1
LM5088MHX-1/NOPB.B	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-1
LM5088MHX-2/NOPB	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-2
LM5088MHX-2/NOPB.A	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-2
LM5088MHX-2/NOPB.B	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-2
LM5088QMH-1/NOPB	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-1
LM5088QMH-1/NOPB.A	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-1
LM5088QMH-1/NOPB.B	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-1
LM5088QMH-2/NOPB	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-2

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5088QMH-2/NOPB.A	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-2
LM5088QMH-2/NOPB.B	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-2
LM5088QMHX-1/NOPB	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-1
LM5088QMHX-1/NOPB.A	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-1
LM5088QMHX-1/NOPB.B	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-1
LM5088QMHX-2/NOPB	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-2
LM5088QMHX-2/NOPB.A	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-2
LM5088QMHX-2/NOPB.B	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM5088, LM5088-Q1 :

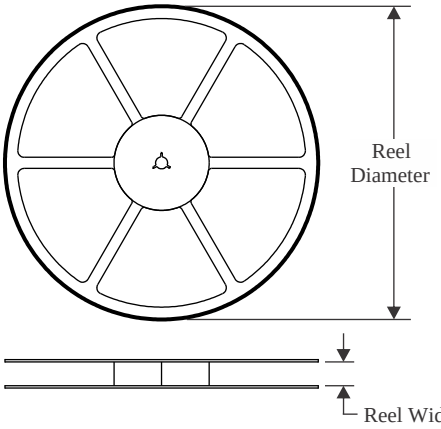
- Catalog : LM5088
- Automotive : LM5088-Q1

NOTE: Qualified Version Definitions:

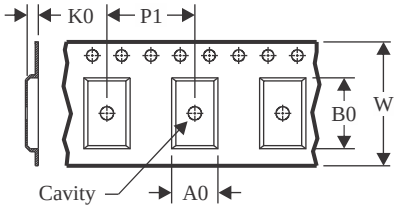
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

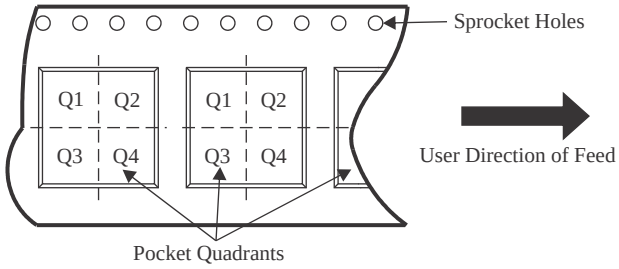


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

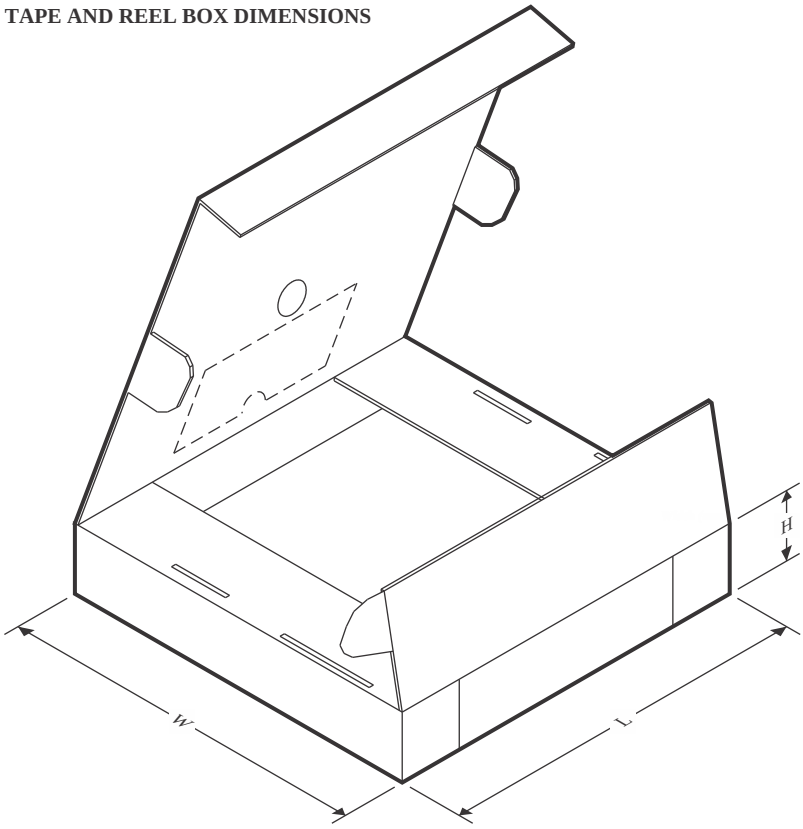
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5088MHX-1/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5088MHX-2/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5088MHX-2/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5088QMHX-1/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5088QMHX-2/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

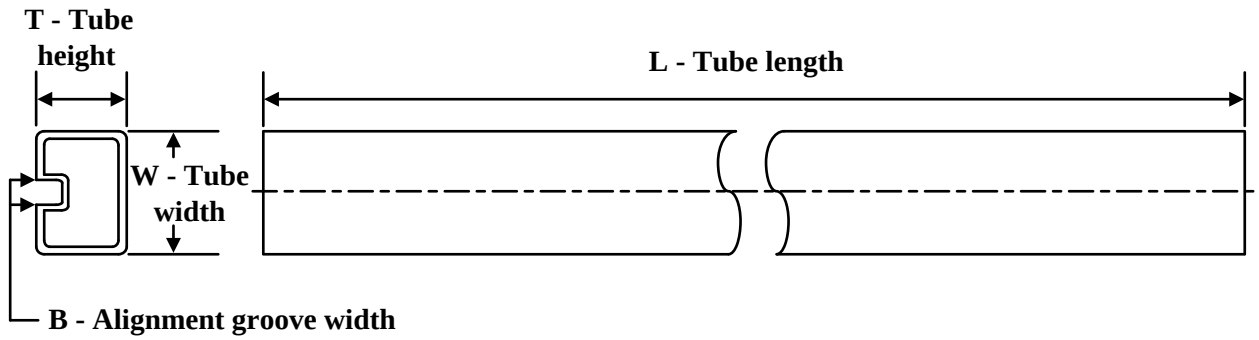
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

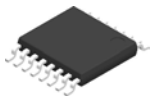
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5088MHX-1/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM5088MHX-2/NOPB	HTSSOP	PWP	16	2500	353.0	353.0	32.0
LM5088MHX-2/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM5088QMHX-1/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM5088QMHX-2/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5088MH-1/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088MH-1/NOPB.A	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088MH-1/NOPB.B	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088MH-2/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088MH-2/NOPB.A	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088MH-2/NOPB.B	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088QMH-1/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088QMH-1/NOPB.A	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088QMH-1/NOPB.B	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088QMH-2/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088QMH-2/NOPB.A	PWP	HTSSOP	16	92	495	8	2514.6	4.06
LM5088QMH-2/NOPB.B	PWP	HTSSOP	16	92	495	8	2514.6	4.06

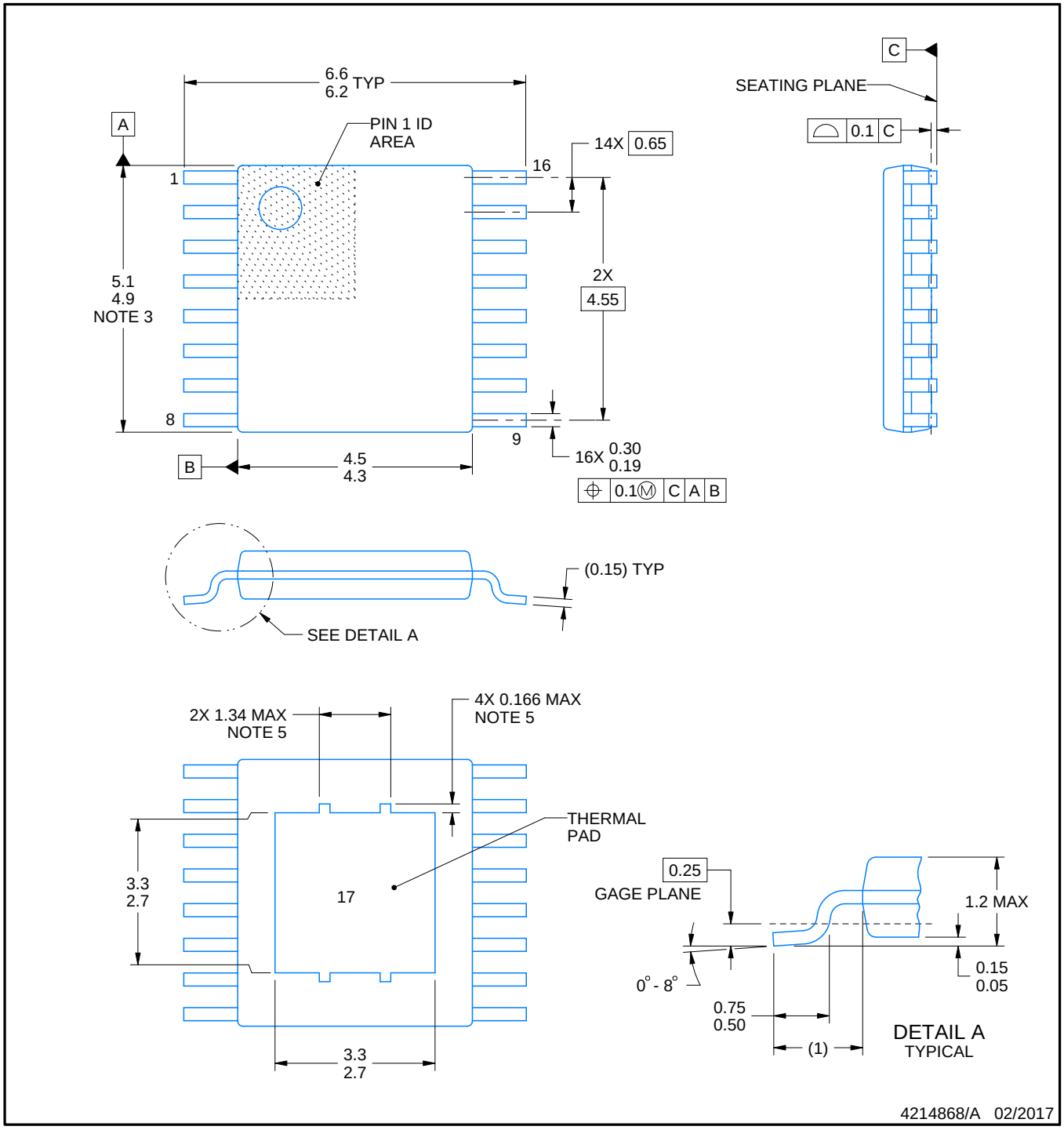


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

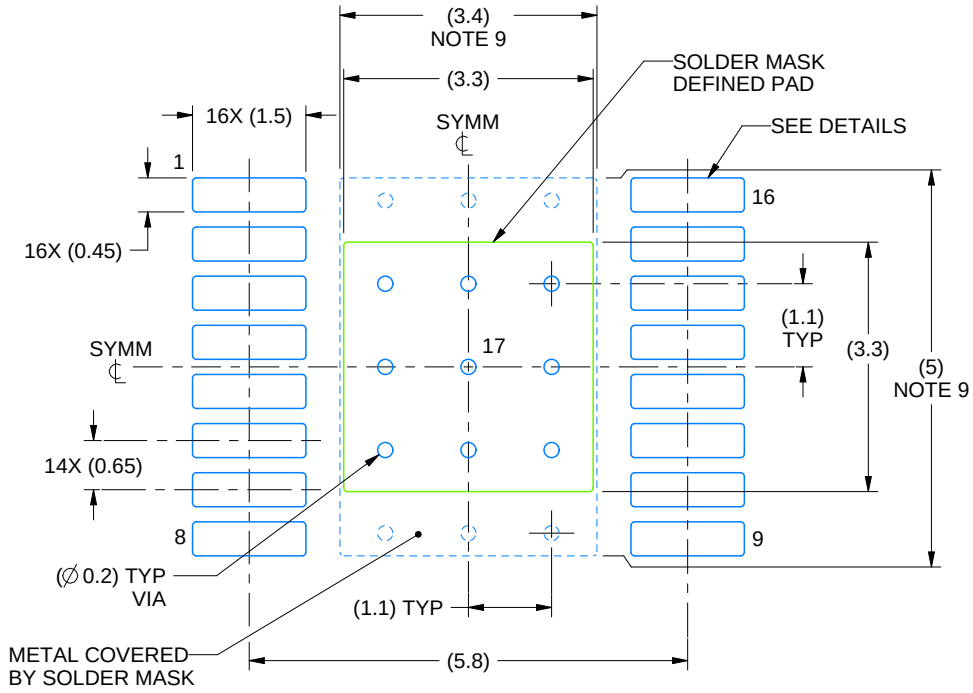
PLASTIC SMALL OUTLINE



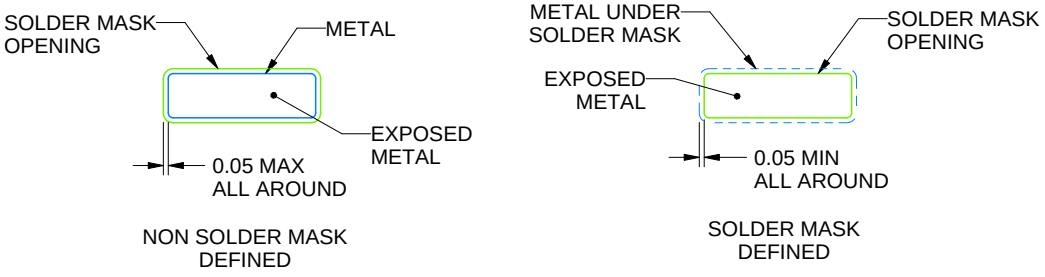
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

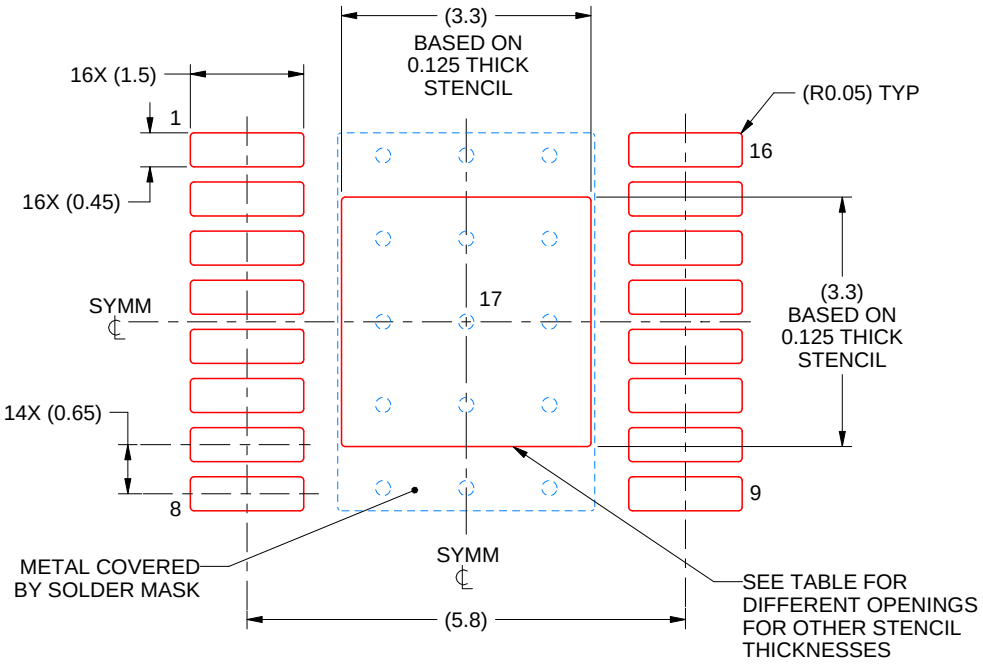


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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