交流-直流准谐振电流模式脉宽调制 (PWM) 控制器

特性

- 临界传导模式
- 峰值电流模式控制模式
- 针对低待机功耗的跳周模式
- 针对持续过载保护的断续模式
- 逐周期过流保护可保持通用交流线路上的准确度
- 线路电流前馈
- 通过感测辅助绕组的 **OVP** 保护
- 集成 **0.7A** 峰值栅极驱动器
- 直接光耦合器件接口
- 电流感测信号的前缘消隐
- 最高频率钳位 **130kHz**
- 可编程软启动
- 热关断
- **8** 引脚表面贴装小外形尺寸 **(MSOP)** 封装

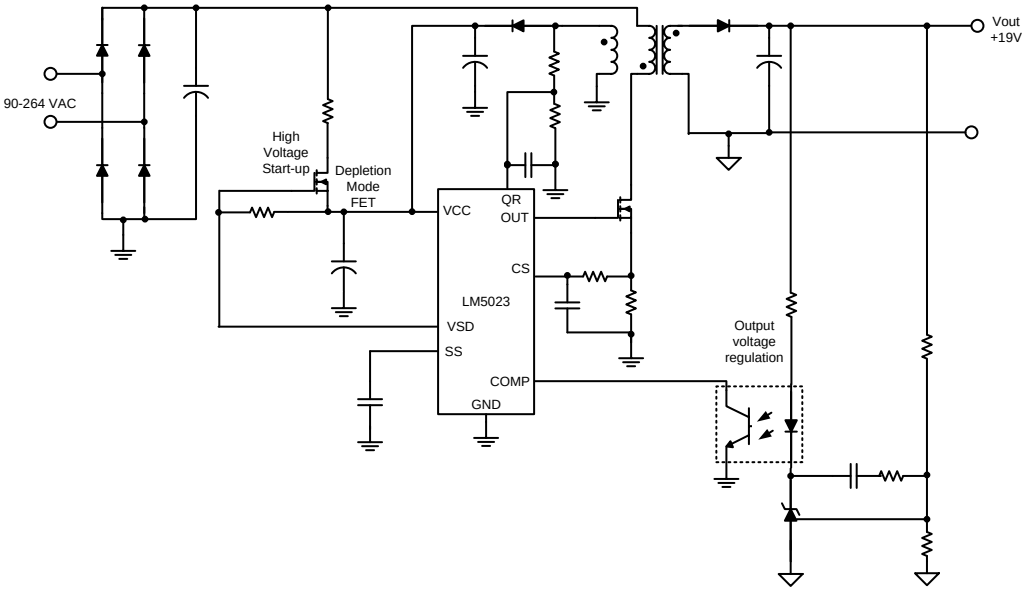
应用范围

- 通用输入交流-直流笔记本电脑适配器 **10W** 至 **65W**
- 高效辅助电路和辅助电源
- 电池充电器
- 消费类电子产品（**DVD** 播放器、机顶盒、数字电视、游戏机、打印机等）

说明

LM5023 是一款准谐振脉宽调制 (PWM) 控制器，此控制器包含有实现一个高效离线电源所需的全部功能。LM5023 使用变压器辅助绕组来实现消磁检测，从而确保了临界传导模式 (CCM) 运行。 LM5023 特有一个用于过流保护的断续模式，它具有的自动重启功能可减少过载期间功率元件上的应力。 针对节能应用（ENERGY STAR®，CEPCP 等）的跳周模式可在轻负载时减少功耗。 LM5023 还使用变压器辅助绕组来实现输出过压 (OVP) 保护，如果检测到 OVP 故障，LM5023 就锁存控制器。

经简化电路原理图



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ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
I_{QR}	Negative Injection Current When the QR Pin is Being Driven Below Ground	–	4	mA
VSD	Maximum Voltage	–0.3	45	V
I_{VSD}	VSD Clamp Continuous Current	–	500	µA
Voltage Range	SS, COMP, QR	–0.3	7	V
Voltage Range	CS	–0.3	1.25	V
OUT	Gate-Drive Voltage at DRV	–0.3	Self-limiting	V
I_{OUT}	Peak OUT Current, Source	–	0.3	A
IOUT	Peak OUT Current Sink	–	0.7	A
VCC	Bias Supply Voltage	–0.3	16	V
T_J	Operating Junction Temperature Range	–40	+125	ºC
T_{STG}	Storage Temperature	–55	+150	ºC
ESD	Human Body Model (HBM) JESD22-A114		2	kV
	Charged-Device Model (CDM) JESD22-C101		1	kV

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL CHARACTERISTICS

			UNIT
θ_{JA}	MSOP-8 Junction to Ambient	107	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
VCC	Bias Supply Voltage	8	14	V
I_{VSD}	Current Sense	2	10	µA
I_{QR}	QR Pin Current	1	4	mA
T_J	Junction Temperature	–40	125	ºC

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ELECTRICAL CHARACTERISTICS

Minimum and Maximum apply over the junction temperature range of –40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at +25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply: VCC = 10 V, F_{SW} = 100 kHz 50% Duty Cycle, No Load on OUT.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY INPUT						
VCC_{ON}	Controller enable threshold		12	12.8	13.5	V
VCC_{OFF}	Minimum operating voltage		7.0	7.5	8.0	V
V_{RST}	Internal logic reset (fault latch)		4.5	5.0	5.5	V
ICC_{ST}	ICC current while in standby mode	COMP = 0.5V, CS = 0 V, no switching		340	420	µA
ICC_{OP}	Operating supply current	COMP = 2.25 V, OUT switching		800		µA
SHUTDOWN CONTROL (VSD pin)						
$I_{VSD\ OFF}$	Off state leakage current			0.1		µA
$V_{VSD\ ON1}$	ON state pull-down voltage at 10 uA	After VCC_{ON} (I_{VSD} = 10 uA)		0.65		V
V_{VSD_ON2}	ON state pull-down voltage at 100 uA	After VCC_{ON} (I_{VSD} = 100 uA)		0.84		V
SKIP CYCLE MODE COMPARATOR						
V_{SKIP}	Skip cycle mode enable threshold	CS Rising	70	120	170	mV
$V_{SK\text{-}HYS}$	Skip cycle mode hysteresis			12		mV
QR DETECT						
V_{OVP}	Overvoltage comparator threshold		2.85	3	3.17	V
T_{OVP}	Sample delay for OVP		870	1050	1270	ns
V_{DEM}	VDEM demagnetization threshold			0.35		V
F_{MAX}	Maximum frequency		114	130	148	kHz
T_{RST}	$T_{RESTART}$		9.4	12	15.7	µs
PWM COMPARATORS						
TP_{PWM}	COMP to OUT delay	COMP set to 2 V CS stepped 0 to 0.4 V, time to OUT transition low, C_{LOAD} = 0		20		ns
D_{MIN}	Minimum duty cycle	COMP = 0 V			0	%
G_{COMP}	COMP to PWM comparator gain			0.33		
$V_{COMP\text{-}O}$	COMP open circuit voltage	I(COMP)=20µa	4.3	4.9	5.8	V
$V_{COMP\text{-}H}$	COMP at maximum VCS			2.25		V
I_{COMP}	COMP short circuit current	COMP = 0 V		132		µA
R_{COMP}	R pull-up		41	45	49	kΩ

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ELECTRICAL CHARACTERISTICS (continued)

Minimum and Maximum apply over the junction temperature range of –40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at +25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply: VCC = 10 V, F_{SW} = 100 kHz 50% Duty Cycle, No Load on OUT.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
V_{CS}	Cycle-by-cycle sense voltage threshold		450	500	550	mV
T_{LEB}	Leading edge blanking time			130		ns
T_{PCS}	Current limit to OUT delay	CS step from 0 to 0.6 V time to onset of OUT transition low, C_{LOAD} = 0		22		ns
R_{LEB}	CS blanking sinking impedance			15	35	Ω
G_{CM}	Current mirror gain	I_{QR} = 2 ma		100		A/A
C_{FF}	Current feed forward	I_{QR} = 2 ma		140		mV
HICCUP MODE						
$T_{OL\_}10$	Over load detection timer	I_{VSD}= 10 uA		12		ms
$T_{OL\_}100$	Over load detection timer	I_{VSD}= 100 uA		1.2		ms
OUTPUT GATE DRIVER						
V_{OH}	OUT high saturated	I_{OUT} = 50 mA, VCC-OUT		0.3	1.1	V
V_{OL}	OUT low saturated	I_{OUT} = 100 mA		0.3	1	V
I_{PH}	Peak OUT source current	OUT = VCC/2		0.3		A
I_{PL}	Peak OUT sink current	OUT = VCC/2		0.7		A
t_r	Rise time	C_{LOAD} = 1 nF		25		ns
t_f	Fall time	C_{LOAD} = 1 nF		15		ns
SOFT-START						
I_{SS}	Soft-start		17	22	30	µA
THERMAL						
T_{SD}	Thermal shutdown temp			165		ºC

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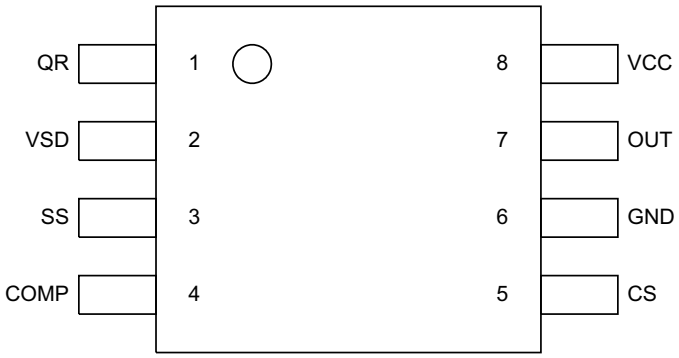
PIN FUNCTIONS

NAME	NO.	TYPE	DESCRIPTION
COMP	4	I	Control input for the Pulse Width Modulator and Skip cycle comparators. COMP pull-up is provided by an internal 42 K resistor which may be used to bias an opto-coupler transistor.
CS	5	I	Current sense input for current mode control and over-current protection. Current limiting is accomplished using a dedicated current sense comparator. If the CS comparator input exceeds 0.5 V, the OUT pin switches low for cycle-by-cycle current limit. CS is held low for 90 ns after OUT switches high to blank the leading edge current spike.
GND	6	G	Ground connection return for internal circuits.
OUT	7	O	High current output to the external MOSFET gate input with source/sink current capability of 0.3 A and 0.7 A respectively.
QR	1	I	The auxiliary FLYBACK winding of the power transformer is monitored to detect the Quasi-Resonant operation. The peak auxiliary voltage is sensed to detect an output overvoltage (OVP) fault and shuts down the controller.
SS	3	O	An external capacitor and an internal 22 μA current source sets the soft-start ramp.
VSD	2	O	Connect this pin to the Gate of the external start-up circuit FET; it will disable the start-up FET after VCC is valid.
VCC	8	P	VCC provides bias to controller and gate drive sections of the LM5023. An external capacitor must be connected from this pin to ground.

DEVICE INFORMATION



LM5023 Pin Configuration

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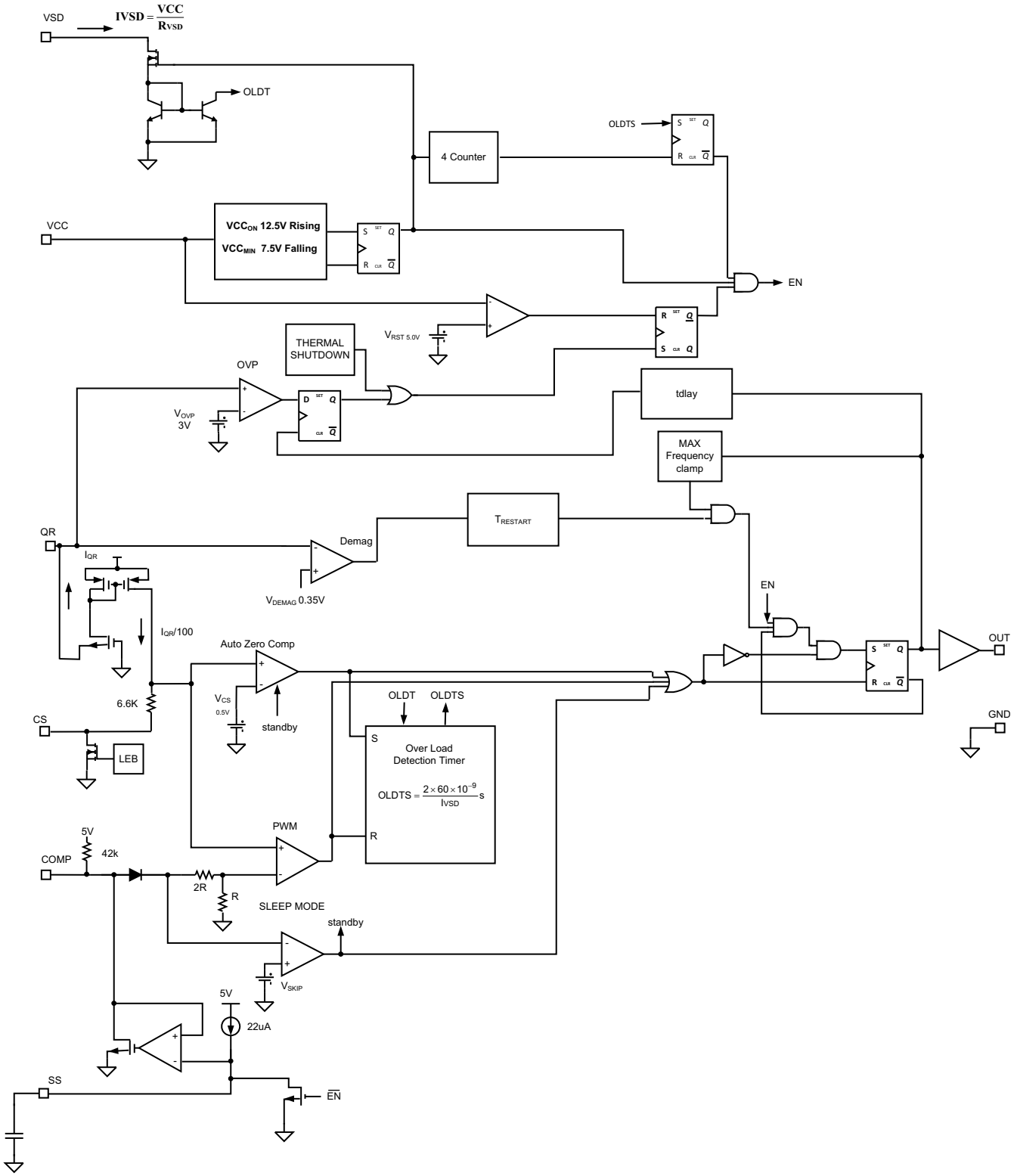
FUNCTIONAL BLOCK DIAGRAM



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TYPICAL CHARACTERISTICS

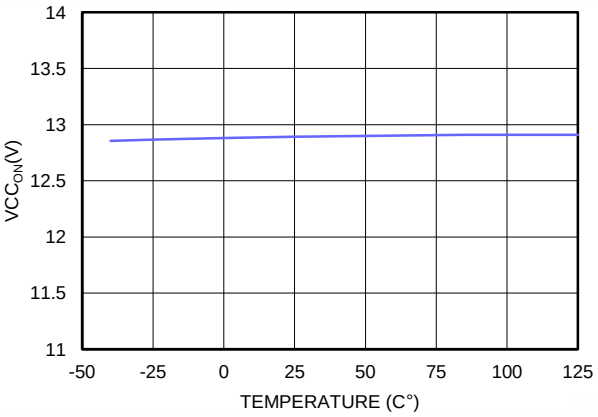

Figure 1. VCC_{ON} vs. Temperature

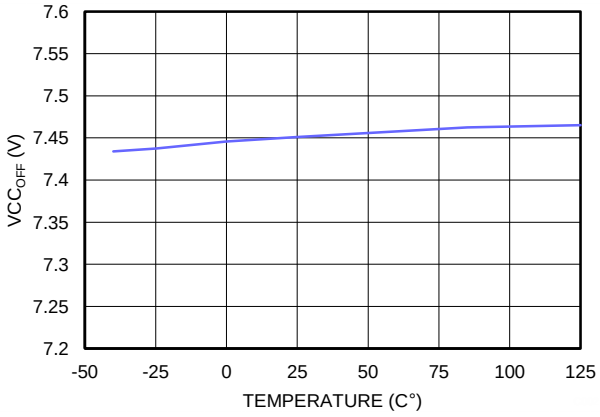

Figure 2. VCC_{OFF} vs. Temperature

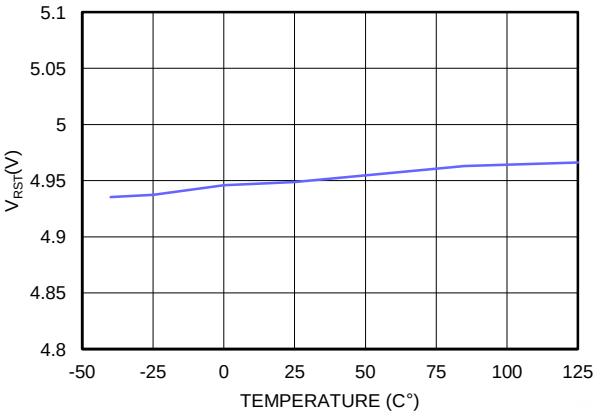

Figure 3. V_{RST} vs. Temperature

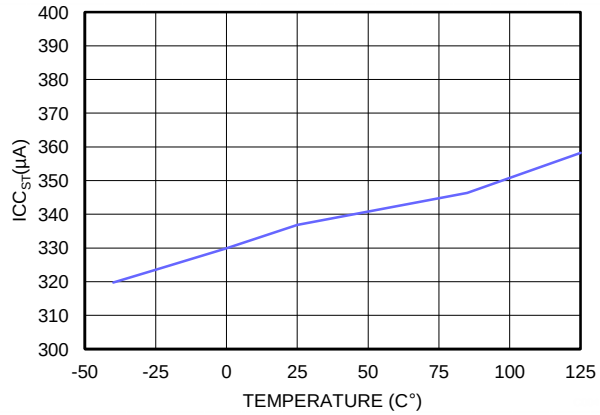

Figure 4. ICC_{ST} vs. Temperature

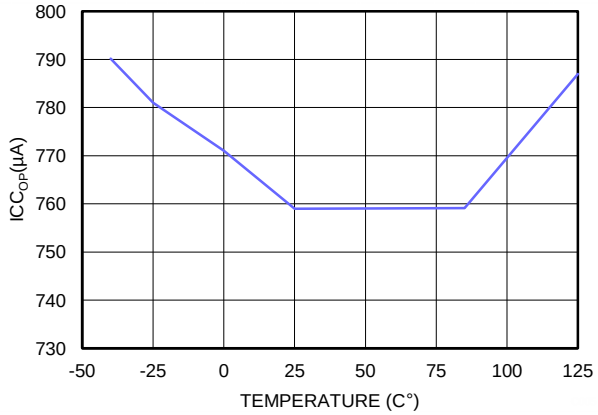

Figure 5. ICC_{OP} vs. Temperature

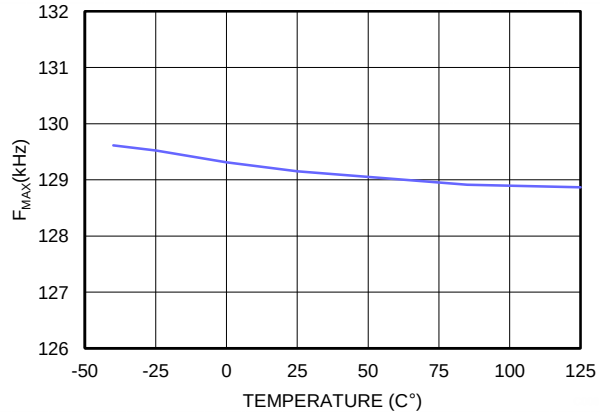

Figure 6. F_{MAX} vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

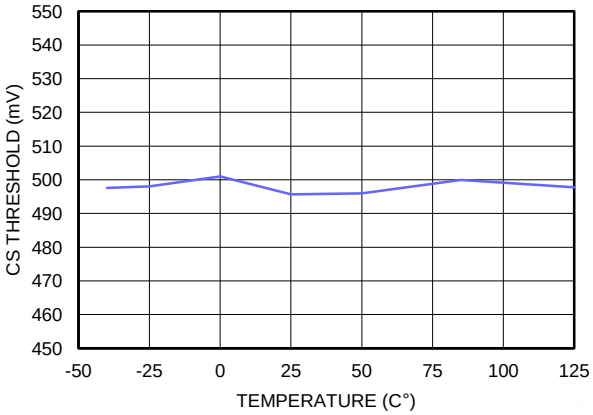

Figure 7. CS Threshold vs. Temperature

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FUNCTIONAL DESCRIPTION

The LM5023 is a Quasi-Resonant controller which contains all of the features needed to implement a highly efficient off-line power supply. The LM5023 uses the transformer auxiliary winding for demagnetization detection to ensure Quasi-Resonant operation (Valley-Switching) to minimize switching losses. For application that need to meet the ENERGY STAR® low standby power requirements, the LM5023 features an extremely low Iq current (346 µA) and skip cycle mode which reduces power consumption at light loads. The LM5023 uses a feedback signal from the output to provide a very accurate output voltage regulation <1%. To reduce overheating and stress during a sustained overload conditions the LM5023 offers a hiccup mode for over current protection and provides a current limit restart timer to disable the outputs and forcing a delayed restart (hiccup mode).

For offline start-up, an external Depletion Mode N Channel MOSFET can be used. This method is recommended for applications where a very low standby power (<50 mW) is required. For application where a low standby power is not as critical an enhancement mode, N Channel MOSFET can be used. If an OVP is detected on the auxiliary winding (QR pin), the IC permanently latches off, requiring recycling of power to restart Additional features include line-current-feed forward, pulse-by-pulse current limit, and a maximum frequency clamp of 130 kHz.

START-UP

Referring to Figure 8, when the AC rectified line voltage is applied to the bulk energy storage capacitor; the N Channel Depletion Mode MOSFET is turned on and supplies the charging current to the VCC capacitor. When the voltage on the VCC pin reaches 12.5 V typical, the PWM controller, soft-start circuit and gate driver are enabled.

When the LM5023 is enabled and the OUT drive signal starts switching the Flyback MOSFET, energy is being stored and then transferred from the transformer primary to the secondary windings. A bias winding, shown in Figure 8, delivers energy to the VCC capacitor to sustain the voltage on the VCC pin. The voltage supplied from the auxiliary winding should be within the range of 10 V to 14 V (where 16 V is the absolute maximum rating).

After reaching the VCC_{ON} threshold the LM5023 VSD open Drain output, which is pulled up to VCC during start-up, goes low. This applies a negative Gate to Source voltage on the Depletion Mode MOSFET turning it off. This disables the high voltage start-up circuit. The high voltage start-up circuit can be implemented in either of two ways; the first is shown in Figure 8, which uses an N Channel Depletion Mode FET, the second is shown in Figure 9, which uses an N Channel Enhancement Mode FET. The circuit using the Depletion Mode FET will have the lowest standby power. The standby power consumption of the FET is the voltage across the start-up FET multiplied by the Drain to Source Cutoff current with Gate negatively biased, this is typically 0.1 µA.

Standby Power of the Start-up FET calculation:

- $Vin = 230Vac$
- $VCC = 10V$
- $Vdc\,max = 230Vac \bullet \sqrt{2} = 325Vdc$
- $I_{DOFF} = 0.1\mu A$, I_{DOFF} is the Depletion MODE FETs leakage current
- $Pd = I_{DOFF} \bullet Vdc\,max = 0.1uA \bullet 325Vdc = 32.5\mu W$

When VCC < VCC(on) the current consumption of the $I_C = I_{CC(st)}$, nominally 340 µA.

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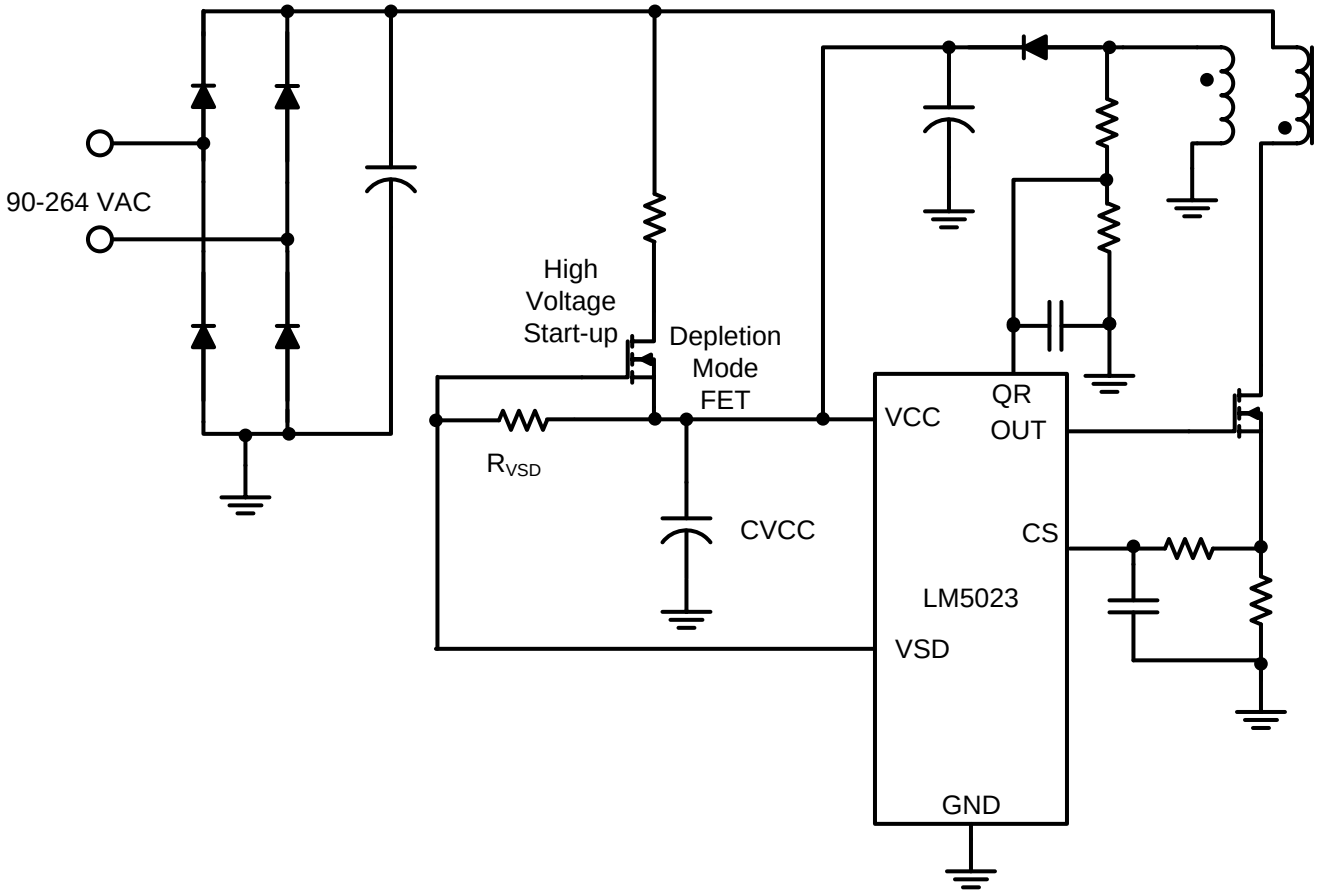

Figure 8. Start-Up With a Depletion Mode FET

An alternative start-up circuit employs an Enhancement Mode FET with resistors connected from the rectified dc bus to the Gate of the FET, Figure 9. After the input AC power is applied the Enhancement Mode FET supplies the charging current to the VCC capacitor C_{VCC}. After reaching the VCC_{ON} threshold the LM5023 VSD open Drain output, which is pulled up to VCC during start-up, goes low. This grounds the Gate of the start-up MOSFET turning it off. The start-up resistors are always in the circuit, therefore the standby power consumed will be higher than if a Depletion Mode FET were used.

- Vin = 230 Vac
- VCC = 10 V
- $Vdc\,max = 230Vac \bullet \sqrt{2} = 325Vdc$
- $Rstart - up = 10M\Omega$
- $P_{Resistors} = \frac{Vdc^2}{Rstart - up} = \frac{325^2}{10M\Omega} = 10.56mW$

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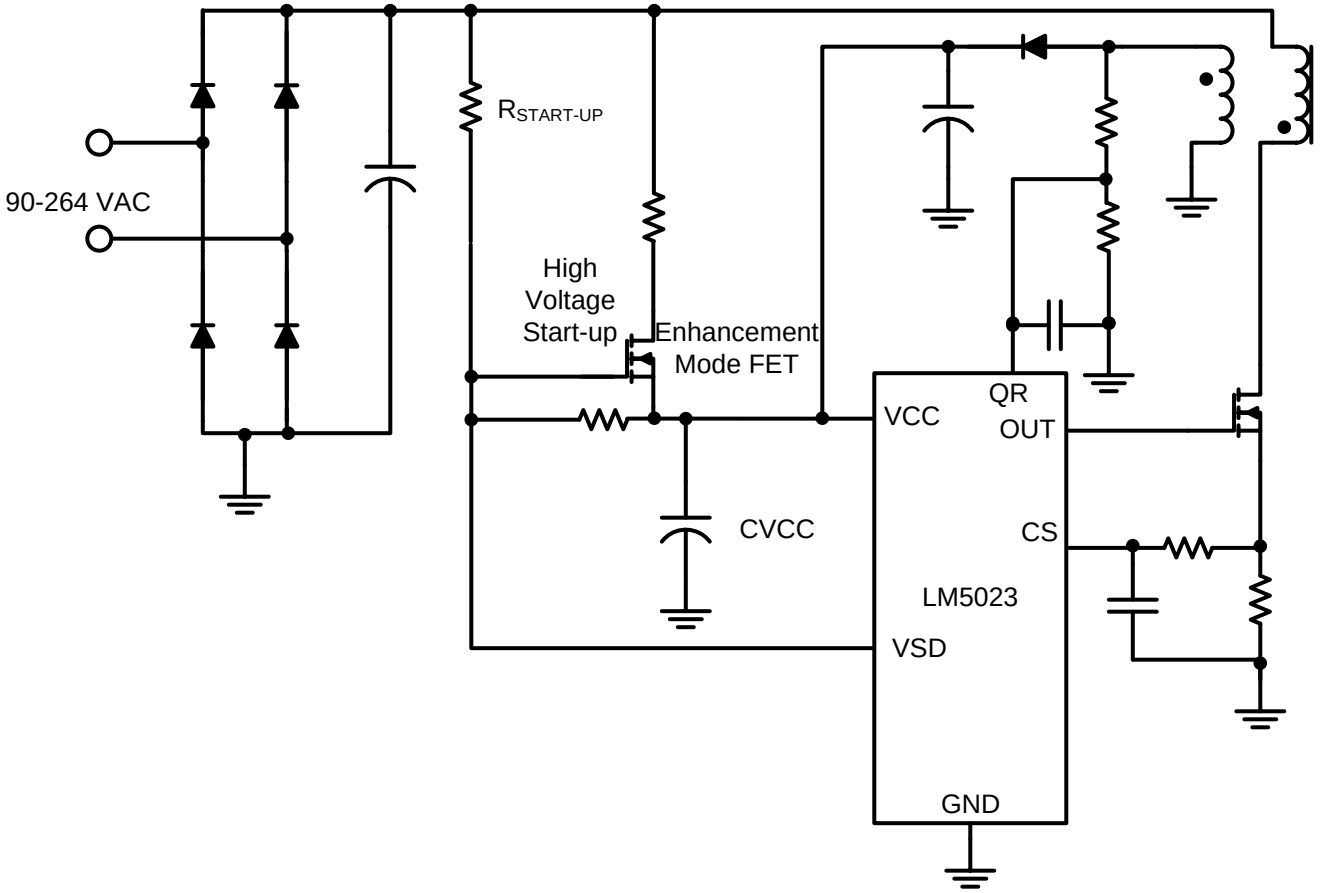

Figure 9. Start-Up With an Enhancement Mode FET

Quasi Resonant Operation

A Quasi-Resonant controlled Flyback converter operates by storing energy in the transformers primary during the MOSFETs on-time. During the on-time (T_{ON}) VIN is applied across the primary of the transformer. The primary current starts out at zero and ramps towards a peak value (I_{PEAK}). When the peak primary current reaches the feedback compensation error voltage the PWM comparator resets the output drive, turning off the MOSFET. Due to the phasing of the transformer, the output diode is reversed biased during the MOSFET on-time.

During the MOSFETs off time the output diode is forward biased and the stored energy in the transformer primary inductor is transferred to the output. The voltage seen on the secondary inductor is V_{OUT} plus the output diodes forward voltage drop, V_F. The current in the output inductor linearly decreases from I_{PEAK} • Ns/Np to zero, refer to Figure 11.

When the current in the secondary reaches zero, the transformer is demagnetized, and there is an open circuit on the secondary, and with the primary MOSFET also turned off, there is an open on the primary. A resonant circuit is formed between the transformers primary inductance and the MOSFET output capacitance. The resonant frequency is calculated by:

$$\text{Freq} = 2 \bullet \pi \sqrt{\text{Lp} \bullet \text{COSS}}$$

During the resonant period the Drain voltage of the MOSFET will ring down towards ground, refer to Figure 10. When the Drain voltage is at its minimum the Flyback MOSFET is turned back on. The point where the voltage is at its minimum is calculated by:

$$\text{td} = \pi \bullet \sqrt{\text{Lp} \bullet \text{COSS}}$$

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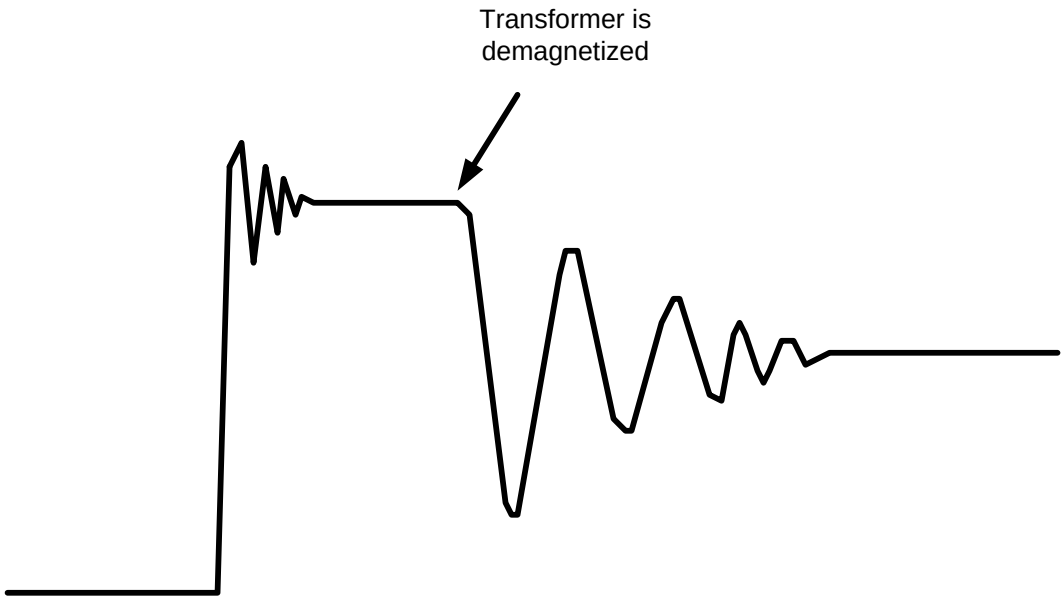

Figure 10. The Flyback Drain Voltage Waveform

Transformer demagnetization is detected by sensing the transformers auxiliary winding. When the transformer is demagnetized the auxiliary winding voltage follows the Drain of the MOSFET and changes from Vout•Naux/Ns to -Vin•Naux/Np. Internal to the LM5203 QR pin is a comparator with a 0.35 V reference. As the auxiliary winding voltage falls below 0.35 V, the voltage is sensed and the comparator sets the PWM Flip-Flop turning on the Flyback MOSFET. Figure 11 shows the QR Converter typical waveforms; the auxiliary winding voltage, primary, and secondary current waveforms. It is possible to adjustable the delay on the auxiliary winding with a resistor and external capacitor to ensures that the MOSFET switches when its Drain voltage is at its minimum, refer to the schematic in Figure 14 and the section on Valley Switching for details. The benefits of QR operation are reduced EMI, and turn-on switching losses.

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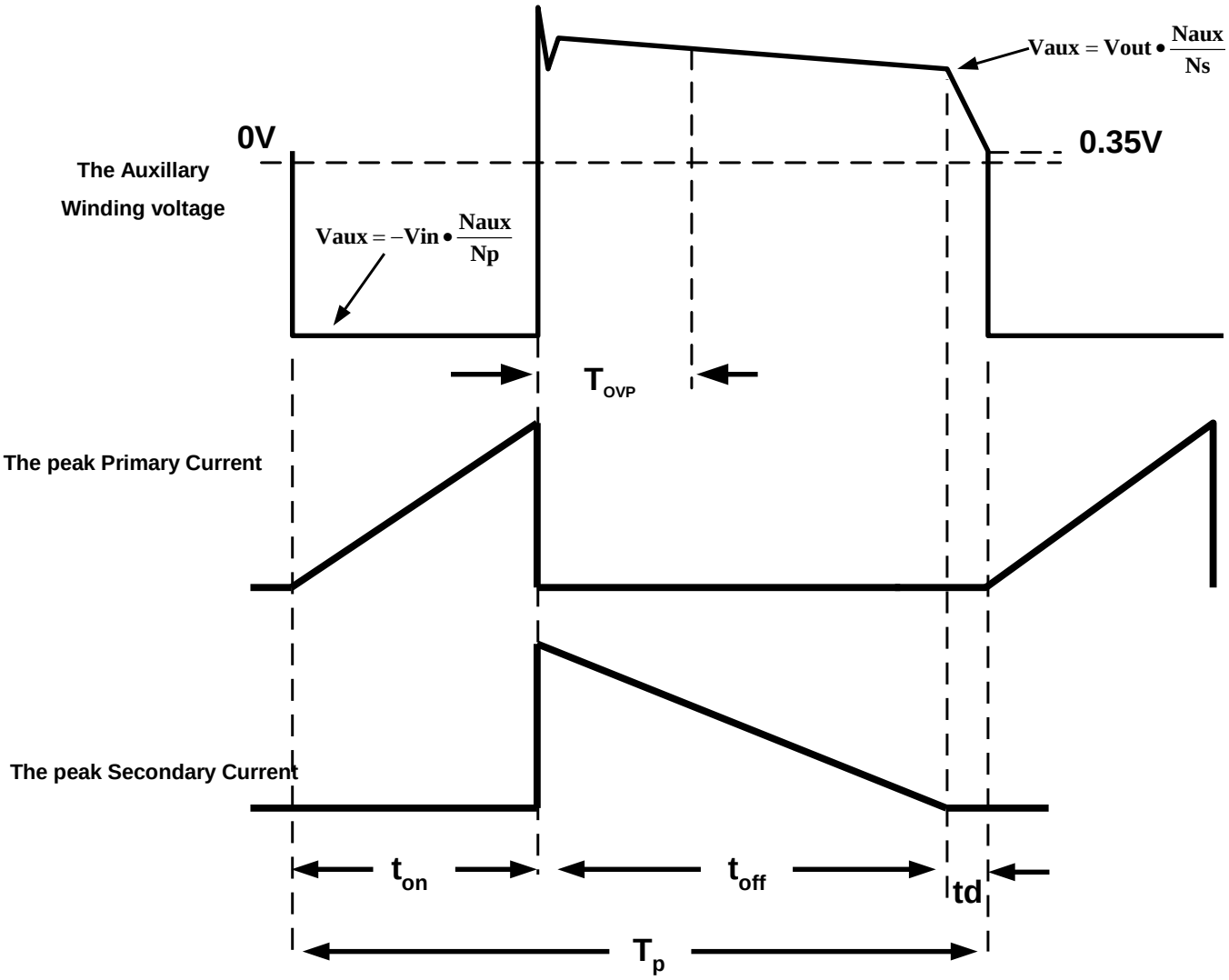

Figure 11. QR Converter Typical Waveforms

Quasi Resonant Operating Frequency

When the primary side Flyback MOSFET turns on, the current ramps up until the peak primary current exceeds the feedback compensation error voltage. When this occurs the PWM comparator resets the output drive, turning off the MOSFET. The current ramps up with a slope of:

$$\frac{Vin}{Lp} = \frac{di}{dt}$$

The t_{ON} time of the switch is calculated by:

$$ton = \frac{Lp}{Vin} \bullet Ipk$$

When the primary side Flyback MOSFET is turned off, the energy stored in the primary inductance is transfer to the secondary inductance, the off time to transfer all of the energy is:

$$toff = Ipk \bullet \frac{n \bullet Lp}{Vo + Vf}$$

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The total switching period is:

$$Tp = ton + toff + tdly$$

The resonant circuit created by the transformer primary inductance and the MOSFETs output capacitance is the tdly time, refer to Figure 11.

$$tdly = \frac{\pi}{2} \bullet \sqrt{Lp \bullet COSS}$$

$$Pout = \frac{1}{2} \bullet Lp \bullet Ipk^2 \bullet Freq \bullet \eta$$

Combining equations:

$$Freq := \frac{1}{\left[Lp \cdot 2 \cdot Pout \cdot \left[\frac{n \cdot (Vo + Vf + Vin}{\eta \cdot \left[Vin \cdot \left[n \cdot (Vo + Vf) \right] \right]} \right]^2 \right] + tdly}$$

From inspection of the equations, it can be seen that the QR Flyback converter does not operate at a fixed frequency. The frequency varies with the output load, input line voltage, or a combination of the two. In order to keep LM5023 frequency below the EMI starting limit of 150 kHz per CISPR--22, the LM5023 has an internal timer which prevents the output drive from restarting within 7.69 µs of the previous driver output (OUT) high to low transition. This timer clamps the maximum switching frequency from exceeding 130 kHz (typical).

PWM Comparator

The PWM comparator compares the current sense signal with the loop error voltage from the COMP pin. The COMP pin voltage is reduced by a fixed 0.75 V offset and then attenuated by a 3:1 resistor divider. The PWM comparator input offset voltage is designed such that less than 0.75 V at the COMP pin will result in a zero duty cycle at the controller output.

Soft-Start

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thereby reducing start-up stresses and current surges. At power on, after the VCC reaches the VCC_{ON} threshold an internal 22 µA current source charges an external capacitor connected to the SS pin. The capacitor voltage will ramp up slowly and will limit the COMP pin voltage and the duty cycle of the output pulses.

Gate Driver

The LM5023 driver (OUT) was designed to drive the gate of an N Channel MOSFET and is capable of sourcing a peak current of 0.4 A and sinking 0.7 A.

Skip Cycle Operation

During light load conditions, the efficiency of the switching power supply typically drops as the losses associated with switching and operating bias currents of the converter become a significant percentage of the power delivered to the load. The largest component of the power loss is the switching loss associated with the gate driver and external MOSFET gate charge. Each PWM cycle consumes a finite amount of energy as the MOSFET is turned on and then turned off. These switching losses are proportional to the frequency of operation.

To improve the light load efficiency the LM5023 enters a Skip Cycle mode during light load conditions. As the output load is decreased, the COMP pin voltage is reduced by the voltage feedback loop to reduce the Flyback converters peak primary current. Referring to the Block Diagram , the PWM comparator input tracks the COMP pin voltage through a 0.75 V level shift circuit and a 3:1 resistor divider. As the COMP pin voltage falls, the input to the PWM comparator falls proportionately. When the PWM comparator input falls to 125 mV, the Skip Cycle comparator detects the light load condition and disables output pulses from the controller. The LM5023 also reduces all internal bias currents, while in skip mode, to further reduce quiescent power. The controller continues to skip switching cycles until the power supply output falls and the COMP pin voltage increases to demand more output current. The number of cycles skipped will depend on the load and the response time of the frequency

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voltage loop compensation network. Eventually the COMP voltage will increase when the voltage loop requires more current to sustain the regulated output voltage. When the PWM comparator input exceeds 135 mV (10 mV hysteresis), normal fixed frequency switching resumes. Typical light load operation power supply designs will produce a short burst of output pulses followed by a long skip cycle interval (no drive pulses). The result is a large reduction in the average input power.

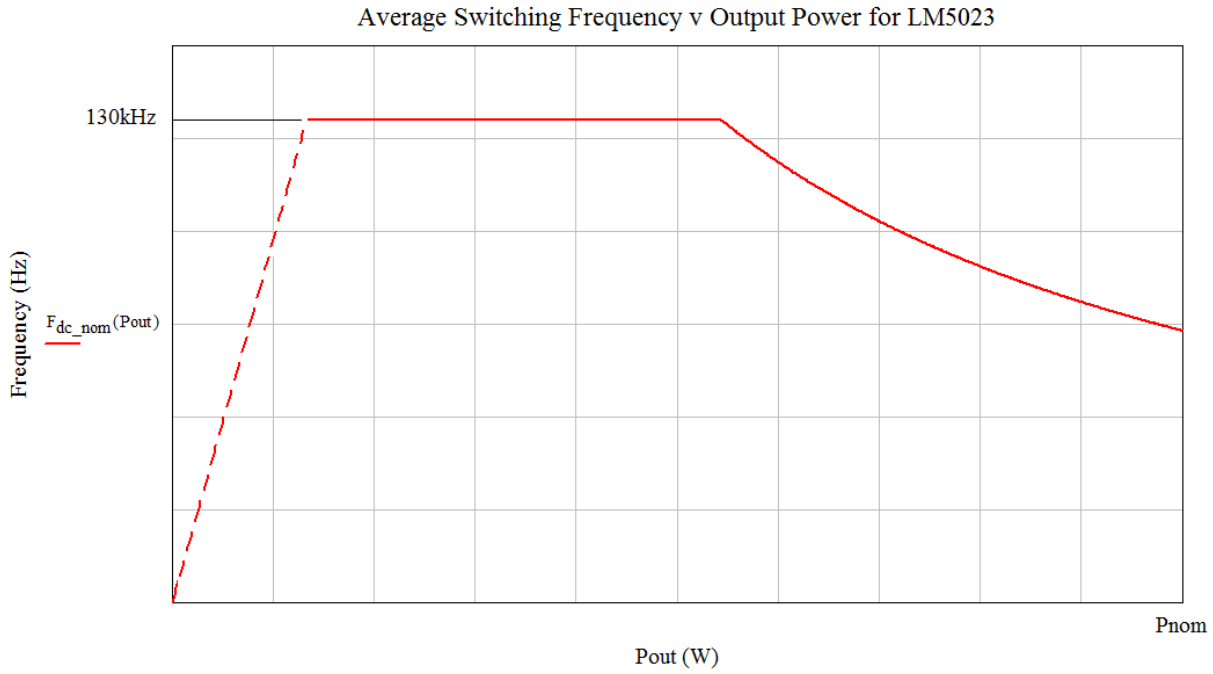

Figure 12. LM5023 Modulation Curve

Current Limit/Current Sense

The LM5023 provides a cycle-by-cycle over current protection feature. Current limit is triggered by an internal current sense comparator with a threshold of 500 mV. If the CS pin voltage plus the current limit feed forward signal voltage exceeds 500 mV, the MOSFET drive signal (OUT) will be terminated. An RC filter, located near the LM5023 CS pin is recommended to attenuate the noise coupled from the power FET's gate to source switching. The CS pin capacitance is discharged at the end of each PWM cycle by an internal switch. The discharge switch remains on for an additional 90 ns for Leading Edge Blanking (LEB). LEB prevents the LM5023 current sense comparator from being falsely triggered due to the noise generated by the switch currents initial spike. The LM5023 current sense comparator is very fast, and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the IC (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor, which should also be located close to the IC. If a current sense resistor located in the power FET's source is used for current sense, a low inductance resistor is required. In this case, all of the noise sensitive low current grounds should be connected in common near the IC and then a single connection should be made.

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APPLICATION INFORMATION

Line Current Limit Feed Forward

In a peak current mode controlled when the power supply is in an overload, the peak current (measured across the current sense resistor VCS) is compared to a voltage reference for overload protection. If the peak current exceeds the reference the LM5023 controller will turn off the primary side Flyback MOSFET on a cycle-by-cycle basIs. However, the primary switch can't be turned off instantly, as there are several unavoidable delays. The first delay is caused by the LEB circuit which provides leading-edge blanking. The second delay is caused by the propagation delay between the detecting point of VCS and the actual turn off of the power MOSFET. The total delay time (tprop) refer to Figure 13, includes the current limit comparator, the logic, the gate driver, and the power MOSFET turning off.

The propagation delay causes the peak primary current to overshoot, the overshoot increase the maximum peak current beyond the calculated value. The peak current overshoot increase as the AC line voltage increase because of the increase in the slope of the primary current:

$$\frac{Vin}{Lp} = \frac{di}{tprop}$$

This increase in the peak input current overshoot causes a wide variation of overpower limit in a Flyback converter. In Figure 4, it can be seen that the overpower limit increases with the input line voltage, because of Ipkmax increase:

$$Ipk\,max = \sqrt{\frac{Pout \bullet 2}{Lp \bullet Freq \bullet \eta}} + \frac{Vin}{Lp} \bullet tprop$$

$$Pin = \frac{1}{2} \bullet Ipk_{max}^{2} \bullet Lp \bullet Freq$$

$$Pout = \frac{Pin}{\eta}$$

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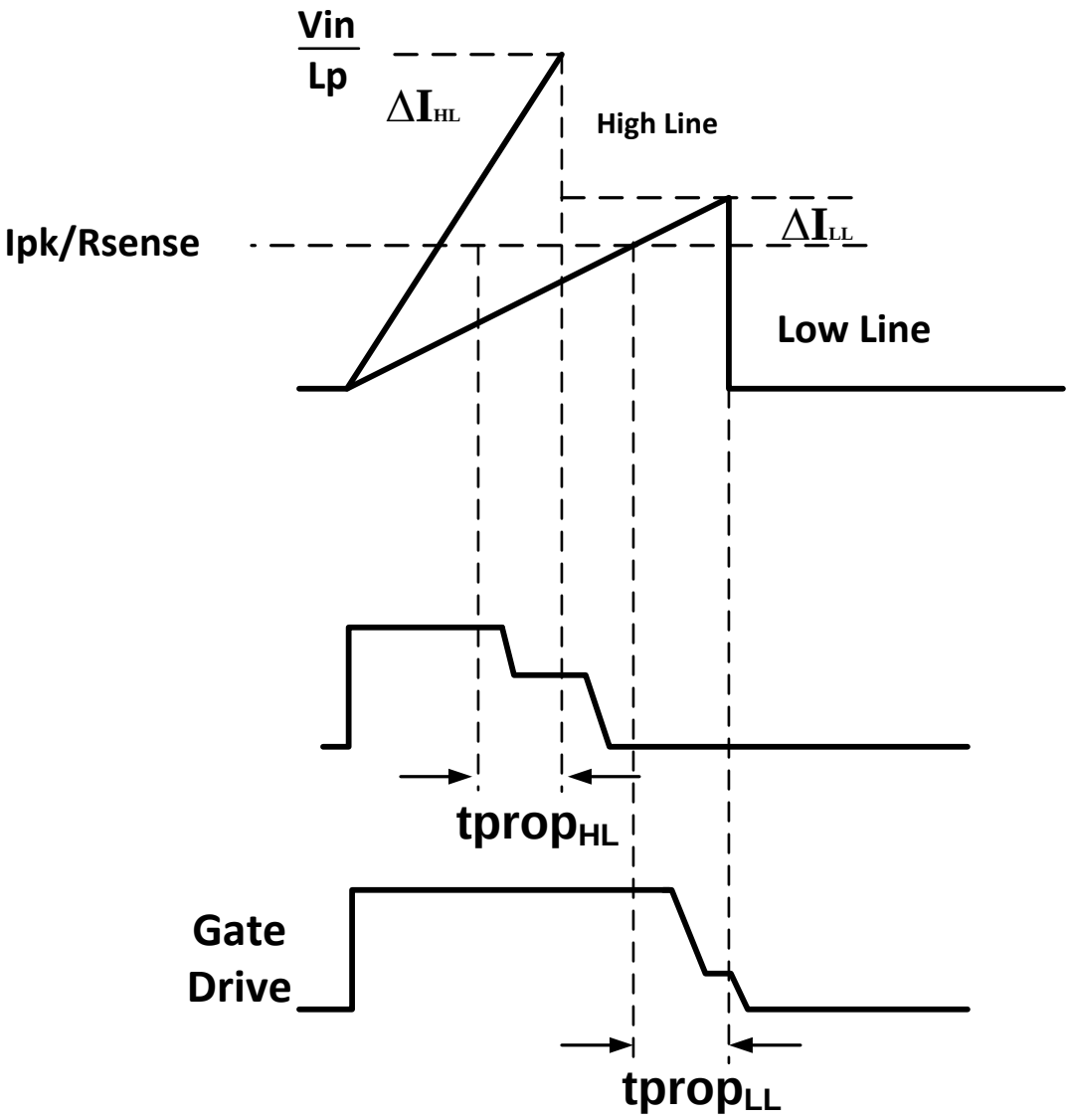

Figure 13. Line Current Feed Forward

To improve the overpower limit accuracy over the full Universal Input Line; the LM5023 integrates Line Current Limit Feed Forward. Line Current Limit Feed Forward improve the overpower limit by summing a current proportional to the input rectified line into the current sense resistor R_{SENSE}), refer to Figure 14. The current proportional to the input line biases up the current sense pin, this turns off the Flyback MOSFET earlier at high input line. This feature compensates for the propagation delays creating a overpower protection that is nearly constant over the Universal Input Line.

To implement Line Current Limit Feed Forward, the first step is to calculate the QR switching frequency at low line and then at high line when the power supply is operating in current limit.

For our example:

- Lp = 400 µH
- R_{SENSE} = 0.15 Ω
- Vdc_{min} = 127 V
- Vdc_{max} = 325 V
- Tprop = 160 ns
- V_{CS} = 0.5 V

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- naux = 10.9
- n = ns/np = .167
- tdly = 580 ns

$$Freq\_LL = \frac{1}{\left(\frac{Vcs}{Rsense}\right) \bullet Lp \bullet \left[\left(\frac{1}{Vdc\,min}\right) + \frac{1}{(Vout + Vf) \bullet n}\right] + tdly}$$

$$Freq\_LL = \frac{1}{\left(\frac{0.5V}{0.15\Omega}\right) \bullet 400\mu H \bullet \left[\left(\frac{1}{127V}\right) + \frac{1}{(19V + 0.7V) \bullet 6}\right] + 580ns} = 49.6kHz$$

$$Freq\_HL = \frac{1}{\left(\frac{Vcs}{Rsense}\right) \bullet Lp \bullet \left[\left(\frac{1}{Vdc\,max}\right) + \frac{1}{(Vout + Vf) \bullet 6}\right] + tdly}$$

$$Freq\_HL = \frac{1}{\left(\frac{0.5V}{0.15\Omega}\right) \bullet 400\mu H \bullet \left[\left(\frac{1}{325V}\right) + \frac{1}{(19V + 0.7V) \bullet 6}\right] + 580ns} = 62.3kHz$$

The next step is to calculate the uncompensated output power at the minimum and maximum input line voltage while in current limit.

$$Pout\_LL = \frac{1}{2} \bullet Lp \bullet \left(\frac{VCS}{Rsense}\right)^2 \bullet Freq\_LL \bullet \eta$$

$$Pout\_LL = \frac{1}{2} \bullet 400\mu H \bullet \left(\frac{0.5}{0.15}\right)^2 \bullet 49.6kHz \bullet 0.86 = 94.9W$$

$$Pout\_HL = \frac{1}{2} \bullet Lp \bullet \left(\frac{VCS}{Rsense}\right)^2 \bullet Freq\_HL \bullet \eta$$

$$Pout\_HL = \frac{1}{2} \bullet 400\mu H \bullet \left(\frac{0.5}{0.15}\right)^2 \bullet 62.3kHz \bullet 0.86 = 119.1W$$

Step three is to calculate the peak current at high line so it does not deliver more power than while it is operating at low line (94.9 W). One thing that complicates the Line Current Limit Feed Forward calculation is that with Quasi Resonant operation the switching frequency changes with line and load. We have two equations and two unknowns, the peak primary current and the QR frequency. This requires use of the quadratic equation:

$$ax^2 + Bx + C = 0$$

The positive root is:

$$x = \frac{\left(B + \sqrt{B^2 + 4DT}\right)}{4}$$

$$Freq\_Comp = \frac{4}{\left[\left(\sqrt{4 \bullet tdly + \frac{2 \bullet Lp \bullet Pout\_LL \bullet (Vout + Vf + n \bullet Vdc\,max)^2}{\eta \bullet Vdc\,max^2 \bullet (Vout + Vf)^2}}\right) + \frac{\sqrt{2} \bullet Lp \bullet Vout + Vf + n \bullet Vdc\,max \bullet \sqrt{\frac{Pout\_LL}{\eta \bullet Lp}}}{Vdc\,max \bullet (Vout + Vf)}\right]^2}$$

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$$Freq\_Comp = \frac{4}{\left[\left(\sqrt{4 \bullet 580ns + \frac{2 \bullet 400\mu H \bullet 94.9 \bullet (19 + 0.7 + 0.167 \bullet 325V)^2}{0.86 \bullet 325V^2 \bullet (19V + 0.7V)^2}}\right) + \frac{\sqrt{2} \bullet 400\mu H \bullet (19V + 0.7V + 0.167 \bullet 325V) \bullet \sqrt{\frac{94.9W}{0.86 \bullet 400\mu H}}}{325V \bullet (19V + 0.7V)}\right]^2} = 76.8kHz$$

Step four is to calculate the peak current.

$$ILmax\_LL = \sqrt{\frac{2 \bullet Pout\_LL}{\eta \bullet Lp \bullet Freq\_Comp}}$$

$$ILmax\_LL = \sqrt{\frac{2 \bullet 94.9W}{0.86 \bullet 400\mu H \bullet 76.8kHz}} = 2.679Apk$$

$$VCS\_CL = Rsense \bullet \left[ILmax\_CL - \left(\frac{Vdc\,max}{Lp}\right) \bullet tprop\right]$$

$$VCS\_CL = 0.15\Omega \bullet \left[2.679Apk - \left(\frac{325V}{400\mu H}\right) \bullet 160ns\right] = 0.382V$$

For the power supply to go into pulse-by-pulse current limit the voltage across the current sense resistor must be 0.5 V, so:

$$VCS\_OFFSET := V_{CS} - VCS\_CL$$

VCS_OFFSET is the required voltage offset that must be injected across the current sense resistor, R_{SENSE}.

$$VCS\_OFFSET := V_{CS} - VCS\_CL = 0.5V - 0.382V = 0.118V$$

After calculating the required offset voltage, use the following equations to calculate the required current feed forward:

While the main Flyback switch is on, Q1, the voltage on the Auxiliary winding will be negative and proportional to the rectified line.

$$-Vaux = \frac{Vdc}{Naux}$$

$$IQR = \frac{-Vaux}{R1}$$

IQR should be chosen in the range of 1 ma to 4 ma. The demagnetization circuit impedance should be calculated to limit the maximum current flowing through Pin 1 to less than 4 mA.

R_{OFFSET} = 6.6 kΩ + $R_{EXTERNAL}$ (the 6.6 kΩ resistance is internal to the LM5023).

Where: Naux is the number of turns on the Flyback primary (Np) divided by the number of turns on the transformer Auxiliary (Naux) winding. The current mirror in the QR pin input has a gain of 100; this will offset the voltage on the current sense pin by:

$$VCS_{OFFSET} = \frac{IQR}{100} \bullet \left(6.6k\Omega + R_{EXTERNAL}\right)$$

Set IQR= 1.75 mA

$$R_1 = \frac{\frac{Vdc\,max}{naux}}{IQR} = \frac{325V}{\frac{10.9}{1.75mA}} = 17.0k\Omega$$

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$$ROFFSET = \frac{VOFFSET}{IQR} \bullet 100 = \frac{0.118V}{1.75mA} \bullet 100 = 6742\Omega$$

$$ROFFSET = RINTERNAL + REXTERNAL$$

$$REXTERNAL = ROFFSET - 6.6k\Omega = 6742\Omega - 6.6k\Omega = 142\Omega$$

No external resistor is required based on the applications describe above, so a 499 Ω resistor and 100 pF capacitor are installed in the CS pin input as a noise filter.

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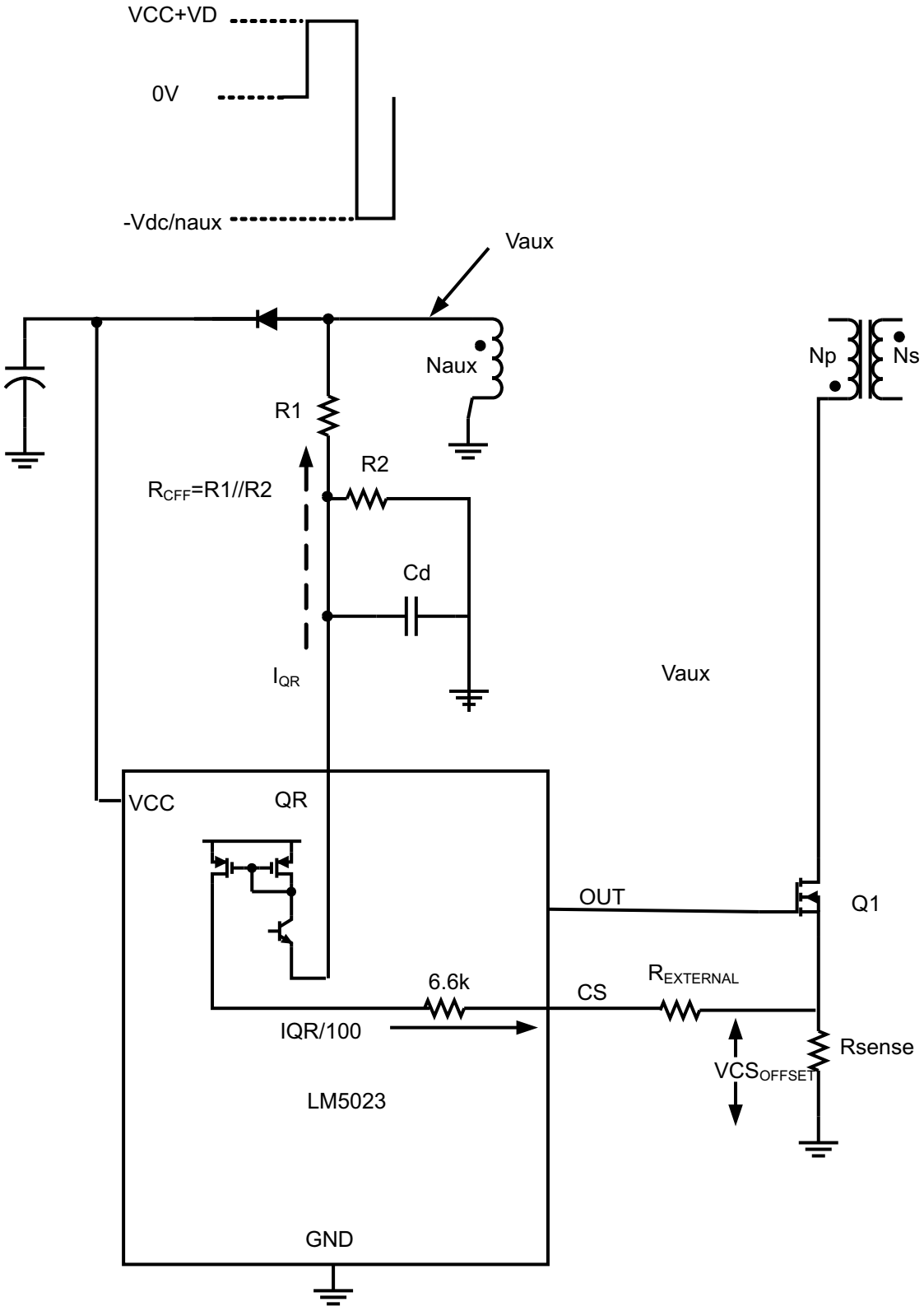

Figure 14. Current Feed Forward

Overvoltage Protection

Output overvoltage protection is implemented with the LM5023 by monitoring the QR pin during the time when the main Flyback MOSFET is off and the energy stored in the transformer primary is being transferred to the secondary. There is a delay prior to sampling the QR pin during the MOSFETs off time, TOVP. There are two reasons for the delay, the first is to blank the voltage spike which is a result of the transformers leakage inductance. The second is to improve the accuracy of the output voltage sensing, referring to the transformer auxiliary winding voltage shown in Figure 11. It is clear there is a down slope in the voltage which represents the decreasing VF of the output rectifier and resistance voltage drop (IS x RS) as the secondary current decreases to zero, so by delaying the sampling of the QR voltage a more accurate representation of the output voltage is achieved.

Connected to the QR pin is a comparator with a 3.0 V reference. The transformers auxiliary voltage is proportional to Vout by the transformers turns ratio:

$$Vaux=(V_O+V_F)\cdot Naux/Ns \quad (1)$$

To set the OVP, a voltage divider is connected to the transformers auxiliary winding, refer to Figure 13. In the section titled Line Current Limit Feed Forward, we developed equations to improve the power limit. Resistor R1 was calculated for Line Current Limit Feed Forward; to implement OVP we now need to calculate R2.

$$V_{OVP} = Vaux\_OVP \bullet \frac{R2}{R1+R2}$$

$$R2 = 3.0V \bullet \frac{R1}{Vaux\_OVP - 3V}$$

When an OVP fault has been detected, the LM5023 OUT driver is latched-off. VCC will discharge to VCCMIN and the VSD pin will be asserted high, allowing the Depletion Mode FET to turn-on and charge up the VCC capacitor to VCC_{ON}. The VSD pin will be toggled on-off-on to maintain VCC to the controller. The only way to clear the fault is to removed the input power and allow the controllers VCC voltage to drop below V_{RST}, 5.0 V.

Valley Switching

For QR operation the Flyback MOSFET is turned on with the minimum Drain voltage. The delay on the auxiliary winding can be adjusted with an external resistor and capacitor to improve valley switching. The delay-time, tdly, must equal half of the natural oscillation period:

$$tdly = \frac{\pi}{2} \bullet \sqrt{Lp \bullet COSS}$$

By substituting

$$tdly = RFF \bullet Cd$$

We can calculate the RC time constant to achieve the minimum Drain voltage when the LM5023 turns on the Flyback MOSFET.

$$Cd := \frac{\left[\left(\frac{\pi}{2}\right) \bullet \sqrt{Lp_{used} \bullet Coss}\right]}{RFF}$$

The LM5023 QR pin's capacitance is approximately 20 pF, so CdUSED = Cd -20 pF

$$RFF := \frac{(R1 \bullet R2)}{(R1+R2)}$$

R1 and R2 were previously calculated to set the Line Current Limit Feed Forward and Overvoltage protection.

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Hiccup Mode

Hiccup Mode is a method to prevent the power supply from over-heating during and extended overload condition. In an overload fault, the current limit comparator turns off the driver output on pulse-by-pulse basis. This starts the Over Load Detection Timer, after the Over Load Detection Timer (OLDT) times out, the current limit comparator is rechecked, if the power supply is still in an overload condition, the OUT drive is Latched-off and VCC is allowed to drop to VCC_{OFF} (7.5 V).

When VCC reaches VCC_{OFF}, the VSD open drain output is disabled allowing the Depletion Mode start-up FET to turn-on, charging up the VCC capacitor to VCC_{ON} (12.5 V). When VCC reaches VCC_{ON}, the VSD output goes low turning-off the Depletion Mode FET. The VCC capacitor is discharged from VCC_{ON} to VCC_{OFF} at a rate proportional to the VCC capacitor and the ICC_{ST} current (346 µA typical). The charging and discharging of the VCC capacitor is repeated four times (refer to Figure 15) so the total Hiccup time is:

$$t_{HICCUP} = t_{CHARGE} \bullet 4 + t_{DISCHARGE} \bullet 4$$

After allowing VCC to charge and discharge four times, the LM5023 goes through an auto restart sequence, enabling the LM5023 soft-start and driver output. It is important to set the Over Load Detection Timer long enough so that under low input line and full load conditions that the power supply will have enough time to start-up.

The Over Load Detection Timer can be set with the resister in series with the VSD pin ®$_{VSD}$), refer to Figure 8.

$$I_{VSD} = \frac{VCC}{R_{VSD}} = \frac{10V}{1M\Omega} = 10\mu A$$

$$OVER\_Load\_Detection\_Timer = \frac{2 \bullet 60nA}{I_{VSD}} = \frac{2 \bullet 60nA}{10\mu A} = 12m\,sec$$

Normally it is recommended that R_{VSD}>1 MΩ, if a lower value is used then the standby power will be higher.

Assuming:
If the Depletion Mode FET charges the VCC capacitor with 2 mA, VCC Capacitor is 10 uF.

$$t_{CHARGE} = \frac{(VCC_{ON} - VCC_{OFF})}{I_{CHARGE}} \bullet C_{VCC} = \frac{12.5V - 7.5V}{2mA} \bullet 10\mu F = 25ms$$

$$t_{DISCHARGE} = \frac{(VCC_{ON} - VCC_{OFF})}{ICC_{ST}} \bullet C_{VCC} = \frac{12.5V - 7.5V}{346\mu A} \bullet 10\mu F = 145ms$$

$$t_{HICCUP} = 25ms \bullet 4 + 145ms \bullet 4 = 680ms$$

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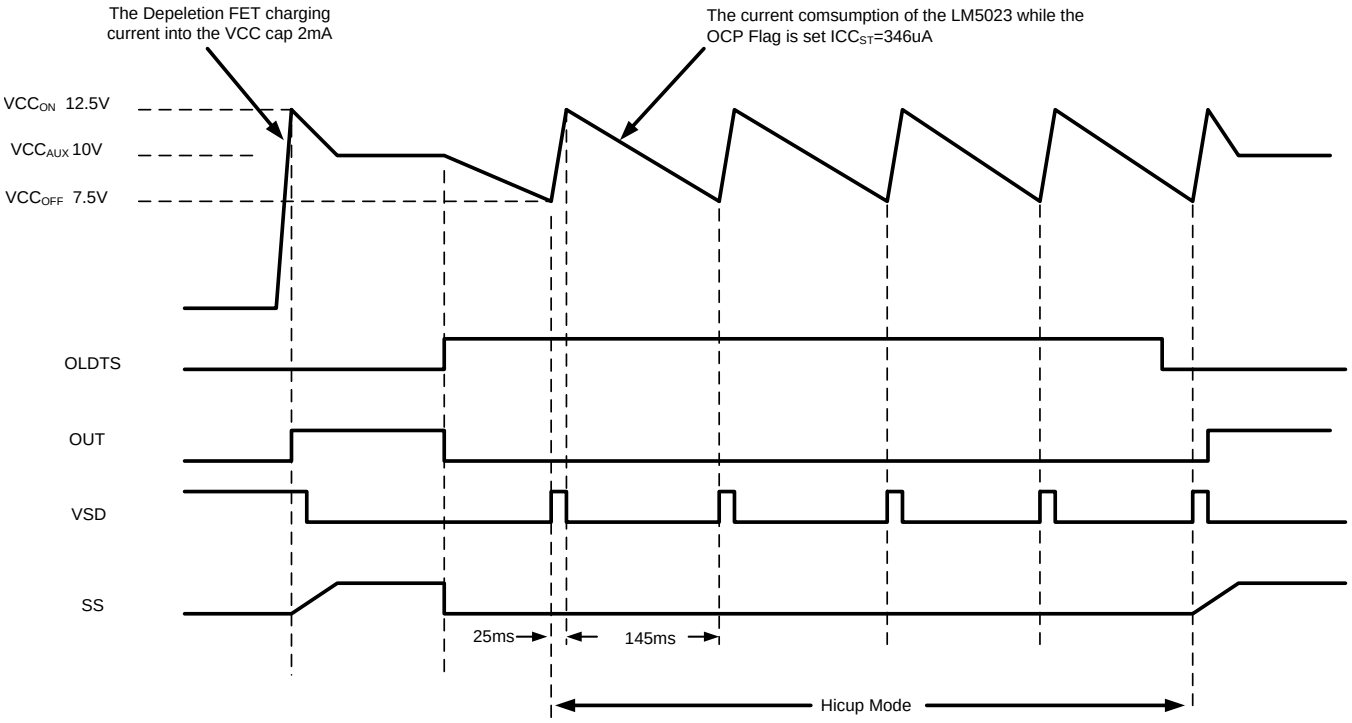

Figure 15. Hiccup Mode Timing

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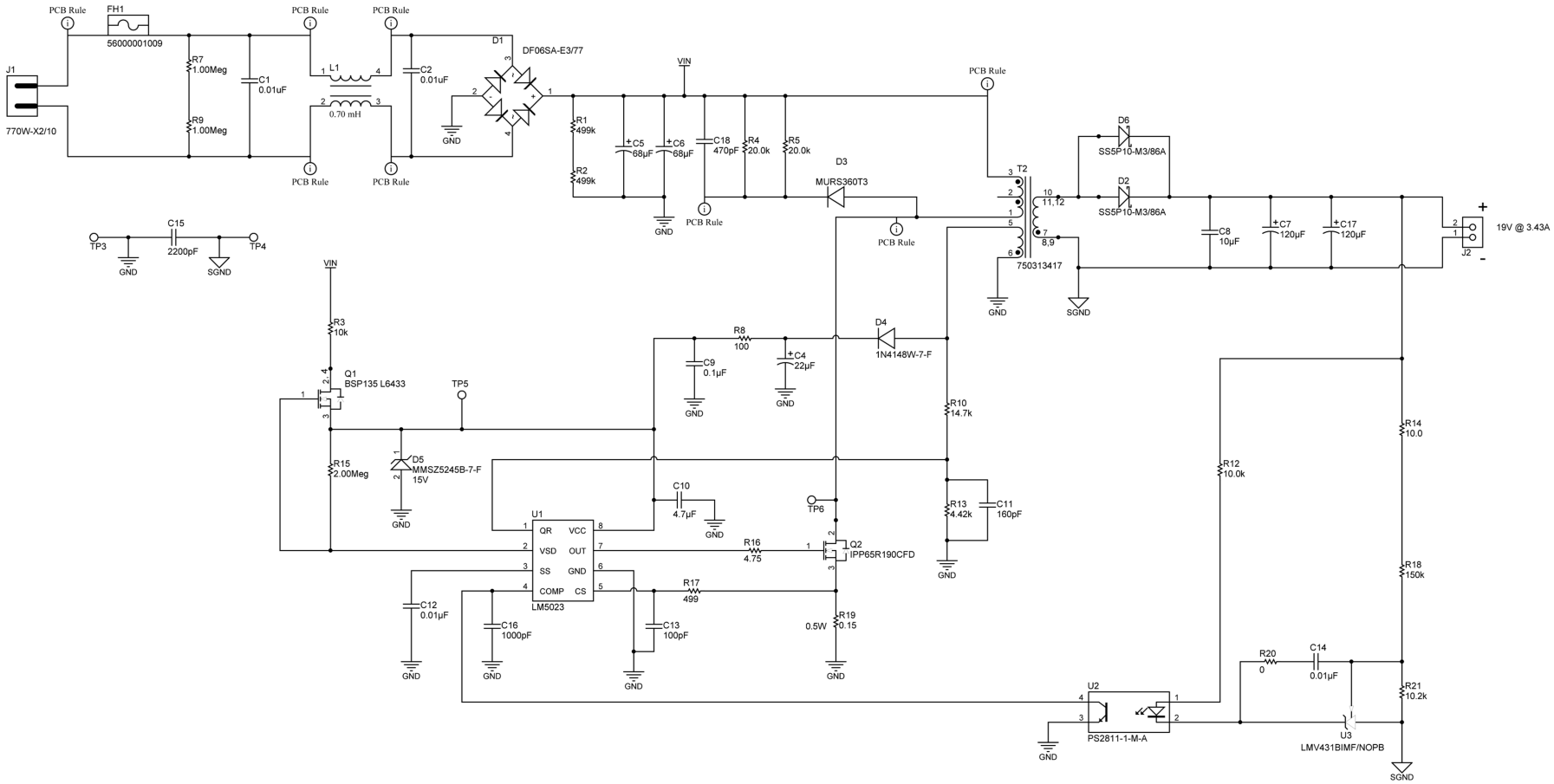
EVALUATION BOARD SCHEMATIC



REVISION HISTORY

Changes from Revision C (August, 2013) to Revision D **Page**

- Added LM5023 Pin Configuration 5
- Changed FUNCTIONAL BLOCK DIAGRAM. 6
- Added VCC < VCC(on) the current consumption. 9
- Changed IQR equation from R_{OFFSET} to R1. 19
- Changed Current Feed Forward resistor value from 1 kΩ to 6.6 kΩ. 21

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5023MM-2/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SK9B
LM5023MM-2/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SK9B
LM5023MMX-2/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SK9B
LM5023MMX-2/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SK9B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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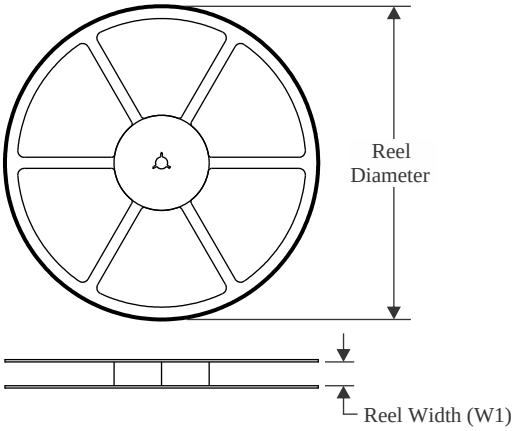
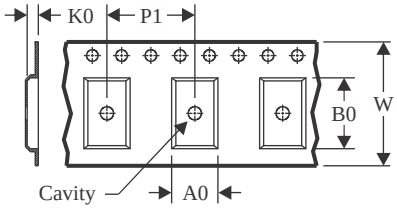
TAPE AND REEL INFORMATION

REEL DIMENSIONS

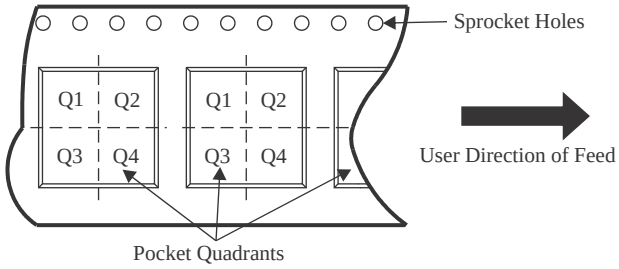


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

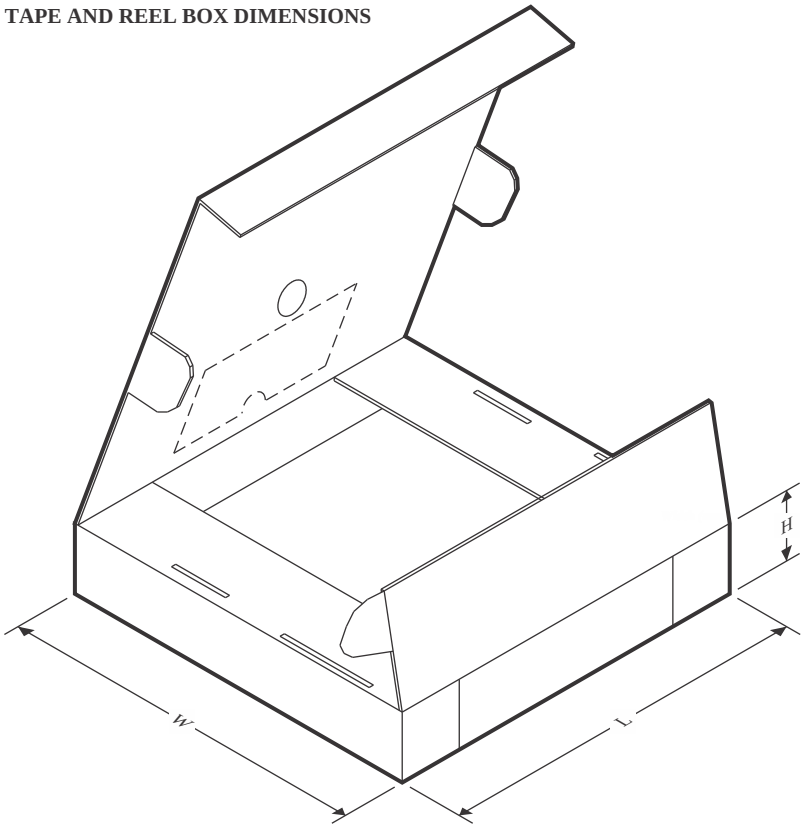
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5023MM-2/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5023MMX-2/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

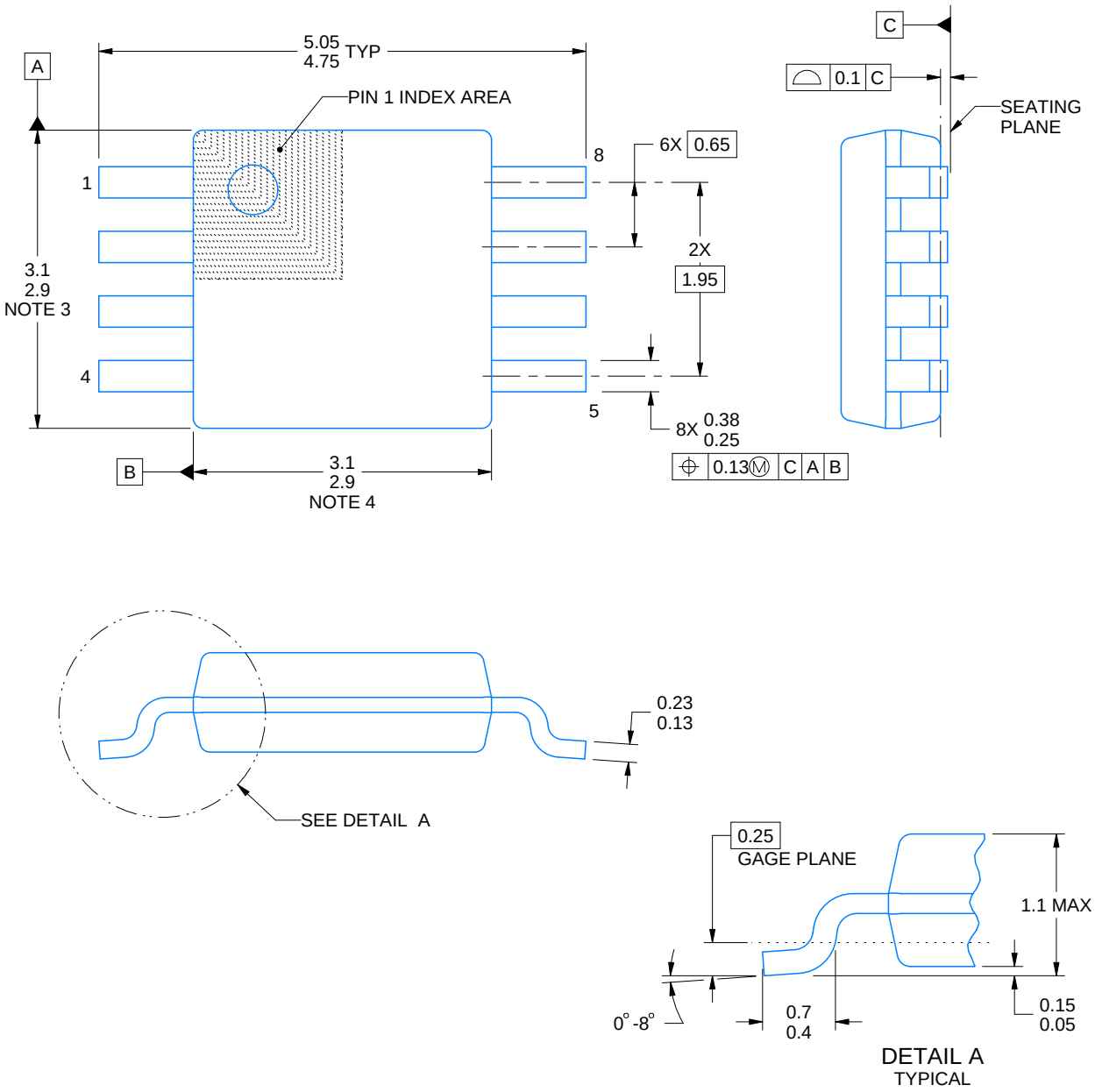
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5023MM-2/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM5023MMX-2/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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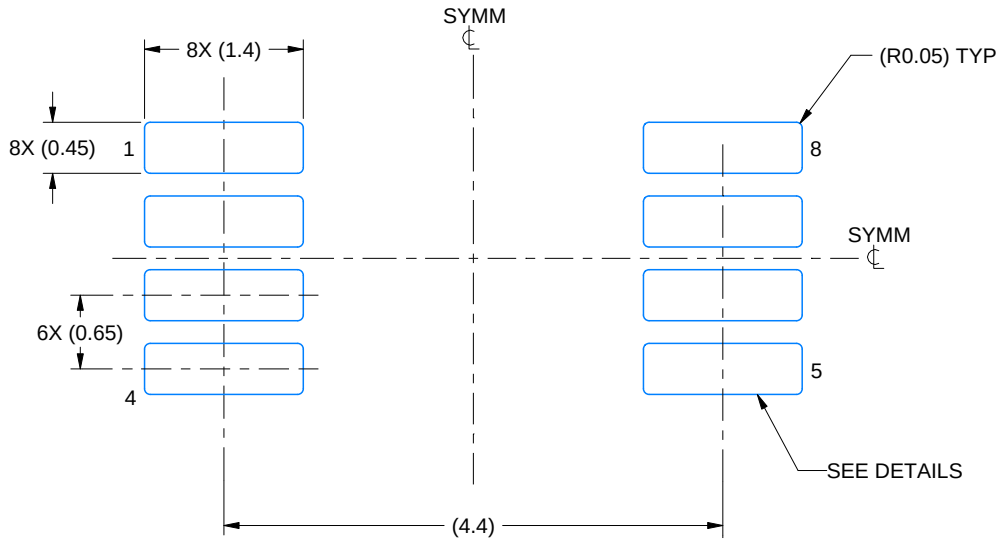
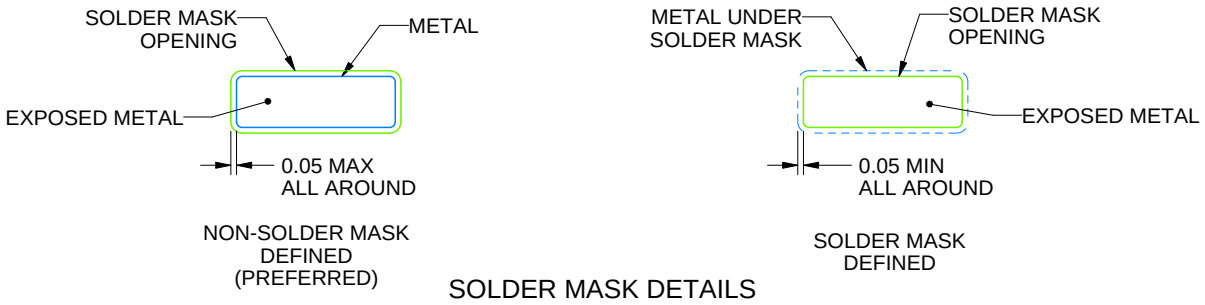
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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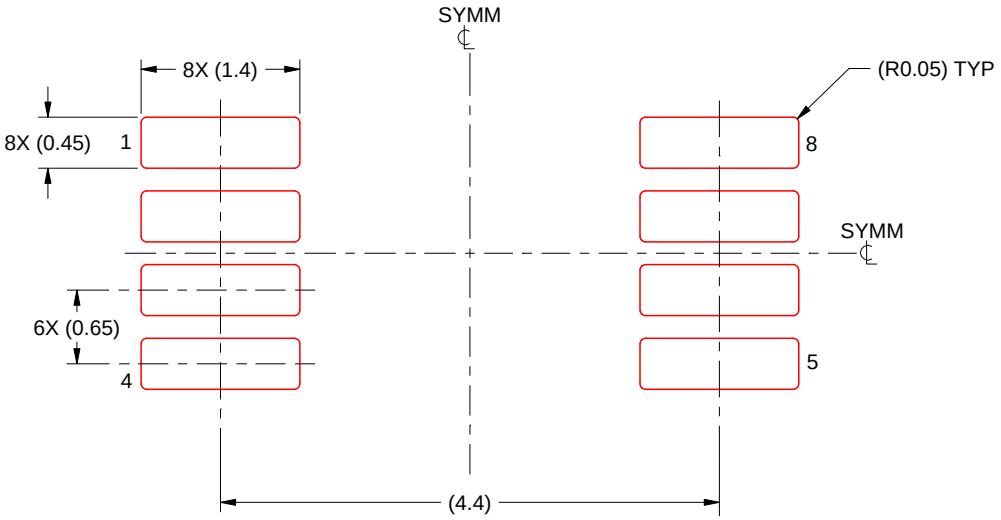
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月