LM5015 High Voltage Monolithic Two-Switch Forward DC-DC Regulator

Check for Samples: LM5015

FEATURES

- **Dual Integrated 75V N-Channel MOSFETs**
- **Ultra-Wide Input Voltage Range: 4.25V to 75V**
- **Integrated High Voltage Bias Regulator**
- **Adjustable Output Voltage**
- **1.5% Feedback Reference Accuracy**
- **Current Mode Control with Selectable Compensation**
- **Wide Bandwidth Error Amplifier**
- **Integrated Current Sensing and Limiting**
- **50% Maximum Duty Cycle Limit**
- **Single Resistor Oscillator Programming**
- **Oscillator Synchronization Capability**
- **Programmable Soft-Start**
- **Enable / Under-Voltage Lockout (UVLO) Pin**
- **Thermal Shutdown**

PACKAGE

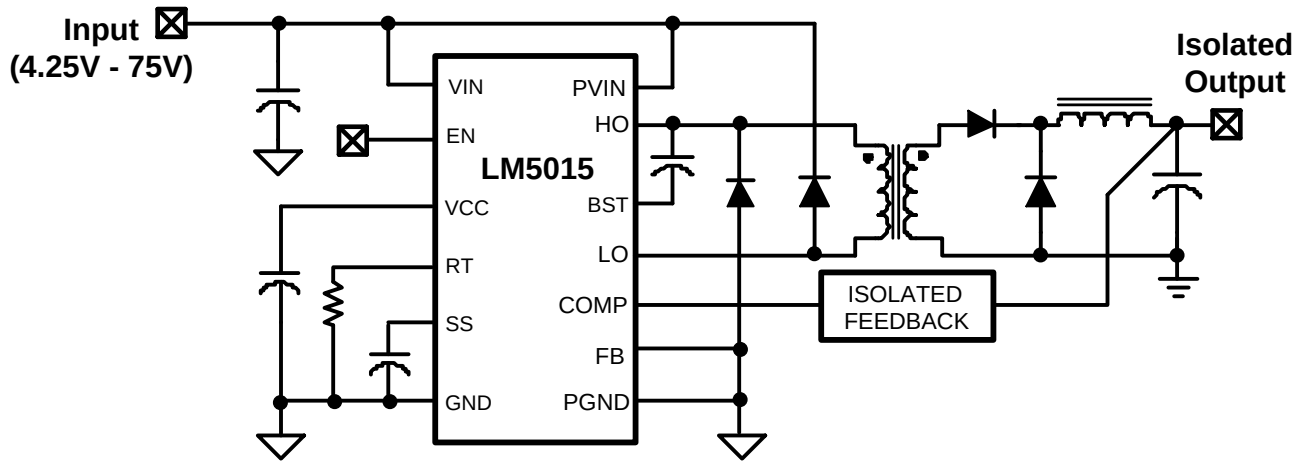
- **HTSSOP-14EP (Exposed Pad)**

DESCRIPTION

The LM5015 high voltage switch mode regulator features all the functions necessary to implement efficient high voltage Two-Switch Forward and Two-Switch Flyback regulators, using a minimum of external components. This easy to use regulator integrates high side and low side 75 Volt N-Channel MOSFETs with a minimum 1 Amp peak current limit. The voltage across the MOSFETs employed in the two-switch topology is clamped to the input voltage, allowing the input voltage range to approach the rating of the MOSFETs. The regulator control method is based on current mode control providing inherent ease of loop compensation and line feed-forward for superior rejection of input transients.

The operating frequency is set with a single resistor and is programmable up to 750 kHz. The oscillator can also be synchronized to an external clock. Additional protection features include cycle-by-cycle current limiting, thermal shutdown, under-voltage lockout and remote shutdown capability. The device is available in the HTSSOP-14EP package featuring an exposed die attach pad to enhance thermal dissipation.

Typical Application Schematic



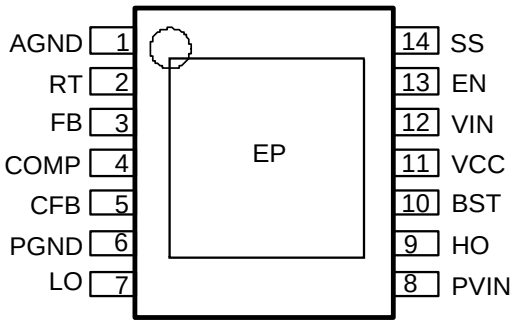
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Connection Diagram



HTSSOP-14 EP Package
Top View

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	AGND	Analog ground	Internal reference for the regulator control functions. The AGND pin and the PGND pin should be connected directly to minimize switching noise and prevent erratic operation.
2	RT	Oscillator frequency programming and optional synchronization input	The internal oscillator is set with a resistor between this pin and the AGND pin. The recommended switching frequency range is 25KHz to 750 kHz. The RT pin can accept synchronization pulses from an external clock. A 100 pF capacitor is recommended for coupling the synchronizing clock to the RT pin.
3	FB	Feedback input of the internal error amplifier, for non-isolated applications	This pin is connected to the inverting input of the internal error amplifier. The 1.26V reference is internally connected to the non-inverting input of the error amplifier. In isolated application using an external error amplifier, this pin should be connected to the AGND pin.
4	COMP	Control input for the PWM comparator	Internally connected to the open drain output of the internal error amplifier. COMP pull-up is provided by an internal 5 kΩ resistor which may be used to bias an opto-coupler transistor in isolated applications.
5	CFB	Current feedback pin	Feedback in put for high bandwidth isolated applications. An NPN current mirror couples the external opto-coupler current to the PWM comparator while maintaining a relatively constant opto-coupler voltage.
6	PGND	Power ground	Internally connected to the current sense resistor in the source of the low side MOSFET switch.
7	LO	Low side switch drain	The drain terminal of the internal low side power MOSFET.
8	PVIN	Input supply pin for high side switch	Internally connected to the drain of the high side power MOSFET.
9	HO	High side switch source	The source terminal of the high side power MOSFET.
10	BST	High side bootstrap bias	An external capacitor is required between the BST and the HO pins. A minimum capacitor value of 0.022 µF is recommended. The capacitor is charged from VCC via an internal diode during the power MOSFET off-time.
11	VCC	Bias regulator output, or input for external bias supply	VCC tracks VIN up to 6.9V. At higher VIN voltages, VCC is regulated to 6.9 Volts. A 0.47µF or greater ceramic decoupling capacitor is required on the VCC pin. An external bias voltage between 7V and 14V applied to the VCC pin will disable the internal VCC regulator, reduce internal power dissipation, and improve the converter efficiency.
12	VIN	Analog input voltage pin	Power supply Input for the switching regulator control blocks.
13	EN	Enable / Under-Voltage Lock-Out / Shutdown input	An external voltage divider can be used to set the input under-voltage lockout threshold. If the EN pin is left unconnected, a 6 µA pull-up current source pulls the EN pin high to enable the regulator.
14	SS	Soft-start	An internal 11 µA current source charges an external capacitor connected to the SS pin to soft-start the switching regulator by gradually raising the COMP pin voltage.
NA	EP	Exposed Pad	Exposed metal pad on the underside of the package. It is recommended to connect this pad to the PGND and AGND pins, and also to the PC board ground plane in order to improve heat dissipation.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

V_{IN} to AGND	76V
BST to AGND	90V
PVIN to HO, LO, PGND	76V
HO to PGND (Steady State)	-3V to 76V
LO to PGND (Steady State)	-0.3V to 76V
BST to VCC	76V
BST to HO	14V
V_{CC}, EN to AGND	14V
COMP, FB, RT, SS to AGND	-0.3V to 7V
PGND to AGND	-0.3V to +0.3V
CFB Sink Current	10 mA
Maximum Junction Temperature	150°C
Storage Temperature	−65°C to + 150°C
ESD Rating	
Human Body Model (3)	2 kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test Method is per JESD-22-A114.

Operating Ratings

V_{IN}	4.25V to 75V
Operation Junction Temperature	−40°C to + 125°C

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Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of −40°C to + 125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{VIN} = 48V, R_{RT} = 31.6 kΩ unless otherwise stated. See (1).

Symbol	Parameters	Conditions	Min	Typ	Max	Units
STARTUP REGULATOR						
$V_{VCC-REG}$	VCC Regulator Output		**6.35**	6.85	**7.25**	V
	VCC Current Limit	V_{VCC} = 6V	**20**	25		mA
	VCC UVLO Threshold	VCC increasing, VIN = VCC, EN=open	**3.45**	3.75	**4.05**	V
	VCC UVLO Hysteresis	VIN = VCC, EN = open		0.15		V
	Bias Current (IIN)	V_{FB} = 1.5V		3.1	**4.5**	mA
I_Q	Shutdown Current (IIN)	V_{EN} = 0V		110	**170**	µA
EN THRESHOLDS						
	EN Shutdown Threshold	V_{EN} increasing	**0.25**	0.45	**0.65**	V
	EN Shutdown Hysteresis			0.1		V
	EN Standby Threshold	V_{EN} increasing	**1.19**	1.26	**1.3**	V
	EN Standby Hysteresis			0.1		V
	EN Current Source			6		µA
MOSFET CHARACTERSTICS						
	Low side MOSFET RDS(ON) plus Current Sense Resistance	I_D = 0.6A		0.49	**0.93**	Ω
	MOSFET Leakage Current	V_{LO} = 75V		0.05	**5**	µA
	High side MOSFET RDS(ON)	I_D = 0.6A		0.45	**0.90**	Ω
	MOSFET Leakage Current	V_{PVIN}= 75V, V_{HO} = PGND		0.05	**5**	µA
	Total Gate Charge including both Low and High side MOSFETs	V_{VCC} = 8V		9		nC
	Pre-charge Switch ON Voltage including series blocking diode	I_D = 1 mA		0.82		V
CURRENT LIMIT						
I_{LIM}	Cycle by Cycle Current Limit		**1**	1.2	**1.4**	A
	Cycle by Cycle Current Limit Delay			130		ns
OSCILLATOR						
F_{SW1}	Frequency1	R_{RT} = 31.6k	**180**	200	**220**	kHz
F_{SW2}	Frequency2	R_{RT} = 15.4k	**365**	405	**445**	kHz
$V_{RT-SYNC}$	SYNC Threshold	V_{RT} Increasing	**3.2**			V
	SYNC Pulse Width Minimum	V_{RT} > $V_{RT-SYNC}$ + 0.5V		15		ns
PWM COMPARATOR						
	Maximum Duty Cycle			49		%
	Min On-time	V_{COMP} > $V_{COMP-OS}$		140		ns
	Min On-time	V_{COMP} < $V_{COMP-OS}$		0		ns
$V_{COMP-OS}$	COMP to PWM Comparator Offset		**0.9**	1.3	**1.55**	V
ERROR AMPLIFIER						
V_{FB-REF}	Feedback Reference Voltage	Internal reference, V_{FB} = V_{COMP}	**1.236**	1.26	**1.274**	V
	FB Bias Current			10		nA
	DC Gain			72		dB
	COMP Sink Current	V_{COMP} = 250mV	**2**			mA
	COMP Short Circuit Current	V_{FB} = 0, V_{COMP} = 0	**0.9**	1.2	**1.5**	mA
	COMP Open Circuit Voltage	V_{FB} = 0	**4.5**	5.15	**5.95**	V

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

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Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of −40°C to + 125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{VIN} = 48V, R_{RT} = 31.6 kΩ unless otherwise stated. See (1).

Symbol	Parameters	Conditions	Min	Typ	Max	Units
	COMP to SW Delay			50		ns
	Unity Gain Bandwidth			4		MHz
SOFT START						
	Soft-start Current Source		**8**	11	**14**	µA
	Soft-start to COMP Offset		**0.3**	0.5	**0.7**	V
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			165		°C
	Thermal Shutdown Hysteresis			25		°C
THERMAL RESISTANCE						
θ_{JC}	Junction to Case			6.6		°C/W
θ_{JA}	Junction to Ambient			40		°C/W

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Typical Performance Characteristics

Demo-board Efficiency vs I_{OUT} and V_{IN}

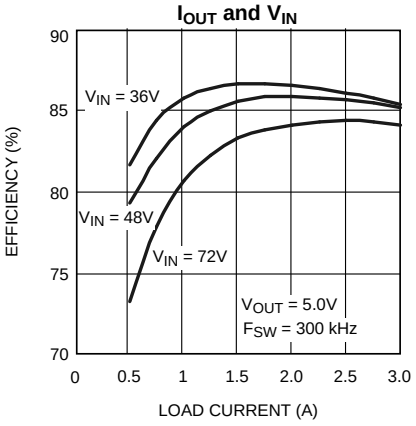


Figure 1.

VFB vs Temperature

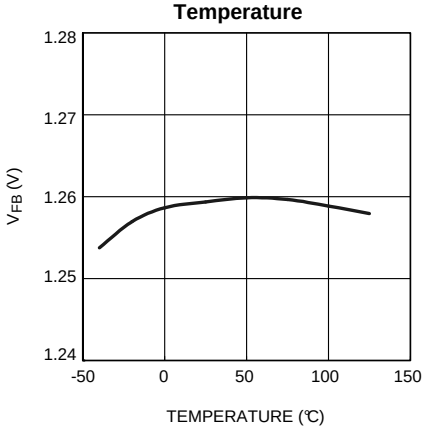


Figure 2.

IQ (non-switching) vs VIN

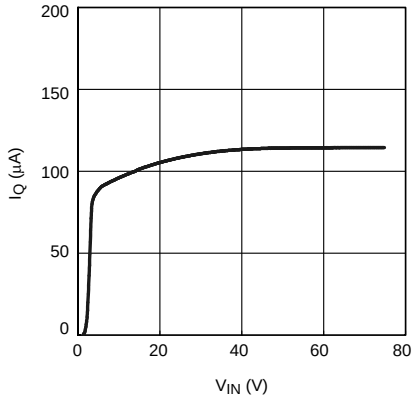


Figure 3.

VCC vs VIN

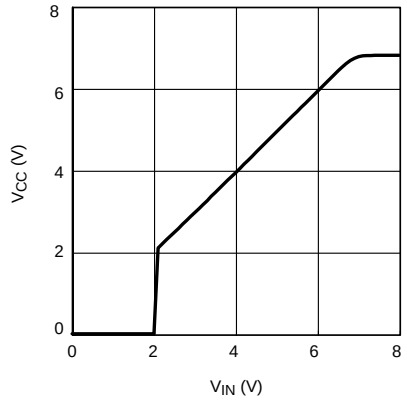


Figure 4.

RDS(ON) vs VCC vs Temperature

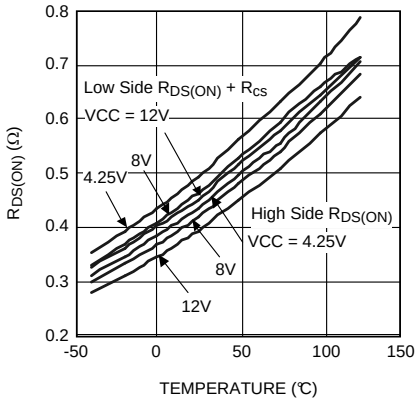


Figure 5.

IEN vs VIN vs Temperature

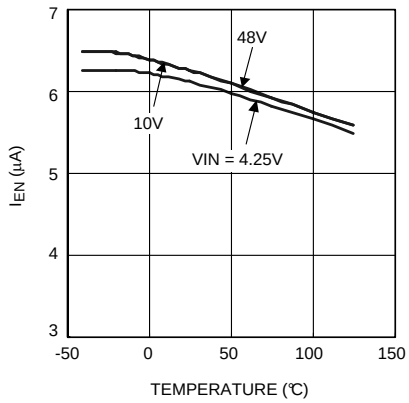


Figure 6.

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Typical Performance Characteristics (continued)

ILIM vs VCC

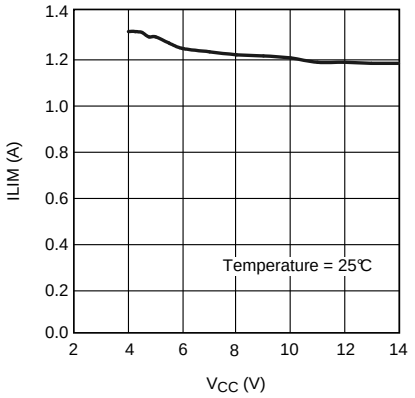


Figure 7.

ILIM vs VCC vs Temperature

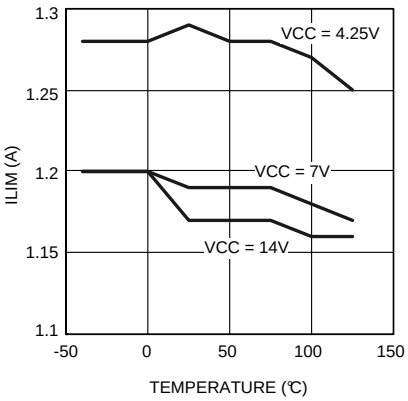


Figure 8.

Fsw vs R_{RT}

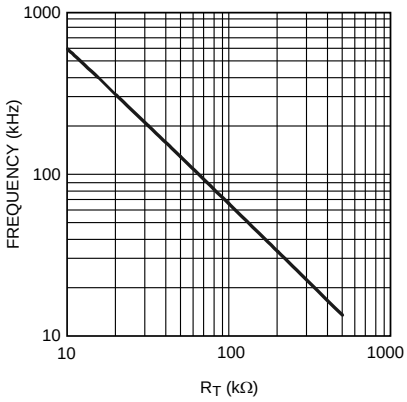


Figure 9.

Fsw vs Temperature

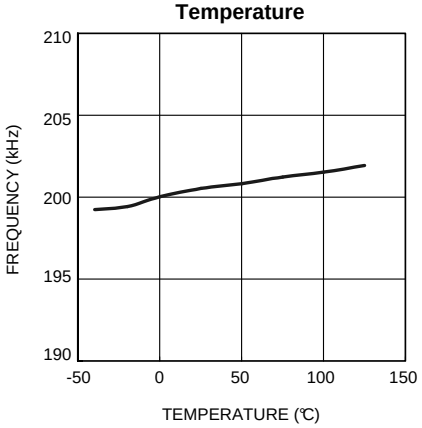


Figure 10.

Fsw vs VCC

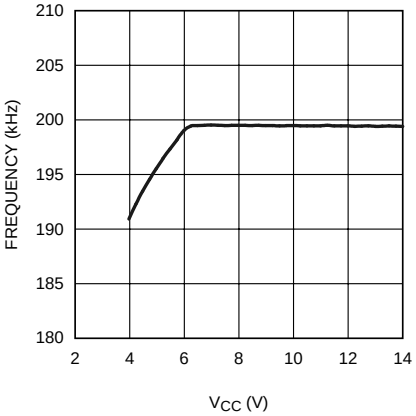


Figure 11.

Error Amplifier Gain/Phase

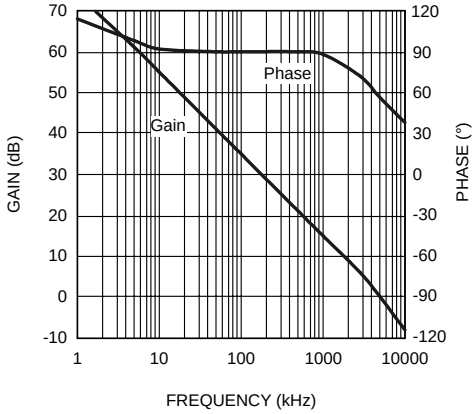


Figure 12.

Block Diagram

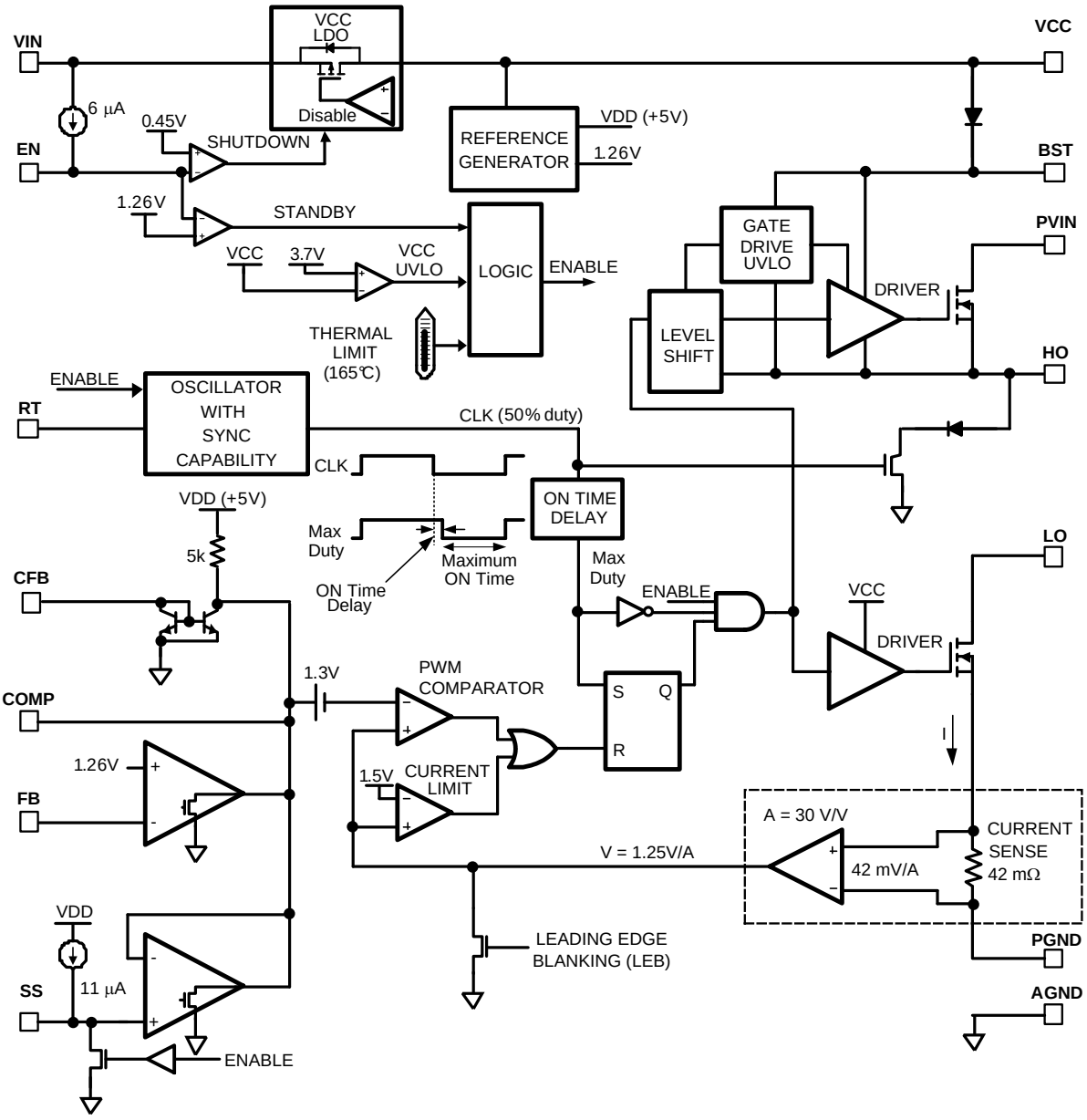


Figure 13.

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FUNCTIONAL DESCRIPTION

The LM5015 high voltage switching regulator features all the functions necessary to implement an efficient power converter using a Two-Switch Forward or Two-Switch Flyback topology. The voltage across the MOSFETs employed in the two-switch topology is clamped to the input voltage, allowing the input voltage range to approach the rating of the MOSFETs. The regulator control method is based upon current mode control providing cycle-by-cycle current limit, inherent input voltage feed-forward and simple feedback loop compensation.

Referring to Figure 13, the operating principle of the LM5015 regulator is as follows:

At the beginning of each switching cycle, the oscillator sets the driver logic and turns on both the high and low side power MOSFETs to conduct current through the inductor or power transformer. The peak current in the MOSFET is controlled by the voltage at the COMP pin. The COMP voltage, which is determined by the feedback circuit, is compared with the sensed current signal of the internal low side power MOSFET. When the current signal exceeds the COMP voltage, the PWM comparator resets the driver logic, turning off both power MOSFETs. At the end of the switching cycle the driver logic is set again by the oscillator to initiate the next switching period.

The LM5015 also contains dedicated circuitry to protect the IC from abnormal operating conditions. Cycle-by-cycle current limiting prevents the power MOSFET current from exceeding 1 Amp. Thermal Shutdown circuitry holds the driver logic in reset when the die temperature reaches 165°C, and returns to normal operation when the die temperature drops by approximately 25°C. The EN pin can be used as an input voltage under-voltage lockout (UVLO) during start-up to prevent operation with less than the minimum desired input voltage.

Bias Input (VIN) and Power Input (PVIN)

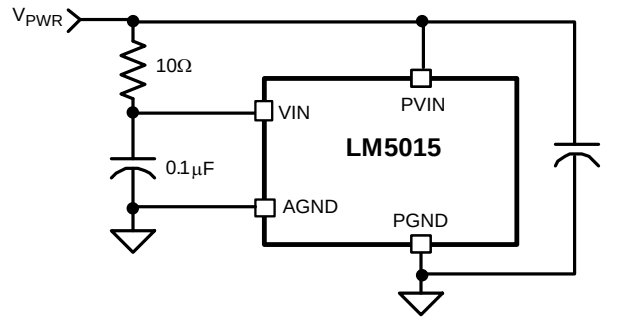
The LM5015 provides two separate input power pins, VIN and PVIN, allowing for flexible decoupling options. The VIN pin provides power to the low drop-out VCC bias regulator which powers all internal control blocks. The PVIN connects directly to the high side MOSFET drain.

If used with a single input source, the recommended configuration is shown in Figure 2a. Separate input pins allow the bias input (VIN) to be de-coupled from the main power input as shown. It is possible to directly connect the VIN and PVIN pins for applications with localized de-coupling capacitors.

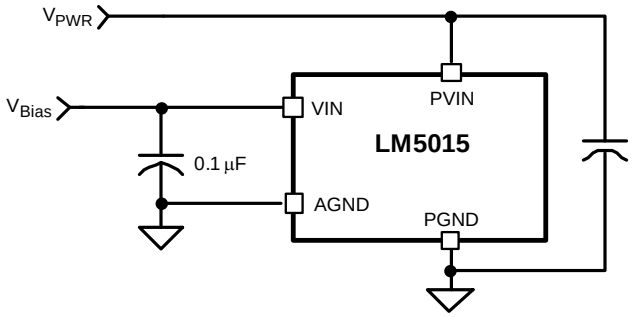
For applications where a lower voltage auxiliary source is available, the configuration shown in Figure 2b can be used. Powering the VIN pin with a relatively low voltage auxiliary source reduces the IC power dissipation and increases the conversion efficiency, especially when the main power source for PVIN is relatively large. The VIN and PVIN pins are independent and can be separately biased at any voltages within the 4.25V to 75V recommended operating range.

In high voltage applications extra care should be taken to ensure that the VIN and PVIN pins do not exceed the Absolute Maximum Voltage Ratings of 76V. Voltage ringing on the input line during line transients that exceeds the Absolute Maximum Ratings can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and AGND pins, and to the PVIN to PGND pins, are essential.

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(a) Analog Input Powered from the Main Power



(b) Analog Input Powered from a Separate Bias Source

Figure 14. Analog and Power Input Ports

The PVIN and PGND pins are internally connected to the high and low side power MOSFETs, respectively. When designing the PC board, the input filter capacitor should connect directly to these pins with short connection traces.

The VIN operating range is 4.25V to 75V. The current drawn into the VIN pin depends primarily on the gate charge of the internal power MOSFETs, the switching frequency, and any external load on the VCC pin. It is recommended that a small filter shown in Figure 14 be used for the VIN input to suppress transients which may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM5015.

High Voltage VCC Regulator

The LM5015 VCC Low Drop Out (LDO) regulator allows the LM5015 to operate at the lowest possible input voltage. When power is applied to the VIN pin and the EN pin voltage is greater than 0.45V, the VCC regulator is enabled, supplying current into the external capacitor connected to the VCC pin. When the VIN voltage is between 4.25V and 6.9V, the VCC voltage is approximately equal to the VIN voltage. When the voltage on the VIN pin exceeds 6.9V, the VCC pin voltage is regulated at 6.9V. The total input operating range of the VCC LDO regulator is 4.25V to 75V.

The output of the VCC regulator is current limited to 20mA. During power-up, the VCC regulator supplies current into the required decoupling capacitor (0.47 µF or greater ceramic capacitor) at the VCC pin. When the voltage at the VCC pin exceeds the VCC UVLO threshold of 3.75V and the EN pin is greater than 1.26V the PWM controller is enabled and switching begins. The controller remains enabled until VCC falls below 3.60V or the EN pin falls below 1.16V.

An auxiliary supply voltage can be applied to the VCC pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 6.9V, the internal regulator will essentially shutoff, and internal power dissipation will be decreased by the VIN-VCC voltage difference times the operating current. The externally applied VCC voltage should not exceed 14V. The VCC regulator series pass MOSFET includes a body diode (see Figure 13) between VCC and VIN that should not be forward biased in normal operation. Therefore, the auxiliary VCC voltage should never exceed the VIN voltage.

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High Side Bootstrap Bias

The high side bootstrap bias provides power to drive the high side power MOSFET. An external capacitor is required between the BST and the HO pins. A minimum capacitor value of 0.022 µF is recommended. The capacitor is charged from VCC via an internal diode during each power MOSFET off-time.

Oscillator

A single external resistor connected between RT and AGND pins sets the LM5015 oscillator frequency. To set a desired oscillator frequency (F_{SW}), the necessary value for the R_T resistor can be calculated from the following equation:

$$R_T = 32.4\ k\Omega \times \frac{200\ kHz}{F_{SW}\ (kHz)} - 0.8\ k\Omega \quad (1)$$

The tolerance of the external resistor and the frequency tolerance indicated in the Electrical Characteristics table must be taken into account when determining the total variation of the switching frequency.

External Synchronization

The LM5015 can be synchronized to the rising edge of an external clock. Because the oscillator uses a divide-by-two circuit, the switching frequency F_{SW} in the above equation is actually half the native oscillator frequency. Therefore, in order to synchronize, the external clock must have a frequency higher than twice the free running F_{SW} set by the R_T resistor. The clock signal should be coupled through a 100 pF capacitor into the RT pin. A peak voltage level greater than 3.2V at the RT pin is required for detection of the sync pulse. The DC voltage across the R_T resistor is internally regulated at 1.5 volts. The negative portion of the AC voltage of the synchronizing clock is clamped to 1.5V by an amplifier inside the LM5015 with approximately 100Ω output impedance. Therefore, the AC pulse superimposed on the R_T resistor must have positive pulse amplitude of 1.7V or greater to successfully synchronize the oscillator. The sync pulse width measured at the RT pin should have a duration greater than 15 ns and less than 5% of the switching period. The R_T resistor is always required, whether the oscillator is free running or externally synchronized. The R_T resistor should be located very close to the device and connected directly to the RT and AGND pins of the LM5015.

Enable / Standby

The LM5015 contains a dual level Enable circuit. When the EN pin voltage is below 0.45V, the IC is in a low current shutdown mode with the VCC LDO disabled. When the EN pin voltage is raised above the 0.45V shutdown threshold but below the 1.26V standby threshold, the VCC LDO regulator is enabled, while the remainder of the IC is disabled. When the EN pin voltage is raised above the 1.26V standby threshold, all functions are enabled and normal operation begins. An internal 6 µA current source pulls up the EN pin to activate the IC when the EN pin is left disconnected.

An external set-point resistor divider from VIN to AGND can be used to determine the minimum operating input voltage of the regulator. The divider must be designed such that the EN pin exceeds the 1.26V standby threshold when VIN is in the desired operating range. The internal 6 µA current source should be included when determining the resistor values. The shutdown and standby thresholds have 100 mV hysteresis to prevent noise from toggling between modes. The EN pin is internally protected by a 6V Zener diode through a 1 kΩ resistor. The enabling voltage may exceed the Zener voltage, however the Zener current should be limited to less than 4 mA.

Error Amplifier and PWM Comparator

An internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference. The output of the error amplifier is connected to the COMP pin allowing the user to add loop compensation, typically a Type II network, as illustrated in Figure 15. This network creates a pole at the origin that rolls off the high DC gain of the amplifier, which is necessary to accurately regulate the output voltage. A zero provides phase boost near the open loop unity gain frequency, and a high frequency pole attenuates switching noise. The PWM comparator compares the current sense signal from the current sense amplifier to the error amplifier output voltage at the COMP pin.

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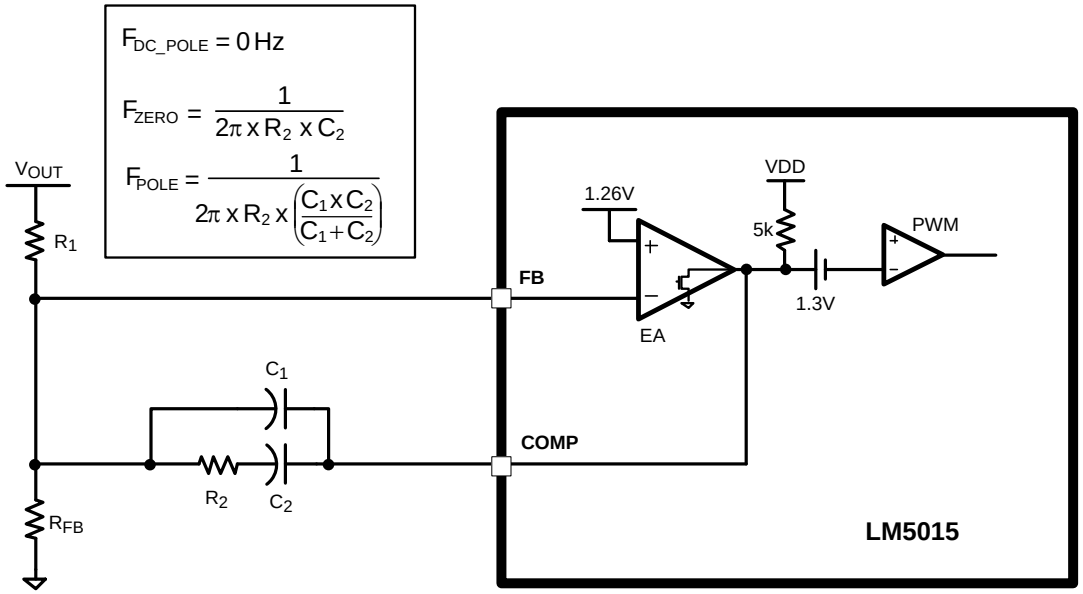


Figure 15. Type II Compensator

When isolation between primary and secondary circuits is required, the Error Amplifier is usually disabled by connecting the FB pin to AGND. This allows the COMP pin to be driven directly by the collector of an opto-coupler. In isolated designs the error amplifier is located on the secondary circuit and drives the opto-coupler LED. The compensation network is connected to the secondary side error amplifier. An example of an isolated regulator with an opto-coupler is shown in Figure 25.

Current Sense Amplifier

The LM5015 employs peak current mode control which also provides a cycle-by-cycle over current protection feature. An internal 42 milli-Ohm current sense resistor measures the current in the low side power MOSFET source. The sense resistor voltage is amplified 30 times to provide a 1.25V/A signal into the current limit comparator. Current limiting is initiated if the internal current limit comparator input exceeds the 1.5V threshold, corresponding to 1.2A. When the current limit comparator is triggered, the HO and LO output pins immediately switches to the high impedance state.

The current sense signal provides the PWM comparator with a control signal that reaches 1.5V when the MOSFET current is 1.2A. To prevent erratic operation at low duty cycle, a leading edge blanking circuit attenuates the current sense signal for 100 ns when the power MOSFET is turned on. When the MOSFET is initially turned on, current spikes from the power MOSFET drain-source and gate-source capacitances flow through the current sense resistor. These transient currents normally cease within 50 ns with proper selection of rectifier diodes and proper PC board layout.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When the 165°C junction temperature threshold is reached, the regulator is forced into a low power standby state, disabling all functions except the VCC regulator. Thermal hysteresis allows the IC to cool down by 25°C before it is re-enabled.

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Power MOSFETs

The LM5015 switching regulator includes two N-Channel MOSFETs each with 450 mΩ nominal on-resistance. The drain of the high side MOSFET is the PVIN pin, and the source the HO pin. The drain of the low side MOSFET is the LO pin, and the source is internally connected to the PGND pin via the 42 mΩ internal current sense resistor. The on-resistance of the LM5015 MOSFETs varies with temperature as shown in the Typical Performance Characteristics graph. The typical gate charge for each MOSFETs is 4.5 nC which is supplied from the VCC and BST pins, respectively, when the MOSFETs are turned on.

The maximum duty cycle of the power MOSFETs is limited less than 50%. This is achieved by an oscillator divide-by-two circuit with an additional 50 ns of forced off-time introduced between the CLK and RS Flip-Flop. Consequently, the maximum duty cycle is limited by the following equation:

$$Duty_{Max_Limit} = (0.5 - 50\ ns \times F_{SW}) \times 100\% \quad (2)$$

where

- F_{SW} is the switching frequency in Hertz (Hz)

The purpose of limiting the maximum duty cycle less than 50% is to ensure successful reset of the power transformer in the Two-Switch Forward converter topology. See Application Information below for more detail.

Application Information

The following information is intended to provide guidelines for the power supply designer using the LM5015.

TWO-SWITCH FORWARD TOPOLOGY

Two-Switch Forward converter, like the conventional Single-Switch Forward converter, is derived from the Buck converter topology. The main difference between a Forward converter and a Buck is that a power transformer is introduced in the forward converter. The transformer realizes the input-output isolation, and the turns ratio provides a means to optimize the duty cycle for the particular input and output voltage requirements of the application.

The Two-Switch Forward converter employs two power MOSFET switches instead of the one switch of the Single-Switch Forward converter. However the two-switch approach offers two major advantages over its single-switch counterpart:

1. The voltage across the power MOSFET switches in a Two-Switch Forward converter is clamped to the input voltage, allowing the input voltage range to approach the rating of the MOSFETs. Whereas, the maximum operating voltage of a Single-Switch Forward converter is typically limited to half the MOSFET voltage rating.
2. The power transformer of a Two-Switch Forward converter is simpler, and hence costs less, than that of a Single-Switch Forward converter, because the Two-Switch converter transformer eliminates the tertiary reset winding that is normally required in the Single-Switch converter.

Figure 16 illustrates the Two-Switch Forward converter topology. The power circuit consists of an input capacitor C_{IN}, two MOSFET switches Q_H and Q_L, two clamp diodes D_H and D_L, a power transformer T_1, two rectifier diodes D_1 and D_2, an output inductor L_O, and an output capacitor C_o. Since the LM5015 integrates both Q_H and Q_L, a low cost Two-Switch Forward converter can be realized without a need for discrete power MOSFETs. With a slightly higher cost, the two rectifier diodes D_1 and D_2 on the secondary side of the power transformer can be replaced with synchronous rectifier MOSFETs to improve efficiency in applications with relatively low output voltage.

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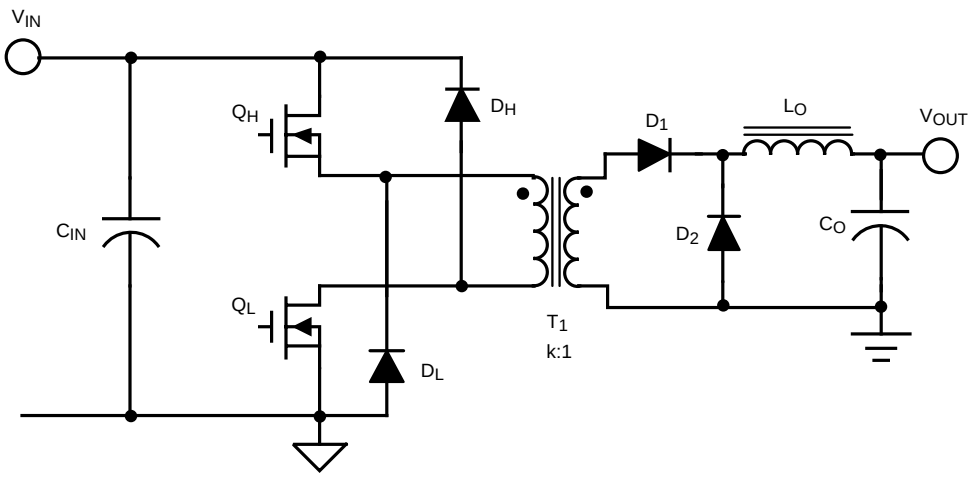


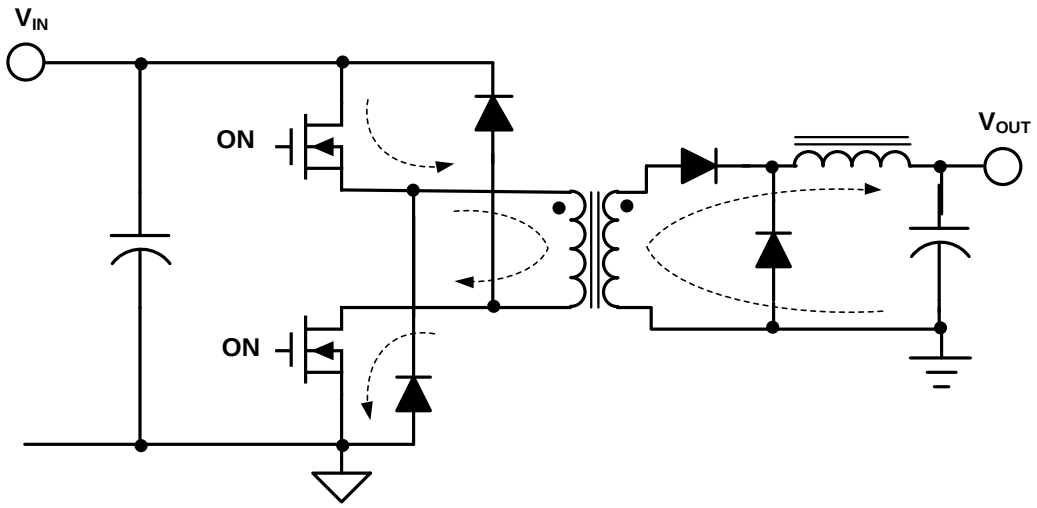
Figure 16. Two-Switch Forward Converter Topology

Figure 17 shows the two operating modes of the Two-Switch Forward converter. During operation, the two MOSFETS are turned ON and OFF simultaneously. The output voltage is regulated by modulating the duty cycle of the MOSFETs. The relationship between the input voltage V_{IN}, output voltage V_{OUT}, duty cycle D, rectifier diode forward drop V_F, and transformer turns ratio k is defined by the following equation.

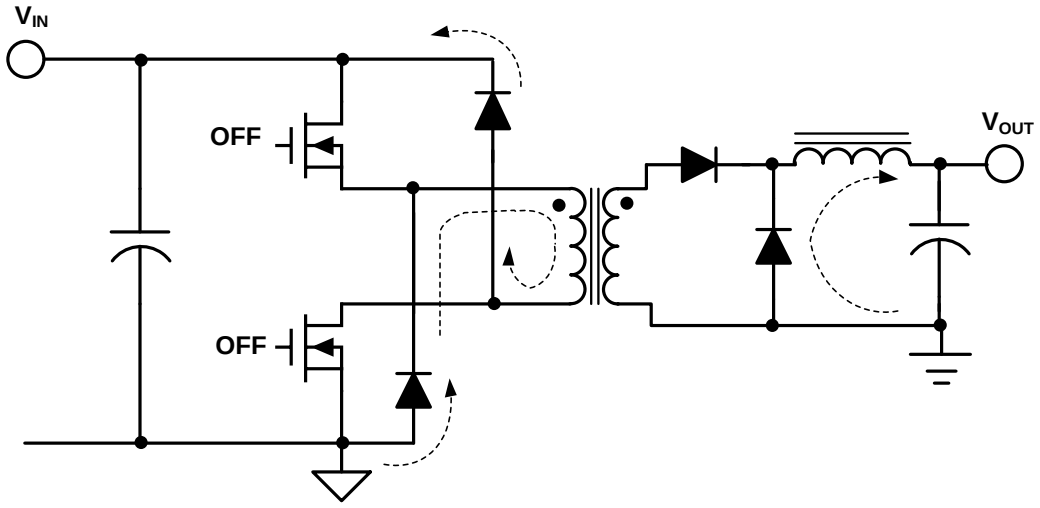
$$D = \frac{k \times (V_{OUT} + V_F)}{V_{IN}} \quad (3)$$

When the MOSFETS are turned ON, as shown in Figure 5a, the input voltage is applied to the power transformer primary. The power transformer is magnetized by the application of the input voltage, and power flows to the secondary side circuit via transformer coupling. When the MOSFETS are turned OFF, as shown in Figure 5b, the power flow to the primary is cut off. The residual magnetizing inductance of the power transformer reverses the voltage across the primary winding and forces the two clamp diodes D_H and D_L to conduct. This effectively clamps the MOSFETs voltage to the input voltage, and applies the input voltage in reversed polarity to the power transformer primary winding to demagnetize and reset the transformer.

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(a) Current Paths when MOSFETs are Turned On



(b) Current Paths when MOSFETs are Turned Off

Figure 17. Operating Modes of Two-Switch Forward Converter

Note that the power transformer primary receives the voltage of the nearly equal magnitude but opposite polarities during the ON and OFF period of the power MOSFETs. In order to ensure the volt-second balance between the magnetizing and demagnetizing intervals, the LM5015 limits the maximum duty cycle less than 50%. Therefore, an LM5015 Two-Switch Forward regulator always achieves a complete reset of the power transformer during each switching cycle.

The LM5015 can also be used to implement a Two-Switch Flyback regulator (Figure 26). The voltage across the MOSFETs employed in the Two-Switch Flyback converter is also clamped to the input voltage, allowing the input voltage range to approach the rating of the MOSFETs. Generally the Flyback converter is simpler and costs less than the Forward converter. However, the Flyback converter will have higher ripple current and voltages, and the conversion efficiency is typically lower.

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EN / UVLO VOLTAGE DIVIDER SELECTION

Two dedicated comparators connected to the EN pin are used to implement input under-voltage lockout and a shutdown condition. When the EN pin voltage is below 0.45V, the controller is in a low current shutdown mode where the VIN current is reduced to 110 µA. For an EN pin voltage greater than 0.45V but less than 1.26V the controller is in standby mode, with all internal circuits operational, but with the power MOSFETs disabled. Once the EN pin voltage is greater than 1.26V, the controller is fully enabled and the HO and LO outputs commence switching. Two external resistors can be used to program the minimum operational voltage for the power converter as shown in Figure 18. When the EN pin voltage falls below the 1.26V threshold, an internal 100 mV threshold hysteresis prevents noise from toggling the state. Therefore, the voltage at the EN pin must be reduced to 1.16V to transition to the standby state. Resistance values for R1 and R2 can be determined from the following equations, where V_{PWR} is the desired turn-on voltage and $I_{DIVIDER}$ is the user-defined current through R1 and R2.

$$R1 = \frac{V_{PWR} - 1.26V}{I_{DIVIDER}}$$

$$R2 = \frac{1.26V}{I_{DIVIDER} + 6\ \mu A} \quad (4)$$

For example, if the LM5015 is to be enabled when V_{PWR} reaches 16V, $I_{DIVIDER}$ could be chosen as 500 µA which would set R1 to 29.4 kΩ and R2 to 2.49 kΩ. If the voltage at the EN pin can exceed 6V, then the current into the 6V protection Zener must be limited below 4 mA by the external resistors. Be sure to check both the power and voltage rating for the selected R1 resistor (some 0603 resistors are rated as low as 50V maximum operating voltage).

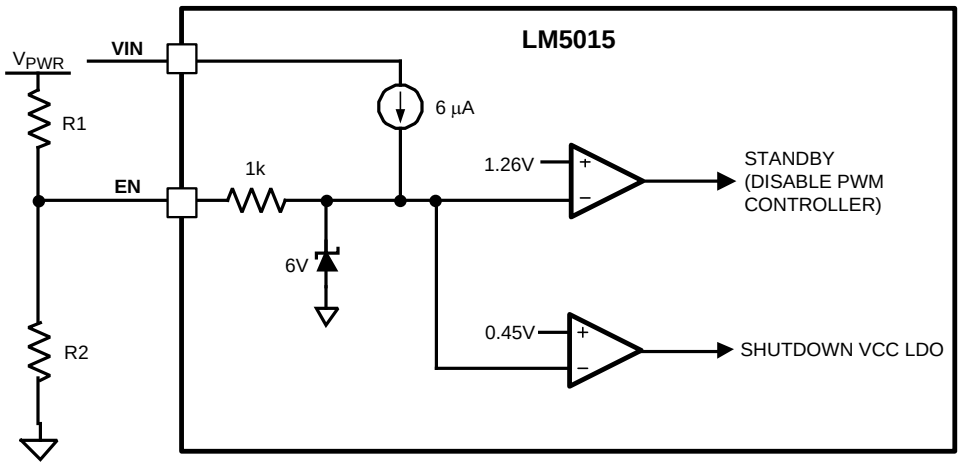


Figure 18. Basic EN (UVLO) Configuration

A remote enable function can be accomplished with open drain device(s) connected to the EN pin as shown in Figure 19. A MOSFET or an NPN transistor connected to the EN pin will force the regulator into the low power 'off' state. Adding a PN diode in the drain (or collector) provides the offset to achieve the standby state. The advantage of standby is that the VCC LDO is not disabled and external circuitry powered by VCC remains functional.

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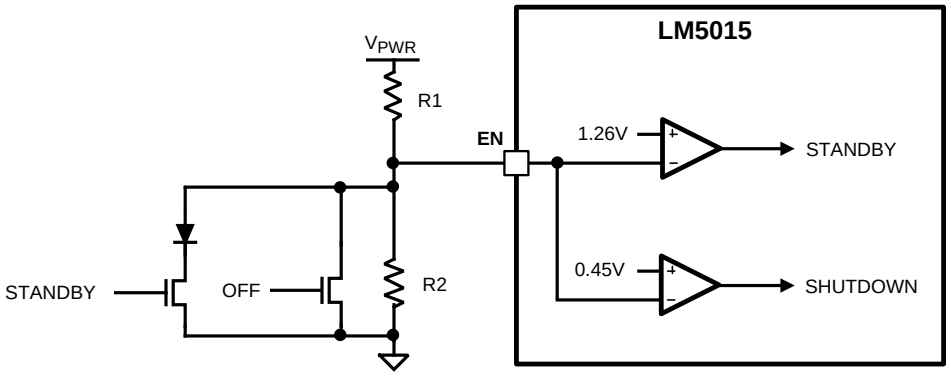


Figure 19. Remote Standby and Disable Control

SOFT-START

Soft-start is implemented with an external capacitor C_{SS} connected to the SS pin as shown in Figure 20. The SS discharge MOSFET conducts during Shutdown and Standby modes. When the SS pin is low, the COMP voltage is held below the PWM offset voltage (1.3V) by the SS buffer amplifier, thus inhibiting PWM pulses. When the EN pin exceeds the 1.26V standby threshold, the ENABLE signal will turn-off the SS discharge MOSFET and allow the internal 11 µA current source to charge the SS capacitor. The COMP voltage will follow the SS voltage under the control of the open-drain SS buffer amplifier. The C_{SS} capacitor will cause the COMP voltage to gradually increase, until the output voltage achieves regulation, and the error amplifier assumes control of the COMP and the PWM duty cycle. The C_{SS} capacitor continues charging by the internal 11 µA current source, preventing the SS voltage from interfering with the normal error amplifier function. During shutdown, the SS discharge MOSFET conducts to discharge the C_{SS} capacitor.

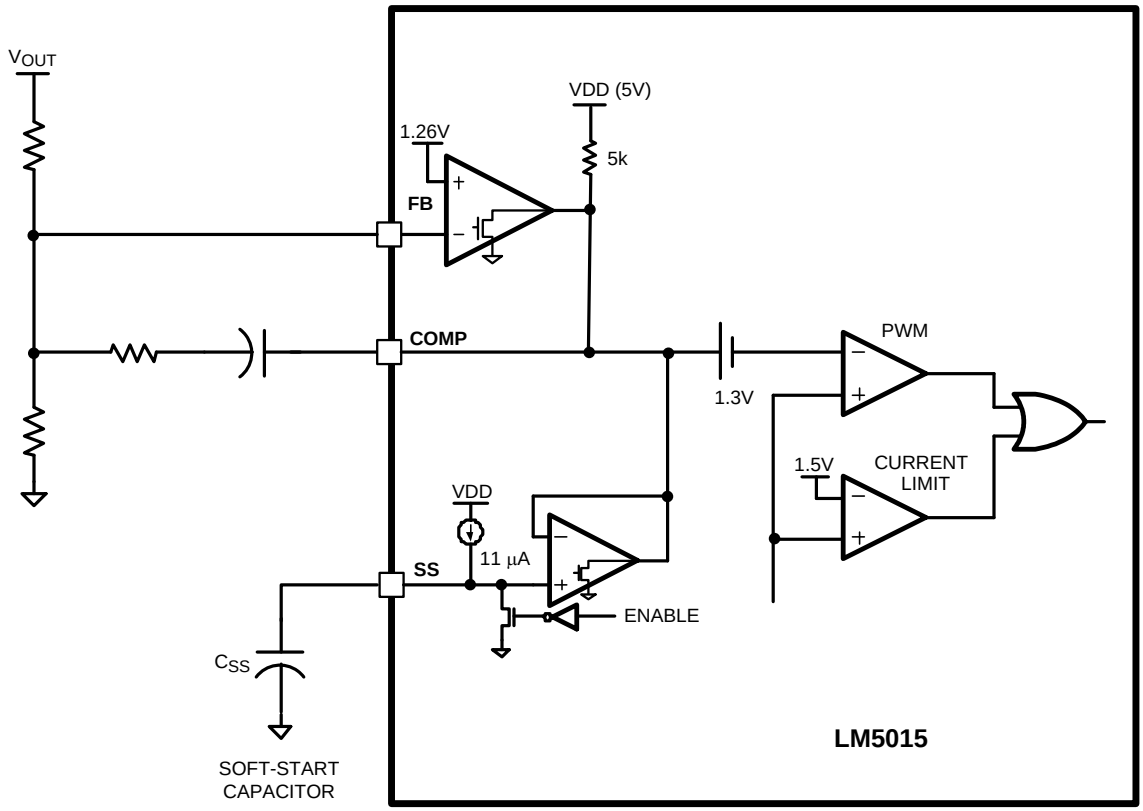


Figure 20. Soft-Start

CONVENTIONAL ISOLATED OUTPUT FEEDBACK DESIGNS

When isolation between the primary and secondary circuits is required, the internal error amplifier is usually disabled by connecting the FB pin to AGND, and an external error amplifier is employed on the secondary side of the isolation boundary. An opto-coupler is normally used to send the feedback signal across the isolation boundary, as shown in Figure 21. The LM5015 provides built-in pull-up for the collector of the opto-coupler at the COMP pin through a 5 kΩ internal resistor. Similar compensation network used in Figure 15 is applicable to the external, secondary-side error amplifier. The LM431A shown in Figure 21 provides both the voltage reference and error amplifier required to regulate the isolated output voltage.

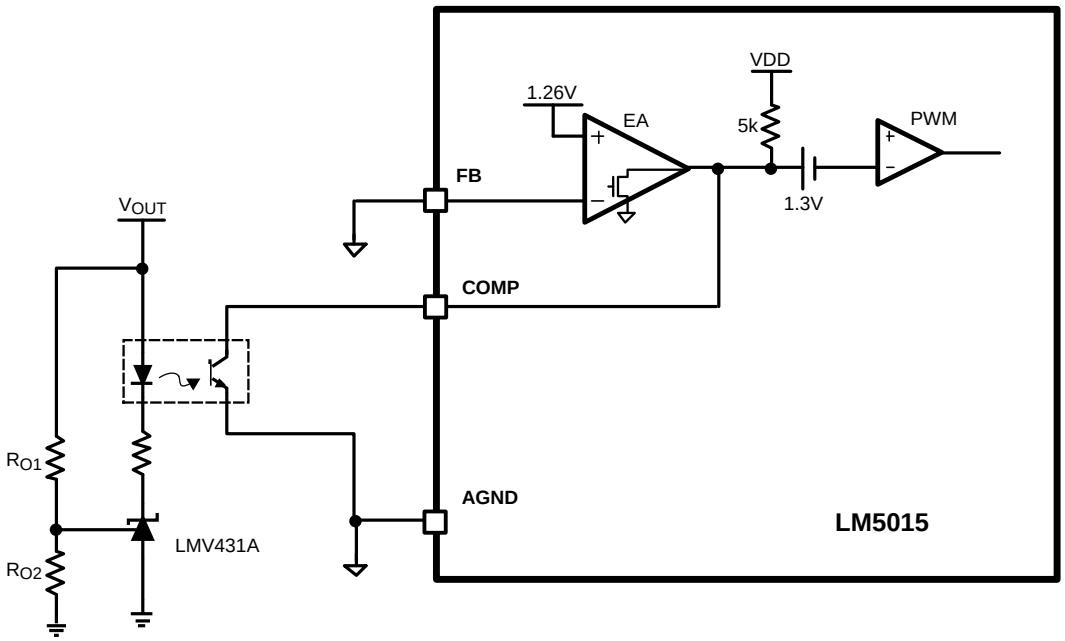


Figure 21. Conventional Isolated Feedback

HIGH BANDWIDTH ISOLATED FEEDBACK DESIGN USING THE CFB PIN

The LM5015 also includes a current mirror circuit for optional high bandwidth feedback loop design. As shown in Figure 22, the emitter of the opto-coupler transistor can be connected to the CFB pin, and the collector connected to VCC through an external 1 kΩ resistor. The 1 kΩ resistor to VCC is used to protect the CFB pin by limiting the opto-coupler current to less than 10 mA. The 1 kΩ resistor from the opto-coupler collector to ground is introduced to protect the opto-coupler from excess voltage by limiting its V_{CE} to less than 50% of Vcc max. When the output voltage is below regulation, no current flows into the CFB pin and the PWM of the LM5015 operates at maximum duty cycle.

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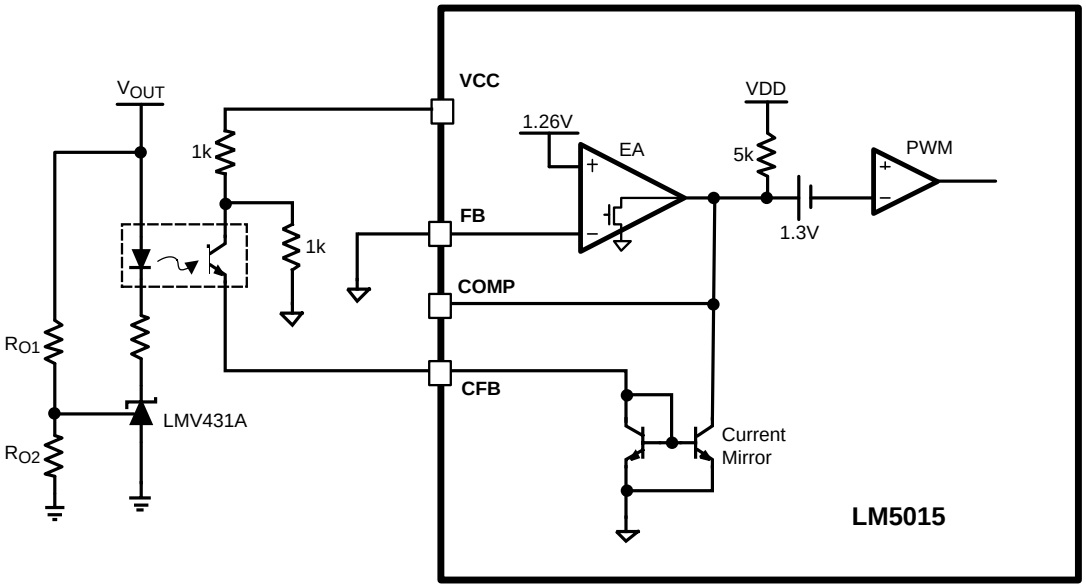


Figure 22. High bandwidth Isolated Feedback Using CFB Pin

The two external pull-up and pull-down resistors are effectively connected in parallel for ac signal, yielding a collector resistance on the opto-coupler of 0.5 kΩ. This resistance is 10 times smaller than the internal pull up resistor and the pole associated with the collector-base capacitance of the opto-coupler transistor is pushed out to a decade higher frequency. Moving the opto-coupler pole to a higher frequency allows higher loop bandwidth capability than conventional isolated feedback designs (see Figure 21).

OUTPUT VOLTAGE

Output voltage is normally set with a resistor divider shown in Figure 23 . To set the regulator's output voltage to V_O, the two resistors must satisfy the following equation:

$$\frac{R_{O2}}{R_{O1}} = \frac{V_{REF}}{V_O - V_{REF}} \quad (5)$$

where

- V_{REF} is the reference voltage of the error amplifier, which is 1.26V for the LM5015's internal error amplifier

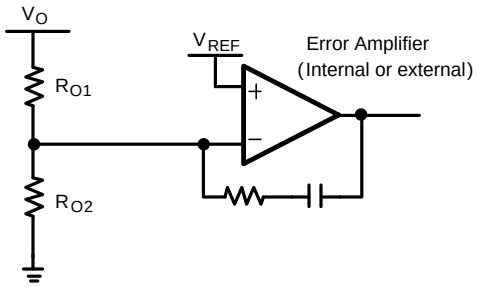


Figure 23. Output Voltage Setting

In isolated designs, the reference and error amplifier are located on the secondary side. To obtain a 5V output in an isolated feedback design using LMV431A (whose nominal V_{REF} is1.24V), the feedback divider resistors ratio specified by above equation is 0.330. Selecting 24.3 kΩ for R_{O1}, then R_{O2} should be 8.06 kΩ. In a similar non-isolated converter design using the internal error amplifier, the divider's resistors ratio is 0.337, therefore if 24.3 kΩ is selected for R_{O1}, then R_{O2} should be 8.20 kΩ.

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Multiple resistors in series or parallel combinations for either R_{O1}, or R_{O2}, or both, may be necessary to set a required output voltage. Note that the accuracy of the output voltage setting is determined by the tolerance of the divider resistors as well as the accuracy of V_{REF}. The accuracy of the LM5015 internal V_{REF} is 1.5%, and the most popular chip resistors have a tolerance of 1%, therefore the achievable output accuracy with the internal error amplifier and 1% resistors is about 2.5%. To achieve better output voltage accuracy, use an external voltage reference with higher precision and resistors of tighter tolerance, such as the 0.1%, resistors for R_{O1} and R_{O2}.

PRINTED CIRCUIT BOARD LAYOUT

The LM5015 Current Sense and PWM comparators are very fast and may respond to short duration noise pulses. The components at the HO, LO, COMP, EN, VCC and the RT pins should be as physically close as possible to the IC, thereby minimizing noise pickup on the PC board tracks. The HO and LO output pins of the LM5015 should have short, wide conductors to the power path inductors, transformers and capacitors in order to minimize parasitic inductance that reduces efficiency and increases conducted and radiated noise. Ceramic decoupling capacitors are recommended between the VIN pin to the AGND pin, between the PVIN pin and PGND pin, and between the VCC pin to the AGND pin. Use short, direct connections to avoid clock jitter due to ground voltage differentials. Small package surface mount X7R or X5R capacitors are preferred for high frequency performance and limited variation over temperature and applied voltage.

If an application using the LM5015 produces high junction temperatures during normal operation, multiple vias from the exposed metal pad on the underside of the IC package to a PC board ground plane will help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow will help reduce the junction temperature. If using forced air cooling, avoid placing the LM5015 in the airflow shadow of large components, such as input or output capacitors, inductors or transformers.

Application Examples

The following schematics present four examples dc-dc converters utilizing the LM5015 switching regulator IC:

1. Non-Isolated Two-Switch Forward for 48V input and 5V 2.5A output,
2. Isolated Two-Switch Forward for 48V input and 5V 2.5A output
3. Isolated Two-Switch Flyback converter for 48V input and 5V 2.5A output,
4. A 1:1 dc-dc transformer with the input/output operating range of 5V to 15V

48V NON-ISOLATED TWO-SWITCH FORWARD

The Non-Isolated Two-Switch Forward converter shown in Figure 24 utilizes the internal voltage reference for the regulation set-point. The output is +5V at 2.5A while the input voltage can vary from 36V to 72V. The switching frequency is 300 kHz. An auxiliary winding on transformer (T1) provides 10V to power the LM5015 when the output is in regulation. This disables the internal high voltage VCC LDO regulator and improves efficiency. The converter can be shut down by driving the EN input below 1.26V with an open-collector or open-drain transistor. An external synchronizing frequency can be applied to the SYNC input.

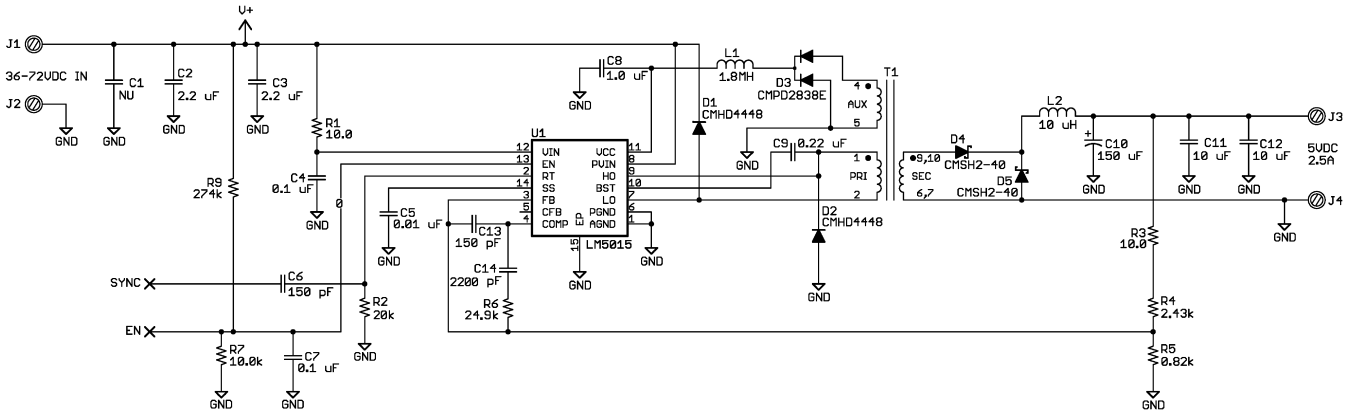


Figure 24. Non-Isolated Two-Switch Forward

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48V ISOLATED TWO-SWITCH FORWARD

The Isolated Two-Switch Forward converter shown in Figure 25 utilizes a 1.24V voltage reference (LMV431A) located on the isolated secondary side for the regulation set-point. The LM5015 internal error amplifier is disabled by grounding the FB pin. The LMV431A controls the current through the opto-coupler LED, which sets the COMP pin voltage. The output is +5V at 2.5A and the input voltage ranges from 36V to 72V. The switching frequency is 300 kHz. The functions of the EN and SYNC inputs are the same as in the previous example circuit.

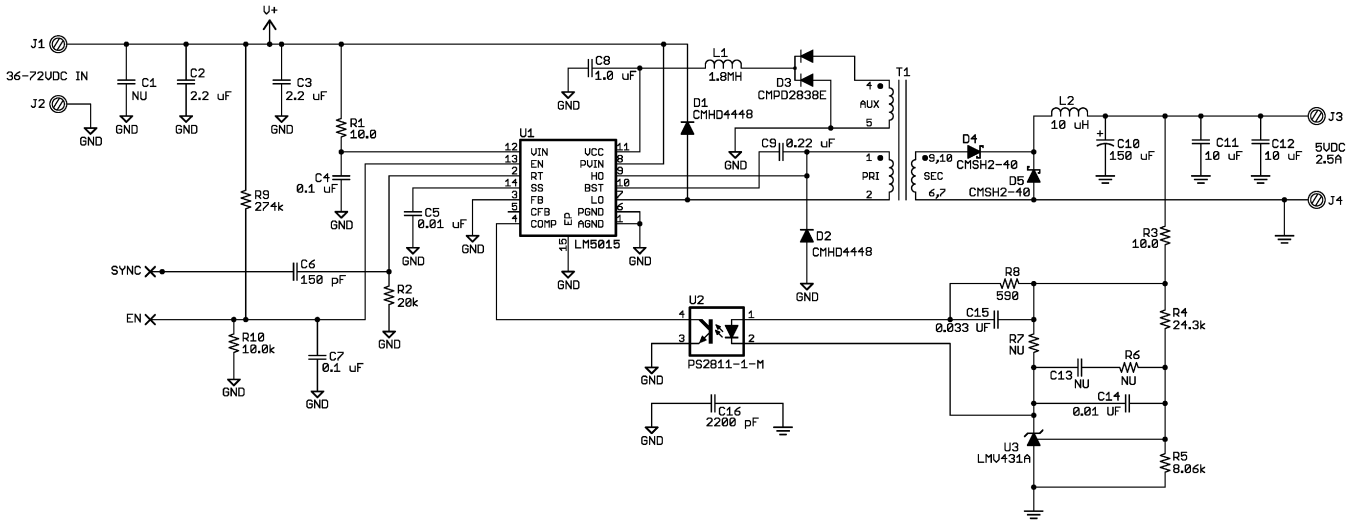


Figure 25. Isolated Two-Switch Forward

ISOLATED TWO-SWITCH FLYBACK

The Isolated Two-Switch Flyback converter shown in Figure 26 utilizes a 1.24V voltage reference (LMV431A) located on the isolated secondary side for the regulation set-point. The LM5015 internal error amplifier is disabled by grounding the FB pin. The LMV431A controls the current through the opto-coupler LED, which sets the COMP pin voltage. The output is +5V at 2.5A and the input voltage ranges from 36V to 72V. The switching frequency is 300 kHz. The Flyback converter is less complex than the previous Forward converter example in Figure 25. However, the Flyback converter produces higher input and output ripples of voltage and currents, and lower conversion efficiency by about 2%. The functions of the EN and SYNC inputs are the same as in the previous example circuits.

This circuit can be used with the LM5073 for a low cost isolated Power over Ethernet (PoE) Power Device (PD) application that does not require a discrete power MOSFET.

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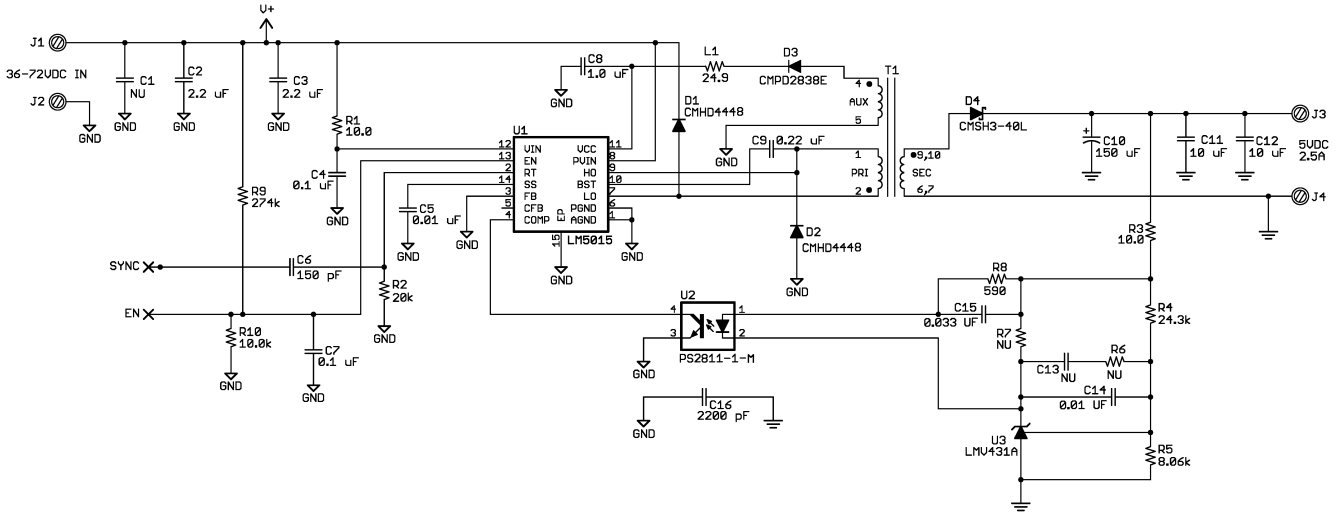


Figure 26. Isolated Two-Switch Flyback

DC-DC TRANSFORMER

The DC-DC transformer shown in Figure 27 provides a 1:1 input voltage to output voltage conversion with ground isolation. The circuit operates in open loop manner operating at the maximum duty cycle limit of the LM5015. The power transformer primary-secondary turns ratio is 1:2 (primary to secondary). Therefore, at the maximum duty cycle of 0.5, the output voltage will be approximately equal to the input voltage. A Zener diode Z1 is used at the output rail as a simple means to protect the output against over-voltage under light and no load conditions. The maximum load of this example circuit is 0.3A, and the operating voltage range is from 5V to 15V.

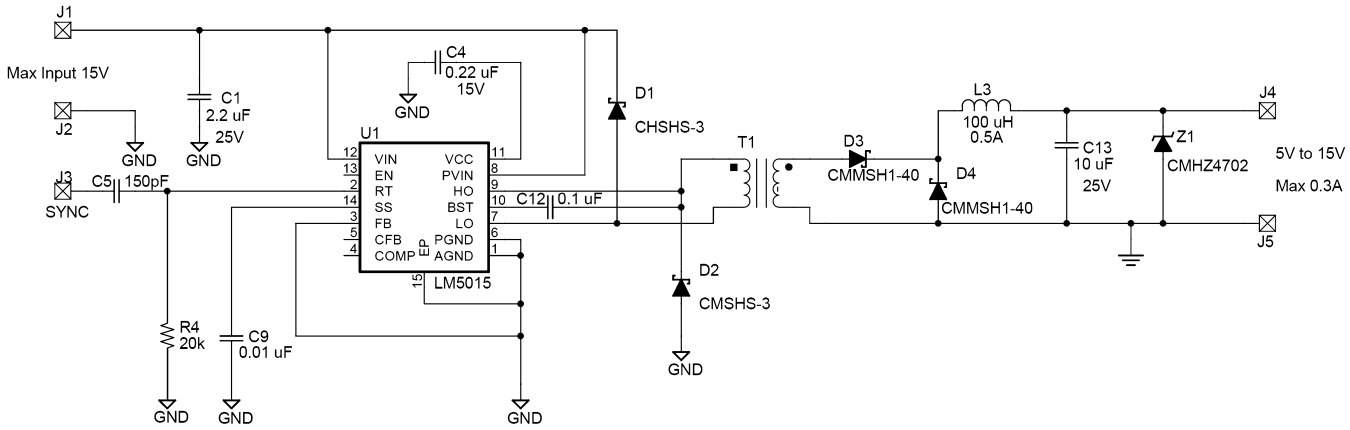


Figure 27. DC-DC Transformer

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REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	22

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5015MH/NOPB	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5015 MH
LM5015MH/NOPB.A	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5015 MH
LM5015MH/NOPB.B	Active	Production	HTSSOP (PWP) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5015 MH
LM5015MHE/NOPB	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5015 MH
LM5015MHE/NOPB.A	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5015 MH
LM5015MHE/NOPB.B	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5015 MH
LM5015MHX/NOPB	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5015 MH
LM5015MHX/NOPB.A	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5015 MH
LM5015MHX/NOPB.B	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5015 MH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

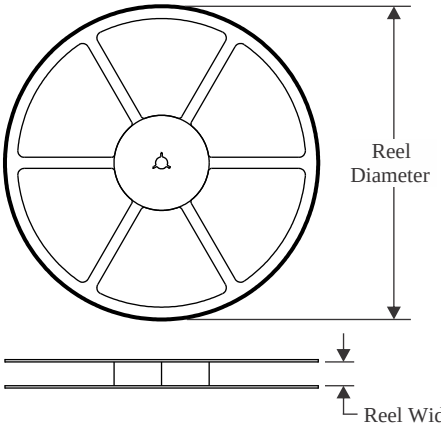
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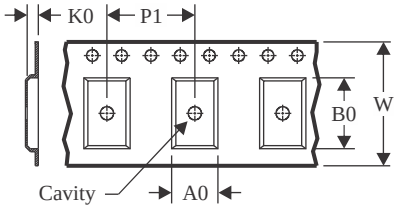
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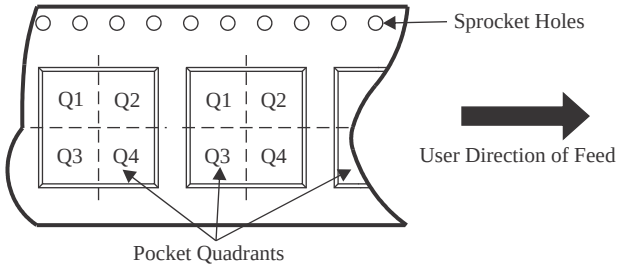


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

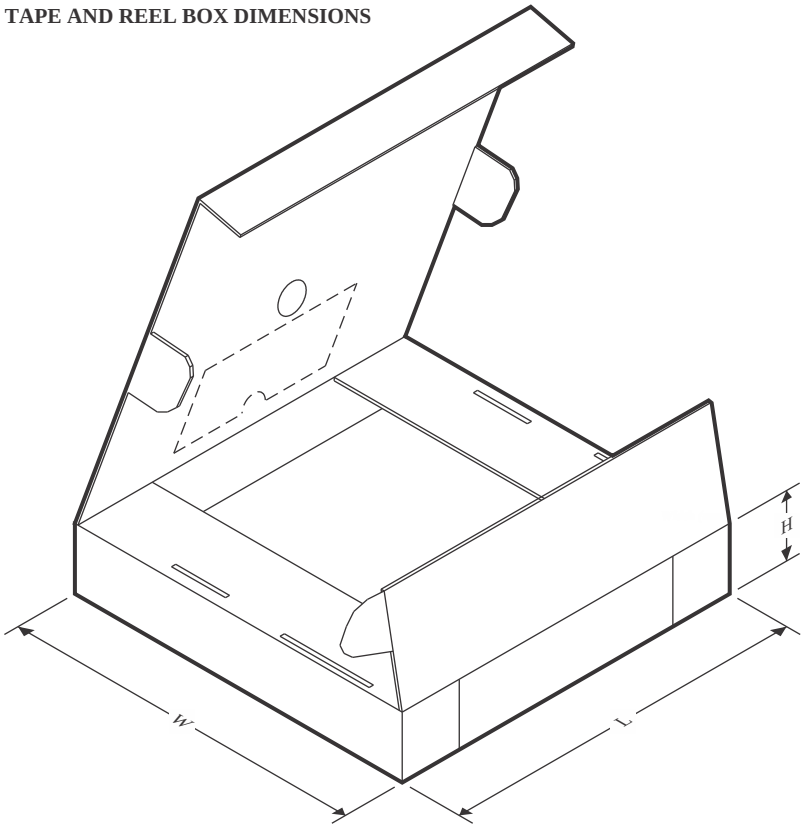
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5015MHE/NOPB	HTSSOP	PWP	14	250	177.8	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM5015MHX/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

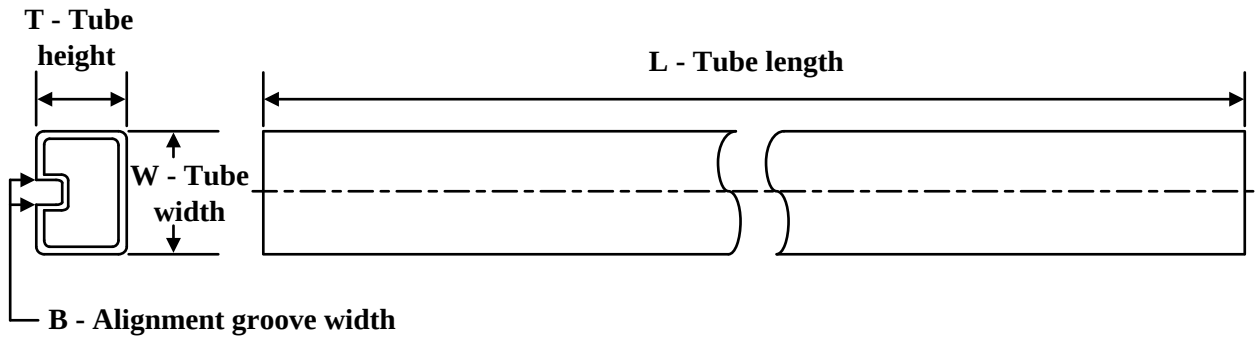
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

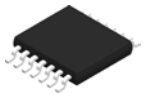
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5015MHE/NOPB	HTSSOP	PWP	14	250	208.0	191.0	35.0
LM5015MHX/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5015MH/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5015MH/NOPB.A	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM5015MH/NOPB.B	PWP	HTSSOP	14	94	495	8	2514.6	4.06

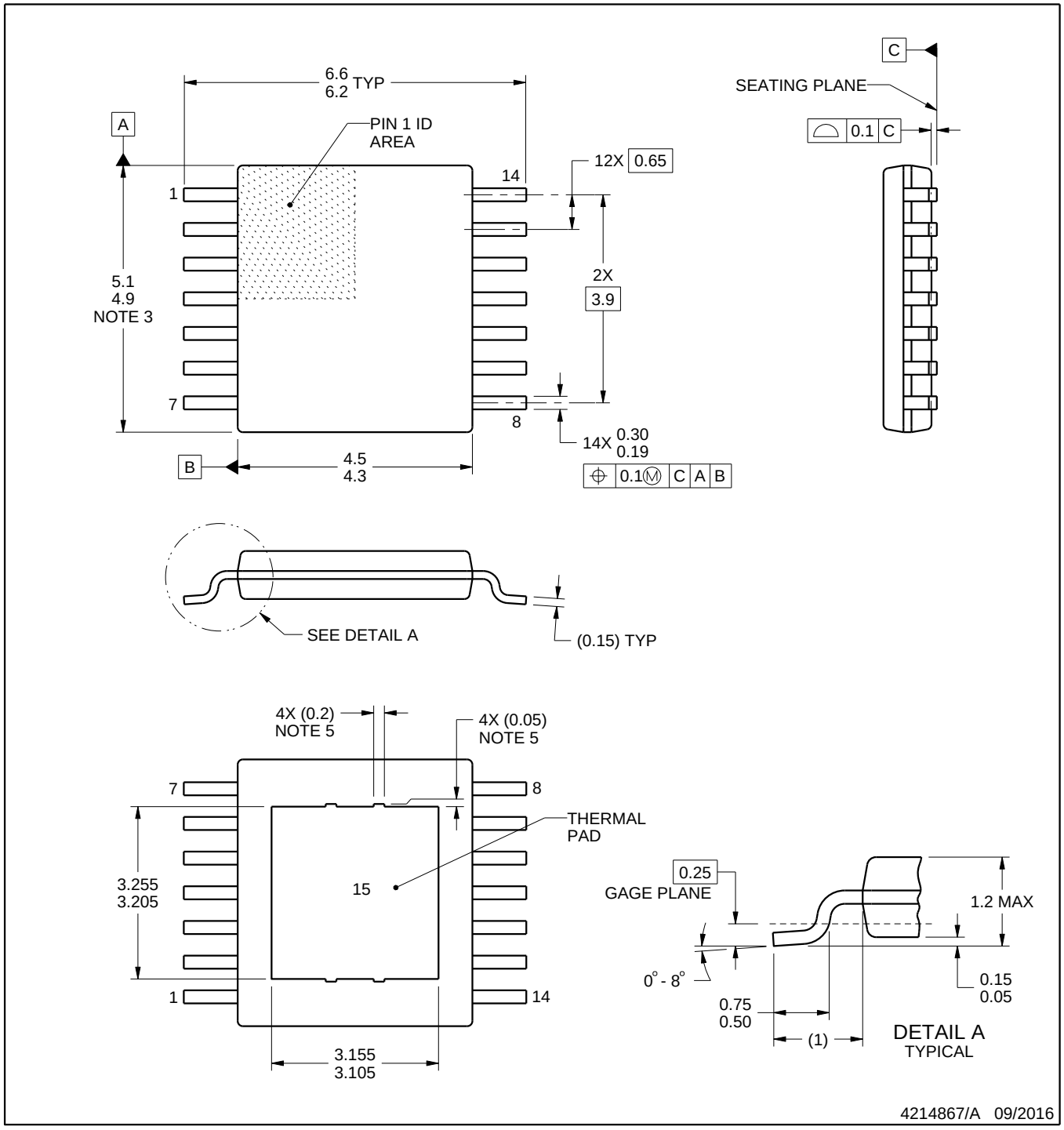


PACKAGE OUTLINE

PWP0014A

PowerPAD™ TSSOP - 1.2 mm max height

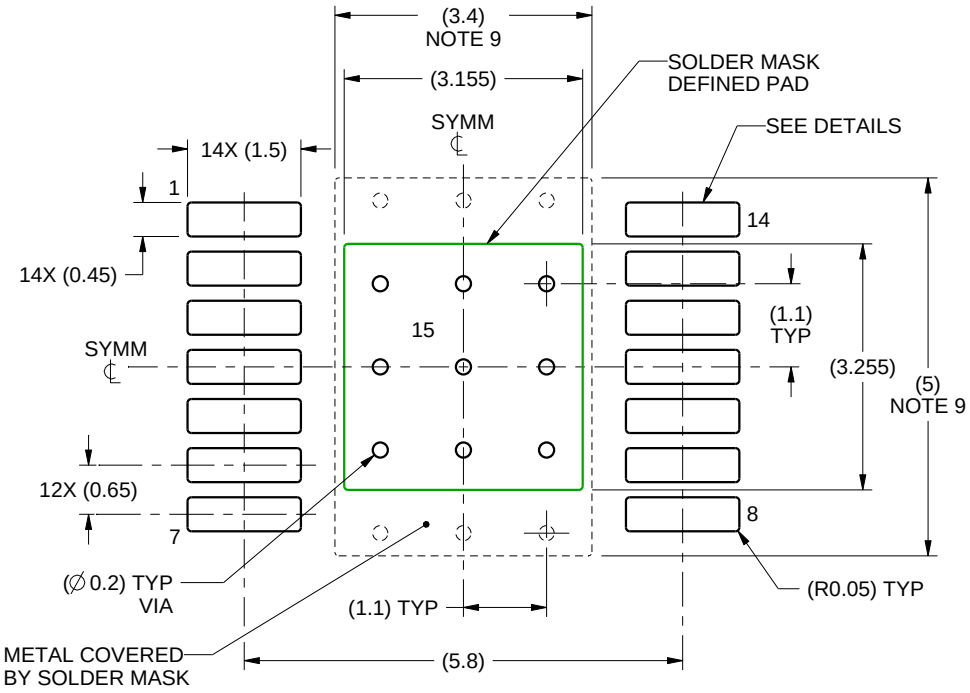
PLASTIC SMALL OUTLINE



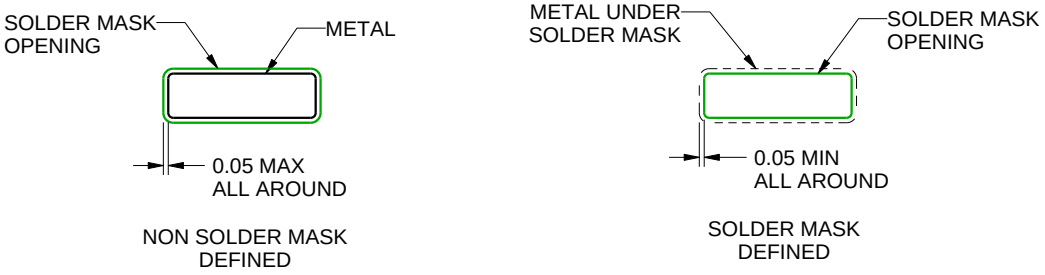
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

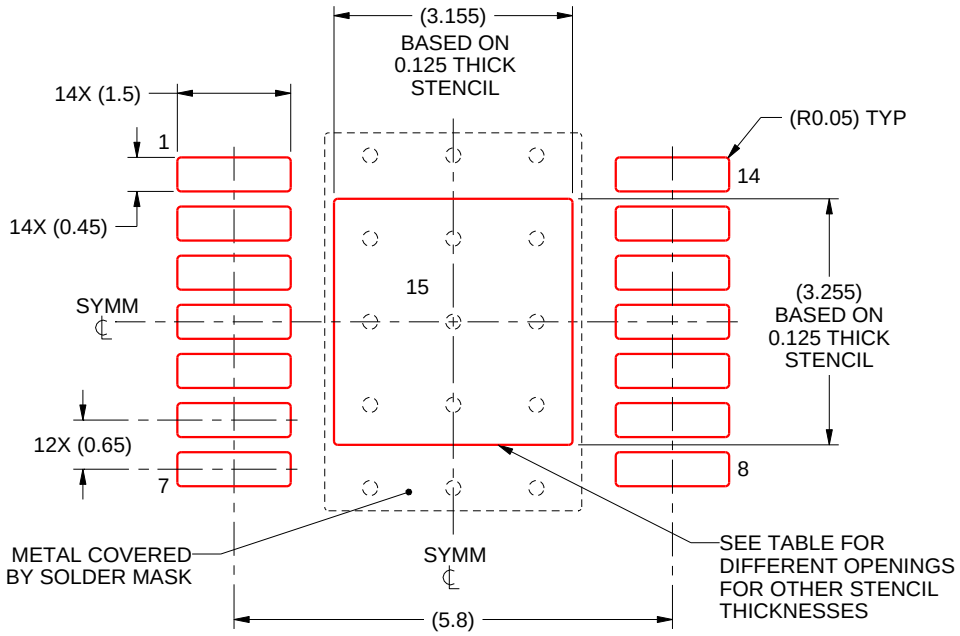


SOLDER MASK DETAILS
PADS 1-14

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.53 X 3.64
0.125	3.155 X 3.255 (SHOWN)
0.15	2.88 X 2.97
0.175	2.67 X 2.75

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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