具有 80V 集成功率 MOSFET 的 LM5007 75V 0.5A 直流/直流降压转换器

1 特性

- 多功能同步降压直流/直流转换器
  - 工作输入电压范围：9V 至 75V
  - 集成型 80V 0.7A N 通道降压开关
  - 内部高电压 V_{CC} 稳压器
  - 可调节输出电压
  - 高效运行
- 自适应恒定导通时间控制架构
  - 超快速瞬态响应
  - 无需控制环路补偿
- 近似恒定的开关频率
  - PWM 导通时间与输入电压成反比变化
- 高精度 2.5V 基准电压
- 低输入静态电流
- 固有保护 特性 可实现稳健设计
  - 智能电流限制保护
  - VCC 和栅极驱动 UVLO 保护
  - 具有迟滞的热关断保护
  - 外部关断控制
- 8 引脚 VSSOP 和 WSON 封装
- 使用 WEBENCH® 电源设计器创建定制稳压器设计

2 应用

- 非隔离式直流/直流降压稳压器
- 次级侧高电压后稳压器
- 48V 汽车系统

3 说明

LM5007 0.5A 降压开关转换器 具有 实现低成本高效率的降压稳压器所需的全部功能。此高电压转换器具有集成型 80V、0.7A N 通道降压开关，可在 9V 至 75V 的输入电压范围内运行。该器件易于实施，采用 8 引脚 VSSOP 封装和热增强型 8 引脚 WSON 封装。

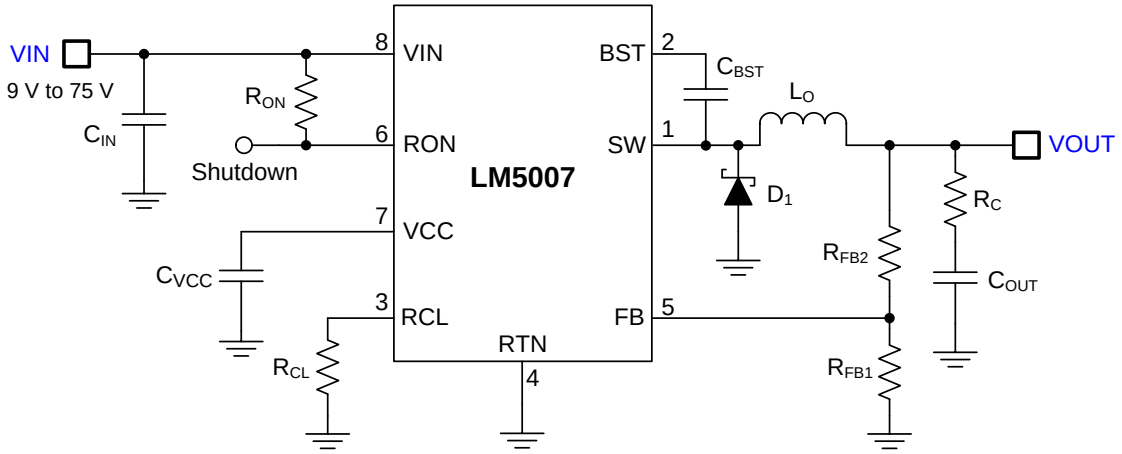
该转换器使用了滞环控制方案，PWM 导通时间与 V_{IN} 成反比。凭借这一特性，该器件在负载和输入电压发生变化时，工作频率能够保持相对恒定。滞环控制无需任何环路补偿并可提供快速瞬态响应。该器件实现了智能电流限制，其强制关闭时间与 V_{OUT} 成反比。该电流限制方案可在减小负载电流折返的同时确保实现短路保护。其他保护 特性 包括通过自动恢复功能实现的热关断、V_{CC} 和栅极驱动欠压锁定以及最大占空比限幅器。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM5007	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (October 2015) to Revision H **Page**

- 已更改 *特性*，编辑性更改 ... 1
- 已更改 *典型应用原理图*，编辑性更改 ... 1
- Changed *Overcurrent Protection*, editorial ... 10
- Changed *Figure 7*, editorial ... 13
- Changed *Power Supply Recommendations*, editorial ... 17
- Changed *Layout Example* to specify recommended component placement ... 18
- 已更改 *器件支持*，添加了新内容 ... 19
- 已更改 *文档支持*，添加了新内容 ... 19

Changes from Revision F (March 2013) to Revision G **Page**

- 添加了*器件信息* 表、*ESD 额定值* 表、*热性能信息* 表、*应用信息*、*设计要求*、*应用曲线*、*电源建议*、*布局* 和*社区资源*。 ... 1
- 添加了*典型应用原理图* ... 1
- Updated pinout drawing description ... 3

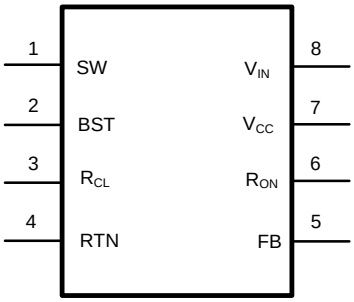
Changes from Revision E (March 2013) to Revision F **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 11

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5 Pin Configuration and Functions

DGK Package and NGT Package
8-Pin VSSOP and 8-Pin WSON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	SW	O	Switching node.	Power switching node. Connect to the LC output filter.
2	BST	I	Boost bootstrap capacitor input.	An external capacitor is required between the BST and SW pins. A 0.01-µF ceramic capacitor is recommended. An internal diode between V_{CC} and BST completes the buck gate drive bias network.
3	R_{CL}	I	Current Limit OFF-time programming pin $t_{OFF} = 10^{-5} / (0.59 + (V_{FB} / 7.22 \times 10^{-6} \times R_{CL}))$	A resistor between this pin and RTN determines the variation of off-time along with the FB pin voltage per cycle while in current limit. The off-time is preset to 17 µs if FB = 0 V and decreases as the FB voltage increases.
4	RTN	—	Circuit ground.	
5	FB	I	Feedback signal from regulated output.	This pin is connected to the inverting input of the internal regulation comparator. The regulation threshold is 2.5 V.
6	R_{ON}	I	On-time set pin $t_{ON} = 1.42 \times 10^{-10} R_{ON} / V_{IN}$	A resistor between this pin and V_{IN} sets the switch on-time as a function of V_{IN}. The minimum recommended on-time is 300 ns at the maximum input voltage.
7	V_{CC}	O	Output from the internal high-voltage bias regulator. V_{CC} is nominally regulated to 7 V.	If an auxiliary voltage is available to raise the voltage on this pin, above the regulation set point (7V), the internal series pass regulator will shutdown, reducing the IC power dissipation. Do not exceed 14V. This output provides gate drive power for the internal buck switch. An internal diode is provided between this pin and the BST pin. A local 0.1-uF decoupling capacitor is recommended. The series pass regulator is current limited to 10 mA.
8	V_{IN}	I	Input supply voltage.	Recommended operating range: 9 V to 75 V.
—	EP	—	Exposed PAD, underside of the WSON-8 package option.	Internally bonded to the die substrate. Connect to GND potential for low thermal impedance.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1).

		MIN	MAX	UNIT
	V_{IN} to RTN		80	V
	BST to RTN		94	V
	SW to RTN (steady state)	–1		V
	BST to V_{CC}		80	V
	BST to SW		14	V
	V_{CC} to RTN		14	V
	All other inputs to RTN	–0.3	7	V
	Lead temperature (soldering 4 sec)		260	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharge through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin. The machine model ESD compliance level for Pin 5 is 150 V. The human body ESD compliance level for Pin 7 and 8 is 1000 V.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	9		75	V
T_J	Junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM5007		UNIT
		DGK (VSSOP)	NGT (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.3	38.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.3	27.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.5	15.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.2	15.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

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6.5 Electrical Characteristics

At T_J = 25°C, V_{IN} = 48 V (unless otherwise noted)(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR						
V_{CC}	V_{CC} Regulator Output		6.6	7	7.4	V
I_{VCC-CL}	V_{CC} Current Limit(2)			11		mA
V_{CC} SUPPLY						
$V_{CC-UVLO}$	V_{CC} Undervoltage Lockout Voltage (V_{CC} increasing)			6.3		V
$V_{CC-UVLO-HYS}$	V_{CC} Undervoltage Hysteresis			206		mV
$t_{VCC-UV-DELAY}$	V_{CC} UVLO Delay (filter)			3		µs
$I_{CC-OPER}$	I_{CC} Operating Current	Not switching, V_{FB} = 3 V		500	675	µA
I_{SHD}	Shutdown/Standby Current	V_{RON} = 0 V		100	200	µA
SWITCH CHARACTERISTICS						
$R_{DS(on)1}$	Buck Switch On-State Resistance	I_{SW} = 0.2 A, $V_{BST} – V_{SW}$ = 6.3 V(3)		0.74	1.34	Ω
$V_{GATE-UV}$	Gate Drive UVLO ($V_{BST} – V_{SW}$)	Rising	3.4	4.5	5.5	V
$V_{GATE-UV-HYS}$	Gate Drive UVLO Hysteresis			400		mV
$V_{DS((max)}$	Breakdown Voltage, V_{IN} to RTN	T_J = 25°C	80			V
		T_J = –40°C to 125°C	76			V
$V_{BST-VCC(max)}$	Breakdown voltage, BST to V_{CC}	T_J = 25°C	80			V
		T_J = –40°C to 125°C	76			V
CURRENT LIMIT						
I_{CL}	Current Limit Threshold		535	725	900	mA
$t_{CL-RESP}$	Current Limit Response Time	I_{SW} overdrive = 0.1 A, time to switch off		225		ns
$t_{CL-OFF1}$	OFF-Time Generator (test 1)	V_{FB} = 0 V, R_{CL} = 100 kΩ		17		µs
$t_{CL-OFF2}$	OFF-Time Generator (test 2)	V_{FB} = 2.3 V, R_{CL} = 100 kΩ		2.65		µs
ON-TIME GENERATOR						
t_{ON1}	TON-1	V_{IN} = 10 V, R_{ON} = 200 kΩ	2.15	2.77	3.5	µs
t_{ON2}	TON-2	V_{IN} = 75 V, R_{ON} = 200 kΩ	290	390	490	ns
V_{SHD}	Remote Shutdown Threshold	Rising	0.45	0.7	1.1	V
$V_{SHD-HYS}$	Remote Shutdown Hysteresis			40		mV
MINIMUM OFF-TIME						
$t_{OFF(min)}$	Minimum Off-Timer	V_{FB} = 0 V		300		ns
REGULATION AND OV COMPARATORS						
V_{REF}	FB Reference Threshold	Internal reference, trip point for switch ON	2.445	2.5	2.550	V
V_{OV-REF}	FB Overvoltage Threshold	Trip point for switch OFF		2.875		V
I_{FB}	FB Bias Current			100		nA
THERMAL SHUTDOWN						
T_{SHD}	Thermal Shutdown Temperature			165		°C
T_{HYS}	Thermal Shutdown Hysteresis			25		°C

(1) All electrical characteristics having room temperature limits are tested during production with $T_A = T_J$ = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The V_{CC} output is intended as a self bias for the internal gate drive power and control circuits. Device thermal limitations limit external loading.
(3) For devices in the WSON-8 package, the MOSFET $R_{DS(on)}$ limits are specified by design characterization data only.

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6.6 Typical Characteristics

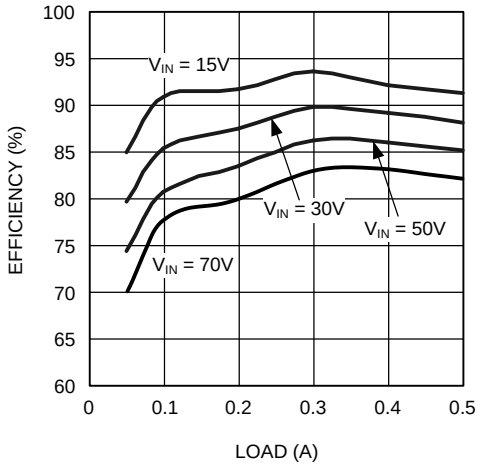
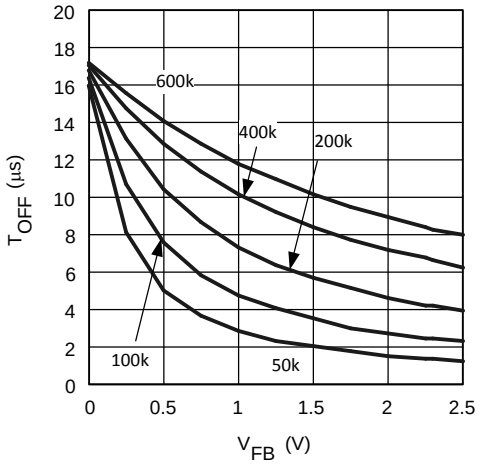
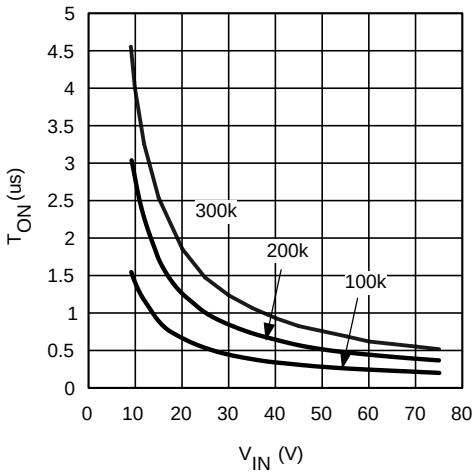


Figure 1. Converter Efficiency at 10-V Output



R_{CL} = 50 kΩ – 600 kΩ

Figure 2. Current Limit T_{OFF} vs. V_{FB}



R_{ON} = 100kΩ, 200kΩ, 300kΩ

Figure 3. T_{ON} vs. V_{IN}

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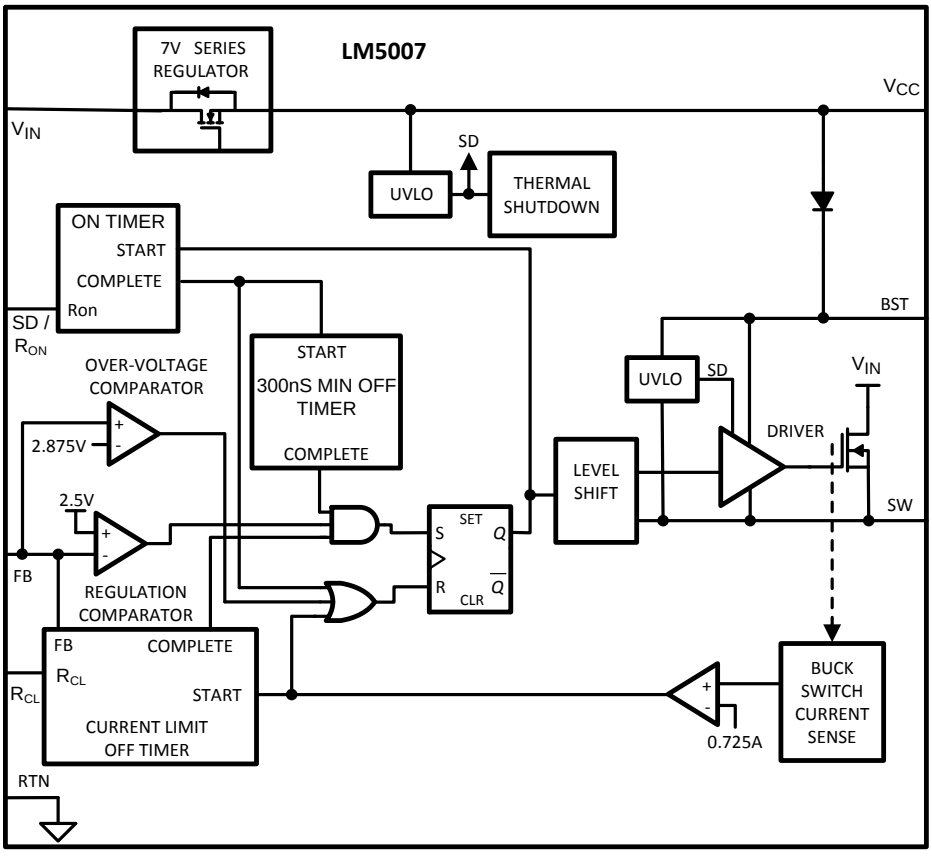
7 Detailed Description

7.1 Overview

The LM5007 regulator is an easy-to-use buck DC/DC converter that operates from 9-V to 75-V supply voltage. The device is intended for step-down conversions from 12-V, 24-V, and 48-V unregulated, semi-regulated and fully-regulated supply rails. With integrated 80-V, 0.7-A buck power MOSFET, the LM5007 delivers up to 500-mA DC load current with exceptional efficiency and low input quiescent current in a very small solution size. The device is easy to use and is provided in VSSOP-8 and thermally-enhanced WSON-8 packages. Designed for simple implementation, a nearly fixed-frequency, constant on-time (COT) operation with discontinuous conduction mode (DCM) at light loads is ideal for low-noise, high current, fast transient load requirements. Control loop compensation is not required, reducing design time and external component count. An intelligent current limit scheme is implemented in the LM5007 with forced off-time after current limit detection, which is inversely proportional to V_{OUT}. This current limiting scheme reduces load current foldback.

The LM5007 incorporates numerous other features for comprehensive system requirements, including VCC undervoltage lockout (UVLO), gate drive UVLO, maximum duty cycle limiter, intelligent current limit off-timer, and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications, such as 48-V telecom and the 48-V automotive power bus designs. The pin arrangement is designed for simple and optimized PCB layout, requiring only a few external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hysteretic Control Circuit Overview

The LM5007 is a buck DC/DC converter that uses a constant on-time (COT) control scheme. The on-time is programmed by an external resistor and varies inversely with line input voltage (V_{IN}). The core regulation elements of the LM5007 are the feedback comparator and the programmed on-time one-shot. The regulator output voltage is sensed at the feedback pin (FB) and compared to an internal reference voltage (2.5 V). If the FB voltage is below the reference voltage, the buck switch is turned on for a fixed time interval determined by the input voltage and a programming resistor (R_{ON}). Following the on period, the switch remains off for at least the minimum off-time interval of 300 ns. If the FB voltage is still below the reference after the 300-ns off-time, the switch turns on again for another on-time interval. This switching behavior continues until the FB voltage reaches the reference voltage level.

The LM5007 operates in discontinuous conduction mode (DCM) at light load currents and continuous conduction mode (CCM) at heavier load currents. In DCM, current through the output inductor starts at zero and ramps up to a peak value during the buck switch on-time and then back to zero during the off-time. The inductor current remains at zero until the next on-time interval begins when FB falls below the internal reference voltage. The operating frequency in DCM is relatively low and varies with load. Thus, the conversion efficiency is maintained at light loads, since the switching losses decrease with the reduction in load current and switching frequency. Calculate the approximate switching frequency in DCM with Equation 1.

$$F_{SW(DCM)} = \frac{{V_{OUT}}^2 \cdot L_O}{R_{LOAD} \cdot {R_{ON}}^2} \cdot 10^{20} \tag{1}$$

In CCM, current flows continuously through the inductor and never ramps down to zero. The switching frequency in CCM is greater than that in DCM and remains relatively constant with load and line variations. Calculate the approximate switching frequency in CCM with Equation 2.

$$F_{SW(CCM)} = \frac{V_{OUT}}{1.42 \cdot 10^{-10} \cdot R_{ON}} \tag{2}$$

The output voltage (V_{OUT}) can be programmed by two external resistors as shown in Figure 4. Calculate the output voltage setpoint using Equation 3.

$$V_{OUT} = 2.5\,V \cdot \left(1 + \frac{R_1}{R_2}\right) \tag{3}$$

The feedback comparator in hysteretic regulators depend upon the output ripple voltage to switch the power MOSFET on and off at regular intervals. In order for the internal comparator to respond quickly to changes in output voltage, proportional to inductor current, a minimum amount of capacitor Equivalent Series Resistance (ESR) is required. A ripple voltage of 25 mV to 50 mV is recommended at the feedback pin (FB) for stable operation. In cases where the intrinsic capacitor ESR is too small, additional series resistance may be added.

For applications where lower output voltage ripple is required, the load can be connected directly to the low ESR output capacitor as shown in Figure 4. The series resistor (R) will degrade the load regulation. Another technique for enhancing the ripple voltage at FB is to place a capacitor in parallel with the upper feedback resistor, R1. The addition of this feedforward capacitor reduces the attenuation of the ripple voltage from the feedback divider.

7.3.2 High-Voltage Bias Supply Regulator

The LM5007 contains an internal high-voltage bias supply regulator. The input pin (V_{IN}) can be connected directly to line voltages from 9 V to 75 V. To avoid supply voltage transients due to long lead inductances on the input pin (V_{IN}), it is always recommended to connect a low-ESR ceramic capacitor (≈ 0.1 µF) between V_{IN} and RTN, located close to the respective pins of the LM5007. The bias regulator is internally current limited to 10 mA. Upon power up, the regulator is enabled and sources current into an external capacitor connected to the V_{CC} pin. When the V_{CC} voltage reaches the regulation point of 7 V, the controller output is enabled.

An external auxiliary supply voltage can be applied to the V_{CC} pin. If this auxiliary voltage is greater than 7 V, the internal regulator will essentially shutoff, thus reducing internal power dissipation.

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Feature Description (continued)

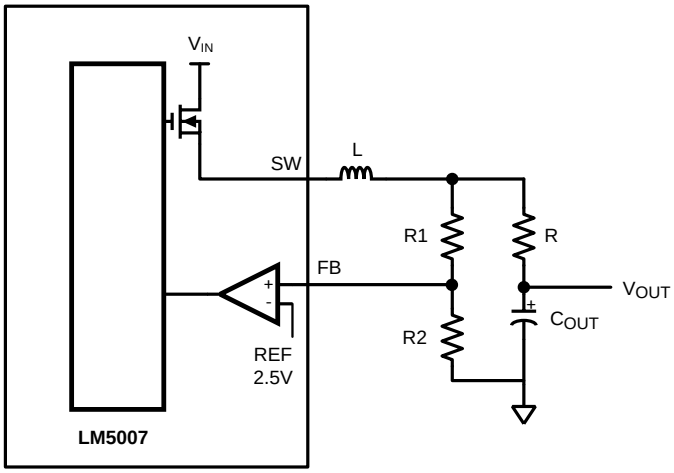


Figure 4. Low Output Ripple Voltage Configuration

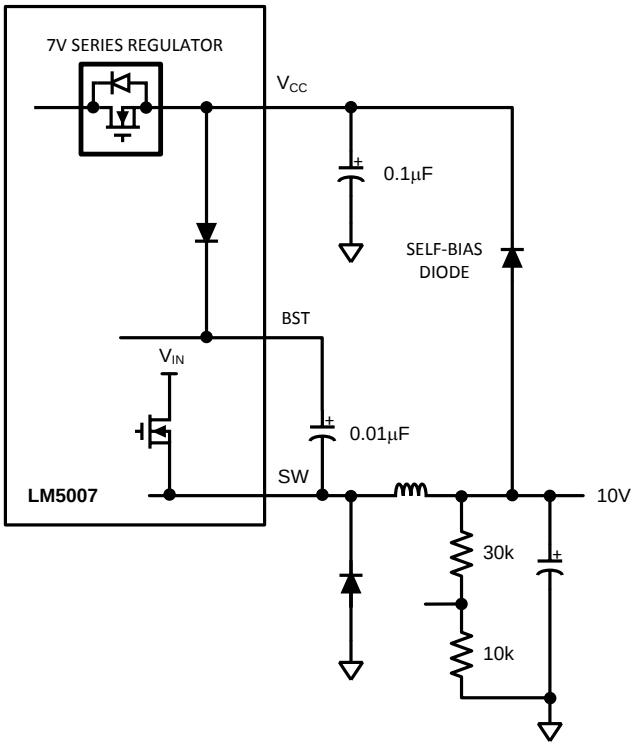


Figure 5. Self-Biased Configuration with V_{OUT} Feeding V_{CC} Through a Diode

7.3.3 Overvoltage Comparator

The overvoltage comparator is provided to protect the output from overvoltage conditions due to sudden input line voltage changes or output loading changes. The overvoltage comparator monitors the FB voltage relative to an internal 2.875-V reference, $V_{OV\text{-}REF}$. If the voltage at FB rises above $V_{OV\text{-}REF}$, the comparator immediately terminates the buck switch on-time pulse.

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Feature Description (continued)

7.3.4 On-Time Generator and Shutdown

The on-time of the LM5007 is set inversely proportional to the input voltage by an external resistor connected between V_{IN} and R_{ON}. The R_{ON} pin is a low impedance input biased at approximately 1.5 V. Thus, the current through the resistor and into the R_{ON} pin is approximately proportional to V_{IN} and used internally to control the on-timer. This scheme of input voltage feedforward hysteretic operation achieves nearly constant switching frequency over varying line and load conditions. Equation 4 specifies the on-time equation for the LM5007.

$$t_{ON} = 1.42 \cdot 10^{-10} \cdot \frac{R_{ON}}{V_{IN}} \tag{4}$$

The R_{ON} pin of the LM5007 also provides a shutdown function that disables the converter and significantly decreases quiescent power dissipation. Pulling the voltage at R_{ON} below a 0.7-V logic threshold activates a low-power shutdown mode. The V_{IN} quiescent current in this shutdown mode is approximately 100 µA internal to the LM5007 plus the current in the R_{ON} resistor.

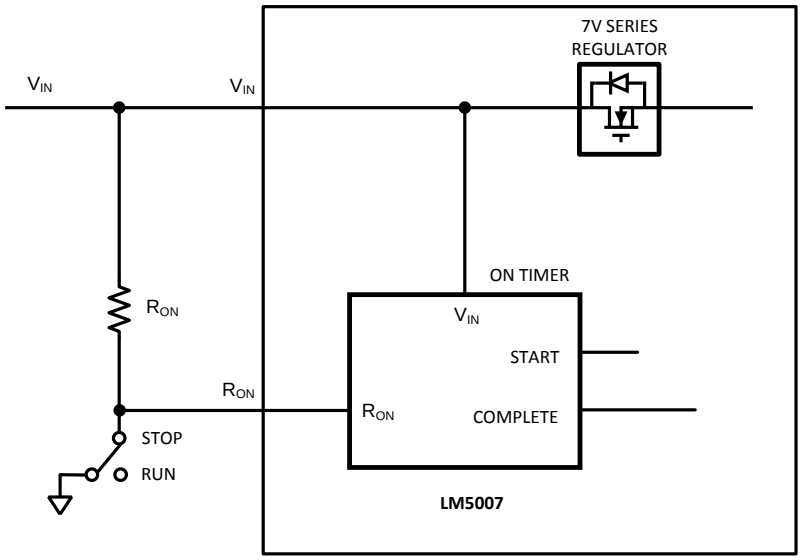


Figure 6. Shutdown Implementation

7.3.5 Overcurrent Protection

The LM5007 contains an intelligent current limit off-timer intended to reduce the foldback characteristic inherent with fixed off-time overcurrent protection (OCP) schemes. If the current in the buck switch exceeds 725 mA, the present cycle on-time is immediately terminated (cycle-by-cycle current limit). Following the termination of the cycle a non-resettable current limit off-timer is initiated. The duration of the off-time is a function of the external resistor (R_{CL}) and the FB voltage. When the FB voltage equals zero, the current limit off-time is internally preset to 17 µs. This condition occurs during a short-circuit condition when a maximum amount of off-time is required.

In case of output overload (not a complete short circuit), the current limit off-time is reduced as a function of the output voltage (measured at the FB pin). Scaling the off-time with smaller overloads reduces the amount of foldback and also reduces the initial start-up time. Calculate the current limit off-time for a given FB voltage and R_{CL} resistor using Equation 5.

$$t_{OFF(CL)} = \cdot \frac{10^{-5}}{0.59 + \frac{V_{FB}}{7.22 \cdot 10^{-6} \cdot R_{CL}}} \tag{5}$$

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Feature Description (continued)

Select the current limit off-time such that it is less than the MOSFET off-time during normal steady-state switching operation. Applications utilizing low-resistance inductors and/or a low-voltage-drop freewheeling power diodes may require special evaluation at high line, short-circuited conditions. In this special case the preset 17-µs off-time (V_{FB} = 0 V) may be insufficient to provide inductor volt-seconds balance. Additional inductor resistance, output resistance or a larger voltage drop diode may be necessary to balance inductor volt-seconds and limit the short-circuit current.

7.3.6 N-Channel Buck Switch and Driver

The LM5007 integrates an N-channel buck switch and associated floating high voltage gate driver. This gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. The bootstrap capacitor is charged by V_{CC} through the internal high voltage diode. A 0.01-µF ceramic capacitor connected between BST and SW is recommended.

During each cycle when the buck switch turns off, the SW voltage is approximately 0 V. When the SW voltage is low, the bootstrap capacitor is charged from V_{CC} through the internal bootstrap diode. The minimum off-timer, set to 300 ns, ensures that there is a minimum interval every switching cycle to recharge the bootstrap capacitor.

An external recirculating diode from the SW to RTN is necessary to carry the inductor current after the internal buck switch turns off. This external diode must be an ultra-fast switching or Schottky type to reduce turn-on losses and switch current overshoot. The reverse voltage rating of the recirculating diode must be greater than the maximum line input voltage.

7.3.7 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When thermal protection is activated, typically at 165°C, the converter is forced into a low power reset state, disabling the output driver. This feature is provided to prevent catastrophic failures from accidental device overheating.

7.3.8 Minimum Load Current

A minimum load current of 1 mA is required to maintain proper operation. If the load current falls below that level, the bootstrap capacitor may discharge during the long off-time, and the circuit will either shutdown or cycle on and off at a low frequency. If the load current is expected to drop below 1 mA in the application, choose the feedback resistors with sufficiently low value to provide the minimum required load current at nominal V_{OUT}.

7.3.9 Ripple Configuration

The LM5007 uses an adaptive constant on-time (COT) control in which the conduction time of the buck MOSFET is terminated by an on-timer and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}). Therefore, for stable operation, the feedback voltage must decrease monotonically and in phase with the inductor current during the off-time interval. Furthermore, this change in feedback voltage (V_{FB}) during the off-time must be larger than any noise component present at the feedback node.

Table 1 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

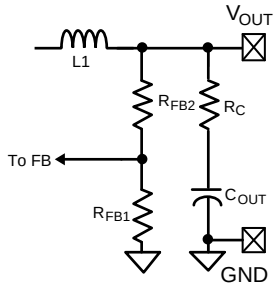
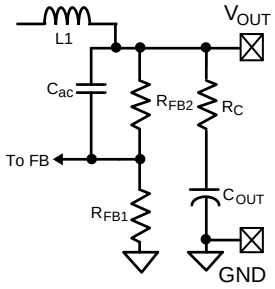
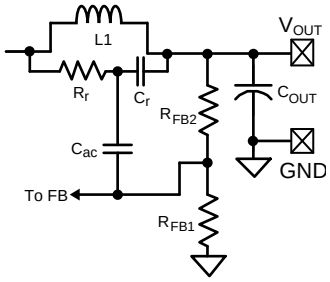
The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output node (V_{OUT}) for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters with multiple on-time bursts in close succession followed by a long off-time.

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Feature Description (continued)

Type 3 ripple method uses R_r and C_r and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is ac coupled using C_{ac} to the feedback node (FB). Since this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs* (SNVA166) for more details for each ripple generation method.

Table 1. Ripple Configuration

TYPE 1 LOWEST COST CONFIGURATION	TYPE 2 REDUCED RIPPLE CONFIGURATION	TYPE 3 MINIMUM RIPPLE CONFIGURATION
		
$R_C = \frac{25mV}{\Delta I_{L(min)}} \cdot \frac{V_{OUT}}{V_{REF}}$ (6)	$C_{ac} \geq \frac{5}{F_{SW} \cdot \left(R_{FB1} \| R_{FB2}\right)}$ $R_C = \frac{25mV}{\Delta I_{L(min)}}$ (7)	$C_r = 3.3nF$ $C_{ac} = 100nF$ $R_r \cdot C_r = \frac{\left(V_{IN(min)} - V_{OUT}\right) \cdot t_{ON}}{25mV}$ (8)

7.4 Device Functional Modes

7.4.1 Standby Mode with V_{IN}

The LM5007 is intended to operate with input voltages above 9 V. The minimum operating input voltage is determined by the V_{CC} undervoltage lockout threshold of 6.3 V (typ). If V_{IN} is too low to support a V_{CC} voltage greater than the V_{CC} UVLO threshold, the converter switches to its standby mode with the buck switch in the off state.

7.4.2 Shutdown Mode

The LM5007 is in shutdown mode when the R_{ON} pin is pulled below 0.7 V (typ). In this mode, the buck MOSFET is held off and the V_{CC} regulator is disabled.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5007 requires only a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing a LM5007-based converter, a comprehensive LM5007 quick-start calculator is available for download to assist the designer with component selection for a given application. WEBENCH® online software is also available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following sections discuss a design procedure using a typical application example. Figure 7 shows the LM5007 in a configuration suitable for several application use cases. See the LM5007 EVM for more details.

8.2 Typical Application

The application schematic of an LM5007-based buck converter is shown in Figure 7. For an output voltage (V_{OUT}) above the maximum regulation threshold of V_{CC} (see *Electrical Characteristics*), the V_{CC} pin can be supplied from V_{OUT} through a diode for higher efficiency and lower power dissipation in the IC.

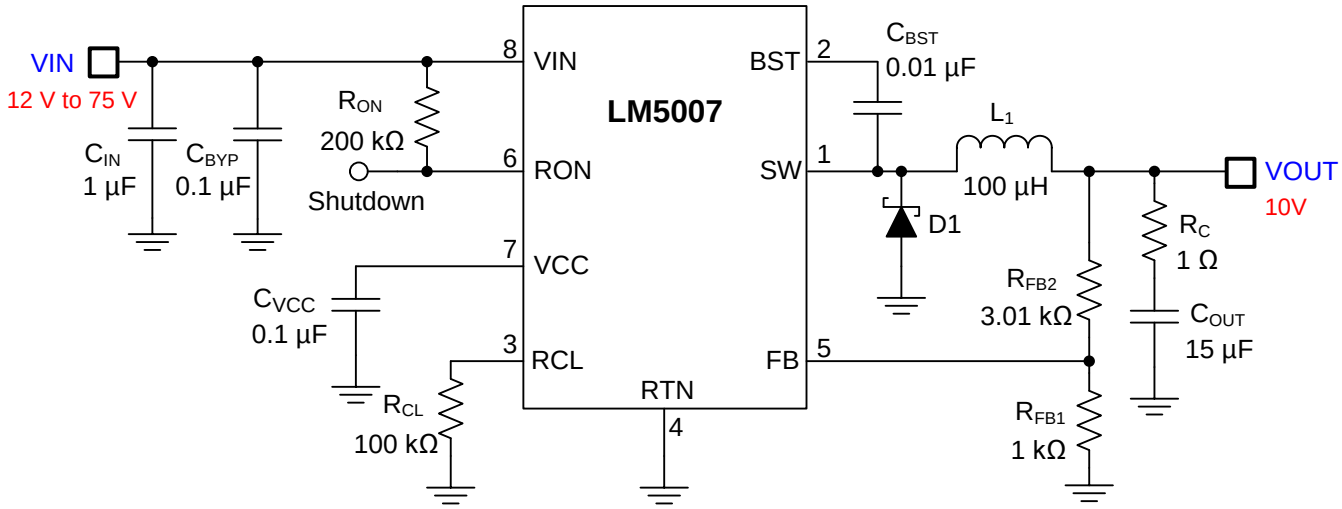


Figure 7. 12-V to 75-V Input and 10-V, 400-mA Output Buck Converter

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETERS	VALUE
Input Voltage	12 V to 75 V
Output Voltage	10 V
Maximum Output Current	400 mA
Nominal Switching Frequency	380 kHz

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8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5007 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Custom Design With Excel Quickstart Tool

Select components based on the converter specifications using the LM5007 quick-start calculator available for download from the LM5007 product folder.

8.2.2.3 Feedback Resistors, R_{FB1} and R_{FB2}

$V_{OUT} = V_{FB} \times (R_{FB2}/R_{FB1} + 1)$, and since V_{FB} = 2.5 V in regulation, the ratio of R_{FB2} to R_{FB1} is 3 : 1. Select standard values of R_{FB1} = 1 kΩ and R_{FB2} = 3.01 kΩ. Other values can be chosen as long as the 3 : 1 ratio is maintained.

8.2.2.4 Switching Frequency Selection, R_{ON}

Set the switching frequency by resistor R_{ON} using Equation 9.

$$R_{ON} = \frac{V_{OUT}}{1.42 \cdot 10^{-10} \cdot F_{SW}} \tag{9}$$

Selecting F_{SW} = 380 kHz results in R_{ON}= 185 kΩ. Choose a standard value of 200 kΩ for this design.

8.2.2.5 Buck Inductor, L_1

The inductor is selected to provide a current ripple of 40% to 50% of the full-load current. In addition, the peak inductor current at maximum load must be smaller than the minimum current limit threshold provided in *Electrical Characteristics*. The inductor current ripple is given by Equation 10.

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L_1 \cdot F_{SW}} \cdot \frac{V_{OUT}}{V_{IN}} \tag{10}$$

The maximum ripple is observed at the maximum input voltage. Using V_{IN} = 75 V and ΔI_L= 50% x $I_{OUT(max)}$ results in L_1 = 114 µH. Select a standard inductor value of 100 µH. The inductor current ripple ranges from 88 mA to 228 mA depending on input voltage. The peak inductor and switch current at full load are given by Equation 11.

$$I_{L1(peak)} = I_{OUT(max)} + \frac{\Delta I_L}{2} \tag{11}$$

At maximum V_{IN}, the peak inductor current is 514 mA, which is lower than the minimum current limit threshold of 535 mA. The selected inductor should be able to operate at the maximum current limit of 900 mA without saturation during startup and overload conditions.

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8.2.2.6 Output Capacitor, C_{OUT}

Select the output capacitor to minimize the capacitive ripple. The maximum ripple is observed at the maximum input voltage and is given by Equation 12.

$$C_{OUT} = \frac{\Delta I_L}{8 \cdot F_{SW} \cdot \Delta V_{COUT}}$$

where

- ΔV_{COUT} is the voltage ripple across the capacitor,
- ΔI_L is the peak-to-peak inductor ripple current. (12)

Substituting V_{IN} = 75 V and targeting ΔV_{COUT}= 10 mV gives C_{OUT} = 7.5 µF. Select a standard 15-µF value for C_{OUT} with X5R or X7R dielectric and a voltage rating of 16 V or higher.

8.2.2.7 Type I Ripple Circuit, R_C

Choose a type I ripple circuit, as described in Ripple Configuration, for this example. For a constant on-time (COT) converter to be stable, the injected in-phase ripple must be larger than the capacitive ripple on C_{OUT}.

Using the type I ripple circuit equations with minimum FB pin ripple of 25 mV, calculate the value of series resistor R_C using Equation 13.

$$R_C = \frac{25\,mV}{\Delta I_{L(min)}} \cdot \frac{V_{OUT}}{V_{REF}} \tag{13}$$

Based on the calculated value of 1.1 Ω, select a standard value of 1 Ω.

8.2.2.8 Input Capacitor, C_{IN}

The input capacitor should be large enough to limit the input voltage ripple that can be calculated using Equation 14.

$$C_{IN} = \frac{I_{OUT(max)} \cdot D \cdot (1 - D)}{F_{SW} \cdot \Delta V_{CIN}} \tag{14}$$

The input ripple reaches its maximum at D = 0.5. Targeting a ΔV_{CIN} = 0.5 V at using a duty cycle of D = 0.5 results in C_{IN} = 0.526 µF. A standard value of 1 µF is selected. The input capacitor should be rated for the maximum input voltage under all conditions. A 100-V, X7R type capacitor is selected for this design. The input capacitor should be placed close to the V_{IN} pin and the anode of the diode (D1) as it supplies high-frequency switching current.

Also place a 0.1-µF bypass capacitor (C_{BYP}) very close to V_{IN} and RTN pins of the IC to reduce switching power loop parasitic inductance and mitigate SW node overshoot and ringing.

8.2.2.9 Current Limit, R_{CL}

Resistor R_{CL} sets the current limit off-timer according to Equation 5. The useable values tend to be in the range of 100 kΩ to 1 MΩ. Equation 15 specifies the off-time required for volt-second balance on the inductor in current limit.

$$t_{OFF(ILIM)} = \frac{V_{IN(max)} \cdot 225\,ns}{V_{OUT} + V_F + I_{LIM} \cdot R_{DCR}}$$

where

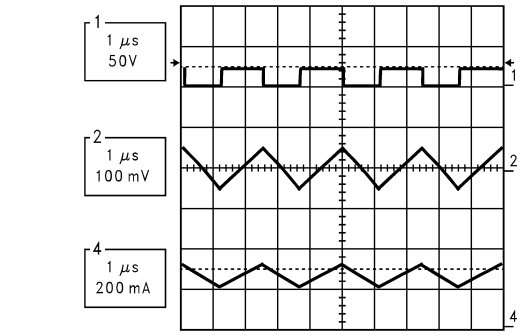
- 225 ns is the current limit response time,
- V_F is the forward voltage drop of the freewheeling power diode,
- V_{OUT} is the output voltage,
- I_{LIM} is the current limit,
- R_{DCR} is the inductor DC resistance. (15)

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The programmed current limit off-time should be higher than the off-time needed for volt-second balance on the inductor. For a short at the output (V_{OUT} = 0 V) and V_F = 0.7 V, an inductor DCR of 390 mΩ or higher is needed to achieve volt-second balance at the maximum programmed current limit off-time of 17 µs. Using Equation 5, an R_{CL} of greater than 10 kΩ can be used. Select a conservative value of 100 kΩ for this design.

For step-by-step design procedures, circuit schematics, bill of materials, PCB files, simulation and test results of LM5007-powered implementations, refer to the *TI Designs* reference design library.

8.2.3 Application Curves

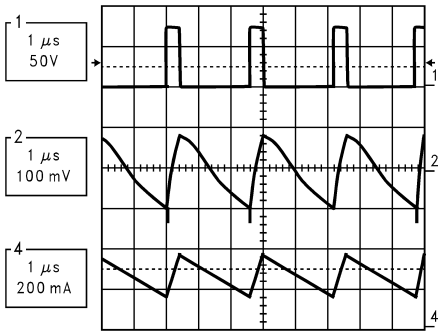


V_{OUT} = 10 V
CH1: Switch Node

V_{IN} = 20 V
CH2: V_{OUT} (AC)

I_{OUT} = 250 mA
CH4: Inductor Current

Figure 8. Switching Waveforms, V_{IN} = 20 V



V_{OUT} = 10 V
CH1: Switch Node

V_{IN} = 75 V
CH2: V_{OUT} (AC)

I_{OUT} = 250 mA
CH4: Inductor Current

Figure 9. Switching Waveforms, V_{IN} = 75 V

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9 Power Supply Recommendations

The LM5007 converter is designed to operate from a wide input voltage range from 9 V to 75 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with Equation 16.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (16)$$

where

- η is the efficiency

If the converter is connected to an input supply through long wires or PCB traces with large impedance, achieving stable performance requires special care. The parasitic inductance and resistance of the input cables may have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The user's guide *Simple Success with Conducted EMI for DC-DC Converters* (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator.

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10 Layout

10.1 Layout Guidelines

The LM5007 regulation and overvoltage comparators are very fast, and as such respond to short-duration noise pulses. Layout considerations are therefore critical for optimum performance:

1. Minimize the area of the high di/dt switching current loop consisting of the VIN and SW pins, freewheeling power diode, and input ceramic capacitor. Keep the input capacitor(s) close to the VIN pin of the LM5007. Place the cathode of the freewheeling diode close to the SW pin and and its anode near the return terminal of the input capacitor as illustrated in Figure 10. Route a short, direct connection to the RTN pin using polygon copper pours under the IC.
2. Place the inductor close to the SW pin of the LM5007. Minimize SW node copper area to reduce radiated noise related to high dv/dt.
3. Locate C_{BST}, R_{CL}, R_{ON} and C_{VCC} components as physically close as possible to their respective pins, thereby minimizing noise pickup in the printed-circuit tracks.
4. Locate the VOUT sense trace away from noise sources such as inductors. Place both feedback resistors close to the FB pin to minimize the length of the FB trace.
5. Place a solid GND plane on layer 2 of the PCB.

If the internal dissipation of the LM5007 converter produces excessive junction temperatures during normal operation, optimal use of the PCB ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the WSON-8 package can be soldered to a ground plane on the PCB, and that plane should extend out from beneath the IC to help dissipate the heat. Additionally, the use of wide PCB traces for power connection can also help conduct heat away from the IC. Judicious positioning of the LM5007 converter within the end product, along with use of any available air flow (forced or natural convection), can help reduce the operating junction temperature.

10.2 Layout Example

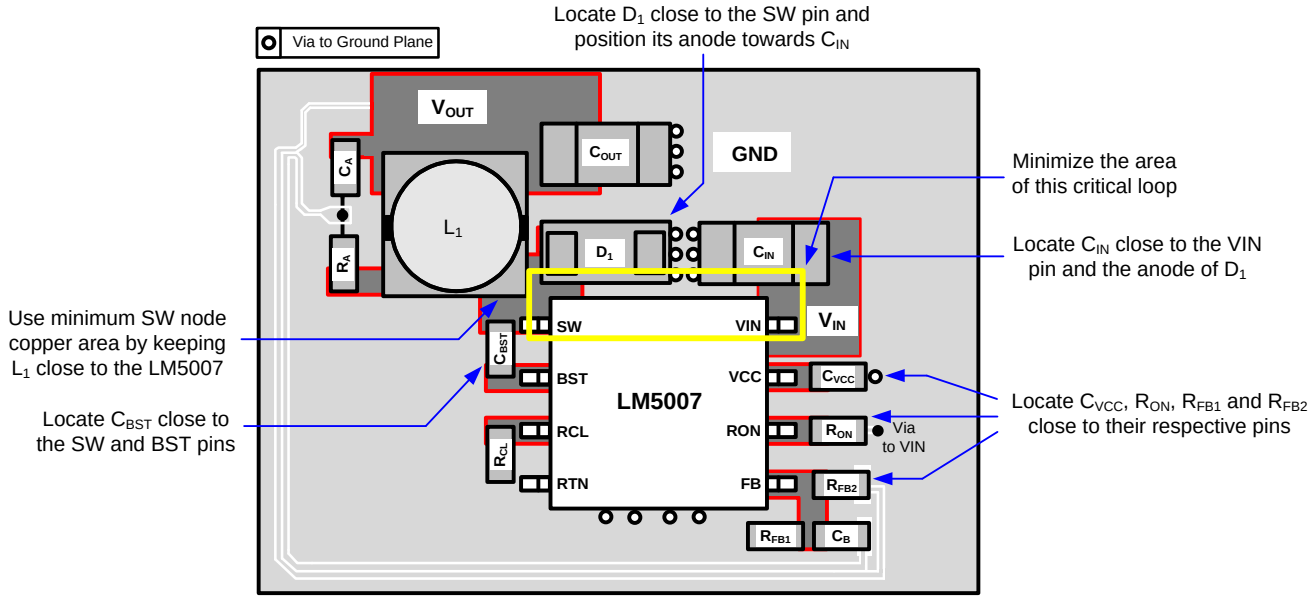


Figure 10. PCB Layout Example

NOTE

It is critical to minimize switching loop parasitic inductance by locating the input capacitor close to the VIN pin of the LM5007. Also, place the freewheeling power diode near the SW pin with its anode adjacent to the input capacitor as shown in Figure 10.

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11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.1.2 使用 WEBENCH® 工具创建定制设计

请单击此处，使用 LM5007 器件及其 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.1.3 开发支持

相关开发支持请参阅以下资源：

- 有关 TI 的参考设计库，请访问 TI Designs
- 有关 TI WEBENCH 设计环境，请访问 WEBENCH® 设计中心

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- *LM5007 快速入门计算器*
- *LM5007EVAL 评估板*
- *LM5007SD-EVAL 评估板*
- *LM5006EVAL 评估板*
- *LM5008EVAL 评估板*
- *LM5008AEVAL 评估板*
- *LM5009EVAL 评估板*
- *LM5010-EVAL 评估板*
- *LM5010AEVAL 评估板*
- *《支持宽输入/输出电压差异的降压稳压器拓朴》*(SNVA594)
- *AN-1481《使用恒定导通时间稳压器设计控制输出纹波并实现 ESR 独立性》*(SNVA166)
- 白皮书：
  - *《评估适用于成本驱动型严苛应用的宽 V_{IN}、低 EMI 同步降压 电路》*(SLYY104)
  - *《电源的传导 EMI 规格概述》*(SLYY136)
  - *《电源的辐射 EMI 规格概述》*(SLYY142)
- TI Designs：
  - *PoE PSE Type 2 (30W) IEEE 802.3at 完全自主的四端口解决方案*
  - *适用于数字输出模块的 8 通道 2A 高侧驱动器参考设计*
  - *适用于 PLC 的低侧 0.5A、8 通道数字输出模块*

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文档支持 **(**接下页**)**

- *具有数字输入和处理功能的高保真 175W D 类音频放大器参考设计*
- *适用于 12V/48V 汽车系统的双向直流/直流转换器参考设计*

11.2.1.1 PCB 布局资源

- *《AN-1149 开关电源布局指南》*(SNVA021)
- *《AN-1229 Simple Switcher PCB 布局指南》*(SNVA054)
- *构建电源 - 布局注意事项* (SLUP230)
- *《使用 LM4360x 与 LM4600x 简化低辐射 EMI 布局》*(SNVA721)
- *《AN-2162：轻松解决直流/直流转换器的传导 EMI 问题》*(SNVA489)
- *《通过将电感寄生效应降至最低来降低降压转换器 EMI 和电压应力》*(SLYT682)
- Power House 博客：
  - *直流/直流转换器的高密度 PCB 布局*

11.2.1.2 热设计资源

- *《AN-2020 热设计：学会洞察先机，不做事后诸葛》*(SNVA419)
- *《确保外露焊盘封装的最佳热阻性的 AN-1520 电路板布局指南》*(SNVA183)
- *《半导体和 IC 封装热指标》*（文献编号：SPRA953）
- *《使用 LM43603 和 LM43602 简化热设计》*(SNVA719)
- *《PowerPAD™ 热增强型封装》*(SLMA002)
- *《PowerPAD 速成》*（文献编号：SLMA004）
- *《使用新的热指标》*(SBVA025)

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

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WEBENCH is a registered trademark of Texas Instruments.

11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5007MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S81B
LM5007MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S81B
LM5007MM/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S81B
LM5007MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S81B
LM5007MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S81B
LM5007MMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S81B
LM5007SD/NOPB	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L00031B
LM5007SD/NOPB.A	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L00031B
LM5007SD/NOPB.B	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L00031B
LM5007SDX/NOPB	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L00031B
LM5007SDX/NOPB.A	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L00031B
LM5007SDX/NOPB.B	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L00031B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

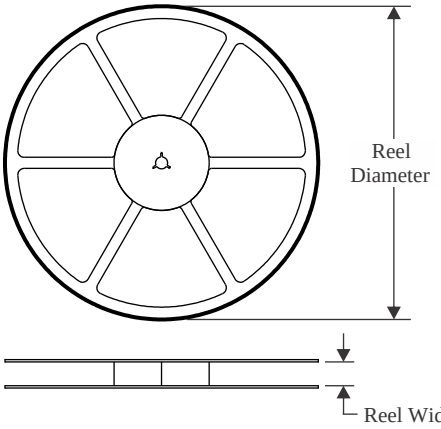
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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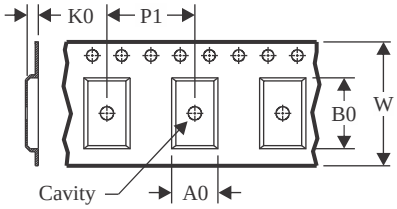
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

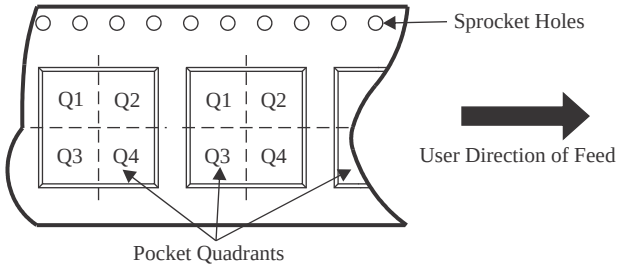


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

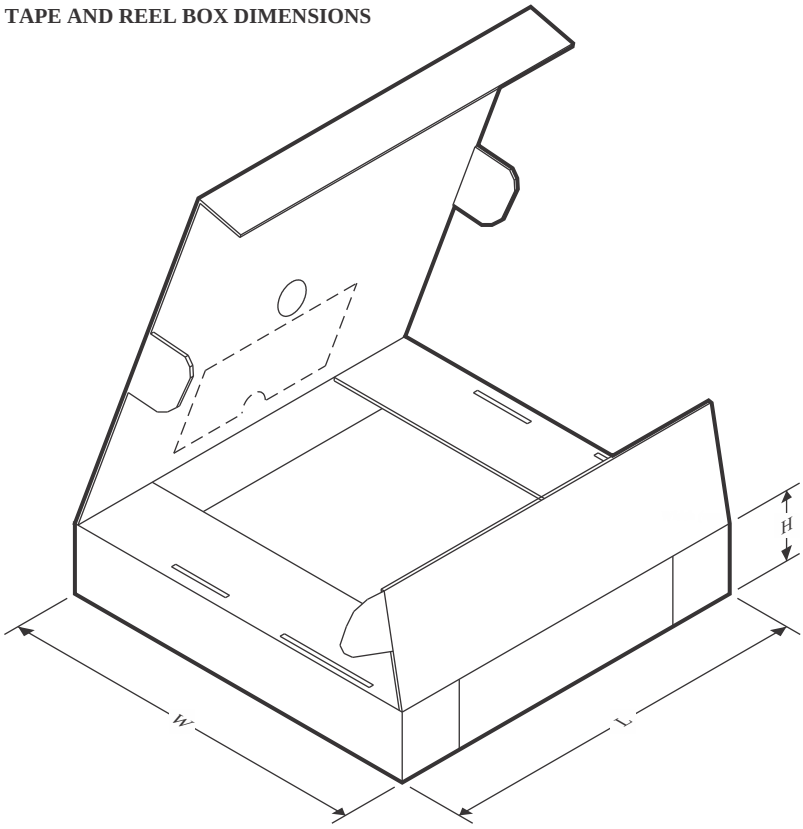
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5007MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5007MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5007MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LM5007SD/NOPB	WSON	NGT	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5007SDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

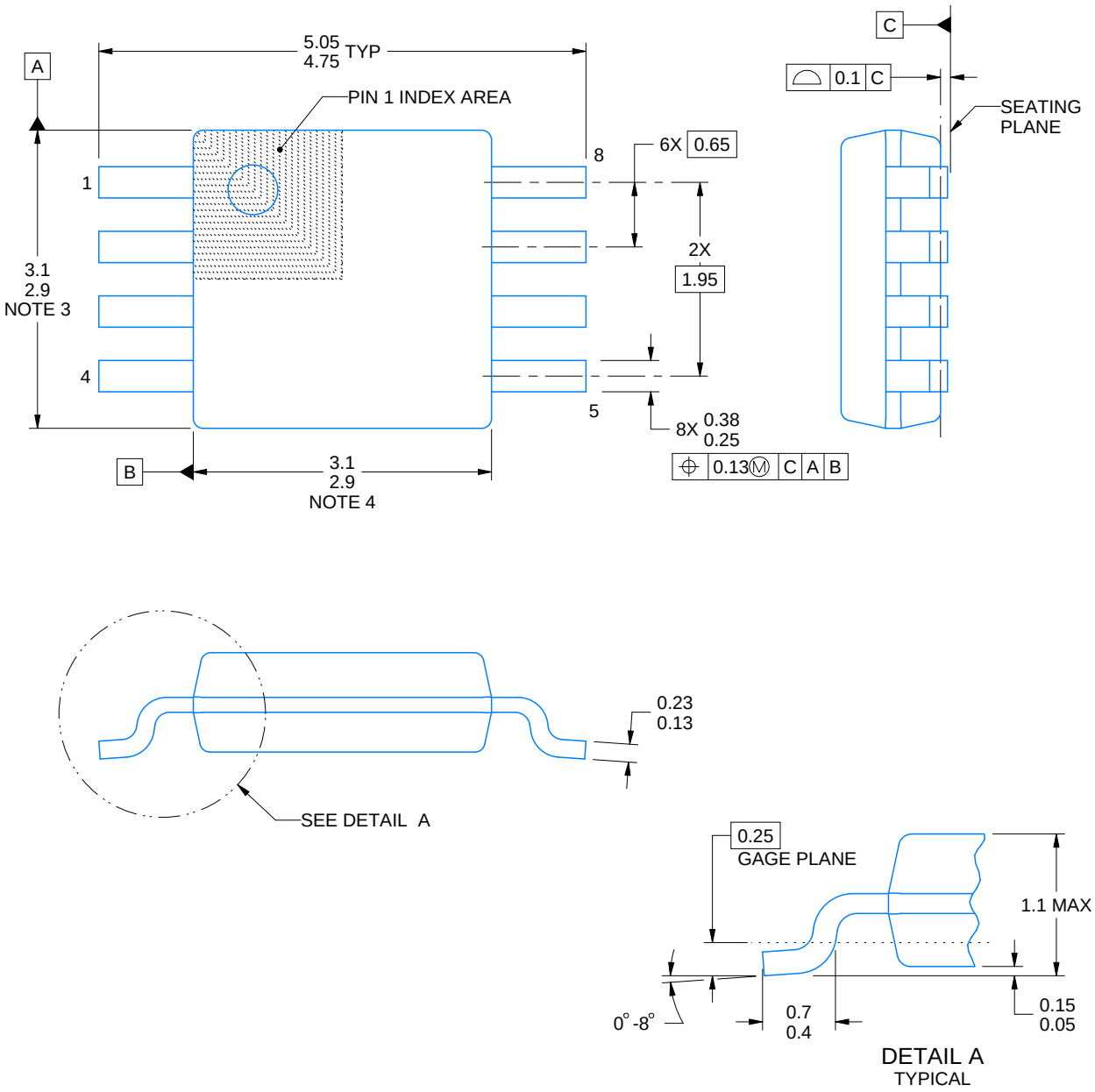
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5007MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM5007MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM5007MMX/NOPB	VSSOP	DGK	8	3500	366.0	364.0	50.0
LM5007SD/NOPB	WSON	NGT	8	1000	208.0	191.0	35.0
LM5007SDX/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

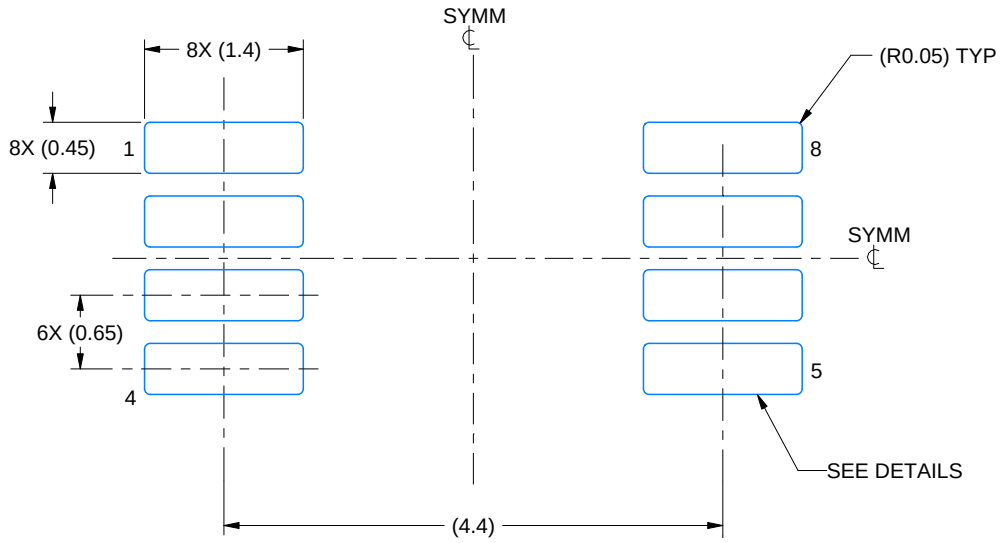
SMALL OUTLINE PACKAGE



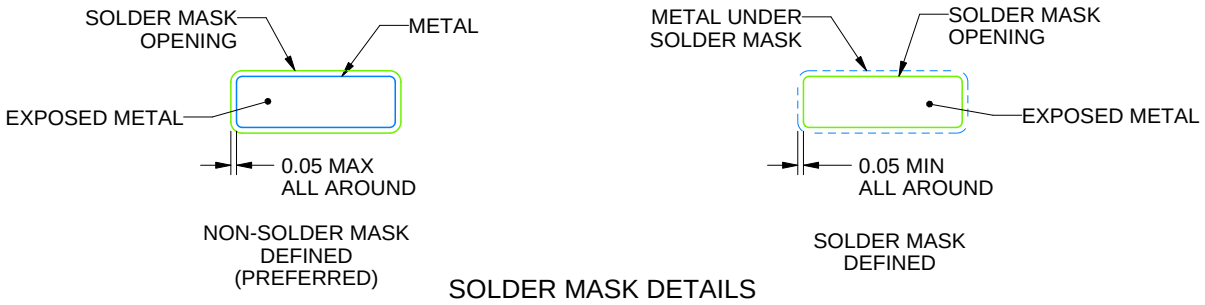
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

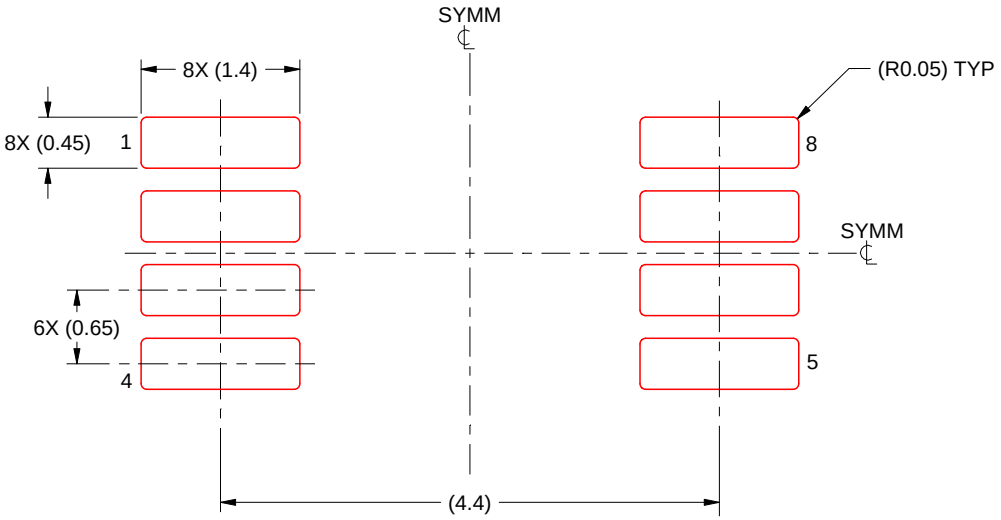


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

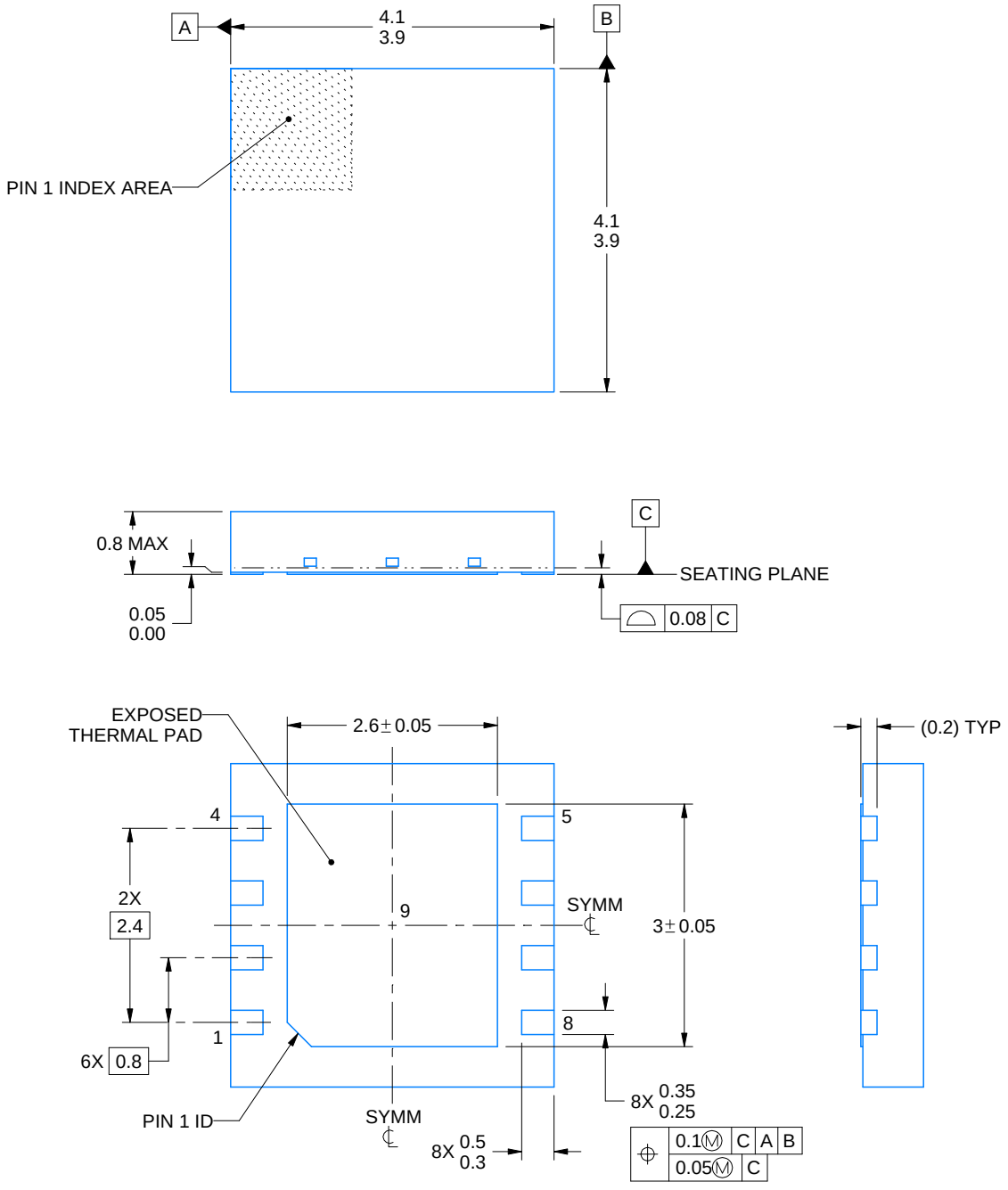
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

NGT0008A

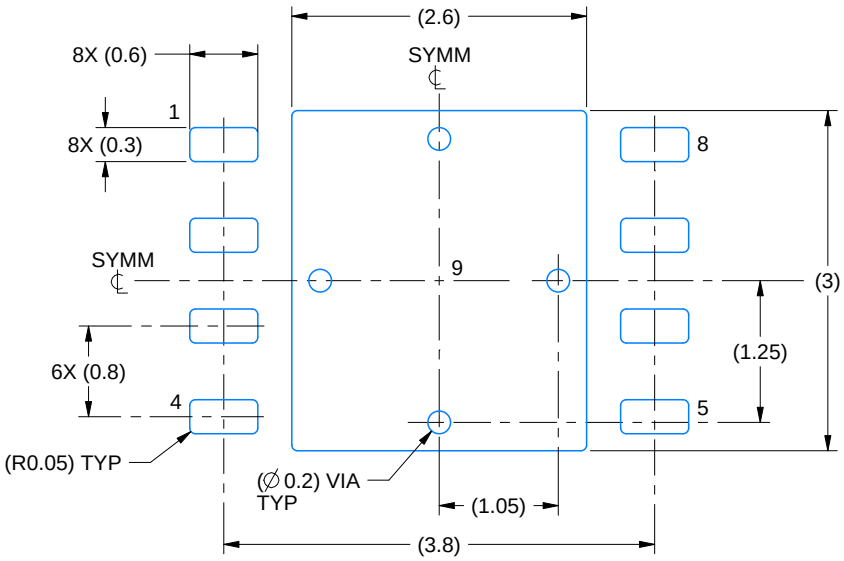
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

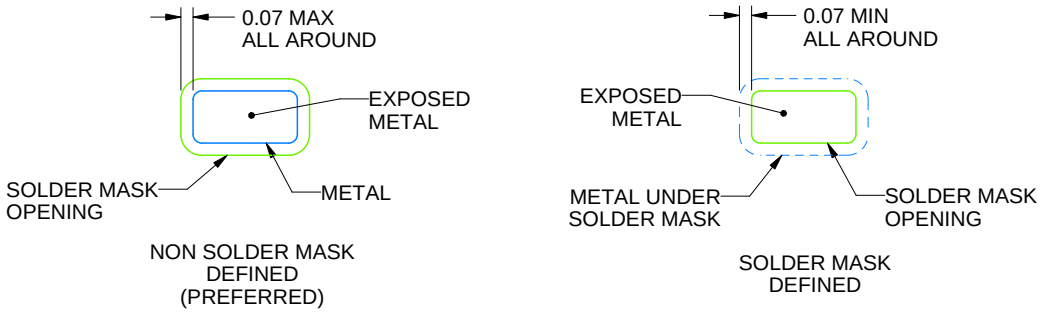


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

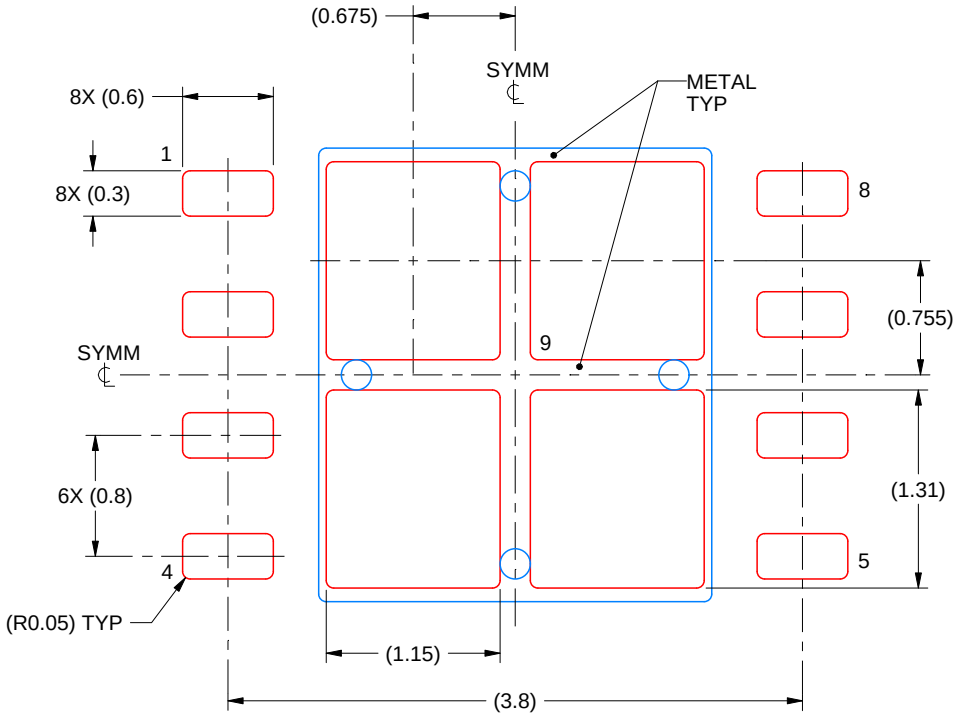


SOLDER MASK DETAILS

4214935/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214935/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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