LM3686 Step-Down DC-DC Converter With Integrated Post Linear Regulators System And Low-Noise Linear Regulator

1 Features

- DC-DC Regulator
  - V_{OUT_DCDC} = 1.2 V to 2.5 V
  - 600-mA Maximum I_{LOAD}
  - 3-MHz Typical PWM Fixed Switching Frequency
  - Automatic PFM/PWM Mode Switching
  - Internal Synchronous Rectification
  - Internal Soft Start
- Dual-Rail Linear Regulator: LILO
  - Load Transients < 50-mV Peak Typical
  - Line Transients < 1-mV Peak Typical
  - V_{OUT_LILO} = 0.7 V to 2 V
  - 70-µA Typical I_Q and 300-mA Maximum I_{LOAD}
- Linear Regulator: LDO
  - Load Transients < 80-mV Peak Typical
  - Line Transients < 1-mV Peak Typical
  - V_{OUT_LDO} = 1.5 V to 3.3 V
  - 50-µA Typical I_Q and 350-mA Maximum I_{LOAD}
- Combined Global Features
  - V_{BATT} ≥ Maximum (V_{OUT_LILO} + 1.5 V, 2.7 V)
  - Operates From a Single Li-Ion Cell or 3-Cell NiMH/NiCd Batteries
  - 100-µA I_Q and 900-mA Maximum I_{LOAD}

2 Applications

- Mobile TVs, Hand-Held Radios
- Personal Digital Assistants, Palm-Top PCs
- Portable Instruments and Personal Clients
- Battery-Powered Devices

3 Description

The LM3686 is a step-down DC-DC converter with a very low-dropout linear regulator and a low-noise linear regulator optimized for powering ultra-low voltage circuits. It provides three outputs with combined load current up to 900 mA over an input voltage range from 2.7 V to 5.5 V.

The device offers superior features and performance for many applications. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved system control. During full-power operation, a fixed-frequency 3 MHz (typical), PWM mode drives loads from approximately 70 mA to 600 mA maximum. Hysteretic PFM mode extends the battery life through reduction of the quiescent current to 28 µA (typical) at light load and system standby. Internal synchronous rectification provides high efficiency.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3686	DSBGA (12)	2.435 mm × 1.687 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

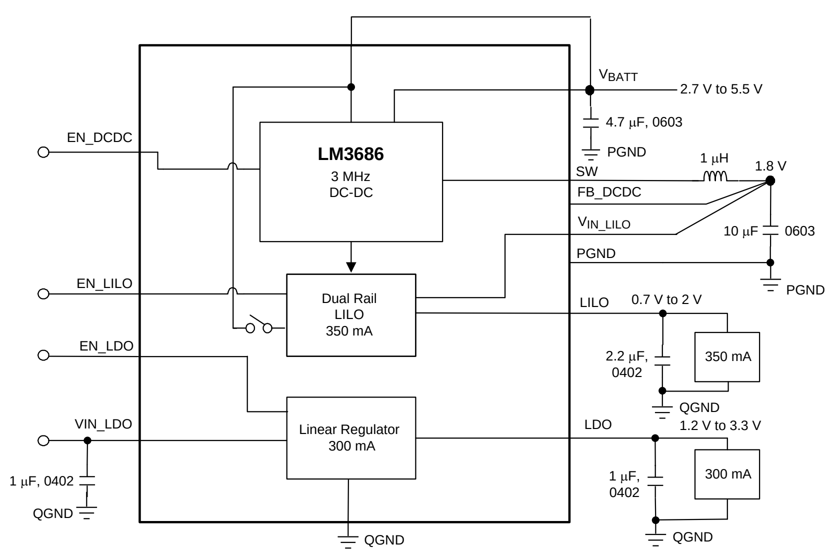


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (May 2013) to Revision F — **Page**

- Deleted "one integrated" ... 1
- Deleted "from a single Li-Ion cell or 3-cell NiMH/NiCd batteries." ... 1
- Added *Device Information* and *ESD Ratings* tables, *Pin Configuration and Functions*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Combine some bullet items and delete parentheticals from *Features* to get more space ... 1
- Deleted out-of-date *Device Comparison* table ... 3
- Deleted lead temperature from *Abs Max* per TI data sheet standard ... 4
- Changed $R_{\theta JA}$ from "120°C/W" to "80.9°C/W"; added additional thermal values ... 4
- Changed "drains conductor" to "drains inductor" on Figure 13 ... 14

Changes from Revision D (April 2013) to Revision E — **Page**

- Changed layout of National Semiconductor data sheet to TI format ... 22

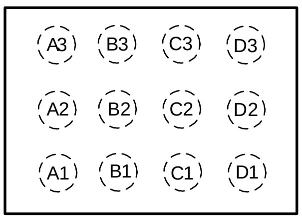
5 Description (Continued)

Three enable (EN_x) pins allow the separate operation of either the DC-DC, post-regulation linear regulator, or the linear regulator alone. If the DC-DC is not enabled during start-up of the post-regulation linear regulator, a parallel small-pass transistor supplies the linear regulator from V_{BATT} with maximal 50 mA. In the combined operation where both enables are raised together, the small-pass transistor is deactivated and the big pass transistor provides 350 mA output current. In shutdown mode (EN_x pins pulled low), the device turns off and reduces battery consumption to 2.5 µA (typical).

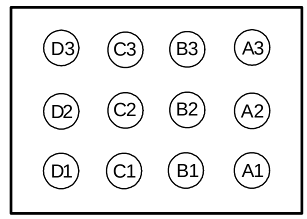
The LM3686 is available in a 12-pin DSBGA package. A high-switching frequency of 3 MHz (typical) allows the use of a few tiny surface-mount components. Only six external surface-mount components, an inductor and five ceramic capacitors, are required to establish a 15.66 mm^2 total solution size.

6 Pin Configuration and Functions

YZR Package
12-Pin DSBGA
Top View



YZR Package
12-Pin DSBGA
Bottom View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	PGND	Ground	Power ground pin
A2	SW	Analog	Switching node connection to the internal PFET switch and NFET synchronous rectifier.
A3	FB_DCDC	Input	Feedback analog input for the DC-DC converter. Connect to the output filter capacitor.
B1	V_{BATT}	Power	Power supply input for switcher. Connect to the input filter capacitor.
B2	EN_LILO	Input	Enable input for the linear regulator. The linear regulator is in shutdown mode if voltage at this pin is < 0.4 V and enabled if > 1.1 V. Do not leave this pin floating.
B3	EN_DCDC	Input	Enable input for the DC-DC converter. The DC-DC converter is in shutdown mode if voltage at this pin is < 0.4 V and enabled if > 1.1 V. Do not leave this pin floating.
C1	V_{IN_LDO}	Input	Input power to LDO — must tie to V_{BATT} at all times.
C2	EN_LDO	Input	Enable input for the linear regulator. The linear regulator is in shutdown mode if voltage at this pin is < 0.4 V and enabled if > 1.1 V. Do not leave this pin floating.
C3	QGND	Ground	Quiet GND pin for LDO and reference circuit
D1	V_{OUT_LDO}	Output	Voltage output of the linear regulator
D2	V_{OUT_LILO}	Output	Voltage output of the low input linear regulator
D3	V_{IN_LILO}	Input	Input power to LILO (V_{IN_LILO}) connects to output of DCDC or standalone.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)(4)

	MIN	MAX	UNIT
V_{BATT} pin to GND and QGND	–0.2	6	V
EN_x pins, FB_DC-DC pin, SW pin	(GND – 0.2 V) to (V_{BATT}+0.2 V) with 6 V maximum		
Continuous power dissipation(5)	Internally limited		
Junction temperature, $T_{J\text{-}MAX}$		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) For detailed soldering specifications and information, see *AN-1112 DSBGA Wafer Level Chip Scale Package*.
(5) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 130°C (typical).

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage, V_{BATT} (DC-DC and LDO)	2.7	5.5	V
Junction temperature, T_J	–40	125	°C
Ambient temperature, T_A(1)	–40	85	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

7.4 Thermal Information

THERMAL METRIC(1)		LM3686 YZR (DSBGA) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.9	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

7.5 Electrical Characteristics: Linear Regulator - LILO

Unless otherwise noted, limits apply for T_A = 25°C, specifications apply to the closed-loop typical application circuits (linear regulator) with V_{IN_LDO} = V_{BATT} = 3.6 V[(1)] , V_{IN_LILO} = $V_{OUT\_DCDC(NOM)}$, V_{EN} (All) = V_{BATT}, C_{IN_DC} = 4.7 µF, C_{OUT_LILO} = 2.2 µF, C_{IN_LDO} = 1 µF , C_{OUT_LDO} = 1 µF, C_{OUT_DC} = C_{IN_LILO} = 10 µF.[(2)(3)(4)(5)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_DC-DC = EN_LILO = ON – LARGE NMOS						
ΔV_{OUT_LILO}, V_{OUT_LILO}	Output voltage accuracy, $V_{OUT-LILO}$	I_{OUT_LILO} = 1 mA to 350 mA, V_{IN_LILO} = V_{OUT_DCDC} V_{BATT} = 3.6 V		1.2		V
		I_{OUT_LILO} = 1 mA to 350 mA, V_{IN_LILO} = V_{OUT_DCDC} V_{BATT} = 3.6 V, –40°C ≤ T_A = T_J ≤ 85°C	1.176		1.224	
ΔV_{OUT_LILO} / ΔmA	Load regulation[(6)]	I_{OUT_LILO} = 1 mA to 350 mA, V_{IN_LILO} = V_{OUT_DCDC} V_{BATT} = 3.6 V		4		µV/mA
		I_{OUT_LILO} = 1 mA to 350 mA, V_{IN_LILO} = V_{OUT_DCDC} V_{BATT} = 3.6 V, –40°C ≤ T_A = T_J ≤ 85°C			12	
V_{DROP}	Dropout voltage[(7)]	V_{BATT} = V_{OUT_LILO} + 1.5 V (V_{IN_LILO} disconnected from V_{OUT_DCDC}) I_{OUT} = 350 mA		50		mV
		V_{BATT} = V_{OUT_LILO} + 1.5 V (V_{IN_LILO} disconnected from V_{OUT_DCDC}) I_{OUT} = 350 mA, –40°C ≤ T_A = T_J ≤ 85°C			80	
$I_{Q\_VIN\_LILO}$	Quiescent current	V_{BATT} = V_{IN_LILO} = 3.6 V		70		µA
		V_{BATT} = V_{IN_LILO} = 3.6 V –40°C ≤ T_A = T_J ≤ 85°C			90	
I_{SC_LILO}	Short-circuit current limit	V_{OUT} = GND (V_{OUT_LILO} = 0) –40°C ≤ T_A = T_J ≤ 85°C	400			mA
EN_DC-DC = OFF, EN_LILO = ON – SMALL NMOS						
ΔV_{OUT_LILO}, V_{OUT_LILO}	Output voltage accuracy V_{OUT_LILO}	I_{OUT} = 1 mA to 50 mA –40°C ≤ T_A = T_J ≤ 85°C	1.176		1.224	V
ΔV_{OUT_LILO}, ΔV_{BATT}	Line regulation (small NMOS)[(8)]	V_{IN_LILO} = (V_{OUT_LILO} + 0.3 V) to 5.5 V		0.4		mV/V
		V_{IN_LILO} = (V_{OUT_LILO} + 0.3 V) to 5.5 V –40°C ≤ T_A = T_J ≤ 85°C			1.5	
I_{SC_LILO}	Short-circuit current	V_{OUT_LILO} = GND, –40°C ≤ T_A = T_J ≤ 85°C	70			
$T_{STARTUP}$	Start-up time	EN to 0.95 V_{OUT}		70		µs

(1) V_{IN_LDO} must be ON at all time for biasing internal reference circuits.
(2) All voltages are with respect to the potential at the GND pin.
(3) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{BATT} = 3.6 V and T_A = 25°C.
(4) The parameters in the electrical characteristic table are tested at V_{BATT} = 3.6 V unless otherwise specified. For performance over the input voltage range refer to *Typical Characteristics*.
(5) The input voltage ranges recommended for ideal application performance for the specified output voltages are:
V_{BATT} = 2.7 V to 5.5 V for 1 V ≤ V_{OUT_DCDC} < 1.8 V
V_{BATT} = (V_{OUT_DCDC} + 1 V) to 5.5 V for 1.8 V ≤ V_{OUT_DCDC} < 3.6 V.
(6) To calculate the output voltage from the load regulation specified, use the following equation:
ΔV_{OUT} = load regulation (%/mA) × nominal V_{OUT} (V) × ΔI_{OUT} (mA).
(7) Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100 mV below the nominal output voltage.
(8) To calculate the output voltage from the line regulation specified, use the following equation:
ΔV_{OUT} = line regulation (%/V) × nominal V_{OUT} (V) × ΔV_{IN} (V).

Electrical Characteristics: Linear Regulator - LILO (continued)

Unless otherwise noted, limits apply for T_A = 25°C, specifications apply to the closed-loop typical application circuits (linear regulator) with V_{IN_LDO} = V_{BATT} = 3.6 V[1] , V_{IN_LILO} = $V_{OUT\_DCDC(NOM)}$, V_{EN} (All) = V_{BATT}, C_{IN_DC} = 4.7 µF, C_{OUT_LILO} = 2.2 µF, C_{IN_LDO} = 1 µF , C_{OUT_LDO} = 1 µF, C_{OUT_DC} = C_{IN_LILO} = 10 µF.[2][3][4][5]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM CHARACTERISTICS[9]						
PSRR	Power supply rejection ratio	Signal to V_{BATT} = 3.6 V, V_{IN_LILO} = 1.8 V, I_{OUT} = 200 mA, f = 100 Hz		68		dB
		Signal to V_{IN_LILO} = 1.8 V, I_{OUT} = 200 mA, f = 100 kHz		60		
e_{N_LILO}	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN_LILO} = 1.8 V, I_{OUT} = 200 mA, V_{IN_LDO} = 3.6 V		166		μV_{RMS}
ΔV_{OUT_LILO}	Dynamic load transient response	Pulsed load 1 mA to 350 mA di/dt = 350 mA / 1 µs		±30[10]		mV
ΔV_{IN_LILO}	Dynamic load transient response on V_{BATT}	V_{BATT} = 3.1 V to 3.7 V V_{IN_LILO} = V_{OUT_DCDC} tr, tf = 10 µs, I_{OUT} = 200 mA		±15[10]		mV

(9) Specified by design. Not production tested.
(10) For line and load transient specifications, the + symbol represents an overshoot in the output voltage and the – symbol represents an undershoot in the output voltage. The first value signifies overshoot or undershoot at the rising edge and the second value signifies the overshoot or undershoot at the falling edge.

7.6 Electrical Characteristics: Linear Regulator - LDO

Unless otherwise noted, limits apply for T_A = 25°C.[1][2][3][4]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN_LDO}	LDO input voltage range		2.7		5.5	V
ΔV_{OUT_LDO} / V_{OUT_LDO}	Output voltage accuracy, $V_{OUT\text{-}LDO}$	V_{IN} = 3.6 V, I_{OUT_LDO} = 1 mA and 300 mA		2.8		V
		V_{IN} = 3.6 V, I_{OUT_LDO} = 1 mA and 300 mA –40°C ≤ T_A = T_J ≤ 85°C	2.744		2.856	
		V_{IN} = 3.6 V, I_{OUT_LDO} = 1 mA and 300 mA		3	3.06	
		V_{IN} = 3.6 V, I_{OUT_LDO} = 1 mA and 300 mA –40°C ≤ T_A = T_J ≤ 85°C	2.94			
ΔV_{OUT_LDO} / ΔmA	Load regulation[5]	I_{OUT_LDO} = 1 mA and 300 mA		8		µV/mA
ΔV_{OUT_LDO} / ΔV_{BATT}	Line regulation[6]	V_{IN_LDO} = ($V_{OUT\_LDO(NOM)}$ + 0.3 V) to 5.5 V		0.2		mV/V
V_{DROP}	Dropout voltage[7]	I_{OUT} = 300 mA		120		mV
		I_{OUT} = 300 mA, –40°C ≤ T_A = T_J ≤ 85°C			200	
I_Q	Quiescent current	V_{en} = 0.95 V, I_{OUT} = 0 mA		50		µA
		V_{en} = 0.95 V, I_{OUT} = 0 mA –40°C ≤ T_A = T_J ≤ 85°C			80	
I_{SC_LDO}	Short-circuit current limit	V_{OUT} = GND, –40°C ≤ T_A = T_J ≤ 85°C	350			mA

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{BATT} = 3.6 V and T_A = 25°C.
(3) The parameters in the *Electrical Characteristics* tables are tested at V_{BATT} = 3.6 V unless otherwise specified. For performance over the input voltage range refer to *Typical Characteristics*.
(4) The input voltage ranges recommended for ideal application performance for the specified output voltages are
V_{BATT} = 2.7 V to 5.5 V for 1 V ≤ V_{OUT_DCDC} < 1.8 V
V_{BATT} = (V_{OUT_DCDC} + 1 V) to 5.5 V for 1.8 V ≤ V_{OUT_DCDC} < 3.6 V
(5) To calculate the output voltage from the load regulation specified, use the following equation:
ΔV_{OUT} = load regulation (%/mA) × nominal V_{OUT} (V) × ΔI_{OUT} (mA)
(6) To calculate the output voltage from the line regulation specified, use the following equation:
ΔV_{OUT} = line regulation (%/V) × nominal V_{OUT} (V) × ΔV_{IN} (V)
(7) Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100 mV below the nominal output voltage.

Electrical Characteristics: Linear Regulator - LDO (continued)

Unless otherwise noted, limits apply for T_A = 25°C.(1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM CHARACTERISTICS(8)						
PSRR	Power supply rejection ratio	EN_DC = EN_LILO = GND I_{OUT} = 200 mA, f = 1 kHz		85		dB
		Signal to V_{IN_LDO} = 3.6 V, I_{OUT} = 200 mA, f = 10 kHz		70		
e_{N_LDO}	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN_LDO} = 3.6 V, I_{OUT} = 200 mA		6.7		µV_{RMS}
ΔV_{IN_LDO}	Dynamic line transient response	V_{IN_LDO} = 3.8 V to 4.4 V tr, tf = 30 µs, I_{OUT} = 1 mA		±2(9)		mV
ΔV_{IN_LILO}	Dynamic load transient response on V_{BATT}	Pulsed load 1 mA and 300 mA tr, tf = 10 µs		±30(9)		mV

(8) Specified by design. Not production tested.
(9) For line and load transient specifications, the + symbol represents an overshoot in the output voltage and the – symbol represents an undershoot in the output voltage. The first value signifies overshoot or undershoot at the rising edge and the second value signifies the overshoot or undershoot at the falling edge.

7.7 Electrical Characteristics: DC-DC Converter

Unless otherwise noted, limits apply for T_A = 25°C.(1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB_DCDC}	Feedback voltage accuracy	PWM mode(5)		1.8		V
		PWM mode(5), –40°C ≤ T_A = T_J ≤ 85°C	1.746		1.836	
V_{REF}	Internal reference voltage			0.5		V
$R_{DSON(P)}$	Pin-pin resistance for PFET	V_{BATT} = 3.6 V I_{SW} = 100 mA		350	450	mΩ
$R_{DSON(N)}$	Pin-pin resistance for NFET	V_{BATT} = 3.6 V I_{SW} = 100 mA		150	250	mΩ
I_{Q_AUTO}	Quiescent current for auto mode	No load, device is not switching, FB = HIGH		28		µA
		No load, device is not switching, FB = HIGH –40°C ≤ T_A = T_J ≤ 85°C			40	
I_{LIM}	Switch peak current limit	Open loop		1.22		A
		Open loop, –40°C ≤ T_A = T_J ≤ 85°C	1.035		1.375	
f_{OSC}	Internal oscillator frequency	PWM mode		3		MHz
		PWM mode, –40°C ≤ T_A = T_J ≤ 85°C	2.4		3.4	

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{BATT} = 3.6 V and T_A = 25°C.
(3) The parameters in the electrical characteristic table are tested at V_{BATT} = 3.6 V unless otherwise specified. For performance over the input voltage range refer to *Typical Characteristics*.
(4) The input voltage ranges recommended for ideal application performance for the specified output voltages are:
V_{BATT} = 2.7 V to 5.5 V for 1 V ≤ V_{OUT_DCDC} < 1.8 V
V_{BATT} = (V_{OUT_DCDC} + 1 V) to 5.5 V for 1.8 V ≤ V_{OUT_DCDC} < 3.6 V
(5) *Electrical Characteristics* tables reflects open loop data (FB = 0 V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

7.8 Electrical Characteristics: Global Parameters (DCDC, LILO, and LDO)

Unless otherwise noted, limits apply for T_A = 25°C.(1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q_VBATT}	Quiescent current into V_{BATT}	Full power mode $I_{OUT\_DCDC} = I_{OUT\_LILO} = I_{OUT\_LDO}$ = 0 mA, DC-DC is not switching (FB_DCDC forced higher than V_{OUT_DCDC}) V_{en} = 1.1V,		100		µA
		Full power mode $I_{OUT\_DCDC} = I_{OUT\_LILO} = I_{OUT\_LDO}$ = 0 mA, DC-DC is not switching (FB_DCDC forced higher than V_{OUT_DCDC}) V_{en} = 1.1V, –40°C ≤ $T_A = T_J$ ≤ 85°C			130	
I_{Q_GLOBAL}	Shutdown current into V_{BATT}	$V_{EN\_DCDC} = V_{EN\_LILO} = V_{EN\_LDO}$ = 0 V		2.5		µA
		$V_{EN\_DCDC} = V_{EN\_LILO} = V_{EN\_LDO}$ = 0 –40°C ≤ $T_A = T_J$ ≤ 85°C			4	
ENABLE PINS (EN_DCDC, EN_LILO, EN_LDO)						
I_{EN}	Enable pin input current	All EN = 0 V		.01		µA
		All EN = 0 V, –40°C ≤ $T_A = T_J$ ≤ 85°C			1	
V_{IH}	Logic high input	–40°C ≤ $T_A = T_J$ ≤ 85°C	1.1			V
V_{IL}	Logic low input	–40°C ≤ $T_A = T_J$ ≤ 85°C			0.4	V

(1) All voltages are with respect to the potential at the GND pin.
(2) Mininum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{BATT} = 3.6 V and T_A = 25°C.
(3) The parameters in the *Electrical Characteristics* tables are tested at V_{BATT} = 3.6 V unless otherwise specified. For performance over the input voltage range refer to *Typical Characteristics*.
(4) The input voltage ranges recommended for ideal application performance for the specified output voltages are:
V_{BATT} = 2.7 V to 5.5 V for 1 V ≤ V_{OUT_DCDC} < 1.8 V
V_{BATT} = (V_{OUT_DCDC} + 1 V) to 5.5 V for 1.8 V ≤ V_{OUT_DCDC} < 3.6 V

7.9 Typical Characteristics

Unless otherwise specified, typical application (post regulation), V_{BATT} = 3.6 V, T_A = 25°C, enable pins tied to V_{BATT}, V_{OUT_DCDC} = 1.8 V, V_{OUT_LILO} = 1.2 V, V_{OUT_LDO} = 2.8 V.

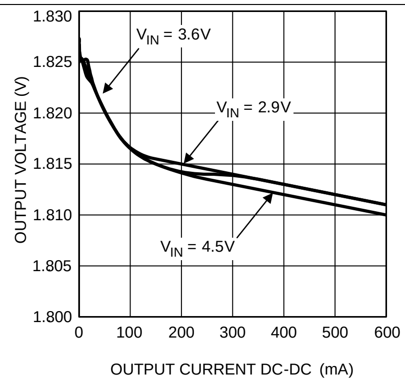


Figure 1. V_{OUT_DCDC} vs I_{OUT_DCDC}

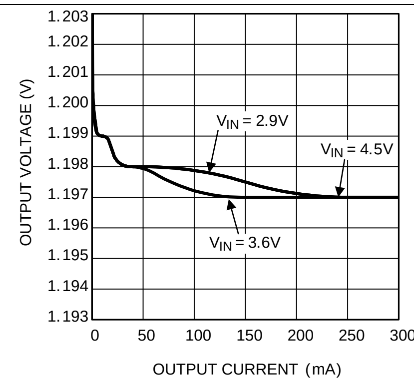


Figure 2. V_{OUT_LILO} vs I_{OUT_LILO}

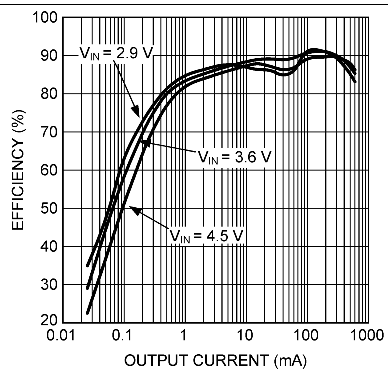
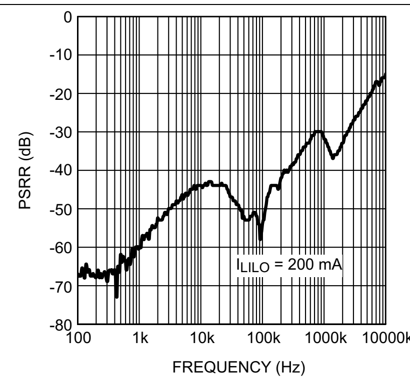
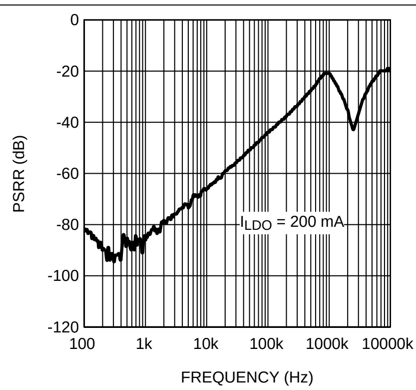


Figure 3. Efficiency DC-DC vs Output Current LILO and LDO Disabled



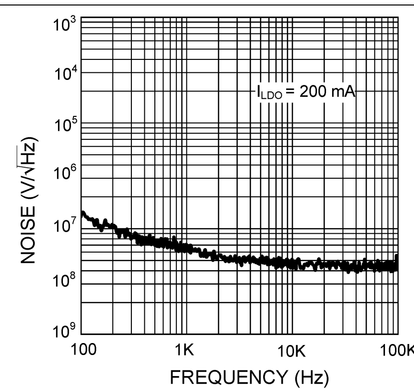
LILO – V_{IN_LILO} = 3.6 V

Figure 4. PSRR vs Frequency



LDO – V_{IN_LDO} = 3.6 V

Figure 5. PSRR vs Frequency



LDO – V_{IN_LDO} = 3.6 V

Figure 6. Noise vs Frequency

Typical Characteristics (continued)

Unless otherwise specified, typical application (post regulation), V_{BATT} = 3.6 V, T_A = 25°C, enable pins tied to V_{BATT}, V_{OUT_DCDC} = 1.8 V, V_{OUT_LILO} = 1.2 V, V_{OUT_LDO} = 2.8 V.

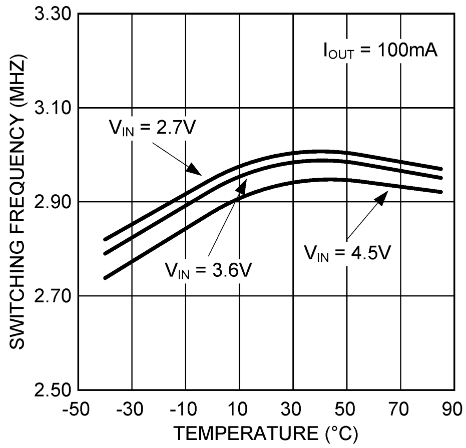
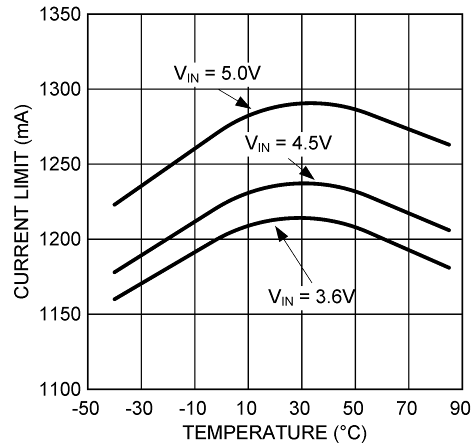


Figure 7. Switching Frequency vs Temperature



Open Loop

Figure 8. Current Limit vs Temperature

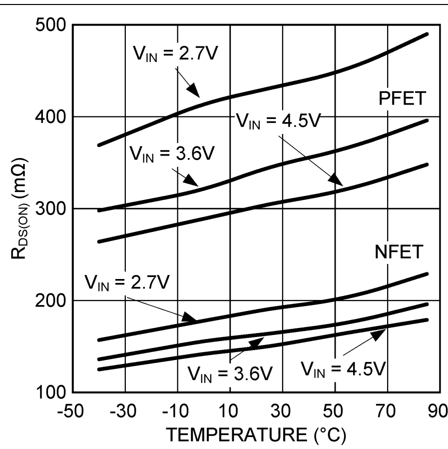
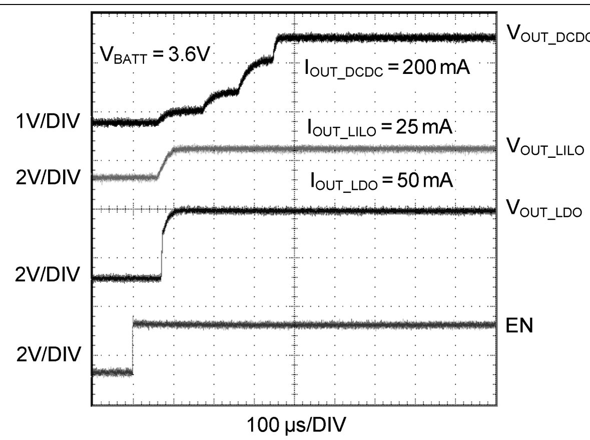


Figure 9. R_{DSON} vs Temperature



All Three Enables Tied Together

Figure 10. Start-up

8 Detailed Description

8.1 Overview

The LM3686 incorporates a high efficiency synchronous switching step-down DC-DC converter, a very low dropout linear regulator (LILO), and ultra-low-noise linear regulator.

The DC-DC converter delivers a constant voltage from a single Li- Ion battery and input voltage rails from 2.7 V to 5.5 V to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, it has the ability to deliver up to 600-mA load current (when not powering the LILO) depending on the input voltage, output voltage, ambient temperature, and the inductor chosen.

The linear regulator delivers a constant voltage biased from V_{IN_LILO} power input typically the output voltage of the DC-DC converter is used (post regulation) with a maximum load current of 350 mA.

The other linear regulator delivers a constant voltage biased from V_{IN_LDO} power input with a maximum load current of 300 mA.

Three enable pins allow the independent control of the three outputs. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 2.5 µA typical).

Besides the shutdown feature, there are two more modes of operation for the DC-DC converter, depending on the current required:

- Pulse width modulation (PWM) and
- Pulse frequency modulation (PFM).

The device operates in PWM mode at load current of approximately 80 mA or higher. Lighter load current cause the device to automatically switch into PFM for reduced current consumption (I_{Q_VBATT} = 28 µA typical) and a longer battery life.

Additional features include soft-start, start-up mode of the linear regulator, undervoltage protection, current overload protection, and overtemperature protection.

An internal reference generates a 1.8-V biasing an internal resistive divider to create a reference voltage range from 0.7 V to 1.8 V (in 50-mV steps) for the LILO and the 0.5-V reference used for the DC-DC converter. The ultra-low-noise linear regulator also has internal reference that generates a 1.8-V biasing for a internal resistor divider, thus creating a reference voltage ranging from 1.5 V to 3.3 V.

The undervoltage lockout feature enables the device to start-up once V_{BATT} has reached 2.65 V typically and turns the device off if V_{BATT} drops below 2.41 V typically.

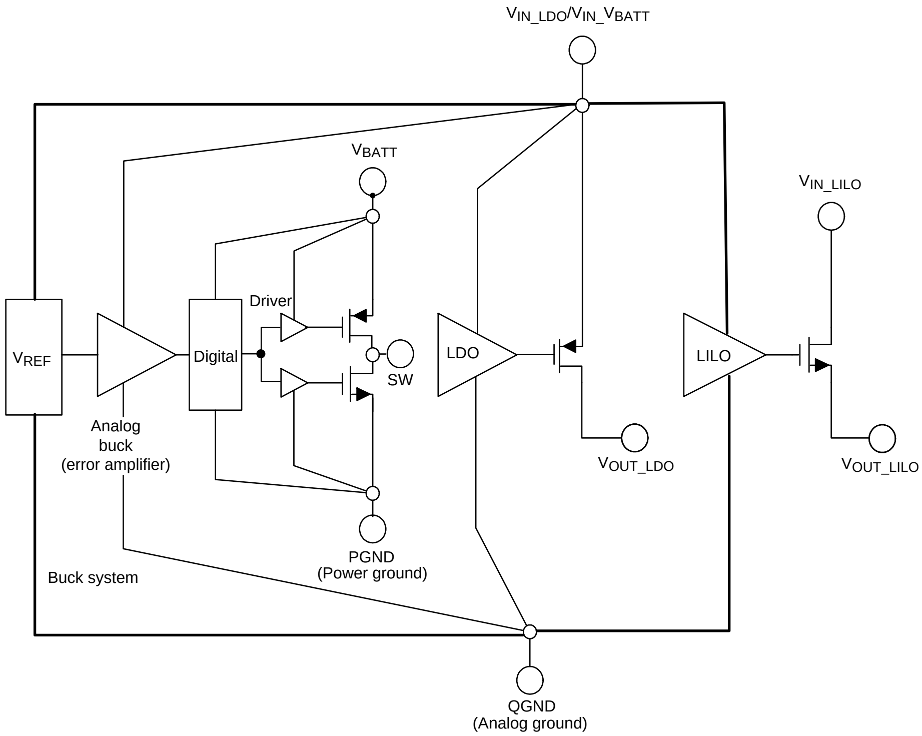
NOTE

Post regulation: When the DC-DC converter is switched off while the linear regulator is still enabled, the LILO can still support up to 50 mA. The linear regulator LILO is turned on via a small NMOS device supplied by V_{IN_LDO} . The maximum current is 50 mA when this small NMOS is ON. If higher current > 50 mA is desired the following condition must be met:

- EN_DC = HIGH

When the condition is met, the LILO transitions to the large NMOS and can support up to 350 mA.

8.2 Functional Block Diagram



Always connect V_{IN_LDO} to V_{BATT}.

8.3 Feature Description

8.3.1 DC-DC Converter Operation

During the first part of each switching cycle, the control block in the LM3686 turns on the internal PFET switch. This allows current to flow from the input V_{BATT} through the switch pin SW and the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{BATT} – V_{OUT\_DCDC})$ / L, by storing energy in the magnetic field.

During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $(– V_{OUT\_DCDC}$ / L).

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

Feature Description (continued)

8.3.1.1 PWM Operation

During pulse width modulation (PWM) operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependency, feed forward inversely proportional to the input voltage is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the duty-cycle comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

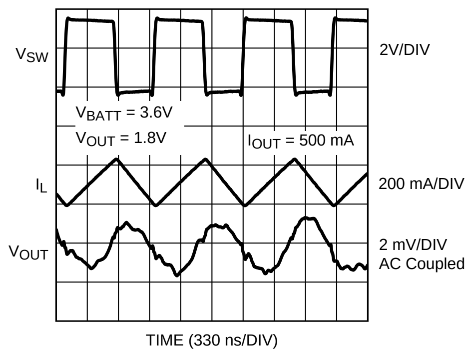


Figure 11. Typical PWM Operation

8.3.1.2 PFM Operation

At very light load, the DC-DC converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency. The part automatically transitions into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The NFET current reaches zero.
2. The peak PMOS switch current drops below the I_{MODE} level, (typically I_{MODE} < 75 mA + V_{BATT} / 55 Ω).

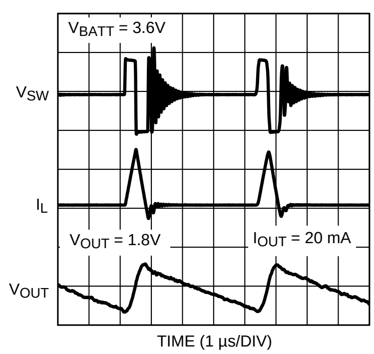


Figure 12. Typical PFM Operation

Feature Description (continued)

During PFM operation, the DC-DC converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between approximately 0.2% and approximately 1.8% above the nominal PWM output voltage. If the output voltage is below the high PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the high PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is: I_{PFM} = 112 mA + V_{BATT} / 20 Ω.

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the high PFM comparator threshold (see Figure 13), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the high PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero. Both output switches are then turned off, and the device enters an extremely low power mode. Quiescent supply current during this sleep mode is 28 µA (typical), which allows the part to achieve high efficiency under extremely light load conditions.

If the load current should increase during PFM mode (see Figure 13) causing the output voltage to fall below the low2 PFM threshold, the part automatically transitions into fixed-frequency PWM mode.

When V_{BATT} = 2.7 V the device transitions from PWM to PFM mode at approximately 35 mA output current and from PFM mode to PWM mode at approximately 95 mA. When V_{BATT}= 3.6 V, PWM-to-PFM transition happens at approximately 42 mA and PFM-to-PWM transition happens at approximately 115 mA. When V_{BATT} = 4.5 V, PWM-to-PFM transition happens at approximately 60 mA and PFM-to-PWM transition happens at approximately 135 mA.

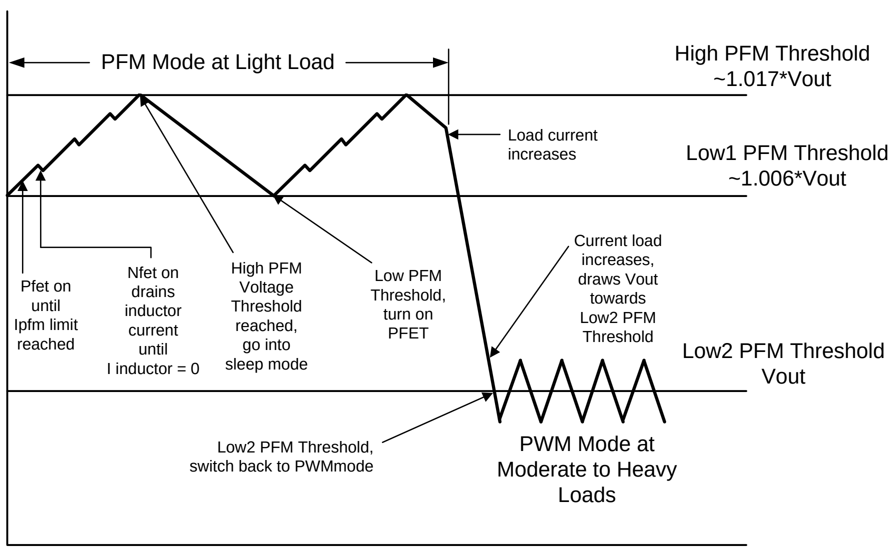


Figure 13. Operation In PFM Mode and Transfer to PWM Mode

8.3.1.3 Internal Synchronous Rectification

While in PWM mode, the DC-DC converter uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Feature Description (continued)

8.3.1.4 Current Limiting

A current limit feature allows the LM3686 to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1220 mA (typical). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold. This allows the inductor current more time to decay, thereby preventing runaway.

8.3.1.5 Soft Start

The DC-DC converter has a soft-start circuit that limits in-rush current during start-up. During start-up the switch-current limit is increased in steps. Soft start is activated only if EN_DCDC goes from logic low to logic high after V_{BATT} reaches 2.7 V. Soft start is implemented by increasing switch current limit in steps of 200 mA, 400 mA, 600 mA and 1220 mA (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with a 10 µF output capacitor and 200 mA load is 350 µs and with 1 mA load is 200 µs.

8.3.2 Linear Regulator Operation (LILO)

In a typical post-regulation application the power input voltage V_{IN_LILO} for the linear regulator is generated by the DC-DC converter. Using a buck converter to reduce the battery voltage to a lower input voltage for the linear regulator translates to higher efficiency and lower power dissipation.

It is also possible to operate the linear regulator independent of the DC-DC converter output voltage either from $V_{IN\_LDO/}V_{BATT}$ or from a different source (V_{IN_LILO}) – (I_{OUT_LILO} = 50 mA maximum in independent mode).

An input capacitor of 1 µF at V_{IN_LILO} is needed to be added if no other filter or bypass capacitor is present in the V_{IN_LILO} path.

8.3.2.1 Start-up Mode

If $V_{IN\_LILO} > V_{OUT\_LILO(NOM)}$ + 250 mV the main regulator is active, offering a rated output current of 350 mA and supplied by V_{IN_LILO} (large NMOS).

If $V_{IN\_LILO} < V_{OUT\_LILO(NOM)}$ + 150 mV the start-up LILO is active, providing a reduced rated output current of 50 mA typical, supplied by V_{BATT} (small NMOS).

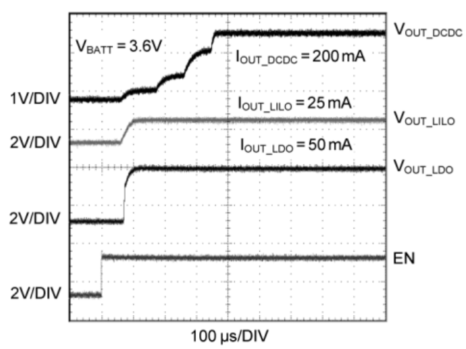


Figure 14. Start-Up Sequence, $V_{EN\_DCDC} = V_{EN\_LILO} = V_{EN\_LDO} = V_{BATT}$

8.3.3 Current Limiting (LDO and LILO)

The LM3686 incorporates also a current limit for the LDO and LILO to protect itself and external components during overload conditions at their outputs. In the event of a peak overcurrent condition at V_{OUT_LDO} or V_{OUT_LILO} , the output current through the NFET pass device is limited.

8.4 Device Functional Modes

Table 1. Enable Combinations

EN_DCDC	EN_LILO	EN_LDO	FUNCTION
0	0	0	No outputs
0	0	1	Linear regulator enabled only (EN_LDO), supply from V_{IN_LDO}, I_{OUT_MAX} = 300 mA
0	1	0	Linear regulator enabled only LILO supplies from V_{IN_LDO}, I_{OUT_MAX} = 50 mA, V_{IN_LDO} > = V_{OUT_LILO}
1	0	0	DC-DC converter enabled only
1	1	0	Linear regulator and DC-DC enabled 1. V_{IN_LILO} < V_{OUT_LILO} + 150 mV (typical), the small NMOS device is active (I_{MAX} = 50 mA) and supplied by V_{IN_LDO}. 2. If V_{IN_LILO} > V_{OUT_LILO} + 250 mV (typical), the large NMOS device is active (I_{MAX} = 350 mA) and supplied by V_{IN_LILO}. Maxium current of DC-DC when EN_LILO = High is 250 mA(1)(2)
1	1	1	DC-DC converter and linear regulator active. Linear regulator starts after DC-DC converter.

(1) The LILO is turned on via a small NMOS device supplied by V_{IN_LDO} . The maximum current is 50 mA when this small NMOS is ON. If higher current > 50 mA is desired this condition must be done: EN_DC = HIGH .
(2) When the switcher is enabled, a transition occurs from the small NMOS to a larger NMOS. The transition occurs when V_{IN_LILO} > V_{OUT_LILO} + 250 mV. If V_{IN_LILO} < V_{OUT_LILO} + 150 mV, the LILO switches back to small NMOS (switcher EN = low).

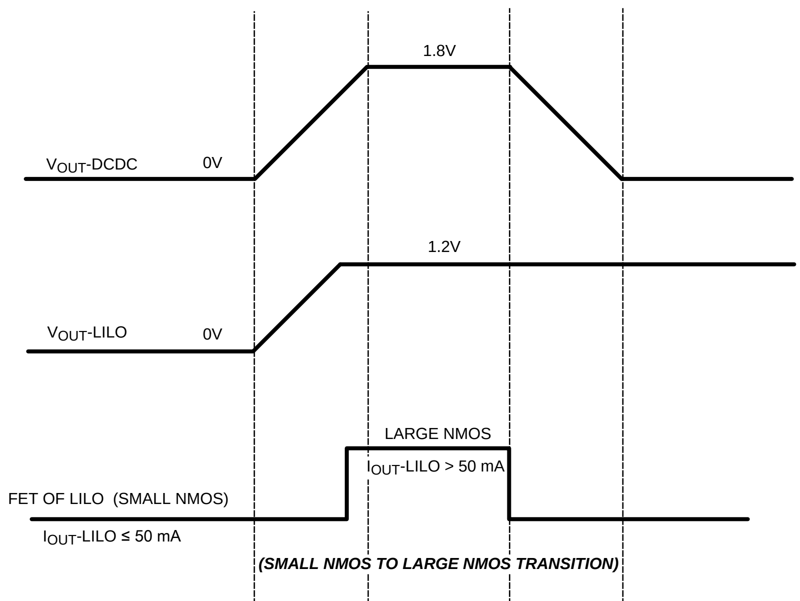


Figure 15. Mode Transition

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM3686 is a step-down DC-DC converter with integrated low-dropout linear regular and a low-noise linear regulator optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3-cell NiMH/NiCd batteries. It provides three outputs with combined load current up to 900 mA over an input-voltage range from 2.7 V to 5.5 V.

9.2 Typical Application

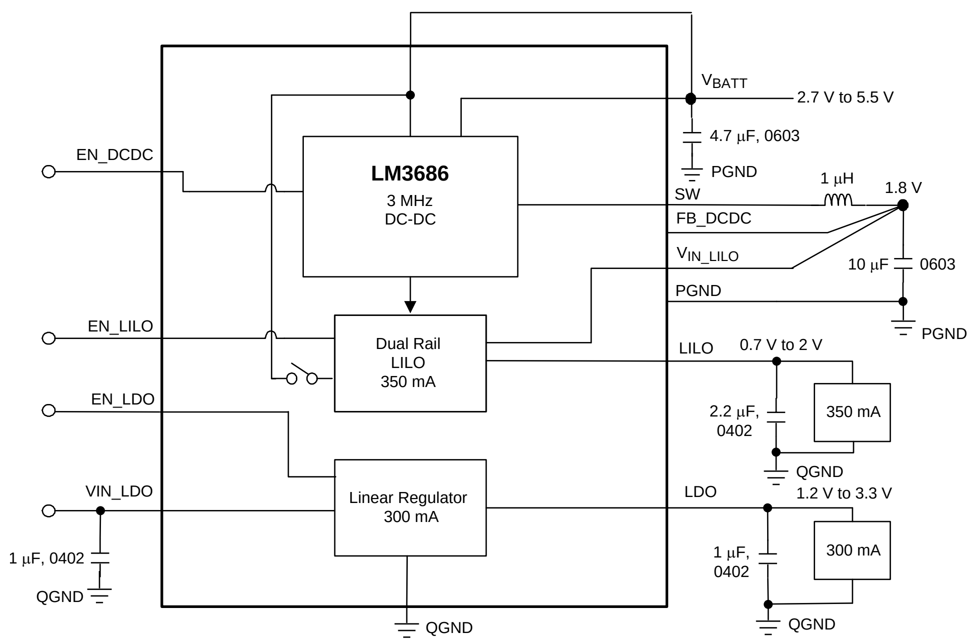


Figure 16. LM3686 Typical Application

9.2.1 Design Requirements

For typical step-down DC-DC converter applications, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.7 V to 5.5 V
Output voltage	1.8 V
Output current	100 mA
Minimum switching frequency	2.55 MHz
RMS noise, 10 Hz to100 kHz	166 μV_{RMS}
PSRR at 100 kHz	60 dB

9.2.2 Detailed Design Procedure

9.2.2.1 Application Selection

TI strongly recommends selection of the required components for the LM3686 device as described within the data sheet. If other components are selected, the device will not perform up to standards, and electrical characteristics cannot be ensured.

9.2.2.2 Inductor Selection

There are two main considerations when choosing an inductor: the inductor must not saturate, and the inductor current ripple must be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. *The minimum value of inductance to ensure good performance is 0.7 µH at* I_{LIM} *(typical) DC current over the ambient temperature range.* Shielded inductors radiate less noise and are preferred. There are two methods to choose the inductor saturation current rating.

9.2.2.2.1 Method 1

The saturation current must be greater than the sum of the maximum load current and the worst case average-to-peak inductor current. This can be written as:

$$I_{SAT} > I_{OUT\_DCDC\_MAX} + I_{RIPPLE} \quad (1)$$

where

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{BATT} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{BATT}}\right) \times \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: average-to-peak inductor current
- $I_{OUT\_DCDCMAX}$: maximum load current (600 mA)
- V_{BATT}: maximum input voltage in application
- L: minimum inductor value including worst case tolerances (30% drop can be considered for *Method 1*)
- f: minimum switching frequency (2.55 MHz) (2)

9.2.2.2.2 Method 2

A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 1375 mA.

A 1-µH inductor with a saturation current rating of at least 1375 mA is recommended for most applications. Resistance of the inductor must less than 0.3 Ω for good efficiency. Table 3 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded- bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

Table 3. Suggested Inductors and Their Suppliers

MODEL	VENDOR	DIMENSIONS L × W × H (mm)	DCR (maximum)
BRL2518T1R0M	TAIYO YUDEN	2.5 × 1.8 × 1.2	80
MDT2520CR1R0M	TOKO	2.5 × 2.0 × 1.0	80
KSLI252010AG1R0	HITACHI METALS	2.5 × 2.0 × 1.0	75

9.2.2.3 External Capacitors

As common with most regulators, the LM3686 requires external capacitors to ensure stable operation. The LM3686 is specifically designed for portable applications requiring minimum board space and the smallest size components. These capacitors must be correctly selected for good performance.

9.2.2.4 Input Capacitor Selection

9.2.2.4.1 $C_{IN\_DC\text{-}DC}$

A ceramic input capacitor of 4.7 µF, 6.3 V is sufficient for most applications. Place the input capacitor as close as possible to the V_{BATT} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The minimum input capacitance to ensure good performance is 2.2 µF at 3-V DC bias; 1.5 µF at 5-V DC bias including tolerances and over ambient temperature range. The input filter capacitor supplies current to the PFET switch of the LM3686 DC-DC converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. The low ESR of a ceramic capacitor provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} \times \sqrt{\frac{V_{OUT}}{V_{BATT}} \times \left(1 - \frac{V_{OUT}}{V_{BATT}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{BATT} - V_{OUT}) \times V_{OUT}}{L \times f \times I_{OUTMAX} \times V_{BATT}}$$

The worst case is when $V_{BATT} = 2 \times V_{OUT}$ (3)

9.2.2.4.2 C_{IN_LILO}

If the LILO is used as post regulation no additional capacitor is needed at V_{IN_LILO} as the output filter capacitor of the DC-DC converter is close by and therefore sufficient.

In case of independent mode use, a 1-µF ceramic capacitor is recommended at V_{IN_LILO} if no other filter capacitor is present in the V_{IN_LILO} supply path. This capacitor must be located a distance of not more than 1 cm from the V_{IN_LILO} input pin and returned to Q_{GND}.

9.2.2.4.3 C_{IN_LDO}

An input capacitor is required for stability. TI recommends using a 1-µF ceramic capacitor and connected between the V_{IN_LDO} and QGND.

9.2.2.5 Output Capacitor

9.2.2.5.1 C_{OUT_DCDC}

A ceramic output capacitor of 10 µF, 6.3 V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process.

The minimum output capacitance to ensure good performance is 5.75 µF at 1.8-V DC bias including tolerances and over ambient temperature range. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low equivalent series resistance (ESR) to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and by the R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as:

$$V_{PP\text{-}C} = \frac{I_{RIPPLE}}{4 \times f \times C} \quad (4)$$

Voltage peak-to-peak ripple due to ESR can be expressed as:

$$V_{PP\text{-}ESR} = (2 \times I_{RIPPLE}) \times R_{ESR} \quad (5)$$

Because these two components are out of phase, the root mean squared (RMS) value can be used to get an approximate value of peak-to-peak ripple. The peak-to-peak ripple voltage, RMS value can be expressed as:

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^{\,2} + V_{PP\text{-}ESR}^{\,2}} \tag{6}$$

Note that the output voltage ripple is dependent on the inductor current ripple and the ESR of the output capacitor (R_{ESR}). The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

9.2.2.5.2 C_{OUT_LILO}

The linear regulator is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X7R, Z5U, or Y5V) in the 2.2-µF range (up to 10 µF) and with an ESR between 3 mΩ to 300 mΩ is suitable as C_{OUT_LIN} in the LM3686 application circuit.

This capacitor must be located a distance of not more than 1 cm from the V_{OUT_LILO} pin and returned to a clean analog ground. Tantalum or film capacitors may also be used at the device output, V_{OUT_LILO} but these are not as attractive for reasons of size and cost (see Table 4).

9.2.2.5.3 C_{OUT_LDO}

A ceramic capacitor in the 1-uF to 2.2-uF range, and with ESR between 5 mΩ to 500 mΩ, is suitable for the linear regulator. Connect this output capacitor no more than 1 cm from V_{OUT_LDO} and QGND.

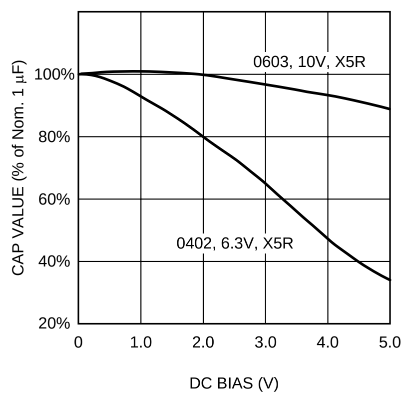


Figure 17. Graph Showing A Typical Variation In Capacitance vs DC Bias

Table 4. Suggested Capacitors and Their Suppliers

CAPACITANCE (µF)	MODEL	VOLTAGE RATING (V)	Vendor	Type	Case Size / Inch (mm)
10	C1608X5R0J106K	6.3	TDK	Ceramic, X5R	0603 (1608)
4.7	C1608X5R0J475	6.3	TDK	Ceramic, X5R	0603 (1608)
2.2	C1608X5R0J225M	6.3	TDK	Ceramic, X5R	0603 (1608)
1	C1005JB0J105KT	6.3	TDK	Ceramic, X5R	0402 (1005)

9.2.3 Application Curves

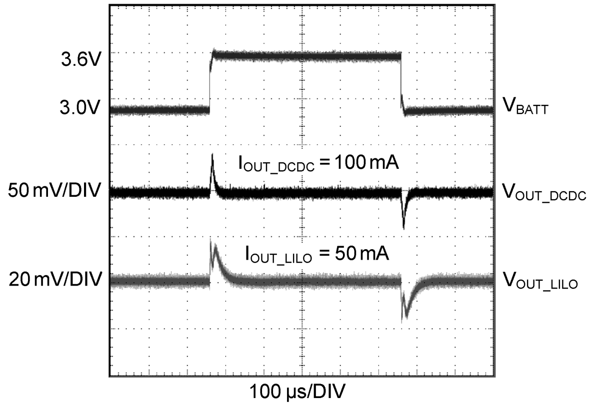


Figure 18. V_{BATT} Line Transient Response

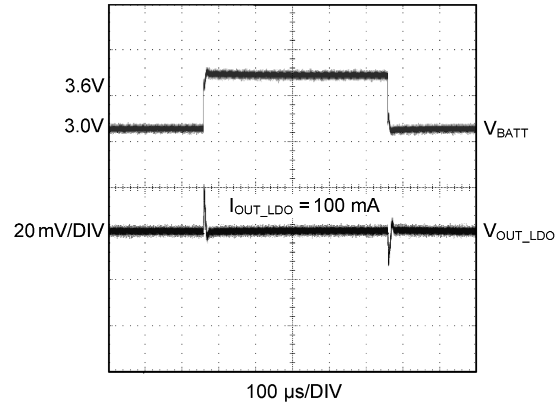
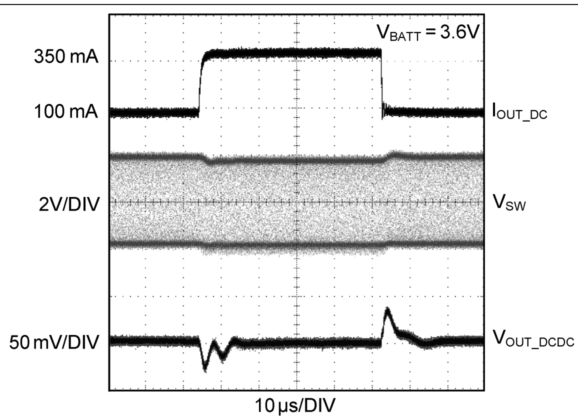
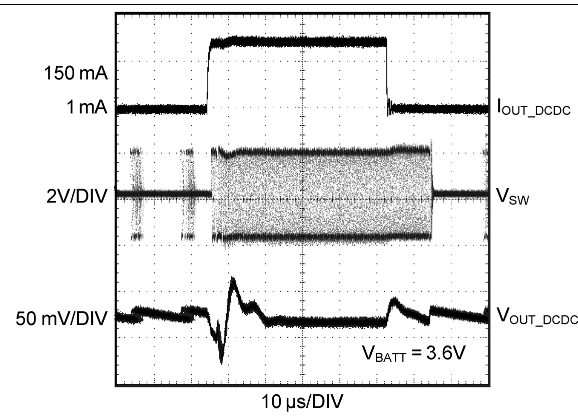


Figure 19. Line Transient Response



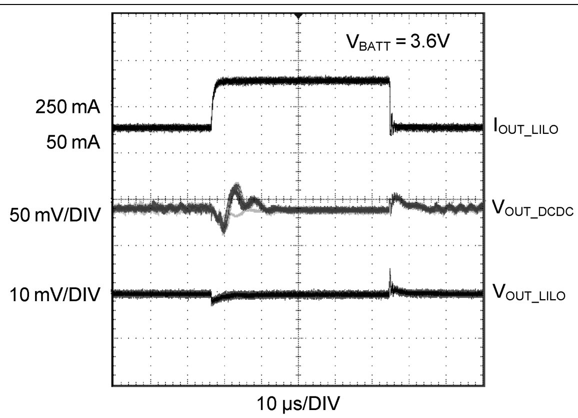
PWM Mode: 100 mA to 350 mA

Figure 20. Load Transient Response DC-DC



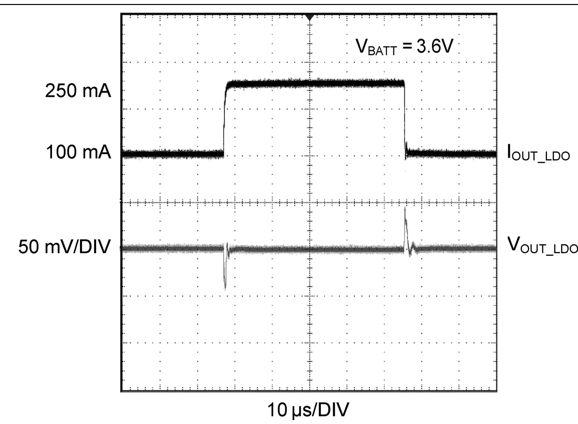
PFM Mode: 1 mA to 150 mA

Figure 21. Load Transient Response DC-DC



LILO 50 mA to 250 mA

Figure 22. Load Transient Response



LDO 100 mA to 250 mA

Figure 23. Load Transient Response

10 Power Supply Recommendations

The LM3686 requires a single supply input voltage. This voltage can range between 2.7 V to 5.5 V and must be able to supply enough current for a given application.

11 Layout

11.1 Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter device, resulting in poor regulation or instability. Implement good layout for the LM3686 by following a few simple design rules:

1. Place the LM3686, inductor,and filter capacitor close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{BATT} and PGND pin. Place the output capacitor of the linear regulator close to the output pin.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor through the LM3686 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LM3686 by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. Connect the ground pins of the LM3686 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3686 by giving it a low impedance ground connection. Route SGND to the ground-plane by a separate trace.
4. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
5. Route noise sensitive traces, such as the voltage feedback path (FB_DCDC), away from noisy traces between the power components. The voltage feedback trace must remain close to the LM3686 circuit, must be direct, and must be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed.
6. Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive pre-amplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal plane; power to it is post-regulated to reduce conducted noise, a good field of application for the on-chip low-dropout linear regulator.

11.2 Layout Example

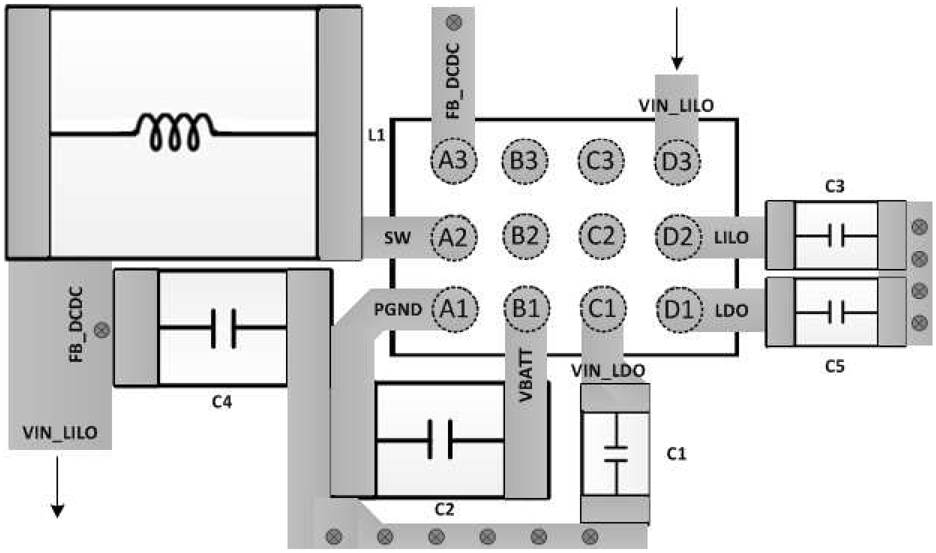


Figure 24. LM3686 Layout

11.3 DSBGA Package Assembly and Use

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in *AN-1112 DSBGA Wafer Level Chip Scale Package*. Refer to the section *Surface Mount Technology (SMD) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board must be used to facilitate placement of the device. The pad style used with DSBGA package must be the non-solder mask defined (NSMD) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See *AN-1112 DSBGA Wafer Level Chip Scale Package* for specific instructions how to do this. The 12-pin package used for LM3686 has 300 micron solder balls and requires 275 micron pads for mounting on the circuit board. The trace to each pad must enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad must not exceed 183 micron, for a section approximately 183 micron long or longer, as a thermal relief —then each trace must neck up or down to its optimal width. The important criteria is symmetry. This ensures the solder bumps on the LM3686 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1 and B1 because PGND and VBATT are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps. The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with frontside shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on the exposed die edges of the package.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Documentation

For additional information, see the following:

AN-1112 DSBGA Wafer Level Chip Scale Package

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3686TLE-AADW/NO.A	Active	Production	DSBGA (YZR) | 12	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SUEB
LM3686TLE-AADW/NOPB	Active	Production	DSBGA (YZR) | 12	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SUEB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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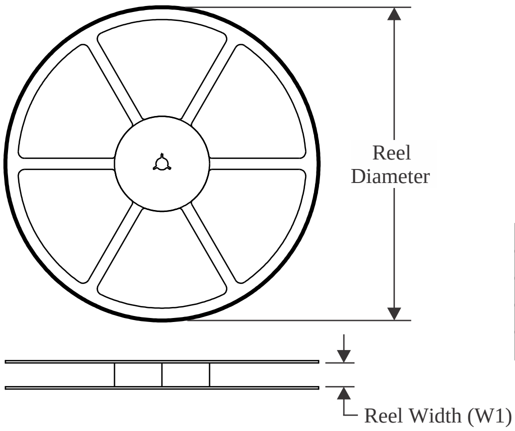
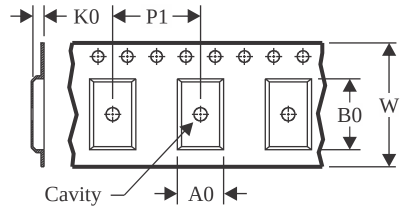
TAPE AND REEL INFORMATION

REEL DIMENSIONS

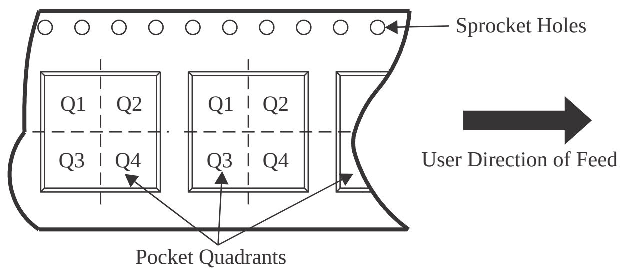


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

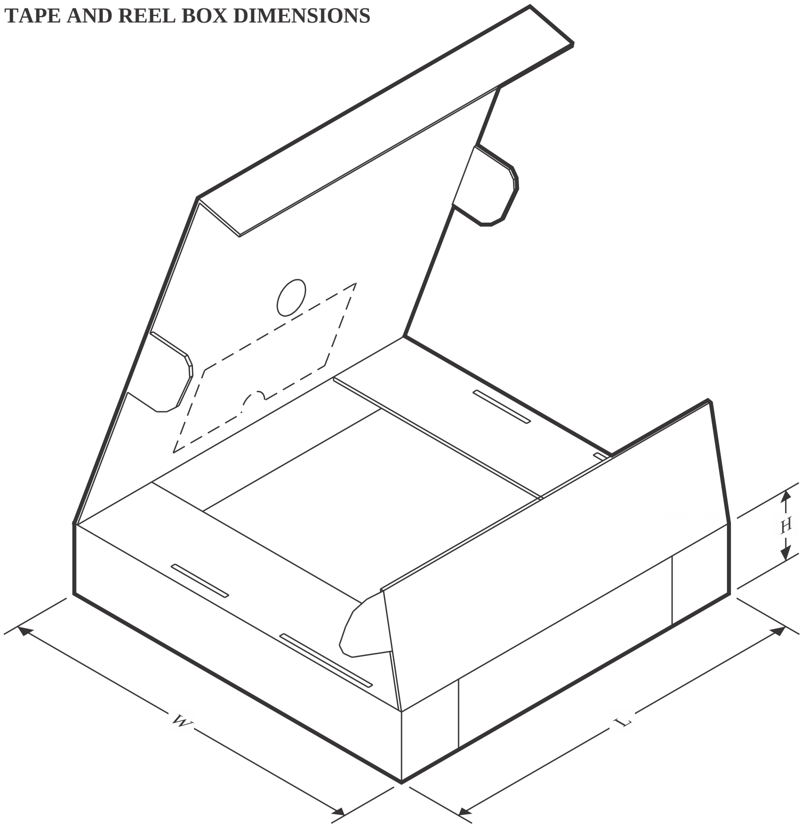
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3686TLE-AADW/NOPB	DSBGA	YZR	12	250	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1

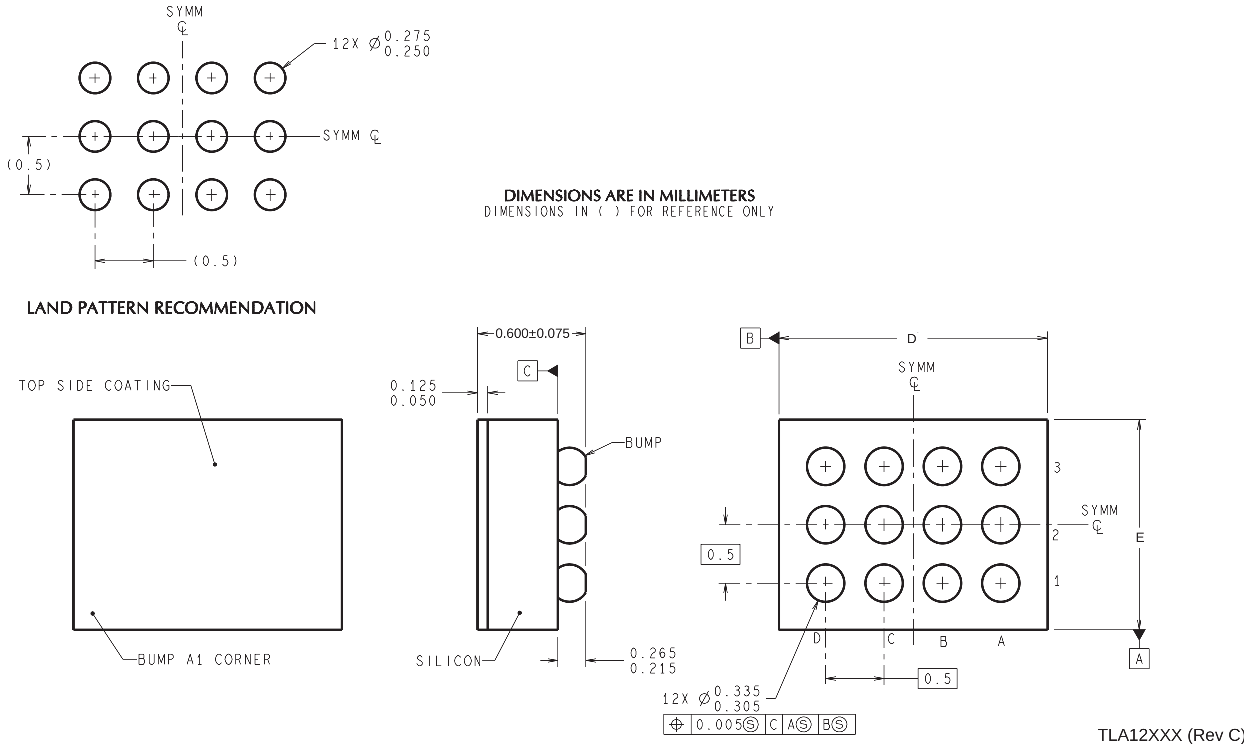
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3686TLE-AADW/NOPB	DSBGA	YZR	12	250	208.0	191.0	35.0

YZR0012



D: Max = 2.465 mm, Min =2.405 mm

E: Max = 1.717 mm, Min =1.656 mm

4215049/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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