具有跟踪功能的 LM2743 2.2V 至 16V 输入电压模式同步降压控制器

1 特性

- 1V 至 16V 的功率级输入电压
- 3V 至 6V 的控制级输入电压
- 低至 0.6V 的可调节输出电压
- 电源正常状态标志和关断功能
- 过压和欠压检测
- 整个温度范围内的反馈电压精度为 ±2%
- 低侧可调节电流检测
- 可调节软启动
- 具有关断和软启动引脚的跟踪和定序功能
- 50kHz 至 1MHz 的开关频率
- TSSOP-14 封装
- 使用 LM2743 并借助 WEBENCH® 电源设计器创建定制设计

2 应用

- 3.3V 降压稳压
- 电缆调制解调器、DSL 和 ADSL
- 激光打印机和喷墨打印机
- 低电压电源模块
- DSP、ASIC、内核和 I/O

3 说明

LM2743 是一款具有精确反馈电压（精度为 ±2%）的高速同步降压稳压器控制器。它可以提供简单的降压转换，输出电压低至 0.6V。尽管 IC 的控制部分额定电压为 3V 至 6V，但驱动器部分的设计可接受高达 16V 的输入电源轨。使用自适应非重叠 MOSFET 栅极驱动器有助于避免潜在的击穿问题，同时可以保持高效率。该 IC 专为更具有成本效益的选项（仅驱动高侧和低侧位置的 N 沟道 MOSFET）而设计。它检测低侧开关电压降，以提供简单、可调节的电流限制。

固定频率电压模式 PWM 控制架构可通过一个外部电阻器在 50kHz 至 1MHz 范围内调节。该宽范围的开关频率使电源设计人员能够灵活地在组件尺寸、成本和效率之间实现更好的折衷。

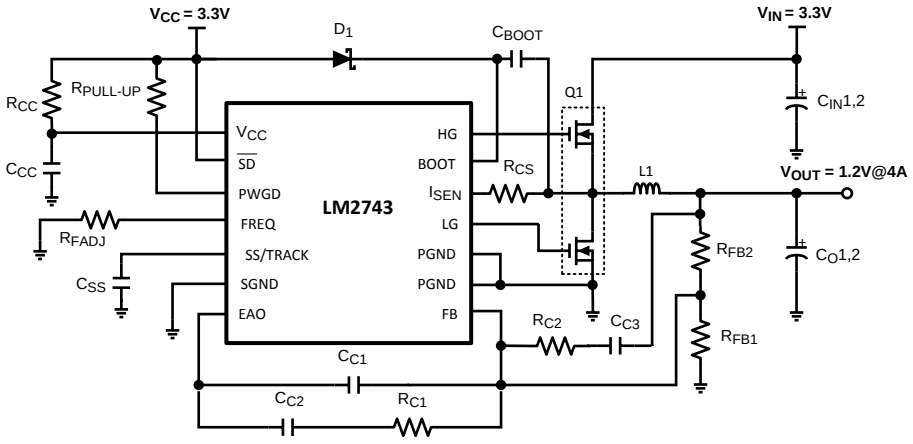
功能 包括软启动、输入欠压锁定 (UVLO) 和电源正常指示（基于欠压和过压检测）。此外，IC 的关断引脚可用于提供启动延迟，软启动引脚可用于实现精确跟踪，以便相对于外部电源轨进行定序。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM2743	TSSOP (14)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision H (October 2015) to Revision I **Page**

- 进行了编辑性更新；添加了 WEBENCH 链接；无技术更改 ... 1

Changes from Revision G (March 2013) to Revision H **Page**

- 添加了 *ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1

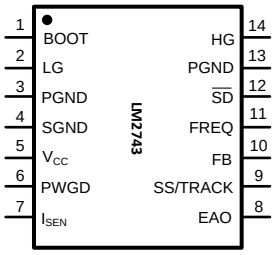
Changes from Revision F (March 2013) to Revision G **Page**

- Changed layout of National Data Sheet to TI format ... 32

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5 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
BOOT	1	Bootstrap pin. This is the supply rail for the gate drivers. When the high-side MOSFET turns on, the voltage on this pin should be at least one gate threshold above the regulator input voltage V_{IN} to properly turn on the MOSFET. See *MOSFET Gate Drivers* for more details on how to select MOSFETs.
LG	2	Low-gate drive pin. This is the gate drive for the low-side N-channel MOSFET. This signal is interlocked with the high-side gate drive HG (Pin 14), so as to avoid shoot-through.
PGND	3	Power ground. This is also the ground for the low-side MOSFET driver. Both the pins must be connected together on the PCB and form a ground plane, which is usually also the system ground.
	13	
SGND	4	Signal ground. It should be connected appropriately to the ground plane with due regard to good layout practices in switching power regulator circuits.
V_{CC}	5	Supply rail for the control sections of the IC.
PWGD	6	Power Good pin. This is an open drain output, which is typically meant to be connected to V_{CC} or any other low voltage source through a pull-up resistor. Choose the pull-up resistor so that the current going into this pin is kept below 1 mA. For most applications a recommended value for the pull-up resistor is 100 kΩ. The voltage on this pin is thus pulled low under output under-voltage or over-voltage fault conditions and also under input UVLO.
I_{SEN}	7	Current limit threshold setting pin. This sources a fixed 40 µA current. A resistor of appropriate value should be connected between this pin and the drain of the low-side MOSFET (switch node).
EAO	8	Output of the error amplifier. The voltage level on this pin is compared with an internally generated ramp signal to determine the duty cycle. This pin is necessary for compensating the control loop.
SS/TRACK	9	Soft-start and tracking pin. This pin is internally connected to the non-inverting input of the error amplifier during soft-start, and in fact any time the SS/TRACK pin voltage happens to be below the internal reference voltage. For the basic soft-start function, a capacitor of minimum value 1 nF is connected from this pin to ground. To track the rising ramp of another power supply's output, connect a resistor divider from the output of that supply to this pin as described in *Application and Implementation*.
FB	10	Feedback pin. This is the inverting input of the error amplifier, which is used for sensing the output voltage and compensating the control loop.
FREQ	11	Frequency adjust pin. The switching frequency is set by connecting a resistor of suitable value between this pin and ground. The equation for calculating the exact value is provided in *Application and Implementation*, but some typical values (rounded up to the nearest standard values) are 324 kΩ for 100 kHz, 97.6 kΩ for 300 kHz, 56.2 kΩ for 500 kHz, 24.9 kΩ for 1 MHz.
$\overline{SD}$	12	IC shutdown pin. Pull this pin to V_{CC} to ensure the IC is enabled. Connect to ground to disable the IC. Under shutdown, both high-side and low-side drives are off. This pin also features a precision threshold for power supply sequencing purposes, as well as a low threshold to ensure minimal quiescent current.
HG	14	High-gate drive pin. This is the gate drive for the high-side N-channel MOSFET. This signal is interlocked with LG (Pin 2) to avoid shoot-through.

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6 Specifications

6.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
V_{CC}			–0.3	7	V
	BOOT voltage		–0.3	21	V
I_{SEN}			–0.3	9.5	V
	All other pins		–0.3	V_{CC} + 0.3	V
T_J	Junction temperature			150	°C
	Soldering information	Lead temperature (soldering, 10 s)		260	°C
		Infrared or convection (20 s)		235	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	2000	V

(1) The human body model is a 100 pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range	3		6	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM2743 TSSOP (PW) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Typical limits are for T_J = 25°C only, represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only; minimum and maximum limits apply over the junction temperature range of –40°C to 125°C. Unless otherwise specified, V_{CC} = 3.3 V. Data sheet minimum and maximum specification limits are specified by design, test, or statistical analysis. (See (1))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	FB Pin Voltage	V_{CC} = 3 V to 6 V	0.588	0.6	0.612	V
V_{ON}	UVLO Thresholds	Rising Falling		2.76 2.42		V
I_{Q_VCC}	Operating V_{CC} Current	V_{CC} = 3.3 V, V_{SD} = 3.3 V Fsw = 600 kHz	1	1.5	2.1	mA
		V_{CC} = 5V, V_{SD} = 3.3 V Fsw = 600 kHz	1	1.7	2.1	
	Shutdown V_{CC} Current	V_{CC} = 3.3 V, V_{SD} = 0 V		110	185	µA
t_{PWGD1}	PWGD Pin Response Time	V_{FB} Rising		6		µs
t_{PWGD2}	PWGD Pin Response Time	V_{FB} Falling		6		µs
I_{SS-ON}	SS Pin Source Current	V_{SS} = 0 V	7	10	14	µA
I_{SS-OC}	SS Pin Sink Current During Over Current	V_{SS} = 2.5 V		90		µA
I_{SEN-TH}	I_{SEN} Pin Source Current Trip Point		25	40	55	µA
ERROR AMPLIFIER						
GBW	Error Amplifier Unity Gain Bandwidth			9		MHz
G	Error Amplifier DC Gain			106		dB
SR	Error Amplifier Slew Rate			3.2		V/µs
I_{EAO}	EAO Pin Current Sourcing and Sinking Capability	V_{EAO} = 1.5, FB = 0.55 V V_{EAO} = 1.5, FB = 0.65 V		2.6 9.2		mA
V_{EA}	Error Amplifier Output Voltage	Minimum		1		V
		Maximum		2		V
GATE DRIVE						
I_{Q-BOOT}	BOOT Pin Quiescent Current	V_{BOOT} = 12 V, V_{SD} = 0		18	90	µA
R_{HG_UP}	High-Side MOSFET Driver Pull-Up ON resistance	V_{BOOT} = 5 V at 350 mA Sourcing		3		Ω
R_{HG_DN}	High-Side MOSFET Driver Pull-Down ON resistance	HG = 5 V at 350 mA Sourcing		2		Ω
R_{LG_UP}	Low-Side MOSFET Driver Pull-Up ON resistance	V_{BOOT} = 5 V at 350 mA Sourcing		3		Ω
R_{LG_DN}	Low-Side MOSFET Driver Pull-Down ON resistance	LG = 5 V at 350 mA Sourcing		2		Ω
OSCILLATOR						
f_{SW}	PWM Frequency	R_{FADJ} = 702.1 kΩ		50		kHz
		R_{FADJ} = 98.74 kΩ		300		
		R_{FADJ} = 45.74 kΩ	475	600	725	
		R_{FADJ} = 24.91 kΩ		1000		
D	Max High-Side Duty Cycle	f_{SW} = 300 kHz f_{SW} = 600 kHz f_{SW} = 1 MHz		80% 76% 73%		
LOGIC INPUTS AND OUTPUTS						
$V_{STBY-IH}$	Standby High Trip Point	V_{FB} = 0.575 V, V_{BOOT} = 3.3 V, V_{SD} Rising			1.1	V
$V_{STBY-IL}$	Standby Low Trip Point	V_{FB} = 0.575 V, V_{BOOT} = 3.3 V, V_{SD} Falling	0.232			V
V_{SD-IH}	$\overline{SD}$ Pin Logic High Trip Point	V_{SD} Rising			1.3	V

(1) The power MOSFETs can run on a separate 1-V to 16-V rail (Input voltage, V_{IN}). Practical lower limit of V_{IN} depends on selection of the external MOSFET.

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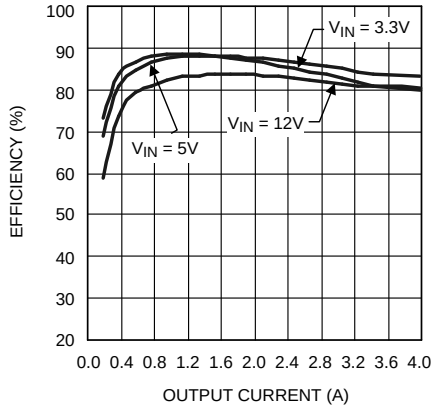
Electrical Characteristics (continued)

Typical limits are for T_J = 25°C only, represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only; minimum and maximum limits apply over the junction temperature range of –40°C to 125°C. Unless otherwise specified, V_{CC} = 3.3 V. Data sheet minimum and maximum specification limits are specified by design, test, or statistical analysis. (See (1))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD-IL}	$\overline{SD}$ Pin Logic Low Trip Point	V_{SD} Falling	0.8			V
$V_{PWGD-TH-LO}$	PWGD Pin Trip Points	FB Falling	0.408	0.434	0.457	V
$V_{PWGD-TH-HI}$	PWGD Pin Trip Points	FB Rising	0.677	0.710	0.742	V
$V_{PWGD-HYS}$	PWGD Hysteresis	FB Falling		60		mV
		FB Rising		90		

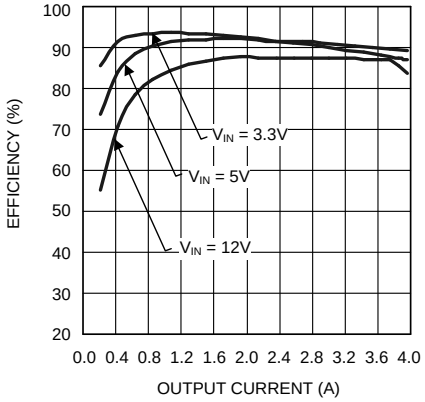
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6.6 Typical Characteristics



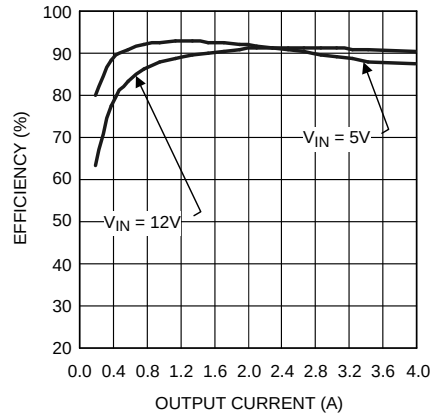
V_{CC} = 3.3 V f_{SW} = 300 kHz

Figure 1. Efficiency V_{OUT} = 1.2 V



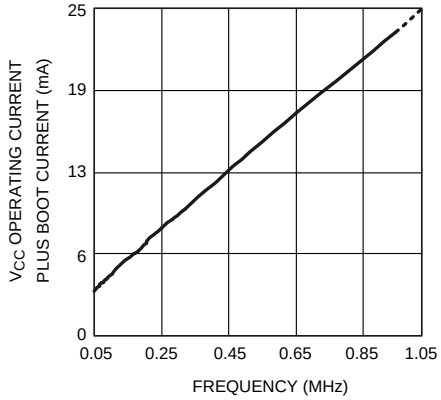
V_{CC} = 3.3 V f_{SW} = 300 kHz

Figure 2. Efficiency V_{OUT} = 2.5 V



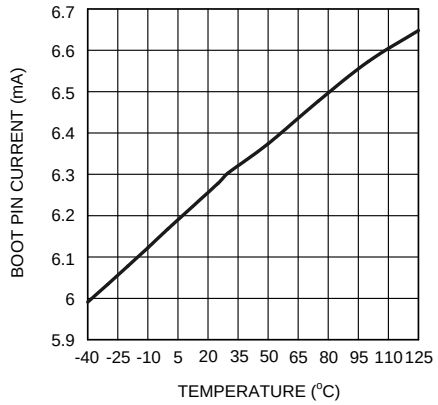
V_{CC} = 5 V f_{SW} = 300 kHz

Figure 3. Efficiency V_{OUT} = 3.3 V



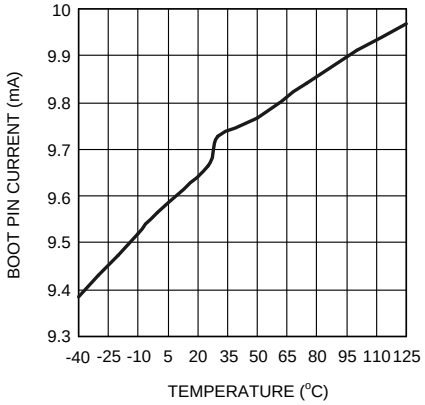
FDS6898A FET T_A = 25°C

Figure 4. V_{CC} Operating Current Plus BOOT Current vs Frequency



f_{SW} = 300 kHz FDS6898A FET No-Load

Figure 5. BOOT Pin Current vs Temperature for BOOT Voltage = 3.3 V

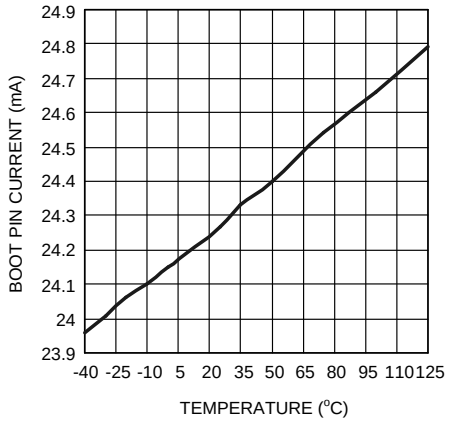


f_{SW} = 300 kHz FDS6898A FET No-Load

Figure 6. BOOT Pin Current vs Temperature for BOOT Voltage = 5 V

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Typical Characteristics (continued)



f_{SW} = 300 kHz FDS6898A FET No-Load

Figure 7. BOOT Pin Current vs Temperature for BOOT Voltage = 12 V

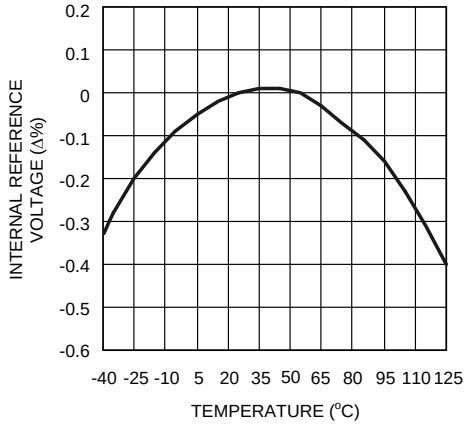


Figure 8. Internal Reference Voltage vs Temperature

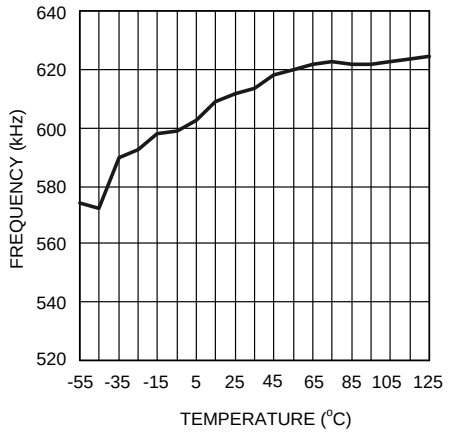


Figure 9. Frequency vs Temperature

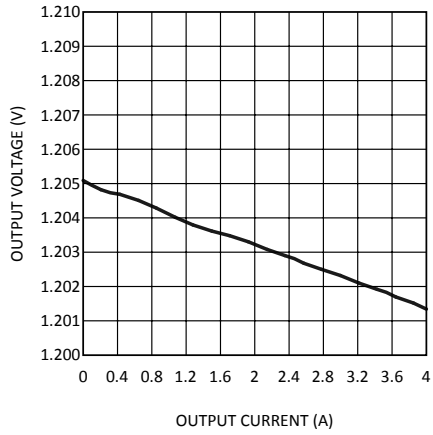
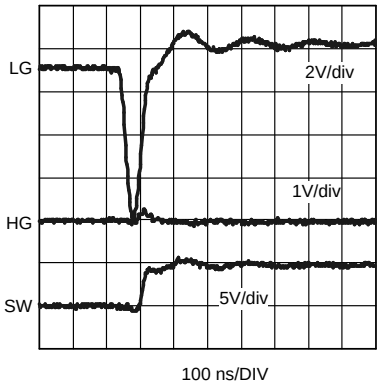
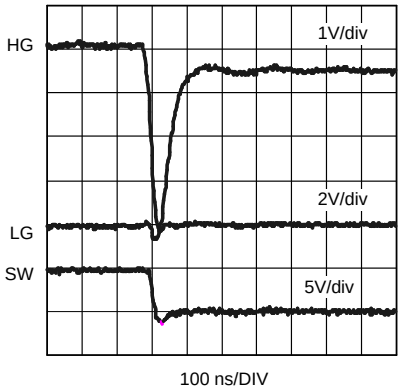


Figure 10. Output Voltage vs Output Current



V_{CC} = 3.3 V V_{IN} = 5 V V_{OUT} = 1.2 V
I_{OUT} = 4 A C_{SS} = 12 nF f_{SW} = 300 kHz

Figure 11. Switch Waveforms (HG Rising)

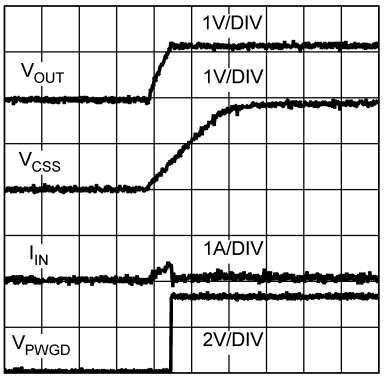


V_{CC} = 3.3 V V_{IN} = 5 V V_{OUT} = 1.2 V
I_{OUT} = 4 A C_{SS} = 12 nF f_{SW} = 300 kHz

Figure 12. Switch Waveforms (HG Falling)

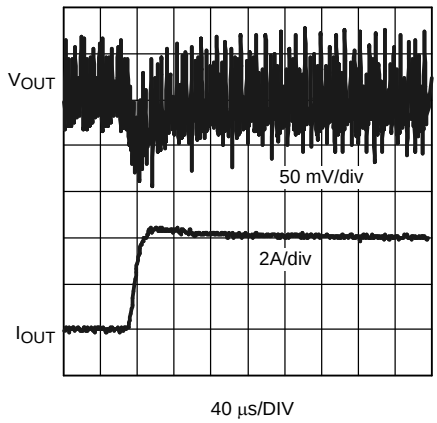
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Typical Characteristics (continued)



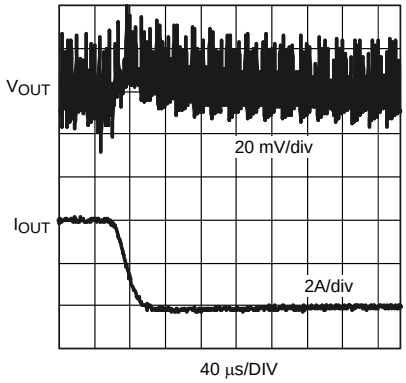
V_{CC} = 3.3 V V_{IN} = 5V V_{OUT} = 1.2V
C_{SS} = 12 nF f_{SW} = 300 kHz

Figure 13. Start-Up (No-Load)



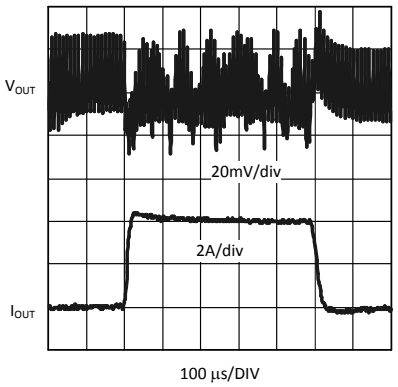
I_{OUT} = 0 A to 4 A V_{CC} = 3.3 V V_{IN} = 5 V
V_{OUT} = 1.2 V C_{SS} = 12nF f_{SW} = 300 kHz

Figure 14. Load Transient Response



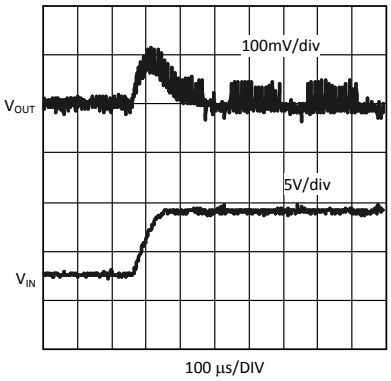
I_{OUT} = 4 A to 0 A V_{CC} = 3.3 V V_{IN} = 5 V
V_{OUT} = 1.2 V C_{SS} = 12 nF f_{SW} = 300 kHz

Figure 15. Load Transient Response



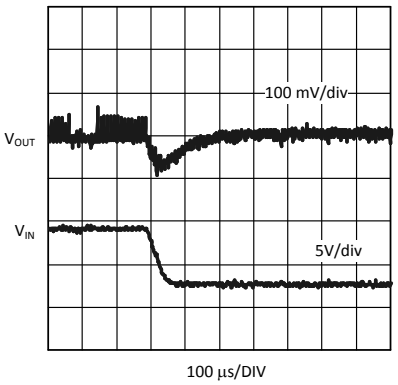
V_{CC} = 3.3 V V_{IN} = 5 V V_{OUT} = 1.2 V
C_{SS} = 12 nF f_{SW} = 300 kHz

Figure 16. Load Transient Response



V_{IN} = 3 V to 9 V V_{CC} = 3.3 V V_{OUT} = 1.2 V
Line () , I_{OUT} = 2 A f_{SW} = 300 kHz

Figure 17. Line Transient Response



V_{IN} = 9 V to 3 V V_{CC} = 3.3 V V_{OUT} = 1.2 V
I_{OUT} = 2 A f_{SW} = 300 kHz

Figure 18. Transient Response

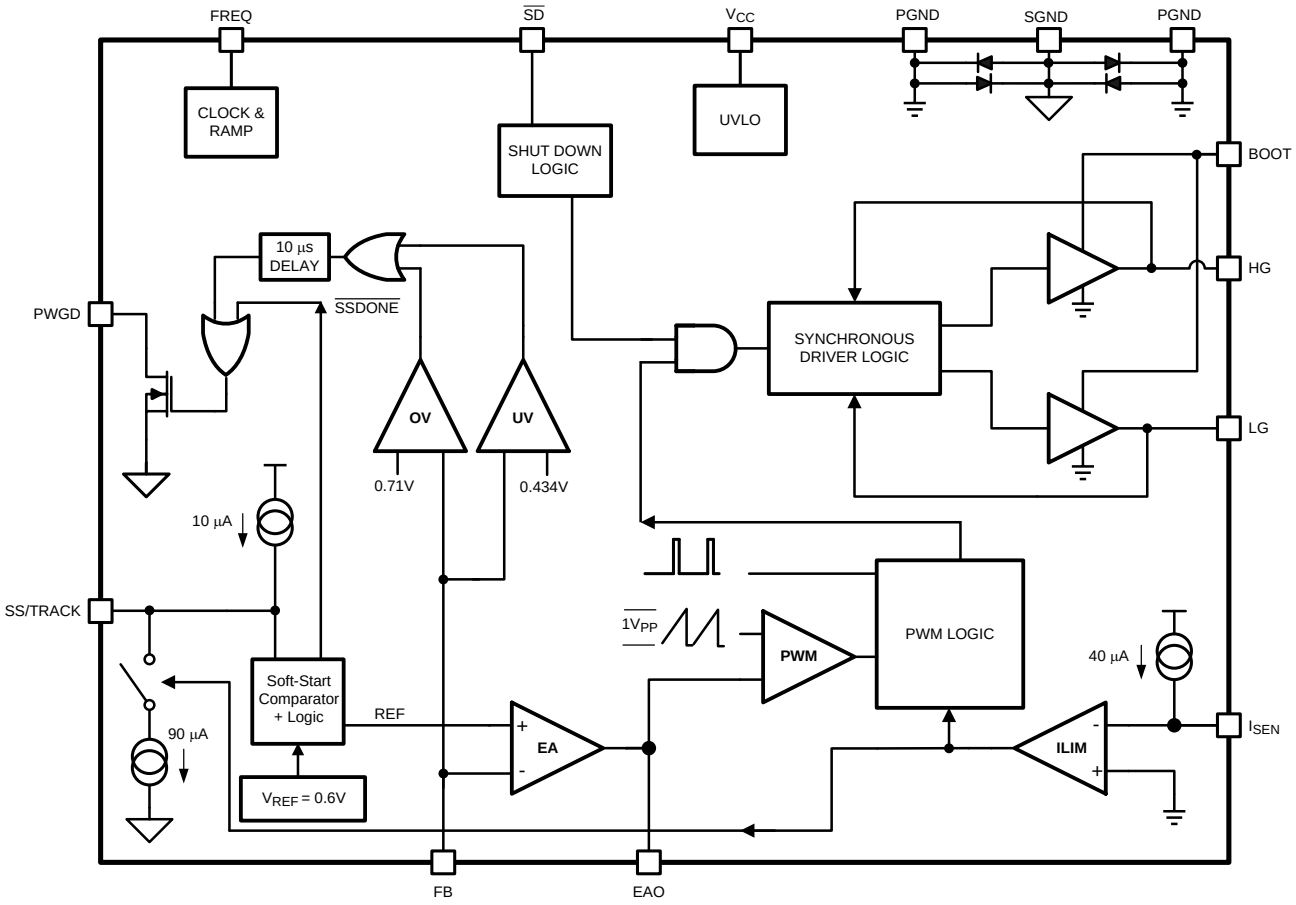
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7 Detailed Description

7.1 Overview

The LM2743 is a voltage-mode, high-speed synchronous buck regulator with a PWM control scheme. It has output shutdown ($\overline{SD}$), input under-voltage lock-out (UVLO) mode and power good (PWGD) flag (based on over-voltage and under-voltage detection). The over-voltage and under-voltage signals are logically OR'ed to drive the power good signal and provide a logic signal to the system if the output voltage goes out of regulation. Current limit is achieved by sensing the voltage V_{DS} across the low-side MOSFET.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Start Up and Soft-Start

When V_{CC} exceeds 2.76V and the shutdown pin ($\overline{SD}$) sees a logic high, the soft-start period begins. Then an internal, fixed 10 µA source begins charging the soft-start capacitor. During soft-start the voltage on the soft-start capacitor C_{SS} is connected internally to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the LM2743 reference voltage of 0.6V. At this point the reference voltage takes over at the non-inverting error amplifier input. The capacitance of C_{SS} determines the length of the soft-start period, and can be approximated by:

$$C_{SS} = \frac{t_{SS}}{60}$$

where

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Feature Description (continued)

- C_{SS} is in µF and t_{SS} is in ms (1)

During soft start the Power Good flag is forced low and it is released when the FB pin voltage reaches 70% of 0.6V. At this point the chip enters normal operation mode, and the output overvoltage and undervoltage monitoring starts.

7.3.2 Normal Operation

While in normal operation mode, the LM2743 regulates the output voltage by controlling the duty cycle of the high side and low side MOSFETs (see *典型应用图*). The equation governing output voltage is:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB1}} V_{FB}$$

$$(V_{FB} = 0.6V) \quad (2)$$

The PWM frequency is adjustable between 50 kHz and 1 MHz and is set by an external resistor, R_{FADJ}, between the FREQ pin and ground. The resistance needed for a desired frequency is approximately:

$$R_{FADJ} = -5.93 + 3.06 \frac{10^7}{f_{SW}} + 0.24 \frac{10^{12}}{(f_{SW})^2} \quad (3)$$

Where f_{SW} is in Hz and R_{FADJ} is in kΩ.

7.3.3 Tracking a Voltage Level

The LM2743 can track the output of a master power supply during soft-start by connecting a resistor divider to the SS/TRACK pin. In this way, the output voltage slew rate of the LM2743 will be controlled by the master supply for loads that require precise sequencing. When the tracking function is used no soft-start capacitor should be connected to the SS/TRACK pin. Otherwise, a C_{SS} value of at least 1 nF between the soft-start pin and ground should be used.

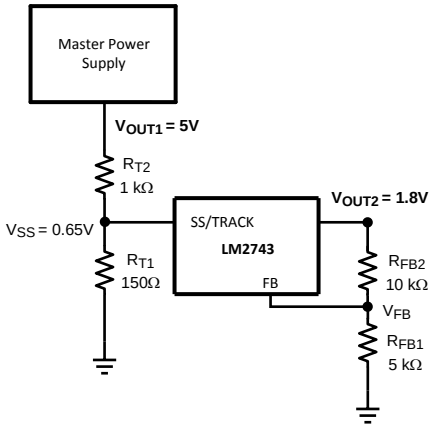


Figure 19. Tracking Circuit

One way to use the tracking feature is to design the tracking resistor divider so that the master supply's output voltage (V_{OUT1}) and the LM2743's output voltage (represented symbolically in Figure 19 as V_{OUT2}, that is, without explicitly showing the power components) both rise together and reach their target values at the same time. For this case, the equation governing the values of the tracking divider resistors R_{T1} and R_{T2} is:

$$0.65 = V_{OUT1} \frac{R_{T1}}{R_{T1} + R_{T2}} \quad (4)$$

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Feature Description (continued)

The current through R_{T1} should be about 3 mA to 4 mA for precise tracking. The final voltage of the SS/TRACK pin should be set higher than the feedback voltage of 0.6 V (say about 0.65 V as in the above equation). If the master supply voltage was 5 V and the LM2743 output voltage was 1.8 V, for example, then the value of R_{T1} needed to give the two supplies identical soft-start times would be 150 Ω. A timing diagram for the equal soft-start time case is shown in Figure 20.

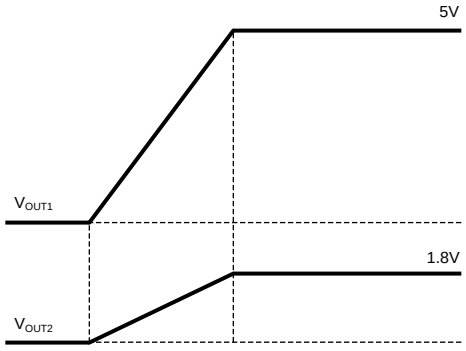


Figure 20. Tracking with Equal Soft-Start Time

7.3.4 Tracking Voltage Slew Rate

The tracking feature can alternatively be used not to make both rails reach regulation at the same time but rather to have similar rise rates (in terms of output dV/dt). This method ensures that the output voltage of the LM2743 always reaches regulation before the output voltage of the master supply. Because the output of the master supply is divided down, in order to track properly the output voltage of the LM2743 must be lower than the voltage of the master supply. In this case, the tracking resistors can be determined based on the following equation:

$$V_{OUT2} = V_{OUT1} \frac{R_{T1}}{R_{T1} + R_{T2}} \tag{5}$$

For the example case of V_{OUT1} = 5 V and V_{OUT2} = 1.8 V, with R_{T1} set to 150 Ω as before, R_{T2} is calculated from the above equation to be 265 Ω. A timing diagram for the case of equal slew rates is shown in Figure 21.

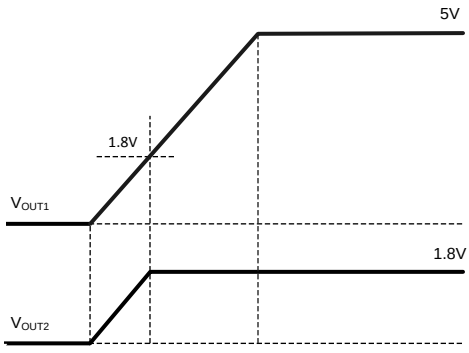


Figure 21. Tracking with Equal Slew Rates

7.3.5 Sequencing

The start up/soft-start of the LM2743 can be delayed for the purpose of sequencing by connecting a resistor divider from the output of a master power supply to the $\overline{SD}$ pin, as shown in Figure 22.

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Feature Description (continued)

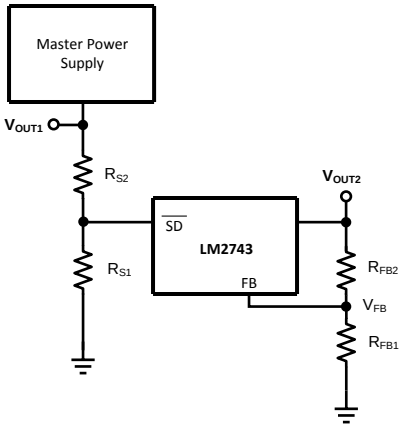


Figure 22. Sequencing Circuit

A desired delay time t_{DELAY} between the startup of the master supply output voltage and the LM2743 output voltage can be set based on the $\overline{SD}$ pin low-to-high threshold V_{SD-IH} and the slew rate of the voltage at the $\overline{SD}$ pin, SR_{SD}:

$$t_{DELAY} = V_{SD-IH} / SR_{SD} \quad (6)$$

Note again, that in Figure 22, the output voltage of the LM2743 has been represented symbolically as V_{OUT2},. without explicitly showing the power components.

V_{SD-IH} is typically 1.08V and SR_{SD} is the slew rate of the $\overline{SD}$ pin voltage. The values of the sequencing divider resistors R_{S1} and R_{S2} set the SR_{SD} based on the master supply output voltage slew rate, SR_{OUT1}, using the following equation:

$$SR_{SD} = SR_{OUT1} \frac{R_{S1}}{R_{S1} + R_{S2}} \quad (7)$$

For example, if the master supply output voltage slew rate was 1V/ms and the desired $\overline{SD}$ delay time between the startup of the master supply and LM2743 output voltage was 5ms, then the desired $\overline{SD}$ pin slew rate would be (1.08V/5 ms) = 0.216 V/ms. Due to the internal impedance of the $\overline{SD}$ pin, the maximum recommended value for R_{S2} is 1 kΩ. To achieve the desired slew rate, R_{S1} would then be 274 Ω. A timing diagram for this example is shown in Figure 23.

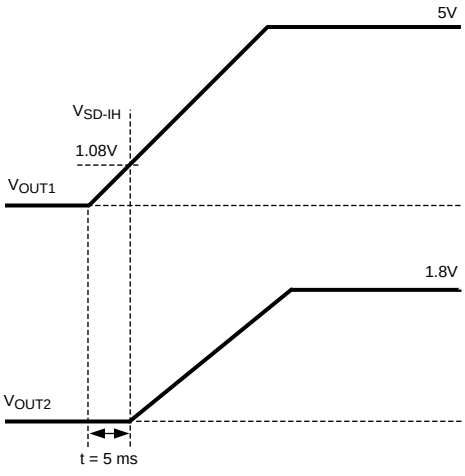


Figure 23. Delay for Sequencing

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Feature Description (continued)

7.3.6 $\overline{SD}$ Pin Impedance

When connecting a resistor divider to the $\overline{SD}$ pin of the LM2743 some care has to be taken. Once the $\overline{SD}$ voltage goes above V_{SD-IH}, a 17-µA pull-up current is activated as shown in Figure 24. This current is used to create the internal hysteresis (≅170 mV); however, high external impedances will affect the $\overline{SD}$ pin logic thresholds as well. The external impedance used for the sequencing divider network should preferably be a small fraction of the impedance of the $\overline{SD}$ pin for good performance (around 1 kΩ).

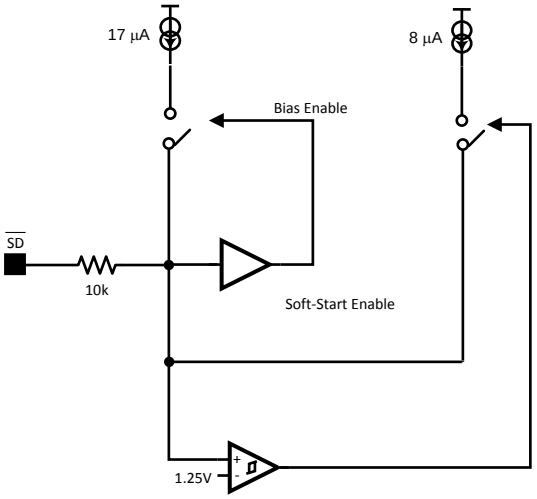


Figure 24. $\overline{SD}$ Pin Logic

7.3.7 MOSFET Gate Drivers

The LM2743 has two gate drivers designed for driving N-channel MOSFETs in a synchronous mode. Note that unlike most other synchronous controllers, the bootstrap capacitor of the LM2743 provides power not only to the driver of the upper MOSFET, but the lower MOSFET driver too (both drivers are ground referenced, i.e. no floating driver). To fully turn the top MOSFET on, the BOOT voltage must be at least one gate threshold greater than V_{IN} when the high-side drive goes high. This bootstrap voltage is usually supplied from a local charge pump structure. But looking at the *Typical Application* schematic, this also means that the difference voltage V_{CC} - V_{D1}, which is the voltage the bootstrap capacitor charges up to, must be always greater than the maximum tolerance limit of the threshold voltage of the upper MOSFET. Here V_{D1} is the forward voltage drop across the bootstrap diode D1. This therefore may place restrictions on the minimum input voltage and/or type of MOSFET used.

The most basic charge bootstrap pump circuit can be built using one Schottky diode and a small capacitor, as shown in Figure 25. The capacitor C_{BOOT} serves to maintain enough voltage between the top MOSFET gate and source to control the device even when the top MOSFET is on and its source has risen up to the input voltage level. The charge pump circuitry is fed from V_{CC}, which can operate over a range from 3.0V to 6.0V. Using this basic method the voltage applied to the gates of both high-side and low-side MOSFETs is $\mathbf{V_{CC} - V_D}$. This method works well when V_{CC} is 5 V±10%, because the gate drives will get at least 4.0V of drive voltage during the worst case of V_{CC-MIN} = 4.5 V and V_{D-MAX} = 0.5 V. Logic level MOSFETs generally specify their on-resistance at V_{GS} = 4.5 V. When V_{CC} = 3.3 V ±10%, the gate drive at worst case could go as low as 2.5 V. Logic level MOSFETs are not specified to turn on, or may have much higher on-resistance at 2.5 V. Sub-logic level MOSFETs, usually specified at V_{GS} = 2.5 V, will work, but are more expensive, and tend to have higher on-resistance. The circuit in Figure 25 works well for input voltages ranging from 1 V up to 16 V and V_{CC} = 5 V ±10%, because the drive voltage depends only on V_{CC}.

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Feature Description (continued)

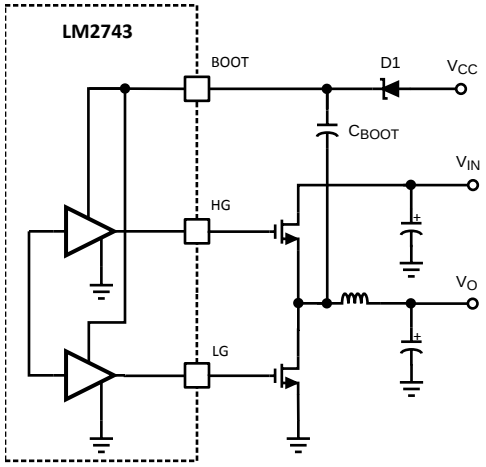


Figure 25. Basic Charge Pump (Bootstrap)

Note that the LM2743 can be paired with a low cost linear regulator like the LM78L05 to run from a single input rail between 6.0 and 14 V. The 5-V output of the linear regulator powers both the V_{CC} and the bootstrap circuit, providing efficient drive for logic level MOSFETs. An example of this circuit is shown in Figure 26.

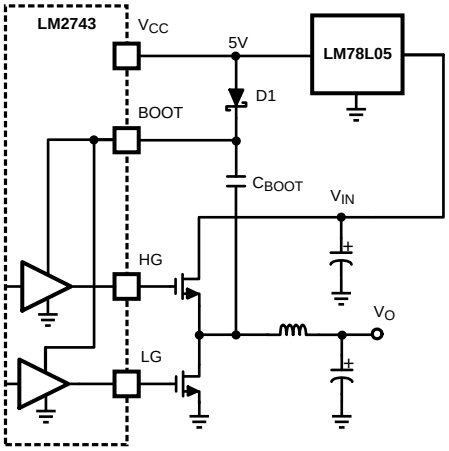


Figure 26. LM78L05 Feeding Basic Charge Pump

Figure 27 shows a second possibility for bootstrapping the MOSFET drives using a doubler. This circuit provides an equal voltage drive of $\mathbf{V_{CC} - 3V_D + V_{IN}}$ to both the high-side and low-side MOSFET drives. This method should only be used in circuits that use 3.3 V for both V_{CC} and V_{IN}. Even with $V_{IN} = V_{CC} = 3.0$ V (10% lower tolerance on 3.3 V) and $V_D = 0.5$ V both high-side and low-side gates will have at least 4.5 V of drive. The power dissipation of the gate drive circuitry is directly proportional to gate drive voltage, hence the thermal limits of the LM2743 IC will quickly be reached if this circuit is used with V_{CC} or V_{IN} voltages over 5V.

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Feature Description (continued)

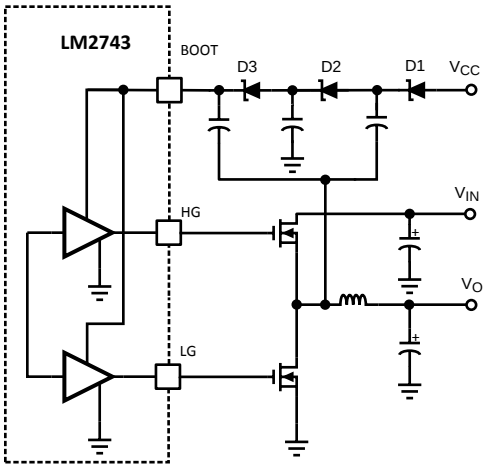


Figure 27. Charge Pump with Added Gate Drive

All the gate drive circuits shown in Figure 25 through Figure 27 typically use 100-nF ceramic capacitors in the bootstrap locations.

7.3.8 Power Good Signal

The open drain output on the Power Good pin needs a pull-up resistor to a low voltage source. The pull-up resistor should be chosen so that the current going into the Power Good pin is less than 1 mA. A 100-kΩ resistor is recommended for most applications.

The Power Good signal is an OR-gated flag which takes into account both output over-voltage and under-voltage conditions. If the feedback pin (FB) voltage is 18% above its nominal value (118% x V_{FB} = 0.708V) or falls 28% below that value (72 %x V_{FB} = 0.42V) the Power Good flag goes low. The Power Good flag can be used to signal other circuits that the output voltage has fallen out of regulation, however the switching of the LM2743 continues regardless of the state of the Power Good signal. The Power Good flag will return to logic high whenever the feedback pin voltage is between 72% and 118% of 0.6V.

7.3.9 UVLO

The 2.76V turn-on threshold on V_{CC} has a built in hysteresis of about 300 mV. If V_{CC} drops below 2.42V, the chip enters UVLO mode. UVLO consists of turning off the top and bottom MOSFETS and remaining in that condition until V_{CC} rises above 2.76V. As with shutdown, the soft-start capacitor is discharged through an internal MOSFET, ensuring that the next start-up will be controlled by the soft-start circuitry.

7.3.10 Current Limit

Current limit is realized by sensing the voltage across the low-side MOSFET while it is on. The $R_{DS(ON)}$ of the MOSFET is a known value; hence the current through the MOSFET can be determined as:

$$V_{DS} = I_{OUT} \times R_{DS(ON)} \quad (8)$$

The current through the low-side MOSFET while it is on is also the falling portion of the inductor current. The current limit threshold is determined by an external resistor, R_{CS}, connected between the switching node and the I_{SEN} pin. A constant current of 40 µA is forced through R_{CS}, causing a fixed voltage drop. This fixed voltage is compared against V_{DS} and if the latter is higher, the current limit of the chip has been reached. To obtain a more accurate value for R_{CS} you must consider the operating values of $R_{DS(ON)}$ and I_{SEN-TH} at their operating temperatures in your application and the effect of slight parameter differences from part to part. R_{CS} can be found by using the following equation using the $R_{DS(ON)}$ value of the low side MOSFET at it's expected hot temperature and the absolute minimum value expected over the full temperature range for the for the I_{SEN-TH} which is 25 µA:

$$R_{CS} = R_{DSON-HOT} \times I_{LIM} / 40\ \mu A \quad (9)$$

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Feature Description (continued)

For example, a conservative 15-A current limit in a 10-A design with a minimum $R_{DS(ON)}$ of 10 mΩ would require a 6-kΩ resistor. To prevent the I_{SEN} pin from sinking too much current when the switch node goes above 9.5 V, the value of the current limit setting resistor R_{CS} should not be too low. The criterion is as follows,

$$R_{CS} \geq \frac{V_{IN} - 9.5V}{10\ mA} \tag{10}$$

where the 10 mA is the maximum current I_{SEN} pin is allowed to sink. For example if V_{IN} = 13.2 V, the minimum value of R_{CS} is 370 Ω. Because current sensing is done across the low-side MOSFET, no minimum high-side on-time is necessary. The LM2743 enters current limit mode if the inductor current exceeds the current limit threshold at the point where the high-side MOSFET turns off and the low-side MOSFET turns on. (The point of peak inductor current, see Figure 28). Note that in normal operation mode the high-side MOSFET always turns on at the beginning of a clock cycle. In current limit mode, by contrast, the high-side MOSFET on-pulse is skipped. This causes inductor current to fall. Unlike a normal operation switching cycle, however, in a current limit mode switching cycle the high-side MOSFET will turn on as soon as inductor current has fallen to the current limit threshold. The LM2743 will continue to skip high-side MOSFET pulses until the inductor current peak is below the current limit threshold, at which point the system resumes normal operation.

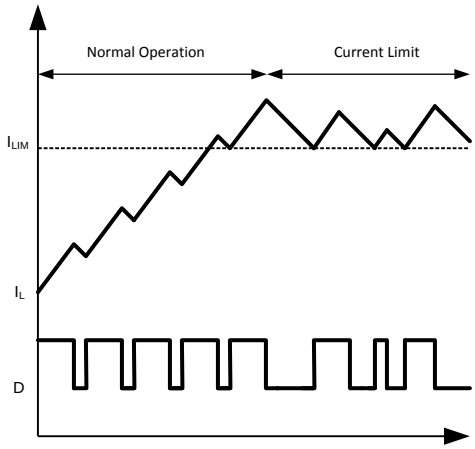


Figure 28. Current Limit Threshold

Unlike a high-side MOSFET current sensing scheme, which limits the peaks of inductor current, low-side current sensing is only allowed to limit the current during the converter off-time, when inductor current is falling. Therefore in a typical current limit plot the valleys are normally well defined, but the peaks are variable, according to the duty cycle. The PWM error amplifier and comparator control the off-pulse of the high-side MOSFET, even during current limit mode, meaning that peak inductor current can exceed the current limit threshold. Assuming that the output inductor does not saturate, the maximum peak inductor current during current limit mode can be calculated with the following equation:

$$I_{PK\text{-}CL} = I_{LIM} + (T_{SW} - 200\ ns)\frac{V_{IN} - V_O}{L} \tag{11}$$

Where T_{SW} is the inverse of switching frequency f_{SW}. The 200 ns term represents the minimum off-time of the duty cycle, which ensures enough time for correct operation of the current sensing circuitry.

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Feature Description (continued)

In order to minimize the time period in which peak inductor current exceeds the current limit threshold, the IC also discharges the soft-start capacitor through a fixed 90-µA sink. The output of the LM2743 internal error amplifier is limited by the voltage on the soft-start capacitor. Hence, discharging the soft-start capacitor reduces the maximum duty cycle D of the controller. During severe current limit this reduction in duty cycle will reduce the output voltage if the current limit conditions last for an extended time. Output inductor current will be reduced in turn to a flat level equal to the current limit threshold. The third benefit of the soft-start capacitor discharge is a smooth, controlled ramp of output voltage when the current limit condition is cleared.

7.3.11 Foldback Current Limit

In the case where extra protection is used to help an output short condition, a current foldback resistor (R_{CLF}) should be considered, see Figure 29. First select the percentage of current limit foldback (P_{LIM}):

$$P_{LIM} = I_{LIM} \times P \tag{12}$$

where P is a ratio between 0 and 1.

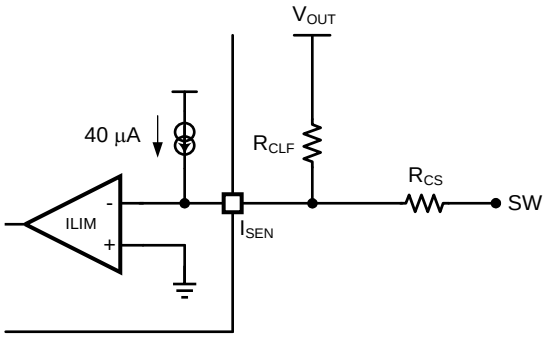


Figure 29. Foldback Current Limit Circuit

Obtain the R_{CS} with the following equation:

$$\frac{P_{LIM} \times R_{DS(ON)}}{I_{SEN}} = R_{CS} \tag{13}$$

where I_{SEN} = 40 µA. If the switch node goes above 9.5 V the following criterion must be satisfied:

$$R_{CS} \geq \frac{V_{IN} - 9.5V}{10\ mA} \tag{14}$$

The equation for calculating the foldback resistance value is:

$$R_{CLF} = \frac{R_{CS} \times V_{OUT}}{(I_{LIM} \times R_{DS(ON)}) - (I_{SEN} \times R_{CS})} \tag{15}$$

7.4 Device Functional Modes

7.4.1 Shutdown

If the shutdown pin is pulled low, (below 0.8 V) the LM2743 enters shutdown mode, and discharges the soft-start capacitor through a MOSFET switch. The high and low-side MOSFETs are turned off. The LM2743 remains in this state as long as V_{SD} sees a logic low (see the *Electrical Characteristics* table). To assure proper IC start-up the shutdown pin should not be left floating. For normal operation this pin should be connected directly to V_{CC} or to another voltage between 1.3 V to V_{CC} (see the *Electrical Characteristics* table).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2743 is a voltage-mode, high-speed synchronous buck regulator with a PWM control scheme. It is designed for use in set-top boxes, thin clients, DSL/Cable modems, and other applications that require high-efficiency buck converters. Use the following design procedure to select component values for the LM2743 device. Use the WEBENCH to generate a complete design (see *Custom Design With WEBENCH® Tools*.

8.2 Typical Applications

8.2.1 Synchronous Buck Converter Typical Application using LM2743

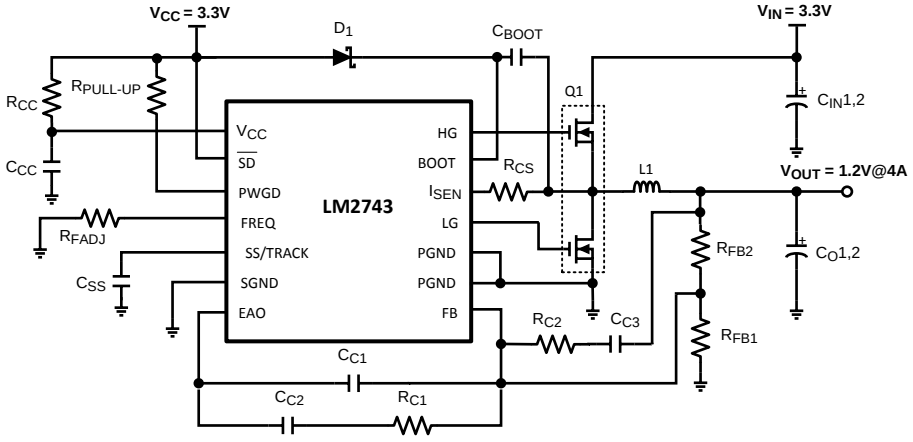


Figure 30. 3.3 V to 1.2 V at 4 A, f_{SW} = 300 kHz

8.2.1.1 Design Requirements

The following section provides a step-by-step design guide of a voltage-mode synchronous buck converter using the LM2743. This design converts 3.3 V (V_{IN}) to 1.2 V (V_{OUT}) at a maximum load of 4 A, with an efficiency of 89% and a switching frequency of 300 kHz. The same procedures can be followed to create many other designs with varying input voltages, output voltages, and load currents.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM2743 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance

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Typical Applications (continued)

- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Duty Cycle Calculation

The complete duty cycle for a buck converter is defined with Equation 16:

$$D = \frac{V_{OUT} + V_{SWL}}{V_{IN} - V_{SWH} + V_{SWL}} \quad (16)$$

where V_{SWL} and V_{SWH} are the respective forward voltage drops that develop across the low side and high side MOSFETs. Assuming the inductor ripple current is 20% to 30% of the output current, therefore:

$$V_{SWL} = I_{OUT} \times R_{DS(ON)LOW} \text{ (Low-Side MOSFET)} \quad (17)$$

$$V_{SWH} = I_{OUT} \times R_{DS(ON)HIGH} \text{ (High-Side MOSFET)} \quad (18)$$

To calculate the maximum duty cycle use the estimated 'hot' $R_{DS(on)}$ value of the MOSFETs, the minimum input voltage, and maximum load. As shown in Figure 31, the worst case maximum duty cycles of the LM2743 occurs at 125°C junction temperature vs V_{CC} (IC control section voltage). Ensure that the operating duty cycle is below the curve in Figure 31, if this condition is not satisfied, the system will be unable to develop the required duty cycle to derive the necessary system power and so the output voltage will fall out of regulation.

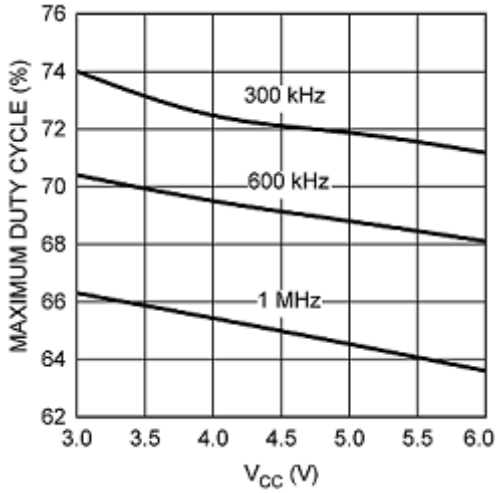


Figure 31. Maximum Duty Cycle vs V_{CC}
T_J = 125°C

8.2.1.2.3 Input Capacitor

The input capacitors in a Buck converter are subjected to high stress due to the input current trapezoidal waveform. Input capacitors are selected for their ripple current capability and their ability to withstand the heat generated since that ripple current passes through their ESR. Input rms ripple current is approximately:

$$I_{RMS_RIP} = I_{OUT} \times \sqrt{D(1 - D)} \quad (19)$$

The power dissipated by each input capacitor is:

$$P_{CAP} = \frac{(I_{RMS_RIP})^2 \times ESR}{n^2} \quad (20)$$

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Typical Applications (continued)

where n is the number of capacitors, and ESR is the equivalent series resistance of each capacitor. The equation above indicates that power loss in each capacitor decreases rapidly as the number of input capacitors increases. The worst-case ripple for a Buck converter occurs during full load and when the duty cycle (D) is 0.5. For this 3.3V to 1.2V design the duty cycle is 0.364. For a 4A maximum load the ripple current is 1.92A.

8.2.1.2.4 Output Inductor

The output inductor forms the first half of the power stage in a Buck converter. It is responsible for smoothing the square wave created by the switching action and for controlling the output current ripple (ΔI_{OUT}). The inductance is chosen by selecting between tradeoffs in efficiency and response time. The smaller the output inductor, the more quickly the converter can respond to transients in the load current. However, as shown in the efficiency calculations, a smaller inductor requires a higher switching frequency to maintain the same level of output current ripple. An increase in frequency can mean increasing loss in the MOSFETs due to the charging and discharging of the gates. Generally the switching frequency is chosen so that conduction loss outweighs switching loss. The equation for output inductor selection is:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_{OUT} \times f_{SW}} \times D \tag{21}$$

$$L = \frac{3.3V - 1.2V}{0.4 \times 4A \times 300\ kHz} \times \frac{1.2V}{3.3V} \tag{22}$$

$$L = 1.6\ \mu H \tag{23}$$

Here we have plugged in the values for output current ripple, input voltage, output voltage, switching frequency, and assumed a 40% peak-to-peak output current ripple. This yields an inductance of 1.6 µH. The output inductor must be rated to handle the peak current (also equal to the peak switch current), which is (I_{OUT} + (0.5 x ΔI_{OUT})) = 4.8 A, for a 4 A design. The Coilcraft DO3316P-222P is 2.2 µH, is rated to 7.4-A peak, and has a direct current resistance (DCR) of 12 mΩ.

After selecting an output inductor, inductor current ripple should be re-calculated with the new inductance value, as this information is needed to select the output capacitor. Re-arranging the equation used to select inductance yields the following:

$$\Delta I_{OUT} = \frac{V_{IN(MAX)} - V_O}{F_{SW} \times L_{ACTUAL}} \times D \tag{24}$$

$V_{IN(MAX)}$ is assumed to be 10% above the steady state input voltage, or 3.6V. The actual current ripple will then be 1.2A. Peak inductor/switch current will be 4.6A.

8.2.1.2.5 Output Capacitor

The output capacitor forms the second half of the power stage of a Buck switching converter. It is used to control the output voltage ripple (ΔV_{OUT}) and to supply load current during fast load transients.

In this example the output current is 4 A and the expected type of capacitor is an aluminum electrolytic, as with the input capacitors. Other possibilities include ceramic, tantalum, and solid electrolyte capacitors, however the ceramic type often do not have the large capacitance needed to supply current for load transients, and tantalums tend to be more expensive than aluminum electrolytic. Aluminum capacitors tend to have very high capacitance and fairly low ESR, meaning that the ESR zero, which affects system stability, will be much lower than the switching frequency. The large capacitance means that at the switching frequency, the ESR is dominant, hence the type and number of output capacitors is selected on the basis of ESR. One simple formula to find the maximum ESR based on the desired output voltage ripple, ΔV_{OUT} and the designed output current ripple, ΔI_{OUT}, is:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \tag{25}$$

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Typical Applications (continued)

In this example, in order to maintain a 2% peak-to-peak output voltage ripple and a 40% peak-to-peak inductor current ripple, the required maximum ESR is 20 mΩ. The Sanyo 4SP560M electrolytic capacitor will give an equivalent ESR of 14 mΩ. The capacitance of 560 µF is enough to supply energy even to meet severe load transient demands.

8.2.1.2.6 MOSFETs

Selection of the power MOSFETs is governed by a tradeoff between cost, size, and efficiency. One method is to determine the maximum cost that can be endured, and then select the most efficient device that fits that price. Breaking down the losses in the high-side and low-side MOSFETs and then creating spreadsheets is one way to determine relative efficiencies between different MOSFETs. Good correlation between the prediction and the bench result is not specified, however. Single-channel buck regulators that use a controller IC and discrete MOSFETs tend to be most efficient for output currents of 2A to 10A.

Losses in the high-side MOSFET can be broken down into conduction loss, gate charging loss, and switching loss. Conduction loss, or I^2R loss, is approximately:

$$P_C = D\ ((I_O)^2 \times R_{DSON\text{-}HI} \times 1.3)\ \text{(High-Side MOSFET)} \quad (26)$$

$$P_C = (1 - D) \times ((I_O)^2 \times R_{DSON\text{-}LO} \times 1.3)\ \text{(Low-Side MOSFET)} \quad (27)$$

In the above equations, the factor 1.3 accounts for the increase in MOSFET R_{DSON} due to heating. Alternatively, the 1.3 can be ignored and the R_{DSON} of the MOSFET estimated using the **R_{DSON} Vs. Temperature** curves in the MOSFET datasheets.

Gate charging loss results from the current driving the gate capacitance of the power MOSFETs, and is approximated as:

$$P_{GC} = n \times (V_{DD}) \times Q_G \times f_{SW} \quad (28)$$

where 'n' is the number of MOSFETs (if multiple devices have been placed in parallel), V_{DD} is the driving voltage (see *MOSFET Gate Drivers* section) and Q_{GS} is the gate charge of the MOSFET. If different types of MOSFETs are used, the *n* term can be ignored and their gate charges simply summed to form a cumulative Q_G. Gate charge loss differs from conduction and switching losses in that the actual dissipation occurs in the LM2743, and not in the MOSFET itself.

Switching loss occurs during the brief transition period as the high-side MOSFET turns on and off, during which both current and voltage are present in the channel of the MOSFET. It can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_O \times (t_r + t_f) \times f_{SW} \quad (29)$$

where t_R and t_F are the rise and fall times of the MOSFET. Switching loss occurs in the high-side MOSFET only.

For this example, the maximum drain-to-source voltage applied to either MOSFET is 3.6V. The maximum drive voltage at the gate of the high-side MOSFET is 3.1V, and the maximum drive voltage for the low-side MOSFET is 3.3V. Due to the low drive voltages in this example, a MOSFET that turns on fully with 3.1V of gate drive is needed. For designs of 5A and under, dual MOSFETs in SOIC-8 package provide a good trade-off between size, cost, and efficiency.

8.2.1.2.7 Support Components

C_{IN2} - A small value (0.1-µF to 1-µF) ceramic capacitor should be placed as close as possible to the drain of the high-side MOSFET and source of the low-side MOSFET (dual MOSFETs make this easy). This capacitor should be X5R type dielectric or better.

R_{CC}, C_{CC}- These are standard filter components designed to ensure smooth DC voltage for the chip supply. R_{CC} should be 1 Ω to 10 Ω. C_{CC} should 1 µF, X5R type or better.

C_{BOOT}- Bootstrap capacitor, typically 100 nF.

$R_{PULL\text{-}UP}$ – This is a standard pull-up resistor for the open-drain power good signal (PWGD). The recommended value is 10 kΩ connected to V_{CC}. If this feature is not necessary, the resistor can be omitted.

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Typical Applications (continued)

D_1 - A small Schottky diode should be used for the bootstrap. It allows for a minimum drop for both high and low-side drivers. The MBR0520 or BAT54 work well in most designs.

R_{CS} - Resistor used to set the current limit. Since the design calls for a peak current magnitude (I_{OUT}+ (0.5 x ΔI_{OUT})) of 4.8 A, a safe setting would be 6A. (This is below the saturation current of the output inductor, which is 7 A.) Following the equation from the *Current Limit* section, a 1.3-kΩ resistor should be used.

R_{FADJ} - This resistor is used to set the switching frequency of the chip. The resistor value is calculated from equation in *Normal Operation* section. For 300-kHz operation, a 97.6-kΩ resistor should be used.

C_{SS} - The soft-start capacitor depends on the user requirements and is calculated based on the equation given in the section titled *Start Up and Soft-Start*. Therefore, for a 700-µs delay, a 12-nF capacitor is suitable.

8.2.1.2.8 Control Loop Compensation

The LM2743 uses voltage-mode ('VM') PWM control to correct changes in output voltage due to line and load transients. One of the attractive advantages of voltage mode control is its relative immunity to noise and layout. However VM requires careful small signal compensation of the control loop for achieving high bandwidth and good phase margin.

The control loop is comprised of two parts. The first is the power stage, which consists of the duty cycle modulator, output inductor, output capacitor, and load. The second part is the error amplifier, which for the LM2743 is a 9-MHz op-amp used in the classic inverting configuration. Figure 32 shows the regulator and control loop components.

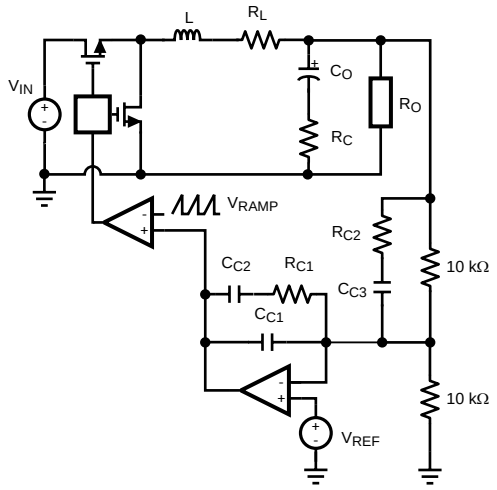


Figure 32. Power Stage and Error Amplifier

One popular method for selecting the compensation components is to create Bode plots of gain and phase for the power stage and error amplifier. Combined, they make the overall bandwidth and phase margin of the regulator easy to see. Software tools such as Excel, MathCAD, and Matlab are useful for showing how changes in compensation or the power stage affect system gain and phase.

The power stage modulator provides a DC gain A_{DC} that is equal to the input voltage divided by the peak-to-peak value of the PWM ramp. This ramp is 1.0VP-P for the LM2743. The inductor and output capacitor create a double pole at frequency f_{DP}, and the capacitor ESR and capacitance create a single zero at frequency f_{ESR}. For this example, with V_{IN} = 3.3 V, these quantities are:

$$A_{DC} = \frac{V_{IN}}{V_{RAMP}} = \frac{3.3}{1.0} = 10.4 \text{ dB} \tag{30}$$

$$f_{DP} = \frac{1}{2\pi}\sqrt{\frac{R_O + R_L}{LC_O(R_O + ESR)}} = 4.5 \text{ kHz} \tag{31}$$

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Typical Applications (continued)

$$f_{ESR} = \frac{1}{2\pi C_O ESR} = 20.3\ kHz \quad (32)$$

In the equation for f_{DP}, the variable R_L is the power stage resistance, and represents the inductor DCR plus the on resistance of the top power MOSFET. R_O is the output voltage divided by output current. The power stage transfer function G_{PS} is given by the following equation, and Figure 34 shows Bode plots of the phase and gain in this example.

$$G_{PS} = \frac{V_{IN} \times R_O}{V_{RAMP}} \times \frac{sC_O R_C + 1}{a \times s^2 + b \times s + c}$$

where

- $a = LC_O(R_O + R_C)$
- $b = L + C_O(R_O R_L + R_O R_C + R_C R_L)$
- $c = R_O + R_L$ (33)

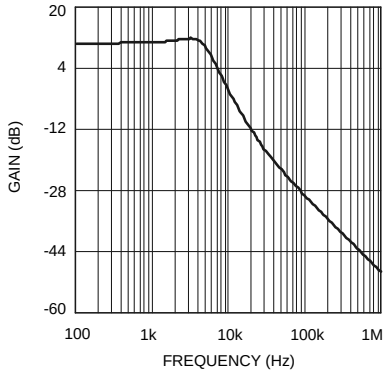


Figure 33. Gain vs Frequency

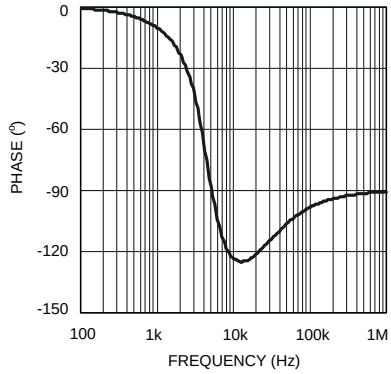


Figure 34. Power Stage Gain and Phase

The double pole at 4.5 kHz causes the phase to drop to approximately -130° at around 10 kHz. The ESR zero, at 20.3 kHz, provides a +90° boost that prevents the phase from dropping to -180º. If this loop were left uncompensated, the bandwidth would be approximately 10 kHz and the phase margin 53°. In theory, the loop would be stable, but would suffer from poor DC regulation (due to the low DC gain) and would be slow to respond to load transients (due to the low bandwidth.) In practice, the loop could easily become unstable due to tolerances in the output inductor, capacitor, or changes in output current, or input voltage. Therefore, the loop is compensated using the error amplifier and a few passive components.

For this example, a Type III, or three-pole-two-zero approach gives optimal bandwidth and phase.

In most voltage mode compensation schemes, including Type III, a single pole is placed at the origin to boost DC gain as high as possible. Two zeroes f_{Z1} and f_{Z2} are placed at the double pole frequency to cancel the double pole phase lag. Then, a pole, f_{P1} is placed at the frequency of the ESR zero. A final pole f_{P2} is placed at one-half of the switching frequency. The gain of the error amplifier transfer function is selected to give the best bandwidth possible without violating the Nyquist stability criteria. In practice, a good crossover point is one-fifth of the switching frequency, or 60 kHz for this example. The generic equation for the error amplifier transfer function is:

$$G_{EA} = A_{EA} \times \frac{\left(\frac{s}{2\pi f_{Z1}} + 1\right)\left(\frac{s}{2\pi f_{Z2}} + 1\right)}{s\left(\frac{s}{2\pi f_{P1}} + 1\right)\left(\frac{s}{2\pi f_{P2}} + 1\right)} \quad (34)$$

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Typical Applications (continued)

In this equation, the variable A_{EA} is a ratio of the values of the capacitance and resistance of the compensation components, arranged as shown in Figure 32. A_{EA} is selected to provide the desired bandwidth. A starting value of 80,000 for A_{EA} should give a conservative bandwidth. Increasing the value will increase the bandwidth, but will also decrease phase margin. Designs with 45° to 60° are usually best because they represent a good trade-off between bandwidth and phase margin. In general, phase margin is lowest and gain highest (worst-case) for maximum input voltage and minimum output current. One method to select A_{EA} is to use an iterative process beginning with these worst-case conditions.

1. Increase A_{EA}
2. Check overall bandwidth and phase margin
3. Change V_{IN} to minimum and recheck overall bandwidth and phase margin
4. Change I_O to maximum and recheck overall bandwidth and phase margin

The process ends when the both bandwidth and the phase margin are sufficiently high. For this example input voltage can vary from 3.0 to 3.6 V and output current can vary from 0 to 4 A, and after a few iterations a moderate gain factor of 101 dB is used.

The error amplifier of the LM2743 has a unity-gain bandwidth of 9 MHz. In order to model the effect of this limitation, the open-loop gain can be calculated as:

$$OPG = \frac{2\pi \times 9\ MHz}{s} \tag{35}$$

The new error amplifier transfer function that takes into account unity-gain bandwidth is:

$$H_{EA} = \frac{G_{EA} \times OPG}{1 + G_{EA} + OPG} \tag{36}$$

The gain and phase of the error amplifier are shown in Figure 36.

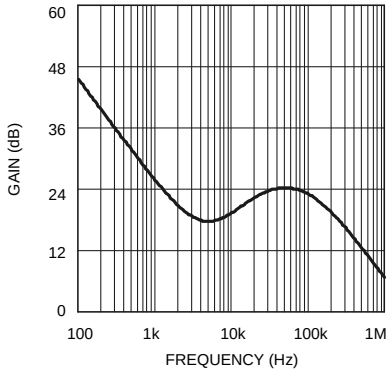


Figure 35. Gain vs Frequency

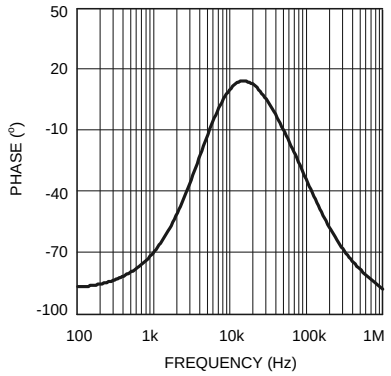


Figure 36. Error Amplifier Gain and Phase

In VM regulators, the top feedback resistor R_{FB2} forms a part of the compensation. Setting R_{FB2} to 10 kΩ, ±1% usually gives values for the other compensation resistors and capacitors that fall within a reasonable range. (Capacitances > 1 pF, resistances < 1 MΩ) C_{C1}, C_{C2}, C_{C3}, R_{C1}, and R_{C2} are selected to provide the poles and zeroes at the desired frequencies, using the following equations:

$$C_{C1} = \frac{f_{Z1}}{A_{EA} \times 10{,}000 \times f_{P2}} = 27\ pF \tag{37}$$

$$C_{C2} = \frac{1}{A_{EA} \times 10{,}000} - C_{C1} = 882\ pF \tag{38}$$

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Typical Applications (continued)

$$C_{C3} = \frac{1}{2\pi \times 10{,}000} \times \left(\frac{1}{f_{Z2}} - \frac{1}{f_{P1}}\right) = 2.73 \text{ nF} \quad (39)$$

$$R_{C1} = \frac{1}{2\pi \times C_{C2} \times f_{Z1}} = 39.8 \text{ k}\Omega \quad (40)$$

$$R_{C2} = \frac{1}{2\pi \times C_{C3} \times f_{P1}} = 2.55 \text{ k}\Omega \quad (41)$$

In practice, a good trade off between phase margin and bandwidth can be obtained by selecting the closest ±10% capacitor values above what are suggested for C_{C1} and C_{C2}, the closest ±10% capacitor value below the suggestion for C_{C3}, and the closest ±1% resistor values below the suggestions for R_{C1}, R_{C2}. Note that if the suggested value for R_{C2} is less than 100Ω, it should be replaced by a short circuit. Following this guideline, the compensation components will be:

C_{C1} = 27 pF ±10%

C_{C2} = 820 pF ±10%

C_{C3} = 2.7 nF ±10%

R_{C1} = 39.2 kΩ ±1%

R_{C2} = 2.55 kΩ ±1%

The transfer function of the compensation block can be derived by considering the compensation components as impedance blocks Z_F and Z_I around an inverting op-amp:

$$G_{EA\text{-}ACTUAL} = \frac{Z_F}{Z_I} \quad (42)$$

$$Z_F = \frac{\frac{1}{sC_{C1}} \times \left(10{,}000 + \frac{1}{sC_{C2}}\right)}{10{,}000 + \frac{1}{sC_{C1}} + \frac{1}{sC_{C2}}} \quad (43)$$

$$Z_1 = \frac{R_{C1}\left(R_{C2} + \frac{1}{sC_{C3}}\right)}{R_{C1} + R_{C2} + \frac{1}{sC_{C3}}} \quad (44)$$

As with the generic equation, $G_{EA\text{-}ACTUAL}$ must be modified to take into account the limited bandwidth of the error amplifier. The result is:

$$H_{EA} = \frac{G_{EA\text{-}ACTUAL} \times OPG}{1 + G_{EA\text{-}ACTUAL} + OPG} \quad (45)$$

The total control loop transfer function H is equal to the power stage transfer function multiplied by the error amplifier transfer function.

$$H = G_{PS} \times H_{EA} \quad (46)$$

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Typical Applications (continued)

The bandwidth and phase margin can be read graphically from Bode plots of H_{EA} are shown in Figure 38.

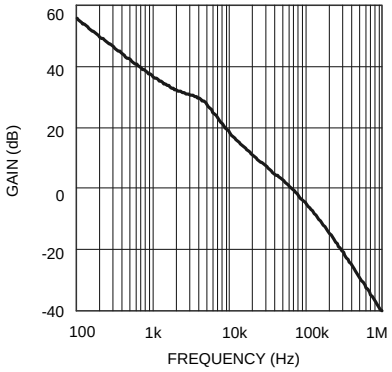


Figure 37. Gain vs Frequency

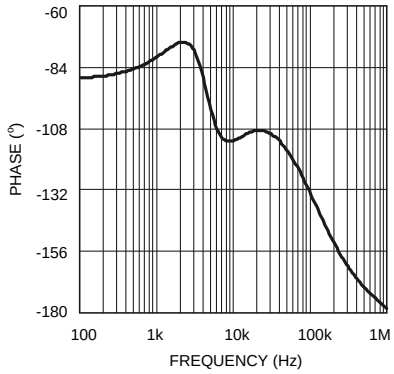


Figure 38. Overall Loop Gain and Phase

The bandwidth of this example circuit is 59 kHz, with a phase margin of 60°.

8.2.1.2.9 Efficiency Calculations

The following is a sample calculation.

A reasonable estimation of the efficiency of a switching buck controller can be obtained by adding together the Output Power (P_{OUT}) loss and the Total Power (P_{TOTAL}) loss:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{TOTAL}} \times 100\% \quad (47)$$

The Output Power (P_{OUT}) for the Figure 30 design is (1.2 V x 4 A) = 4.8 W. The Total Power (P_{TOTAL}), with an efficiency calculation to complement the design, is shown below.

The majority of the power losses are due to low and high side of MOSFET's losses. The losses in any MOSFET are group of switching (P_{SW}) and conduction losses(P_{CND}).

$$P_{FET} = P_{SW} + P_{CND} = 61.38\ mW + 270.42\ mW \quad (48)$$

$$P_{FET} = 331.8\ mW \quad (49)$$

The following equations show FET Switching Loss (P_{SW}).

$$P_{SW} = P_{SW(ON)} + P_{SW(OFF)} \quad (50)$$

$$P_{SW} = 0.5 \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW} \quad (51)$$

$$P_{SW} = 0.5 \times 3.3\ V \times 4\ A \times 300\ kHz \times 31\ ns \quad (52)$$

$$P_{SW} = 61.38\ mW \quad (53)$$

The FDS6898A has a typical turn-on rise time t_r and turn-off fall time t_f of 15 ns and 16 ns, respectively. The switching losses for this type of dual N-Channel MOSFETs are 0.061 W.

The following equations show FET Conduction Loss (P_{CND}).

$$P_{CND} = P_{CND1} + P_{CND2} \quad (54)$$

$$P_{CND1} = (I_{OUT})^2 \times R_{DS(ON)} \times k \times D \quad (55)$$

$$P_{CND2} = (I_{OUT})^2 \times R_{DS(ON)} \times k \times (1\text{-}D) \quad (56)$$

$R_{DS(ON)}$ = 13 mΩ and the factor is a constant value (k = 1.3) to account for the increasing $R_{DS(ON)}$ of a FET due to heating.

$$P_{CND1} = (4A)^2 \times 13\ m\Omega \times 1.3 \times 0.364 \quad (57)$$

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Typical Applications (continued)

$$P_{CND2} = (4A)^2 \times 13\ m\Omega \times 1.3 \times (1 - 0.364) \quad (58)$$

$$P_{CND} = 98.42\ mW + 172\ mW = 270.42\ mW \quad (59)$$

There are few additional losses that are taken into account:

The following equations show IC Operating Loss (P_{IC}).

$$P_{IC} = I_{Q_VCC} \times V_{CC}, \quad (60)$$

where $I_{Q\text{-}VCC}$ is the typical operating V_{CC} current

$$P_{IC} = 1.5\ mA \times 3.3V = 4.95\ mW \quad (61)$$

The following equations show FET Gate Charging Loss (P_{GATE}).

$$P_{GATE} = n \times V_{CC} \times Q_{GS} \times f_{SW} \quad (62)$$

$$P_{GATE} = 2 \times 3.3\ V \times 3\ nC \times 300\ kHz \quad (63)$$

$$P_{GATE} = 5.94\ mW \quad (64)$$

The value n is the total number of FETs used and Q_{GS} is the typical gate-source charge value, which is 3 nC. For the FDS6898A the gate charging loss is 5.94 mW.

The following equations show Input Capacitor Loss (P_{CAP}).

$$P_{CAP} = \frac{(I_{RMS_RIP})^2 \times ESR}{n^2}$$

where (65)

$$I_{RMS_RIP} = I_{OUT} \times \sqrt{D(1 - D)} \quad (66)$$

Here n is the number of paralleled capacitors, ESR is the equivalent series resistance of each, and P_{CAP} is the dissipation in each. So for example if we use only one input capacitor of 24 mΩ.

$$P_{CAP} = \frac{(1.924A)^2 \times 24\ m\Omega}{1^2} \quad (67)$$

$$P_{CAP} = 88.8\ mW \quad (68)$$

The following equation shows Output Inductor Loss (P_{IND}).

$$P_{IND} = I^2_{OUT} \times DCR \quad (69)$$

where DCR is the DC resistance. Therefore, for example

$$P_{IND} = (4A)^2 \times 11\ m\Omega \quad (70)$$

$$P_{IND} = 176\ mW \quad (71)$$

The following equations show Total System Efficiency.

$$P_{TOTAL} = P_{FET} + P_{IC} + P_{GATE} + P_{CAP} + P_{IND} \quad (72)$$

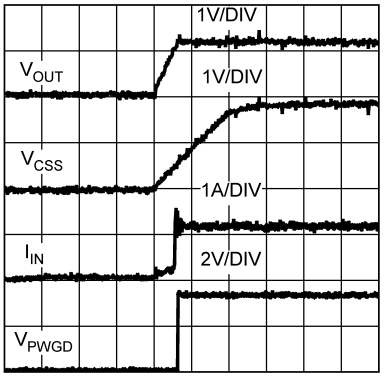
$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{TOTAL}} \times 100\% \quad (73)$$

$$\eta = \frac{4.8W}{4.8W + 0.6W} = 89\% \quad (74)$$

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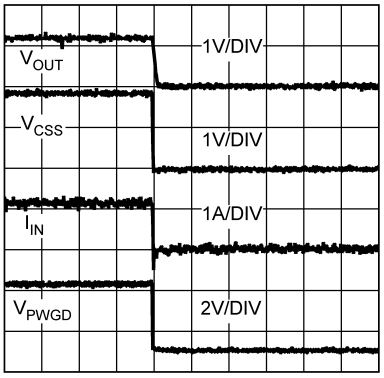
Typical Applications (continued)

8.2.1.3 Application Curves



V_{CC} = 3.3V V_{OUT} = 1.2V
I_{OUT} = 4A C_{SS} = 12nF f_{SW} = 300 kHz

Figure 39. Start-Up (Full-Load)



V_{CC} = 3.3 V V_{OUT} = 1.2 V
I_{OUT} = 4 A C_{SS} = 12 nF f_{SW} = 300 kHz

Figure 40. Shutdown (Full-Load)

8.2.2 Example Circuit 1

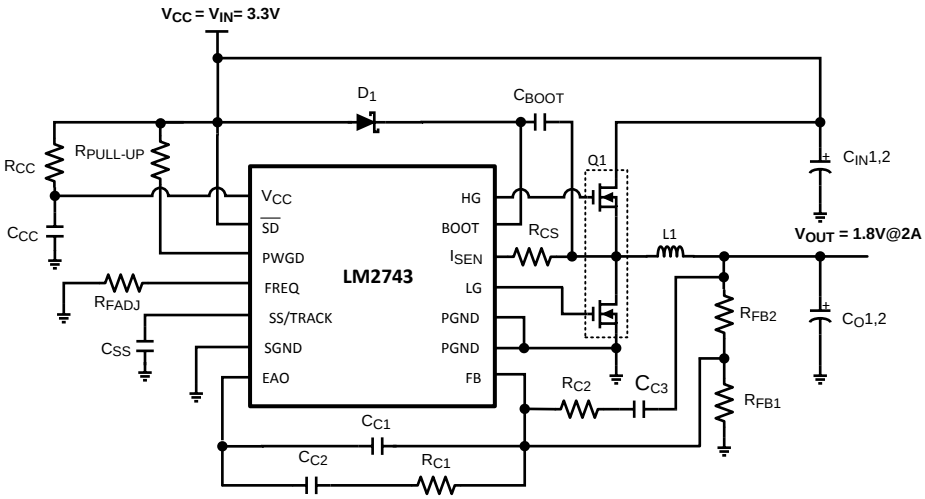


Figure 41. 3.3 V to 1.8 V at 2 A, f_{SW} = 300 kHz

8.2.2.1 Design Requirements

This design converts 3.3 V (V_{IN}) to 1.8 V (V_{OUT}) at a maximum load of 2 A, with a switching frequency of 300 kHz.

8.2.2.2 Detailed Design Procedure

Follow the detailed design procedure in *Detailed Design Procedure*.

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Typical Applications (continued)

8.2.2.3 Bill of Materials

Table 1. Bill of Materials

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
U1	LM2743	Synchronous Controller	TSSOP-14		TI
Q1	FDS6898A	Dual N-MOSFET	SOIC-8	20 V, 10 mΩ at 4.5 V, 16 nC	Fairchild
D1	MBR0520LTI	Schottky Diode	SOD-123		
L1	DO3316P-472	Inductor		4.7 µH, 4.8 Arms, 18 mΩ	Coilcraft
$C_{IN}1$	16SP100M	Aluminum Electrolytic	10mm x 6mm	100 µF, 16 V, 2.89 Arms	Sanyo
C_O1	6SP220M	Aluminum Electrolytic	10mm x 6mm	220 µF, 6.3 V, 3.1 Arms	Sanyo
C_{CC}, C_{BOOT}, $C_{IN}2$, C_O2	VJ1206Y104KXXA	Capacitor	1206	0.1 µF, 10%	Vishay
C_{C3}	VJ0805Y332KXXA	Capacitor	805	3300 pF, 10%	Vishay
C_{SS}	VJ0805A123KXAA	Capacitor	805	12 nF, 10%	Vishay
C_{C2}	VJ0805A821KXAA	Capacitor	805	820 pF 10%	Vishay
C_{C1}	VJ0805A220KXAA	Capacitor	805	22 pF, 10%	Vishay
R_{FB2}	CRCW08051002F	Resistor	805	10.0 kΩ 1%	Vishay
R_{FB1}	CRCW08054991F	Resistor	805	4.99 kΩ1%	Vishay
R_{FADJ}	CRCW08051103F	Resistor	805	110 kΩ 1%	Vishay
R_{C2}	CRCW08052101F	Resistor	805	2.1 kΩ 1%	Vishay
R_{CS}	CRCW08052101F	Resistor	805	2.1 kΩ 1%	Vishay
R_{CC}	CRCW080510R0F	Resistor	805	10.0 Ω 1%	Vishay
R_{C1}	CRCW08055492F	Resistor	805	54.9 kΩ 1%	Vishay
$R_{PULL-UP}$	CRCW08051003J	Resistor	805	100 kΩ 5%	Vishay

8.2.3 Example Circuit 2

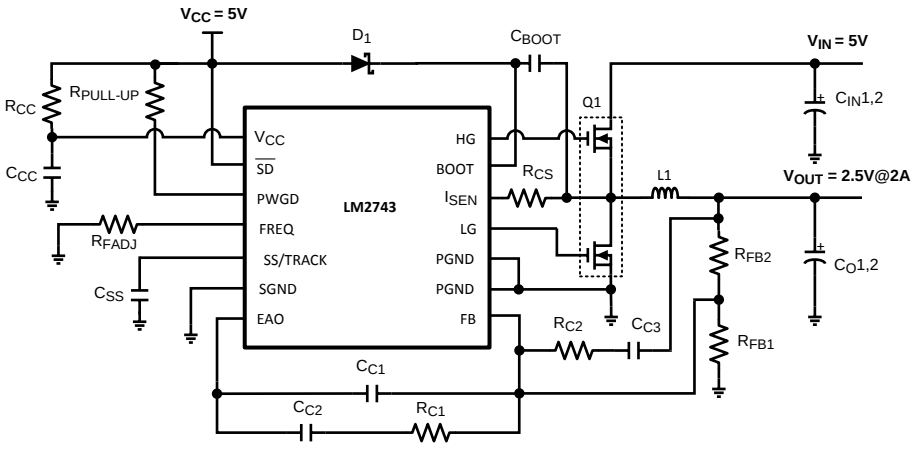


Figure 42. 5 V to 2.5 V at 2A, f_{SW} = 300kHz

8.2.3.1 Design Requirements

This design converts 5 V (V_{IN}) to 2.5 V (V_{OUT}) at a maximum load of 2 A, with a switching frequency of 300 kHz.

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8.2.3.2 Detailed Design Procedure

Follow the detailed design procedure in *Detailed Design Procedure*.

8.2.3.3 Bill of Materials

Table 2. Bill of Materials

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
U1	LM2743	Synchronous Controller	TSSOP-14		TI
Q1	FDS6898A	Dual N-MOSFET	SOIC-8	20 V, 10 mΩ at 4.5 V, 16 nC	Fairchild
D1	MBR0520LTI	Schottky Diode	SOD-123		
L1	DO3316P-682	Inductor		6.8 µH, 4.4 Arms, 27 mΩ	Coilcraft
$C_{IN}1$	16SP100M	Aluminum Electrolytic	10mm x 6mm	100 µF, 16 V, 2.89 Arms	Sanyo
C_O1	10SP56M	Aluminum Electrolytic	6.3mm x 6mm	56 µF, 10 V, 1.7 Arms	Sanyo
C_{CC}, C_{BOOT}, $C_{IN}2$, C_O2	VJ1206Y104KXXA	Capacitor	1206	0.1 µF, 10%	Vishay
C_{C3}	VJ0805Y182KXXA	Capacitor	805	1800 pF, 10%	Vishay
C_{SS}	VJ0805A123KXAA	Capacitor	805	12 nF, 10%	Vishay
C_{C2}	VJ0805A821KXAA	Capacitor	805	820 pF 10%	Vishay
C_{C1}	VJ0805A330KXAA	Capacitor	805	33 pF, 10%	Vishay
R_{FB2}	CRCW08051002F	Resistor	805	10.0 kΩ 1%	Vishay
R_{FB1}	CRCW08053161F	Resistor	805	3.16 kΩ 1%	Vishay
R_{FADJ}	CRCW08051103F	Resistor	805	110 kΩ 1%	Vishay
R_{C2}	CRCW08051301F	Resistor	805	1.3 kΩ 1%	Vishay
R_{CS}	CRCW08052101F	Resistor	805	2.1 kΩ 1%	Vishay
R_{CC}	CRCW080510R0F	Resistor	805	10.0 Ω 1%	Vishay
R_{C1}	CRCW08053322F	Resistor	805	33.2 kΩ 1%	Vishay
$R_{PULL-UP}$	CRCW08051003J	Resistor	805	100 kΩ 5%	Vishay

8.2.4 Example Circuit 3

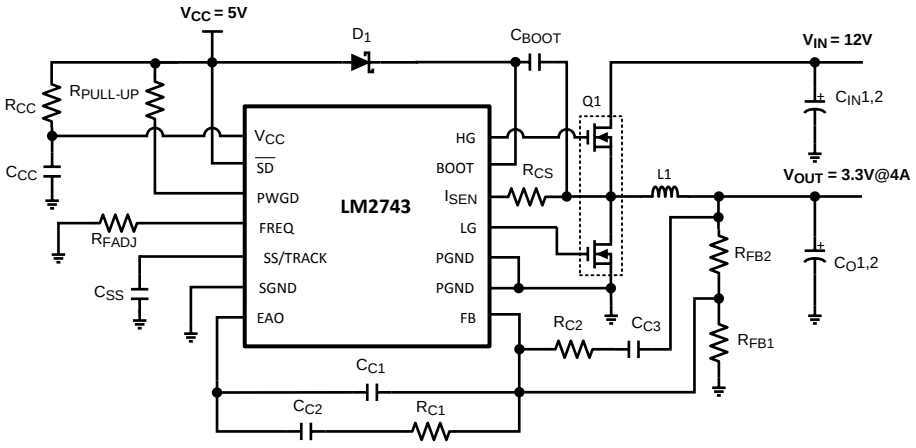


Figure 43. 12 V to 3.3 V at 4 A, f_{SW} = 300 kHz

8.2.4.1 Design Requirements

This design converts 12 V (V_{IN}) to 3.3 V (V_{OUT}) at a maximum load of 4 A, with a switching frequency of 300 kHz.

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8.2.4.2 Detailed Design Procedure

Follow the detailed design procedure in *Detailed Design Procedure*.

8.2.4.3 Bill of Materials

Table 3. Bill of Materials

PART	PART NUMBER	TYPE	PACKAGE	DESCRIPTION	VENDOR
U1	LM2743	Synchronous Controller	TSSOP-14		TI
Q1	FDS6898A	Dual N-MOSFET	SOIC-8	20 V, 10 mΩ at 4.5 V, 16 nC	Fairchild
D1	MBR0520LTI	Schottky Diode	SOD-123		
L1	DO3316P-332	Inductor		3.3 µH, 5.4 Arms, 15 mΩ	Coilcraft
$C_{IN}1$	16SP100M	Aluminum Electrolytic	10 mm x 6 mm	100 µF, 16 V, 2.89 Arms	Sanyo
C_O1	6SP220M	Aluminum Electrolytic	10 mm x 6 mm	220 µF, 6.3 V 3.1 Arms	Sanyo
C_{CC}, C_{BOOT}, $C_{IN}2$, C_O2	VJ1206Y104KXXA	Capacitor	1206	0.1 µF, 10%	Vishay
C_{C3}	VJ0805Y222KXXA	Capacitor	805	2200 pF, 10%	Vishay
C_{SS}	VJ0805A123KXAA	Capacitor	805	12 nF, 10%	Vishay
C_{C2}	VJ0805Y332KXXA	Capacitor	805	3300 pF 10%	Vishay
C_{C1}	VJ0805A820KXAA	Capacitor	805	82 pF, 10%	Vishay
R_{FB2}	CRCW08051002F	Resistor	805	10.0 kΩ 1%	Vishay
R_{FB1}	CRCW08052211F	Resistor	805	2.21 kΩ 1%	Vishay
R_{FADJ}	CRCW08051103F	Resistor	805	110 kΩ 1%	Vishay
R_{C2}	CRCW08052611F	Resistor	805	2.61 kΩ 1%	Vishay
R_{CS}	CRCW08054121F	Resistor	805	4.12 kΩ 1%	Vishay
R_{CC}	CRCW080510R0F	Resistor	805	10.0 Ω 1%	Vishay
R_{C1}	CRCW08051272F	Resistor	805	12.7 kΩ 1%	Vishay
$R_{PULL-UP}$	CRCW08051003J	Resistor	805	100 kΩ 5%	Vishay

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9 Power Supply Recommendations

The LM2743 is a power management device. The power supply for the device is any DC voltage source within the specified input range (see *Design Requirements*).

10 Layout

10.1 Layout Guidelines

In a buck regulator, the primary switching loop consists of the input capacitor and MOSFET switches. Minimixing the area of this loop reduces the stray inductance, and minimizes noise and possible erratic operation. High quality input capacitors should be placed as close as possible to the MOSFET switches, with the positive side of the input capacitor connected directly to the high-side MOSFET drain, and the ground side of the capacitor connected as close as possible to the low-side MOSFET switch ground connection. Connect all of the low power ground connections directly to the SGND pin. Connect the VCC capacitor directly to the PGND pin.

10.2 Layout Example

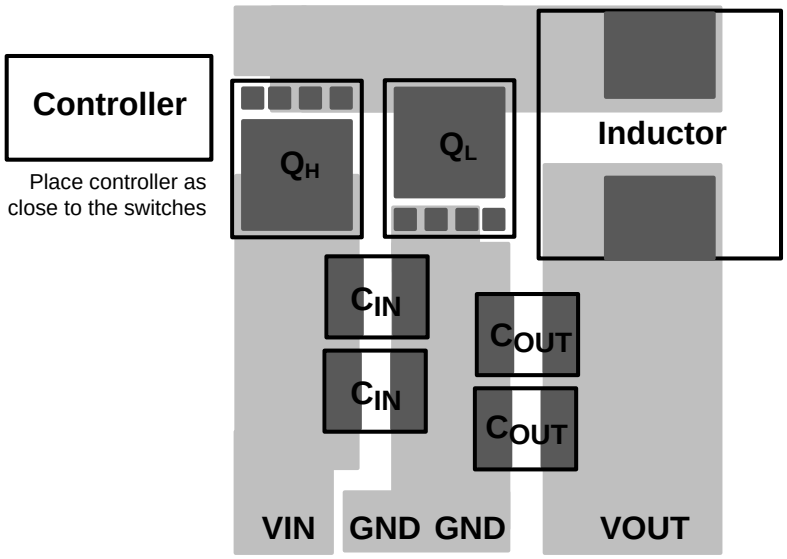


Figure 44. Layout Recommendation

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 使用 WEBENCH® 工具创建定制设计

请单击此处，使用 LM2743 器件并借助 WEBENCH® 电源设计器创建定制设计。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

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WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2743MTC/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2743 MTC
LM2743MTC/NOPB.A	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2743 MTC
LM2743MTC/NOPB.B	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2743 MTC
LM2743MTCX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2743 MTC
LM2743MTCX/NOPB.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2743 MTC
LM2743MTCX/NOPB.B	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2743 MTC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

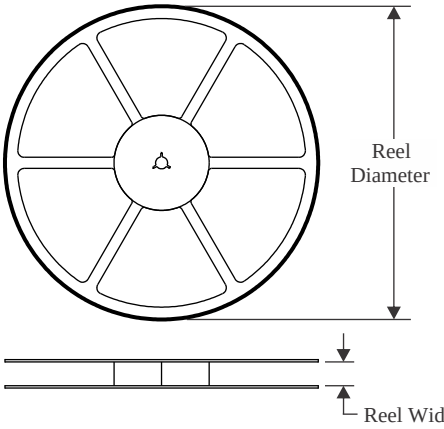
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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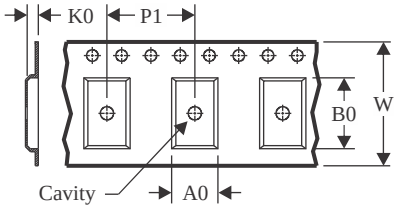
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

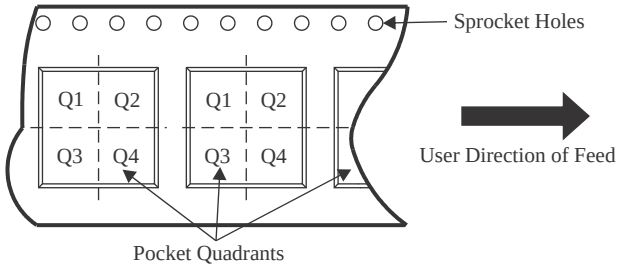


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

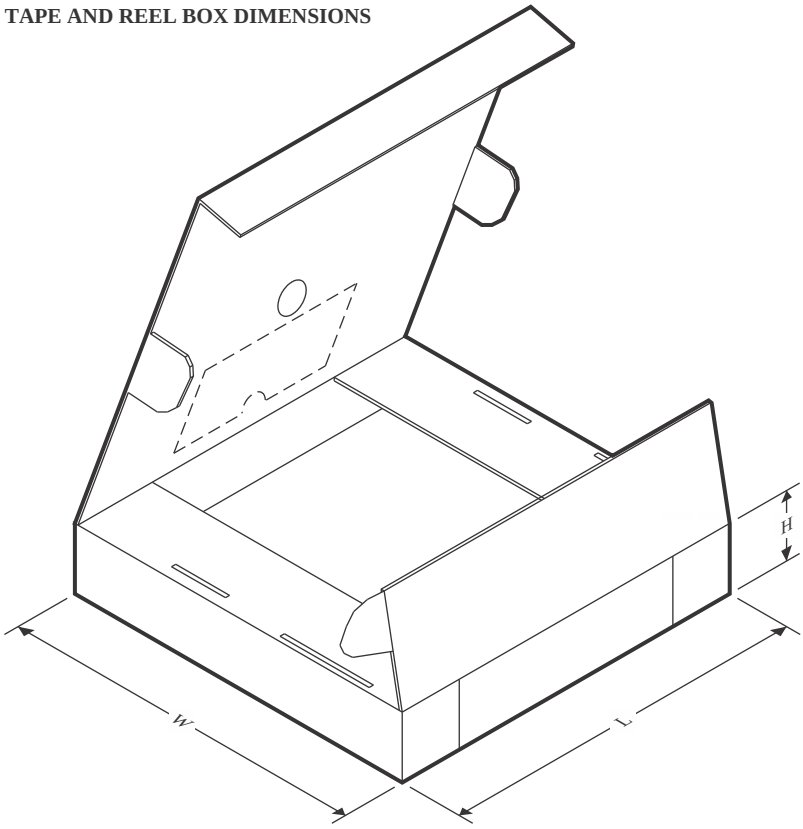
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2743MTCX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2743MTCX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

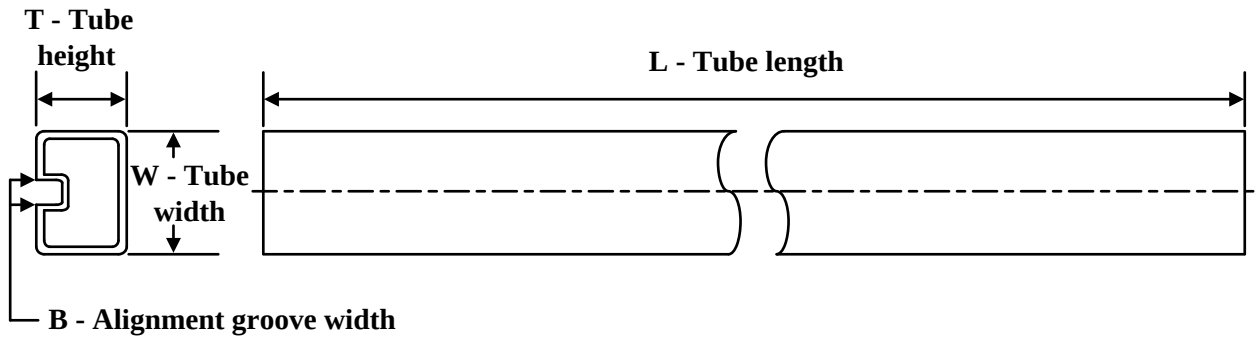
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2743MTCX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LM2743MTCX/NOPB	TSSOP	PW	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

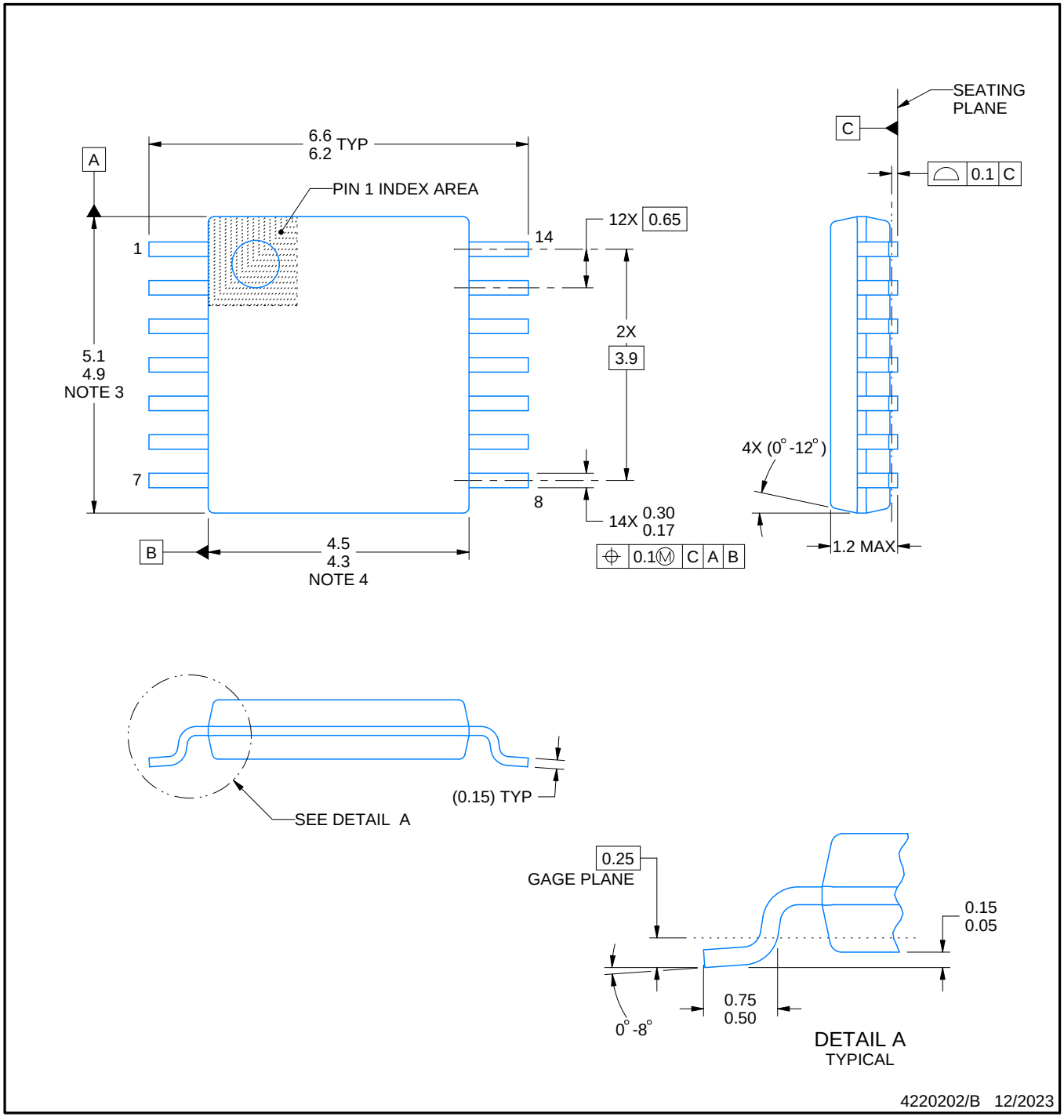
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2743MTC/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LM2743MTC/NOPB	PW	TSSOP	14	94	530	10.2	3600	3.5
LM2743MTC/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LM2743MTC/NOPB.A	PW	TSSOP	14	94	495	8	2514.6	4.06
LM2743MTC/NOPB.A	PW	TSSOP	14	94	495	8	2514.6	4.06
LM2743MTC/NOPB.A	PW	TSSOP	14	94	530	10.2	3600	3.5
LM2743MTC/NOPB.B	PW	TSSOP	14	94	495	8	2514.6	4.06
LM2743MTC/NOPB.B	PW	TSSOP	14	94	495	8	2514.6	4.06
LM2743MTC/NOPB.B	PW	TSSOP	14	94	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

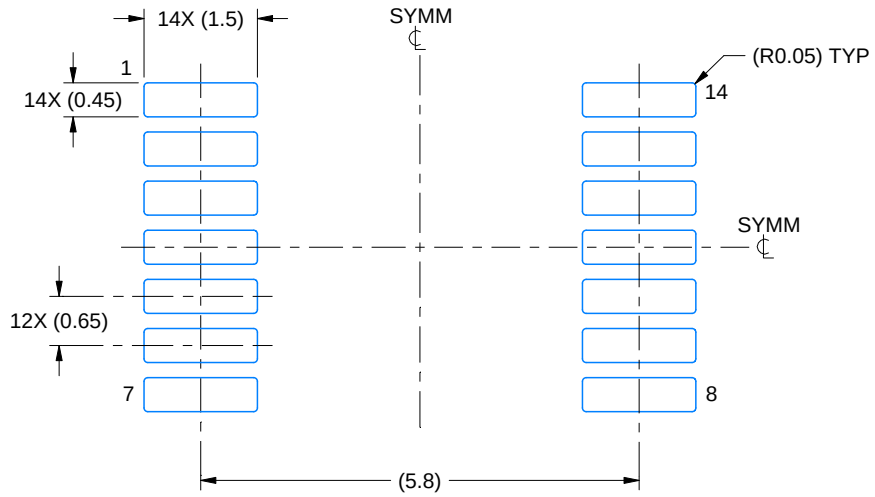
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

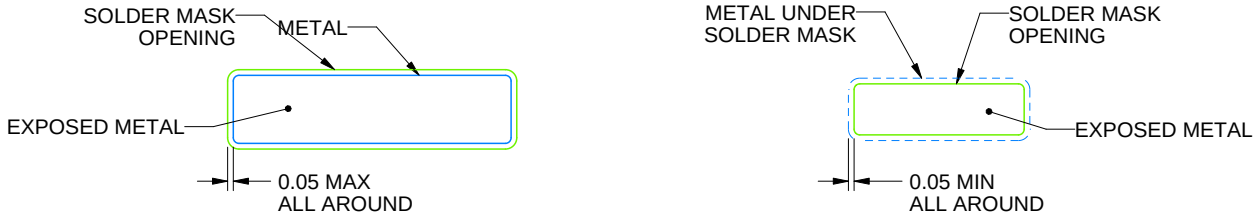


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

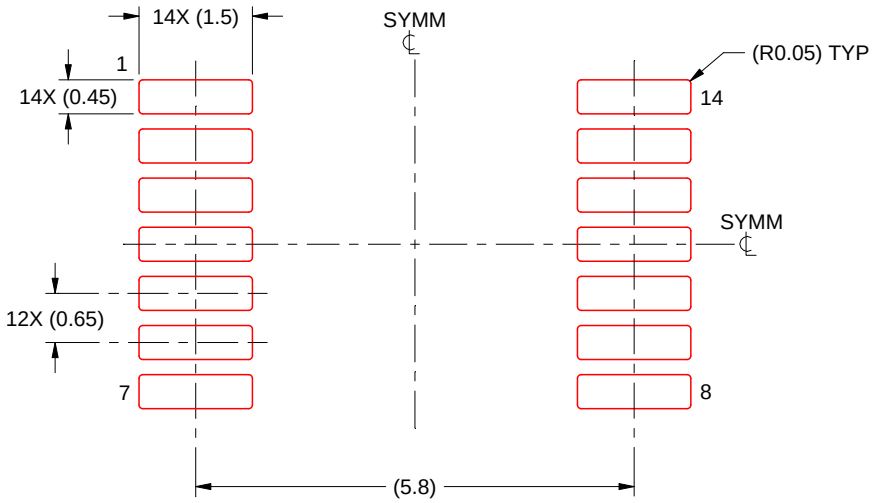


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月