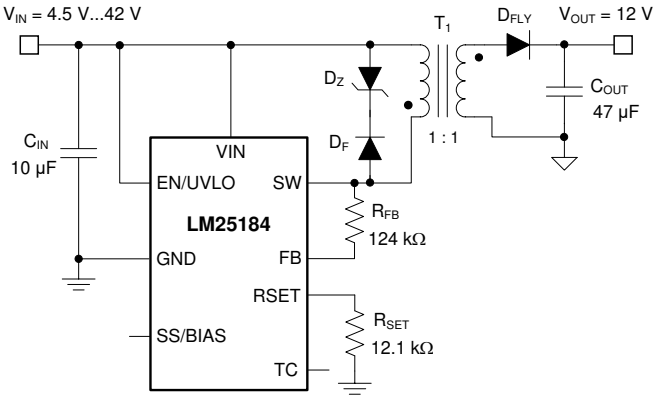
具有 65V、4.1A 功率 MOSFET 的 LM25184 42V_{IN} PSR 反激式直流/直流转换器

1 特性

- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 专为可靠耐用的应用而设计
  - 4.5V 至 42V 的宽输入电压范围，启动后的工作电压低至 3.5V
  - 稳定可靠的解决方案，只有一个元件穿过隔离层
  - ±1.5% 的总输出稳压精度
  - 可选 V_{OUT} 温度补偿
  - 具有 –40°C 至 +150°C 的结温范围
- 通过集成技术减小解决方案尺寸，降低成本
  - 集成 65V、0.11Ω 功率 MOSFET
  - 无需光耦合器或变压器辅助绕组即可进行 V_{OUT} 稳压
  - 内部环路补偿
- 高效率 PSR 反激运行
  - MOSFET 在 BCM 模式下实现准谐振关断
  - 具有用于提升效率的外部偏置选项
  - 具有单输出和多输出实施手段
- 超低的 EMI 传导和辐射信号
  - 软开关可避免二极管反向恢复
  - 针对 CISPR 32 EMI 要求进行了优化
- 使用 WEBENCH® Power Designer 创建定制反激式稳压器设计方案

2 应用

- 电机驱动器：IGBT 和 SiC 栅极驱动器电源
- 隔离式现场发送器和现场传动器
- 隔离式偏置电源轨



典型应用

3 说明

LM25184 是一款初级侧调节 (PSR) 反激式转换器，在 4.5V 至 42V 的宽输入电压范围内具有高效率，可通过初级侧反激式电压对隔离输出电压采样。高集成度可实现简单可靠的高密度设计，其中只有一个元件穿过隔离层。通过采用边界导电模式 (BCM) 开关，可实现紧凑的磁解决方案以及优于 ±1.5% 的负载和线路调节性能。集成的 65V 功率 MOSFET 可提供高达 15W 的输出功率并提高应对线路瞬变的余量。

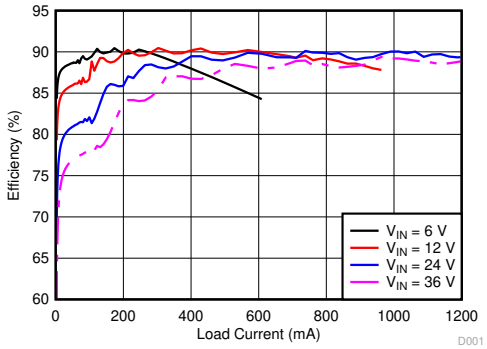
LM25184 简化了隔离式直流/直流电源的实施，且可通过可选功能优化目标终端设备的性能。该器件通过一个电阻器来设置输出电压，同时使用可选的电阻器通过抵消反激式二极管的压降热系数来提高输出电压精度。其他功能包括内部固定或外部可编程软启动、用于可调节线路 UVLO 的精密使能输入（带迟滞功能）、间断模式过载保护和带自动恢复功能的热关断保护。

LM25184 反激式转换器采用 8 引脚 4mm × 4mm 热增强型 WSON 封装（引脚间距为 0.8mm）。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
LM25184	WSON (8)	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型效率 (V_{OUT} = 12V)

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (March 2020) to Revision A (August 2020)	Page
• 将器件状态从“预告信息”更改为“量产数据”	1
• 更新了整个文档中的表格、图和交叉参考的编号格式。	1

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5 Pin Configuration and Functions

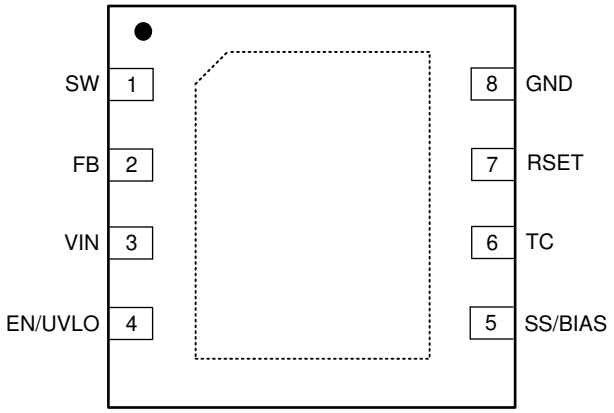

图 5-1. 8-Pin WSON NGU Package With Wettable Flanks (Top View)

Pin Functions

PIN		I/O[(1)]	DESCRIPTION
NO.	NAME		
1	SW	P	Switch node that is internally connected to the drain of the N-channel power MOSFET. Connect to the primary-side switching terminal of the flyback transformer.
2	FB	I	Primary-side feedback pin. Connect a resistor from FB to SW. The ratio of the FB resistor to the resistor at the RSET pin sets the output voltage.
3	VIN	P/I	Input supply connection. Source for internal bias regulators and input voltage sensing pin. Connect directly to the input supply of the converter with short, low impedance paths.
4	EN/UVLO	I	Enable input and undervoltage lockout (UVLO) programming pin. If the EN/UVLO voltage is below 1 V, the converter is in shutdown mode with all functions disabled. If the EN/UVLO voltage is greater than 1 V and below 1.5 V, the converter is in standby mode with the internal regulator operational and no switching. If the EN/UVLO voltage is above 1.5 V, the start-up sequence begins.
5	SS/BIAS	I	Soft start or bias input. Connect a capacitor from SS/BIAS to GND to adjust the output start-up time and input inrush current. If SS/BIAS is left open, the internal 6-ms soft-start timer is activated. Connect an external supply to SS/BIAS to supply bias to the internal voltage regulator and enable internal soft start.
6	TC	I	Temperature compensation pin. Tie a resistor from TC to RSET to compensate for the temperature coefficient of the forward voltage drop of the secondary diode, thus improving regulation at the secondary-side output.
7	RSET	I	Reference resistor tied to GND to set the reference current for FB. Connect a 12.1-kΩ resistor from RSET to GND.
8	GND	G	Analog and power ground. Ground connection of internal control circuits and power MOSFET.

(1) P = Power, G = Ground, I = Input, O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	VIN to GND	–0.3	45	V
	EN/UVLO to GND	–0.3	45	
	TC to GND	–0.3	6	
	SS/BIAS to GND	–0.3	14	
	FB to GND	–0.3	45.3	
	FB to VIN	–0.3	0.3	
	RSET to GND	–0.3	3	
Output voltage	SW to GND	–1.5	70	V
	SW to GND (20-ns transient)	–3		
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, HBM ESD Classification Level 2[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, CDM ESD Classification Level C4B[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	4.5		42	V
V_{SW}	SW voltage			65	V
$V_{EN/UVLO}$	EN/UVLO voltage			42	V
$V_{SS/BIAS}$	SS/BIAS voltage			13	V
T_J	Operating junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM25184 NGU (WSON) 8 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	40.9	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	36.9	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	17.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.7	°C/W

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THERMAL METRIC[1]		LM25184 NGU (WSON) 8 PINS	UNIT
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits aaply over the full –40°C to 150°C junction temperature range unless otherwise indicated. V_{IN} = 12 V and $V_{EN/UVLO}$ = 2 V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{SHUTDOWN}$	VIN shutdown current	$V_{EN/UVLO}$ = 0 V		1.8		μA
I_{ACTIVE}	VIN active current	$V_{EN/UVLO}$ = 2.5 V, V_{RSET} = 1.8 V		260	375	μA
$I_{ACTIVE-BIAS}$	VIN current with BIAS connected	$V_{SS/BIAS}$ = 5 V		25	50	μA
ENABLE AND INPUT UVLO						
$V_{SD-FALLING}$	Shutdown threshold	$V_{EN/UVLO}$ falling	0.3			V
$V_{SD-RISING}$	Standby threshold	$V_{EN/UVLO}$ rising		0.8	1	V
$V_{UV-RISING}$	Enable threshold	$V_{EN/UVLO}$ rising	1.45	1.5	1.53	V
$V_{UV-HYST}$	Enable voltage hysteresis	$V_{EN/UVLO}$ falling	0.04	0.05		V
$I_{UV-HYST}$	Enable current hysteresis	$V_{EN/UVLO}$ = 1.6 V	4.2	5	5.5	μA
FEEDBACK						
I_{RSET}	RSET current	R_{RSET} = 12.1 kΩ		100		μA
V_{RSET}	RSET regulation voltage	R_{RSET} = 12.1 kΩ	1.194	1.21	1.22	V
$V_{FB-VIN1}$	FB to VIN voltage	I_{FB} = 80 μA	–50			mV
$V_{FB-VIN2}$	FB to VIN voltage	I_{FB} = 120 μA			50	mV
SWITCHING FREQUENCY						
F_{SW-MIN}	Minimum switching frequency			12		kHz
F_{SW-MAX}	Maximum switching frequency			350		kHz
t_{ON-MIN}	Minimum switch on-time			140		ns
DIODE THERMAL COMPENSATION						
V_{TC}	TC voltage	I_{TC} = ±10 μA, T_J = 25°C		1.2	1.27	V
POWER SWITCHES						
$R_{DS(on)}$	MOSFET on-state resistance	I_{SW} = 100 mA, T_J = 25°C		0.11	0.135	Ω
SOFT-START AND BIAS						
I_{SS}	SS ext capacitor charging current			5		μA
t_{SS}	Internal SS time			6		ms
$V_{BIAS-UVLO-RISE}$	BIAS enable voltage	$V_{SS/BIAS}$ rising		4.25	4.45	V
$V_{BIAS-UVLO-HYST}$	BIAS UVLO hysteresis	$V_{SS/BIAS}$ falling		130		mV
CURRENT LIMIT						
$I_{SW-PEAK}$	Peak current limit threshold		3.6	4.1	4.4	A
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD-HYS}	Thermal shutdown hysteresis			10		°C

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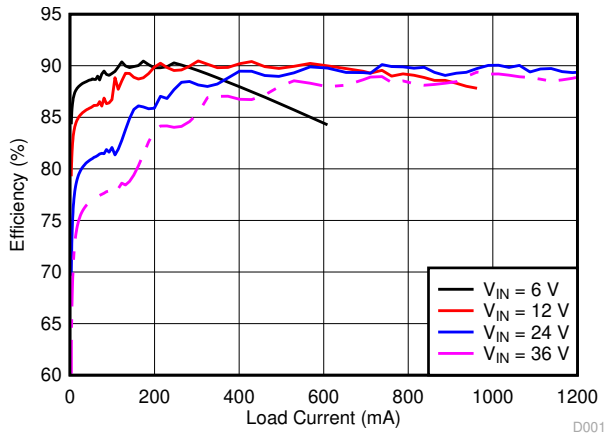
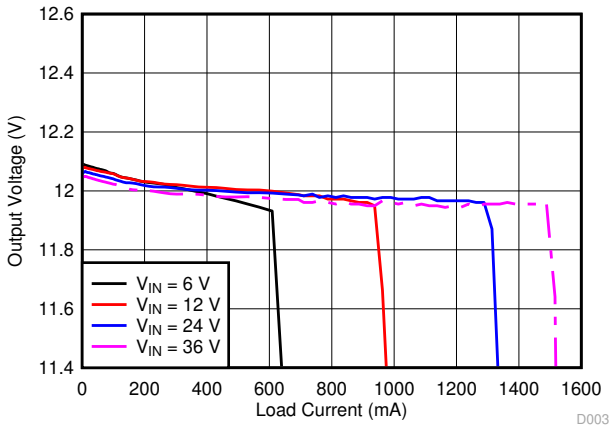
6.6 Typical Characteristics

V_{IN} = 24 V, $V_{EN/UVLO}$ = 2 V (unless otherwise stated).



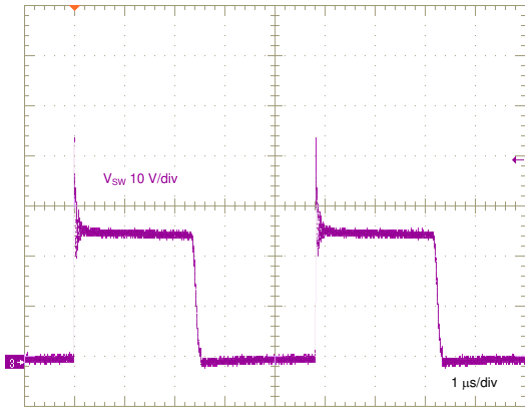
See 图 8-1

图 6-1. Efficiency versus Load



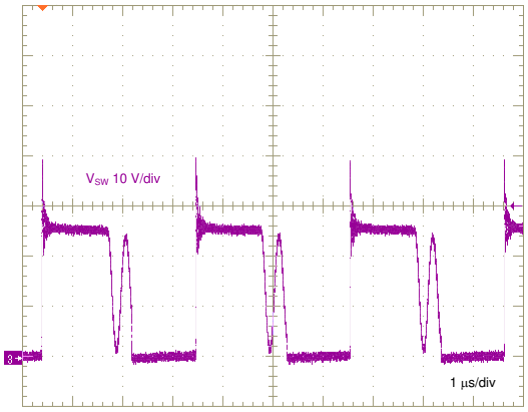
See 图 8-1

图 6-2. Output Voltage versus Load



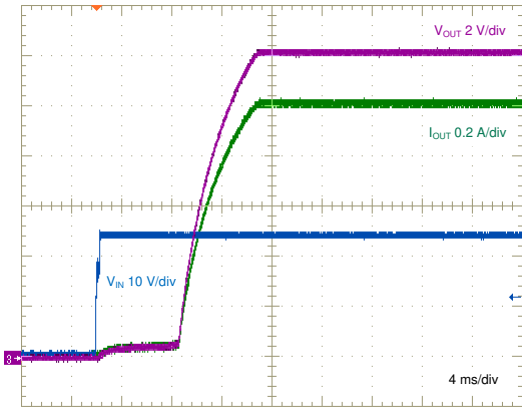
See 图 8-1 V_{IN} = 13.5 V, I_{OUT} = 1 A

图 6-3. Switching Waveform in BCM



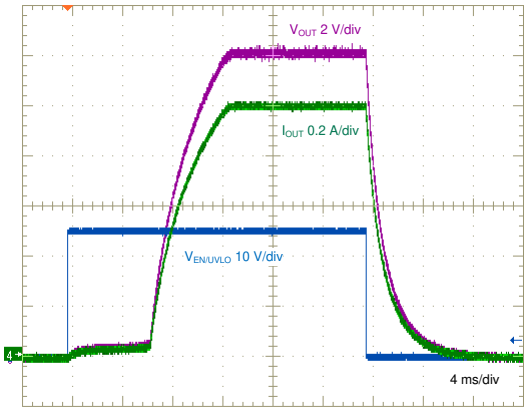
See 图 8-1 V_{IN} = 13.5 V, I_{OUT} = 0.5 A

图 6-4. Switching Waveform in DCM



See 图 8-1

图 6-5. Start-up Characteristic



See 图 8-1

图 6-6. ENABLE ON/OFF Characteristic

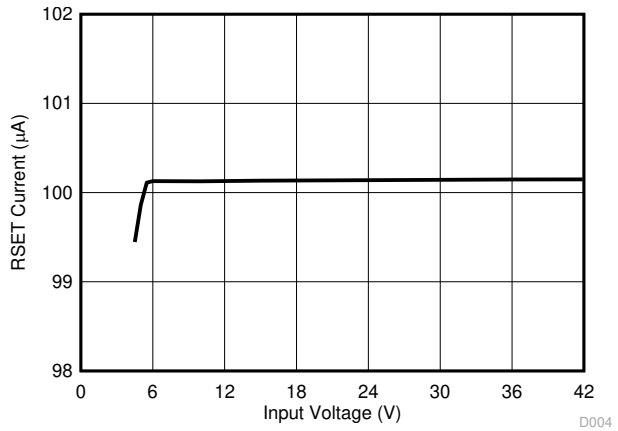


图 6-7. RSET Current versus Input Voltage

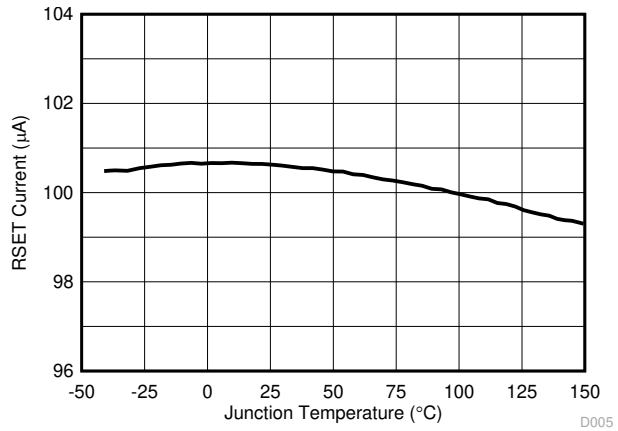


图 6-8. RSET Current versus Temperature

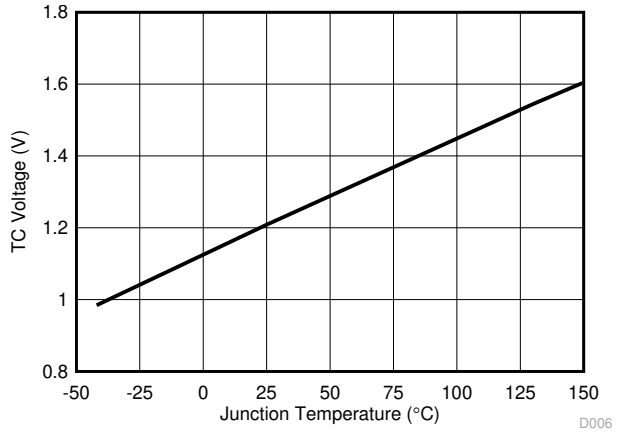


图 6-9. TC Voltage versus Temperature

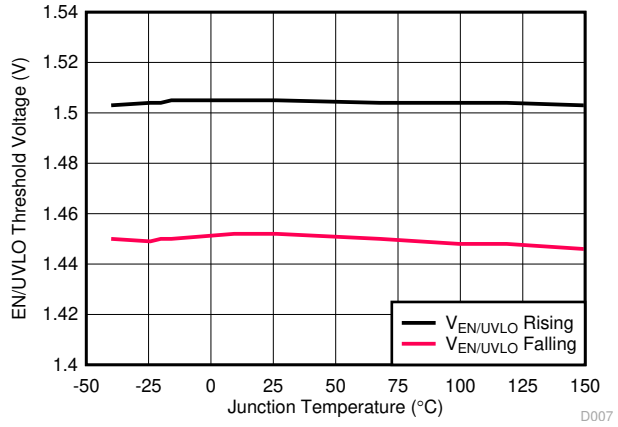


图 6-10. EN/UVLO Threshold Voltages versus Temperature

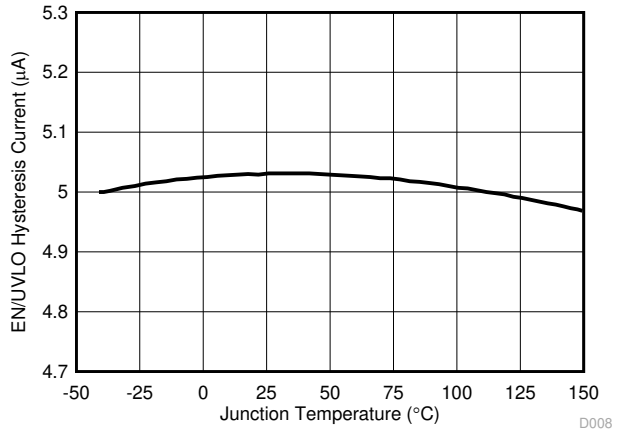


图 6-11. EN/UVLO Hysteresis Current versus Temperature

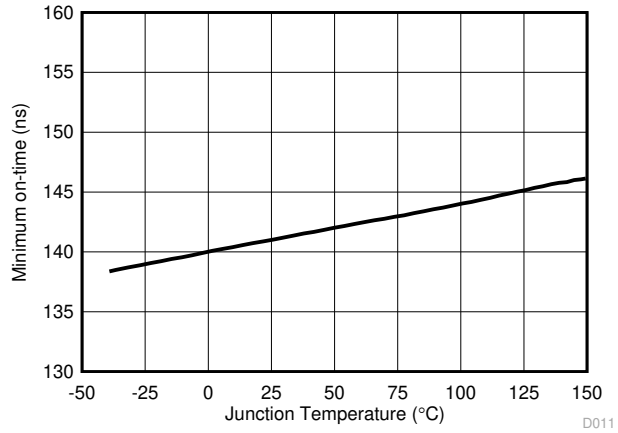


图 6-12. Minimum Switch On-Time versus Temperature

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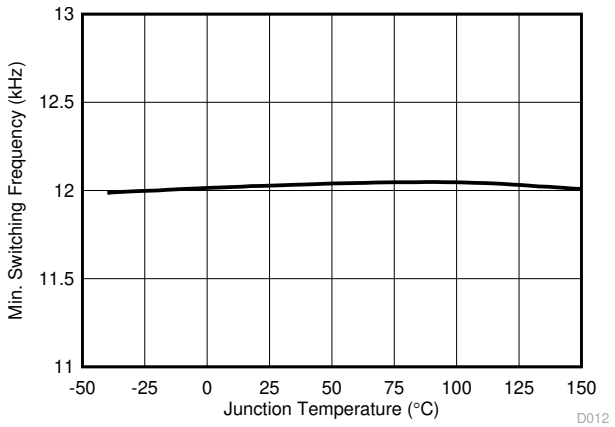


图 6-13. Minimum Switching Frequency versus Temperature

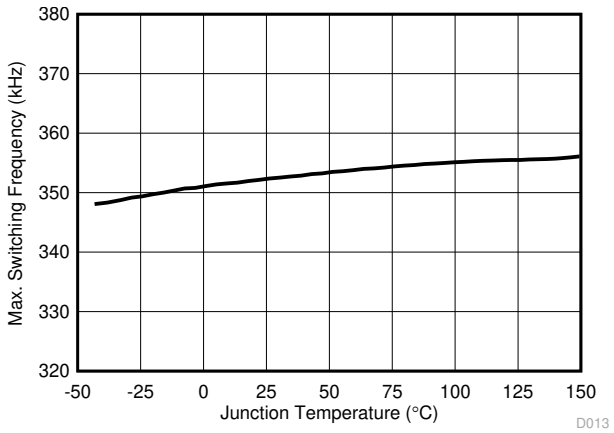


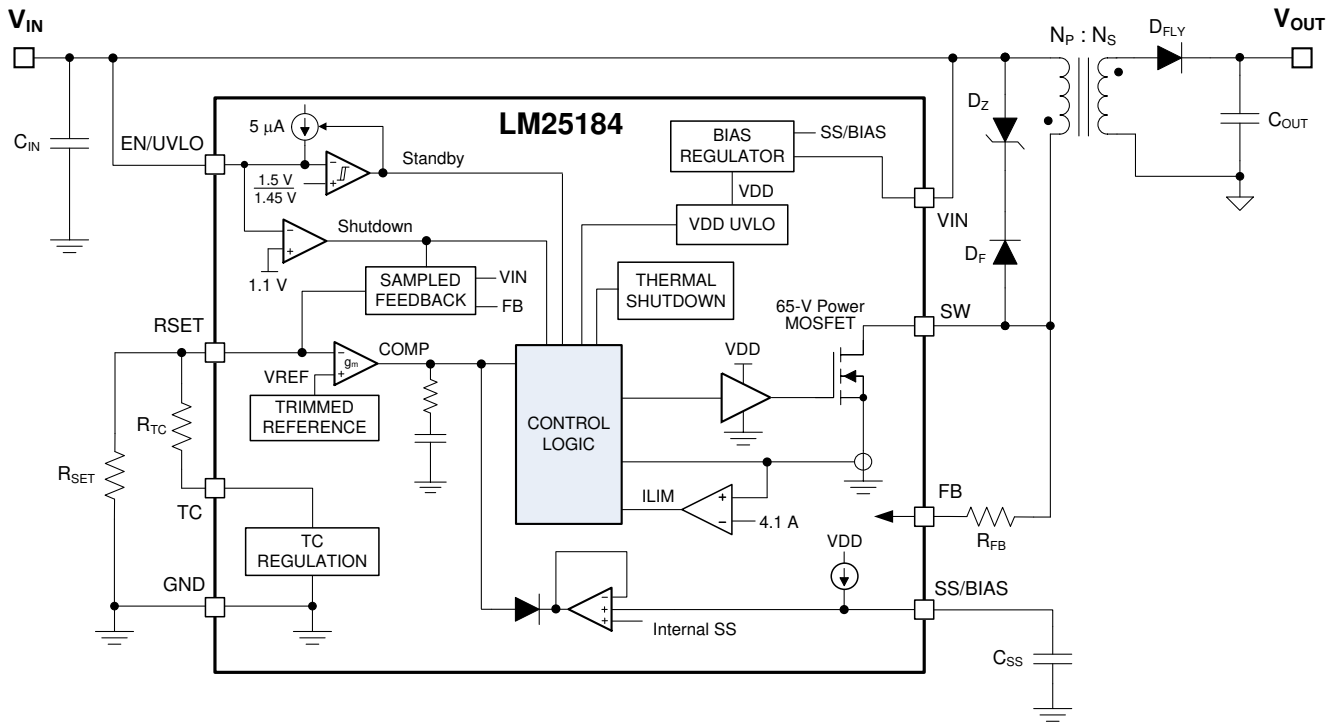
图 6-14. Maximum Switching Frequency versus Temperature

7 Detailed Description

7.1 Overview

The LM25184 primary-side regulated (PSR) flyback converter is a high-density, cost-effective solution for industrial systems requiring less than 10 W of isolated DC/DC power. This compact, easy-to-use flyback converter with low I_Q can be applied over a wide input voltage range from 4.5 V to 42 V, with operation down to 3.5 V after start-up. Innovative frequency and current amplitude modulation enables high conversion efficiency across the entire load and line range. Primary-side regulation of the isolated output voltage using sampled values of the primary winding voltage eliminates the need for an opto-coupler or an auxiliary transformer winding for feedback. Regulation performance that rivals that of traditional opto-coupler solutions is achieved without the associated cost, solution size, and reliability concerns. The LM25184 converter services a wide range of applications including IGBT-based motor drives, factory automation, and medical equipment.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integrated Power MOSFET

The LM25184 is a flyback dc/dc converter with integrated 65-V, 2.5-A N-channel power MOSFET. During the MOSFET on-time, the transformer primary current increases from zero with a slope of V_{IN} / L_{MAG} (where L_{MAG} is the transformer primary-referred magnetizing inductance) while the output capacitor supplies the load current. When the high-side MOSFET is turned off by the control logic, the switch (SW) voltage V_{SW} swings up to approximately V_{IN} + (N_{PS} × V_{OUT}), where N_{PS} = N_P/N_S is the primary-to-secondary turns ratio of the transformer. The magnetizing current flows in the secondary side through the flyback diode, charging the output capacitor and supplying current to the load. Duty cycle D is defined as t_{ON} / t_{SW}, where t_{ON} is the MOSFET conduction time and t_{SW} is the switching period.

图 7-1 shows a typical schematic of the LM25184 PSR flyback circuit. Components denoted in red are optional depending on the application requirements.

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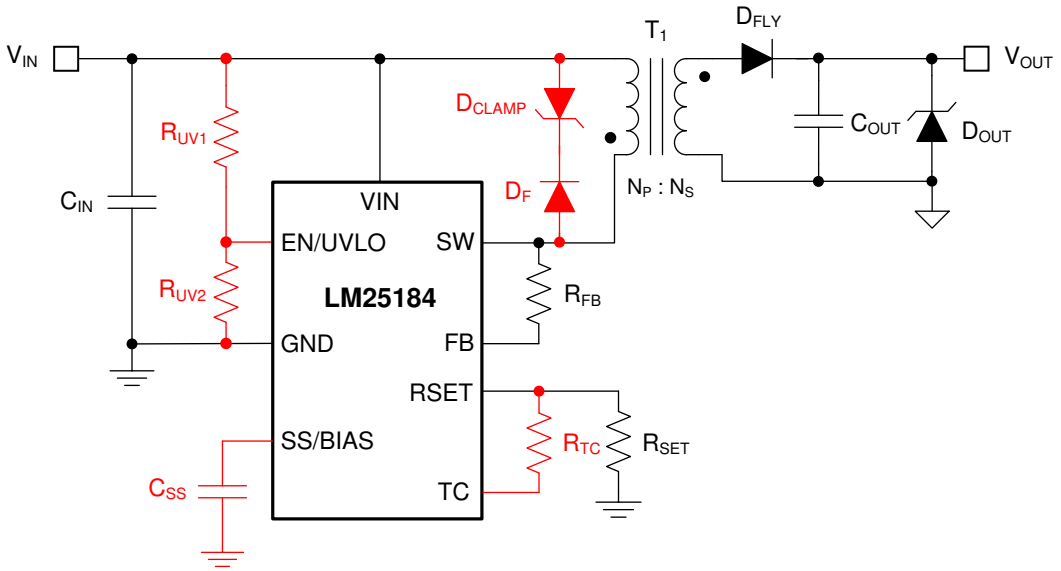

图 7-1. LM25184 Flyback Converter Schematic (Optional Components in Red)

7.3.2 PSR Flyback Modes of Operation

The LM25184 uses a variable-frequency, peak current-mode (VFPCM) control architecture with three possible modes of operation as illustrated in 图 7-2.

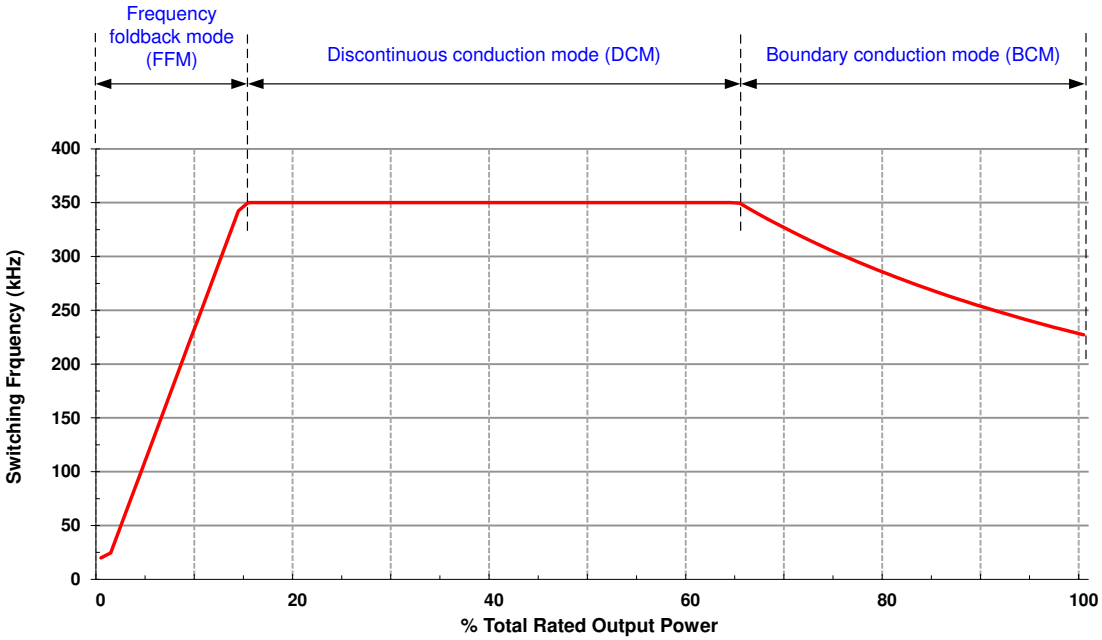

图 7-2. Three Modes of Operation Illustrated by Variation of Switching Frequency With Load

The LM25184 operates in boundary conduction mode (BCM) at heavy loads. The power MOSFET turns on when the current in the secondary winding reaches zero, and the MOSFET turns off when the peak primary current reaches the level dictated by the output of the internal error amplifier. As the load is decreased, the frequency increases to maintain BCM operation. 方程式 1 gives the duty cycle of the flyback converter in BCM.

$$D = \frac{(V_{OUT} + V_D) \cdot N_{PS}}{V_{IN} + (V_{OUT} + V_D) \cdot N_{PS}} \tag{1}$$

where

- V_D is the forward voltage drop of the flyback diode as its current approaches zero

方程式 2 gives the output power in BCM, where the applicable switching frequency and peak primary current are specified by 方程式 3 and 方程式 4, respectively.

$$P_{OUT(BCM)} = \frac{L_{MAG} \cdot I_{PRI\text{-}PK(BCM)}^2}{2} \cdot F_{SW(BCM)} \tag{2}$$

$$F_{SW(BCM)} = \frac{1}{I_{PRI\text{-}PK(BCM)} \cdot \left(\frac{L_{MAG}}{V_{IN}} + \frac{L_{MAG}}{N_{PS} \cdot (V_{OUT} + V_D)} \right)} \tag{3}$$

$$I_{PRI\text{-}PK(BCM)} = \frac{2 \cdot (V_{OUT} + V_D) \cdot I_{OUT}}{V_{IN} \cdot D} \tag{4}$$

As the load decreases, the LM25184 clamps the maximum switching frequency to 350 kHz, and the converter enters discontinuous conduction mode (DCM). The power delivered to the output in DCM is proportional to the peak primary current squared as given by 方程式 5 and 方程式 6. Thus, as the load decreases, the peak current reduces to maintain regulation at 350-kHz switching frequency.

$$P_{OUT(DCM)} = \frac{L_{MAG} \cdot I_{PRI\text{-}PK(DCM)}^2}{2} \cdot F_{SW(DCM)} \tag{5}$$

$$I_{PRI\text{-}PK(DCM)} = \sqrt{\frac{2 \cdot I_{OUT} \cdot (V_{OUT} + V_D)}{L_{MAG} \cdot F_{SW(DCM)}}} \tag{6}$$

$$D_{DCM} = \frac{L_{MAG} \cdot I_{PRI\text{-}PK(DCM)} \cdot F_{SW(DCM)}}{V_{IN}} \tag{7}$$

At even lighter loads, the primary-side peak current set by the internal error amplifier decreases to a minimum level of 0.5 A, or 20% of its 2.5-A peak value, and the MOSFET off-time extends to maintain the output load requirement. The system operates in frequency foldback mode (FFM), and the switching frequency decreases as the load current is reduced. Other than a fault condition, the lowest frequency of operation of the LM25184 is 12 kHz, which sets a minimum load requirement of approximately 0.5% full load.

7.3.3 Setting the Output Voltage

To minimize output voltage regulation error, the LM25184 senses the reflected secondary voltage when the secondary current reaches zero. The feedback (FB) resistor, which is connected between SW and FB is determined using 方程式 8, where R_{SET} is nominally 12.1 kΩ.

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$$R_{FB} = \left(V_{OUT} + V_D\right) \cdot N_{PS} \cdot \frac{R_{SET}}{V_{REF}} \tag{8}$$

7.3.3.1 Diode Thermal Compensation

The LM25184 employs a unique thermal compensation circuit that adjusts the feedback setpoint based on the thermal coefficient of the forward voltage drop of the flyback diode. Even though the output voltage is measured when the secondary current is effectively zero, there is still a non-zero forward voltage drop associated with the flyback diode. Select the thermal compensation resistor using 方程式 9.

$$R_{TC}\left[k\Omega\right] = \frac{R_{FB}\left[k\Omega\right]}{N_{PS}} \cdot \frac{3}{TC_{Diode}\left[mV/°C\right]} \tag{9}$$

The temperature coefficient of the diode voltage drop may not be explicitly provided in the diode data sheet, so the effective value can be estimated based on the measured output voltage shift over temperature when the TC resistor is not installed.

7.3.4 Control Loop Error Amplifier

The inputs of the error amplifier include a level-shifted version of the FB voltage and an internal 1.21-V reference set by the resistor at RSET. A type-2 internal compensation network stabilizes the converter. In BCM operation when the output voltage is in regulation, an on-time interval is initiated when the secondary current reaches zero. The power MOSFET is subsequently turned off when an amplified version of the peak primary current exceeds the error amplifier output.

7.3.5 Precision Enable

The precision EN/UVLO input supports adjustable input undervoltage lockout (UVLO) with hysteresis for application specific power-up and power-down requirements. EN/UVLO connects to a comparator with a 1.5-V reference voltage and 50-mV hysteresis. An external logic signal can be used to drive the EN/UVLO input to toggle the output on and off for system sequencing or protection. The simplest way to enable the LM25184 is to connect EN/UVLO directly to V_{IN}. This allows the LM25184 to start up when V_{IN} is within its valid operating range. However, many applications benefit from using resistor divider R_{UV1} and R_{UV2} as shown in 图 7-3 to establish a precision UVLO level.

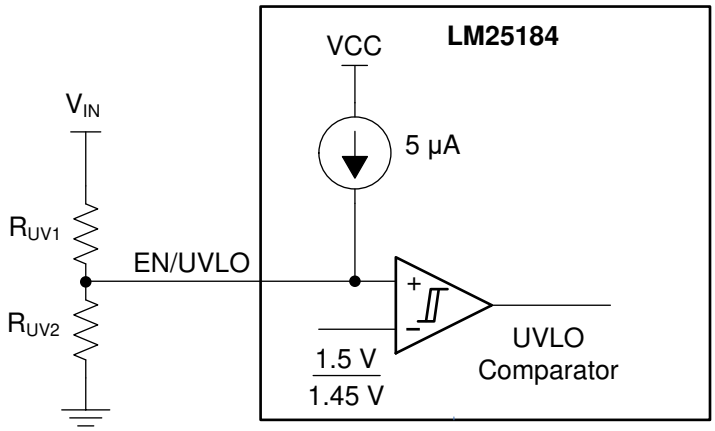

图 7-3. Programmable Input Voltage UVLO With Hysteresis

Use 方程式 10 and 方程式 11 to calculate the input UVLO voltages turnon and turnoff voltages, respectively.

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$$V_{IN(on)} = V_{UV\text{-}RISING}\left(1+\frac{R_{UV1}}{R_{UV2}}\right) \tag{10}$$

$$V_{IN(off)} = V_{UV\text{-}FALLING}\left(1+\frac{R_{UV1}}{R_{UV2}}\right) - I_{UV\text{-}HYST}\cdot R_{UV1} \tag{11}$$

where

- $V_{UV\text{-}RISING}$ and $V_{UV\text{-}FALLING}$ are the UVLO comparator thresholds
- $I_{UV\text{-}HYST}$ is the hysteresis current

The LM25184 also provides a low-I_Q shutdown mode when the EN/UVLO voltage is pulled below a base-emitter voltage drop (approximately 0.6 V at room temperature). If the EN/UVLO voltage is below this hard shutdown threshold, the internal LDO regulator powers off, and the internal bias-supply rail collapses, shutting down the bias currents of the LM25184. The LM25184 operates in standby mode when the EN/UVLO voltage is between the hard shutdown and precision-enable thresholds.

7.3.6 Configurable Soft Start

The LM25184 has a flexible and easy-to-use soft-start control pin, SS/BIAS. The soft-start feature prevents inrush current impacting the LM25184 and the input supply when power is first applied. This is achieved by controlling the voltage at the output of the internal error amplifier. Soft start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. Selectable and adjustable start-up timing options include a 6-ms internally-fixed soft start and an externally-programmable soft start.

The simplest way to use the LM25184 is to leave SS/BIAS open. The LM25184 employs an internal soft-start control ramp and starts up to the regulated output voltage in 6 ms.

However, in applications with a large amount of output capacitance, higher V_{OUT}, or other special requirements, the soft-start time can be extended by connecting an external capacitor C_{SS} from SS/BIAS to GND. A longer soft-start time further reduces the supply current needed to charge the output capacitors while sourcing the required load current. When the EN/UVLO voltage exceeds the UVLO rising threshold and a delay of 20 µs expires, an internal current source I_{SS} of 5 µA charges C_{SS} and generates a ramp to control the primary current amplitude. Calculate the soft-start capacitance for a desired soft-start time, t_{SS}, using 方程式 12.

$$C_{SS}\left[nF\right] = 5\cdot t_{SS}\left[ms\right] \tag{12}$$

C_{SS} is discharged by an internal FET when switching is disabled by EN/UVLO or thermal shutdown.

7.3.7 External Bias Supply

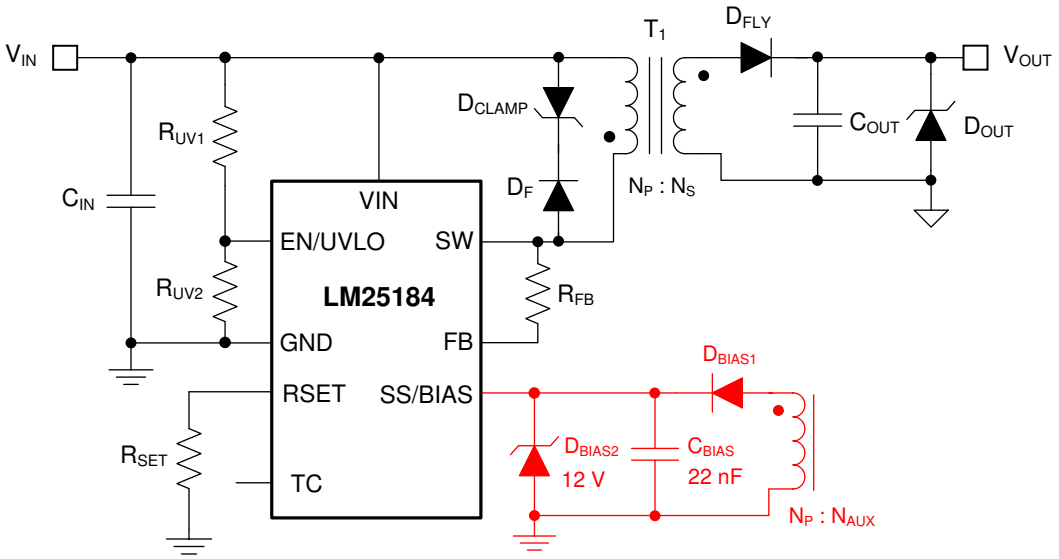

图 7-4. External Bias Supply Using Transformer Auxiliary Winding

The LM25184 has an external bias supply feature that reduces input quiescent current and increases efficiency. When the voltage at SS/BIAS exceeds a rising threshold of 4.25 V, bias power for the internal LDO regulator can be derived from an external voltage source or from a transformer auxiliary winding as shown in 图 7-4. With a bias supply connected, the LM25184 then uses its internal soft-start ramp to control the primary current during start-up.

When using a transformer auxiliary winding for bias power, the total leakage current related to diodes D_{BIAS1} and D_{BIAS2} in 图 7-4 must be less than 1 µA across the full operating temperature range.

7.3.8 Minimum On-Time and Off-Time

When the internal power MOSFET is turned off, the leakage inductance of the transformer resonates with the SW node parasitic capacitance. The resultant ringing behavior can be excessive with large transformer leakage inductance and can corrupt the secondary zero-current detection. To prevent such a situation, a minimum switch off-time, designated as $t_{OFF\text{-}MIN}$, of a maximum of 425 ns is set internally to ensure proper functionality. This sets a lower limit for the transformer magnetizing inductance as discussed in *节 8.2.1.2*.

Furthermore, noise effects as a result of power MOSFET turnon can impact the internal current sense circuit measurement. To mitigate this effect, the LM25184 provides a blanking time after the MOSFET turns on. This blanking time forces a minimum on-time, $t_{ON\text{-}MIN}$, of 140 ns.

7.3.9 Overcurrent Protection

In case of an overcurrent condition on the isolated output or outputs, the output voltage drops lower than the regulation level since the maximum power delivered is limited by the peak current capability on the primary side. The peak primary current is maintained at 2.5 A (plus an amount related to the 100-ns propagation delay of the current limit comparator) until the output decreases to the secondary diode voltage drop to impact the reflected signal on the primary side. At this point, the LM25184 assumes the output cannot be recovered and re-calibrates its switching frequency to 9 kHz until the overload condition is removed. The LM25184 responds with similar behavior to an output short circuit condition.

For a given input voltage, 方程式 13 gives the maximum output current prior to the engagement of overcurrent protection. The typical threshold value for $I_{SW\text{-}PEAK}$ from *节 6.5* is 4.1 A.

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$$I_{OUT(max)} = \frac{\eta}{2} \cdot \frac{I_{SW\text{-}PEAK}}{\left(\frac{V_{OUT}}{V_{IN}} + \frac{1}{N_{PS}}\right)} \tag{13}$$

7.3.10 Thermal Shutdown

Thermal shutdown is an integrated self-protection to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 175°C to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the LM25184 restarts when the junction temperature falls to 165°C.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

EN/UVLO facilitates ON and OFF control for the LM25184. When $V_{EN/UVLO}$ is below approximately 0.6 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 3 μA at V_{IN} = 24 V. The LM25184 also employs internal bias rail undervoltage protection. If the internal bias supply voltage is below its UV threshold, the converter remains off.

7.4.2 Standby Mode

The internal bias rail LDO regulator has a lower enable threshold than the converter itself. When $V_{EN/UVLO}$ is above 0.6 V and below the precision-enable threshold (1.5 V typically), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal VCC is above its UV threshold. The switching action and voltage regulation are not enabled until $V_{EN/UVLO}$ rises above the precision enable threshold.

7.4.3 Active Mode

The LM25184 is in active mode when $V_{EN/UVLO}$ is above the precision-enable threshold and the internal bias rail is above its UV threshold. The LM25184 operates in one of three modes depending on the load current requirement:

1. Boundary conduction mode (BCM) at heavy loads
2. Discontinuous conduction mode (DCM) at medium loads
3. Frequency foldback mode (FFM) at light loads

Refer to 节 *7.3.2* for more detail.

8 Application and Implementation

备注

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The LM25184 requires only a few external components to convert from a wide range of supply voltages to one or more isolated output rails. To expedite and streamline the process of designing of a LM25184-based converter, a comprehensive LM25184 quick-start calculator is available for download to assist the designer with component selection for a given application. WEBENCH® online software is also available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following sections discuss the design procedure for both single- and dual-output implementations using specific circuit design examples.

As mentioned previously, the LM25184 also integrates several optional features to meet system design requirements, including precision enable, input UVLO, programmable soft start, output voltage thermal compensation, and external bias supply connection. Each application incorporates these features as needed for a more comprehensive design.

The application circuits detailed in *节 8.2* show LM25184 configuration options suitable for several application use cases. Refer to the *LM25184EVM-S12 EVM* user's guide for more detail.

8.2 Typical Applications

For step-by-step design procedures, circuit schematics, bill of materials, PCB files, simulation and test results of LM25184-powered implementations, refer to the *TI Reference Design* library.

8.2.1 Design 1: Wide V_{IN}, Low I_Q PSR Flyback Converter Rated at 12 V, 1 A

The schematic diagram of a 12-V, 1-A PSR flyback converter is given in 图 8-1.

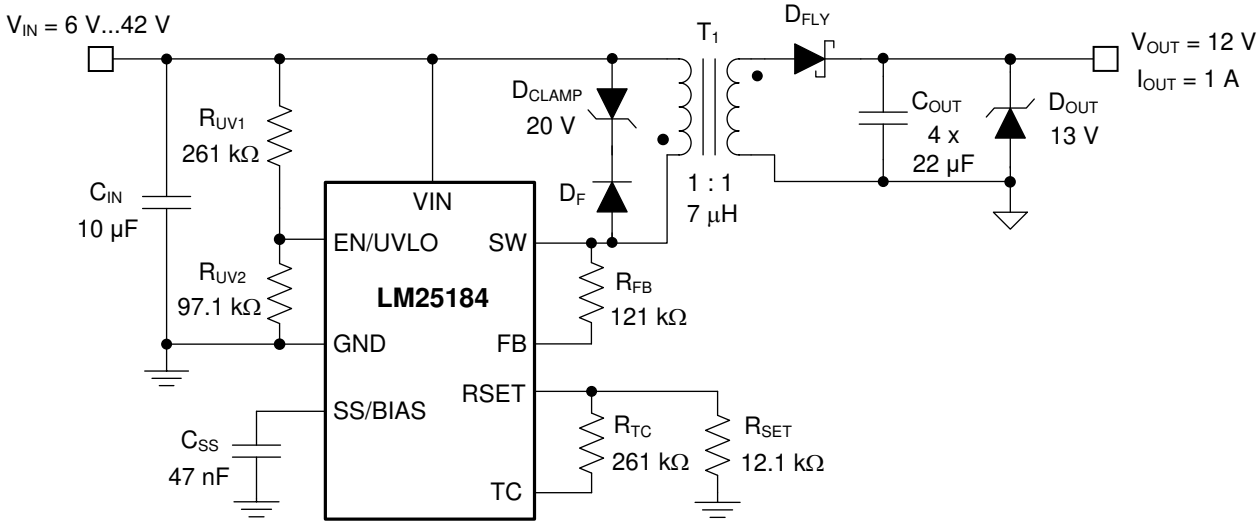

图 8-1. Schematic for Design 1 With $V_{IN(nom)}$ = 24 V, V_{OUT} = 12 V, I_{OUT} = 1 A

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8.2.1.1 Design Requirements

The required input, output, and performance parameters for this application example are shown in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range	6 V to 36 V
Input UVLO thresholds	5.5 V on, 4 V off
Output voltage	12 V
Rated load current, V_{IN} ≥ 13.5 V	1 A
Output voltage regulation	±1.5%
Output voltage ripple	< 120 mV pk-pk

The target full-load efficiency is 89% based on a nominal input voltage of 24 V and an isolated output voltage of 12 V. The LM25184 is chosen to deliver a fixed 12-V output voltage set by resistor R_{FB} connected between the SW and FB pins. The input voltage turnon and turnoff thresholds are established by R_{UV1} and R_{UV2}. The required components are listed in 表 8-2. Transformers for other single-output designs are listed in 表 8-3.

表 8-2. List of Components for Design 1

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	10 µF, 50 V, X7R, 1210, ceramic	TDK	CNA6P1X7R1H106K250AE
C_{OUT1}	4	22 µF, 25 V, X7R, 1210, ceramic	TDK	CNA6P1X7R1H106K250AE
			Taiyo Yuden	TMK325B7226MM-PR
C_{OUT2}	0	100 µF, 16 V, ±20%, electrolytic	Kemet	T598D107M016ATE050
C_{SS}	1	47 nF, 16 V, X7R, 0402	Std	Std
D_{CLAMP}	1	Zener, 20 V, 3 W, SMA	3SMAJ5932B	Micro Commercial
D_F, D_{FLY}	2	Schottky diode, 60 V, 3 A, SOD-123FL	FSV360FP	OnSemi
D_{OUT}	1	Zener, 13 V, 2%, SOD-523	BZX585-B13	Nexperia
R_{FB}	1	121 kΩ, 1%, 0402	Std	Std
R_{SET}	1	12.1 kΩ, 1%, 0402	Std	Std
R_{TC}	1	261 kΩ, 1%, 0402	Std	Std
R_{UV1}	1	261 kΩ, 1%, 0603	Std	Std
R_{UV2}	1	97.6 kΩ, 1%, 0402	Std	Std
T_1	1	7 µH, 5 A, 1 : 1, 13 mm × 11 mm × 10 mm	Coilcraft	ZA9672-BE
			Sumida	12387-T162
		7 µH, 5 A, 1 : 1, 9.8 mm × 9.5 mm ×10.6 mm	Würth Electronik	750318701
U_1	1	LM25184 PSR flyback converter, VSON-8	Texas Instruments	LM25184NGUR

表 8-3. Magnetic Components for Single-Output Designs

OUTPUT VOLTAGE RANGE	TURNS RATIO	L_{MAG}, I_{SAT}	DIMENSIONS	VENDOR	PART NUMBER
3.3 V to 5 V	3 : 1	9 µH, 5 A	13 × 11 × 10 mm	Coilcraft	ZA9671-BE
5 V to 12 V	1 : 1	7 µH, 5 A			ZA9672-BE
12 V to 24 V	1 : 2	7 µH, 5 A			ZA9673-BE
24 V to 48 V	1 : 3	9 µH, 5 A			ZA9674-BE
3.3 V to 6 V	2 : 1	7 µH, 5 A	12 × 10 × 6 mm		ZB1067-AE

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25184 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Custom Design With Excel Quickstart Tool

Use the LM25184 quick-start calculator to select components based on the converter specifications.

8.2.1.2.3 Flyback Transformer – T_1

Choose a turns ratio of 1 : 1 based on an approximate 70% max duty cycle at minimum input voltage using 方程式 14, rounding up or down as needed. While the maximum duty cycle can approach 80% if a particularly wide input voltage application is needed, it increases the peak current stress of the secondary-side components.

$$N_{PS} = \frac{D_{MAX}}{1 - D_{MAX}} \cdot \frac{V_{IN(min)}}{V_{OUT} + V_D} = \frac{0.7}{1 - 0.7} \cdot \frac{5\,V}{12\,V + 0.3\,V} = 0.95 \tag{14}$$

Select a magnetizing inductance based on the minimum off-time constraint using 方程式 15. Choose a value of 7 µH to allow some margin for this application. Specify a saturation current of 5 A, above the maximum switch current specification of the LM25184.

$$L_{MAG} \geq \frac{(V_{OUT} + V_D) \cdot N_{PS} \cdot t_{OFF\text{-}MIN}}{I_{SW\text{-}PEAK(FFM)}} = \frac{(12\,V + 0.3\,V) \cdot 1 \cdot 425\,ns}{0.82\,A} = 6.4\,\mu H \tag{15}$$

Note that a higher magnetizing inductance provides a larger operating range for BCM and FFM, but the leakage inductance can increase based on a higher number of primary turns, N_P. 方程式 16 and 方程式 17 give the primary and secondary winding RMS currents, respectively.

$$I_{PRI\text{-}RMS} = \sqrt{\frac{D}{3}} \cdot I_{PRI\text{-}PK} \tag{16}$$

$$I_{SEC\text{-}RMS} = \sqrt{\frac{2 \cdot I_{OUT} \cdot I_{PRI\text{-}PK} \cdot N_{PS}}{3}} \tag{17}$$

Find the maximum output current for a given turns ratio using 方程式 18, where η is the efficiency and the typical value for $I_{SW\text{-}PEAK}$ is the 4.1-A switch peak current threshold. Iterate by increasing the turns ratio if the output current capability is too low at minimum input voltage, checking that the SW voltage rating of 65 V is not exceeded at maximum input voltage.

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$$I_{OUT(max)} = \frac{\eta}{2} \cdot \frac{I_{SW\text{-}PEAK}}{\left(\frac{V_{OUT}}{V_{IN}} + \frac{1}{N_{PS}}\right)} = \frac{0.92}{2} \cdot \frac{4.1\,A}{\left(\frac{12\,V}{V_{IN}} + \frac{1}{1}\right)} = \begin{cases} 0.95\,A \text{ at } V_{IN} = 12\,V \\ 1.25\,A \text{ at } V_{IN} = 24\,V \end{cases} \tag{18}$$

8.2.1.2.4 Flyback Diode – D_{FLY}

The flyback diode reverse voltage is given by 方程式 19.

$$V_{D\text{-}REV} \geq \frac{V_{IN(max)}}{N_{PS}} + V_{OUT} = \frac{42\,V}{1} + 12\,V = 54\,V \tag{19}$$

Select a 60-V, 3-A Schottky diode for this application to account for inevitable diode voltage overshoot and ringing related to the resonance of transformer leakage inductance and diode parasitic capacitance. Connect an appropriate RC snubber circuit (for example, 100 Ω and 22 pF) across the flyback diode if needed, particularly if the transformer leakage inductance is high. Also, choose a flyback diode with current rating that aligns with the maximum peak secondary winding current of $N_{PS} \times I_{SW\text{-}PEAK}$.

8.2.1.2.5 Leakgae Inductance Clamp Circuit – D_F, D_{CLAMP}

Connect a diode-Zener clamp circuit across the primary winding to limit the peak switch voltage after MOSFET turnoff below the maximum level of 65 V, as given by 方程式 20.

$$V_{DZ(clamp)} < V_{SW(max)} - V_{IN(max)} \tag{20}$$

Choose a 20-V zener diode for D_{CLAMP} to give a clamp voltage of approximately 1.5 times the reflected output voltage, as specified by 方程式 21. This provides a balance between the maximum switch voltage excursion and the leakage inductance demagnetization time. Select a Zener diode with low package parasitic inductance to manage the high slew-rate current during the switch turnoff transition.

$$V_{DZ(clamp)} = 1.5 \cdot N_{PS} \cdot \left(V_{OUT} + V_D\right) = 1.5 \cdot 1 \cdot \left(12\,V + 0.4\,V\right) = 18.6\,V \tag{21}$$

Choose an ultra-fast switching diode or Schottky diode for D_F with reverse voltage rating greater than the maximum input voltage and forward current rating of 3 A or higher.

8.2.1.2.6 Output Capacitor – C_{OUT}

The output capacitor determines the voltage ripple at the converter output, limits the voltage excursion during a load transient, and sets the dominant pole of the small-signal response of the converter. Select an output capacitance using 方程式 22 to limit the ripple voltage amplitude to less than 1% of the output voltage at minimum input voltage and maximum load.

$$C_{OUT} \geq \frac{L_{MAG} \cdot {I_{SW\text{-}PEAK}}^2}{2 \cdot \Delta V_{OUT} \cdot V_{OUT}} \cdot \left(\frac{1+D}{2}\right)^2 = \frac{7\,\mu H \cdot \left(4.1\,A\right)^2}{2 \cdot 120\,mV \cdot 12\,V} \cdot \left(\frac{1+0.7}{2}\right)^2 = 30\,\mu F \tag{22}$$

Mindful of the voltage coefficient of ceramic capacitors, select four 22-µF, 25-V capacitors in 1210 case size with X7S or better dielectric. Assuming operation in BCM, calculate the capacitive ripple voltage at the output using 方程式 23.

$$\Delta V_{OUT} = \frac{L_{MAG} \cdot I_{OUT}^2}{2 \cdot C_{OUT} \cdot V_{OUT} \cdot N_{PS}^2} \cdot \left(\frac{1+D}{1-D}\right)^2 = \frac{L_{MAG} \cdot I_{OUT}^2}{2 \cdot \Delta V_{OUT} \cdot V_{OUT}} \cdot \left[\frac{1}{N_{PS}} + \frac{2 \cdot (V_{OUT} + V_D)}{V_{IN}}\right]^2 \tag{23}$$

方程式 24 gives an expression for the output capacitor RMS ripple current.

$$I_{COUT\text{-}RMS} = I_{OUT} \cdot \sqrt{\frac{2 \cdot N_{PS} \cdot I_{PRI\text{-}PK}}{3 \cdot I_{OUT}} - 1} \tag{24}$$

8.2.1.2.7 Input Capacitor – C_{IN}

Select an input capacitance using 方程式 25 to limit the ripple voltage amplitude to less than 5% of the input voltage when operating at nominal input voltage.

$$C_{IN} \geq \frac{I_{PRI\text{-}PK} \cdot D \cdot \left(1 - \frac{D}{2}\right)^2}{2 \cdot F_{SW} \cdot \Delta V_{IN}} \tag{25}$$

Substituting the input current at full load, switching frequency, peak primary current, and peak-to-peak ripple specification gives C_{IN} greater than 5 µF. Considering the voltage coefficient of ceramic capacitors, select a 10-µF, 50-V, X7R ceramic capacitor in 1210 case size. 方程式 26 gives the input capacitor RMS ripple current.

$$I_{CIN\text{-}RMS} = \frac{D \cdot I_{PRI\text{-}PK}}{2} \cdot \sqrt{\frac{4}{3 \cdot D} - 1} \tag{26}$$

8.2.1.2.8 Feedback Resistor – R_{FB}

Select a feedback resistor, designated R_{FB}, of 121 kΩ based on the secondary winding voltage at the end of the flyback conduction interval (the sum of the 12-V output voltage and the Schottky diode forward voltage drop as its current approaches zero) reflected by the transformer turns ratio of 1 : 1.

$$R_{FB} = \frac{(V_{OUT} + V_D) \cdot N_{PS}}{0.1\,mA} = \frac{(12\,V + 0.2\,V) \cdot 1}{0.1\,mA} = 122\,k\Omega \tag{27}$$

8.2.1.2.9 Thermal Compensation Resistor – R_{TC}

Select a resistor for output voltage thermal compensation, designated R_{TC}, based on 方程式 28.

$$R_{TC}[k\Omega] = \frac{R_{FB}[k\Omega]}{N_{PS}} \cdot \frac{3}{TC_{Diode}[mV/°C]} = \frac{121\,k\Omega \cdot 3}{1 \cdot 1.4} = 261\,k\Omega \tag{28}$$

8.2.1.2.10 UVLO Resistors – R_{UV1}, R_{UV2}

Given $V_{IN(on)}$ and $V_{IN(off)}$ as the input voltage turnon and turnoff thresholds of 5.5 V and 4 V, respectively, select the upper and lower UVLO resistors using the following expressions:

$$R_{UV1} = \frac{V_{IN(on)} \cdot \frac{V_{UV\text{-}FALLING}}{V_{UV\text{-}RISING}} - V_{IN(off)}}{I_{UV\text{-}HYST}} = \frac{5.5\,V \cdot \frac{1.45\,V}{1.5\,V} - 4\,V}{5\,\mu A} = 263\,k\Omega \tag{29}$$

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$$R_{UV2} = R_{UV1} \cdot \frac{V_{UV\text{-}RISING}}{V_{IN(on)} - V_{UV\text{-}RISING}} = 263\,k\Omega \cdot \frac{1.5\ V}{5.5\ V - 1.5\ V} = 98.6\,k\Omega \tag{30}$$

The nearest standard E96 resistor values for R_{UV1} and R_{UV2} are 261 kΩ and 97.6 kΩ, respectively. Calculate the actual input voltage turnon and turnoff thresholds as follows:

$$V_{IN(on)} = V_{UV\text{-}RISING}\left(1 + \frac{R_{UV1}}{R_{UV2}}\right) = 1.5\,V\left(1 + \frac{261\,k\Omega}{97.6\,k\Omega}\right) = 5.51\,V \tag{31}$$

$$V_{IN(off)} = V_{UV\text{-}FALLING}\left(1 + \frac{R_{UV1}}{R_{UV2}}\right) - I_{UV\text{-}HYST} \cdot R_{UV1} = 1.45\,V\left(1 + \frac{261\,k\Omega}{97.6\,k\Omega}\right) - 5\,\mu A \cdot 261\,k\Omega = 4.02\,V \tag{32}$$

8.2.1.2.11 Soft-Start Capacitor – C_{SS}

Connect an external soft-start capacitor for a specific soft-start time. In this example, select a soft-start capacitance of 47 nF based on 方程式 12 to achieve a soft-start time of 9 ms.

For technical solutions, industry trends, and insights for designing and managing power supplies, please refer to TI's *Power Management* technical articles.

8.2.2 Application Curves

Unless otherwise stated, application performance curves were taken at T_A = 25°C.

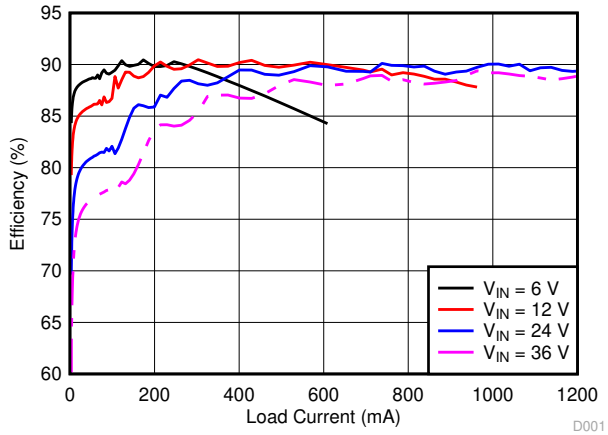


图 8-2. Efficiency (Linear Scale)

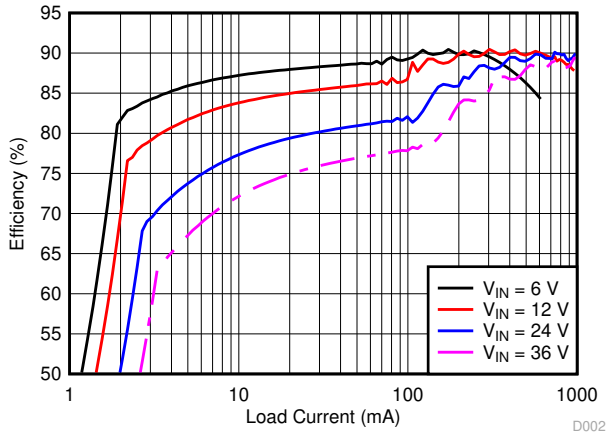


图 8-3. Efficiency (Log Scale)

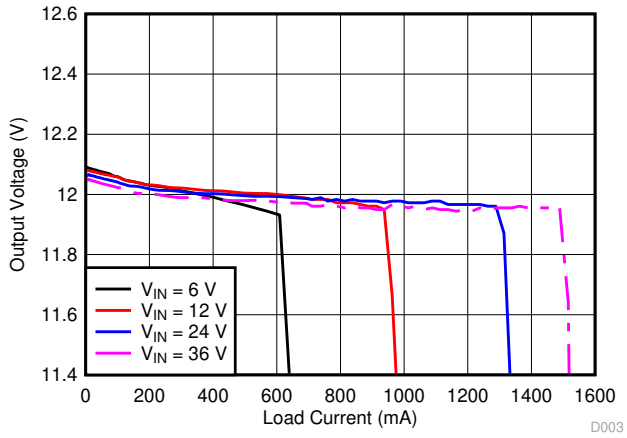


图 8-4. Load Regulation (Linear Scale)

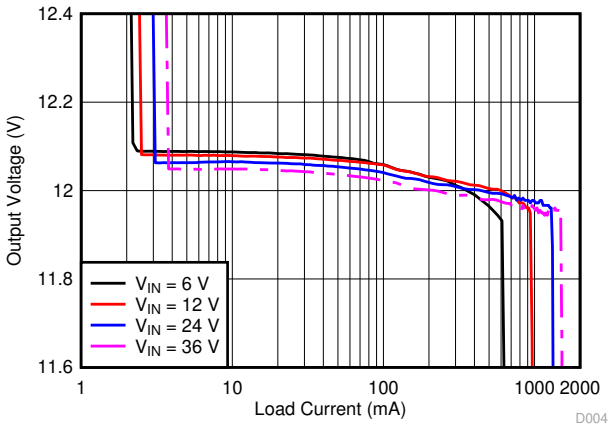
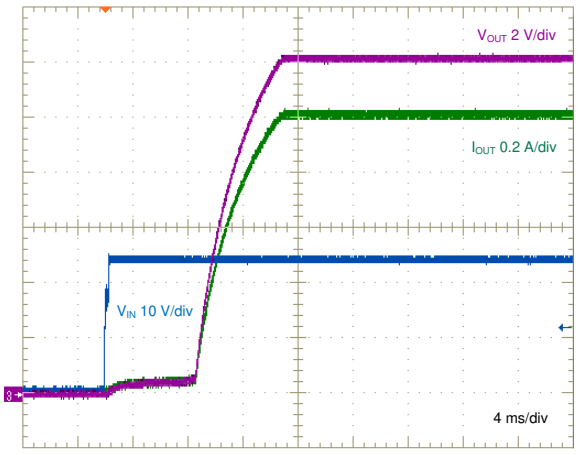
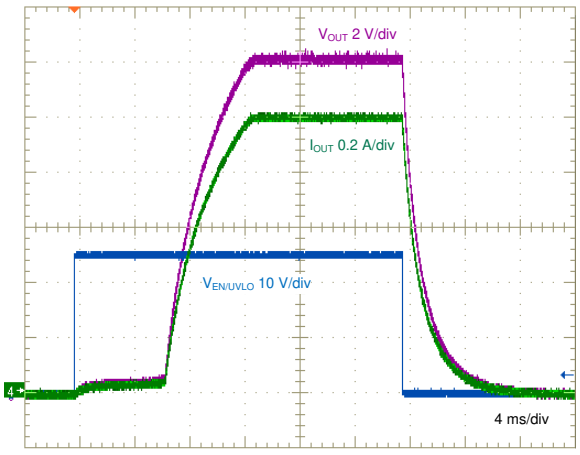


图 8-5. Load Regulation (Log Scale)



VIN stepped to 24 V　　12-Ω Load

图 8-6. Start-up Characteristic



VIN = 24 V　　12-Ω Load

图 8-7. Enable ON and OFF Characteristic

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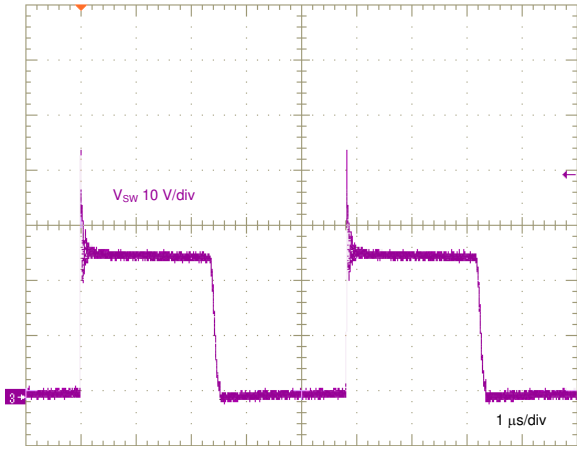
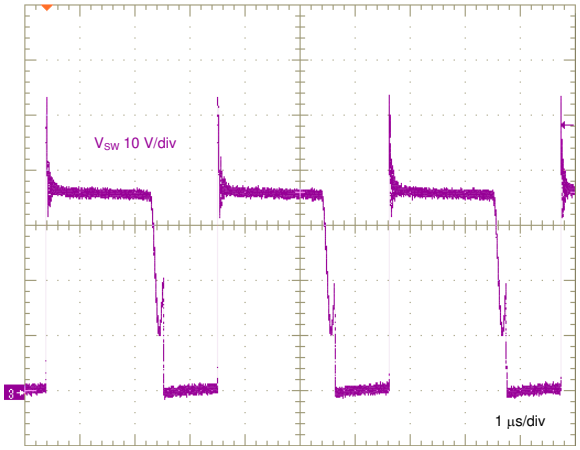


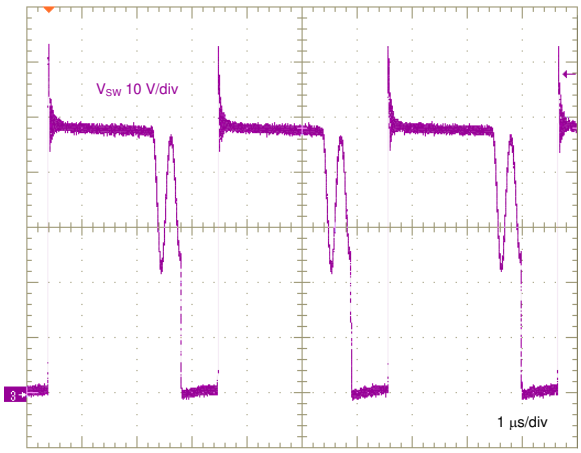
V_{IN} = 13.5 V I_{OUT} = 1 A

图 8-8. Switch Node Voltage



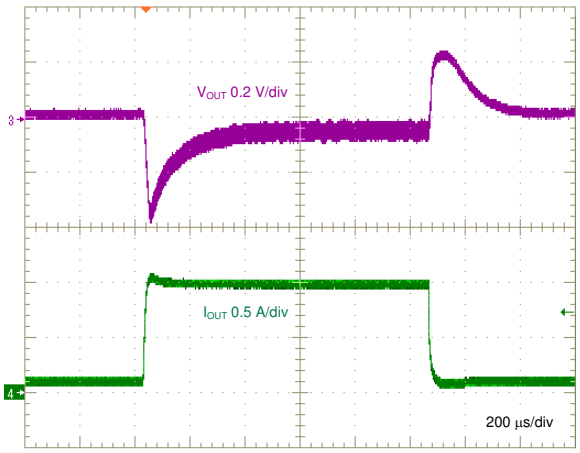
V_{IN} = 24 V I_{OUT} = 1 A

图 8-9. Switch Node Voltage



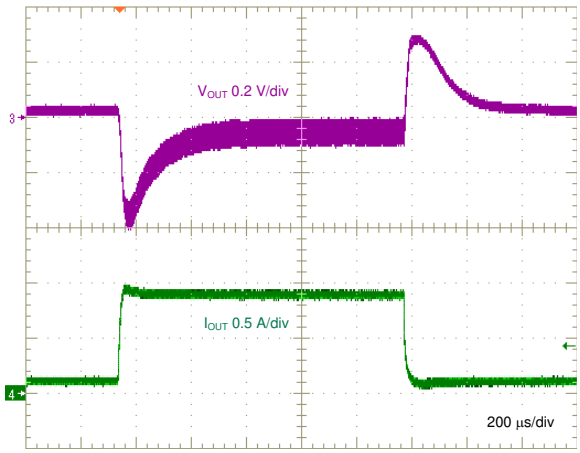
V_{IN} = 36 V I_{OUT} = 1 A

图 8-10. Switch Node Voltage



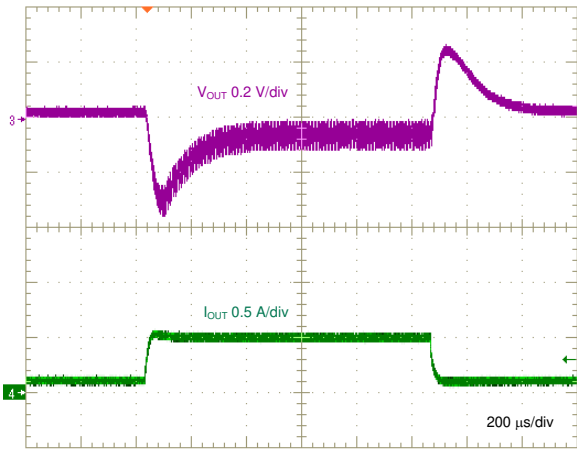
V_{IN} = 24 V

图 8-11. Load Transient, 0.1 A to 1 A, 0.1 A/µs



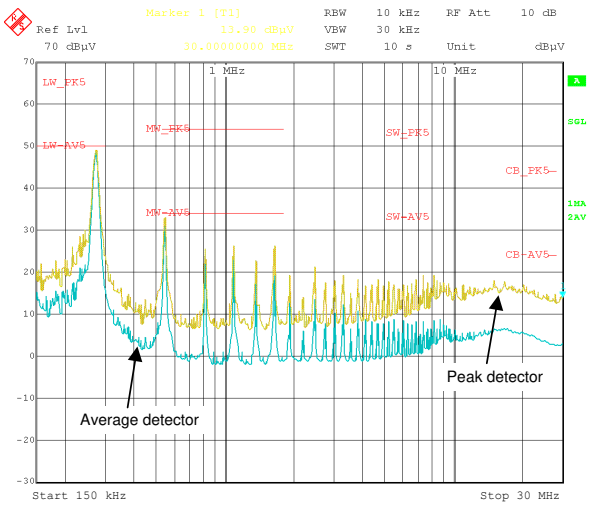
V_{IN} = 13.5 V

图 8-12. Load Transient, 0.1 A to 1 A, 0.1 A/µs



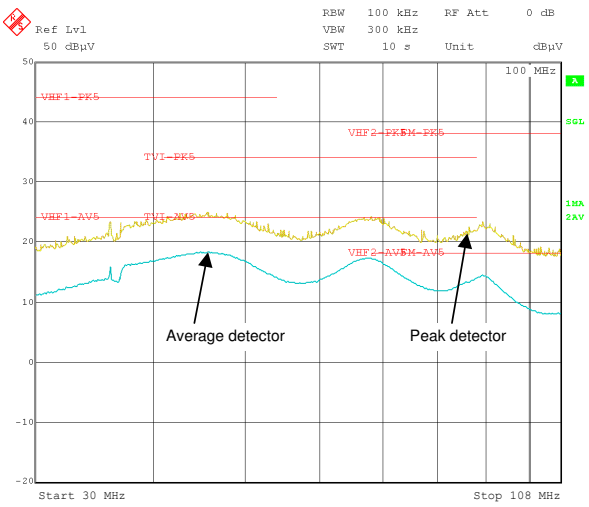
V_{IN} = 6 V

图 8-13. Load Transient, 0.1 A to 0.5 A, 0.1 A/µs



V_{IN} = 24 V　　150 kHz to 30 MHz　　L_{IN} = 4.7 µH
I_{OUT} = 1 A　　C_{IN} = 10 µF

图 8-14. CISPR 25 Class 5 Conducted EMI Plot



V_{IN} = 24 V　　30 MHz to 108 MHz　　L_{IN} = 4.7 µH
I_{OUT} = 1 A　　C_{IN} = 10 µF

图 8-15. CISPR 25 Class 5 Conducted EMI Plot

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8.2.3 Design 2: PSR Flyback Converter With Dual Outputs of 15 V and –8 V at 0.5 A

The schematic diagram of a dual-output flyback converter intended for isolated IGBT and SiC MOSFET gate drive power supply applications is given in 图 8-16.

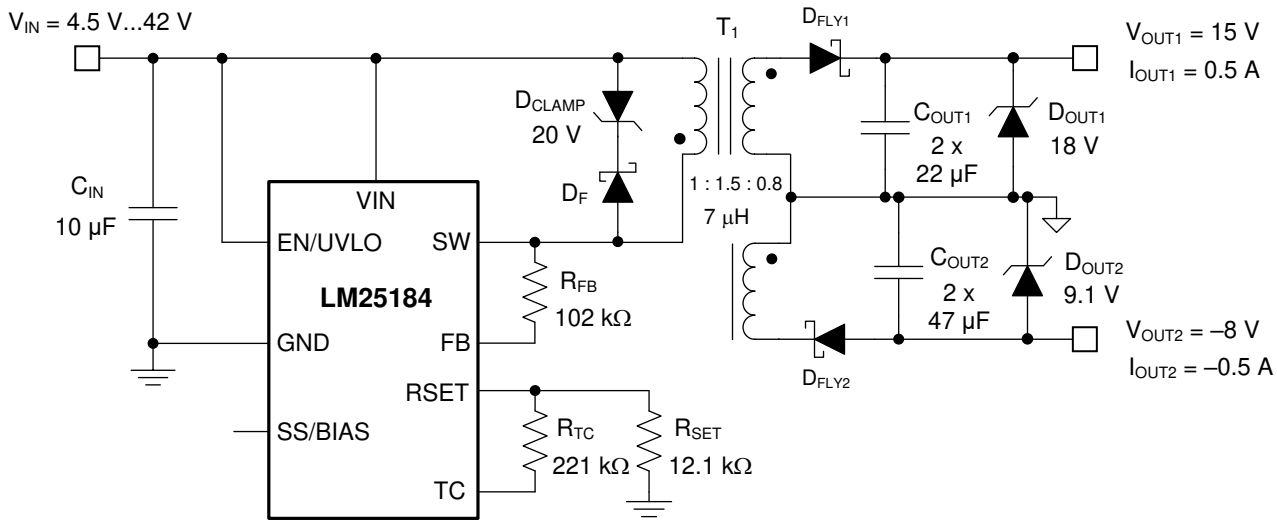

图 8-16. Schematic for Design 2 With $V_{IN(nom)}$ = 24 V, V_{OUT1} = 15 V, V_{OUT2} = –8 V, I_{OUT} = 0.5 A

8.2.3.1 Design Requirements

The required input, output, and performance parameters for this application example are shown in 表 8-4.

表 8-4. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady state)	4.5 V to 42 V
Output 1 voltage and current (at V_{IN} ≥ 24 V)	15 V, 0.5 A
Output 2 voltage and current (at V_{IN} ≥ 24 V)	–8 V, 0.5 A
Input UVLO thresholds	4.5 V on, 4 V off
Output voltage regulation	±2%

The target full-load efficiency of this LM25184 design is 89% based on a nominal input voltage of 24 V and isolated output voltages of 15 V and –8 V sharing a common return. The selected flyback converter components are cited in 表 8-5, including the following:

- A multi-winding flyback transformer
- Input and output capacitors
- Flyback rectifying diodes
- A flyback converter IC

表 8-5. List of Components for Design 2

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	10 µF, 50 V, X7R, 1210, ceramic	TDK	C3225X7R1H106M250AC
			Taiyo Yuden	UMK325AB7106KM-T
C_{OUT1}	2	22 µF, 25 V, X7R, 1210, ceramic	TDK	C3225X7R1E226M250AB
			Taiyo Yuden	TMK325B7226MM-PR
C_{OUT2}	2	47 µF, 16 V, X7S, 1210, Ceramic	Murata	GRM32EC81C476KE15L
			Taiyo Yuden	EMK325AC6476MM-P
		47 µF, 16 V, X7R, 1210, Ceramic	Murata	GRM32ER71A476KE15L
			Taiyo Yuden	LMK325B7476MM-TR
			Kemet	C1210C476K8RAC7800
D_{CLAMP}	1	Zener, 20 V, 3 W, SMA	3SMAJ5932B	Micro Commercial
D_F, D_{FLY2}	1	Schottky diode, 60 V, 3 A, SOD-123FL	FSV360FP	OnSemi
D_{FLY1}	2	Schottky diode, 100 V, 1 A, POWERDI123	DFLS1100-7	Diodes Inc.
D_{OUT1}	1	Zener, 18 V, 5%, SOD-523	BZX585-C18	Nexperia
D_{OUT2}	1	Zener, 9.1 V, 5%, SOD-523	BZX585-C9V1	Nexperia
R_{FB}	1	102 kΩ, 1%, 0402	Std	Std
R_{SET}	1	12.1 kΩ, 1%, 0402	Std	Std
R_{TC}	1	221 kΩ, 1%, 0402	Std	Std
T_1	1	7 µH, 5 A, 1 : 1.5 : 0.8, 9.2 mm × 9.8 mm × 9.8 mm	Würth Electronik	750318704
		7 µH, 5 A, 1 : 1.5 : 0.8, 13 mm × 11 mm × 10 mm	Coilcraft	ZA9675-BE
U_1	1	PSR flyback converter, VSON-8	Texas Instruments	LM25184NGUR

8.2.3.2 Detailed Design Procedure

Using the LM25184 quick-start calculator, components are selected based on the flyback converter specifications.

8.2.3.2.1 Flyback Transformer – T_1

Set the turns ratio of the transformer secondary windings using 方程式 33, where N_{S1} and N_{S2} are the number of secondary turns for the respective outputs.

$$\frac{N_{S2}}{N_{S1}} = \frac{V_{OUT2} + V_{D2}}{V_{OUT1} + V_{D1}} = \frac{8\ V + 0.3\ V}{15\ V + 0.3\ V} = 0.542 \tag{33}$$

Choose a primary-secondary turns ratio for a 15-V output based on an approximate 70% max duty cycle at minimum input voltage using 方程式 34. The transformer turns ratio when considering both outputs is thus specified as 1 : 1.5 : 0.8.

$$N_{PS} = \frac{D_{MAX}}{1 - D_{MAX}} \cdot \frac{V_{IN(min)}}{V_{OUT} + V_D} = \frac{0.7}{1 - 0.7} \cdot \frac{4.5\,V}{15\,V + 0.3\,V} = 0.69 \tag{34}$$

Select a magnetizing inductance based on the minimum off-time constraint using 方程式 35. Choose a value of 7 µH and a saturation current of 5 A for this application.

$$L_{MAG} \geq \frac{(V_{OUT} + V_D) \cdot N_{PS} \cdot t_{OFF\text{-}MIN}}{I_{SW\text{-}PEAK(FFM)}} = \frac{(15\,V + 0.3\,V) \cdot 1/1.5 \cdot 425\,ns}{0.82\,A} = 5.3\,\mu H \tag{35}$$

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Find the maximum output current for a given turns ratio, assuming the outputs are symmetrically loaded, using 方程式 36.

$$I_{OUT(max)} = \frac{\eta}{2} \cdot \frac{I_{SW\text{-}PEAK}}{\left(\frac{V_{OUT}}{V_{IN}} + \frac{1}{N_{PS}}\right)} = \frac{0.9}{2} \cdot \frac{4.1\,A}{\left(\frac{23\,V}{V_{IN}} + \frac{1}{(1/2.3)}\right)} = \begin{cases} 0.45\,A \text{ at } V_{IN} = 12\,V \\ 0.57\,A \text{ at } V_{IN} = 24\,V \end{cases} \tag{36}$$

8.2.3.2.2 Flyback Diodes – D_{FLY1} and D_{FLY2}

The flyback diode reverse voltages for the positive and negative outputs are given respectively by 方程式 37 and 方程式 38.

$$V_{D1\text{-}REV} \geq \frac{V_{IN(max)}}{N_{PS1}} + V_{OUT1} = \frac{42\,V}{(1/1.5)} + 15\,V = 79\,V \tag{37}$$

$$V_{D2\text{-}REV} \geq \frac{V_{IN(max)}}{N_{PS2}} + \left|V_{OUT2}\right| = \frac{42\,V}{(1/0.8)} + 8\,V = 42\,V \tag{38}$$

Choose 100-V, 1-A and 60-V, 3-A Schottky diodes for the positive and negative outputs, respectively, to allow some margin for inevitable voltage overshoot and ringing related to leakage inductance and diode capacitance. Use an RC snubber circuit across each diode, for example, 100 Ω and 22 pF, to mitigate such overshoot and ringing, particularly if the transformer leakage inductance is high.

8.2.3.2.3 Input Capacitor – C_{IN}

The input capacitor filters the primary-winding current waveform. To prevent large ripple voltage, use a low-ESR ceramic input capacitor sized according to 方程式 25 for the RMS ripple current given by 方程式 26. In this design example, choose a 10-µF, 50-V ceramic capacitor with X7R dielectric and 1210 footprint.

8.2.3.2.4 Output Capacitors – C_{OUT1}, C_{OUT2}

The output capacitors determine the voltage ripple at the converter outputs, limit the voltage excursion during a load transient, and set the dominant pole of the small-signal response of the converter.

Mindful of the voltage coefficient of ceramic capacitors, select two 22-µF, 25-V, X7R capacitors in 1210 case size for the positive output and two 47-µF, 10-V, X7R capacitors in 1210 case size for the negative output.

8.2.3.2.5 Feedback Resistor – R_{FB}

Install a 102-kΩ resistor from SW to FB based on an output voltage setpoint of 15 V (plus a flyback diode voltage drop) reflected to the primary side by a transformer turns ratio of 1 : 1.5.

$$R_{FB} = \frac{(V_{OUT1} + V_{D1}) \cdot N_{PS1}}{0.1\,mA} = \frac{(15\,V + 0.3\,V) \cdot (1/1.5)}{0.1\,mA} = 102\,k\Omega \tag{39}$$

8.2.3.2.6 Thermal Compensation Resistor – R_{TC}

Select a resistor value for output voltage thermal compensation based on 方程式 40.

$$R_{TC}\left[k\Omega\right] = \frac{R_{FB}\left[k\Omega\right]}{N_{PS}} \cdot \frac{3}{TC_{Diode}\left[mV/°C\right]} = \frac{102\,k\Omega \cdot 3}{(1/1/5) \cdot 2} = 230\,k\Omega \tag{40}$$

8.2.3.2.7 Output Voltage Clamp Zeners – D_{OUT1} and D_{OUT2}

Calculate the power delivered to the output at no load based on 方程式 41.

$$P_{OUT(min)} = \frac{L_{MAG} \cdot I_{SW\text{-}PEAK(FFM)}^{2}}{2} \cdot F_{SW(min)} = \frac{7\mu H \cdot (0.82\,A)^{2}}{2} \cdot 12kHz = 28\,mW \tag{41}$$

Select Zener clamp diodes to limit the voltages to a range of 110% to 120% of the nominal output voltage setpoints during no-load operation. Connect 18-V and 9.1-V Zener diodes with ±5% tolerance and SOD-523 package across the positive and negative outputs, respectively.

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8.2.3.3 Application Curves

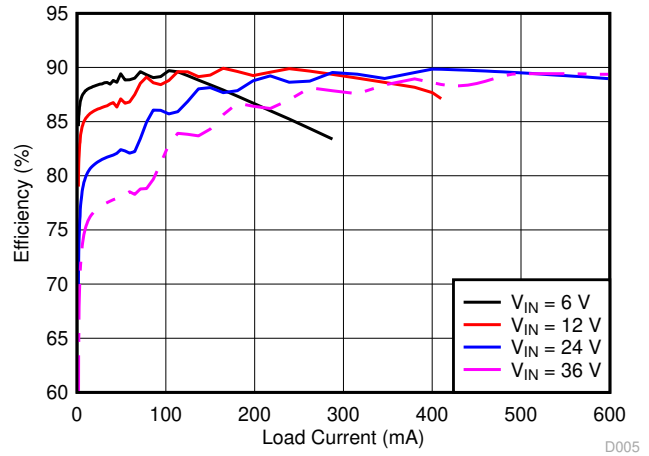


图 8-17. Efficiency (Linear Scale)

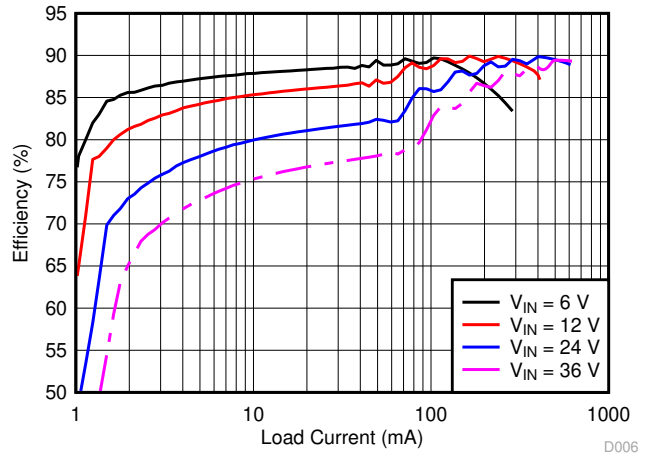


图 8-18. Efficiency (Log Scale)

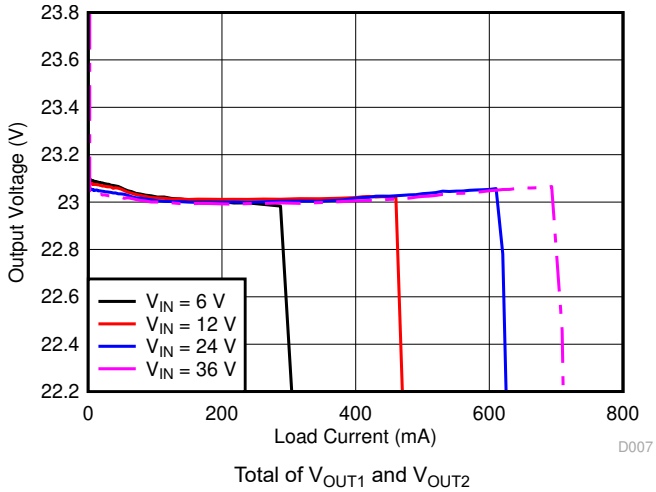


图 8-19. Load Regulation (Linear Scale)

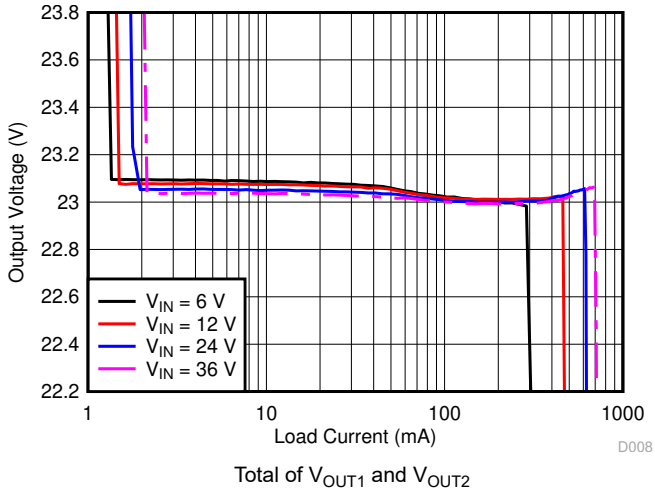
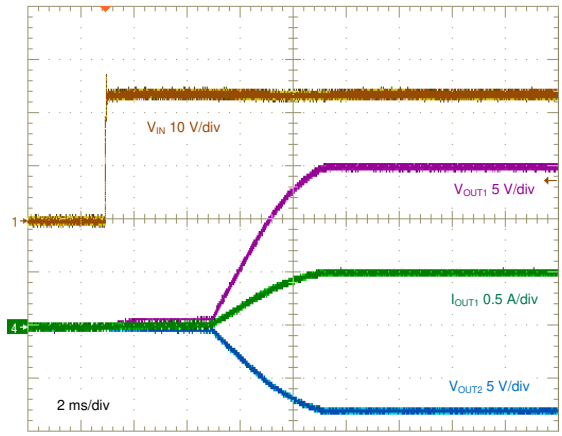
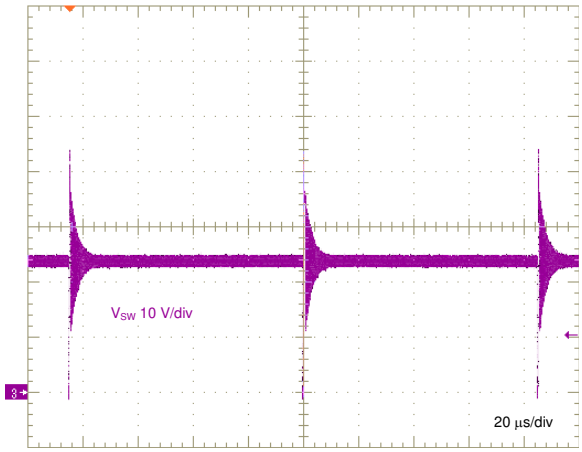


图 8-20. Load Regulation (Log Scale)



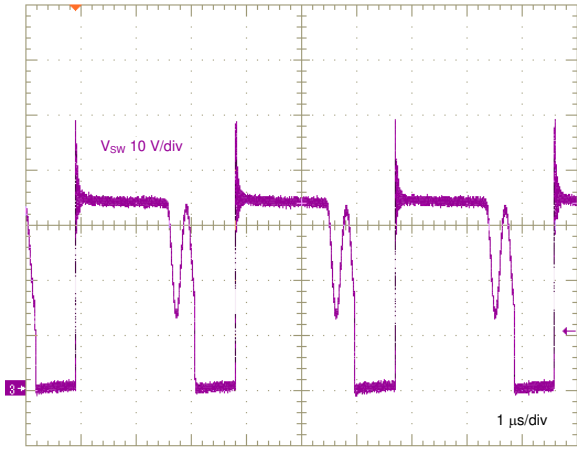
V_{IN} stepped to 24 V 30-Ω and 16-Ω Loads

图 8-21. Start-Up Characteristic



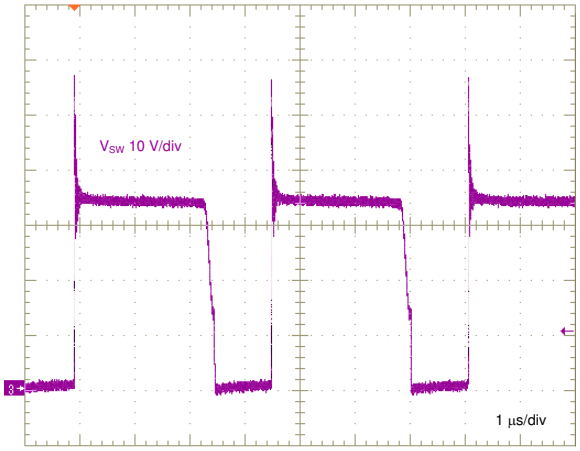
V_{IN} = 24 V I_{OUT1} = I_{OUT2} = 0 A

图 8-22. Switch Voltage, No Load



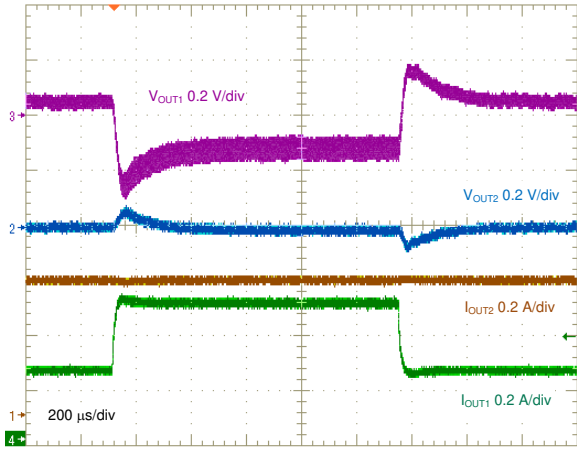
V_{IN} = 24 V I_{OUT1} = I_{OUT2} = 0.3 A

图 8-23. Switch Voltage, Medium Load



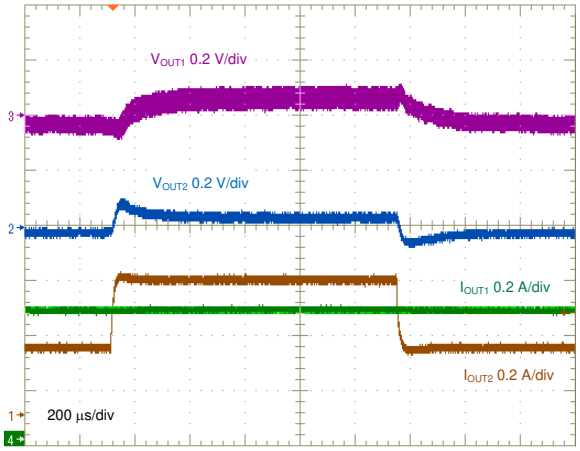
V_{IN} = 24 V I_{OUT1} = I_{OUT2} = 0.5 A

图 8-24. Switch Voltage, Full Load



V_{IN} = 24 V I_{OUT2} = 0.5 A

图 8-25. Positive Output Load Transient, 0.25 A to 0.5 A



V_{IN} = 24 V I_{OUT1} = 0.5 A

图 8-26. Negative Output Load Transient, 0.25 A to 0.5 A

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9 Power Supply Recommendations

The LM25184 flyback converter operates over a wide input voltage range from 4.5 V to 42 V. The characteristics of the input supply must be compatible with 节 6.1 and 节 6.3. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with 方程式 42.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{42}$$

where

- η is the efficiency

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, special care is required to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 22 µF to 100 µF is usually sufficient to provide input damping and helps to hold the input voltage steady during large load transients. A typical ESR of 200 mΩ provides enough damping for most input circuit configurations.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The application report *Simple Success with Conducted EMI for DC-DC Converters* provides helpful suggestions when designing an input filter for any switching regulator.

10 Layout

The performance of any switching converter depends as much upon PCB layout as it does the component selection. The following guidelines are provided to assist with designing a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI. 图 10-1 and 图 10-2 provide layout examples for single-output and dual-output designs, respectively.

10.1 Layout Guidelines

PCB layout is critical for good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with transformer leakage inductance or parasitic capacitance to generate noise and EMI or degrade the performance of the power supply.

1. Bypass VIN to GND with a low-ESR ceramic capacitor, preferably of X7R or X7S dielectric. Place C_{IN} as close as possible to the LM25184 VIN and GND pins. Ground return paths for the input capacitor or capacitors must consist of localized top-side planes that connect to the GND pin and exposed PAD.
2. Minimize the loop area formed by the input capacitor connections and the VIN and GND pins.
3. Locate the transformer close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive e-field or capacitive coupling.
4. Minimize the loop area formed by the diode-Zener clamp circuit connections and the primary winding terminals of the transformer.
5. Minimize the loop area formed by the flyback rectifying diode, output capacitor, and the secondary winding terminals of the transformer.
6. Tie the GND pin directly to the DAP under the device and to a heat-sinking PCB ground plane.
7. Use a ground plane in one of the middle layers as a noise shielding and heat dissipation path.
8. Have a single-point ground connection to the plane. Route the return connections for the reference resistor, soft start, and enable components directly to the GND pin. This prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
9. Make V_{IN+}, V_{OUT+}, and ground bus connections short and wide. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
10. Minimize trace length to the FB pin. Locate the feedback resistor close to the FB pin.
11. Locate components R_{SET}, R_{TC}, and C_{SS} as close as possible to their respective pins. Route with minimal trace lengths.
12. Place a capacitor between input and output return connections to route common-mode noise currents directly back to their source.
13. Provide adequate heatsinking for the LM25184 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the DAP to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. The connection to V_{OUT+} provides heatsinking for the flyback diode.

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10.2 Layout Examples

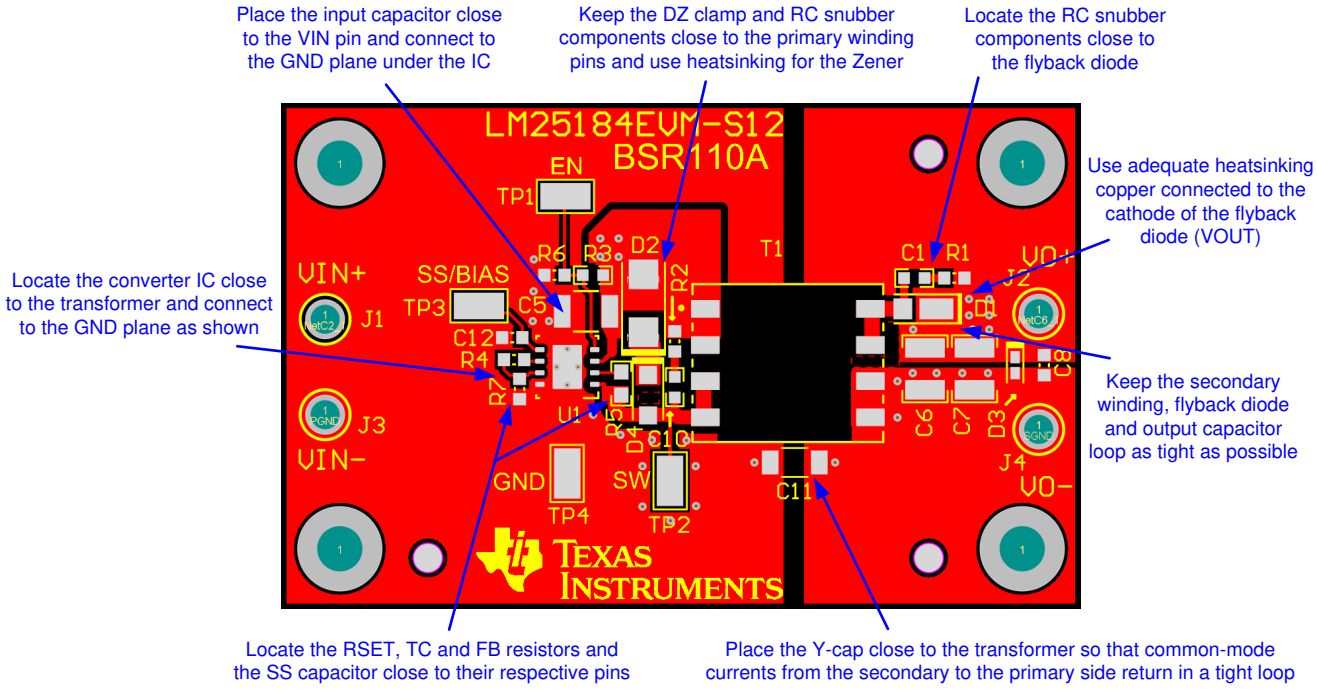

图 10-1. Single-Output PCB Layout Example

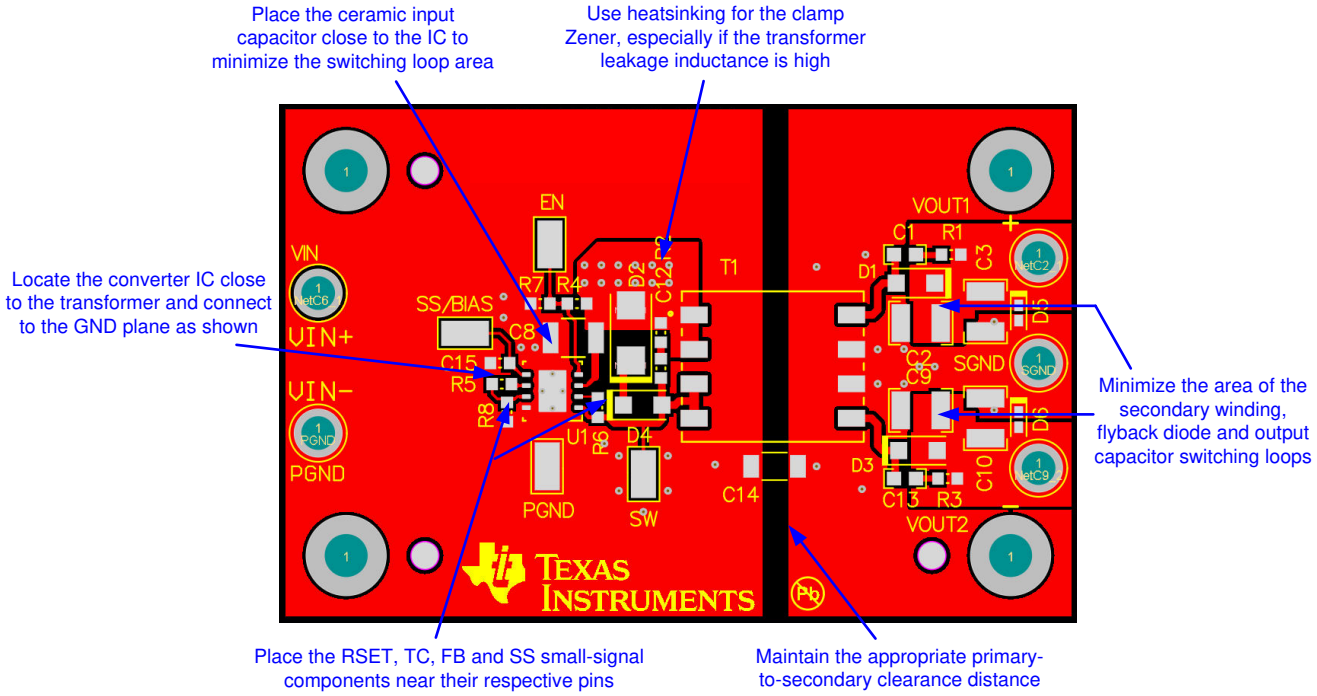

图 10-2. Dual-Output PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

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11.1.2 Development Support

With input voltage range and current capability as specified in 表 11-1, the PSR flyback DC/DC converter family of parts from TI provides flexibility, scalability and optimized solution size for a range of applications. Using an 8-pin WSON package with 4-mm × 4-mm footprint and 0.8-mm pin pitch, these converters enable isolated DC/DC solutions with high density and low component count.

表 11-1. PSR Flyback DC/DC Converter Family

PSR FLYBACK DC/DC CONVERTER	INPUT VOLTAGE RANGE	PEAK SWITCH CURRENT	MAXIMUM LOAD CURRENT, V_{OUT} = 12 V, N_{PS} = 1	
			V_{IN} = 4.5 V	V_{IN} = 13.5 V
LM5181	4.5 V to 65 V	0.75 A	90 mA	180 mA
LM5180	4.5 V to 65 V	1.5 A	180 mA	360 mA
LM25180	4.5 V to 42 V	1.5 A	180 mA	360 mA
LM25183	4.5 V to 42 V	2.5 A	300 mA	600 mA
LM25184	4.5 V to 42 V	4.1 A	500 mA	1 A

For development support, see the following:

- LM25184 *Quick-start Calculator*
- LM25184 *Simulation Models*
- For TI's reference design library, visit TI Designs
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center
- To view a related device of this product, see the LM25183 product page
- TI Designs:
  - *Isolated IGBT Gate-Drive Power Supply Reference Design With Integrated Switch PSR Flyback Controller*
  - *Compact, Efficient, 24-V Input Auxiliary Power Supply Reference Design for Servo Drives*
  - *Reference Design for Power-Isolated Ultra-Compact Analog Output Module*
  - *HEV/EV Traction Inverter Power Stage with 3 Types of IGBT/SiC Bias-Supply Solutions Reference Design*
  - *4.5-V to 65-V Input, Compact Bias Supply With Power Stage Reference Design for IGBT/SiC Gate Drivers*
  - *Channel-to-Channel Isolated Analog Input Module Reference Design*
  - *SiC/IGBT Isolated Gate Driver Reference Design With Thermal Diode and Sensing FET*
  - *>95% Efficiency, 1-kW Analog Control AC/DC Reference Design for 5G Telecom Rectifier*
  - *3.5-W Automotive Dual-output PSR Flyback Regulator Reference Design*
- TI Technical Articles:
  - *Flyback Converters: Two Outputs are Better Than One*
  - *Common Challenges When Choosing the Auxiliary Power Supply for Your Server PSU*
  - *Maximizing PoE PD Efficiency on a Budget*

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25184 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

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In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *LM25184 Single-Output EVM User's Guide* (SNVU680)
- *LM5180 Single-Output EVM User's Guide* (SNVU592)
- *LM5180 Dual-Output EVM User's Guide* (SNVU609)
- *How an Auxless PSR Flyback Converter can Increase PLC Reliability and Density* (SLYT779)
- *Why Use PSR-Flyback Isolated Converters in Dual-Battery mHEV Systems* (SLYT791)
- *IC Package Features Lead to Higher Reliability in Demanding Automotive and Communications Equipment Systems* (SNVA804)
- *PSR Flyback DC/DC Converter Transformer Design for mHEV Applications* (SNVA805)
- *Flyback Transformer Design Considerations for Efficiency and EMI* (SLUP338)
- *Under the Hood of Flyback SMPS Designs* (SLUP261)
- White Papers:
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications* (SLYY104)
  - *An Overview of Conducted EMI Specifications for Power Supplies* (SLYY136)
  - *An Overview of Radiated EMI Specifications for Power Supplies* (SLYY142)
- *Using New Thermal Metrics Application Report* (SBVA025)
- *Semiconductor and IC Package Thermal Metrics Application Report* (SPRA953)
- *AN-2162: Simple Success with Conducted EMI from DC-DC Converters* (SNVA489)

11.3 接收文档更新通知

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11.4 支持资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

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12 Mechanical, Packaging, and Orderable Information

The following pages have mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25184NGUR	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	LM25184 NGU
LM25184NGUR.A	Active	Production	WSON (NGU) | 8	4500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	LM25184 NGU

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM25184 :

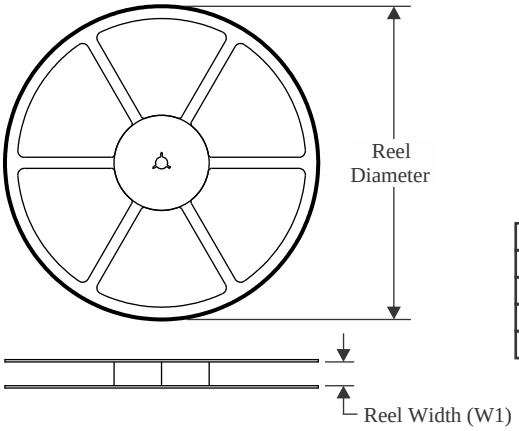
- Automotive : LM25184-Q1

NOTE: Qualified Version Definitions:

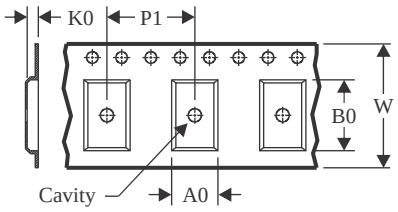
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

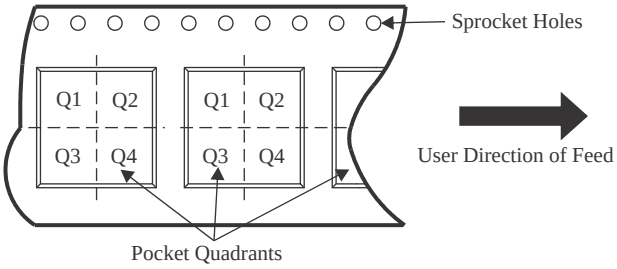


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

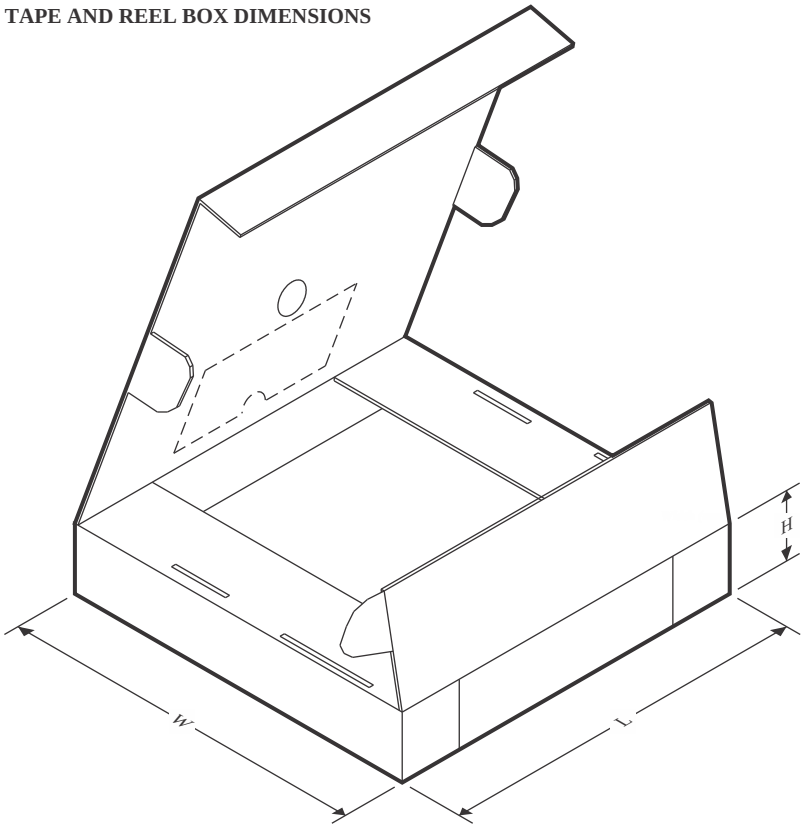
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

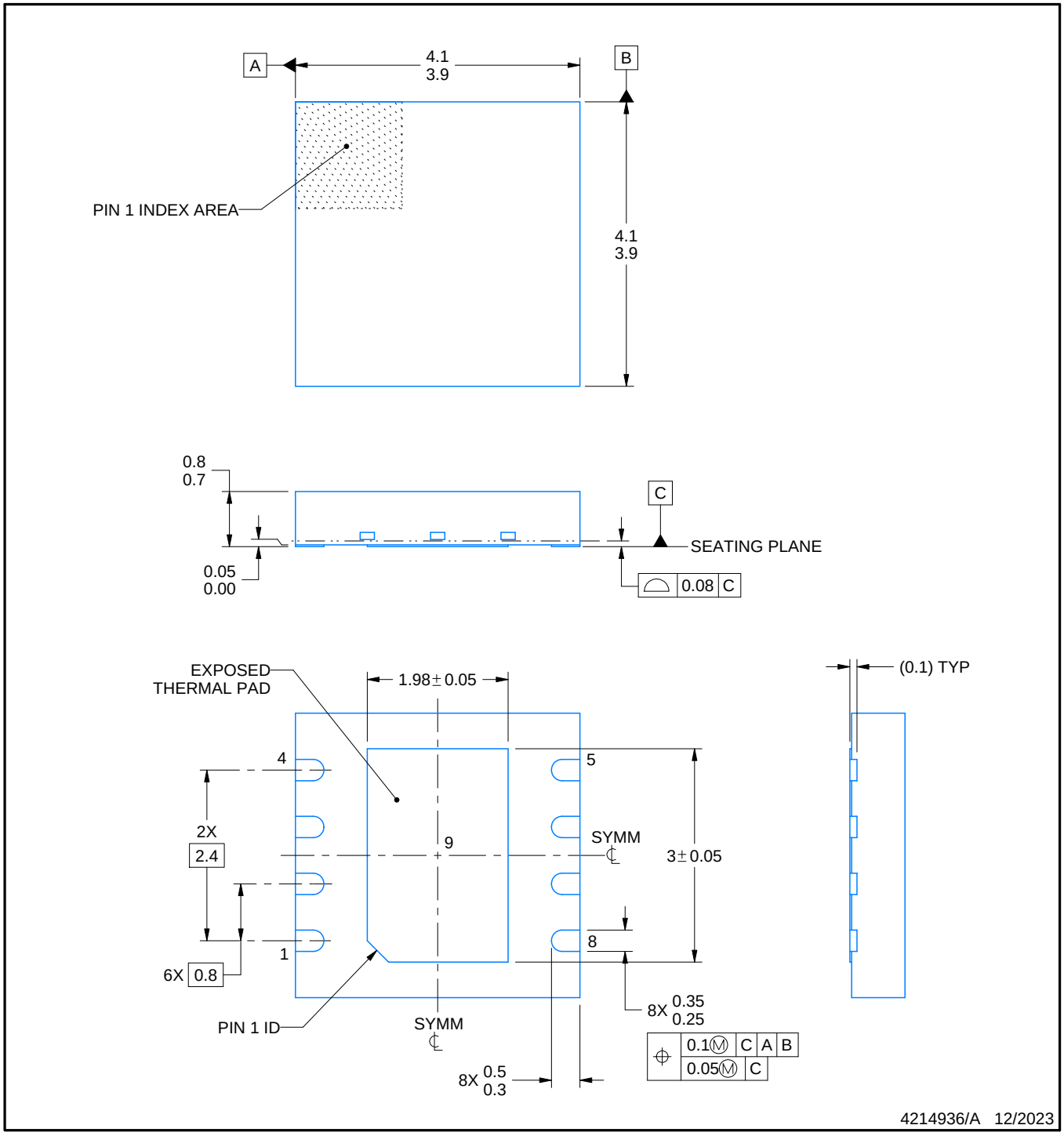
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25184NGUR	WSON	NGU	8	4500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



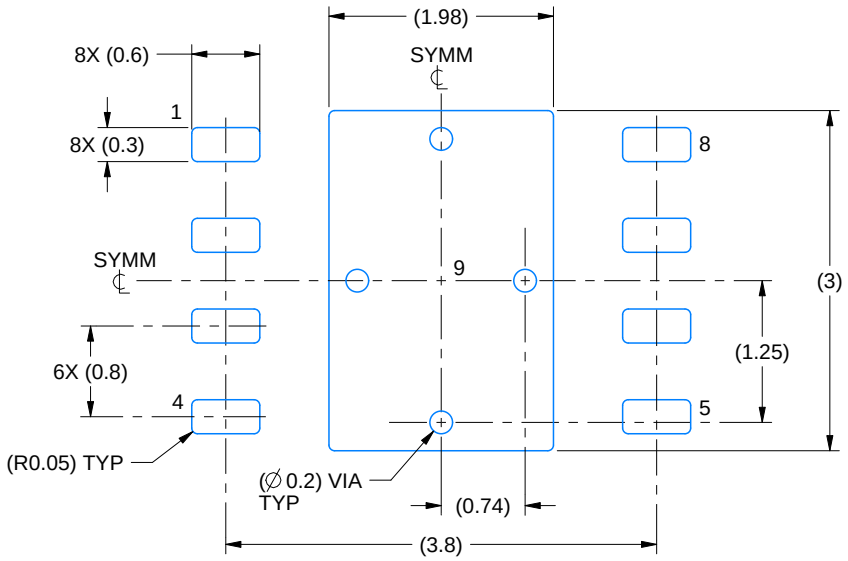
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25184NGUR	WSON	NGU	8	4500	360.0	360.0	36.0

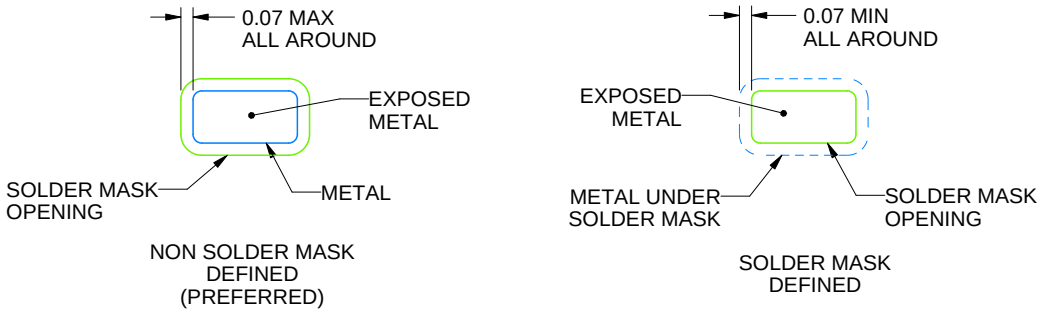


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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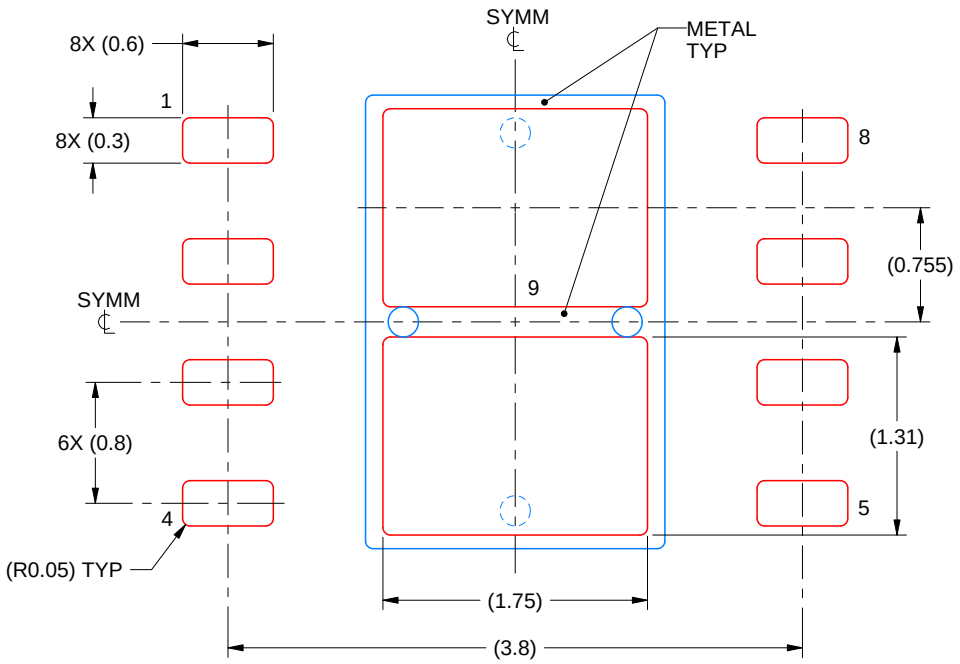
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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