LM117QML-SP RHA 4.25V 至 41.25-V 3 端可调稳压器

1 特性

- 耐辐射加固保障 (RHA) 高达 100krad(Si) 总电离剂量 (TID)
  - 具有高剂量率 (HDR)：50 – 300rad(Si)/s
  - 具有低剂量率 (LDR)：10mrad(Si)/s
- 指定的 0.5A 或 1.5A 输出电流选项
- 低至 1.2V 的可调节输出
- 电流限制在各种温度下保持恒定
- 输出受到短路保护

2 应用

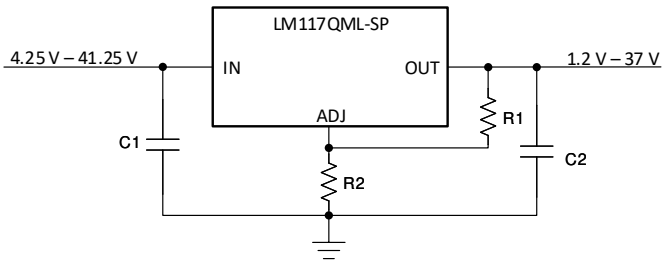
- 卫星电力系统 (EPS)
- PWM 控制器的辅助电源

3 说明

LM117QML-SP 3 端子正电压线性稳压器能够在 1.2V 至 37V 输出范围内提供 0.5A 或 1.5A 的电流。它简单易用，并且仅需要 2 个外部电阻器即可设置输出电压。

该稳压器是浮动的并且仅检测输入到输出差分电压，因此，只要不超过最大输入到输出差分电压，就可以调节几百伏特的电源电压。

经飞行验证的 LM117QML-SP 可提供电流限制、热过载保护和安全区保护等完整的过载保护功能。它用途广泛，还可用作可调节开关稳压器、可编程输出稳压器和精密电流调节器等。



典型电路原理图

对于高电压应用，LM117HVQML-SP 是一款引脚对引脚可直接替代器件，适合不超过 60V 的电压。有关 LM117QML-SP 负电压稳压器，请参阅 LM137QML-SP。

器件信息

器件型号(1)	等级(2)	封装(3)
LM117GWRLQMLV	LDR 飞行等级 QMLV RHA 100krad(Si)	CFP SOIC (NAC) 16 引脚 6.35mm × 9.91mm 质量 = 0.467g(5)
5962R9951707VZA		
LM117GWRQMLV	HDR 飞行等级 QMLV RHA 100krad(Si)	
5962R9951706VZA		
LM117HRLQMLV	LDR 飞行等级 QMLV RHA 100krad(Si)	TO-39 (NDT) 3 引脚 8.26mm × 8.26mm 质量 = 1.036g(5)
5962R9951705VXA		
LM117HRQMLV	HDR 飞行等级 QMLV RHA 100krad(Si)	
5962R9951703VXA		
LM117NDT/EM	工程样片(4)	
LM117KRQMLV	HDR 飞行等级 QMLV RHA 100krad(Si)	TO-3 (K) 2 引脚 25.4mm × 38.94mm 质量 = 12.291g(5)
5962R9951704VYA		
LM117K/EM	工程样片(4)	
LM117H MDE	LDR 飞行等级 QMLV RHA 100krad(Si)	裸片 2.18mm × 2.36mm
5962R9951705V9A		
LM117H MDR	HDR 飞行等级 QMLV RHA 100krad(Si)	
5962R9951703V9A		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 有关器件等级的其他信息，请查看 SLYB235。
(3) 有关更多的封装详细信息，请参考 TI 封装页面。
(4) 这些器件仅适用于工程评估，按照不合规的流程进行加工处理。不适用于鉴定、量产、辐射测试或飞行用途。无法在完整 MIL 额定温度范围（–55°C 至 125°C）内或使用寿命期间保证其性能。
(5) 质量误差在 ±10% 以内。

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
April 2021	*	Initial Release

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5 Device Comparison Table

PART NUMBER	INPUT VOLTAGE RANGE	I_{OUT}	PART NUMBER SUFFIX	PACKAGE	RADIATION TESTING (1)
LM117QML-SP	4.25 V to 41.25 V	1.5 A	K	TO-3 (K) 2 pin	HDR 100 krad(Si)
		0.5 A	H	TO-39 (NDT) 3 pin	LDR 100 krad(Si)
					HDR 100 krad(Si)
				Die	LDR 100 krad(Si)
					HDR 100 krad(Si)
			GW	CFP SOIC (NAC) 16 pin	LDR 100 krad(Si)
					HDR 100 krad(Si)
LM117HVQML-SP	4.25 V to 60 V	0.5 A	H	TO-39 (NDT) 3 pin	LDR 100 krad(Si)
					HDR 100 krad(Si)
				Die	LDR 100 krad(Si)
					HDR 100 krad(Si)
			GW	CFP SOIC (NAC) 16 pin	LDR 100 krad(Si)
					HDR 100 krad(Si)
LM137QML-SP	–41.25 V to –4.25 V	1.5 A	H	TO-39 (NDT) 3 pin	HDR 30 krad(Si)

(1) The Device Information table can be referenced for information on which part numbers correspond to LDR or HDR options.

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6 Pin Configurations and Functions

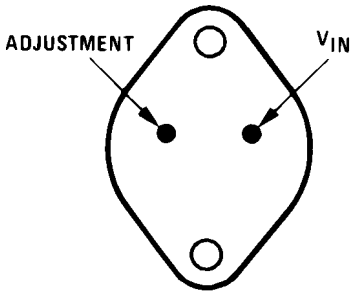


图 6-1. LM117K K Package
2-Pin TO-3 (Metal Can)
Bottom View

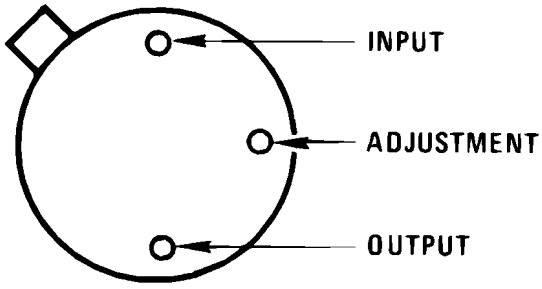


图 6-2. LM117H, LM117NDT NDT Package
3-Pin TO-39 (Metal Can)
Bottom View

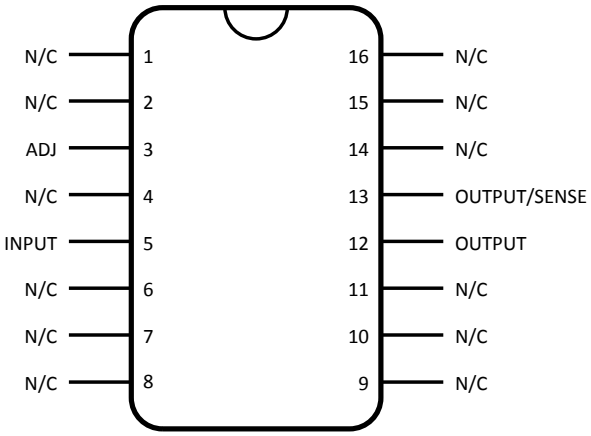


图 6-3. LM117GW NAC Package
16-Pin CFP SOIC
Top View

表 6-1. Pin Functions

PIN				I/O	DESCRIPTION
NAME	TO-3	TO-39	CFP SOIC		
ADJ	1	2	3	—	Adjust pin
V_{IN}	2	1	5	I	Input voltage pin for the regulator
V_{OUT}	CASE	3, CASE	12	O	Output voltage pin for the regulator
OUTPUT/SENSE	—	—	13	—	Used to sense the output voltage. Must be connected to VOUT for proper operation.
N/C	—	—	1, 2, 4, 6, 7, 8, 9, 10, 11, 14, 15, 16	—	No connection. These pins have no internal connections and may be grounded or left floating. They may also be connected to the board heatsink and used for thermal dissipation.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Power dissipation(2)	Internally limited		
	Input-output voltage differential	–0.3	40	V
T_{stg}	Storage temperature	–65	150	°C
T_{Jmax}	Maximum junction temperature		150	°C
	Lead temperature metal package		300	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2 W for the TO-39 and CFP packages, and 20 W for the TO-3 package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1) (2)	±3000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) Human body model, 100 pF discharged through a 1.5-kΩ resistor.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
T_A	Operating temperature	–55	125	°C
V_{IN}	Input voltage	4.25	41.25	V

7.4 Thermal Information

THERMAL METRIC(1)			PACKAGE			UNIT
			TO-3 (K) 2 pin (LM117K)	TO-39 (NDT) 3 pin (LM117H)	CFP SOIC (NAC) 16 pin (LM117GW)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Still air	39	186	130	°C/W
		500 LF/min air flow	14	64	80	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		1.9	21	7	°C/W

(1) For more information, see the *Semiconductor and IC package thermal metrics* application report.

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7.5 Electrical Characteristics: 0.5 – A I_{OUT} Devices (LM117H, LM117GW)

Over operating temperature range (T = – 55°C to 125°C) unless otherwise noted.

PARAMETER		TEST CONDITIONS[(1)]		SUBGROUP[(2)]	MIN	MAX	UNIT
V_O	Output voltage	V_I = 4.25 V, I_L = – 5 mA		1, 2, 3	1.2	1.3	V
			25°C Post-radiation	1		1.35	
		V_I = 4.25 V, I_L = – 500 mA		1, 2, 3	1.2	1.3	
			25°C Post-radiation	1		1.35	
		V_I = 41.25 V, I_L = – 5 mA		1, 2, 3	1.2	1.3	
			25°C Post-radiation	1		1.35	
		V_I = 41.25V, I_L = – 50mA		1, 2, 3	1.2	1.3	
			25°C Post-radiation	1		1.35	
		V_I = 6.25 V, I_L = – 5 mA	125°C	2	1.2	1.3	
V_{RLine}	Line regulation	4.25 V ≤ V_I ≤ 41.25 V, I_L = – 5 mA	25°C	1	– 9	9	mV
			125°C, – 55°C	2, 3	– 23	23	
			25°C Post-radiation	1	– 25	25	
V_{RLoad}	Load regulation	V_I = 6.25 V, – 500 mA ≤ I_L ≤ – 5 mA		1, 2, 3	– 12	12	mV
		V_I = 41.25 V, – 50 mA ≤ I_L ≤ – 5 mA		1, 2, 3	– 12	12	
V_{RTh}	Thermal regulation	V_I = 14.6 V, I_L = – 500 mA	25°C	1	– 12	12	mV
I_{Adj}	Adjust pin current	V_I = 4.25 V, I_L = – 5 mA		1, 2, 3	– 100	– 15	µA
		V_I = 41.25 V, I_L = – 5 mA		1, 2, 3	– 100	– 15	
ΔI_{Adj}/ Line	Adjust pin current change	4.25 V ≤ V_I ≤ 41.25 V, I_L = – 5 mA		1, 2, 3	– 5	5	µA
ΔI_{Adj} / Load	Adjust pin current change	V_I = 6.25 V, – 500 mA ≤ I_L ≤ – 5 mA		1, 2, 3	– 5	5	µA
I_Q	Minimum load current	V_I = 4.25 V, Forced V_O = 1.4 V		1, 2, 3	– 3	– 0.5	mA
		V_I = 14.25 V, Forced V_O = 1.4 V		1, 2, 3	– 3	– 0.5	
		V_I = 41.25 V, Forced V_O = 1.4 V		1, 2, 3	– 5	– 1	
I_{OS}	Output short circuit current	V_I = 4.25 V		1, 2, 3	– 1.8	– 0.5	A
		V_I = 40 V		1, 2, 3	– 0.5	– 0.05	
V_O (Recov)	Output voltage recovery	V_I = 4.25 V, R_L = 2.5 Ω, C_L = 20 µF		1, 2, 3	1.2	1.3	V
			25°C Post-radiation	1		1.35	
		V_I = 40 V, R_L = 250 Ω		1, 2, 3	1.2	1.3	
			25°C Post-radiation	1		1.35	
V_{Start}	Voltage start-up	V_I = 4.25 V, R_L = 2.5 Ω, C_L = 20 µF, I_L = – 500 mA		1, 2, 3	1.2	1.3	V
V_{NO}	Output noise voltage	V_I = 6.25 V, I_L = – 50 mA	25°C	7		120	μV_{RMS}

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7.5 Electrical Characteristics: 0.5 – A I_{OUT} Devices (LM117H, LM117GW) (continued)

Over operating temperature range (T = – 55°C to 125°C) unless otherwise noted.

PARAMETER		TEST CONDITIONS(1)		SUBGROUP(2)	MIN	MAX	UNIT
$\Delta V_O / \Delta V_I$	Line transient response	V_I = 6.25 V, ΔV_I = 3 V, I_L = – 10 mA	25°C	7		6	mV/V
$\Delta V_O / \Delta I_L$	Load transient response	V_I = 6.25V, ΔI_L = – 200 mA, I_L = – 50 mA	25°C	7		0.6	mV/mA
$\Delta V_I / \Delta V_O$	Ripple rejection	V_I = 6.25 V, I_L = – 125 mA, E_I = 1 V_{RMS} at f = 2400 Hz	25°C	4	65		dB
			25°C Post-radiation	4	60		

(1) Pre- and post-irradiation limits are identical for the parameters above unless specified by the test conditions.
(2) For subgroup definitions, see Quality Conformance Inspection table.

7.6 Parameter Drift: 0.5 – A I_{OUT} Devices (LM117H, LM117GW)

The following deltas are for Group C (Life Test). Data is measured at 25°C.

PARAMETER		TEST CONDITIONS	SUBGROUP (1)	MIN	MAX	UNIT
V_O	Output voltage	V_I = 4.25 V, I_L = – 5 mA	1	– 0.01	0.01	V
		V_I = 4.25 V, I_L = – 500 mA	1	– 0.01	0.01	
		V_I = 41.25 V, I_L = – 5 mA	1	– 0.01	0.01	
		V_I = 41.25 V, I_L = – 50 mA	1	– 0.01	0.01	
V_{RLine}	Line regulation	4.25 V ≤ V_I ≤ 41.25 V, I_L = – 5 mA	1	– 4.0	4.0	mV
I_{Adj}	Adjust pin current	V_I = 4.25 V, I_L = – 5 mA	1	– 10	10	µA
		V_I = 41.25 V, I_L = – 5 mA	1	– 10	10	
V_O (Recov)	Output voltage recovery	V_I = 4.25 V, R_L = 2.5 Ω, C_L = 20 µF	1	– 0.01	0.01	V
		V_I = 40 V, R_L = 250 Ω	1	– 0.01	0.01	

(1) For subgroup definitions, see Quality Conformance Inspection table.

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7.7 Electrical Characteristics: 1.5 – A I_{OUT} Devices (LM117K)

Over operating temperature range (T = – 55°C to 125°C) unless otherwise noted.

PARAMETER		TEST CONDITIONS ((1))		SUBGROUP((2))	MIN	MAX	UNIT
V_O	Output voltage	V_I = 4.25 V, I_L = – 5 mA		1, 2, 3	1.2	1.3	V
			25°C Post-radiation	1		1.35	
		V_I = 4.25 V, I_L = – 1.5 A		1, 2, 3	1.2	1.3	
			25°C Post-radiation	1		1.35	
		V_I = 41.25 V, I_L = – 5 mA		1, 2, 3	1.2	1.3	
			25°C Post-radiation	1		1.35	
		V_I = 41.25 V, I_L = – 200 mA		1, 2, 3	1.2	1.3	
			25°C Post-radiation	1		1.35	
		V_I = 6.25 V, I_L = – 5 mA	125°C	2	1.2	1.3	
V_{RLine}	Line regulation	4.25 V ≤ V_I ≤ 41.25 V, I_L = – 5 mA	25°C	1	– 9	9	mV
			125°C, – 55°C	2, 3	– 23	23	
			25°C Post-radiation	1	– 25	25	
V_{RLoad}	Load regulation	V_I = 6.25 V, – 1.5 A ≤ I_L ≤ – 5 mA	25°C	1	– 3.5	3.5	mV
			125°C, – 55°C	2, 3	– 12	12	
			25°C Post-radiation	1	– 7	7	
		V_I = 41.25 V, – 200 mA ≤ I_L ≤ – 5 mA	25°C	1	– 3.5	3.5	
			125°C, – 55°C	2, 3	– 12	12	
			25°C Post-radiation	1	– 7	7	
V_{RTh}	Thermal regulation	V_I = 14.6 V, I_L = – 1.5 A	25°C	1	– 12	12	mV
I_{Adj}	Adjust pin current	V_I = 4.25 V, I_L = – 5 mA		1, 2, 3	– 100	– 15	µA
		V_I = 41.25 V, I_L = – 5 mA		1, 2, 3	– 100	– 15	
ΔI_{Adj}/ Line	Adjust pin current change	4.25 V ≤ V_I ≤ 41.25 V, I_L = – 5 mA		1, 2, 3	– 5	5	µA
ΔI_{Adj} / Load	Adjust pin current change	V_I = 6.25 V, – 1.5 A ≤ I_L ≤ – 5 mA		1, 2, 3	– 5	5	µA
I_Q	Minimum load current	V_I = 4.25 V, Forced V_O = 1.4 V		1, 2, 3	– 3	– 0.2	mA
		V_I = 14.25 V, Forced V_O = 1.4 V		1, 2, 3	– 3	– 0.2	
		V_I = 41.25 V, Forced V_O = 1.4 V		1, 2, 3	– 5	– 0.2	
I_{OS}	Output short circuit current	V_I = 4.25 V		1, 2, 3	– 3.5	– 1.5	A
		V_I = 40 V		1, 2, 3	– 1	– 0.18	

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7.7 Electrical Characteristics: 1.5 – A I_{OUT} Devices (LM117K) (continued)

Over operating temperature range (T = – 55°C to 125°C) unless otherwise noted.

PARAMETER		TEST CONDITIONS ((1))		SUBGROUP((2))	MIN	MAX	UNIT
V_O (Recov)	Output voltage recovery	V_I = 4.25 V, R_L = 0.833 Ω, C_L = 20 µF		1, 2, 3	1.2	1.3	V
			25°C Post-radiation	1		1.35	
		V_I = 40 V, R_L = 250 Ω		1, 2, 3	1.2	1.3	
			25°C Post-radiation	1		1.35	
V_{Start}	Voltage start-up	V_I = 4.25 V, R_L = 0.833 Ω, C_L = 20 µF, I_L = – 1.5 A		1, 2, 3	1.2	1.3	V
V_{NO}	Output noise voltage	V_I = 6.25 V, I_L = – 100 mA	25°C	7		120	μV_{RMS}
ΔV_O / ΔV_I	Line transient response	V_I = 6.25 V, ΔV_I = 3 V, I_L = – 10 mA	25°C	7		18	mV
ΔV_O / ΔI_L	Load transient response	V_I = 6.25 V, ΔI_L = – 400 mA, I_L = – 100 mA	25°C	7		120	mV
ΔV_I / ΔV_O	Ripple rejection	V_I = 6.25 V, I_L = – 500 mA, E_I = 1 V_{RMS} at f = 2400 Hz	25°C	4	65		dB
			25°C Post-radiation	4	60		

(1) Pre- and post-irradiation limits are identical for the parameters above unless specified by the test conditions.
(2) For subgroup definitions, see Quality Conformance Inspection table.

7.8 Parameter Drift: 1.5 – A I_{OUT} Devices (LM117K)

The following deltas are for Group C (Life Test). Data is measured at 25°C.

PARAMETER		TEST CONDITIONS	SUBGROUP ((1))	MIN	MAX	UNIT
V_O	Output voltage	V_I = 4.25 V, I_L = – 5 mA	1	– 0.01	0.01	V
		V_I = 4.25 V, I_L = – 1.5 A	1	– 0.01	0.01	
		V_I = 41.25 V, I_L = – 5 mA	1	– 0.01	0.01	
		V_I = 41.25 V, I_L = – 200 mA	1	– 0.01	0.01	
V_{RLine}	Line regulation	4.25 V ≤ V_I ≤ 41.25 V, I_L = – 5 mA	1	– 4.0	4.0	mV
I_{Adj}	Adjust pin current	V_I = 4.25 V, I_L = – 5 mA	1	– 10	10	µA
		V_I = 41.25 V, I_L = – 5 mA	1	– 10	10	
V_O (Recov)	Output voltage recovery	V_I = 4.25 V, R_L = 0.833 Ω, C_L = 20 µF	1	– 0.01	0.01	V
		V_I = 40 V, R_L = 250 Ω	1	– 0.01	0.01	

(1) For subgroup definitions, see Quality Conformance Inspection table.

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7.9 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	– 55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	– 55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	– 55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	– 55

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7.10 Typical Characteristics

Output capacitor = 0 μF unless otherwise noted

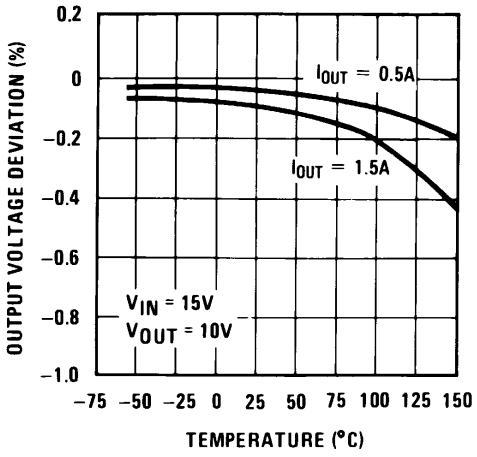


图 7-1. Load Regulation

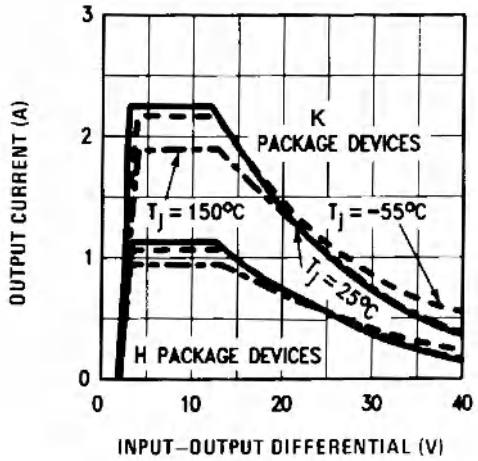


图 7-2. Current Limit

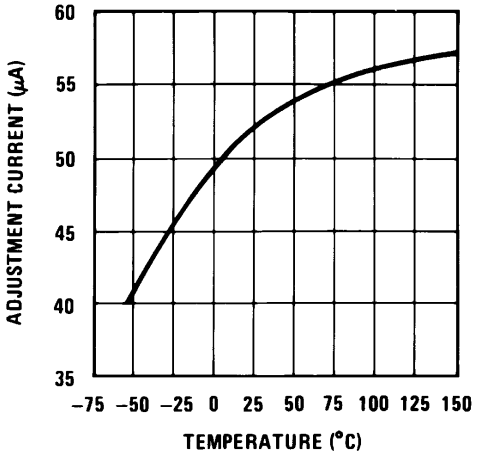


图 7-3. Adjustment Current

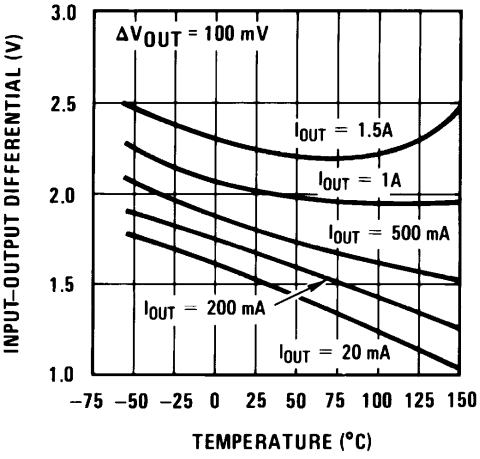


图 7-4. Dropout Voltage

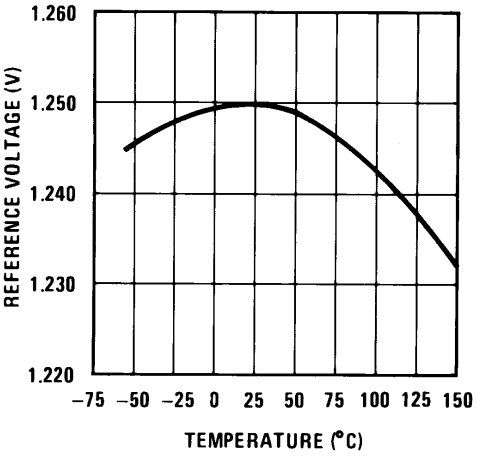


图 7-5. Temperature Stability

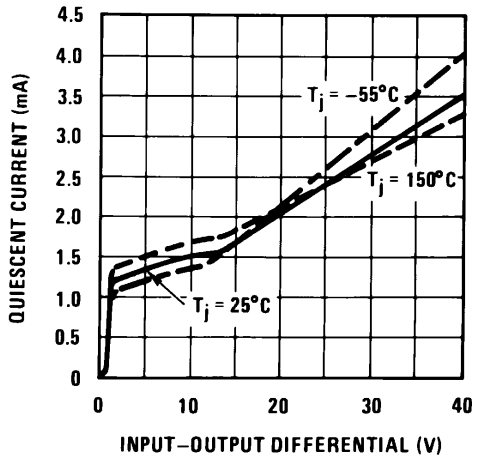


图 7-6. Minimum Operating Current

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7.10 Typical Characteristics (continued)

Output capacitor = 0 μF unless otherwise noted

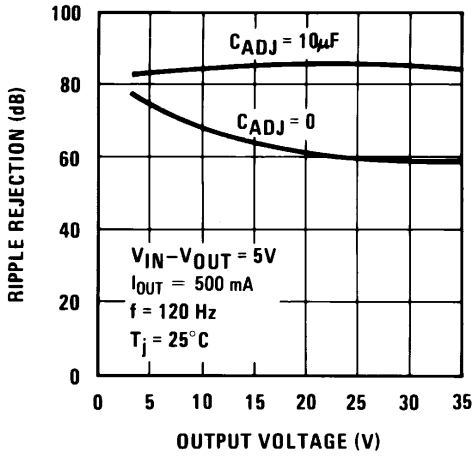


图 7-7. Ripple Rejection

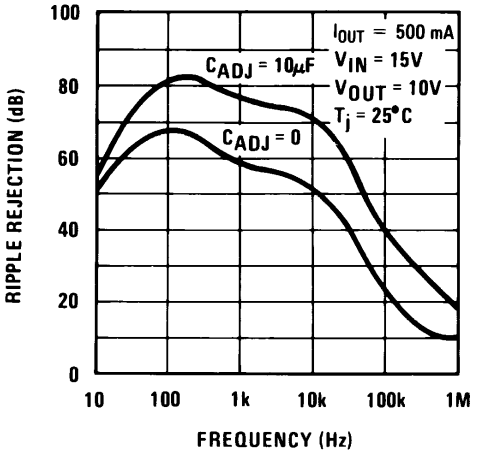


图 7-8. Ripple Rejection

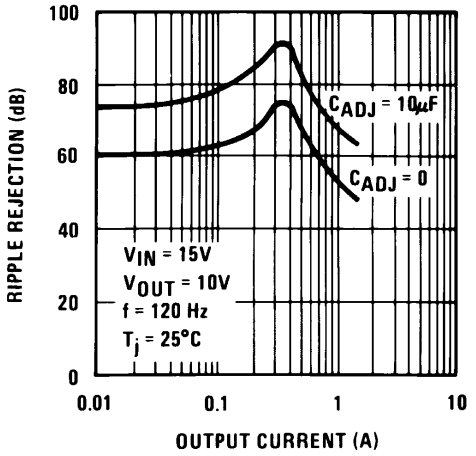


图 7-9. Ripple Rejection

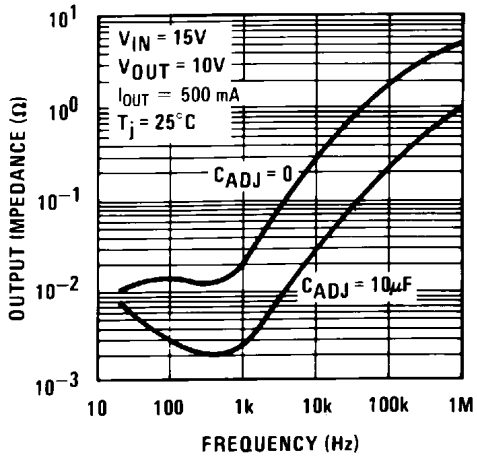


图 7-10. Output Impedance

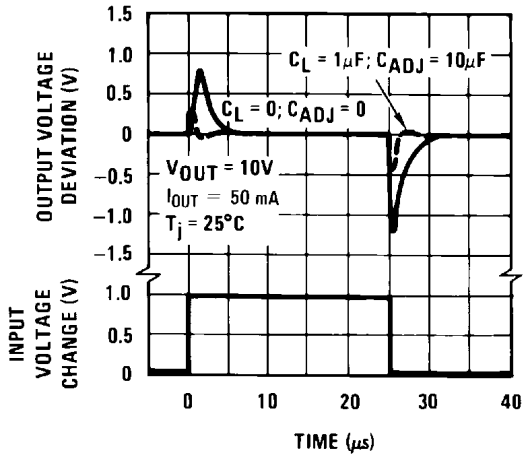


图 7-11. Line Transient Response

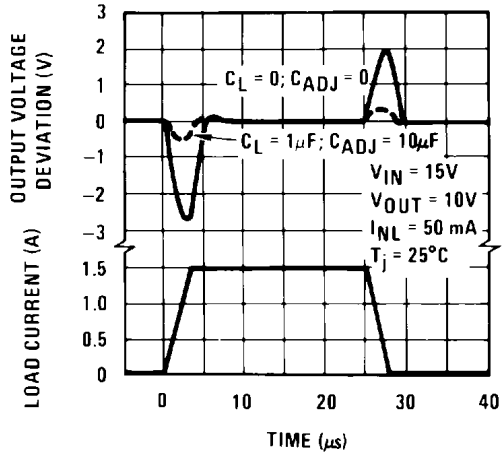


图 7-12. Load Transient Response

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8 Detailed Description

8.1 Overview

The LM117QML-SP 3-terminal positive voltage linear regulator is capable of supplying either 0.5 A or 1.5 A over a 1.2-V to 37-V output range. It is simple to use and requires only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators.

The regulator is "floating" and sees only the input-to-output differential voltage, thus enabling supplies of several hundred volts to be regulated as long as the maximum input-to-output differential is not exceeded (i.e. don’t short circuit the output).

The LM117QML-SP offers full overload protection such as current limit, thermal overload protection, and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Typically, no capacitors are needed unless the device is situated more than 6 in from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

This device makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output it can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2 V where most loads draw little current.

8.2 Functional Block Diagram

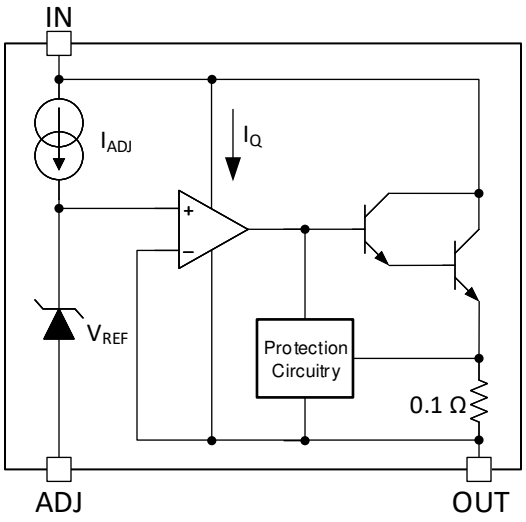


图 8-1. Functional Block Diagram

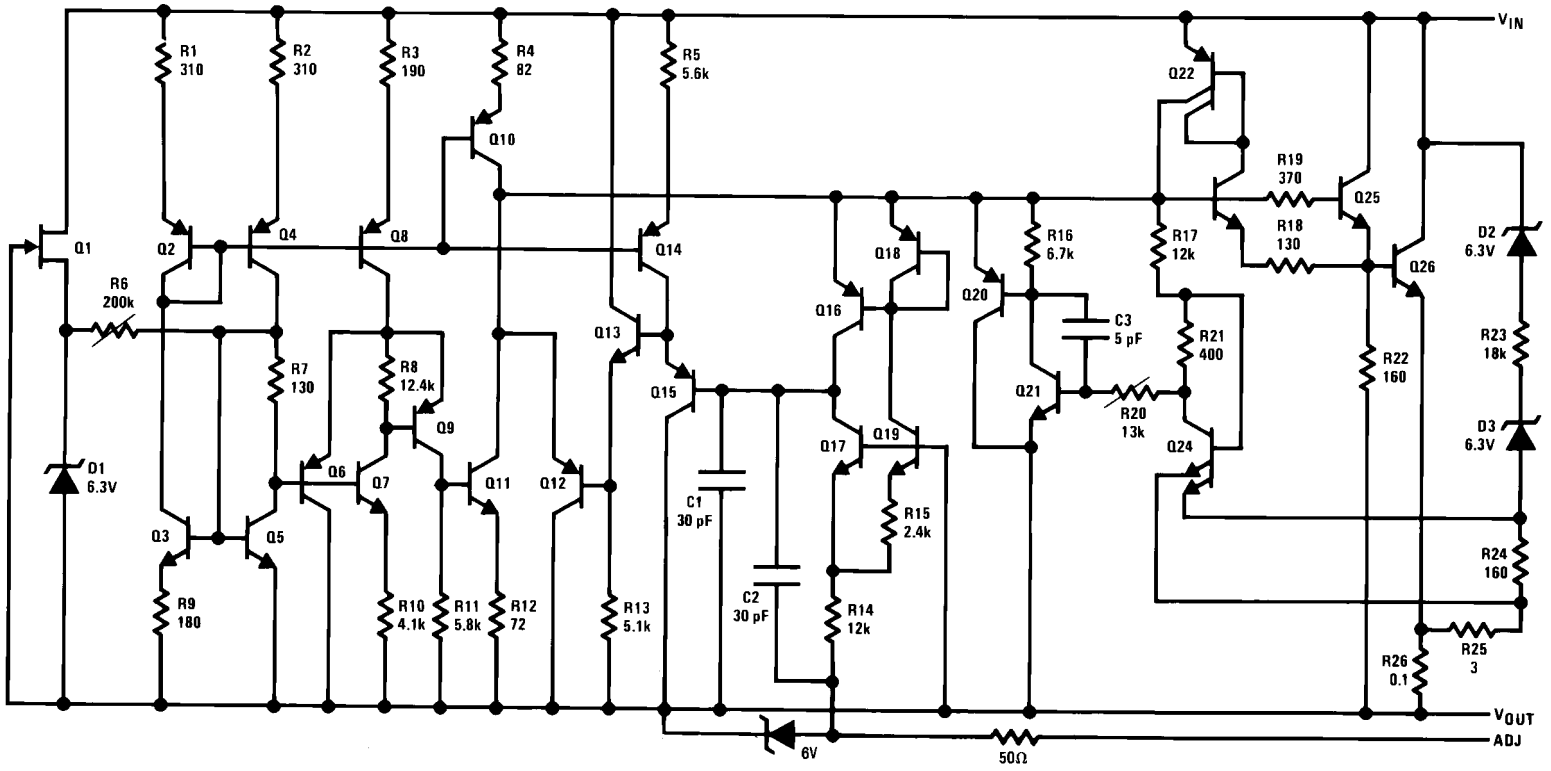
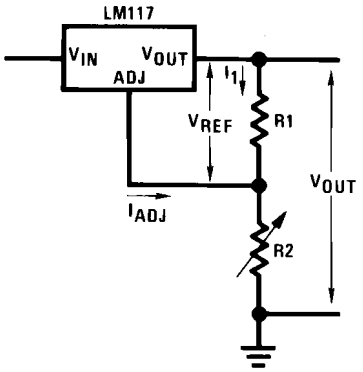


图 8-2. Simplified Device Schematic

8.3 Setting Output Voltage

In operation, the LM117 develops a nominal 1.25-V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is expressed across R1 and, since the voltage is constant, a constant current I_1 then flows through R2, giving an output voltage found by using 方程式 1.

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2 \quad (1)$$



Since the 100- μA current from the adjustment terminal represents an error term, the LM117 was designed to minimize I_{ADJ} and make it relatively constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

To mitigate the requirement for an added load to sink the required output current, the resistor divider may be selected so that it alone can sink the largest specified output load current of 5 mA. This has the additional benefit of minimizing the I_{ADJ} error term (which varies over temperature).

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8.4 External Capacitors

An input bypass capacitor is recommended. A 0.1-μF ceramic disc or 1-μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will minimize the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10-μF bypass capacitor 80-dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device (see 节 8.6).

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1-μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01-μF disc may seem to work better than a 0.1-μF disc as a bypass.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1-μF solid tantalum (or 25-μF aluminum electrolytic) on the output swamps this effect and insures stability. Any increase of the load capacitance larger than 10 μF will merely improve the loop stability and output impedance.

8.5 Load Regulation

The LM117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240 Ω) should be tied directly to the output (case) of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15-V regulator with 0.05-Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05 Ω × I_L. If the set resistor is connected near the load the effective line resistance will be 0.05 Ω (1 + R2 / R1) or in this case, 11.5 times worse.

图 8-3 shows the effect of resistance between the regulator and 240-Ω set resistor.

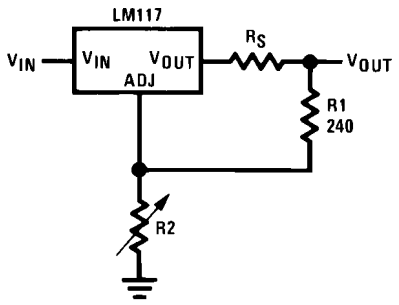


图 8-3. Regulator With Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-39 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

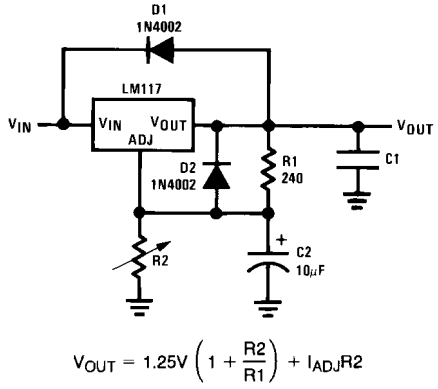
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8.6 Protection Diodes

When external capacitors are used with an IC regulator, it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10-μF capacitors have low enough internal series resistance to deliver 20-A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117, this discharge path is through a large junction that is able to sustain 15-A surge. This is not true of all types of positive regulators. For output capacitors of 25 μF or less, there is generally no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117 is a 50-Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25 V or less and 10-μF capacitance. 图 8-4 shows an LM117 with protection diodes included for use with outputs greater than 25 V and high values of output capacitance.



D1 protects against C1 (such as due to a VIN short)
D2 protects against C2 (such as due to a VOUT short)

图 8-4. Regulator With Protection Diodes

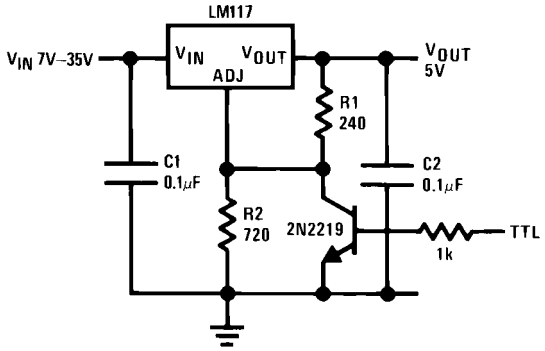
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9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Typical Applications



*Min. output ≅ 1.2 V

图 9-1. 5-V Logic Regulator With Electronic Shutdown*

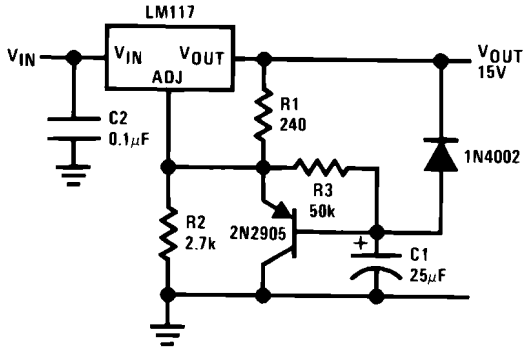
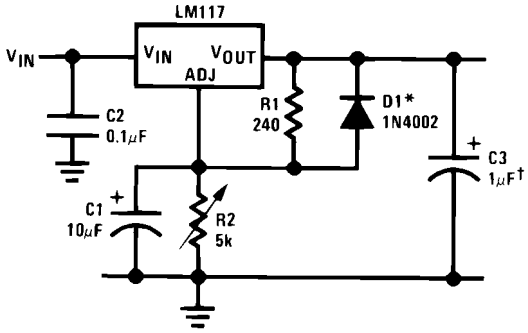


图 9-2. Slow Turn-On 15-V Regulator



†Solid tantalum

*Discharges C1 if output is shorted to ground

图 9-3. Adjustable Regulator With Improved Ripple Rejection

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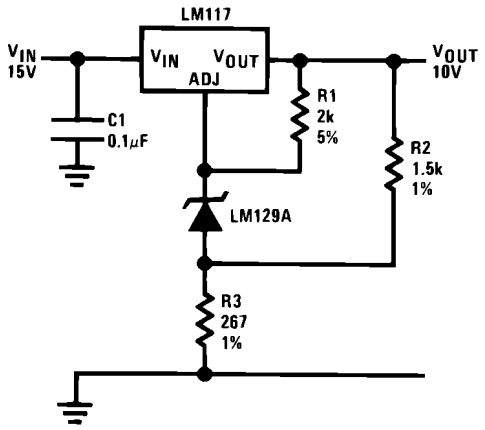
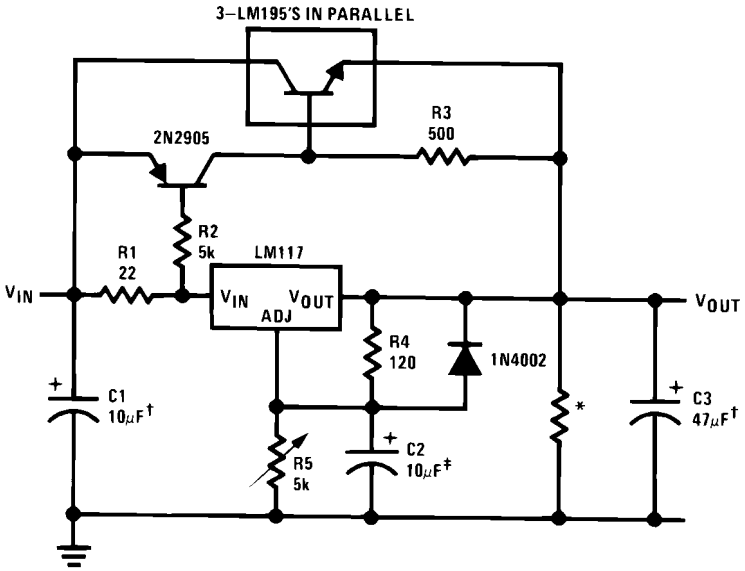


图 9-4. High Stability 10-V Regulator



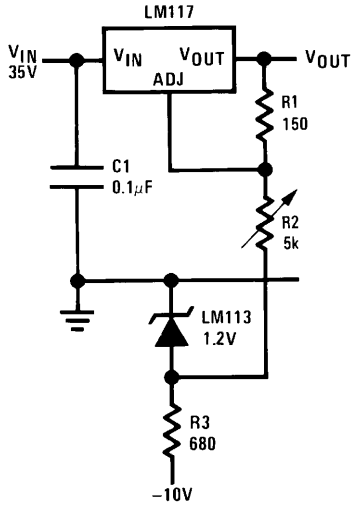
‡Optional, improves ripple rejection

†Solid tantalum

*Minimum load current = 30 mA

图 9-5. High Current Adjustable Regulator

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Full output current not available at high input-output voltages

图 9-6. 0-V to 30-V Regulator

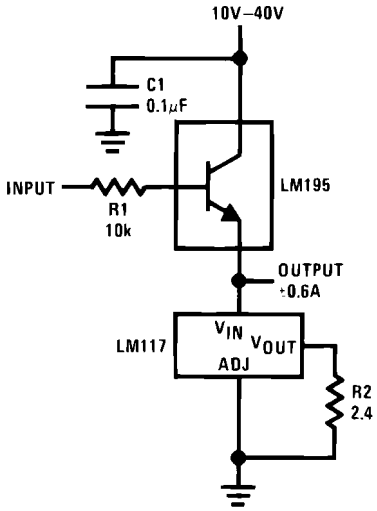
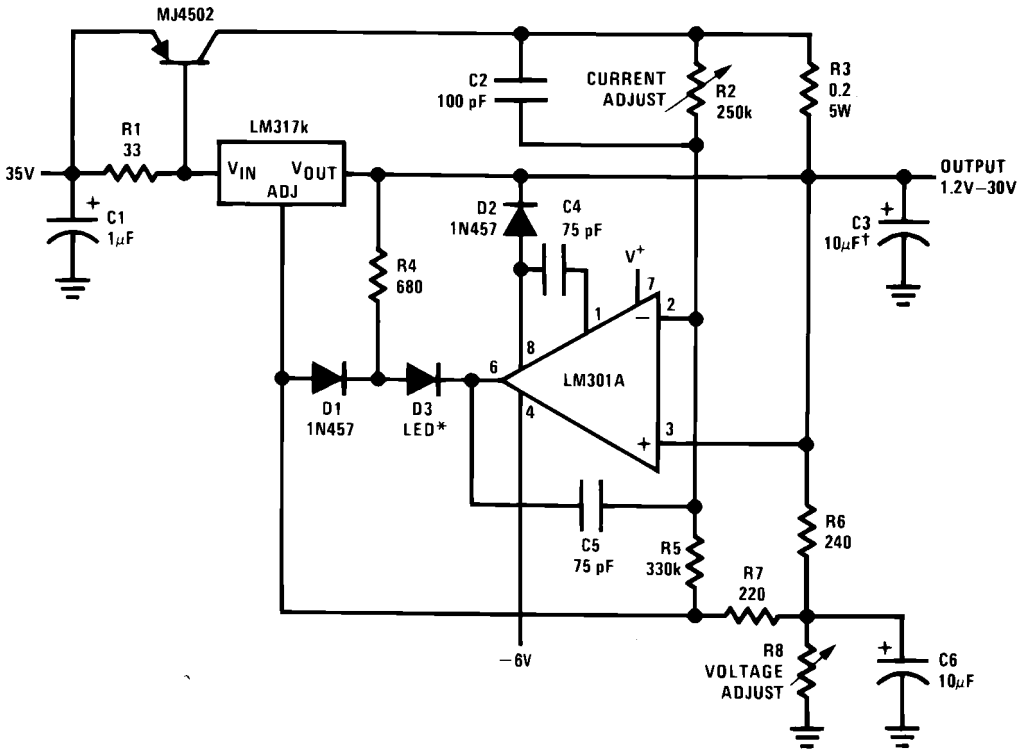


图 9-7. Power Follower



†Solid tantalum

*Lights in constant current mode

图 9-8. 5-A Constant Voltage/Constant Current Regulator

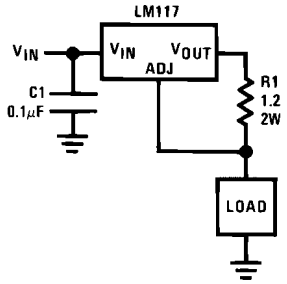
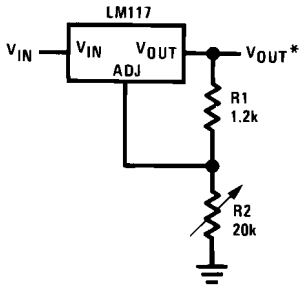


图 9-9. 1-A Current Regulator



*Specified load current requirement ≅ 5 mA

图 9-10. 1.2-V to 20-V Regulator With Minimum Program Current

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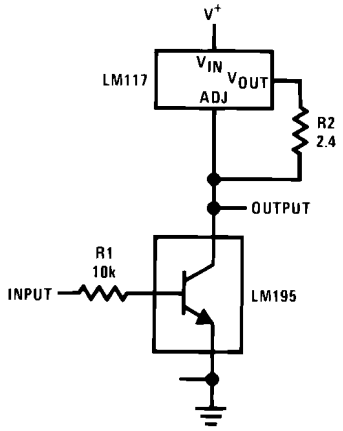
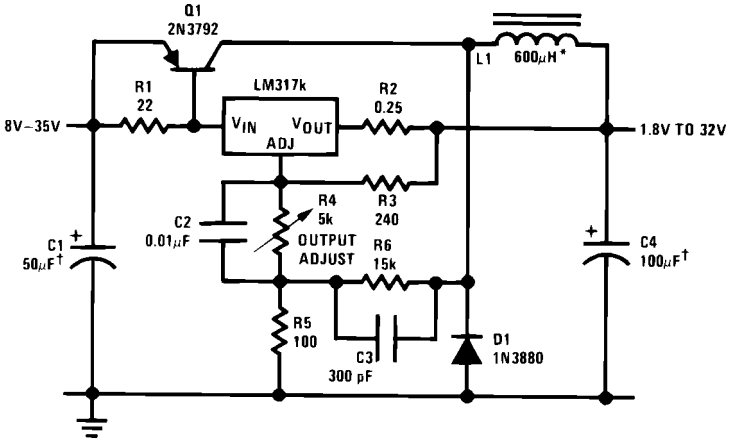


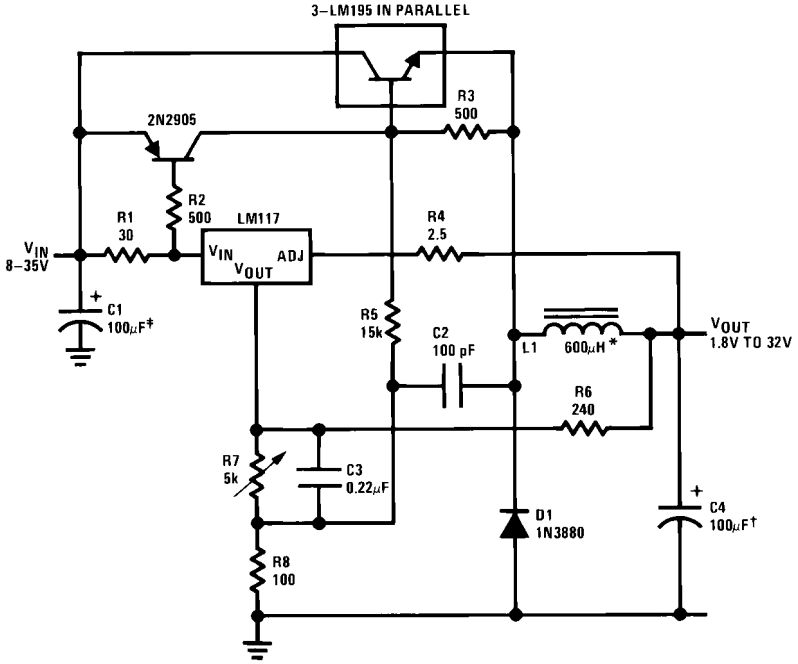
图 9-11. High Gain Amplifier



†Solid tantalum

*Core—Arnold A-254168-2 60 turns

图 9-12. Low Cost 3-A Switching Regulator



†Solid tantalum

*Core—Arnold A-254168-2 60 turns

图 9-13. 4-A Switching Regulator With Overload Protection

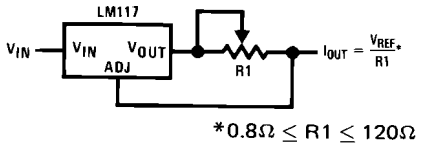


图 9-14. Precision Current Limiter

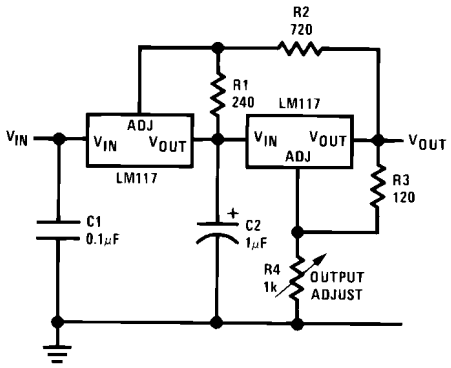
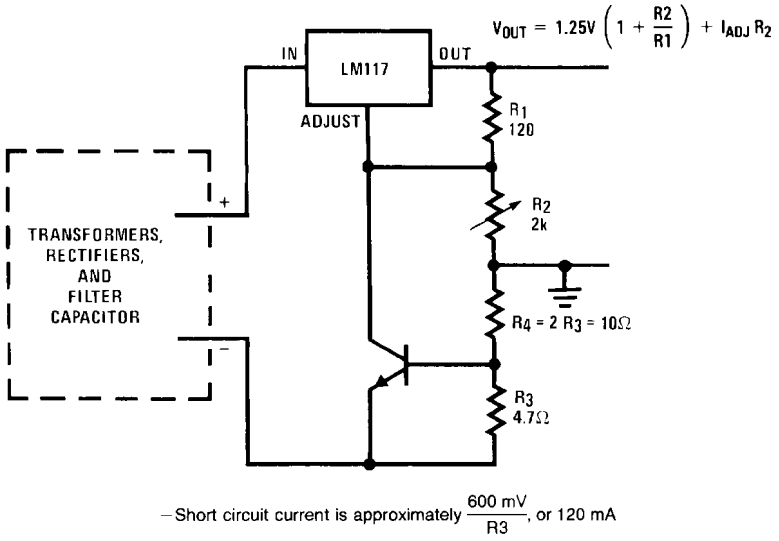


图 9-15. Tracking Preregulator

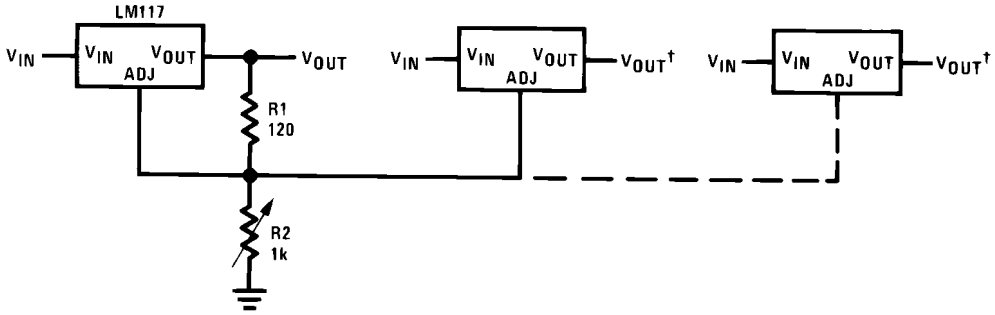
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(Compared to LM117's higher current limit)

—At 50 mA output only ¾ volt of drop occurs in R_3 and R_4

图 9-16. Current Limited Voltage Regulator



*All outputs within ±100 mV

†Minimum load = 10 mA

图 9-17. Adjusting Multiple On-Card Regulators With Single Control*

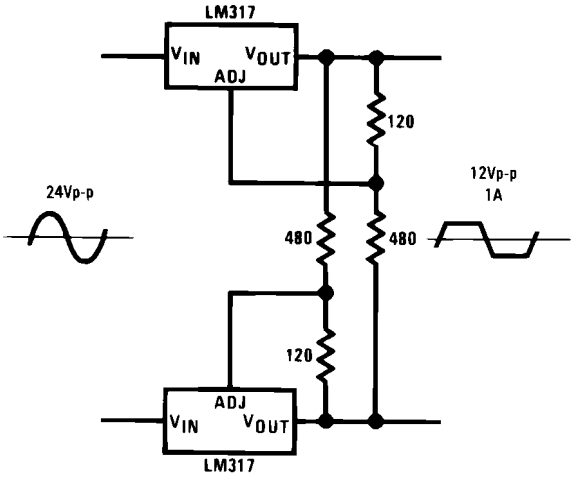
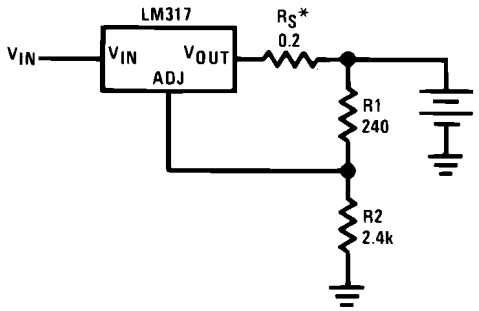


图 9-18. AC Voltage Regulator



*R_S—sets output impedance of charger: $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$

Use of R_S allows low charging rates with fully charged battery.

图 9-19. 12-V Battery Charger

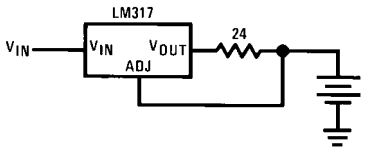


图 9-20. 50-mA Constant Current Battery Charger

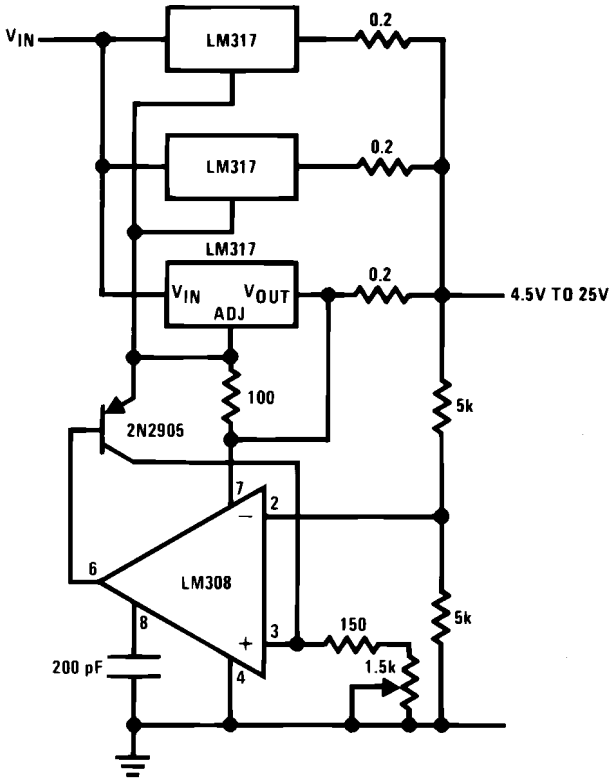
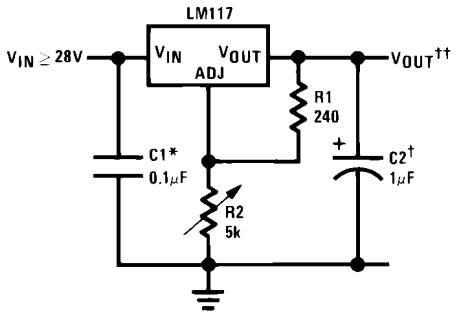


图 9-21. Adjustable 4-A Regulator

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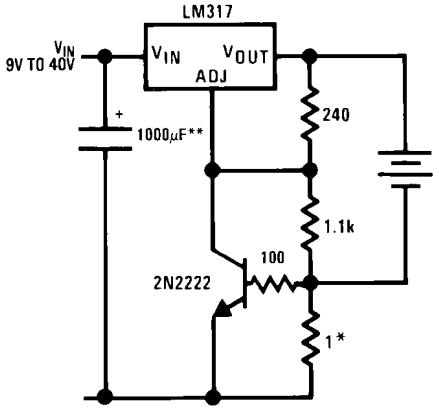
Full output current not available at high input-output voltages

*Needed if device is more than 6 in from filter capacitors.

†Optional, improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

$$\dagger\dagger V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$$

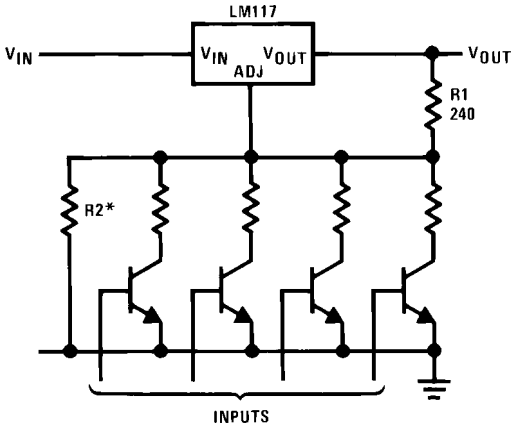
图 9-22. 1.2-V to 25-V Adjustable Regulator



*Sets peak current (0.6 A for 1 Ω)

**The 1000 μF is recommended to filter out input transients

图 9-23. Current Limited 6-V Charger



*Sets maximum V_{OUT}

图 9-24. Digitally Selected Outputs

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10 Power Supply Recommendations

The input supply to the LM117QML-SP must be kept at a voltage level such that its maximum input to output differential voltage is not exceeded. The minimum dropout voltage must also be met with extra headroom when possible to keep the LM117QML-SP in regulation. An input capacitor is recommended, especially when the input pin is located more than 6 in away from the power supply source. For more information regarding capacitor selection, refer to External Capacitors.

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11 Layout

11.1 Layout Guidelines

Ensure wide enough traces for those carrying the load current in order to reduce the amount of parasitic trace inductance. Keep the feedback loop from VOUT to ADJ as short as possible. To improve PSRR, a bypass capacitor can be placed at the ADJ pin and must be located as close as possible to the IC. In cases when VIN shorts to ground, an external diode must be placed from VOUT to VIN to divert the surge current from the output capacitor and protect the IC. Similarly, in cases when a large bypass capacitor is placed at the ADJ pin and VOUT shorts to ground, an external diode must be placed from ADJ to VOUT to provide a path for the bypass capacitor to discharge. These diodes must be placed close to the corresponding LM117QML-SP pins to increase their effectiveness.

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12 Device and Documentation Support

12.1 Device Support

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

1. LM117xRLQMLV ELDRS Report
2. LM117QML-SP SMD 5962R9951707VZA
3. High Reliability Part Numbering System
4. Applications for an Adjustable IC Power Regulator
5. Improving Power Supply Reliability with IC Power Regulators
6. A New Production Technique for Trimming Voltage Regulators
7. LDO basics: capacitor vs. capacitance
8. LDO Basics: Preventing reverse current

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TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R9951703V9A	Active	Production	DIESALE (Y) | 0	42 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
5962R9951703VXA	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-55 to 125	LM117HRQMLV 5962R9951703VXA Q ACO 5962R9951703VXA Q >T
5962R9951704VYA	Active	Production	TO (K) | 2	50 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM117KRQMLV 5962R99517 04VYA Q ACO 04VYA Q >T
5962R9951705V9A	Active	Production	DIESALE (Y) | 0	42 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
5962R9951705VXA	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-55 to 125	LM117HRLQMLV 5962R9951705VXA Q ACO 5962R9951705VXA Q >T
5962R9951706VZA	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM117GWR QMLV Q 5962R99517 06VZA ACO 06VZA >T
5962R9951707VZA	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM117GWRL QMLV Q 5962R99517 07VZA ACO 07VZA >T
LM117GWRLQMLV	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM117GWRL QMLV Q 5962R99517 07VZA ACO 07VZA >T
LM117GWRQMLV	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM117GWR QMLV Q 5962R99517 06VZA ACO 06VZA >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM117GWRQMLV.A	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM117GWR QMLV Q 5962R99517 06VZA ACO 06VZA >T
LM117H MDE	Active	Production	DIESALE (Y) | 0	42 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM117H MDR	Active	Production	DIESALE (Y) | 0	42 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM117H-MDR.A	Active	Production	DIESALE (Y) | 0	42 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM117HRLQMLV	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM117HRLQMLV 5962R9951705VXA Q ACO 5962R9951705VXA Q >T
LM117HRQMLV	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM117HRQMLV 5962R9951703VXA Q ACO 5962R9951703VXA Q >T
LM117HRQMLV.A	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-55 to 125	LM117HRQMLV 5962R9951703VXA Q ACO 5962R9951703VXA Q >T
LM117K/EM	Active	Production	TO (K) | 2	50 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	25 to 25	LM117K/EM EVAL ONLY T
LM117KRQMLV	Active	Production	TO (K) | 2	50 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM117KRQMLV 5962R99517 04VYA Q ACO 04VYA Q >T
LM117KRQMLV.A	Active	Production	TO (K) | 2	50 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM117KRQMLV 5962R99517 04VYA Q ACO 04VYA Q >T
LM117NDT/EM	Active	Production	TO (NDT) | 3	20 | JEDEC TRAY (5+1)	-	Call TI	Call TI	25 to 25	LM117NDT/EM EVAL ONLY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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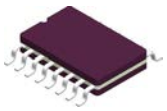
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM117QML-SP :

- Military : LM117QML

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

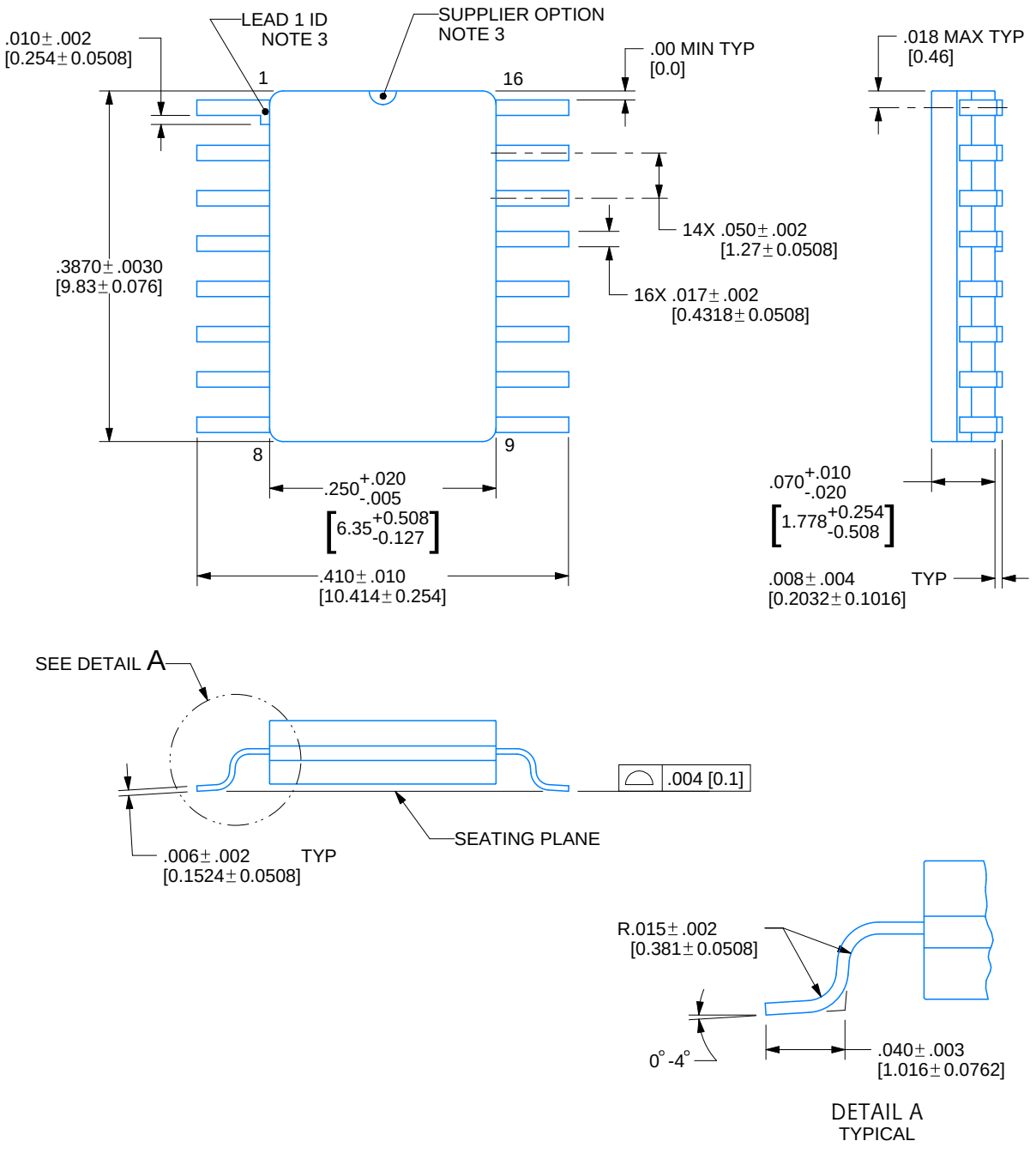


PACKAGE OUTLINE

NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



4215198/C 08/2022

NOTES:

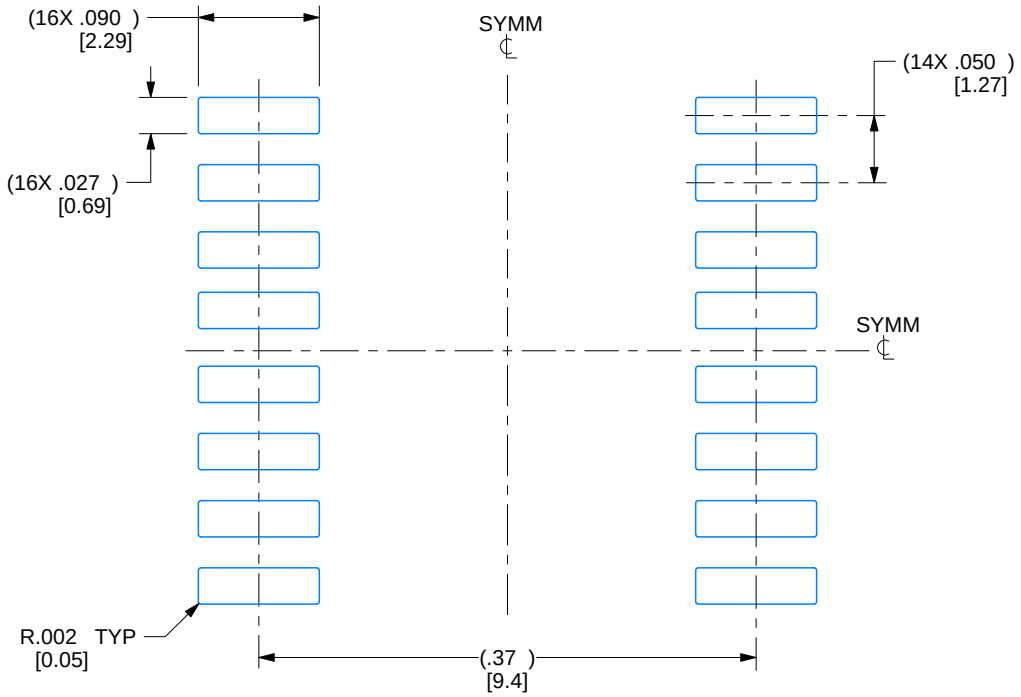
1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

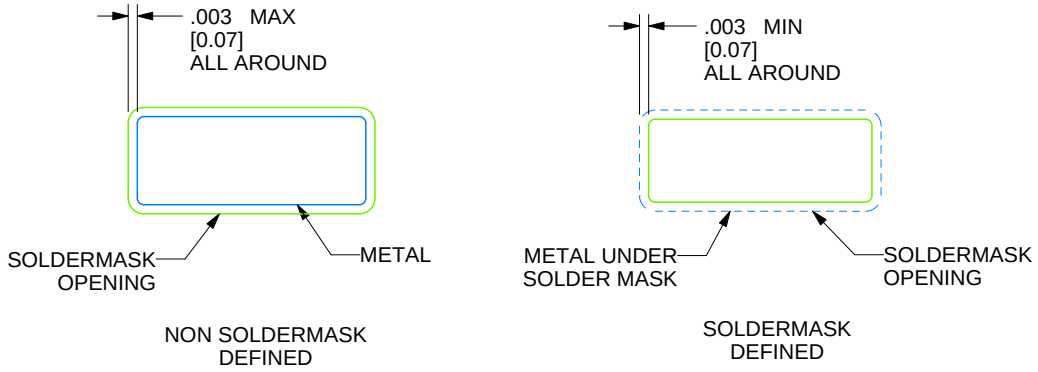
NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



RECOMMENDED LAND PATTERN

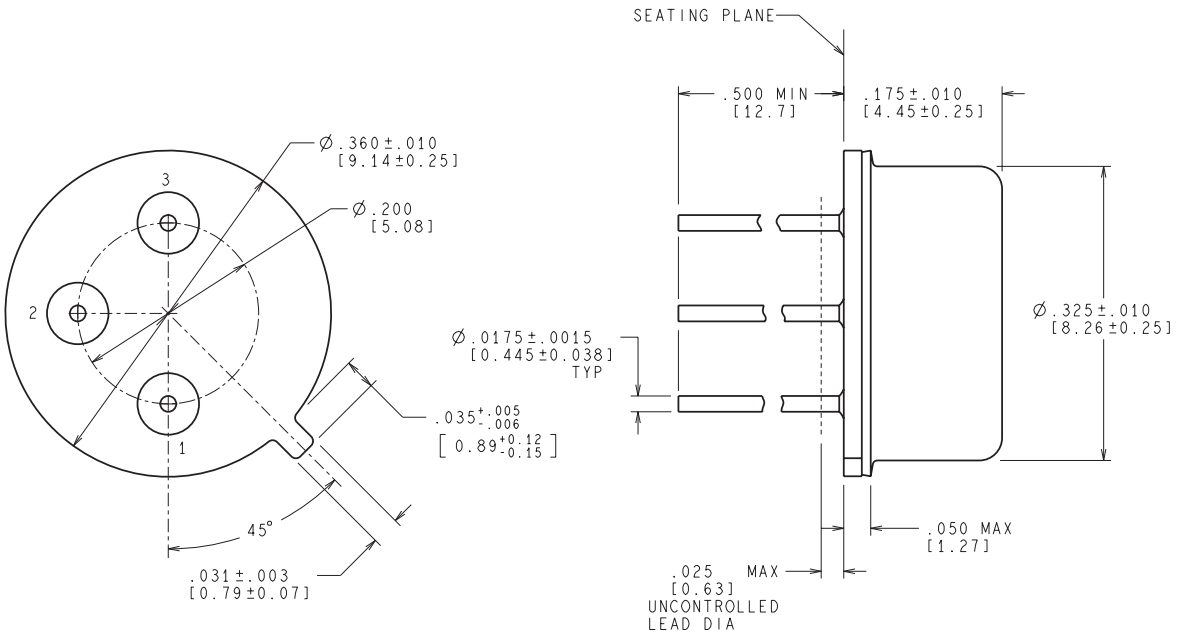


4215198/C 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197879	12/30/2021	TINA TRAN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198832	02/15/2022	K. SINCERBOX
C	.387± .003 WAS .39000± .00012;	2200917	08/08/2022	D. CHIN / K. SINCERBOX

NDT0003A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

H03A (Rev D)

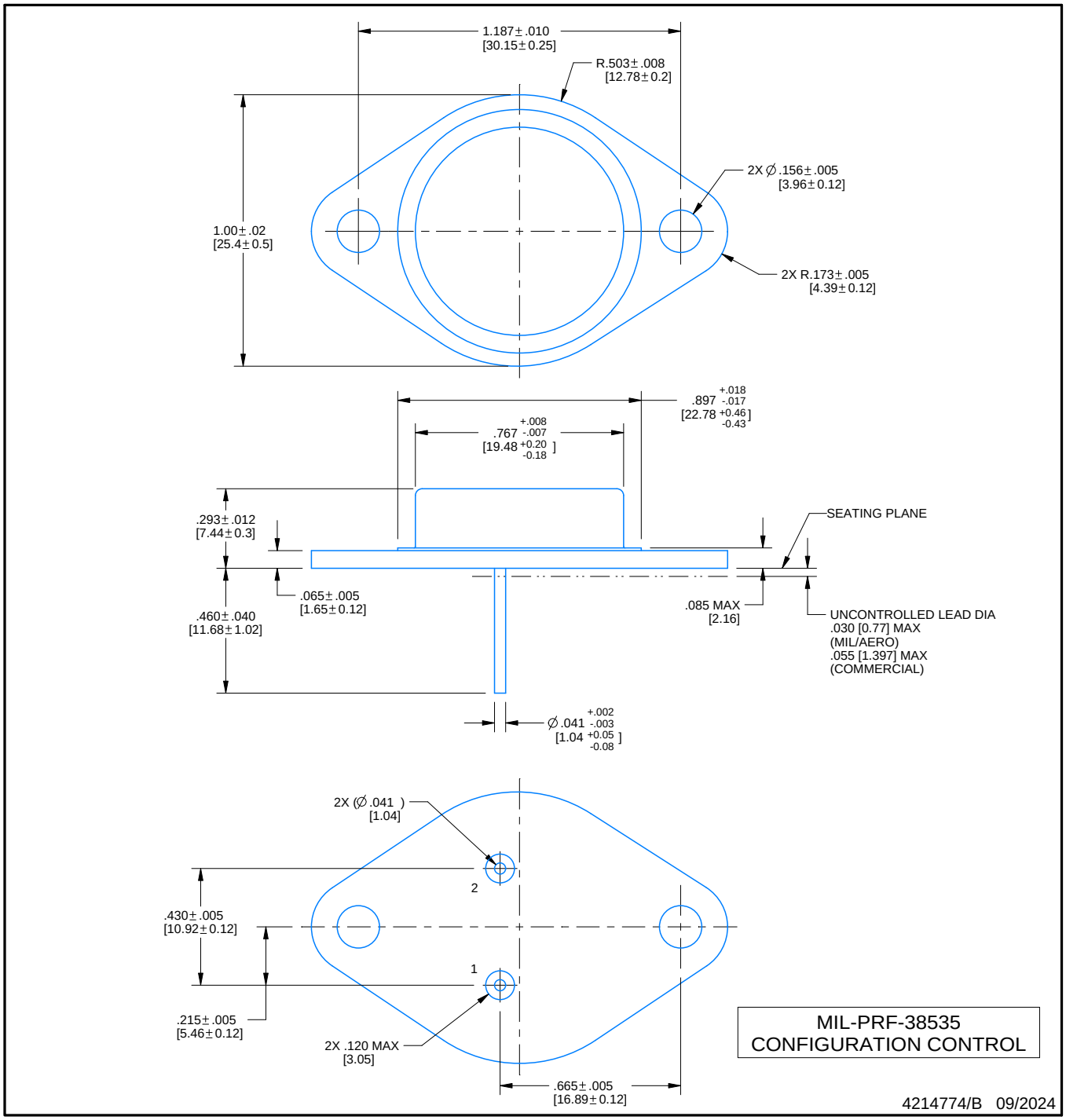
K0002A



PACKAGE OUTLINE

TO-CAN - 7.747 mm max height

TRANSISTOR OUTLINE



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Leads not to be bent greater than 15°.

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最后更新日期：2025 年 10 月