ISO733x-Q1 耐用 EMC 低功耗三通道数字隔离器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件人体模型 (HBM) 分类等级 3A
  - 器件充电器件模型 (CDM) 分类等级 C6
- 信号传输速率：25Mbps
- 输入时使用集成噪声滤波器
- 默认输出*高电平*和*低电平*选项
- 低功耗：每通道的 I_{CC} 典型值（1Mbps 时）：
  - ISO7330-Q1：1mA（5V 电源），0.8mA（3.3V 电源）
  - ISO7331-Q1：1.4mA（5V 电源），1mA（3.3V 电源）
- 低传播延迟：典型值 32ns（5V 电源）
- 可由 3.3V 和 5V 电源供电
- 3.3V 和 5V 电平转换
- 70kV/μs 瞬态抗扰度，典型值（5V 电源）
- 优异的电磁兼容性 (EMC)
  - 系统级静电放电 (ESD)、瞬态放电 (EFT) 以及抗浪涌保护
  - 低辐射
- 宽体小外形尺寸集成电路 (SOIC)-16 封装
- 隔离隔栅寿命：> 25 年
- 安全及管理批准：
  - 符合 DIN V VDE V 0884-10 和 DIN EN 61010-1 标准的 4242 V_{PK} 隔离部分）
  - 符合 UL 1577 标准且长达 1 分钟的 3000 V_{RMS} 隔离
  - CSA 组件验收通知 5A，IEC 60950-1 和 IEC 61010-1 终端设备标准
  - 已通过符合 GB4943.1-2011 的 CQC 认证

2 应用

- 在下列使用中的光电耦合器替代产品：
  - 工业用 FieldBus
    - ProfiBus
    - ModBus
    - DeviceNet™ 数据总线
  - 伺服控制接口
  - 电机控制
  - 电源
  - 电池组

3 说明

ISO733x-Q1 系列器件可提供符合 UL 1577 标准的长达 1 分钟且高达 3000 V_{RMS} 的电流隔离，以及符合 VDE V 0884-10 标准的 4242 V_{PK} 隔离。 这些器件具有三个隔离通道，其逻辑输入和输出缓冲器由二氧化硅 (SiO_2) 绝缘隔栅分离开来。

ISO7330-Q1 具有三个同向通道，而 ISO7331-Q1 具有两个正向通道和一个反向通道。 如果出现输入功率或信号损失，默认输出低电平（器件的订购部件号带有后缀 *F*）或高电平（器件的订购部件号不带后缀 *F*）。更多详细信息，请参见 *Device Functional Modes* 部分。

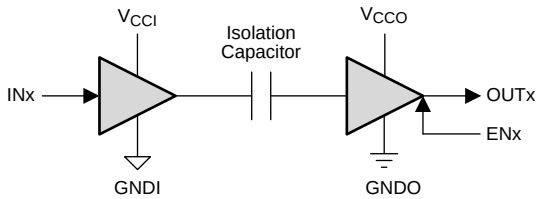
与隔离式电源一起使用时，这些器件有助于防止数据总线或者其他电路上的噪声电流进入本地接地或对敏感电路造成干扰或损坏。 ISO733x-Q1 系列器件已针对恶劣工业环境集成了噪声滤波器。在此类环境下，器件的输入引脚上可能会出现短噪声脉冲。 ISO733x-Q1 系列器件具有晶体管-晶体管逻辑电路 (TTL) 输入阈值，工作电压范围为 3V 到 5.5V。 凭借创新的芯片设计和布线技术，ISO733x-Q1 系列器件的电磁兼容性得到了显著增强，可确保提供系统级 ESD、EFT 和浪涌保护并符合辐射标准。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ISO7330-Q1	SOIC (16)	10.30mm x 7.50mm
ISO7331-Q1		

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



V_{CCI} 和 GNDI 分别是输入通道的电源和接地连接。

V_{CCO} 和 GNDO 分别是输出的电源和接地连接。

目录

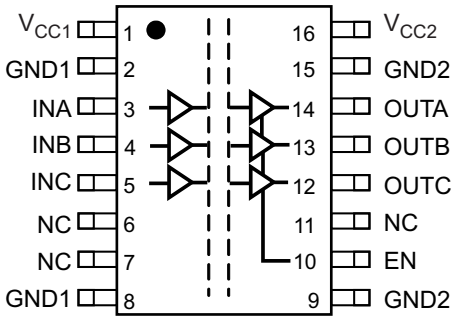
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

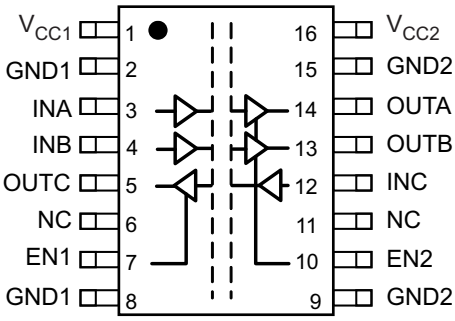
日期	修订版本	注释
2015 年 11 月	*	最初发布。

5 Pin Configuration and Functions

ISO7330-Q1 DW Package
16-Pin SOIC
Top View



ISO7331-Q1 DW Package
16-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	ISO7330-Q1	ISO7331-Q1		
EN	10	—	I	Output enable. OUTA, OUTB, and OUTC are enabled when EN is high or disconnected and disabled when EN is low.
EN1	—	7	I	Output enable 1. OUTC is enabled when EN1 is high or disconnected and disabled when EN1 is low.
EN2	—	10	I	Output enable 2. OUTA and OUTB are enabled when EN2 is high or disconnected and disabled when EN2 is low.
GND1	2	2	—	Ground connection for V_{CC1}
	8	8		
GND2	9	9	—	Ground connection for V_{CC2}
	15	15		
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	12	I	Input, channel C
NC	6	6	—	No Connect. These pins have no internal connection.
	7			
	11	11		
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	5	O	Output, channel C
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	V_{CC1} , V_{CC2}	–0.5	6	V
	Voltage (2)	INx, OUTx, ENx	–0.5	V_{CC}+0.5(3)	V
I_O	Output current			±15	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration	40			ns
1 / t_{ui}	Signaling rate	0		25	Mbps
T_J	Junction temperature(1)			136	°C
T_A	Ambient temperature	–40	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see the *Thermal Information* table.

6.4 Thermal Information

THERMAL METRIC(1)		ISO733x-Q1 DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	40.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics—5-V Supply

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 11	V_{CCO} (1) – 0.5	4.7		V
		I_{OH} = –20 µA; see Figure 11	V_{CCO} (1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 11		0.2	0.4	V
		I_{OL} = 20 µA; see Figure 11		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			480		mV
I_{IH}	High-level input current	IN = V_{CC}			10	µA
I_{IL}	Low-level input current	IN = 0 V	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 14.	25	70		kV/µs

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2}, for the output channel being measured.

6.6 Supply Current Characteristics—5-V Supply

All inputs switching with square wave clock signal for dynamic I_{CC} measurement. V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7330-Q1							
Supply current for V_{CC1} and V_{CC2}	Disable	V_I = V_{CC} or 0 V, EN = 0 V	I_{CC1}		0.5	1.1	mA
			I_{CC2}		0.4	0.9	
	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15 pF	I_{CC1}		0.5	1.1	
			I_{CC2}		2.6	4.2	
	10 Mbps	C_L = 15 pF	I_{CC1}		1.1	1.9	
			I_{CC2}		4.3	6	
	25 Mbps	C_L = 15 pF	I_{CC1}		2.1	3.3	
			I_{CC2}		7	9.3	
ISO7331-Q1							
Supply current for V_{CC1} and V_{CC2}	Disable	V_I = V_{CC} or 0 V, EN1 = EN2 = 0 V	I_{CC1}		0.7	1.6	mA
			I_{CC2}		0.7	1.3	
	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15 pF	I_{CC1}		1.8	3	
			I_{CC2}		2.4	3.6	
	10 Mbps	C_L = 15 pF	I_{CC1}		2.8	4.1	
			I_{CC2}		3.8	5.1	
	25 Mbps	C_L = 15 pF	I_{CC1}		4.3	6.2	
			I_{CC2}		5.8	7.8	

6.7 Electrical Characteristics—3.3-V Supply

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 11	V_{CCO} (1) – 0.5	3		V
		I_{OH} = –20 µA; see Figure 11	V_{CCO} (1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 11		0.2	0.4	V
		I_{OL} = 20 µA; see Figure 11		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			425		mV
I_{IH}	High-level input current	IN = V_{CC}			10	µA
I_{IL}	Low-level input curre	IN = 0 V	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 14	25	50		kV/µs

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2}, for the output channel being measured.

6.8 Supply Current Characteristics—3.3-V Supply

All inputs switching with square wave clock signal for dynamic I_{CC} measurement. V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7330-Q1							
Supply current for V_{CC1} and V_{CC2}	Disable	V_I = V_{CC} or 0 V, EN = 0 V	I_{CC1}		0.3	0.6	mA
			I_{CC2}		0.3	0.6	
	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15 pF	I_{CC1}		0.3	0.6	
			I_{CC2}		2	3.1	
	10 Mbps	C_L = 15 pF	I_{CC1}		0.7	1.1	
			I_{CC2}		3.1	4.3	
	25 Mbps	C_L = 15 pF	I_{CC1}		1.2	2	
			I_{CC2}		4.8	6.3	
ISO7331-Q1							
Supply current for V_{CC1} and V_{CC2}	Disable	V_I = V_{CC} or 0 V, EN = 0 V	I_{CC1}		0.5	0.9	mA
			I_{CC2}		0.5	0.8	
	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15 pF	I_{CC1}		1.3	2.1	
			I_{CC2}		1.7	2.6	
	10 Mbps	C_L = 15 pF	I_{CC1}		1.9	2.7	
			I_{CC2}		2.6	3.5	
	25 Mbps	C_L = 15 pF	I_{CC1}		2.9	4.2	
			I_{CC2}		3.9	5.2	

6.9 Power Dissipation Characteristics

V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 12.5-MHz 50% duty cycle square wave (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum Power Dissipation by ISO7330-Q1				70	mW
P_{D1}	Maximum Power Dissipation by Side-1 of ISO7330-Q1				20	mW
P_{D2}	Maximum Power Dissipation by Side-2 of ISO7330-Q1				50	mW
P_D	Maximum Power Dissipation by ISO7331-Q1				84	mW
P_{D1}	Maximum Power Dissipation by Side-1 of ISO7331-Q1				35	mW
P_{D2}	Maximum Power Dissipation by Side-2 of ISO7331-Q1				49	mW

6.10 Switching Characteristics—5-V Supply

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 11	20	32	58	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$		See Figure 11			4	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time		Same direction channels			2.5	ns
			Opposite direction channels			17	
$t_{sk(pp)}$(3)	Part-to-part skew time					23	ns
t_r	Output signal rise time		See Figure 11		3		ns
t_f	Output signal fall time		See Figure 11		2		ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output		See Figure 12		7	12	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output		See Figure 12		7	12	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	ISO733xCQDWQ1 and ISO733xCQDWRQ1	See Figure 12		7	12	ns
		ISO733xFCQDWQ1 and ISO733xFCQDWRQ1			11000	23000(4)	
t_{PZL}	Enable propagation delay, high impedance-to-low output	ISO733xCQDWQ1 and ISO733xCQDWRQ1	See Figure 12		11000	23000(4)	ns
		ISO733xFCQDWQ1 and ISO733xFCQDWRQ1			7	12	
t_{fs}	Fail-safe output delay time from input power loss		See Figure 13		7		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate should be ≤ 43 Kbps

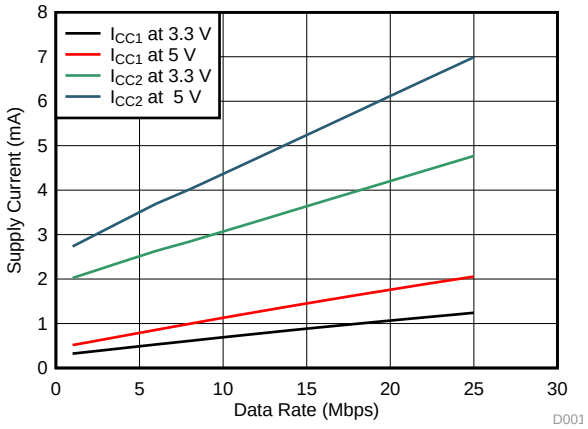
6.11 Switching Characteristics—3.3-V Supply

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 11	22	36	66	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$		See Figure 11			2.5	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time		Same direction channels			3	ns
			Opposite direction channels			16	
$t_{sk(pp)}$(3)	Part-to-part skew time					27	ns
t_r	Output signal rise time		See Figure 11		3		ns
t_f	Output signal fall time		See Figure 11		2		ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output		See Figure 12		9	18	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output		See Figure 12		9	18	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	ISO733xCQDWQ1 and ISO733xCQDWRQ1	See Figure 12		9	18	ns
		ISO733xFCQDWQ1 and ISO733xFCQDWRQ1			13000	24000(4)	
t_{PZL}	Enable propagation delay, high impedance-to-low output	ISO733xCQDWQ1 and ISO733xCQDWRQ1	See Figure 12		13000	24000(4)	ns
		ISO733xFCQDWQ1 and ISO733xFCQDWRQ1			9	18	
t_{fs}	Fail-safe output delay time from input power loss		See Figure 13		7		µs

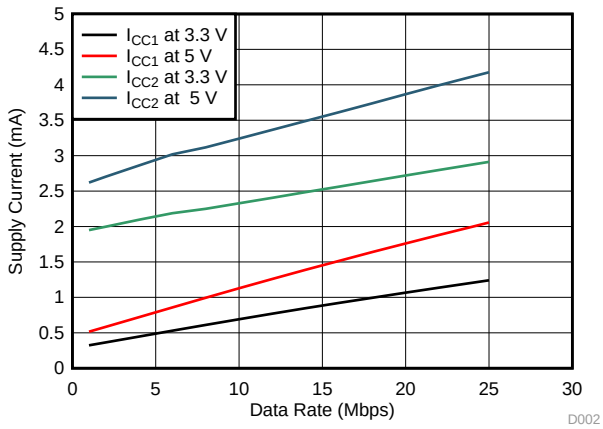
(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate should be ≤ 41 Kbps

6.12 Typical Characteristics



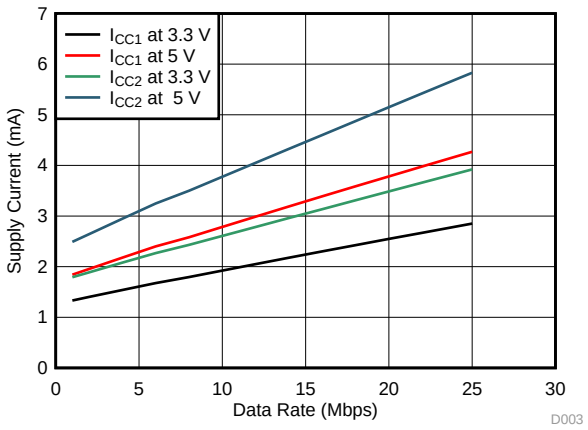
T_A = 25°C C_L = 15 pF

Figure 1. ISO7330-Q1 Supply Current vs Data Rate (With 15-pF Load)



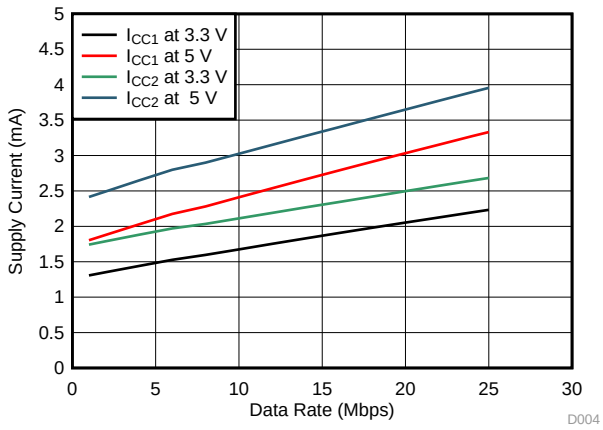
T_A = 25°C C_L = No Load

Figure 2. ISO7330-Q1 Supply Current vs Data Rate (With No Load)



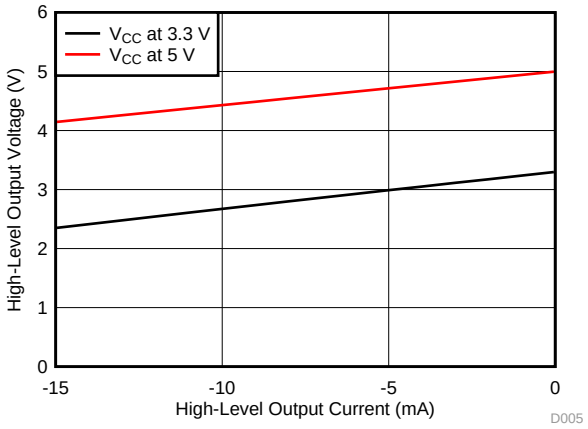
T_A = 25°C C_L = 15 pF

Figure 3. ISO7331-Q1 Supply Current vs Data Rate (With 15-pF Load)



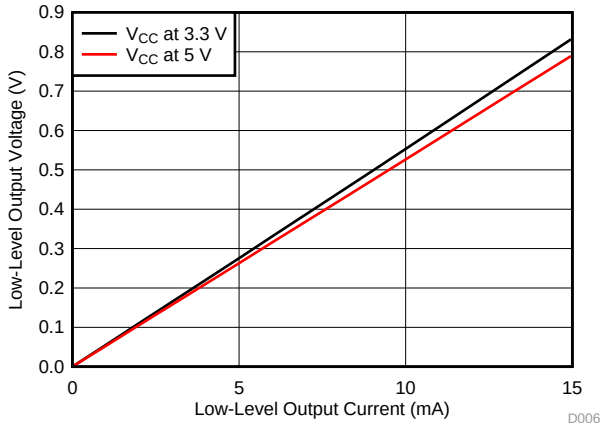
T_A = 25°C C_L = No Load

Figure 4. ISO7331-Q1 Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 5. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

Figure 6. Low-Level Output Voltage vs Low-Level Output Current

Typical Characteristics (continued)

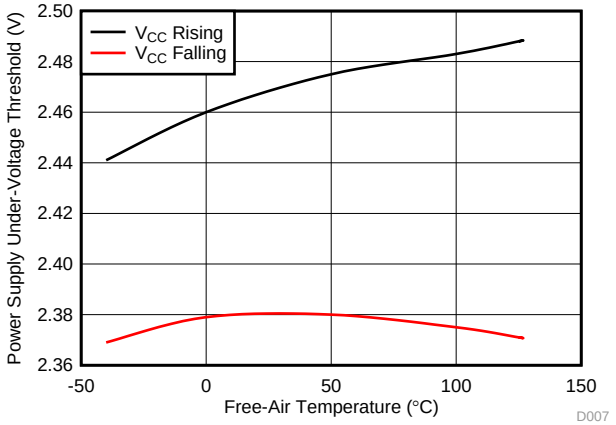


Figure 7. Power Supply Undervoltage Threshold vs Free-Air Temperature

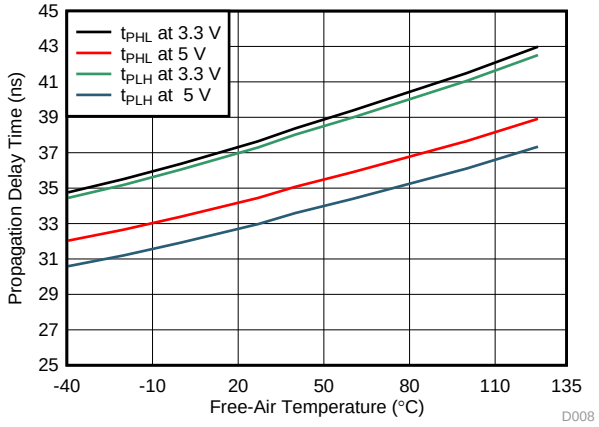


Figure 8. Propagation Delay Time vs Free-Air Temperature

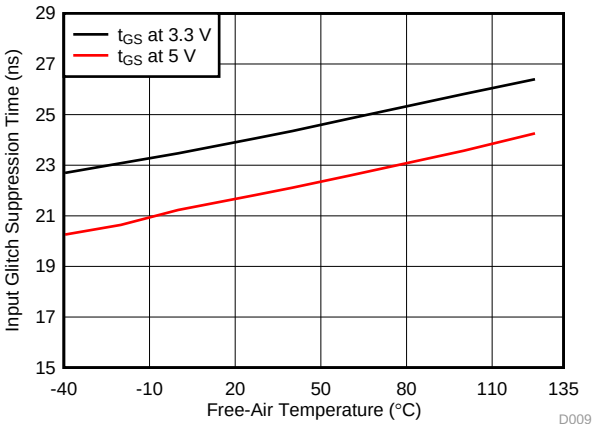


Figure 9. Input Glitch Suppression Time vs Free-Air Temperature

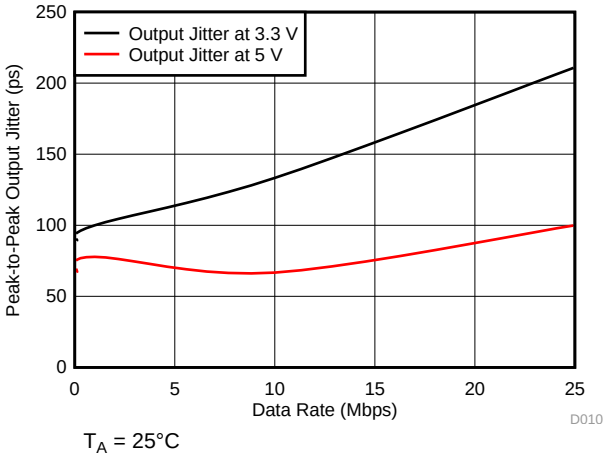
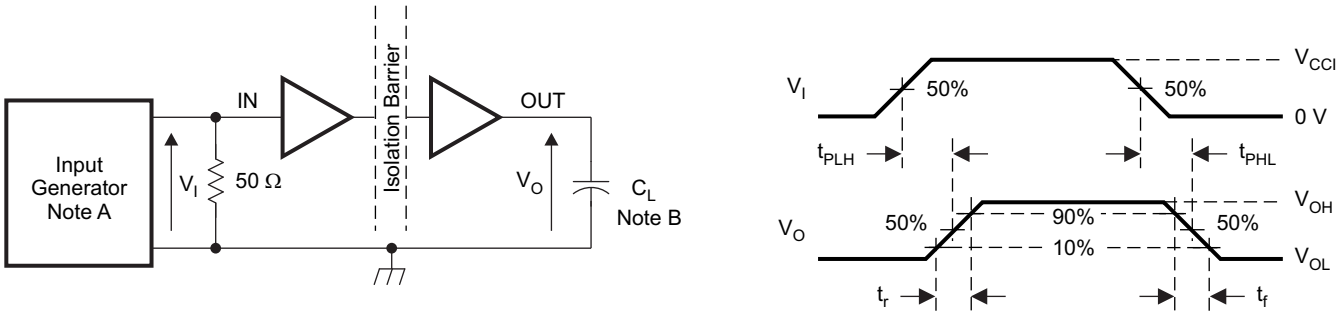


Figure 10. Output Jitter vs Data Rate

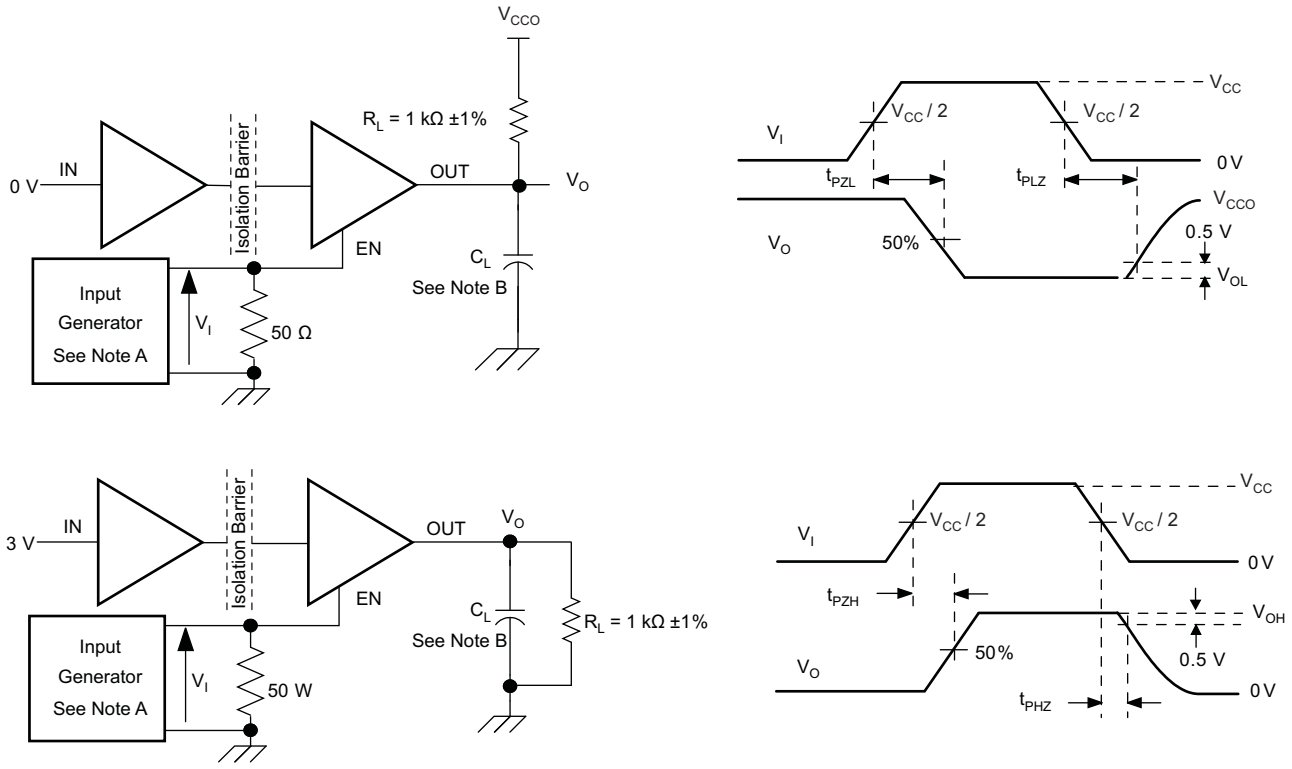
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 11. Switching Characteristic Test Circuit and Voltage Waveforms

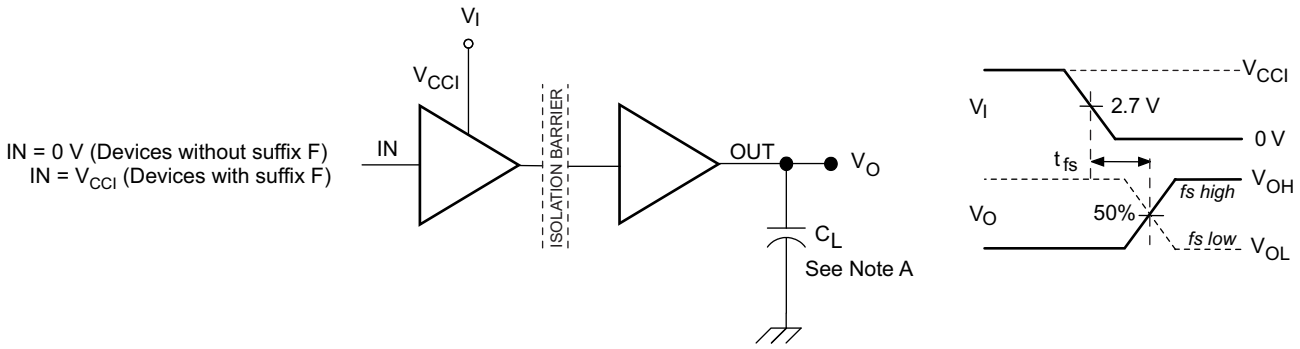


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

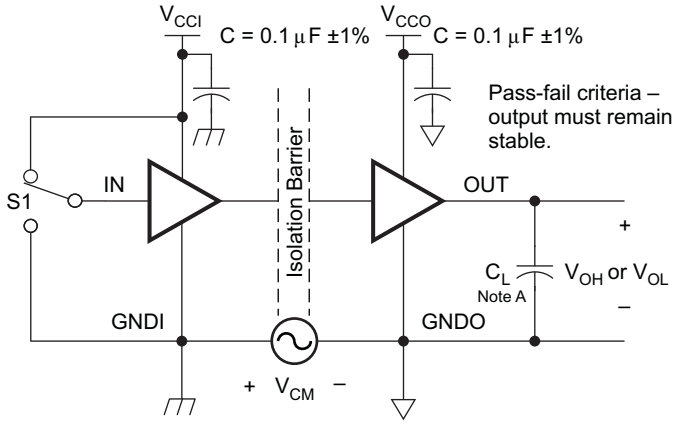
Figure 12. Enable and Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 14. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in Figure 15 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency (HF) channel with a bandwidth from 100 kbps up to 25 Mbps, and a low-frequency (LF) channel covering the range from 100 kbps down to DC.

In principle, a single-ended input signal entering the HF channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transient pulses, which then are converted into CMOS levels by a comparator. The transient pulses at the input of the comparator can be either above or below the common mode voltage V_{REF} depending on whether the input bit transitioned from 0 to 1 or 1 to 0. The comparator threshold is adjusted based on the expected bit transition. A decision logic (DCL) at the output of the HF channel comparator measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

8.2 Functional Block Diagram

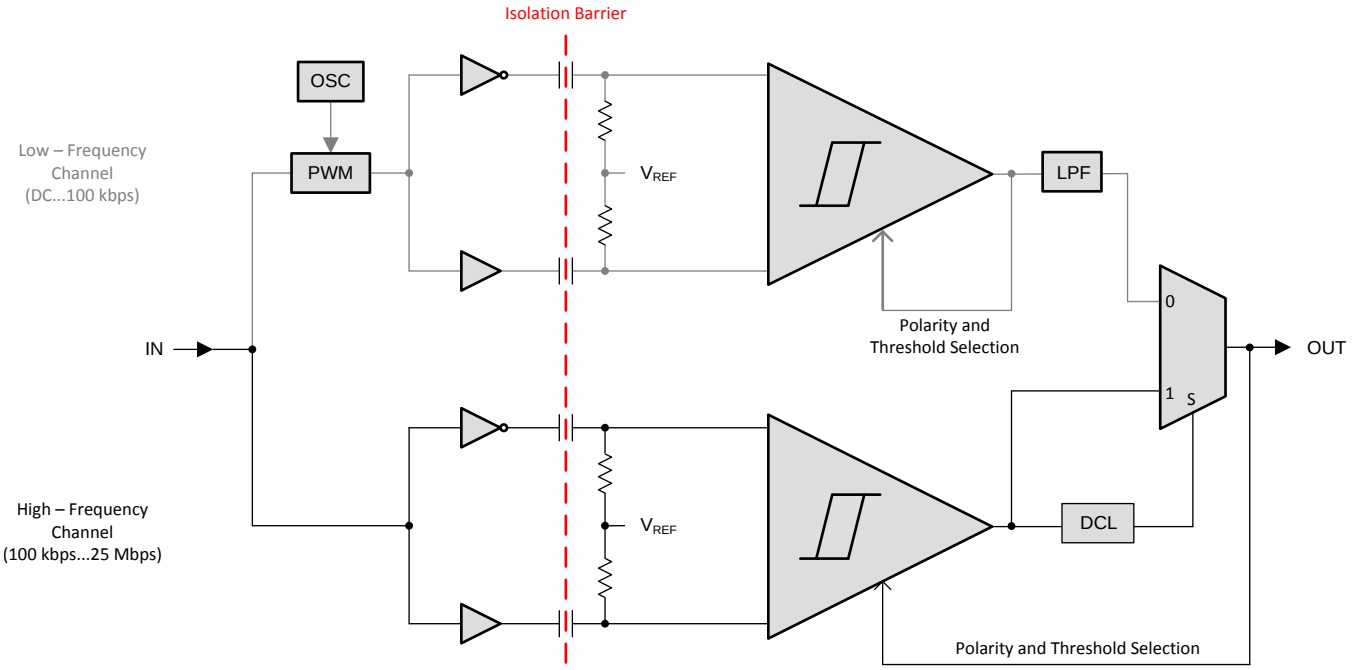


Figure 15. Conceptual Block Diagram of a Digital Capacitive Isolator

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.3 Feature Description

ORDERABLE DEVICE	CHANNEL DIRECTION	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
ISO7330CQDWQ1 and ISO7330CQDWRQ1	3 Forward, 0 Reverse	3000 V_{RMS} / 4242 V_{PK} (1)	25 Mbps	High
ISO7330FCQDWQ1 and ISO7330FCQDWRQ1				Low
ISO7331CQDWQ1 and ISO7331CQDWRQ1	2 Forward, 1 Reverse			High
ISO7331FCQDWQ1 and ISO7331FCQDWRQ1				Low

(1) See the *Regulatory Information* section for detailed Isolation Ratings

8.3.1 High Voltage Feature Description

8.3.1.1 Package Insulation Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	8			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	8			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	>400			V
DTI	Minimum internal gap (internal clearance)	Distance through the insulation	13			µm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C		>10^{12}		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		>10^{11}		Ω
C_{IO}	Isolation capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		2		pF
C_I	Input capacitance(2)	V_I = V_{CC}/2 + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.1.2 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOWM}	Maximum isolation working voltage		1000	V_{RMS}
V_{IORM}	Maximum repetitive peak voltage per DIN V VDE V 0884-10		1414	V_{PK}
V_{PR}	Input-to-output test voltage per DIN V VDE V 0884-10	After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	1697	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, Partial Discharge < 5 pC	2262	
		Method b1, $V_{PR} = V_{IORM} \times 1.875$, t = 1 s (100% Production test) Partial discharge < 5 pC	2651	
V_{IOTM}	Maximum transient overvoltage per DIN V VDE V 0884-10	$V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t= 1 sec (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage per DIN V VDE V 0884-10	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 7800\ V_{PK}$ (qualification)	6000	V_{PK}
V_{ISO}	Withstand isolation voltage per UL 1577	$V_{TEST} = V_{ISO} = 3000\ V_{RMS}$, t = 60 sec (qualification) $V_{TEST} = 1.2 \times V_{ISO} = 3600\ V_{RMS}$, t = 1 sec (100% production)	3000	V_{RMS}
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 300 V_{RMS}	I–IV
	Rated mains voltage ≤ 600 V_{RMS}	I–III
	Rated mains voltage ≤ 1000 V_{RMS}	I–II

8.3.1.3 Regulatory Information

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Planned to be certified according to GB4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK} ; Maximum Surge Isolation Voltage, 6000 V_{PK}; Maximum Repetitive Peak Isolation Voltage', 1414 V_{PK}	800 V_{RMS} Basic Insulation and 400 V_{RMS} Reinforced Insulation working voltage per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2; 300 V_{RMS} Basic Insulation working voltage per CSA 61010-1-12 and IEC 61010-1 3rd Ed.	Single protection, 3000 V_{RMS} (1)	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certification planned

(1) Production tested ≥ 3600 V_{RMS} for 1 second in accordance with UL 1577.

8.3.1.4 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 78.3 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			290	mA
		$R_{\theta JA}$ = 78.3 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			443	
T_S	Maximum safety temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

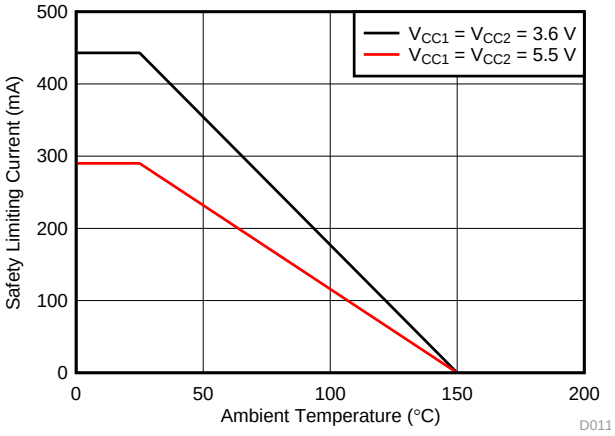


Figure 16. Thermal Derating Curve per VDE

8.4 Device Functional Modes

Table 2 lists the functional modes for the ISO733x-Q1 family of devices.

Table 2. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	
				ISO733xCQDWQ1 AND ISO733xCQDWRQ1	ISO733xFCQDWQ1 AND ISO733xFCQDWRQ1
PU	PU	H	H or Open	H	H
		L	H or Open	L	L
		X	L	Z	Z
		Open	H or Open	H(2)	L(3)
PD	PU	X	H or Open	H(2)	L(3)
X	PU	X	L	Z	Z
X	PD	X	X	Undetermined	Undetermined

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level; Open = Not connected
(2) In fail-safe condition, output defaults to high level
(3) In fail-safe condition, output defaults to low level

8.4.1 Device I/O Schematics

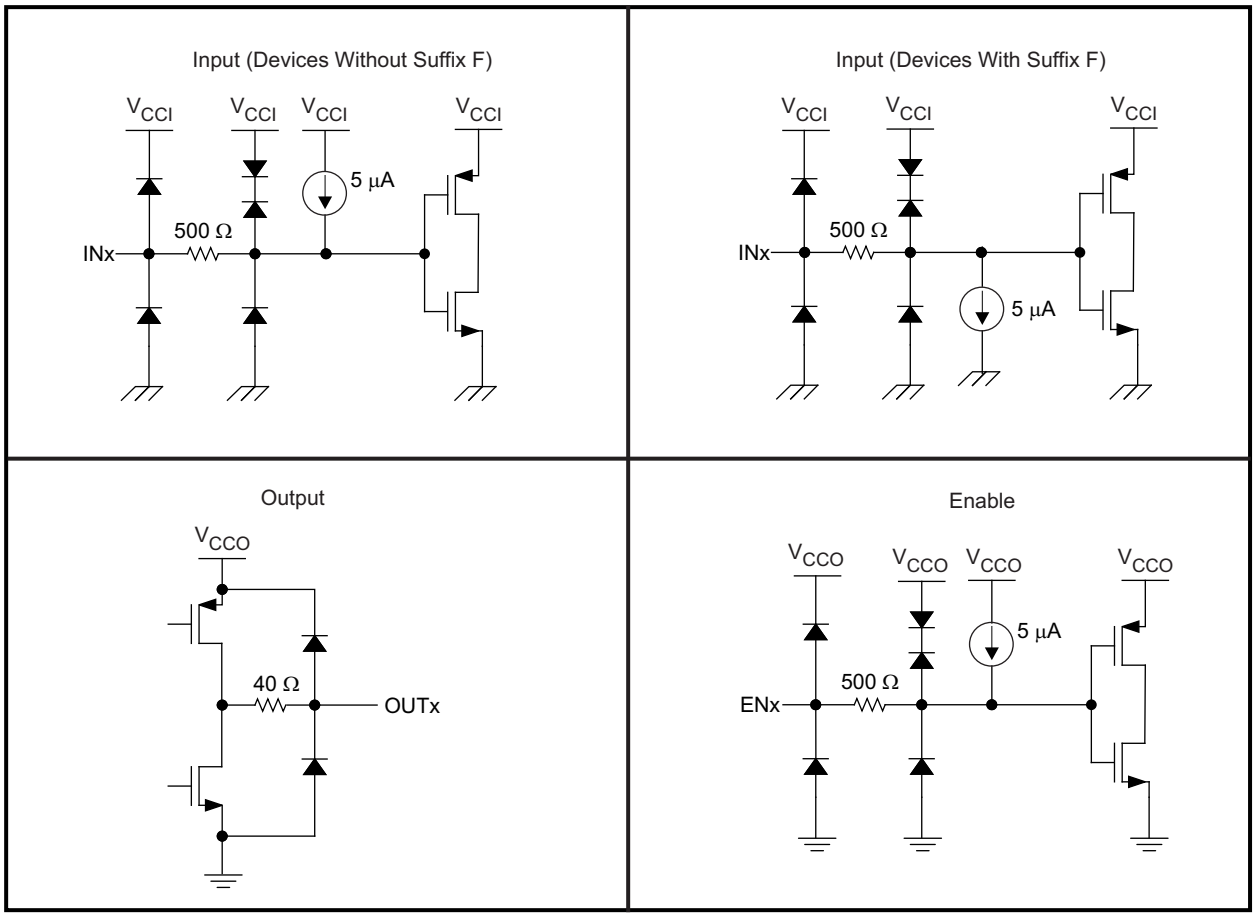


Figure 17. Device I/O Schematics

9 Application and Implementation

NOTE

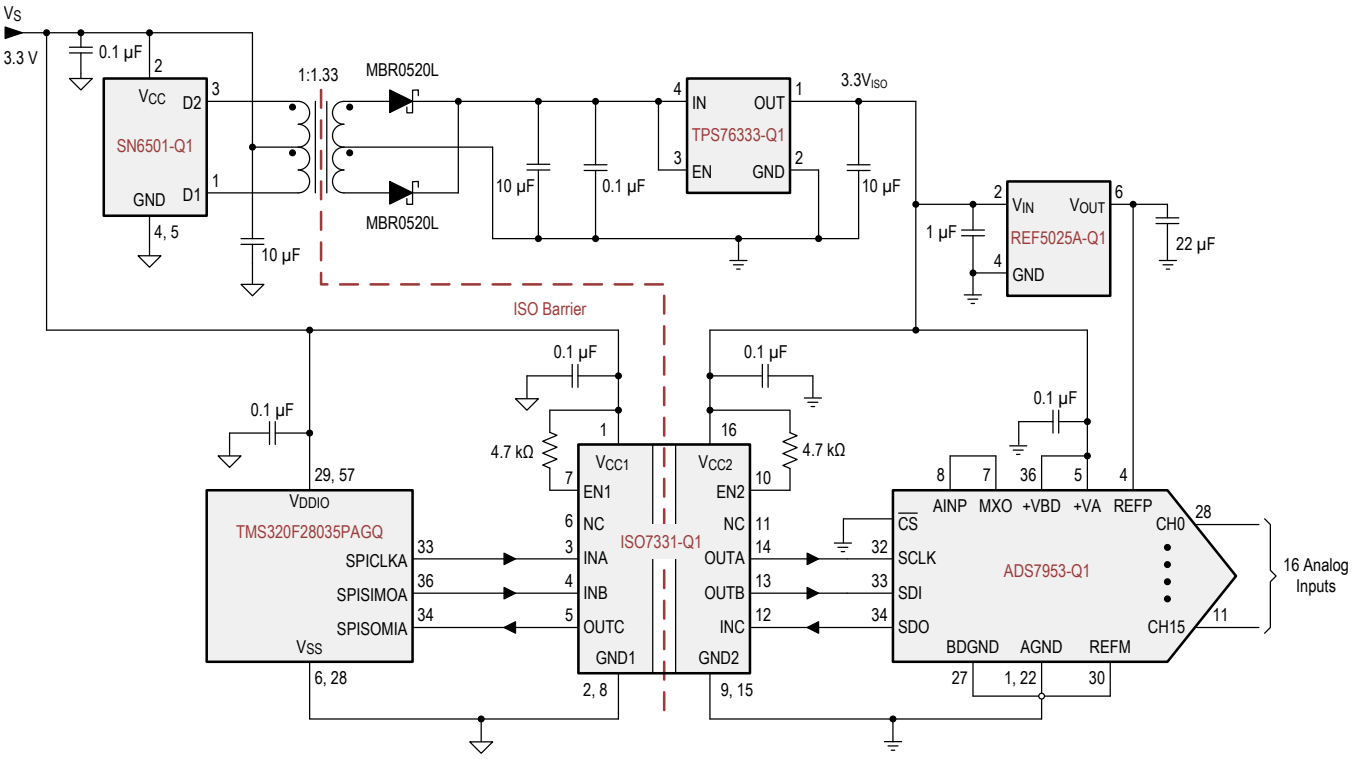
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO733x-Q1 family of devices uses single-ended TTL-logic switching technology. Its supply voltage range is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7331-Q1 device combined with Texas Instruments' Piccolo™ microcontroller, analog-to-digital receiver, transformer driver, and voltage regulator can create an isolated serial peripheral interface (SPI) as shown in Figure 18.



Multiple pins and discrete components are omitted for clarity.

Figure 18. Isolated SPI for an Analog Input Module With 16 Inputs and a Single Slave

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Typical Supply Current Equations

For the equations in this section, the following is true:

- I_{CC1} and I_{CC2} are typical supply currents measured in mA
- f is the data rate measured in Mbps
- C_L is the capacitive load measured in pF

9.2.1.1.1 ISO7330-Q1

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 0.46544 + (0.006455 \times f) \quad (1)$$

$$I_{CC2} = 2.28021 + (0.08242 \times f) + (0.006237 \times f \times C_L) \quad (2)$$

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 0.29211 + (0.03588 \times f) \quad (3)$$

$$I_{CC2} = 1.8414 + (0.02886 \times f) + (0.00548 \times f \times C_L) \quad (4)$$

9.2.1.1.2 ISO7321-Q1

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 1.661 + (0.07916 \times f) + (0.00169 \times f \times C_L) \quad (5)$$

$$I_{CC2} = 2.04 + (0.0778 \times f) + (0.00422 \times f \times C_L) \quad (6)$$

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 1.2402 + (0.03127 \times f) + (0.001954 \times f \times C_L) \quad (7)$$

$$I_{CC2} = 1.53839 + (0.02933 \times f) + (0.0037285 \times f \times C_L) \quad (8)$$

9.2.2 Detailed Design Procedure

9.2.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO733x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

Typical Application (continued)

9.2.3 Application Curves

The following typical eye diagrams of the ISO733x-Q1 family of devices indicate low jitter and wide open eye at the maximum data rate of 25 Mbps.

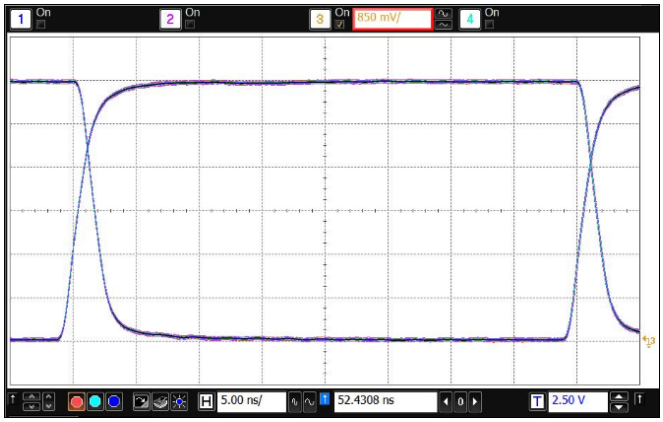


Figure 19. Eye Diagram at 25 Mbps, 5 V and 25°C

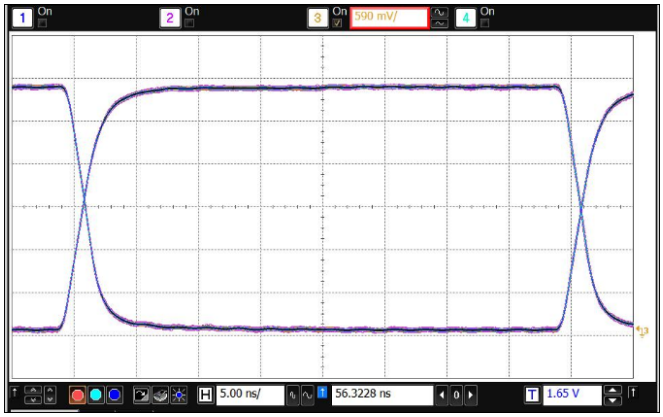


Figure 20. Eye Diagram at 25 Mbps, 3.3 V and 25°C

9.2.4 Systems Examples

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO733x-Q1 family of devices only requires two external bypass capacitors to operate.

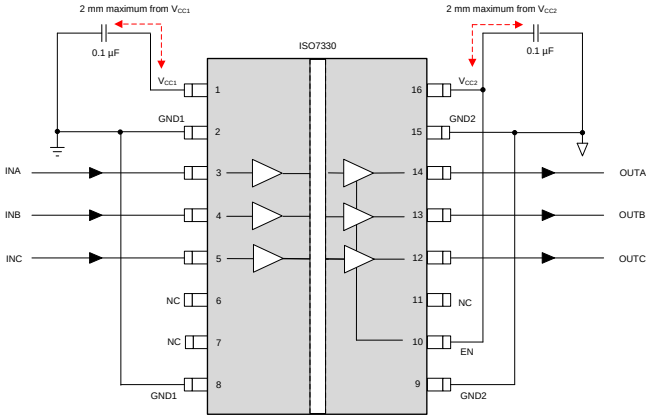


Figure 21. Typical ISO7330-Q1 Circuit Hook-up

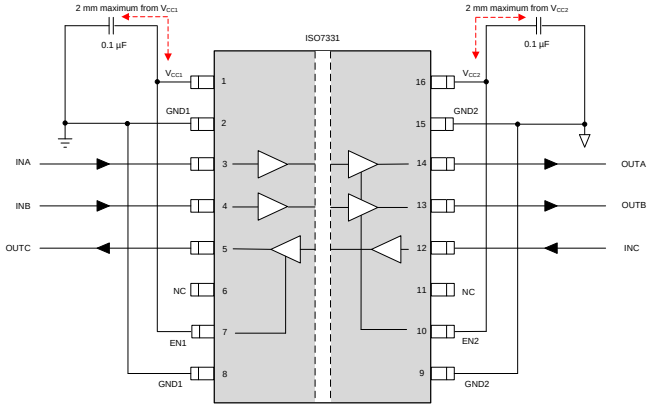


Figure 22. Typical ISO7331-Q1 Circuit Hook-up

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501-Q1. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501-Q1 datasheet (SLLSEF3) .

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 23). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the application note SLLA284, *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

11.2 Layout Example

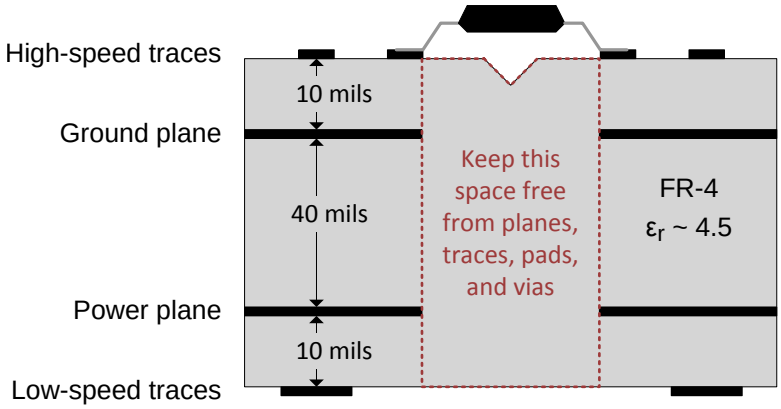


Figure 23. Recommended Layer Stack

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *《ADS79xx-Q1 8 位、10 位和 12 位，1MSPS，4 通道、8 通道、12 通道和 16 通道，单端，微功耗，串行接口，模数转换器》*，SBAS652
- *《数字隔离器设计指南》*，SLLA284
- *《ISO73xx 三/四通道数字隔离器评估模块》*，SLLU209
- *《隔离相关术语》*，SLLA353
- *《REF50xxA-Q1 低噪声、极低漂移、高精度电压基准》*，SBOS456
- *《SN6501-Q1 用于隔离电源的变压器驱动器》*，SLLSEF3
- *《TPS76333-Q1 低功耗 150mA 低压降线性稳压器》*，SGLS247
- *《TMS320F28035 Piccolo™ 微控制器》*，SPRS584

12.2 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **3.** 相关链接

器件	产品文件夹	样片与购买	技术文章	工具与软件	支持与社区
ISO7330-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7331-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

DeviceNet, Piccolo, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

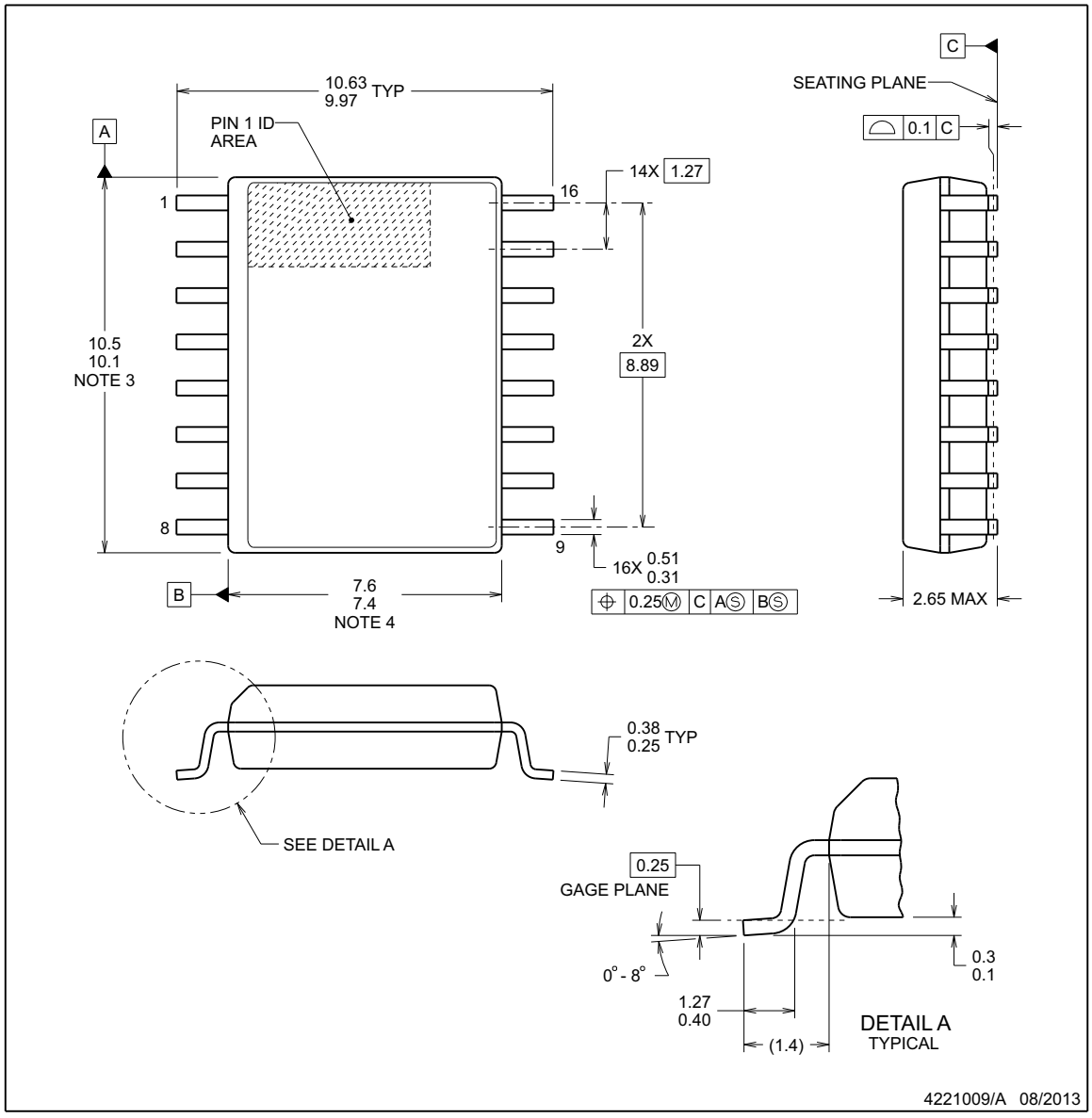
以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

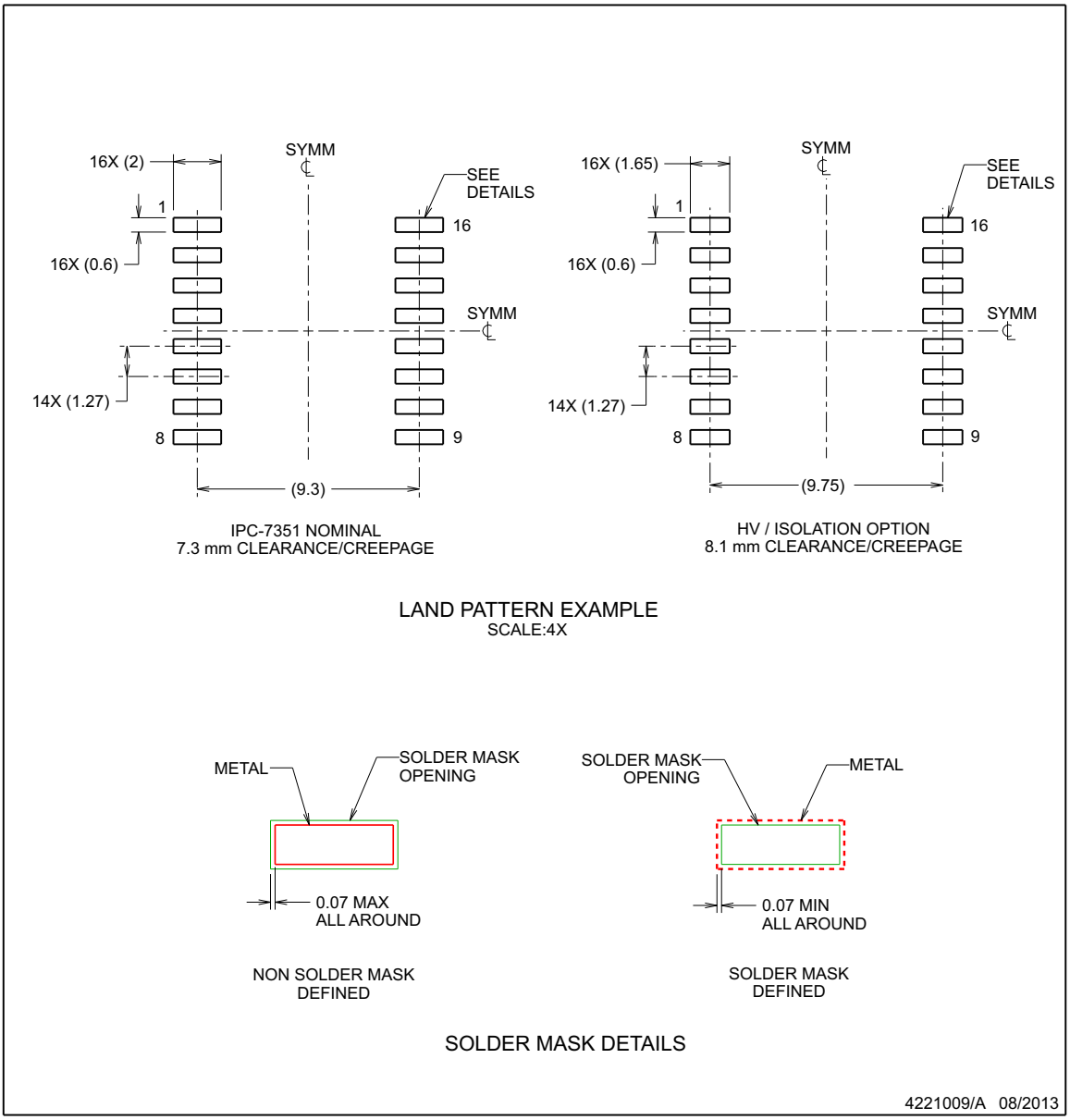
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

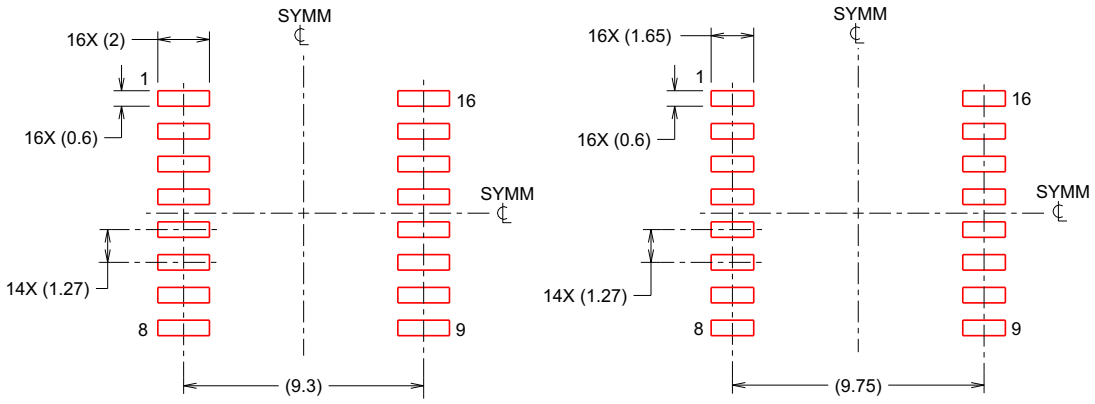
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7330CQDWQ1	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330CQ
ISO7330CQDWQ1.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330CQ
ISO7330CQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330CQ
ISO7330CQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330CQ
ISO7330FCQDWQ1	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330FCQ
ISO7330FCQDWQ1.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330FCQ
ISO7330FCQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330FCQ
ISO7330FCQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7330FCQ
ISO7331CQDWQ1	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331CQ
ISO7331CQDWQ1.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331CQ
ISO7331CQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331CQ
ISO7331CQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331CQ
ISO7331FCQDWQ1	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331FCQ
ISO7331FCQDWQ1.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331FCQ
ISO7331FCQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331FCQ
ISO7331FCQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7331FCQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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最后更新日期：2025 年 10 月