INA851 具有衰减增益和输出钳位的低噪声、全差分输出精密仪表放大器

1 特性

- 可使用外部电阻器
  在 G = 0.2 至 10,000 的范围内对增益进行编程
- 具有集成钳位的全差分输出
- 低失调电压：10 μV（典型值），35 μV（最大值）
- 低温漂：0.1 μV/°C（典型值），0.3 μV/°C（最大值）
- 低输入偏置电流：5 nA（典型值）
- 输入级噪声：3.2 nV/√Hz、0.8 pA/√Hz
- 高带宽：在 G = 0.2 时为 22 MHz，
  在 G = 1 时为 15 MHz
- 共模抑制：在 G = 10 时为 106 dB（最小值），在 100 ≤ G ≤ 1000 时为 120 dB（最小值）
- 电源抑制：在 G = 1 时为 110 dB（最小值）
- 电源电流：6mA（典型值）
- 在超过电源电压多达 ±40V 时提供输入过压保护
- 电源电压范围：
  - 单电源：8V 至 36V
  - 双电源：±4V 至 ±18V
- 额定温度范围：–40°C 至 +125°C
- 微型封装：16 引脚 VQFN

2 应用

- 模拟输入模块
- 流量变送器
- LCD 测试
- 心电图 (ECG)
- 外科手术设备
- 示波器 (DSO)
- 称重计
- 半导体测试

3 说明

INA851 是业内首款具有全差分输出的高精度仪表放大器。该器件经过优化，可驱动具有全差分输入的现代高性能模数转换器 (ADC) 的输入。INA851 可在非常宽的单电源或双电源电压范围内运行。可通过短接或悬空两个引脚，将输出级增益设置为 0.2 或 1。可通过单个外部电阻器在 1 到 10,000 范围内设置任意输入级增益。

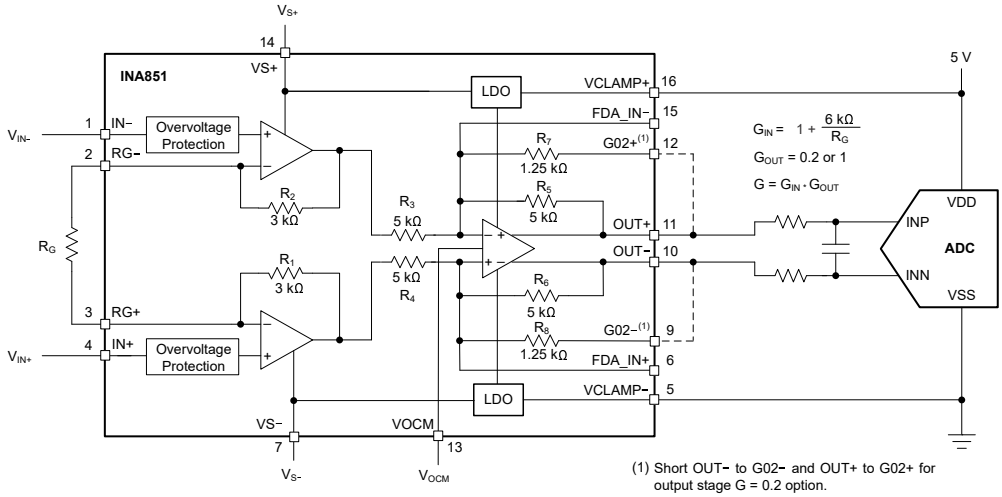
INA851 采用了超级 ß 输入晶体管，因此与同一级别的其他放大器相比，可提供极低的输入偏置电流和低输入参考电流噪声。先进的制造工艺实现了极低的电压噪声、输入失调电压和失调电压漂移。附加电路可保护器件输入免受超过电源电压多达 ±40V 的过压影响。器件输出具有内置钳位电路，可保护 ADC 或下游器件免受过驱损坏。

该器件可在单电源（最小 8V，最大 36V）或双电源（最小 ±4V，最大 ±18V）供电的情况下运行。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
INA851	RGT（VQFN，16）	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



INA851 ADC 驱动器应用

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (March 2022) to Revision A (October 2022)	Page
• 将 INA851 从预告信息（预发布）更改为量产数据（正在供货）	1

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5 Related Products

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA159	G = 0.2 V differential amplifier for ±10-V to 3-V and 5-V conversion	G = 0.2 V/V	N/A
INA818	35-µV offset, 0.4-µV/°C V_{OS} drift, 8-nV/ $\sqrt{Hz}$ noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG	1, 8
INA819	35-µV offset, 0.4-µV/°C V_{OS} drift, 8-nV/ $\sqrt{Hz}$ noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG	2, 3
INA821	35-µV offset, 0.4-µV/°C V_{OS} drift, 7-nV/ $\sqrt{Hz}$ noise, high-bandwidth, precision instrumentation amplifier	G = 1 + 49.4 kΩ / RG	2, 3
INA828	50-µV offset, 0.5-µV/°C V_{OS} drift, 7-nV/ $\sqrt{Hz}$ noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG	1, 8
INA333	25-µV V_{OS}, 0.1-µV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-µA I_Q, chopper-stabilized INA	G = 1 + 100 kΩ / RG	1, 8
INA848	Ultra-low-noise (1.5-nV/ $\sqrt{Hz}$), high-bandwidth instrumentation amplifier with fixed gain of 2000	G = 2000 V/V	N/A
INA849	Ultra-low-noise (1-nV/ $\sqrt{Hz}$), high-bandwidth instrumentation amplifier	G = 1 + 6 kΩ / RG	2, 3
PGA280	20-mV to ±10-V programmable gain IA with 3-V or 5-V differential output; analog supply up to ±18 V	Digital programmable	N/A
PGA281	Precision, zero-drift, programmable gain IA with differential output; binary gain steps from 1/8 V/V to 128 V/V	Digital programmable	N/A
PGA112	Precision programmable gain op amp with SPI	Digital programmable	N/A

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6 Pin Configuration and Functions

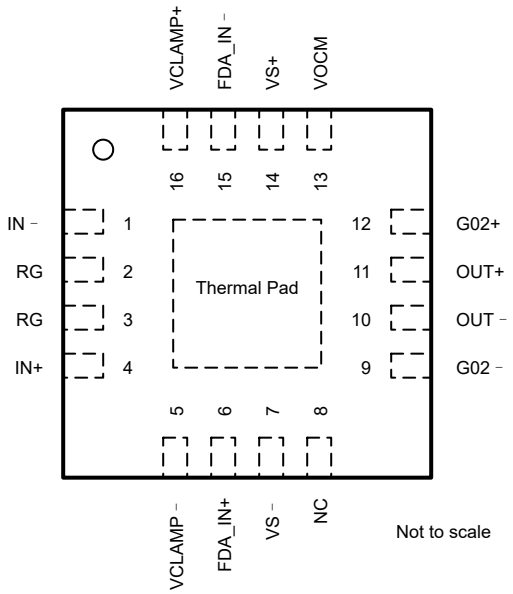

图 6-1. RGT (16-Pin VQFN) Package, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
FDA_IN –	15	Input	Connection to output driver summing node.
FDA_IN+	6	Input	Connection to output driver summing node.
G02 –	9	Input	Connection to gain network. Short to OUT – for output stage gain G_{OUT} of 0.2 V/V.
G02+	12	Input	Connection to gain network. Short to OUT+ for output stage gain G_{OUT} of 0.2 V/V.
IN –	1	Input	Negative (inverting) input.
IN+	4	Input	Positive (noninverting) input.
NC	8	—	No connect
OUT –	10	Output	Negative Output
OUT+	11	Output	Positive Output
RG	2,3	—	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
VCLAMP –	5	Input	Level set for output clamp value. Connect either to an external supply that is at least 1.5 V above VS – or connect to VS – if clamping function is not required.
VCLAMP+	16	Input	Level set for output clamp value. Connect either to an external supply that is at least 1.5 V below VS+ or connect to VS+ if clamping function is not required.
VOCM	13	Input	Level set for output common mode value.
VS –	7	Power	Negative supply
VS+	14	Power	Positive supply
Thermal Pad	Thermal pad	—	The thermal pad must be soldered to the printed-circuit board (PCB). Connect thermal pad to a plane or large copper pour electrically connected to the most negative supply or VS – .

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage on VS+, VS – pins; $V_S = (V_{S+}) - (V_{S-})$		0	40	V
V_{IN}	Input voltage on IN+, IN – pins		$(V_{S-}) - 40$	$(V_{S+}) + 40$	V
V_{DIFF}	Differential input voltage, $V_{DIFF} = (V_{IN+}) - (V_{IN-})$	G_{IN} = 1 V/V, continuous	$(-V_S) - 40$	$V_S + 40$	V
		G_{IN} > 1 V/V[3]	$(-V_S) - 40$	$V_S + 40$	V
	Output voltage on OUT+, OUT – pins		$(V_{S-}) - 0.5$	$(V_{S+}) + 0.5$	V
	FDA_IN+, FDA_IN – , G02+, G02 – , VCLAMP+, VCLAMP – , VOCM pins voltage		$(V_{S-}) - 0.5$	$(V_{S+}) + 0.5$	V
	Output short-circuit[2]		Continuous		
T_A	Operating temperature		–40	125	°C
T_J	Junction temperature			175	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.
(3) Keep operation below 1% duty cycle of device lifecycle.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, $V_S = (V_{S+})$, GND = (V_{S-})	8	36	V
		Dual supply, $V_S = (V_{S+}) - (V_{S-})$	±4	±18	
V_{IN}	Input voltage on IN+, IN – pins		$-V_S$	V_S	V
V_{DIFF}	Differential input voltage, $V_{DIFF} = (V_{IN+}) - (V_{IN-})$	G_{IN} = 1 V/V	$-V_S$	V_S	V
		G_{IN} > 1 V/V[1]	$-1 - (V_S) / G_{IN}$	$1 + (V_S) / G_{IN}$	
T_A	Specified temperature		–40	125	°C

(1) See also INA851 Calculator Tool.

7.4 Thermal Information

THERMAL METRIC[1]		INA851 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OSI}	Input stage offset voltage[1]				±10	±35	μV
		T_A = –40°C to +125°C[4]				±65	
	Input stage offset voltage drift[2]	T_A = –40°C to +125°C[4]			±0.1	±0.3	μV/°C
V_{OSO}	Output stage offset voltage[1]	G = 0.2			±150	±1150	μV
		G = 1			±150	±650	
	Output stage offset voltage drift[2]	T_A = –40°C to +125°C[4]	G = 0.2		±5	±15	μV/°C
			G = 1		±5	±15	
PSRR	Power-supply rejection ratio	±4 V ≤ V_S ≤ ±18 V, RTI	G = 0.2	100	120		dB
			G = 1	110	126		
			G_{IN} = 10	120	140		
			G_{IN} = 100	126	140		
			G_{IN} = 1000	130	140		
z_{id}	Differential impedance				1 || 100		pF || GΩ
z_{ic}	Common-mode impedance				7 || 100		pF || GΩ
V_{IN}	Input voltage[4] [5]	See also INA851 Calculator Tool		(V_{S-}) + 2.5		(V_{S+}) – 2.5	V
	Protected input voltage[8]			(V_{S-}) – 40		(V_{S+}) + 40	V
	Input current in overvoltage mode[9]	(V_{S-}) – 40 V ≤ V_{IN} ≤ (V_{S+}) + 40 V[3]			16		mA
CMRR	Common-mode rejection ratio	At dc to 60 Hz, RTI, V_{CM} = (V_{S-}) + 2.5 V to (V_{S+}) – 2.5 V	G = 0.2	76	90		dB
			G = 1	86	96		
			G_{IN} = 10	106	116		
			G_{IN} = 100	120	132		
			G_{IN} = 1000	120	134		

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7.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BIAS CURRENT							
I_B	Input bias current				5	15	nA
		T_A = –40°C to +125°C[4]				18	
	Input bias current drift	T_A = –40°C to +125°C			25		pA/°C
I_{OS}	Input offset current				0.5	5.5	nA
		T_A = –40°C to +125°C[4]				6	
	Input offset current drift	T_A = –40°C to +125°C			5		pA/°C
NOISE VOLTAGE							
e_{NI}	Input stage voltage noise density	f = 1 kHz, G = 1000			3.2		nV/√Hz
	Input stage voltage noise	f_B = 0.1 Hz to 10 Hz, G = 1000			0.1		μV_{PP}
e_{NO}	Output stage voltage noise density[7]	f = 1 kHz	G = 0.2		83		nV/√Hz
			G = 1		52		
			G = 1; G_{IN} = 5, G_{OUT} = 0.2		12		
	Output stage voltage noise[7]	f_B = 0.1 Hz to 10 Hz	G = 0.2		5.0		μV_{PP}
			G = 1		2.8		μV_{PP}
	Current noise density	f = 1 kHz, G_{IN} = 1000			0.8		pA/√Hz
I_n	Current noise	f_B = 0.1 Hz to 10 Hz, G = 100			37		pA_{PP}
GAIN							
	Gain equation	G = G_{IN} × G_{OUT}			(1 + (6 kΩ / R_G)) × (0.2 or 1)		V/V
G	Gain	G_{OUT} = 0.2		0.2		2000	V/V
		G_{OUT} = 1		1		10000	
GE	Gain error	G = 0.2, V_O = ±2 V				±0.1	%
		G = 1, V_O = ±10 V				±0.02	
		G_{IN} ≥ 10, V_O = ±10 V				±0.2	
	Gain drift[6]	T_A = –40°C to +125°C[4]	G = 0.2			±5	ppm/°C
			G = 1			±5	
			G_{IN} > 1			±35	
	Gain nonlinearity	G = 0.2, V_O = –2 V to +2 V			±5		ppm
		G = 1, V_O = –10 V to +10 V			±5		
OUTPUT							
V_O	Output voltage swing	I_{OUT} = 10 mA, T_A = –40°C to +125°C	No output clamping (V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-})	(V_{S-}) + 1.4		(V_{S+}) – 1.4	V
			Output clamping enabled (V_{CLAMP+} = V_{S+} – 1.5 V, V_{CLAMP-} = V_{S-} +1.5 V)	(V_{CLAMP-}) – 0.1		(V_{CLAMP+}) + 0.1	
C_L	Load capacitance	Stable operation for differential load			100		pF
Z_O	Closed-loop output impedance	f = 1 MHz			0.9		Ω
I_{SC}	Short-circuit current	T_A = –40°C to 125°C, continuous to V_S / 2			±37		mA

7.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 0.2			22		MHz
		G = 1, G_{IN} = 5, G_{OUT} = 0.2			22		
		G = 1			15		
		G_{IN} = 10			11		
		G_{IN} = 100			5		
		G_{IN} = 1000			0.8		
SR	Slew rate	G = 1, V_O = ±10 V			37		V/µs
t_S	Settling time	0.01%	G = 0.2, V_{STEP} = 2 V		0.24		µs
			G = 1, V_{STEP} = 10 V		0.24		
			G_{IN} = 10, 100, V_{STEP} = 10 V		0.5		
			G_{IN} = 1000, V_{STEP} = 10 V		1.7		
		0.001%	G = 0.2, V_{STEP} = 2 V		0.55		µs
			G = 1, V_{STEP} = 10 V		0.55		
			G_{IN} = 10,100, V_{STEP} = 10 V		2.1		
			G_{IN} = 1000, V_{STEP} = 10 V		2.5		
THD+N	Total harmonic distortion plus noise	Differential input, f = 10 kHz	G = 0.2, V_O = 2 V_{PP}		–109		dB
			G = 1, V_O = 10 V_{PP}		–110		
HD2	Second-order harmonic distortion	Differential input, f = 10 kHz	G = 0.2, V_O = 2 V_{PP}		–131		dB
			G = 1, V_O = 10 V_{PP}		–128		
HD3	Third-order harmonic distortion	Differential input, f = 10 kHz	G = 0.2, V_O = 2 V_{PP}		–119		dB
			G = 1, V_O = 10 V_{PP}		–121		
OUTPUT COMMON-MODE VOLTAGE (V_{OCM}) CONTROL							
	V_{OCM} Input voltage	T_A = –40°C to +125°C	No output clamping	(V_{S-}) + 2.5		(V_{S+}) – 2.5	V
			Output clamp enabled	(V_{CLAMP-}) + 1		(V_{CLAMP+}) – 1	
	Small-signal bandwidth from V_{OCM} pin	V_{OCM} = 100 mV_{PP}			30		MHz
	Large-signal bandwidth from V_{OCM} pin	V_{OCM} = 0.5-V step			47		MHz
	Slew rate from V_{OCM} pin	V_{OCM} = 0.5-V step			37		V/µs
	DC output balance	V_{OCM} fixed midsupply (V_O = ±1 V)			70		dB
	Input impedance V_{VOCM} pin				250 || 1		kΩ || pF
	V_{OCM} offset from mid-supply	V_{OCM} pin floating			±2	±6	mV
	V_{OCM} common-mode offset voltage	V_{OCM} = V_{ICM}, V_O = 0 V			±2	±6	mV
			T_A = –40°C to +125°C			±10	
	V_{OCM} common-mode offset voltage drift	V_{OCM} = V_{ICM}, V_O = 0 V, T_A = –40°C to +125°C			±20	±60	µV/°C

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7.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT CLAMPING							
V_{CLAMP+}	Positive clamp voltage(10)	T_A = –40°C to +125°C	No output clamping		V_{S+}		V
			Output clamp enabled			V_{S+} – 1.5	
V_{CLAMP-}	Negative clamp voltage(10)	T_A = –40°C to +125°C	No output clamping		V_{S-}		V
			Output clamp enabled	V_{S-} + 1.5			
ΔV_{CLAMP}	Clamp voltage(10)	$\Delta V_{CLAMP} = (V_{CLAMP+}) - (V_{CLAMP-})$		3			V
	Power-supply rejection ratio from V_{CLAMP} to V_O (3)				120		dB
	Fail-safe current V_{CLAMP+}	$V_{S+} = V_{S-}$ = 0 V, V_{CLAMP+} = 10 V			2		mA
I_{CLAMP+}	Positive clamp current	$V_{CLAMP+} \leqslant V_{S+}$ – 1.5 V		–80	–60		µA
I_{CLAMP-}	Negative clamp current	$V_{CLAMP-} \geqslant V_{S-}$ + 1.5 V			60	80	µA
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0 V			6	7	mA
			T_A = –40°C to +125°C			9	

(1) Offset voltages are uncorrelated. Total offset voltage, referred-to-input (RTI): $V_{OS} = \sqrt{[V_{OSI}^2 + (V_{OSO(Gout1\ or\ Gout0.2)} / G_{IN})^2]}$. See more details on *Offset Voltage* section.
(2) Offset drifts are uncorrelated. Offset drift, referred-to-input (RTI): $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}^2 + (\Delta V_{OSO} / G_{IN})^2]}$.
(3) Specified by design.
(4) Specified by characterization.
(5) Input voltage range of the instrumentation amplifier input stage. The valid input range depends on the common-mode voltage, differential voltage, gain, and V_{OCM}. See also the *Input Common-Mode Range* section.
(6) The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.
(7) e_{NO} refers to output stage noise referred to the input of the FDA. See also the *Noise Equivalent Model* section.
(8) See also the *Input Protection* section.
(9) See also the *Typical Characteristics* section.
(10) See also the *Output Clamping* section.

7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)

表 7-1. Table of Graphs

DESCRIPTION	FIGURE
Typical Distribution of Input Stage Offset Voltage	图 7-1
Typical Distribution of Input Stage Offset Voltage Drift	图 7-2
Typical Distribution of Output Stage Offset Voltage, G = 1	图 7-3
Typical Distribution of Output Stage Offset Voltage, G = 0.2	图 7-4
Typical Distribution of Output Stage Offset Voltage Drift	图 7-5
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7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)

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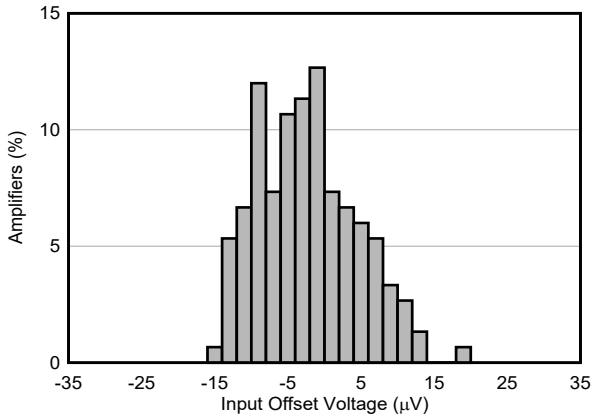
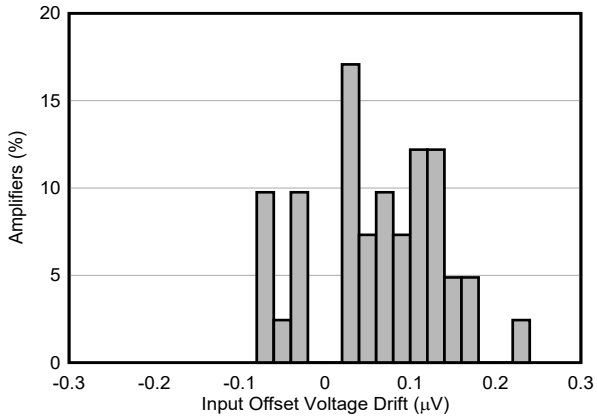
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)



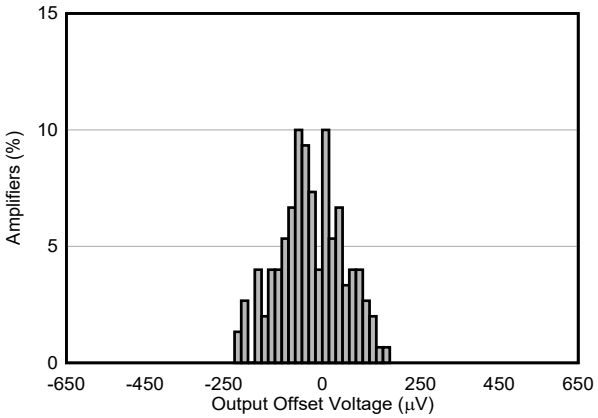
N = 150 Mean = –2.32 µV Std. Dev. = 6.73 µV

图 7-1. Typical Distribution of Input Stage Offset Voltage



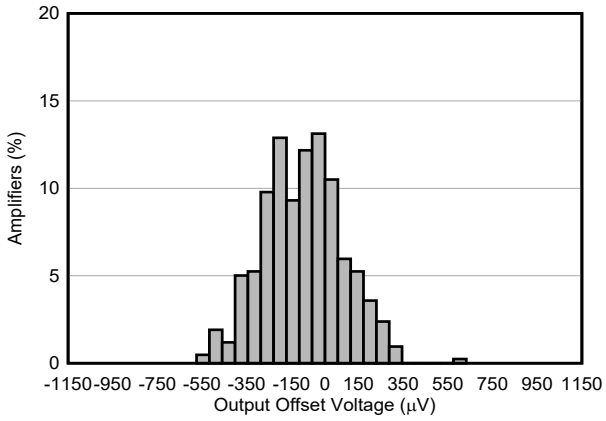
N = 82 Mean = 0.062 µV/°C Std. Dev. = 0.0738 µV/°C

图 7-2. Typical Distribution of Input Stage Offset Voltage Drift



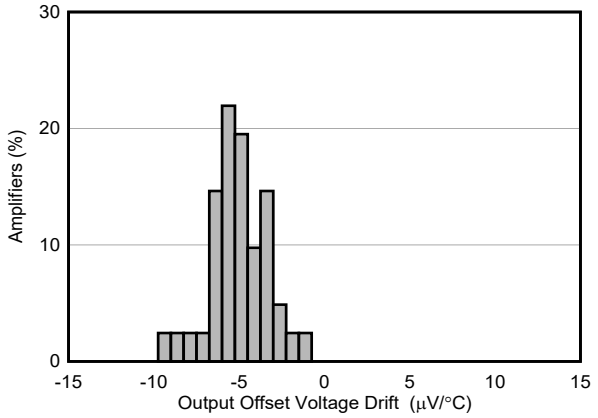
N = 150 Mean = –27.84 µV Std. Dev. = 82.71 µV
G = 1 V/V

图 7-3. Typical Distribution of Output Offset Voltage



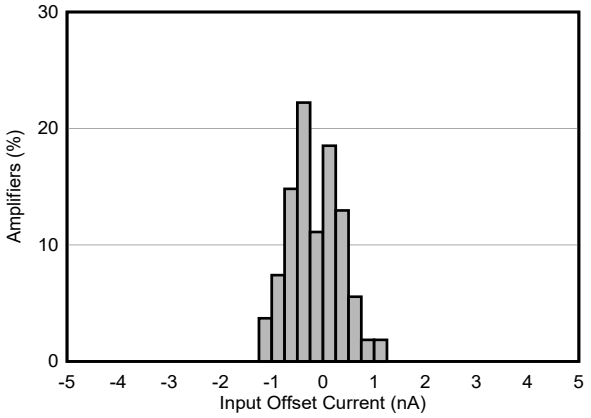
N = 150 Mean = –97.17 µV Std. Dev. = 179.33 µV
G = 0.2 V/V

图 7-4. Typical Distribution of Output Offset Voltage



N = 82 Mean = –4.98 µV/°C Std. Dev. = 1.59 µV/°C

图 7-5. Typical Distribution of Output Stage Offset Voltage Drift



N = 53 Mean = –0.14 nA Std. Dev. = 0.50 nA

图 7-6. Typical Distribution of Input Offset Current

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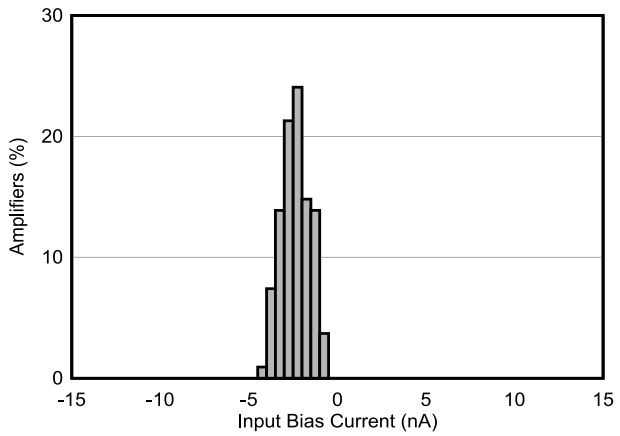
7.6 Typical Characteristics (continued)

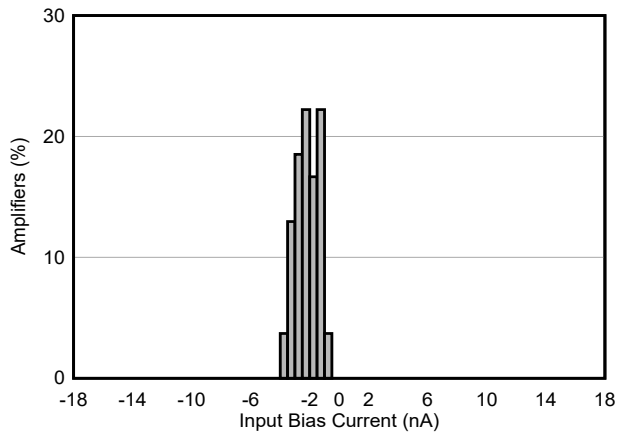
at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)



N = 107 Mean = –2.34 nA Std. Dev. = 0.78 nA

T_A = 25°C

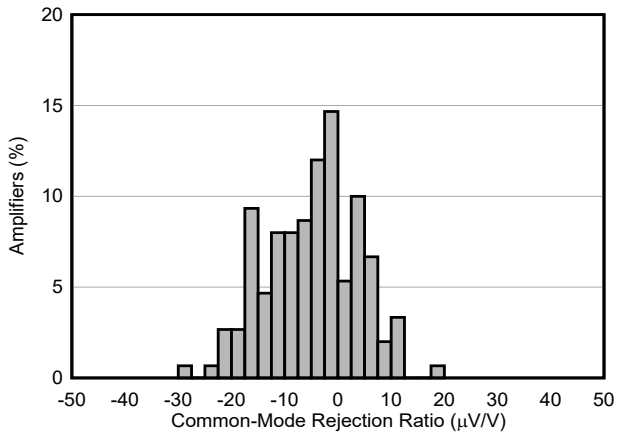
图 7-7. Typical Distribution of Input Bias Current



N = 107 Mean = –2.2 nA Std. Dev. = 0.75 nA

T_A = 90°C

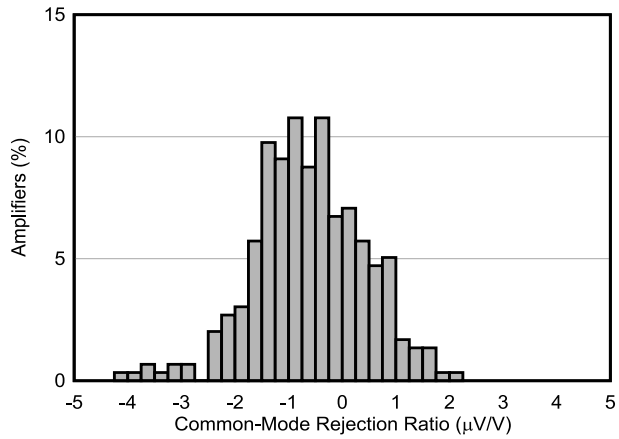
图 7-8. Typical Distribution of Input Bias Current



N = 150 Mean = –4.78 µV/V Std. Dev. = 8.67 µV/V

G = 1 V/V

图 7-9. Typical CMRR Distribution at G = 1 V/V



N = 300 Mean = –0.62 µV/V Std. Dev. = 1.03 µV/V

G = 10 V/V

图 7-10. Typical CMRR Distribution at G = 10 V/V

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)

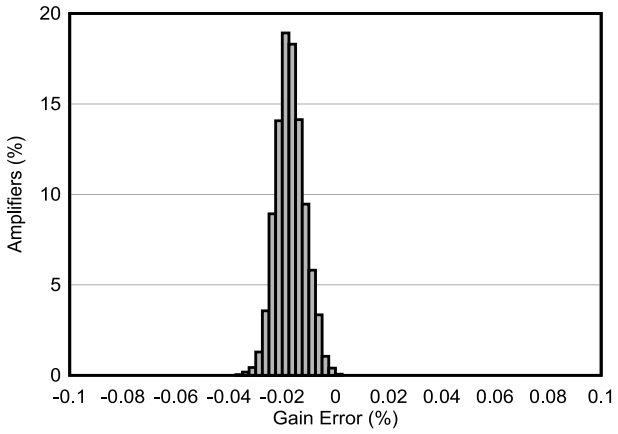


图 7-11. Typical Gain Error Distribution at G = 0.2 V/V

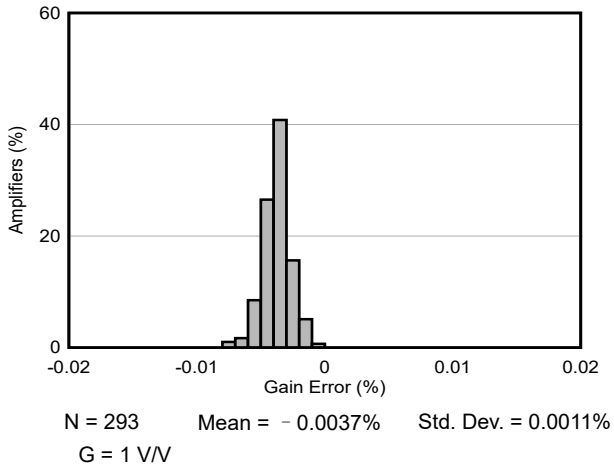


图 7-12. Typical Gain Error Distribution at G = 1 V/V

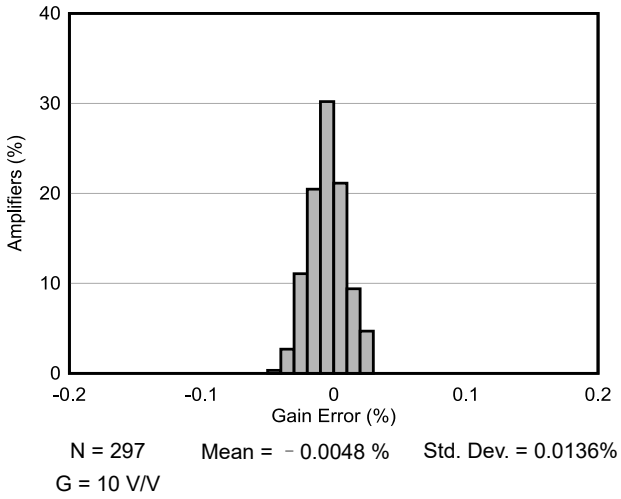


图 7-13. Typical Gain Error Distribution at G = 10 V/V

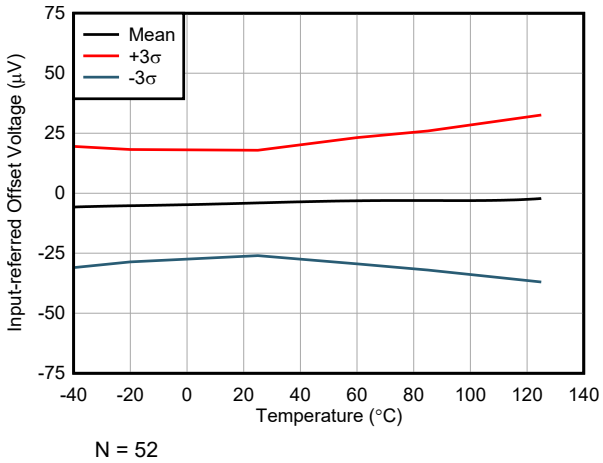


图 7-14. Input Stage Offset Voltage vs Temperature

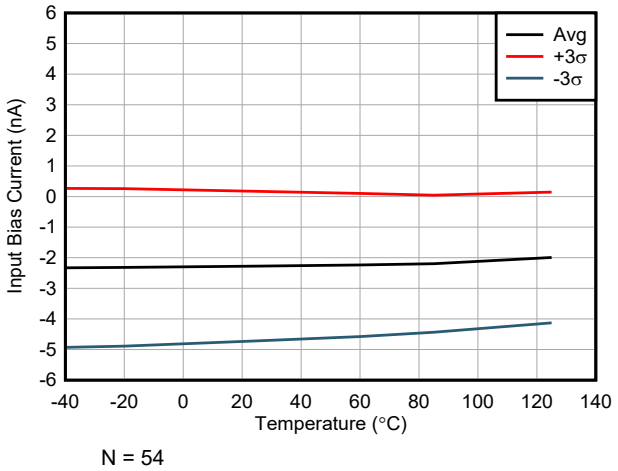


图 7-15. Input Bias Current vs Temperature

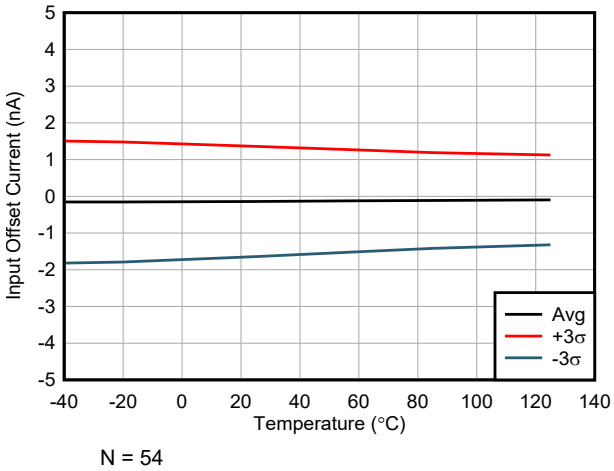


图 7-16. Input Offset Current vs Temperature

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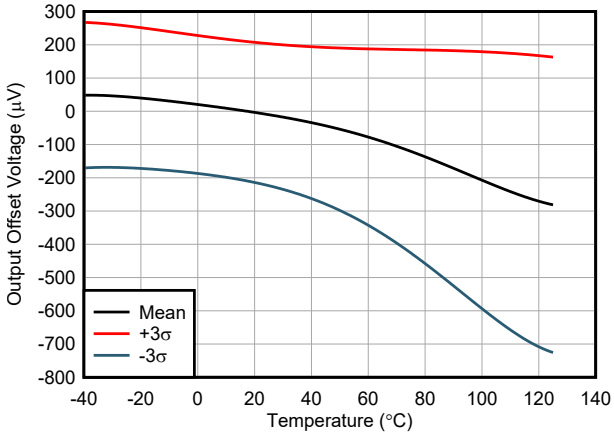
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)



N = 50

图 7-17. Input-Referred Output Offset Voltage vs Temperature

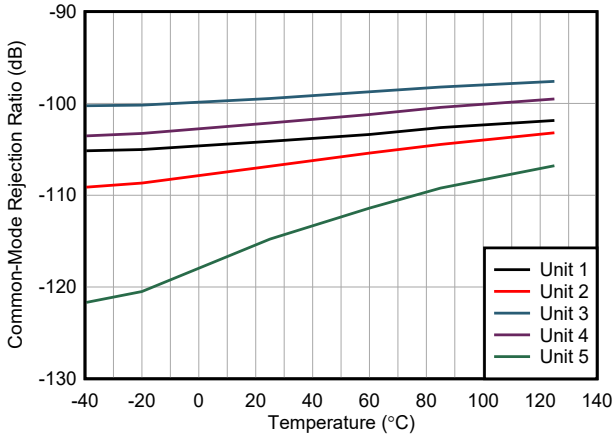
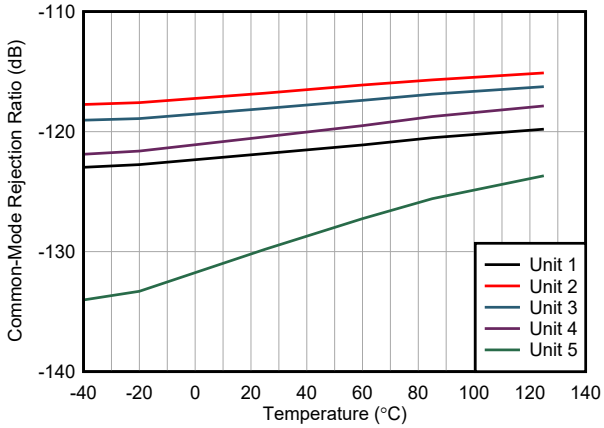


图 7-18. CMRR vs Temperature



G = 10

图 7-19. CMRR vs Temperature

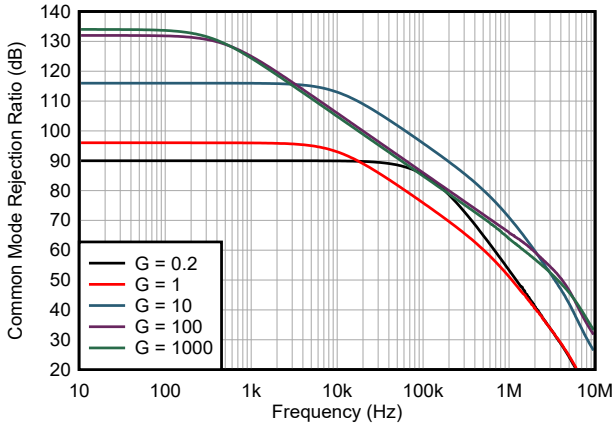
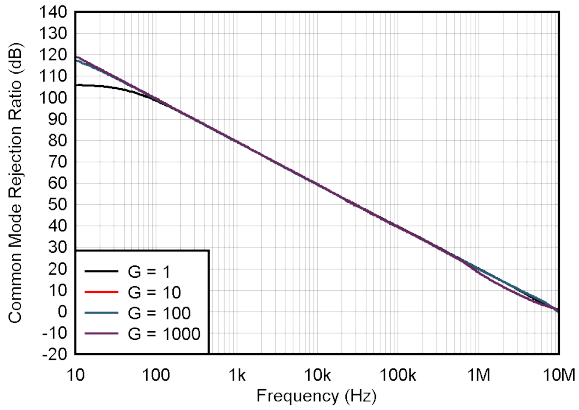


图 7-20. CMRR vs Frequency (RTI)



1-kΩ source imbalance

图 7-21. CMRR vs Frequency (RTI) Imbalance

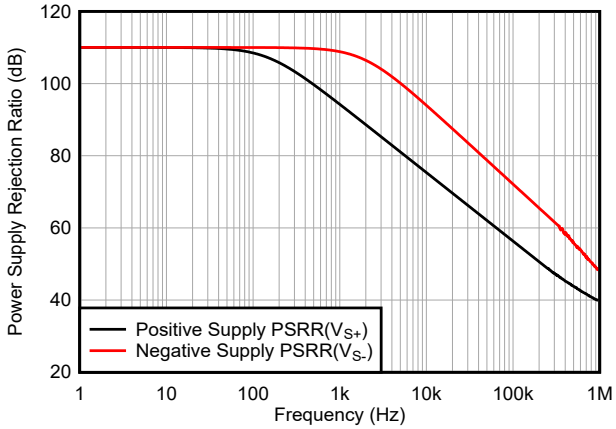


图 7-22. PSRR vs Frequency (RTI)

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)

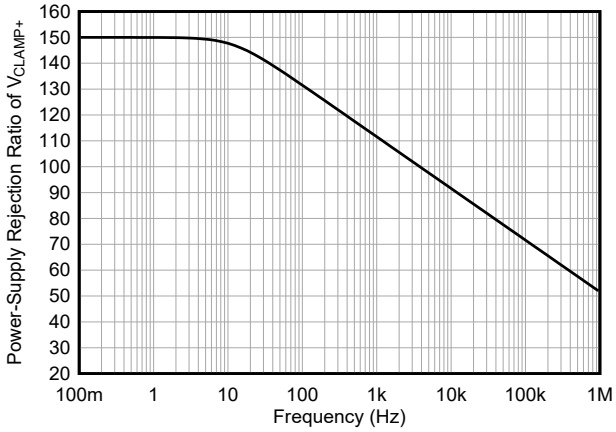


图 7-23. PSRR vs Frequency (RTI) of VCLAMP+

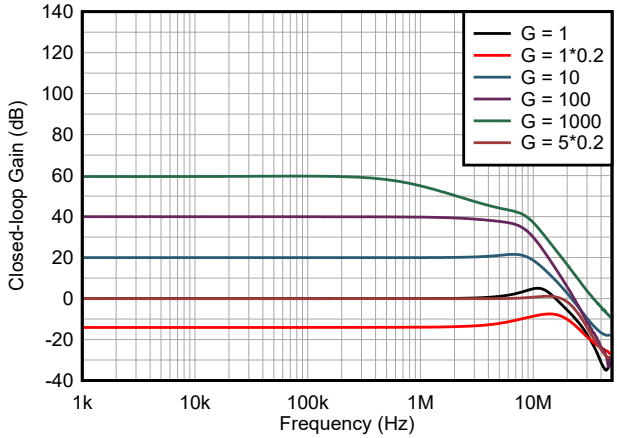
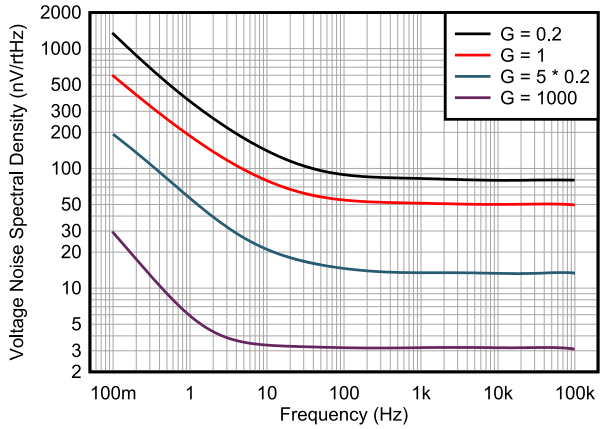
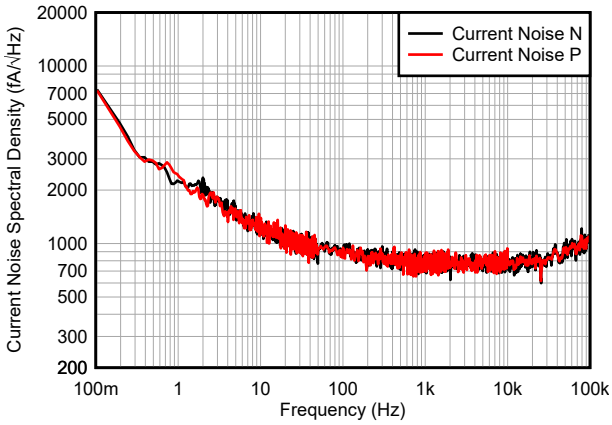


图 7-24. Gain vs Frequency



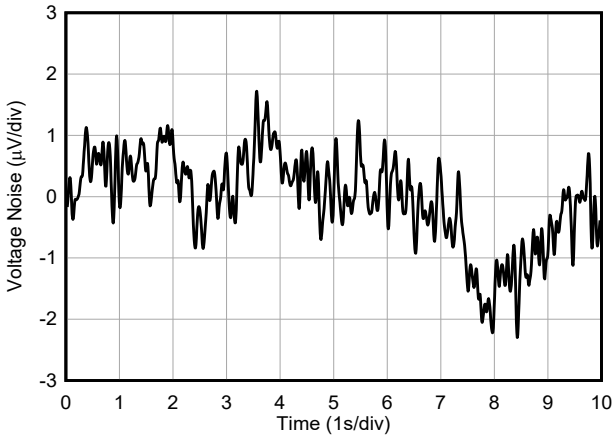
$e_{N(RTI)} = \sqrt{[e_{NI}^2 + (e_{NO(G0.2 \text{ or } G1)} / G_{IN})^2]}$

图 7-25. Voltage Noise Spectral Density vs Frequency (RTI)



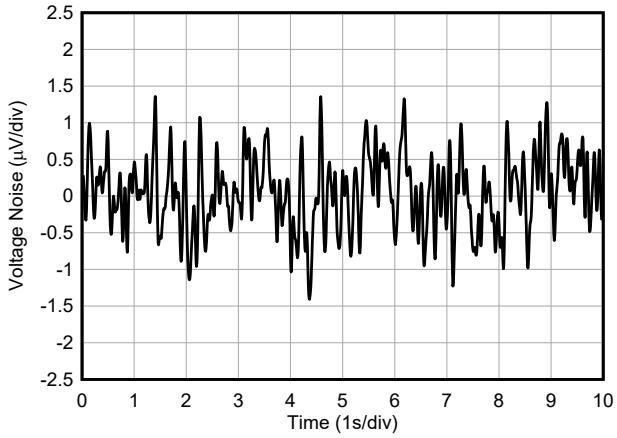
G = 1000 V/V

图 7-26. Current Noise Spectral Density vs Frequency (RTI)



G = 0.2 V/V

图 7-27. 0.1-Hz to 10-Hz RTI Voltage Noise



G = 1 V/V

图 7-28. 0.1-Hz to 10-Hz RTI Voltage Noise

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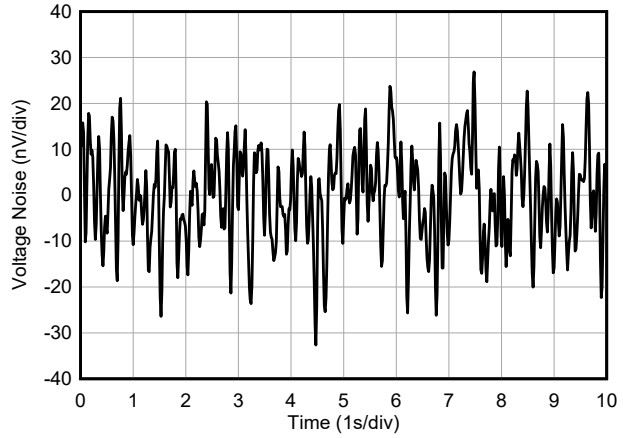
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)



G = 1000 V/V

图 7-29. 0.1-Hz to 10-Hz RTI Voltage Noise

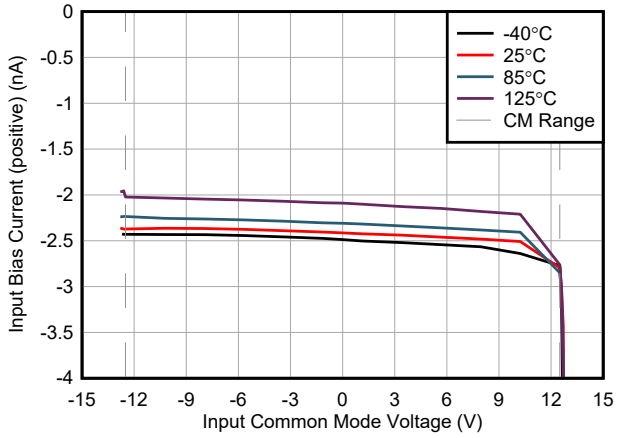


图 7-30. Positive Input Bias Current vs Common-Mode Voltage

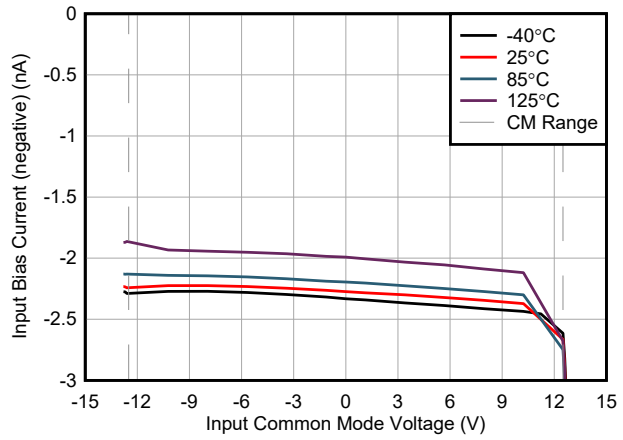


图 7-31. Negative Input Bias Current vs Common-Mode Voltage

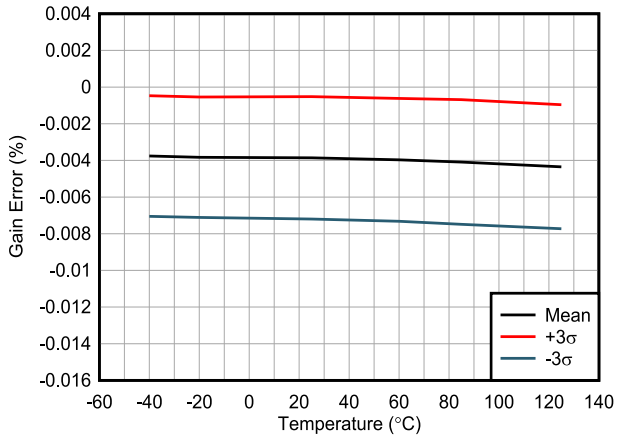


图 7-32. Gain Error vs Temperature

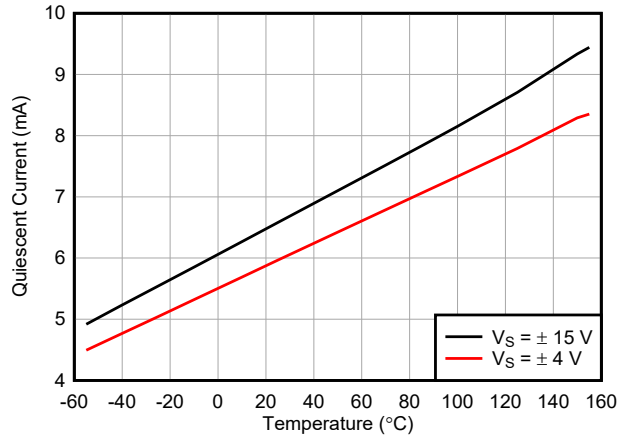
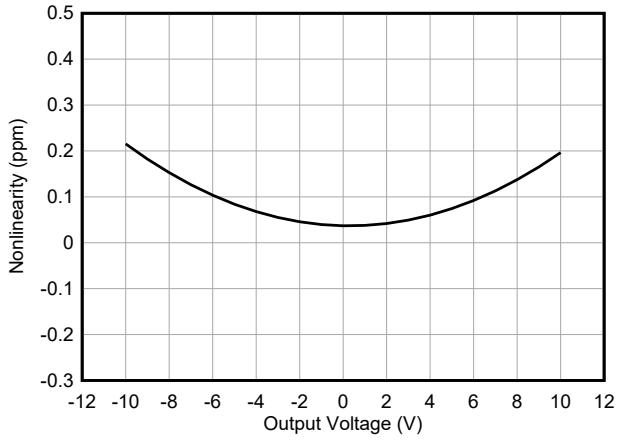


图 7-33. Quiescent Current vs Temperature



G = 1

图 7-34. Gain Nonlinearity, G = 1

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)

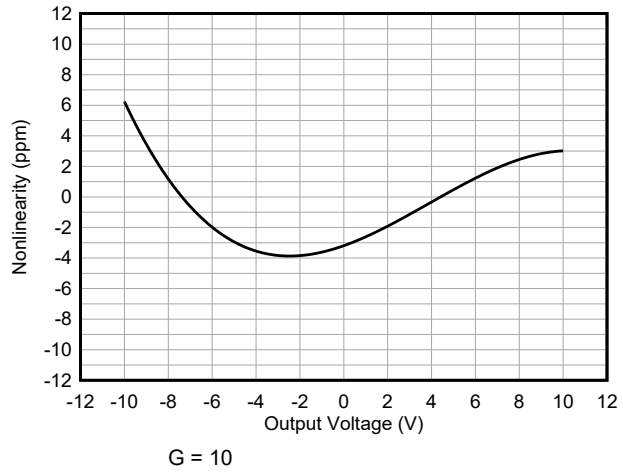


图 7-35. Gain Nonlinearity, G = 10

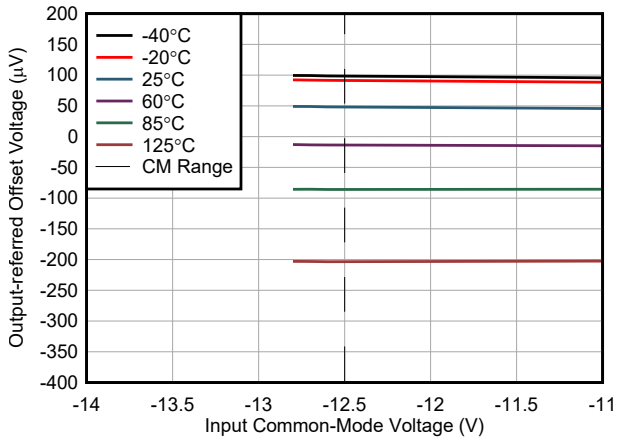


图 7-36. Offset Voltage vs Negative Common-Mode Voltage

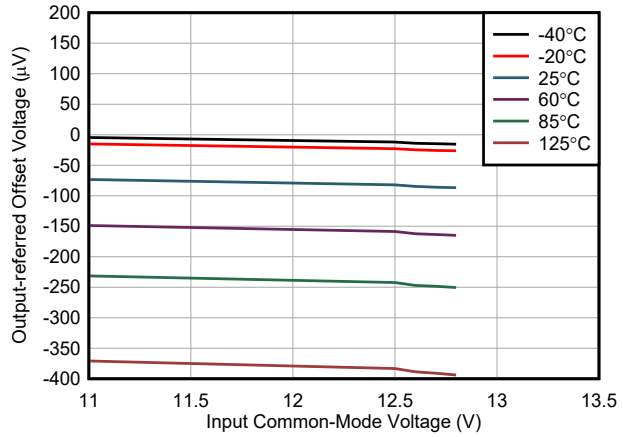


图 7-37. Offset Voltage vs Positive Common-Mode Voltage

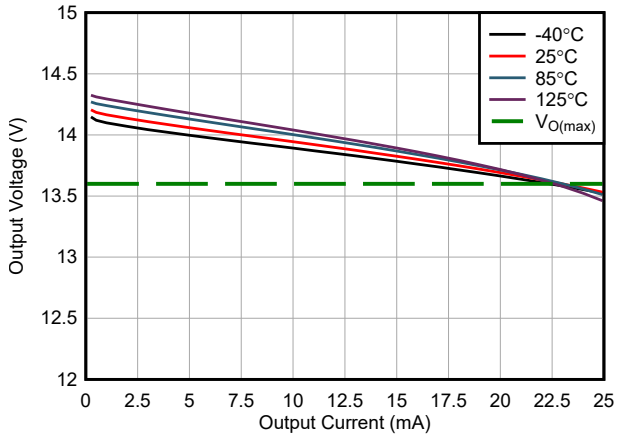


图 7-38. Positive Output Voltage Swing vs Output Current

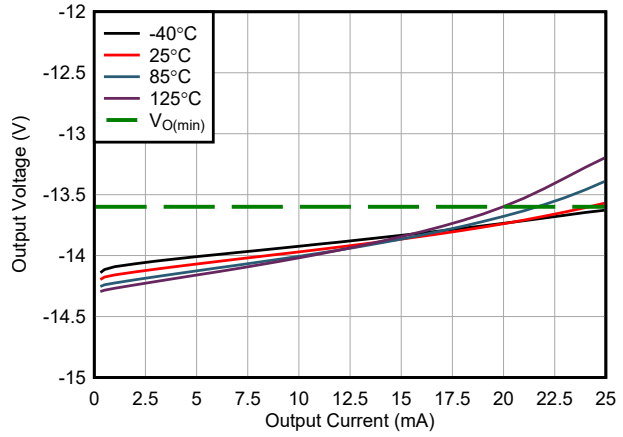


图 7-39. Negative Output Voltage Swing vs Output Current

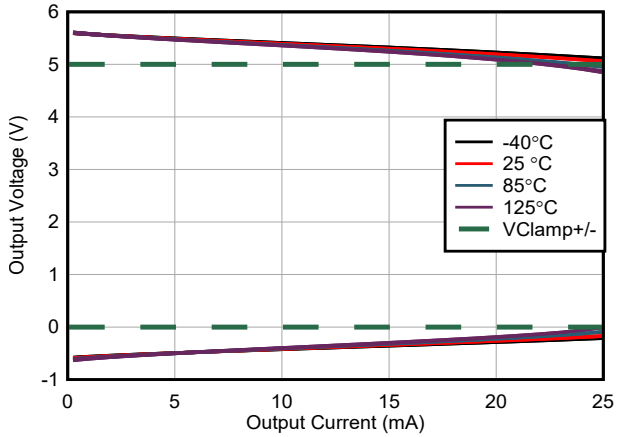


图 7-40. Claw Curve of VCLAMP+/-

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)

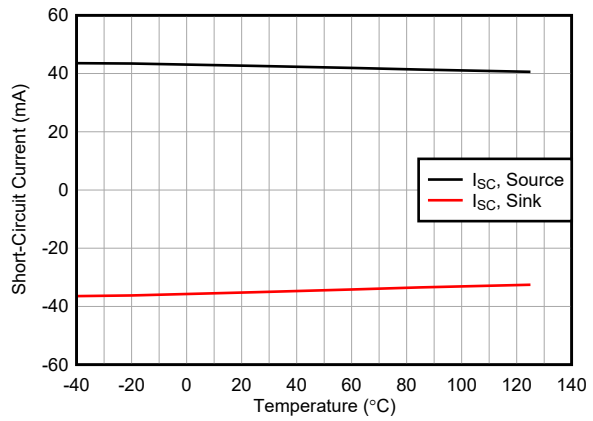


图 7-41. Short Circuit Current vs Temperature

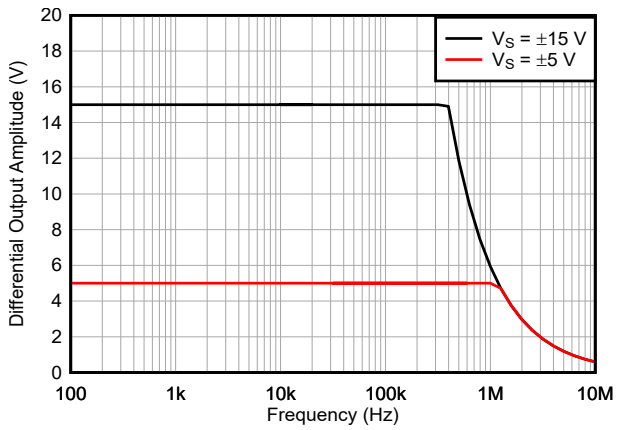
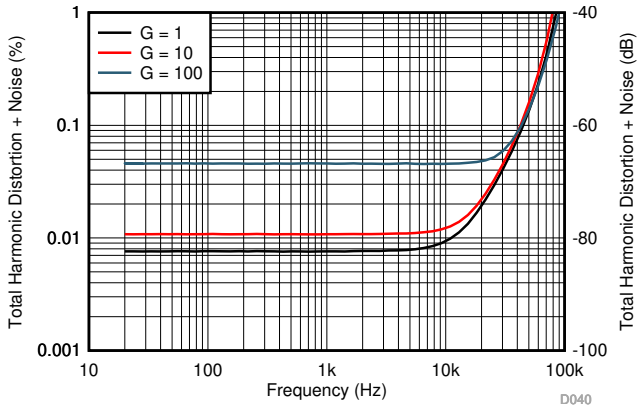


图 7-42. Large-Signal Frequency Response



500-kHz measurement bandwidth

1-V_{RMS} output voltage 100-kΩ load

图 7-43. THD+N vs Frequency

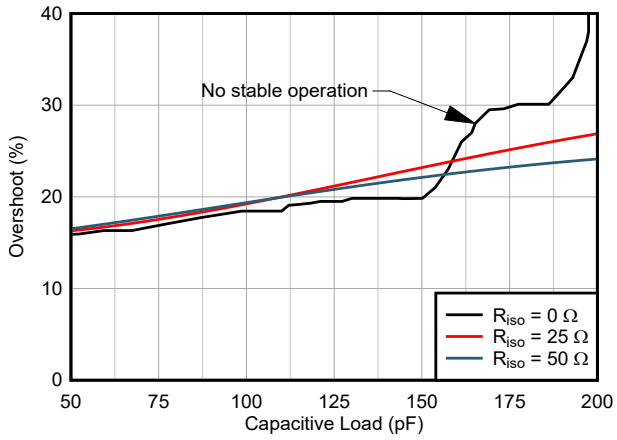
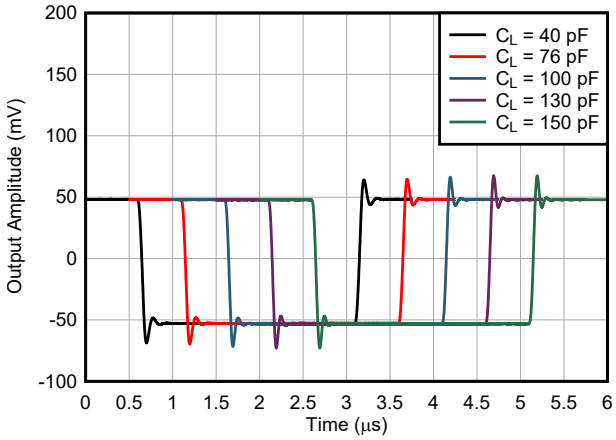
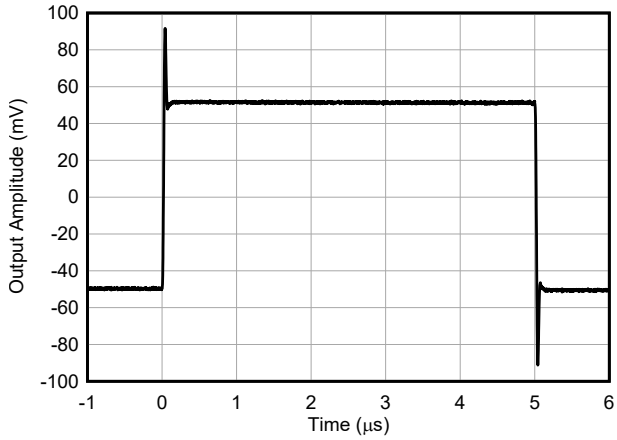


图 7-44. Overshoot vs Capacitive Loads



G = 1 R_L = 10 kΩ

图 7-45. Small-Signal Response with different Output Capacitors G = 1 V/V

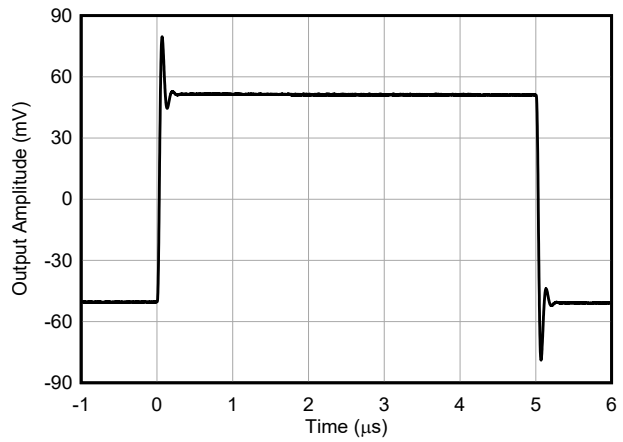


G = 0.2 V/V R_L = 10 kΩ C_L = 100 pF

图 7-46. Small-Signal Response for G = 0.2 V/V

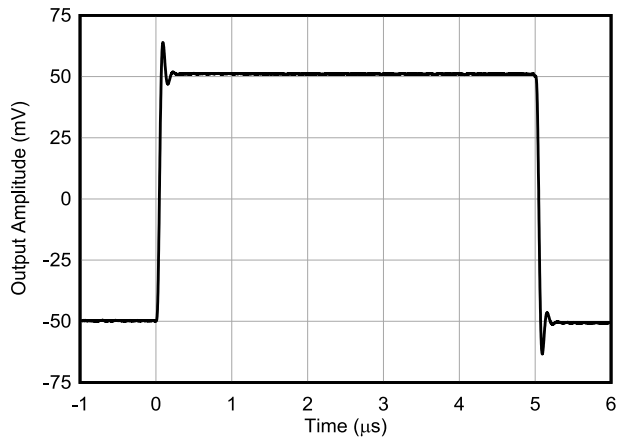
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)



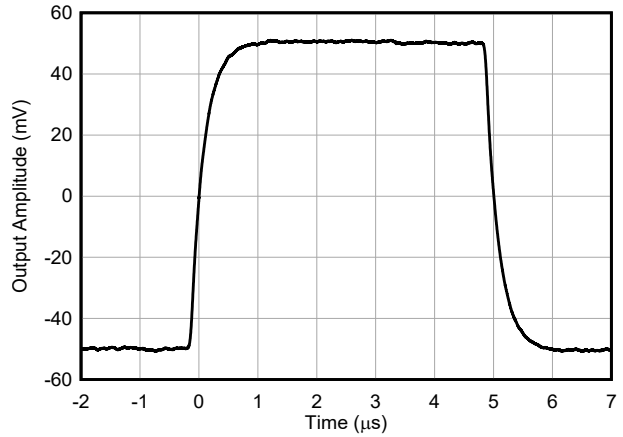
G = 1 V/V R_L = 10 kΩ C_L = 100 pF

图 7-47. Small-Signal Response for G = 1 V/V



G = 10 V/V R_L = 10 kΩ C_L = 100 pF

图 7-48. Small-Signal Response for G = 10 V/V



G = 1000 V/V R_L = 10 kΩ C_L = 100 pF

图 7-49. Small-Signal Response for G = 1000 V/V

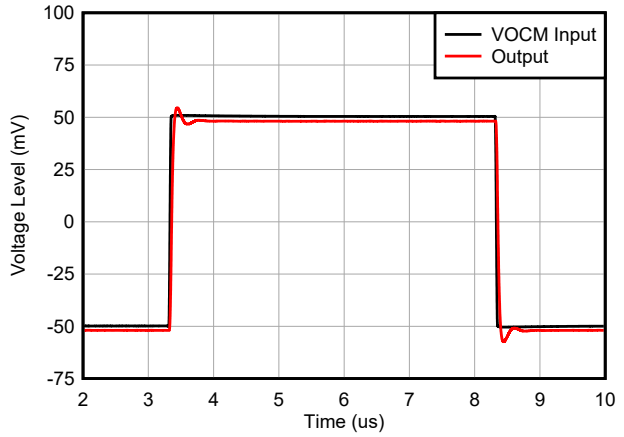


图 7-50. Small-Signal Response of VOCM Amplifier

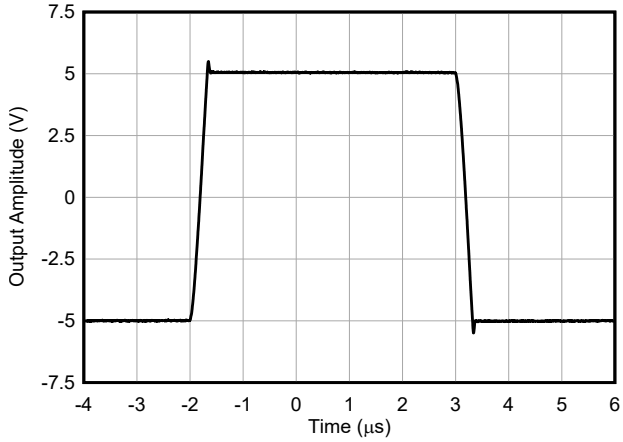


图 7-51. Large Signal Step Response

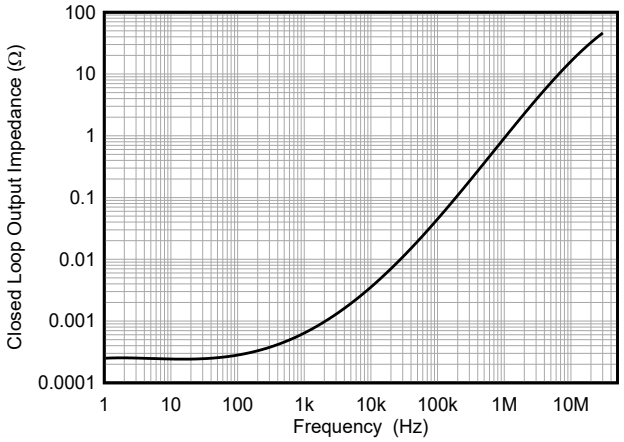


图 7-52. Closed-Loop Output Impedance

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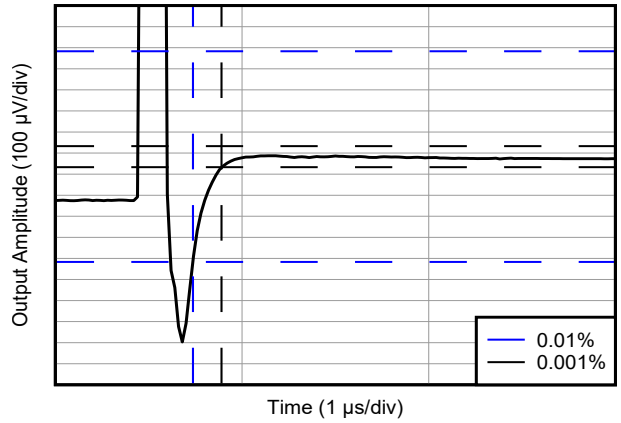
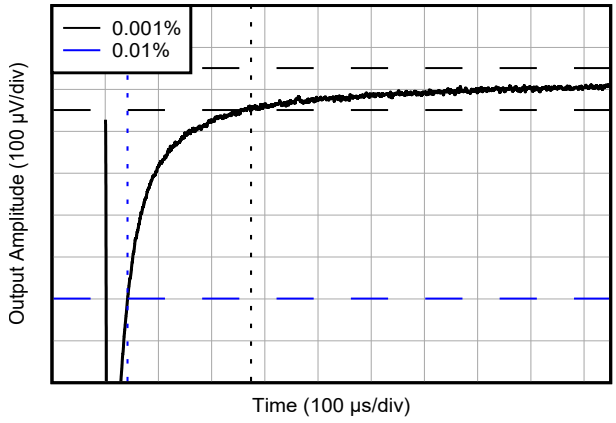
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{ICM} = V_{OCM} = midsupply, V_{CLAMP+} = V_{S+}, V_{CLAMP-} = V_{S-}, G = G_{IN} = G_{OUT} = 1 V/V, and R_L = 10 kΩ (unless otherwise noted)



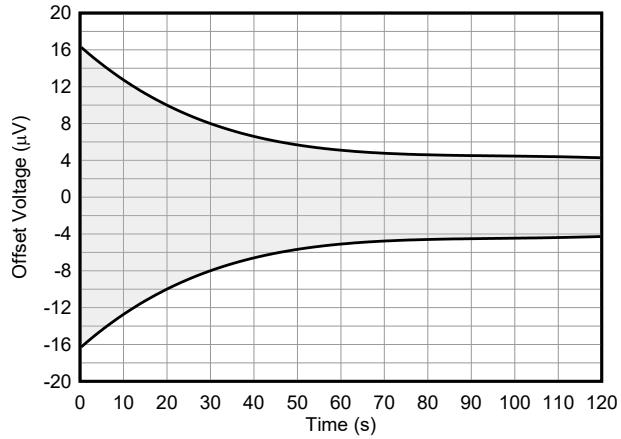
G = 0.2 V/V

图 7-53. Settling Time for G = 0.2 V/V



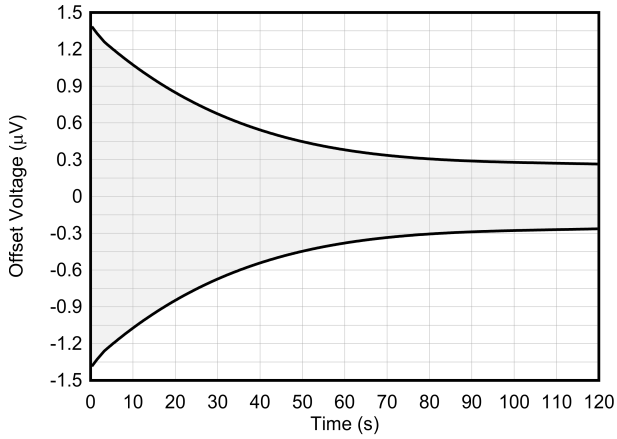
G = 1 V/V

图 7-54. Settling Time for G = 1 V/V



G = 1 V/V

图 7-55. Offset Warm-up for G = 1 V/V



G = 100 V/V

图 7-56. Offset Warm-up for G = 100 V/V

8 Detailed Description

8.1 Overview

The INA851 is a monolithic, precision instrumentation amplifier that incorporates a current-feedback input stage and a four-resistor, fully differential amplifier output stage. The schematic in 图 8-1 shows how the differential input voltage is buffered by Q_1 and Q_2, and is forced across R_G, which causes a signal current to flow through R_G, R_1, and R_2. The fully differential amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the VOCM pin. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V less than the input voltages.

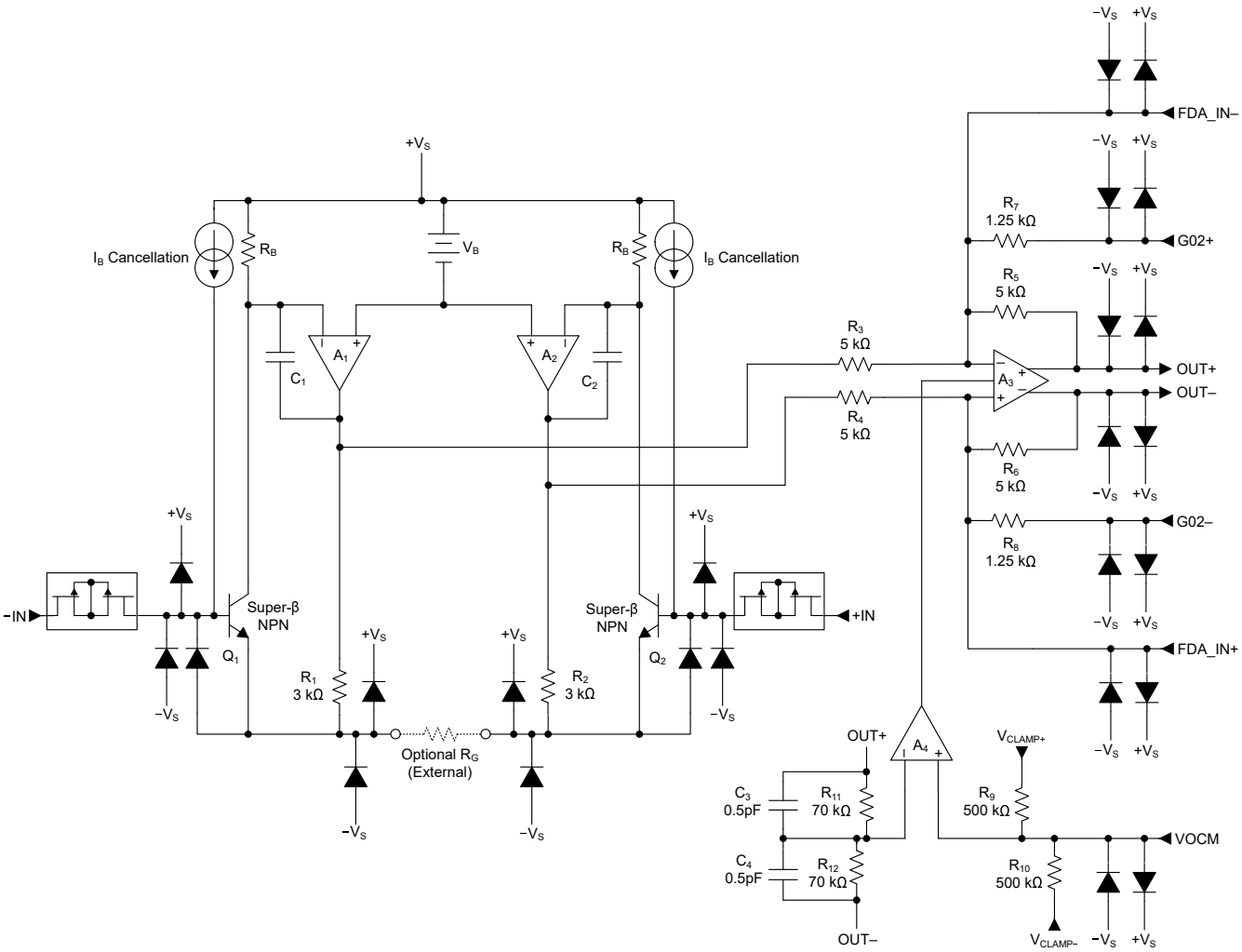


图 8-1. Detailed Schematic

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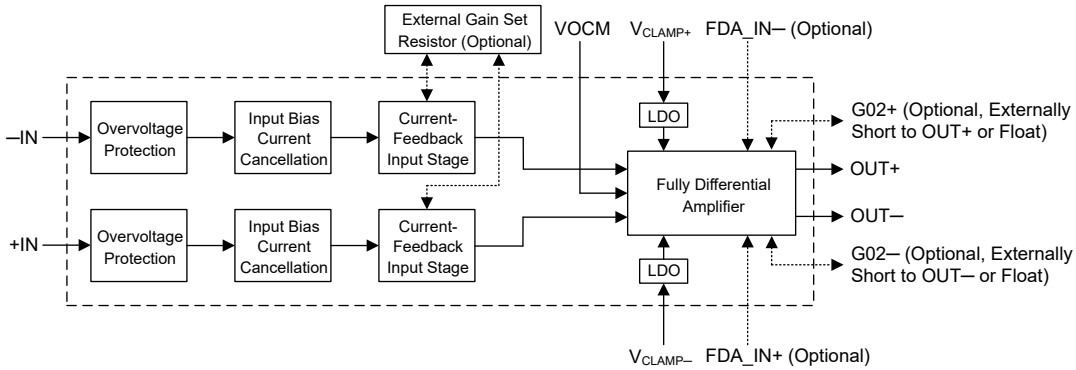
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjustable Gain Setting

图 8-2 shows that the INA851 input-stage gain is set by a single external resistor (R_G) connected between the RG pins. The gain of the output stage can be set to a unity gain of 1 V/V by floating the G02+ and G02 – pins, or to an attenuating gain of 0.2 V/V by shorting those pins to the respective OUT+ and OUT – pins.

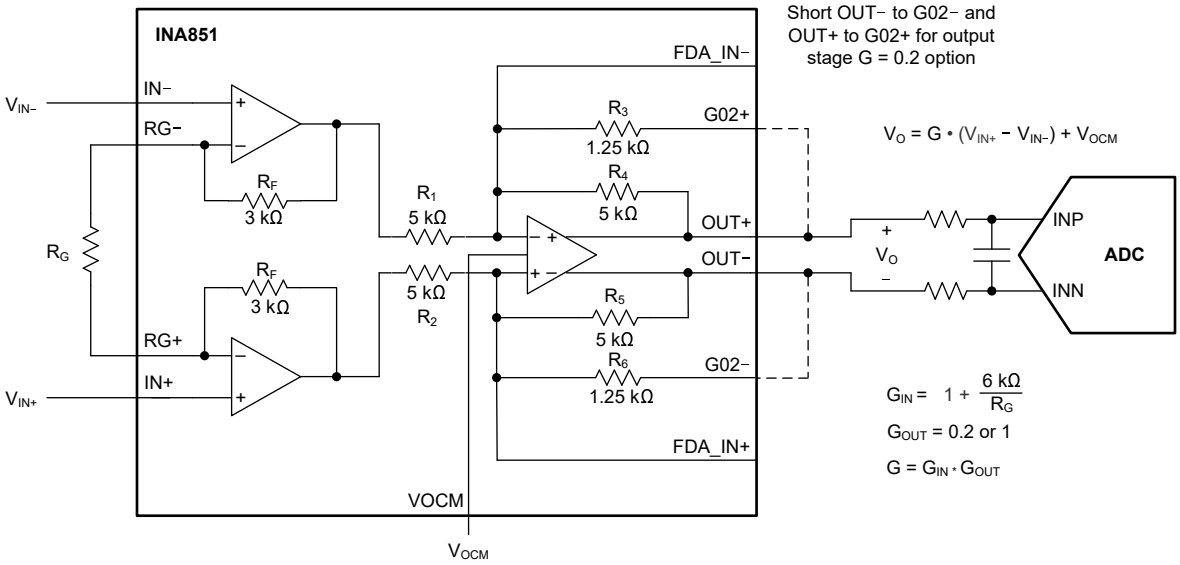


图 8-2. Simplified Diagram of the INA851 With Gain Equations

If the output stage is in the unity gain configuration, the value of R_G is selected according to the following equation:

$$G = \left(1 + \frac{6k\Omega}{R_G}\right) \tag{1}$$

When OUT+ is shorted to G02+ (pin 11 to pin 12) and OUT – is shorted to G02 – (pin 9 to pin 10) so that the output stage is in the attenuating configuration, the gain equation becomes:

$$G = 0.2 \times \left(1 + \frac{6k\Omega}{R_G}\right) \tag{2}$$

表 8-1 lists several commonly used gains and resistor values, as well as the additional gain error that is contributed by the gain resistors. The 6-kΩ term in the gain equation is a result of the sum of the two internal 3-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy

and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA851. The 5-kΩ and 1.25-kΩ resistors used in the output stage are ratiometrically matched to achieve stable 1-V/V and 0.2-V/V gain terms; although, the resistor values can shift up to 15%, depending on production.

表 8-1. Commonly Used Gains and Resistor Values

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G (Ω)	CALCULATED GAIN (V/V)	CONTRIBUTED GAIN ERROR (%)
0.2	NC, short OUT+ to G02+ and OUT – to G02 –	NC	0.200	N/A
0.5	4 k, short OUT+ to G02+ and OUT – to G02 –	4.02 k	0.499	0.30
1	NC	NC	1.000	N/A
2	6 k	5.97 k	2.005	– 0.25
5	1.5 k	1.5 k	5.000	0.00
10	666.67	665	10.023	– 0.23
20	315.79	316	19.987	0.06
50	122.45	124	49.387	1.23
100	60.61	60.4	100.338	– 0.34
200	30.15	30.1	200.336	– 0.17
500	12.02	12.1	496.868	0.63
1000	6.01	6.04	994.377	0.56
10000	600 m	604 m	9934.775	0.65

As shown in 图 8-2 and explained in more detail in 节 9.4, make sure to connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, and to place these capacitors as close as possible to the device pins.

8.3.1.1 Gain Drift

The stability and temperature drift of external gain setting resistor R_G also affects gain. The contribution of R_G to gain accuracy and drift is determined from 方程式 1. The best gain drift of 5 ppm/℃ (maximum) is achieved when the INA851 uses G = 1 in the input stage, without R_G connected. In this case, gain drift is limited by the mismatch of the temperature coefficient of the integrated resistors in fully differential amplifier A_3. When the output stage is in attenuating gain mode (OUT− shorted to G02− and OUT+ shorted to G02+), both the 1.25-kΩ and the 5-kΩ resistors contribute mismatch, as do the traces between the G02x and OUTx pins. Only the 5-kΩ resistors contribute mismatch when the output stage is in unity gain mode (with G02− and G02+ floating).

At input stage gains greater than 1, gain drift increases as a result of the individual drift of the 3-kΩ resistors in the feedback of A_1 and A_2, relative to the drift of external gain resistor R_G. The low temperature coefficient of the internal feedback resistors improves the overall temperature stability of applications using input-stage gains greater than 1 V/V over alternate solutions. The low resistor values required for high gain make wiring resistance an important consideration. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 20 or greater. To maintain stability, avoid parasitic capacitance of more than a few picofarads at the R_G connections. Careful matching of any parasitics on the R_G pins maintains optimal CMRR over frequency.

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8.3.2 Offset Voltage

Low offset voltage is one of the key parameters for an instrumentation amplifier (INA). In a current-feedback INA, this error source is classified in three stages: input, output, and intermediate. The input-stage dc offset (V_{OSI}) is mainly caused by the mismatch of the input transistors Q1 and Q2, (see 图 8-1). The output-stage dc offset (V_{OSO}) is caused partially by the mismatch of the output amplifier A3. In the INA851, A3 is a fully-differential amplifier and gained up by the noise gain of the circuit (1 + R_5 / R_3). An additional intermediate stage offset contribution error adds to V_{OSO} that is caused by the mismatch of the current mirrors in the front end (through R1 and R2).

Unlike typical instrumentation amplifiers that incorporate a difference amplifier (A3) with a fixed output gain, the INA851 has two different output gain stages that subsequently contribute differently to V_{OSO}; see Gaussian distributions for G = G_{OUT} = 1 V/V in 图 7-3 and for G = G_{OUT} = 0.2 V/V in 图 7-4.

The following equation calculates the total offset voltage error referred to the input:

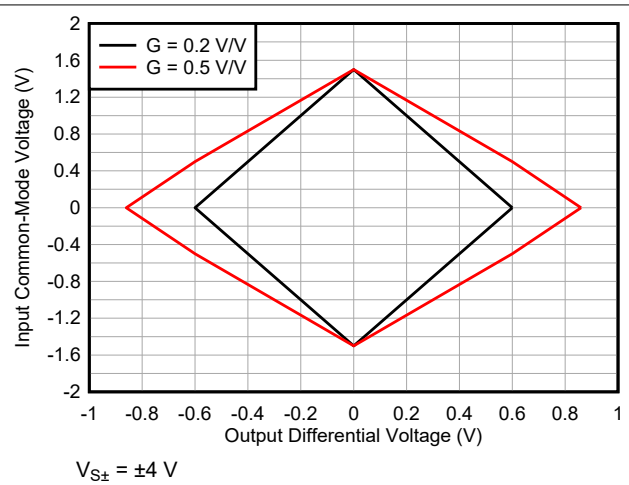
$$V_{OS} = \sqrt{{V_{OSI}}^2 + \left(\frac{V_{OSO(G_{OUT} = 1 \text{ or } G_{OUT} = 0.2)}}{G_{IN}}\right)^2} \tag{3}$$

8.3.3 Input Common-Mode Range

The linear input voltage range of the INA851 input circuitry extends within 2.5 V (maximum) of both power supplies, and maintains excellent common-mode rejection throughout this range. The valid input common-mode range is a function of the input common-mode voltage, input differential voltage, gain, and output common-mode voltage.

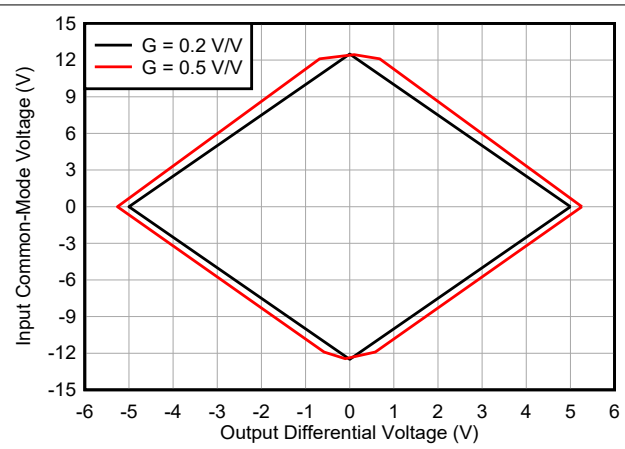
The common-mode range is best calculated using the *INA851 Input-Output Range Design Calculator* .

The common-mode range for the most common operating conditions are shown in 图 8-3 to 图 8-9.



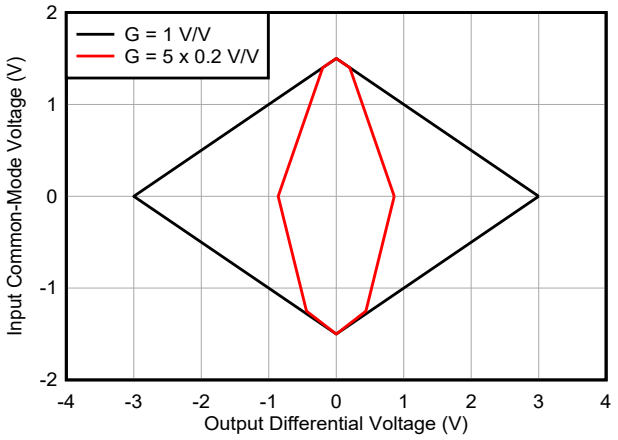
$V_{S\pm}$ = ±4 V

图 8-3. Input Common-Mode Voltage vs Output Voltage, Low Gains



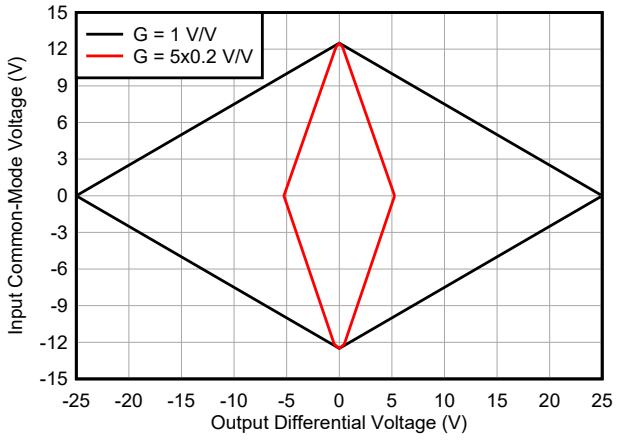
$V_{S\pm}$ = 15 V

图 8-4. Input Common-Mode Voltage vs Output Voltage, Low Gains



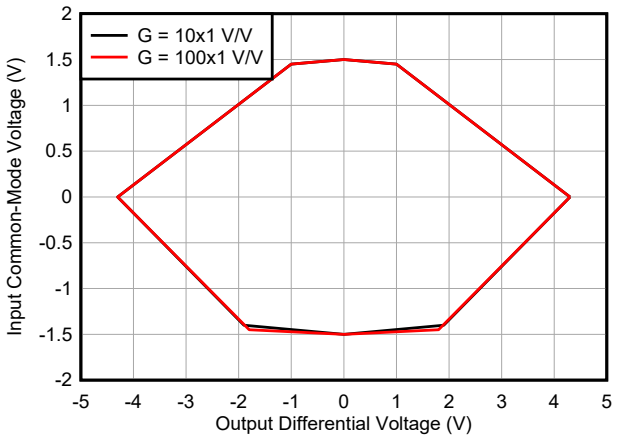
$V_{S\pm}$ = ±4 V

图 8-5. Input Common-Mode Voltage vs Output Voltage, Unity-Gain



$V_{S\pm}$ = ±15 V

图 8-6. Input Common-Mode Voltage vs Output Voltage, Unity-Gains



$V_{S\pm}$ = ±4 V High Gains

图 8-7. Input Common-Mode Voltage vs Output Voltage, High Gains

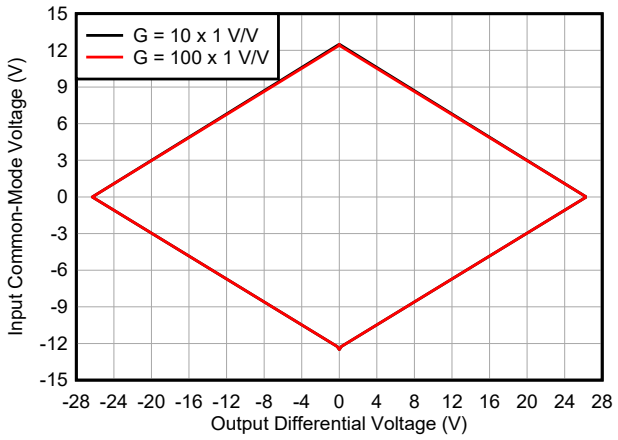
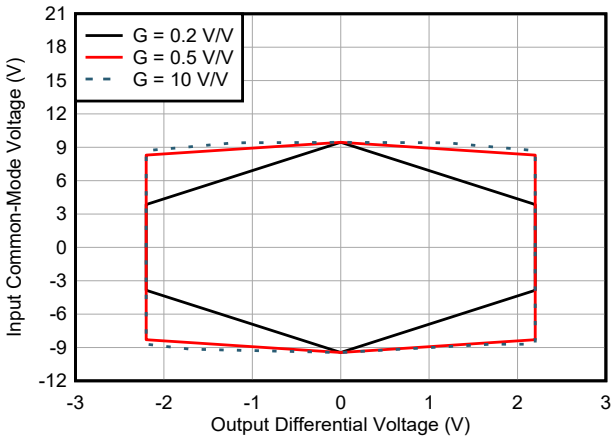


图 8-8. Input Common-Mode Voltage vs Output Voltage, High Gains



$V_{S\pm}$ = ±12 V V_{clamp+} = 5 V, V_{clamp-} = GND

图 8-9. Input Common-Mode Voltage vs Output Voltage With Output Clamping

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8.3.4 Input Protection

The inputs of the INA851 device are individually protected for voltages up to ±40 V beyond the power supply rails. For example, a condition of V_{S-} = –55 V on one input and V_{S+} = 55 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. 图 8-10 shows that if the input is overloaded, the protection circuitry limits the input current to a value of approximately 16 mA.

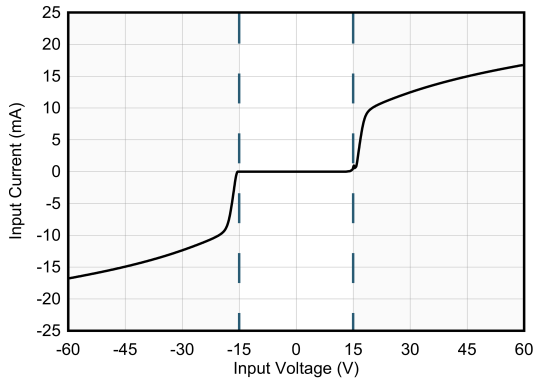

图 8-10. Input Current During an Overvoltage Condition

图 8-11 shows that during an input overvoltage condition, current flows through the input protection diodes into the power supplies. If the power supplies are unable to sink current, then place Zener diode clamps (ZD1 and ZD2 in 图 8-11) on the power supplies to provide a current pathway to ground.

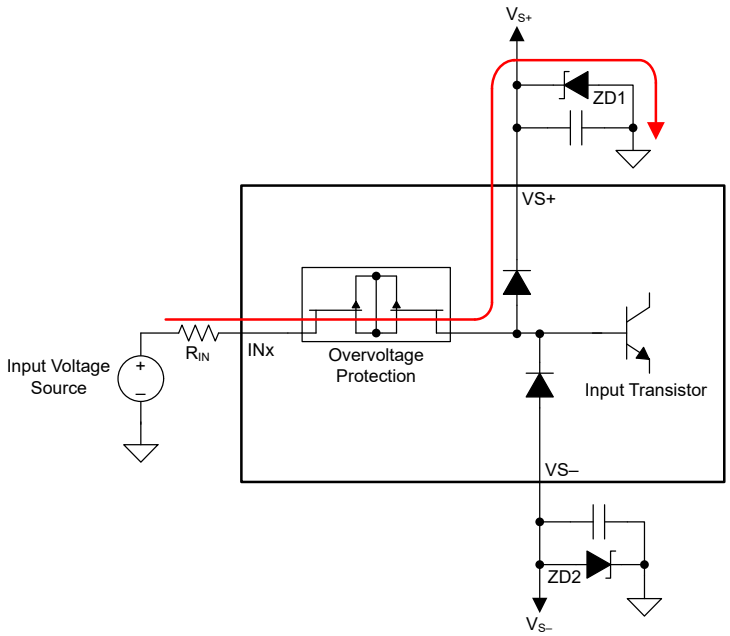

图 8-11. Input Current Path During an Overvoltage Condition

If an input stage gain greater than G_{IN} = 1 V/V is implemented, where a gain resistor is present across the RG pins, the inputs are still well protected against overvoltage conditions; however, make sure that the input differential voltage limitations of the INA851 are not exceeded. For example, a condition of (V_{S+}) + 40 V on both inputs does not cause damage. However, a condition of (V_{S-}) – 40 V on one input and (V_{S+}) + 40 V on the other input can cause damage. Precautions can include the use of external resistors in series with each of the inputs.

8.3.5 Output Clamping

The INA851 features a unique output clamping function that protects the downstream device against damage that results from inadvertent over-driving. Usually the downstream device is an ADC that typically operates at a lower supply voltage than the INA851.

To implement this function, use the VCLAMP+ and VCLAMP– pins to limit the supply voltage range of the differential output drive amplifier. For typical operation, use a low-impedance connection from the pins to the power supplies of the ADC. For proper operation of the clamp circuitry, set the V_{S+} or V_{S-} supply voltages at least 1.5 V beyond the respective V_{CLAMP+} and V_{CLAMP-} clamping voltages. In addition, for the output driver to function correctly, the V_{CLAMP+} and V_{CLAMP-} voltages must be at least 3 V apart. If the output clamping functionality is not desired, short the VCLAMP+ and VCLAMP– pins to the amplifier VS+ and VS– supply pins.

The output driver operates up to the V_{CLAMP+} or V_{CLAMP-} limits without experiencing distortion. When the clamping function is in use the output voltage is clamped at approximately 600 mV beyond the clamp voltage.), so that the device output spans the full input range of the ADC. However, if the predriver output swings beyond the V_{CLAMP+} or V_{CLAMP-} voltage, the output driver begins to run out of headroom as a result of the clamped supply voltage, shown in 图 8-12.

The output is unable to swing greater than approximately 500 mV beyond the V_{CLAMP+} or V_{CLAMP-} voltage (at zero load), helping prevent or reduce damage to the ADC from overvoltage conditions.

The linear operation becomes distorted when the driver load becomes higher than 20 mA, see 图 8-13.

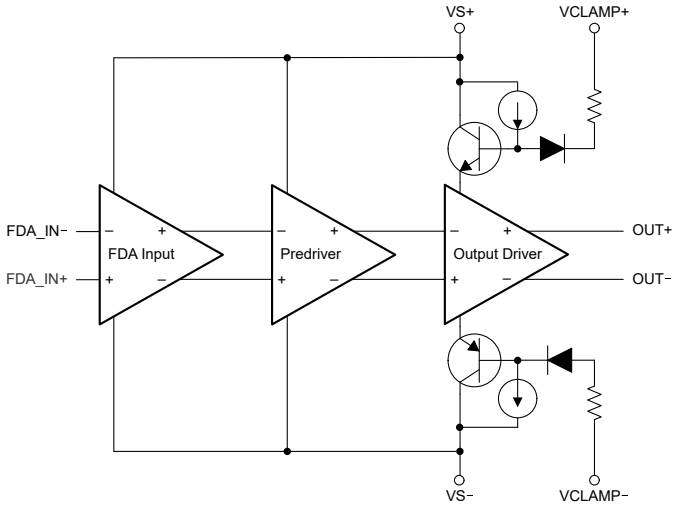

图 8-12. Simplified Schematic of Output Driver Clamping Structure

备注

Be aware that instead of providing an immediate *hard-stop* voltage limit, the output driver is not clamped until V_{CLAMP+} or V_{CLAMP-} voltage has been exceeded, and the driver starts to run out of headroom. This configuration prevents distortion of the amplifier output when operating near the V_{CLAMP+} and V_{CLAMP-} rails. However, the output voltage exceeds V_{CLAMP+} and V_{CLAMP-} by several hundreds of millivolts before the clamps turn on strongly. When used in conjunction with several tens of ohms of resistance between the amplifier output and ADC input pins (commonly implemented as part of a low-pass filter for proper ADC acquisition), output clamping helps severely diminish any potential damage to the ADC that can otherwise result.

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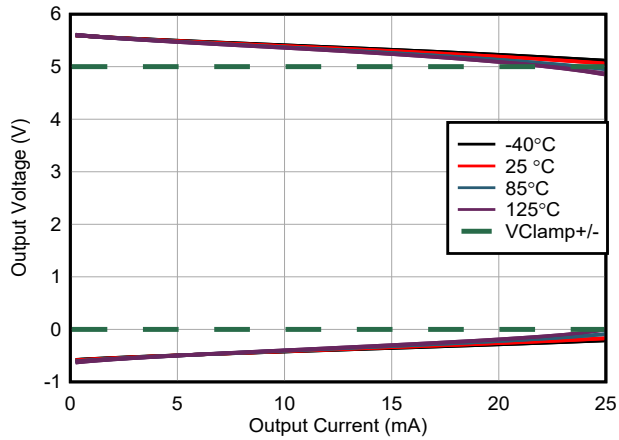

图 8-13. Output Voltage With Output Clamping Enabled

The VCLAMP+ pin features a fail-safe against power-up sequencing issues between the INA851 and a downstream device. For example, a condition of $V_{(CLAMP+)}$ + 10 V on this pin does not cause damage. Therefore, the ADC supply can safely turn on while the INA851 supply is still off or just beginning to turn on. In this case, the current draw through the VCLAMP+ pin is limited to a safe value of typically 3 mA.

8.3.6 Low Noise

An output noise calculation helps design a low-noise circuit to drive high-precision ADC applications and optimize the signal-to-noise ratio (SNR).

图 8-14 shows a simplified noise model for the INA851. The e_{NO} noise refers to the input resistor network of the FDA. This term incorporates the thermal noise of the internal feedback resistors, and the interaction of the internal current noise density of the output stage with the internal feedback resistors.

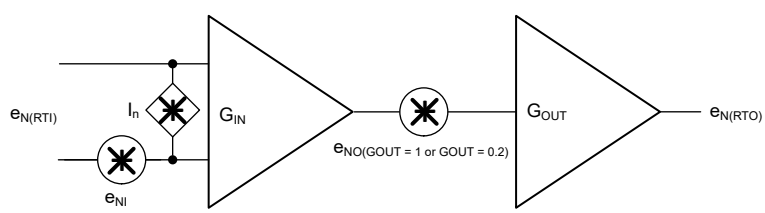

图 8-14. Simplified Noise Model for the INA851

The internal feedback resistor network is considered in the e_{NO} specification; therefore, the calculation of the total input-referred noise, $e_{N(RTI)}$, is simplified to the following equation:

$$e_{N(RTI)} = \sqrt{{e_{NI}}^2 + \left(\frac{e_{NO(G_{OUT} = 1 \text{ or } G_{OUT} = 0.2)}}{G_{IN}}\right)^2} \tag{4}$$

The total output-referred noise, $e_{N(RTO)}$, multiplies directly by the output stage gain, G_{OUT}, by G_{OUT} = 0.2 V/V or G_{OUT} = 1 V/V respectively, as shown in the following equation:

$$e_{N(RTO)} = \sqrt{\left(e_{NI} \times G_{IN} \times 0.2\text{ V/V or } 1\text{ V/V}\right)^2 + \left(e_{NO(G_{OUT} = 1 \text{ or } G_{OUT} = 0.2)} \times 0.2\text{ V/V or } 1\text{ V/V}\right)^2} \tag{5}$$

8.4 Device Functional Modes

The INA851 has a single functional mode and operates when the power-supply voltage is greater than 8 V (±4 V). The maximum power-supply voltage for the INA851 is 36 V (±18 V).

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.1.1 Output Common-Mode Pin

The output voltage of the INA851 is developed with respect to the voltage on the output common-mode pin, VOCM. The starting point for most designs is to assign an output common-mode voltage for the INA851. For ac-coupled signal paths, this voltage is often the default midsupply voltage, so as to retain the most available output swing around the voltage centered at V_{OCM}. For dc-coupled signal paths, set this voltage between a minimum of V_{S+} – 2.5 V and maximum of V_{S-} + 2.5 V. For precision ADC applications, this voltage is typically the input common mode voltage of the ADC.

The voltage at the VOCM pin is internally buffered to bias the fully differential output amplifier, eliminating the need for an additional external V_{OCM} buffer. While the buffer input is high-ohmic, the VOCM pin also connects through internal 500-kΩ resistors to V_{CLAMP+} and V_{CLAMP-}, which sets the output common-mode voltage to midsupply in the event that the pin is floating.

While the V_{OCM} buffer has high small-signal bandwidth, be aware that large-signal steps with fast edges at the VOCM pin cause delays in the output. For best tracking between the buffer input and output signals, use rise times of 200 ns or greater for large steps.

9.1.2 Output-Stage Gain Selection and Noise-Gain Shaping

In the default unity-gain configuration, the INA851 fully differential amplifier output stage uses 5-kΩ feedback resistors between the OUT+ and OUT– outputs and the inverting and noninverting inputs, respectively. However, the INA851 also features internal 1.25-kΩ feedback resistors between those inputs and the G02+ and G02– pins. By shorting the G02+ pin to the OUT+ pin, and the G02– pin to the OUT– pin, the amplifier is placed in an attenuating gain of 0.2 V/V.

Additionally, access directly to the inverting and noninverting inputs of the fully differential amplifier is provided through the FDA_IN– and FDA_IN+ pins, respectively. This option allows circuit designers to add external feedback capacitors in parallel with the internal feedback resistors to implement noise filtering or noise-gain shaping techniques. These pins can also be used to implement customized attenuating gains for the output stage. Do not treat these pins as outputs, nor use the pins to source or sink current.

备注

These pins are internally disconnected on preliminary samples of the INA851; these pins will be connected to the aforementioned internal nodes in the final device release.

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9.1.3 Input Bias Current Return Path

The input impedance of the INA851 is very high at approximately 1 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 5 nA. High input impedance means that this input bias current changes very little with varying input voltage.

For proper operation, input circuitry must provide a path for input bias current. 图 9-1 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA851, and the input amplifiers saturate. If the differential source resistance is low, the thermocouple example in 图 9-1 shows that the bias current return path can connect to one input. With a higher source impedance, using two equal resistors provides a balanced input with the possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

For more details about why a valid input bias current return path is necessary, see the *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application report.

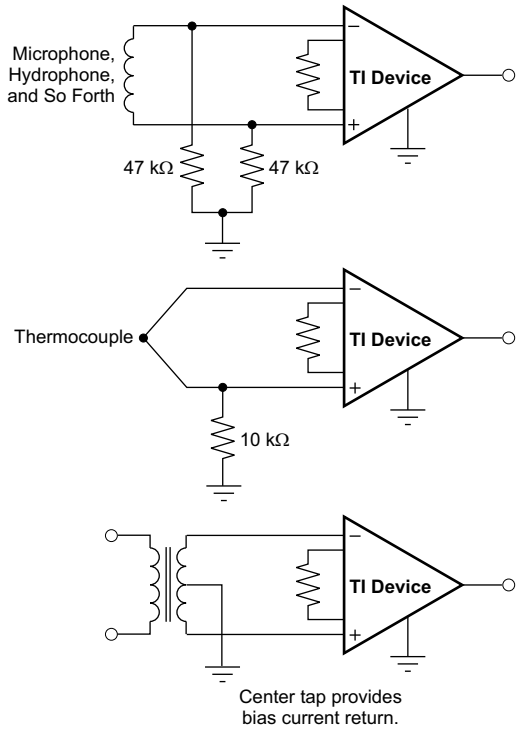

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图 9-1. Providing an Input Common-Mode Current Path

9.1.4 Thermal Effects due to Power Dissipation

The INA851 dissipates approximately 180 mW of power under quiescent conditions at a ±15-V supply voltage. The internal resistor network and output load drive causes an additional power dissipation that depends on the input signal. The small silicon area of the INA851 causes the internal circuitry to experience temperature gradients that can adversely affect the electrical performance.

Precision parameters, such as offset voltage, linearity, common-mode rejection ratio, and total harmonic distortion, can be impacted as a result of these thermal effects in the silicon. The thermal gradient particularly affects the performance of low-frequency input signals with higher gains (> 10) and large output voltage variation. 图 9-2 shows that the thermal effect can be minimized by lowering the supply voltage, if the application permits.

To properly dissipate heat from the INA851, connect the thermal pad with sufficient thermal vias to a large copper plane that is connected to the negative supply, VS–. A thorough PCB layout is of key importance (see also 节 9.4).

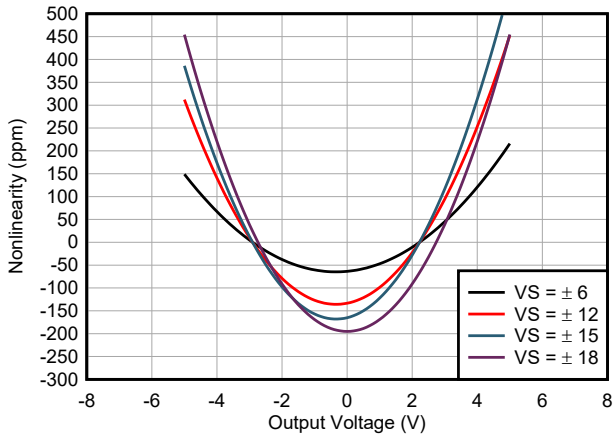

图 9-2. Linearity vs Supply Voltage for G = 1000

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9.2 Typical Applications

9.2.1 Three-Pin Programmable Logic Controller (PLC)

图 9-3 shows a three-pin programmable-logic controller (PLC) design for the INA851. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a differential voltage of ±4.95 V with a V_{OCM} of 2.5 V (or 25 mV to 4.975 V on OUT+ and OUT−) to be measured by the ADS8920B SAR ADC.

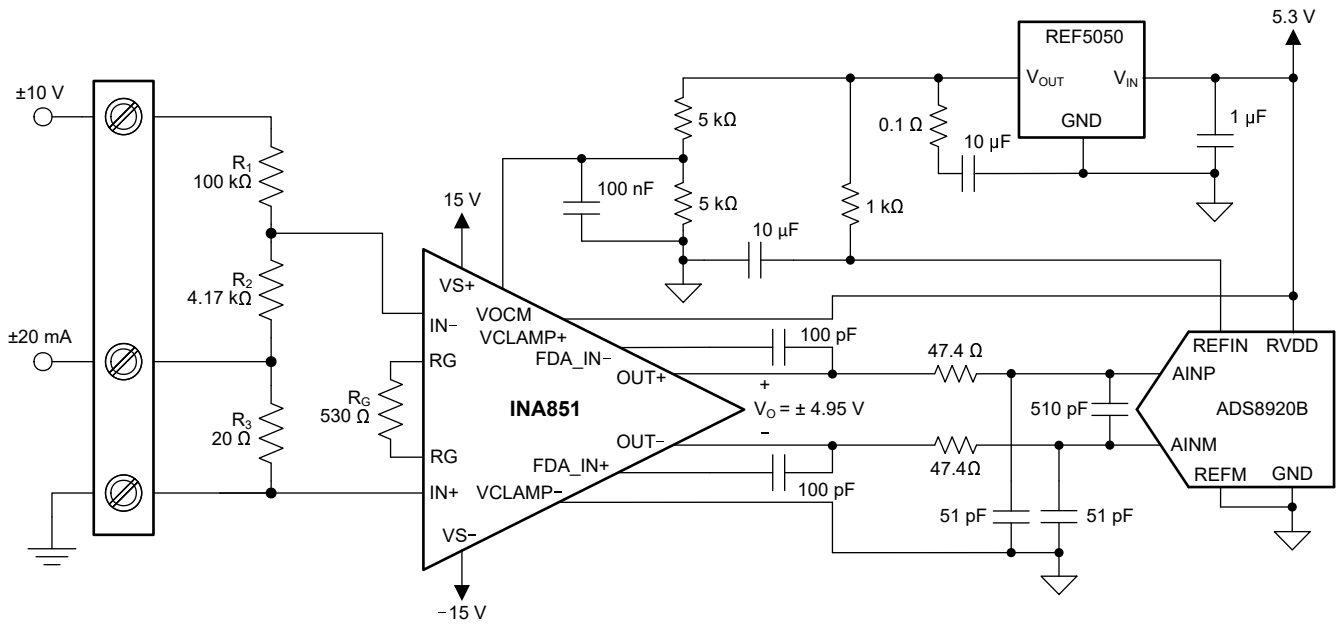

图 9-3. PLC Input with INA851 (±10 V, 4 mA to 20 mA)

9.2.1.1 Design Requirements

For this application, the design requirements are as follows:

- 4-mA to 20-mA input with less than 20-Ω burden
- ±20-mA input with less than 20-Ω burden
- ±10-V input with impedance of approximately 100 kΩ
- Maximum 4-mA to 20-mA or ±20-mA burden voltage equal to ±0.4 V
- Output range within 0 V to 5 V

9.2.1.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in 图 9-3: current input and voltage input. This design requires R_1 >> R_2 >> R_3. Given this relationship, the following equation calculates the current input mode transfer function.

$$V_{OUT} = V_{DIFF} \times G = -(I_{IN} \times R_3) \tag{6}$$

where

- V_{OUT} represents the differential voltage at the INA851 outputs in current input mode.
- V_{DIFF} represents the differential voltage at the INA851 inputs.
- G represents the total gain of the INA851
- I_{IN} is the input current to the PLC.

The following equation shows the transfer function for the voltage input mode:

$$V_{OUT} = V_{DIFF} \times G = -\left(V_{IN} \times \left(\frac{R_2}{R_2 + R_1}\right)\right) \tag{7}$$

where

- V_{OUT} represents the differential voltage at the INA851 outputs in voltage input mode.
- V_{IN} is the input voltage to the PLC.

The voltages on the output pins of the INA851 follow the relationships in 方程式 8 and 方程式 9.

$$V_{OUT+} = V_{DIFF} \times \frac{G}{2} + V_{OCM} \tag{8}$$

$$V_{OUT-} = -V_{DIFF} \times \frac{G}{2} + V_{OCM} \tag{9}$$

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. The R_1 value is 100 kΩ because increasing the R_1 value also increases noise. The value of R_3 must be extremely small compared to R_1 and R_2. A 20-Ω value is selected for R_3 because that resistance value is much smaller than R_1 and yields an input voltage of ±400 mV when operated in current mode (±20 mA).

Use 方程式 10 to calculate R_2 given V_{DIFF} = ±400 mV, V_{IN} = ±10 V, and R_1 = 100 kΩ.

$$V_{DIFF} = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_{DIFF}}{V_{IN} - V_{DIFF}} = 4.167\ \text{k}\Omega \tag{10}$$

The value obtained from 方程式 10 is not a standard 0.1% value; therefore, 4.17 kΩ is selected. R_1 and R_2 also use 0.1% tolerance resistors to minimize error.

Use 方程式 11 to calculate the gain of the instrumentation amplifier.

$$G = \frac{V_{OUT}}{V_{DIFF}} = \frac{4.95\ \text{V}}{400\ \text{mV}} = 12.375\ \text{V/V} \tag{11}$$

方程式 12 calculates the gain-setting resistor value using the INA851 gain equation for G_{OUT} = 1 V/V (方程式 1).

$$R_G = \frac{6\ \text{k}\Omega}{G-1} = \frac{6\ \text{k}\Omega}{12.375 - 1} = 527.473\ \Omega \tag{12}$$

Use a standard 0.1% resistor value of 530 Ω for this design.

The ADS8920B is selected because of the differential input, 1-MSPS sampling rate, and integrated reference buffer. Implement the antialiasing R-C-R filter using two 47.4-Ω resistors, a COG or NPO-type 510-pF differential capacitor, and two ceramic 51-pF common-mode capacitors. The REF5050 is selected to create a 5-V reference voltage for the ADC. Use well-matched precision resistors to create a voltage divider that generates a stable 2.5-V V_{OCM} reference. Connect the VCLAMP+ and VCLAMP− pins of the INA851 to the supplies of the ADC to protect against overdrive damage in the event of a fault. Consider implementing a TVS diode from the ADC supply to GND for additional protection, and include 100-nF decoupling capacitors between the amplifier and ADC supplies and GND.

9.2.1.3 应用曲线

图 9-4 和图 9-5 展示了图 9-3 中电路的典型特性曲线。

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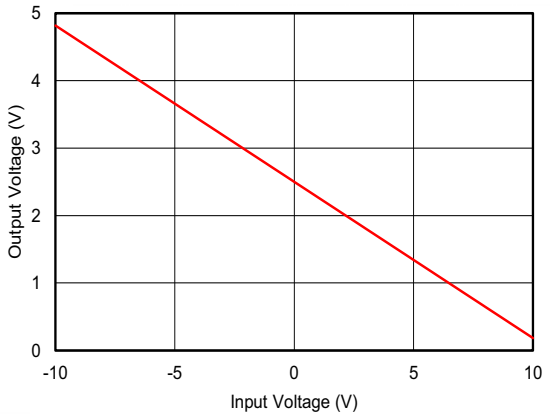

图 9-4. PLC 输出电压与输入电压之间的关系

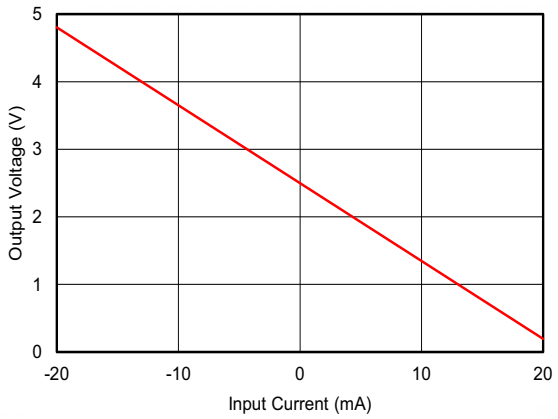

图 9-5. PLC 输出电压与输入电流间的关系

9.2.2 20-Bit, 1-MSPS ADS8900B Driver Circuit With FDA Noise Filter

The application circuit in 图 9-6 shows the schematic of a complete input and reference driver circuit for the ADS8900B, a 20-bit, precision, 1-MSPS, successive approximation register (SAR), analog-to-digital converter (ADC). This circuit is used to measure the driving capability of the INA851 with the ADS8900B ADC.

To test the complete dynamic range of the circuit, the common-mode voltage V_{OCM} of the input of the ADC is established at a value of V_{REF} / 2.

To exclude noise caused by supply voltage, the test circuit uses the TPS7A4700, a low-noise 4-µVRMS, RF LDO voltage regulator, to generate the 5.2-V supply rail.

For V_{OCM}, the circuit uses the REF5050, a low-noise, low-drift, 5-V reference, a 20k-20k voltage divider to establish VREF/2 and an additional RC filter (10 Ω, 150 pF) into the VOCM pin. See also the ADS8900EVM-PDK user's guide.

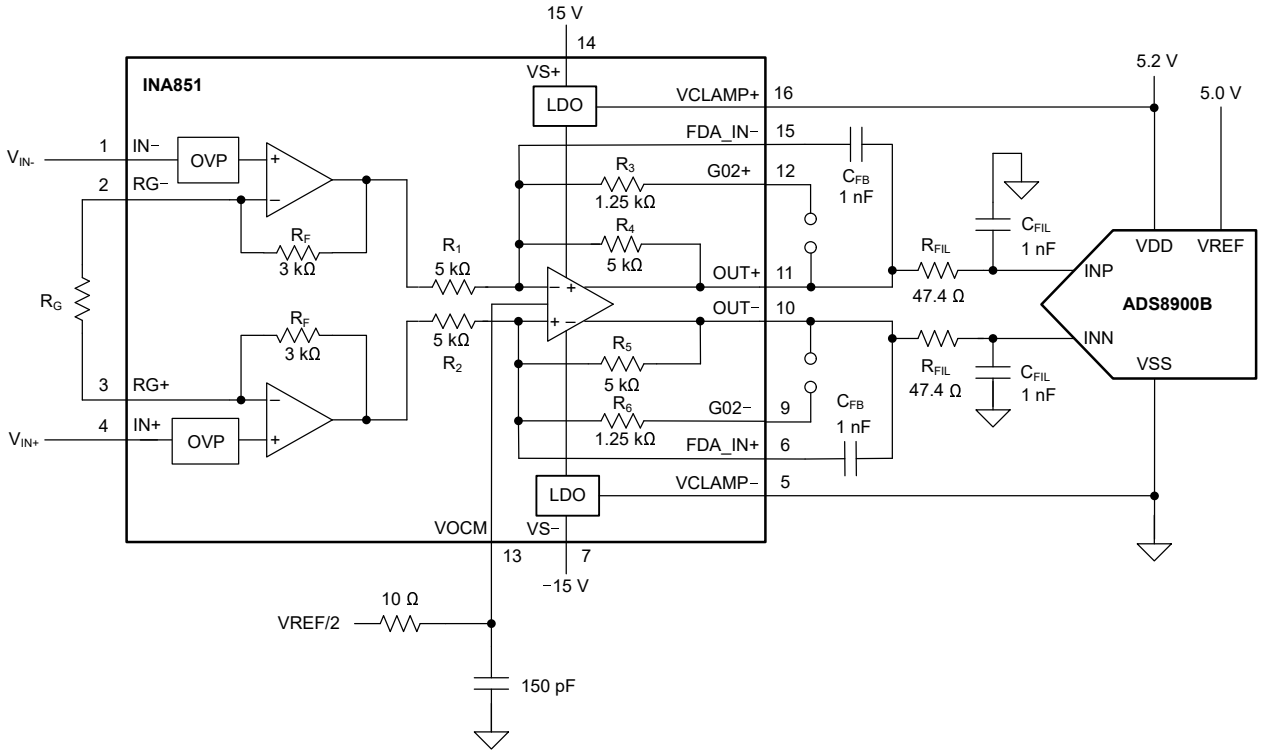

图 9-6. Driving ADS8900B With FDA Noise Filter

9.2.2.1 Design Requirements

The requirements for the application driving the ADS8900B ADC are listed in the following table.

表 9-1. Design Parameters

PARAMETER	VALUE
Differential to differential conversion	V_{INDIFF} to $V_{OUTDIFF}$
Supply voltages	VS± = ± 15 V, VDD = 5.2 V, VREF = 5 V
Full-scale range of ADC for FSR	FSR = ± 5 V
Driver configuration	See 表 9-2
Circuit bandwidth	$f_{(-3dB)}$ = 31.7 kHz
Output RC elements	See ADS8900B input requirements

To eliminate ground loops, unwanted parasitic effects, and distortion, use appropriate PCB layout and grounding techniques (see also 节 9.4).

9.2.2.2 Application Curves

表 9-2 show the typical signal-to-noise (SNR) and total harmonic distortion (THD) of the INA851 driving the ADS8900B SAR ADC at full-scale range and at different gain configurations. The RC filter combination (R_{FIL}, C_{FIL}) shown in 图 9-6 helps attenuate the nonlinear charge kickback of the ADC and optimize for best THD performance. The combination of the RC filter and the feedback capacitor C_{FB} allow for the best trade-off between harmonic distortion and maintaining stability of the FDA. Low voltage-coefficient C0G capacitors are used everywhere in the signal path (C_{FB}, C_{FIL}) for the low-distortion properties.

For other bandwidth requirements, adjust the feedback capacitor accordingly, and verify the circuit performance using a SPICE simulation using the INA851 TINA-TI™ SPICE Model. The amplifier output voltage must settle within the ADC bit accuracy during the ADC acquisition time window. Verify the desired circuit is stable; that is, the FDA has more than a 45º phase margin.

表 9-2. INA851 + ADS8900B FFT Data Summary

INPUT AMPLITUDE (Vpk)	RG RESISTOR (Ω)	G_{IN} (V/V)	G_{OUT} (V/V)	SNR (dB)	THD (dB)	ENOB (Bits)
23.7378	None	1	0.2	100.7	–117.3	16.42
4.7476	None	1	1	100.6	–122.7	16.41
0.2374	316	20	1	99.1	–112.0	16.10
0.0475	60.4	100	1	91.1	–99.0	14.64

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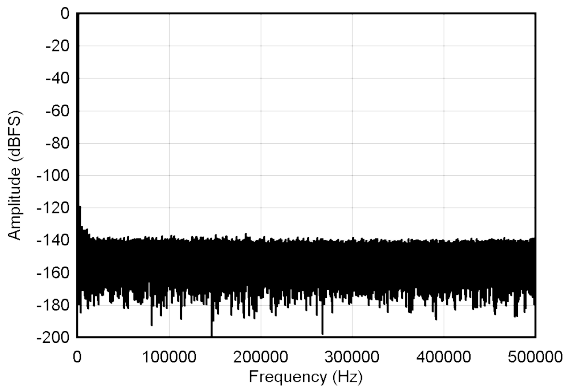
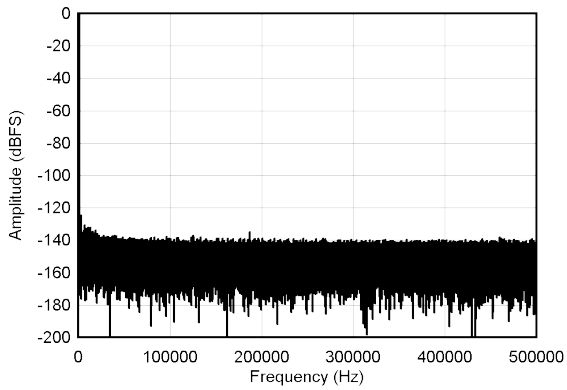


G = 0.2 V/V, f_{IN} = 1 kHz, SNR = 100.73 dB, THD = –117.28 dB

图 9-7. Noise Performance FFT Plots for G = 0.2 V/V



G = 1 V/V, f_{IN} = 1 kHz, SNR = 100.6 dB, THD = –122.74 dB

图 9-8. Noise Performance FFT Plots for G = 1 V/V

9.2.3 24-Bit, 200 kSPS, Delta-Sigma ADS127L11 ADC Driver Circuit With FDA Noise Filter

The application circuit in 图 9-9 shows an schematic for a 24-bit-precision, 200-kSPS, delta-sigma, ADC. The circuit is used to measure the driving capacity of the INA851 with the ADS127L11 ADC.

The ADS127L11 ADC offers two digital filters to optimize for ac applications (wideband filter) or dc applications (Sinc4 filter). Application Curves shows measurement results in both filter settings. For detailed design procedure to operate the ADS127L11 ADC, see the ADS127L11EVM-PDK evaluation module.

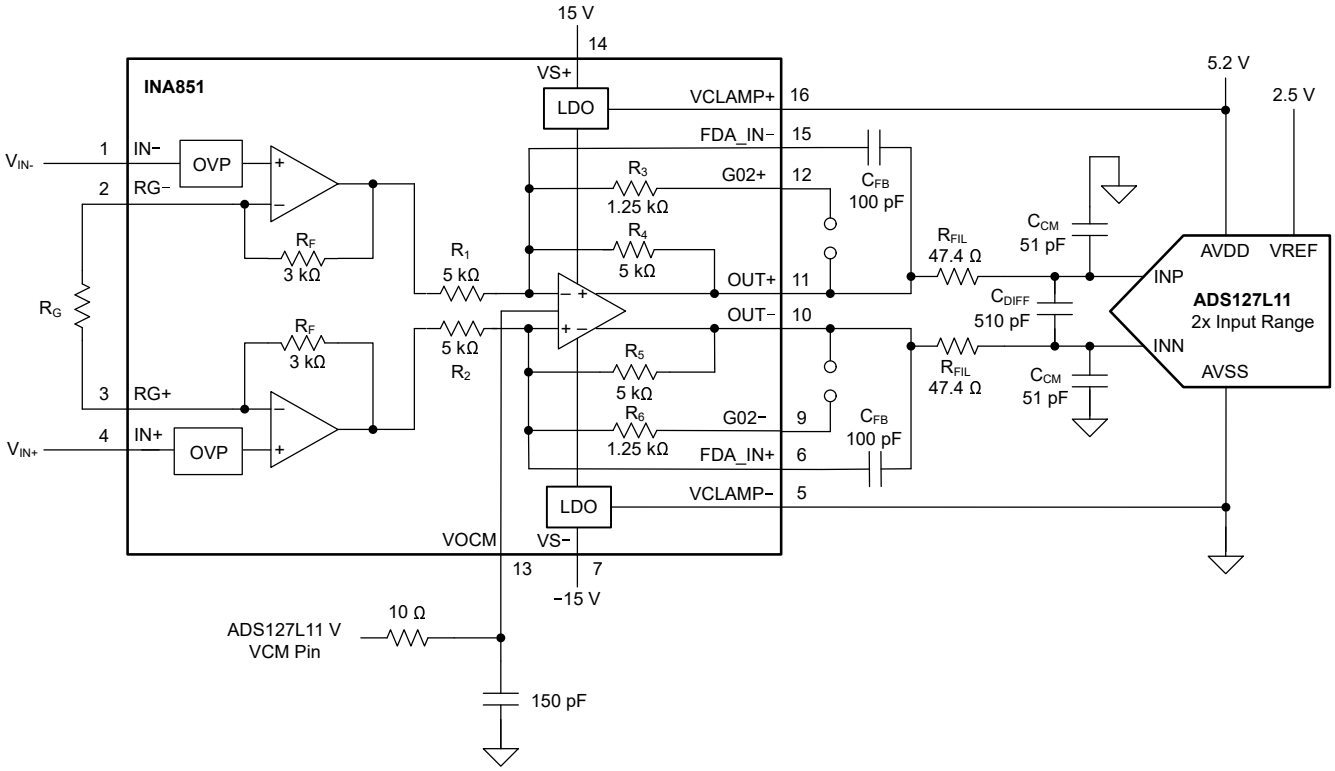


图 9-9. Driving the Delta-Sigma ADC ADS127L11

9.2.3.1 Design Requirements

The design requirements for the application driving the ADS127L11 ADC are listed in the following table.

表 9-3. Design Parameters

PARAMETER	VALUE
Differential-to-differential conversion	V_{INDIFF} to $V_{OUTDIFF}$
Supply voltages	VS± = ±15 V, AVDD = 5.2 V, VREF = 2.5 V
Full-scale range of ADC for FSR	FSR = ± 5 V
Data rate of ADC	f_{DATA} = 187.5 kSPS
ADC filter configuration	(1) High-speed mode, Sinc4 filter, OSR = 64
	(2) High-speed mode, wideband filter, OSR = 64
INA gain and filter configuration	See 表 9-4 and 表 9-5
Signal frequency	f_{IN} = 1 kHz
RC kickback filter(1)	R_{FIL} = 47.4 Ω + C_{DIFF} = 510 pF + R_{FIL} = 47.4 Ω, C_{FIL} = 51 pF

(1) A trade-off must be considered between THD, frequency response and drift. The differential current drift into the ADC can interact with this filter resistors and result in higher drift errors. However, low resistance degrades the phase margin of the INA851. For low drift applications, keep R_{FIL} < 50 Ω.

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For optimized linearity and THD performance, use good printed circuit board (PCB) layout practice. For proper heat dissipation of the INA851, connect the thermal pad to a plane or a large copper pour at the bottom connected to VS– (see also 节 9.4.2).

9.2.3.2 Application Curves

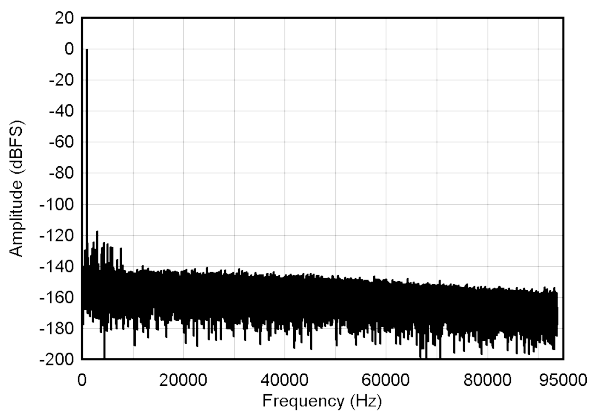
表 9-4 and 表 9-5 show the typical signal-to-noise (SNR) and total harmonic distortion (THD) of the INA851 driving the ADS127L11 delta-sigma ADC at full-scale range and at different gain configurations.

The RC filter combination is dimensioned such to help attenuate the nonlinear charge kickback and optimize for best THD performance. The ADC requires a low impedance input for lowest distortion performance; however, driving heavier loads degrades the phase margin of the INA851. Use a feedback capacitor (C_{FB}) in the range of 47 pF to 100 pF to optimize for stability versus THD performance. Low voltage-coefficient C0G capacitors are used everywhere in the signal path (C_{FB}, C_{DIFF}, C_{CM}) for their low distortion properties.

For other bandwidth requirements, adjust the feedback capacitor accordingly and verify the circuit performance using a SPICE simulation using INA851 TINA-TI™ SPICE Model. Confirm that the desired circuit is stable; that is, the FDA has more than a 45º phase margin.

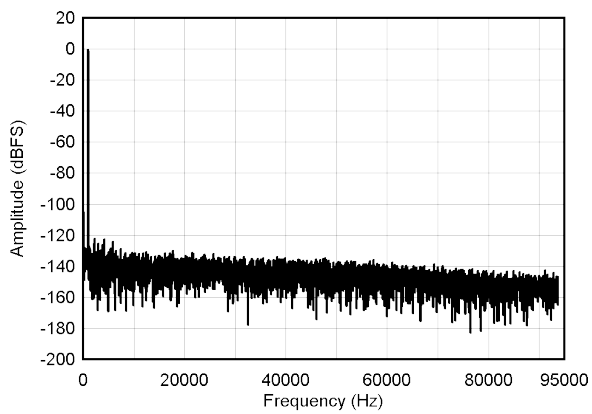
表 9-4. INA851 + ADS127L11 (Sinc4 Filter) FFT Data Summary

INPUT AMPLITUDE (Vpk)	RG RESISTOR (Ω)	G_{IN} (V/V)	G_{OUT} (V/V)	SNR (dB)	THD (dB)	ENOB (Bits)
23.7378	None	1	0.2	106.8	–116.0	17.36
4.7476	None	1	1	105.9	–122.0	17.28
2.3738[(1)]	1500	5	0.2	107.2	–113.8	17.25
0.2374	316	20	1	102.5	–112.0	16.59
0.0475	60.4	100	1	92.5	–99.0	14.81



G = 0.2 V/V, f_{IN} = 1 kHz, SNR = 106.75 dB, THD = –115.95 dB

图 9-10. Noise Performance FFT Plots with Sinc4 Filter for G = 0.2 V/V

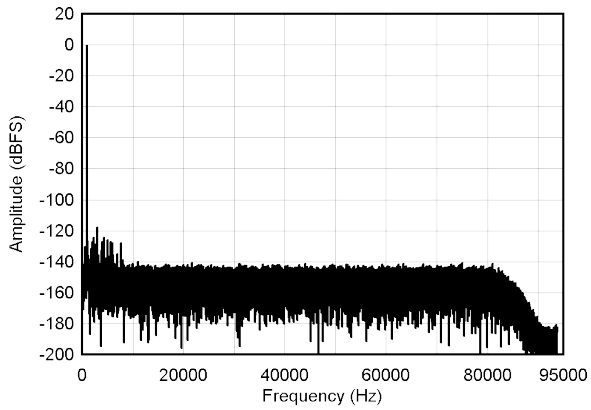


G = 0.2 V/V, f_{IN} = 1 kHz, SNR = 105.88 dB, THD = –122.00 dB

图 9-11. Noise Performance FFT Plots with Sinc4 Filter for G = 1 V/V

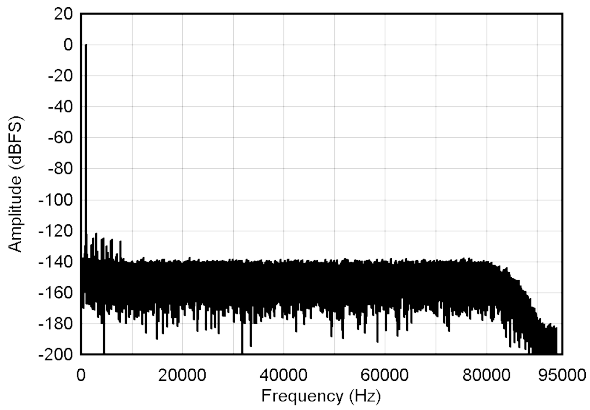
表 9-5. INA851 + ADS127L11 (Wideband Filter) FFT Data Summary

INPUT AMPLITUDE (Vpk)	RG RESISTOR (Ω)	G_{IN} (V/V)	G_{OUT} (V/V)	SNR (dB)	THD (dB)	ENOB (Bits)
23.76015	None	1	0.2	105.3	–116.2	17.14
4.7476	None	1	1	103.1	–120.0	16.81
2.3738	1500	5	0.2	104.2	–113.0	16.85
0.2360	316	20	1	99.0	–112.0	16.08
0.0472	60.4	100	1	89.3	–99.0	14.40



G = 0.2 V/V, f_{IN} = 1 kHz, SNR = 105.29 dB, THD = –116.21 dB

图 9-12. Noise Performance FFT Plots with Wideband Filter for G = 0.2 V/V



G = 1 V/V, f_{IN} = 1 kHz, SNR = 103.07 dB, THD = –120.01 dB

图 9-13. Noise Performance FFT Plots with Wideband Filter for G = 1 V/V

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9.3 Power Supply Recommendations

The nominal performance of the INA851 is specified with a supply voltage of ±15 V, and V_{ICM} and V_{OCM} at midsupply. The device also operates using power supplies from ±4 V (8 V) to ±18 V (36 V) and non-midsupply input and output common-mode voltages with excellent performance.

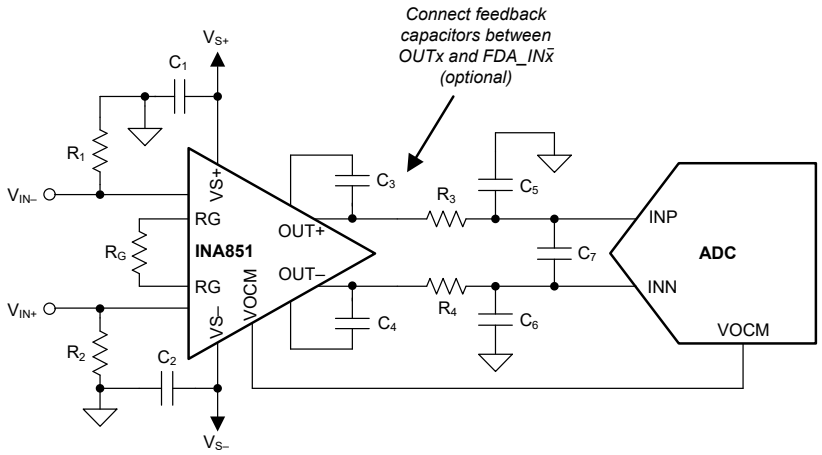
9.4 Layout

9.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good printed circuit board (PCB) layout practices:

- To avoid converting common-mode signals into differential signals and thermal electromotive forces (EMFs), make sure that both input paths are symmetrical and well-matched for source impedance and capacitance.
- As shown in 图 9-14, keep the external gain resistor close to the RG pins to keep the loop inductance as low as possible and to avoid a potential parasitic coupling path. Even slight mismatch in parasitic capacitance at the gain setting pins can degrade CMRR over frequency. In applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible, and most importantly, so that capacitance mismatch between the RG pins is minimized.
- Noise can propagate into analog circuitry through the power pins of the device and of the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular to the noisy trace is much better than in parallel.
- Leakage on the FDA_IN+ and FDA_IN– pins can cause in a dc offset error in the output voltages. Additionally, excessive parasitic capacitance at these pins can result in decreased phase margin and affect the stability of the output stage. If these pins are not used to implement deliberate capacitive feedback, follow best practices to minimize leakage and parasitic capacitance. Consider implementing *keep-out* areas in any ground planes that lie immediately below the pins.
- Minimize the number of thermal junctions. Ideally, the signal path is routed within a single layer without vias.
- Keep sufficient distance from major thermal energy sources (circuits with high power dissipation). If not possible, place the device so that the effects of the thermal energy source on the high and low sides of the differential signal path are evenly matched.
- Solder the thermal pad to the PCB. For the INA851 to properly dissipate heat, connect the thermal pad to a plane or large copper pour that is electrically connected to VS–, even for low-power applications.
- Keep the traces as short as possible.

9.4.2 Layout Example



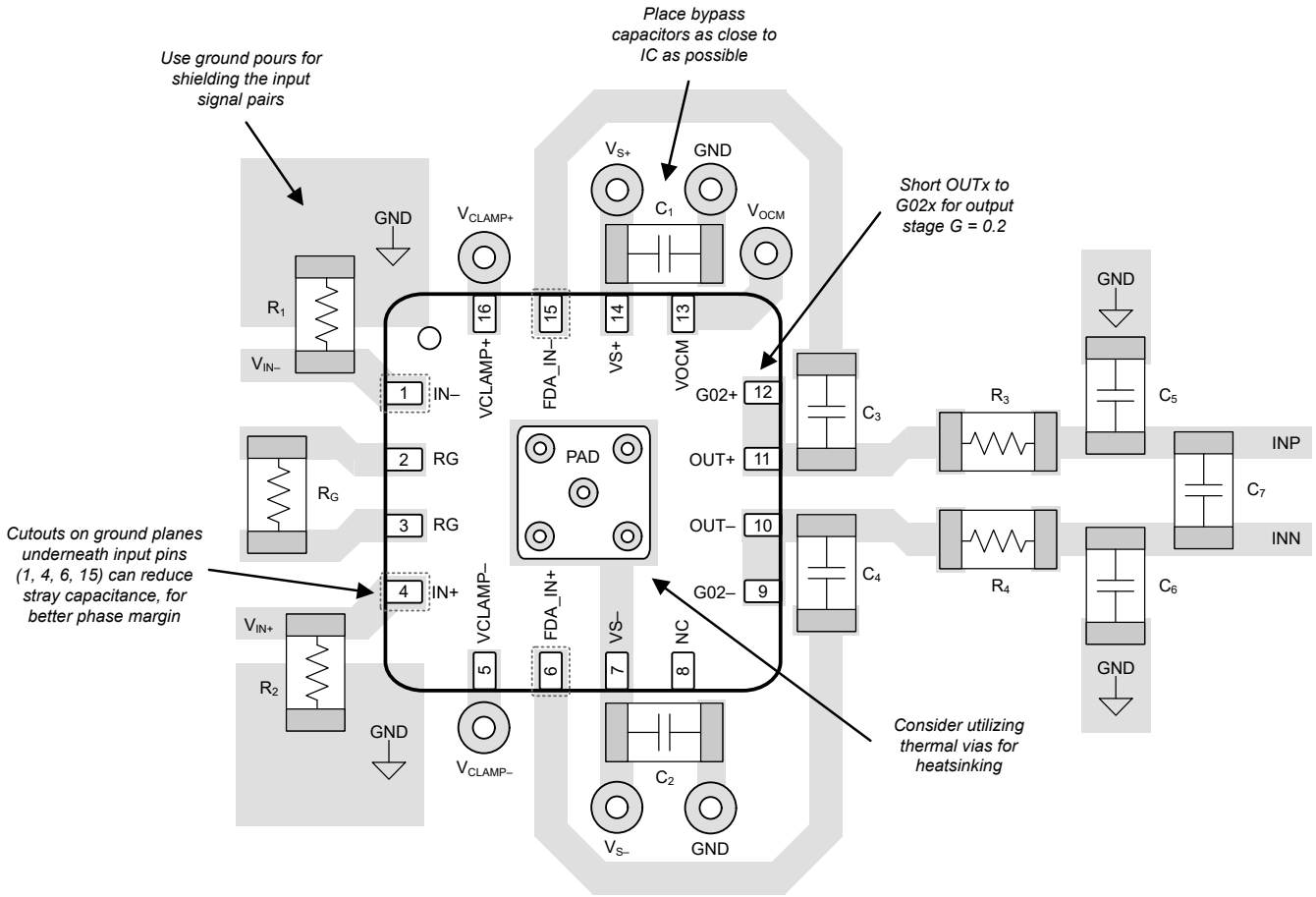


图 9-14. Example Schematic and Associated PCB Layout

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10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 PSpice® for TI

PSpice® for TI 是可帮助评估模拟电路性能的设计和仿真环境。在进行布局和制造之前创建子系统设计和原型解决方案，可降低开发成本并缩短上市时间。

10.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

备注

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers* application note
- Texas Instruments, *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application note

10.3 接收文档更新通知

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10.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA851RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	INA851
INA851RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	INA851
INA851RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	INA851
INA851RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	INA851

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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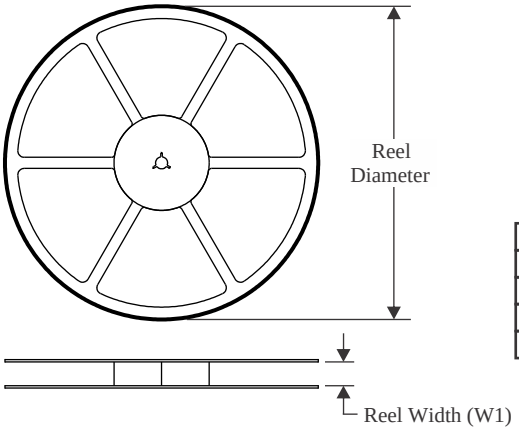
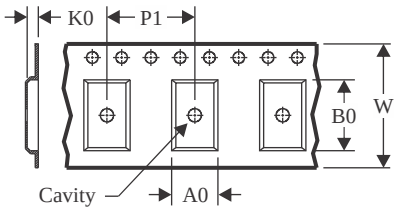
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

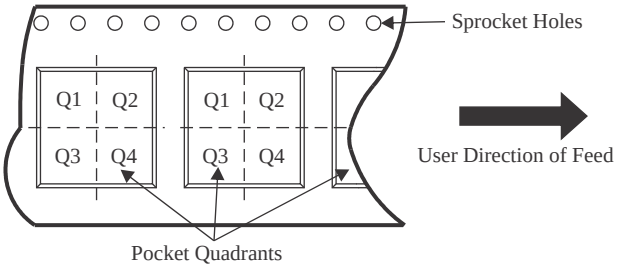


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

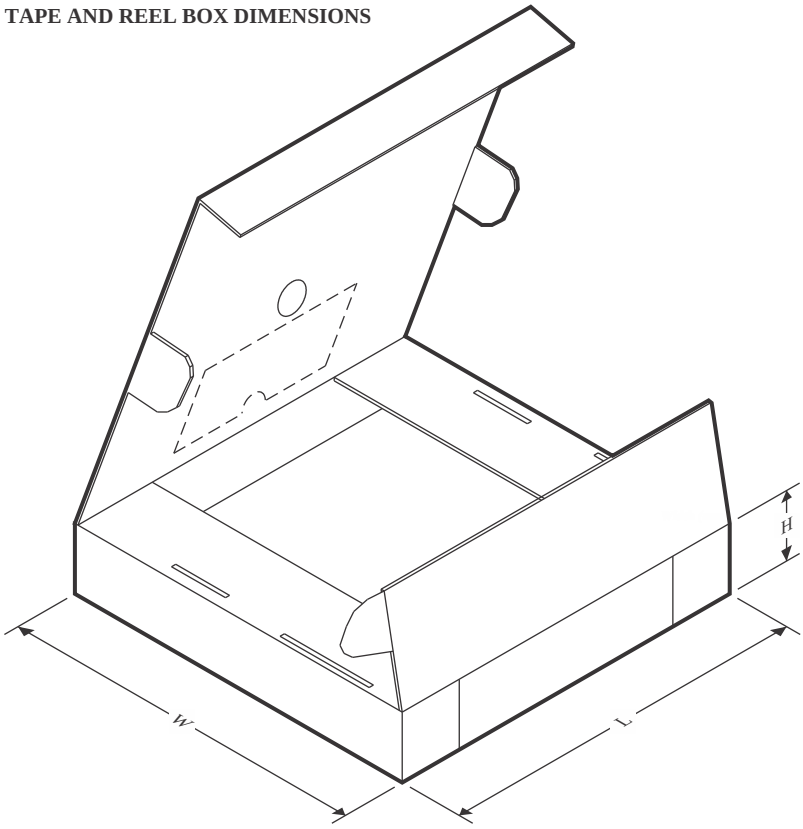
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA851RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA851RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



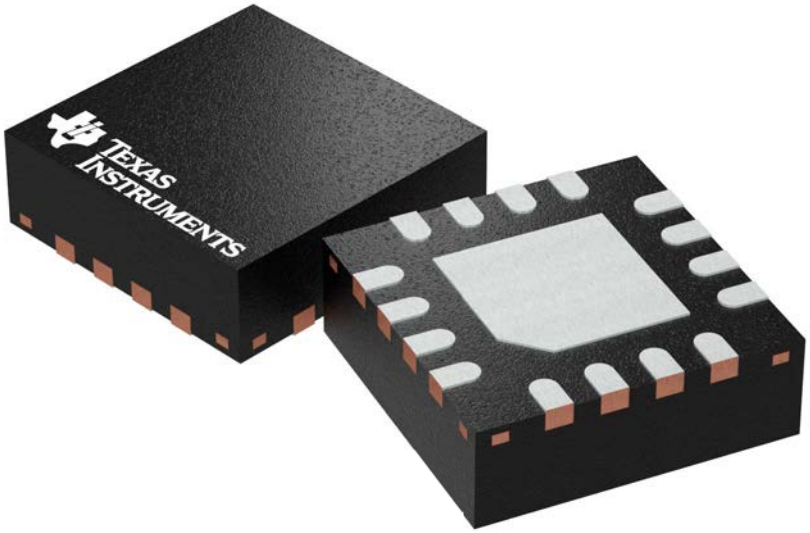
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA851RGTR	VQFN	RGT	16	3000	360.0	360.0	36.0
INA851RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16

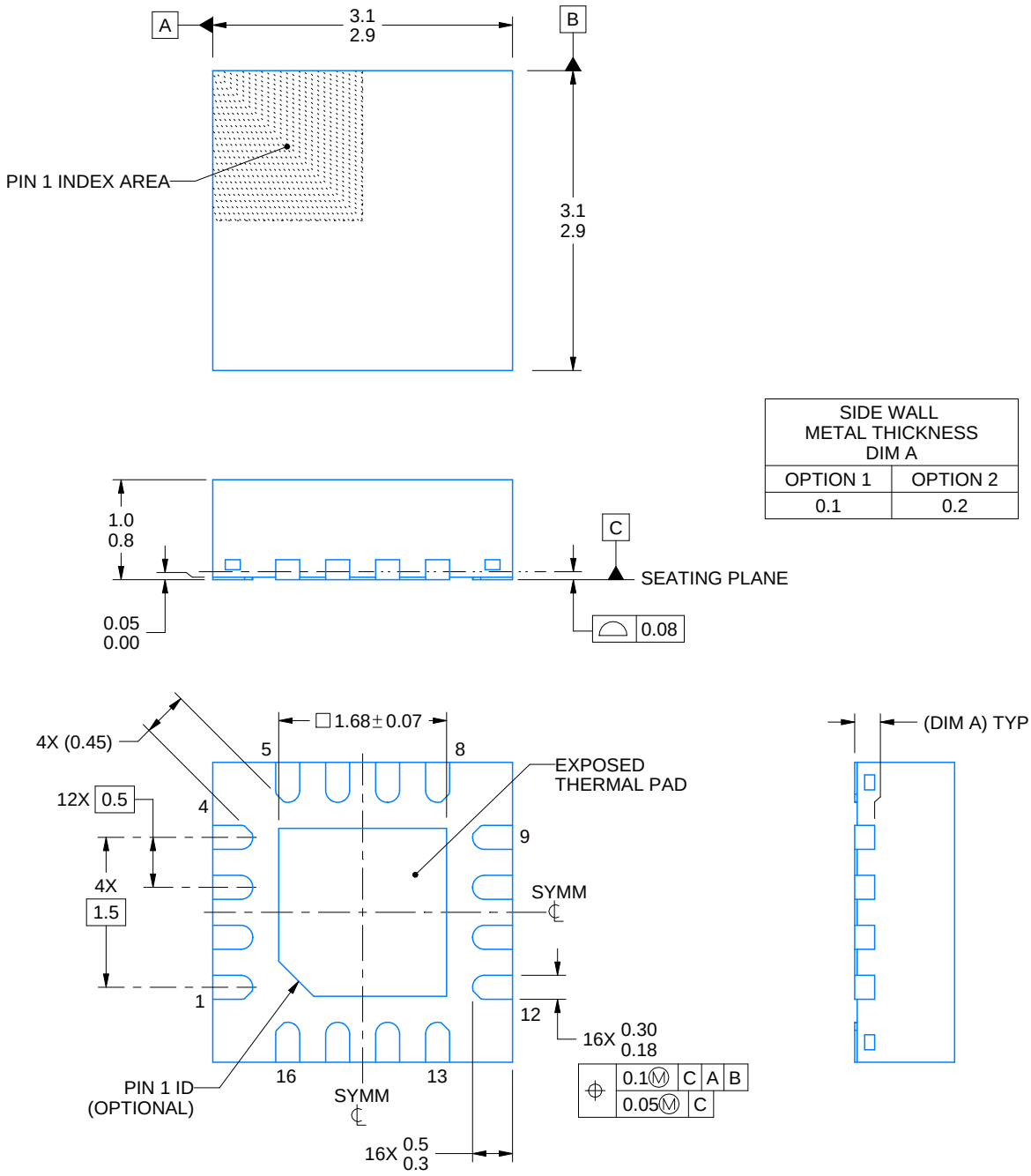
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/I



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

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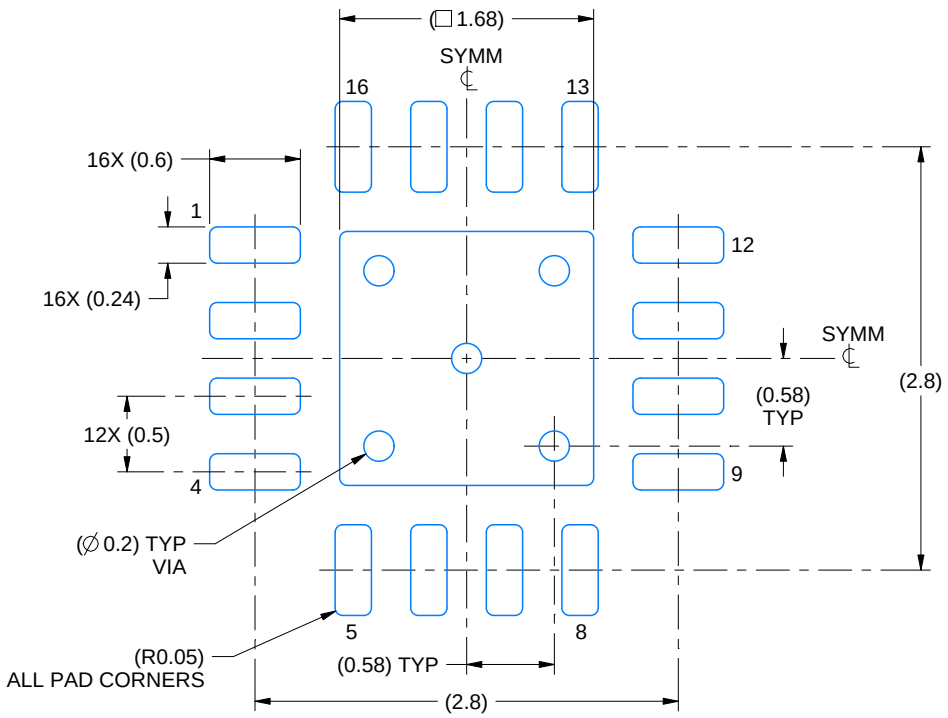
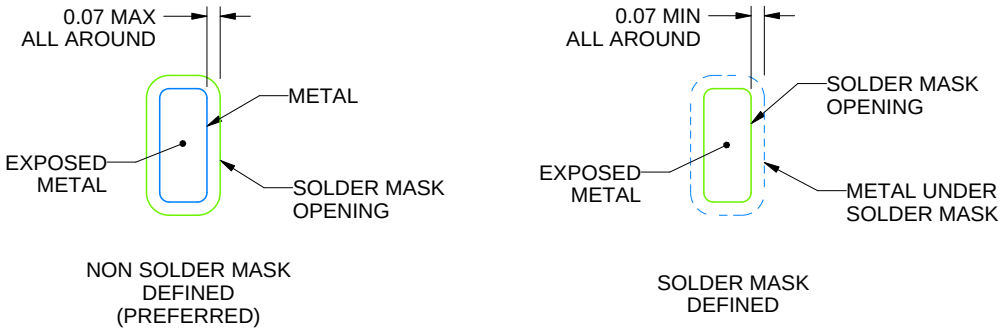
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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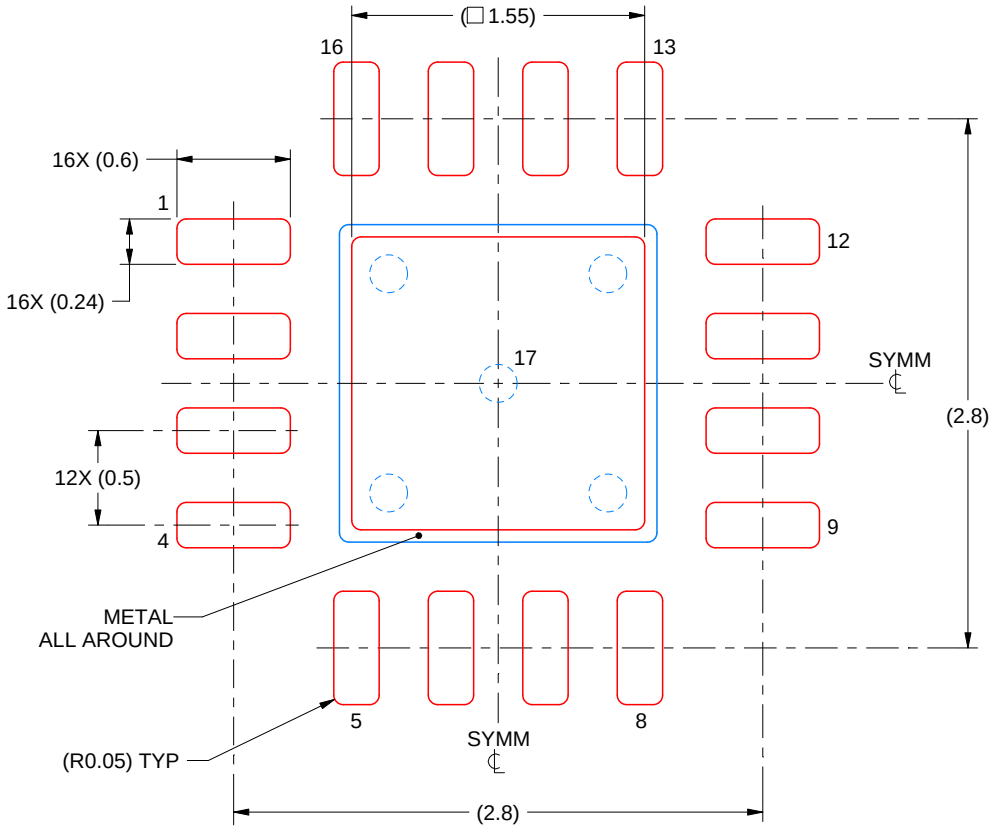
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月