



INA333 低功耗 (50μA)、零漂移、轨到轨输出仪表放大器

1 特性

- 低偏移电压: 25μV (最大值), $G \geq 100$
- 低漂移: $0.1\mu\text{V}/^\circ\text{C}$, $G \geq 100$
- 低噪声: $50\text{nV}/\sqrt{\text{Hz}}$, $G \geq 100$
- 高共模抑制比 (CMRR): 100dB (最小值), $G \geq 10$
- 低输入偏置电流: 200pA (最大值)
- 电源范围: 1.8V 至 5.5V
- 输入电压: $(V-) + 0.1\text{V}$ 至 $(V+) - 0.1\text{V}$
- 输出电压: $(V-) + 0.05\text{V}$ 至 $(V+) - 0.05\text{V}$
- 低静态电流: 50μA
- 工作温度范围: -40°C 至 $+125^\circ\text{C}$
- 已过滤射频干扰 (RFI) 的输入
- 8 引脚 VSSOP 和 8 引脚 WSON 封装

2 应用范围

- 桥式放大器
- 心电图 (ECG) 放大器
- 压力传感器
- 医疗仪表
- 便携式仪表
- 衡器
- 热电偶放大器
- 电阻式温度检测器 (RTD) 传感器放大器
- 数据采集

3 说明

INA333 器件是一款低功耗的精密仪表放大器, 具有出色的精度。该器件采用通用的三运算放大器设计, 并且拥有小巧尺寸和低功耗特性, 非常适合各类便携式应用。

可通过单个外部电阻在 1 到 1000 范围内设置增益。

INA333 设计为采用符合行业标准的增益公式: $G = 1 + (100\text{k}\Omega/R_G)$ 。

INA333 器件拥有超低的偏移电压 ($25\mu\text{V}$, $G \geq 100$), 出色的偏移电压漂移

($0.1\mu\text{V}/^\circ\text{C}$, $G \geq 100$), 以及较高的共模抑制比

(100dB, $G \geq 10$)。该器件可由低至 1.8V ($\pm 0.9\text{V}$)

的电源供电运行, 静态电流仅为 50μA, 因此非常适合电池供电类系统。INA333 器件采用自动校准技术在扩展工业温度范围内保证了出色的精度, 同时还提供了向下扩展至直流的超低噪声密度 ($50\text{nV}/\sqrt{\text{Hz}}$)。

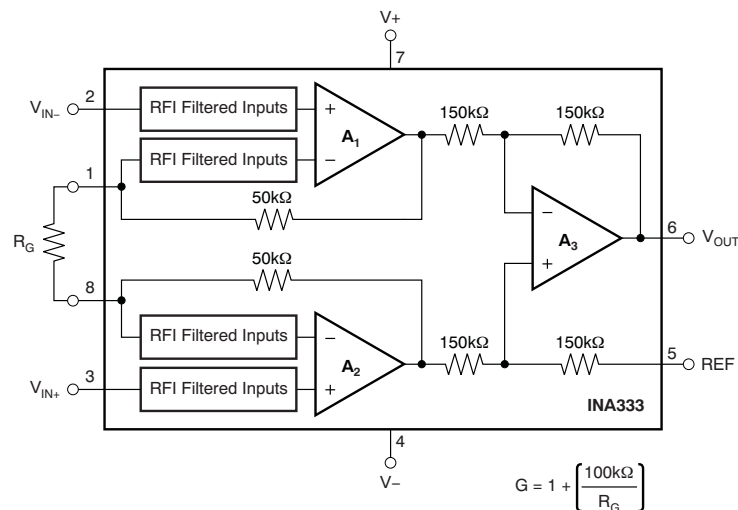
INA333 器件采用 8 引脚 VSSOP 和 WSON 表面贴装封装, 额定温度范围 $T_A = -40^\circ\text{C}$ 至 $+125^\circ\text{C}$ 。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
INA333	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

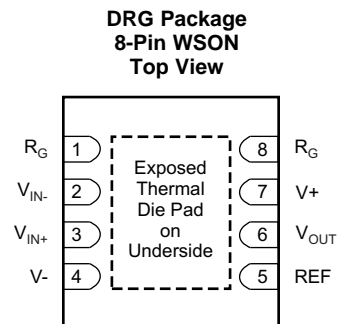
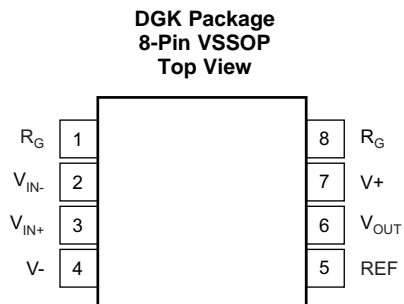
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (October 2008) to Revision C

Page

•	已添加 ESD 额定值表，特性 描述 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分	1
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5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
REF	5	I	Reference input. This pin must be driven by low impedance or connected to ground.
R_G	1, 8	—	Gain setting pins. For gains greater than 1, place a gain resistor between pins 1 and 8.
V^+	7	—	Positive supply
V^-	4	—	Negative supply
V_{IN+}	3	I	Positive input
V_{IN-}	2	I	Negative input
V_{OUT}	6	O	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT
Supply voltage	7		V
Analog input voltage ⁽²⁾	(V ₋) – 0.3	(V ₊) + 0.3	V
Output short-circuit ⁽³⁾	Continuous		
Operating temperature, T _A	–40	150	°C
Junction temperature, T _J		150	°C
Storage temperature, T _{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to ground.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	
	Machine model (MM)	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V _S Supply voltage	1.8	5.5	V
Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA333		UNIT
		DGK (VSSOP)	DRG (WSON)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	169.5	60	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	62.7	60	°C/W
R _{θJB}	Junction-to-board thermal resistance	90.3	50	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	7.6	—	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	88.7	—	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	6	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

for $V_S = 1.8 \text{ V}$ to 5.5 V at $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$, $V_{REF} = V_S / 2$, and $G = 1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT ⁽¹⁾						
V _{OSI}	Offset voltage, RTI ⁽²⁾			±10 ±25/G	±25 ±75/G	μV
PSR	vs temperature	T _A = −40°C to +125°C			±0.1 ±0.5 / G	μV/°C
	vs power supply	1.8 V ≤ V _S ≤ 5.5 V		±1 ±5/G	±5 ±15/G	μV/V
	Long-term stability			See ⁽³⁾		
	Turnon time to specified V _{OSI}	T _A = −40°C to +125°C		See <i>Typical Characteristics</i>		
	Impedance					
Z _{IN}	Differential			100 3		GΩ pF
Z _{IN}	Common-mode			100 3		GΩ pF
V _{CM}	Common-mode voltage range	V _O = 0 V	(V−) + 0.1		(V+) − 0.1	V
CMR	Common-mode rejection	DC to 60 Hz				
	G = 1	V _{CM} = (V−) + 0.1 V to (V+) − 0.1 V	80	90		dB
	G = 10	V _{CM} = (V−) + 0.1 V to (V+) − 0.1 V	100	110		dB
	G = 100	V _{CM} = (V−) + 0.1 V to (V+) − 0.1 V	100	115		dB
	G = 1000	V _{CM} = (V−) + 0.1 V to (V+) − 0.1 V	100	115		dB
INPUT BIAS CURRENT						
I _B	Input bias current			±70	±200	pA
	vs temperature	T _A = −40°C to +125°C		See Figure 26		pA/°C
I _{OS}	Input offset current			±50	±200	pA
	vs temperature	T _A = −40°C to +125°C		See Figure 28		pA/°C
INPUT VOLTAGE NOISE						
e _{NI}	Input voltage noise	G = 100, R _S = 0 Ω, f = 10 Hz		50		nV/√Hz
		G = 100, R _S = 0 Ω, f = 100 Hz		50		nV/√Hz
		G = 100, R _S = 0 Ω, f = 1 kHz		50		nV/√Hz
		G = 100, R _S = 0 Ω, f = 0.1 Hz to 10 Hz		1		μV _{PP}
i _N	Input current noise	f = 10 Hz		100		fA/√Hz
		f = 0.1 Hz to 10 Hz		2		pA _{PP}
GAIN						
G	Gain equation			1 + (100 kΩ/R _G)		V/V
	Range of gain		1		1000	V/V
Gain error		V _S = 5.5 V, (V−) + 100 mV ≤ V _O ≤ (V+) − 100 mV				
		G = 1		±0.01%	±0.1%	
		G = 10		±0.05%	±0.25%	
		G = 100		±0.07%	±0.25%	
		G = 1000		±0.25%	±0.5%	
Gain vs temperature, G = 1		T _A = −40°C to +125°C		±1	±5	ppm/°C
Gain vs temperature, G > 1 ⁽⁴⁾		T _A = −40°C to +125°C		±15	±50	ppm/°C
Gain nonlinearity		V _S = 5.5 V, (V−) + 100 mV ≤ V _O ≤ (V+) − 100 mV				
Gain nonlinearity, G = 1 to 1000		R _L = 10 kΩ		10		ppm
OUTPUT						
Output voltage swing from rail		V _S = 5.5 V, R _L = 10 kΩ		See Figure 29	50	mV
Capacitive load drive				500		pF
I _{SC}	Short-circuit current	Continuous to common		−40, +5		mA

(1) Total V_{OS} , referred-to-input = $(V_{OSI}) + (V_{OSO} / G)$

(2) RTI = Referred-to-input

(3) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately $1 \mu\text{V}$

(4) Does not include effects of external resistor R_G

INA333

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Electrical Characteristics (continued)

 for $V_S = 1.8\text{ V}$ to 5.5 V at $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$, $V_{REF} = V_S / 2$, and $G = 1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
Bandwidth, –3dB		$G = 1$		150		kHz
		$G = 10$		35		kHz
		$G = 100$		3.5		kHz
		$G = 1000$		350		Hz
SR Slew rate		$V_S = 5\text{ V}$, $V_O = 4\text{-V step}$, $G = 1$		0.16		V/ μs
		$V_S = 5\text{ V}$, $V_O = 4\text{-V step}$, $G = 100$		0.05		V/ μs
t_S Settling time to 0.01%		$V_{STEP} = 4\text{ V}$, $G = 1$		50		μs
		$V_{STEP} = 4\text{ V}$, $G = 100$		400		μs
t_S Settling time to 0.001%		$V_{STEP} = 4\text{ V}$, $G = 1$		60		μs
		$V_{STEP} = 4\text{ V}$, $G = 100$		500		μs
Overload recovery		50% overdrive		75		μs
REFERENCE INPUT						
R_{IN}				300		k Ω
Voltage range			V_-		V_+	V
POWER SUPPLY						
Voltage range		Single voltage range	+1.8		+5.5	V
		Dual voltage range	± 0.9		± 2.75	V
I_Q	Quiescent current	$V_{IN} = V_S / 2$		50	75	μA
	vs temperature	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			80	μA
TEMPERATURE RANGE						
Specified temperature range			–40		125	$^\circ\text{C}$
Operating temperature range			–40		150	$^\circ\text{C}$

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = \text{midsupply}$, and $G = 1$ (unless otherwise noted)

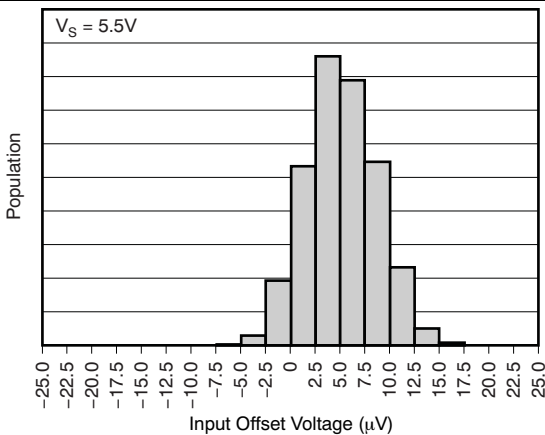


Figure 1. Input Offset Voltage

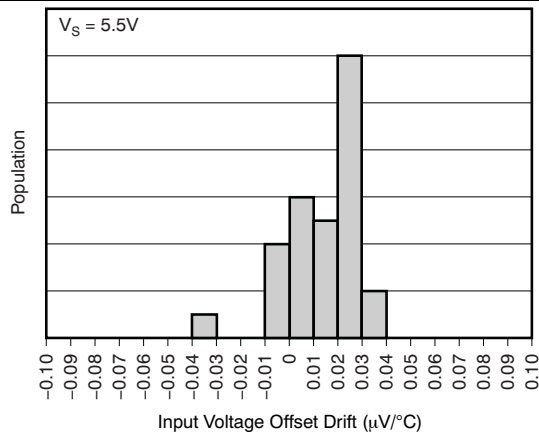


Figure 2. Input Voltage Offset Drift (-40°C to 125°C)

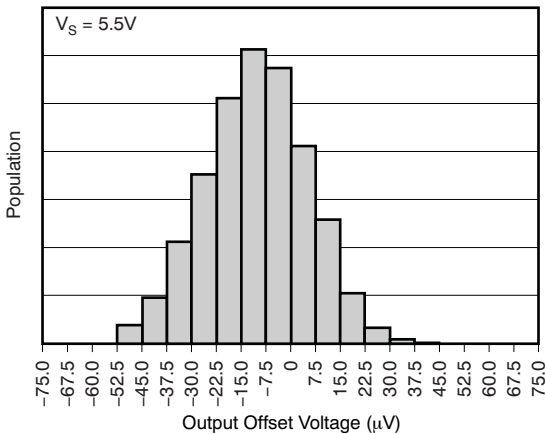


Figure 3. Output Offset Voltage

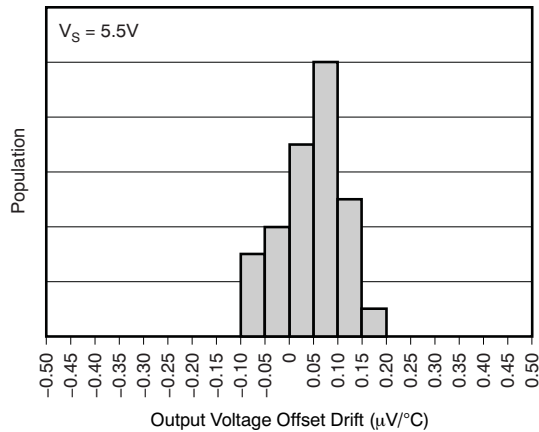


Figure 4. Output Voltage Offset Drift (-40°C to 125°C)

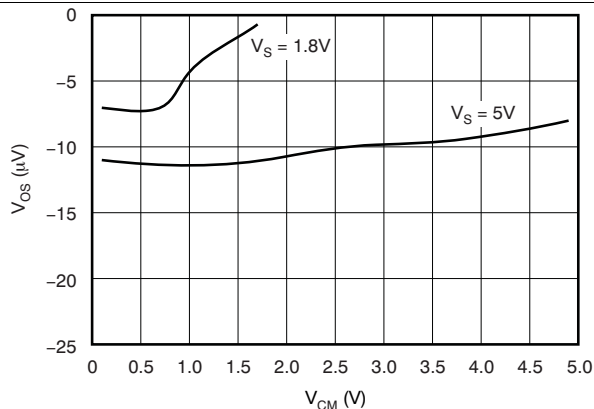


Figure 5. Offset Voltage vs Common-Mode Voltage

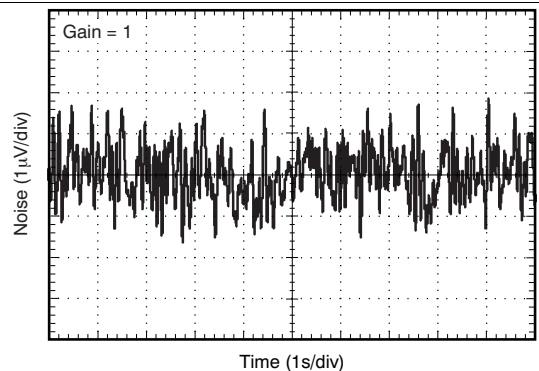


Figure 6. 0.1-Hz to 10-Hz Noise

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = \text{midsupply}$, and $G = 1$ (unless otherwise noted)

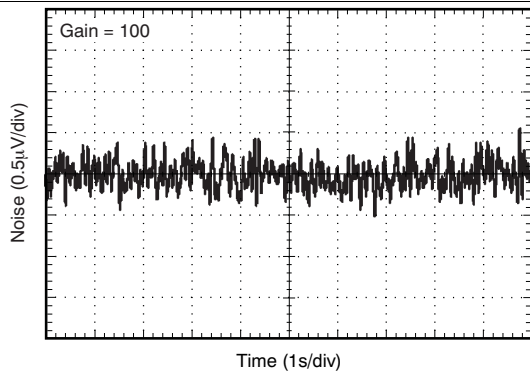


Figure 7. 0.1-Hz to 10-Hz Noise

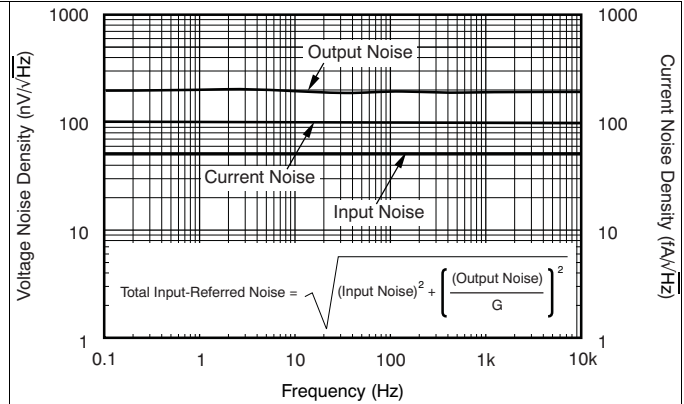


Figure 8. Spectral Noise Density

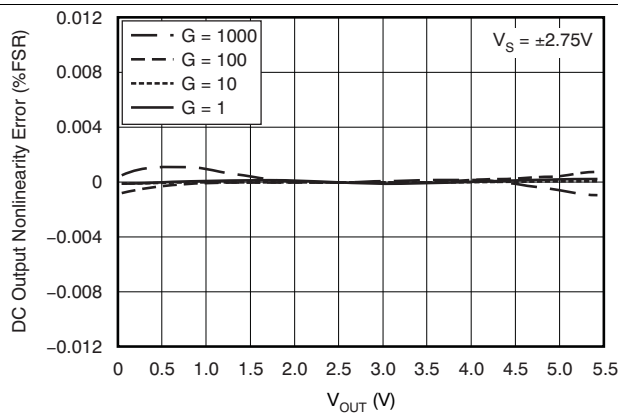


Figure 9. Nonlinearity Error

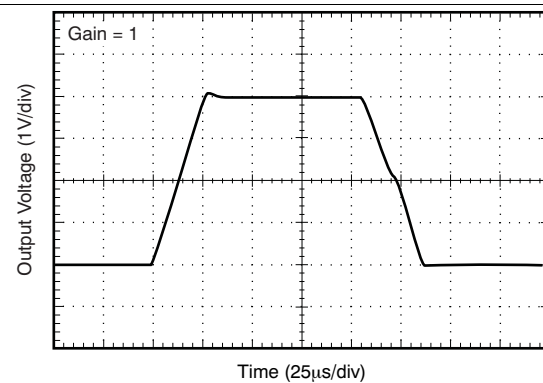


Figure 10. Large Signal Response

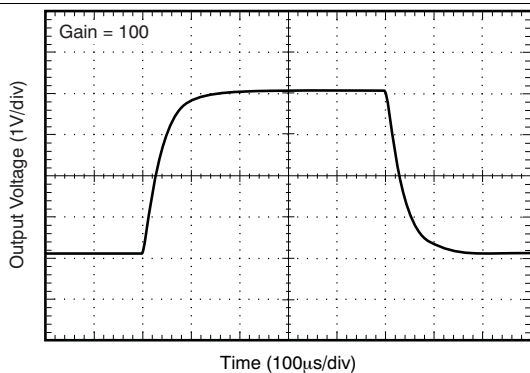


Figure 11. Large-Signal Step Response

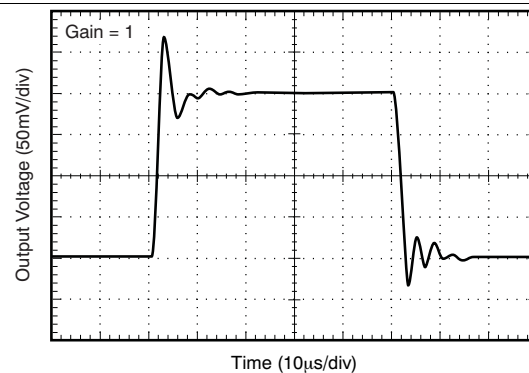


Figure 12. Small-Signal Step Response

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = \text{midsupply}$, and $G = 1$ (unless otherwise noted)

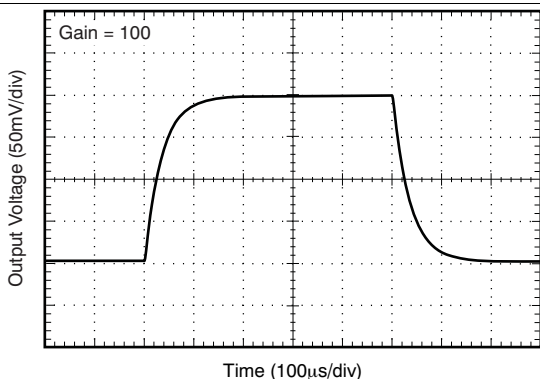


Figure 13. Small-Signal Step Response

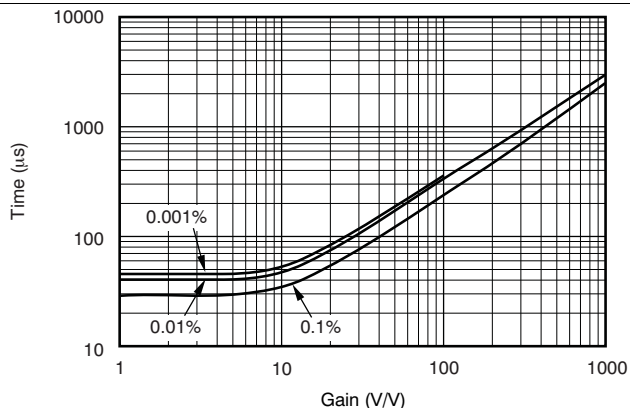


Figure 14. Settling Time vs Gain

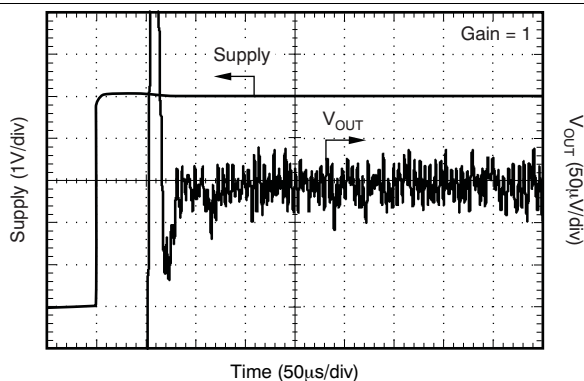


Figure 15. Start-Up Settling Time

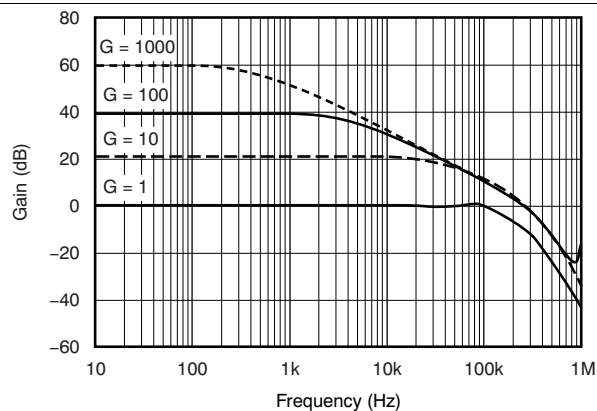


Figure 16. Gain vs Frequency

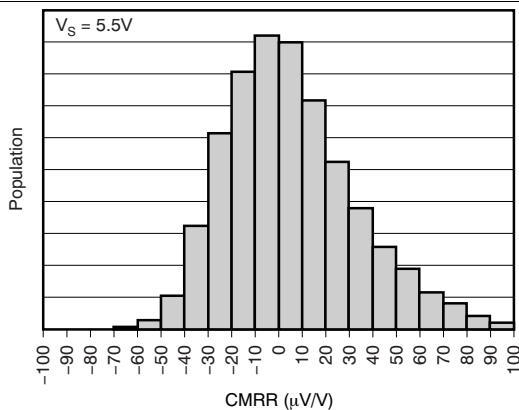


Figure 17. Common-Mode Rejection Ratio

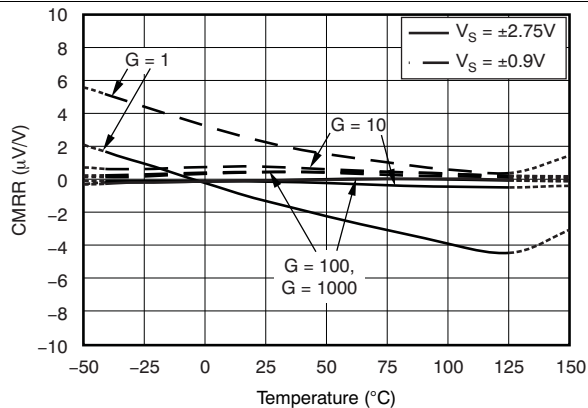


Figure 18. Common-Mode Rejection Ratio vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = \text{mid supply}$, and $G = 1$ (unless otherwise noted)

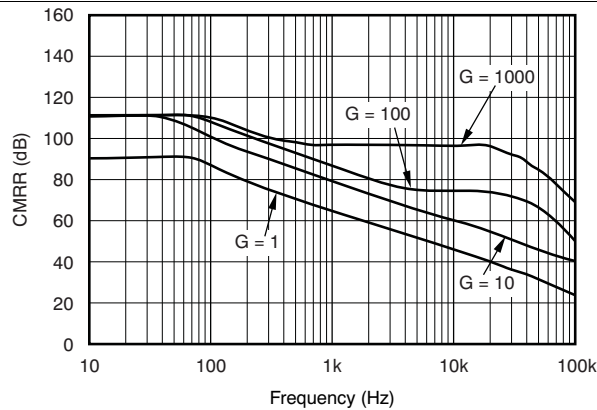


Figure 19. Common-Mode Rejection Ratio vs Frequency

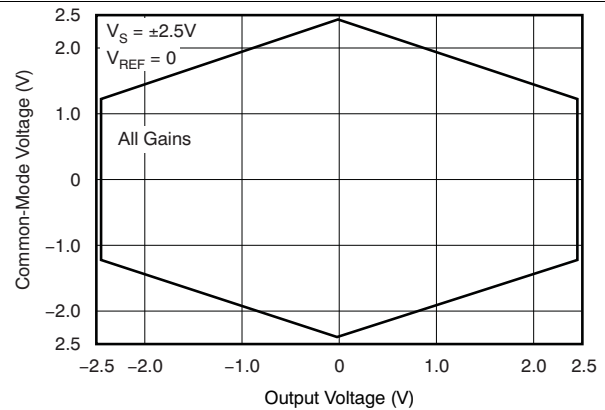


Figure 20. Typical Common-Mode Range vs Output Voltage

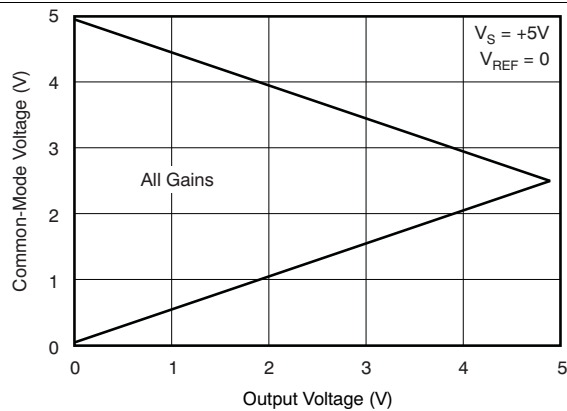


Figure 21. Typical Common-Mode Range vs Output Voltage

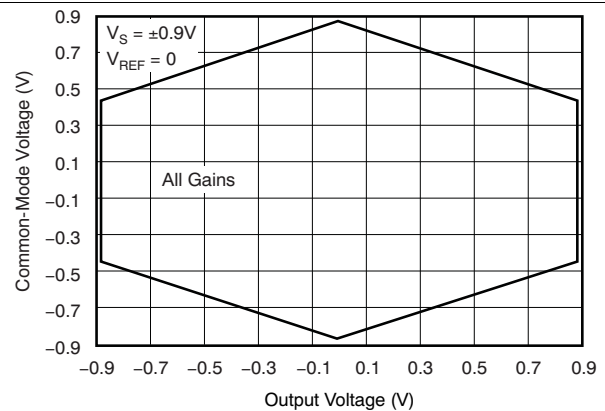


Figure 22. Typical Common-Mode Range vs Output Voltage

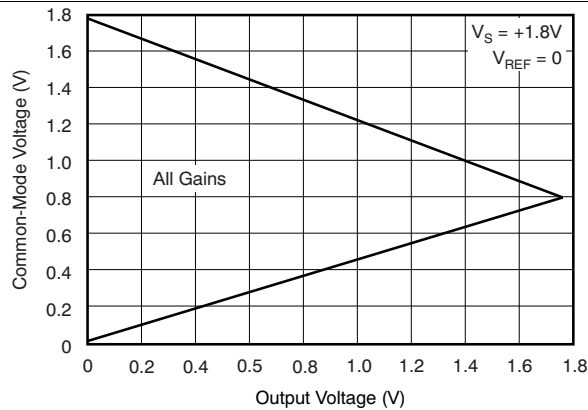


Figure 23. Typical Common-Mode Range vs Output Voltage

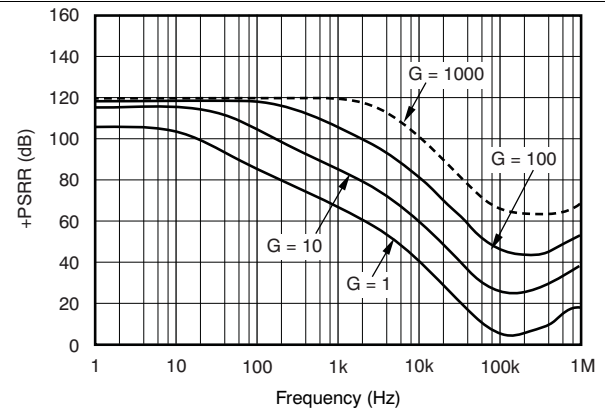


Figure 24. Positive Power-Supply Rejection Ratio

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = \text{mid supply}$, and $G = 1$ (unless otherwise noted)

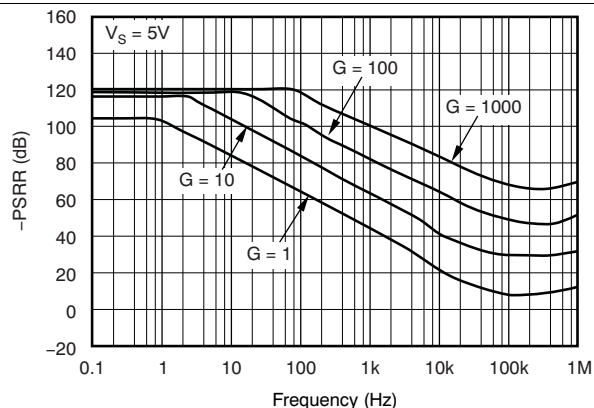


Figure 25. Negative Power-Supply Rejection Ratio

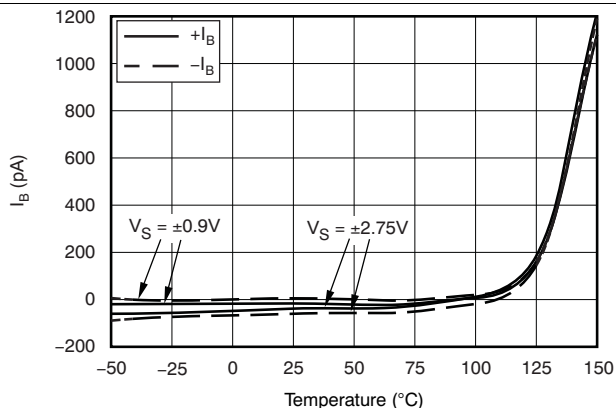


Figure 26. Input Bias Current vs Temperature

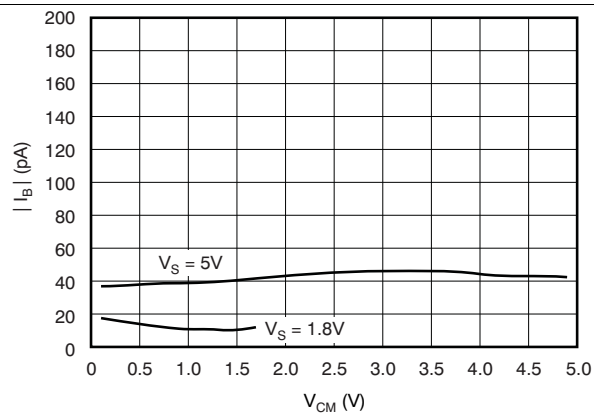


Figure 27. Input Bias Current vs Common-Mode Voltage

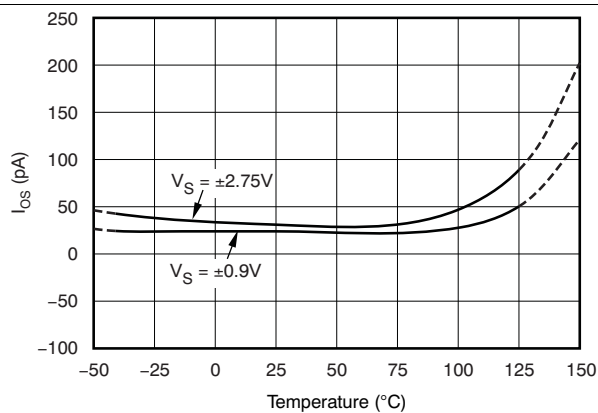


Figure 28. Input Offset Current vs Temperature

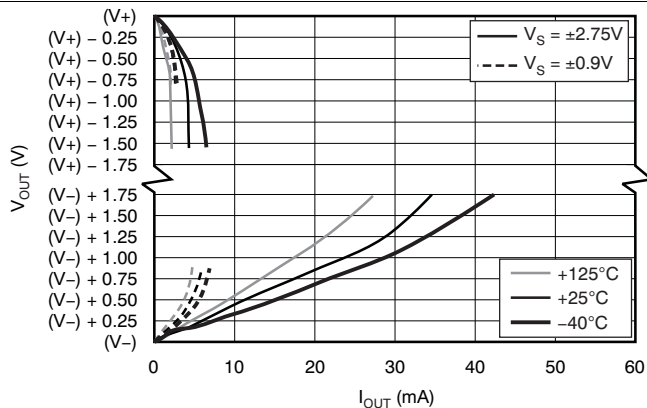


Figure 29. Output Voltage Swing vs Output Current

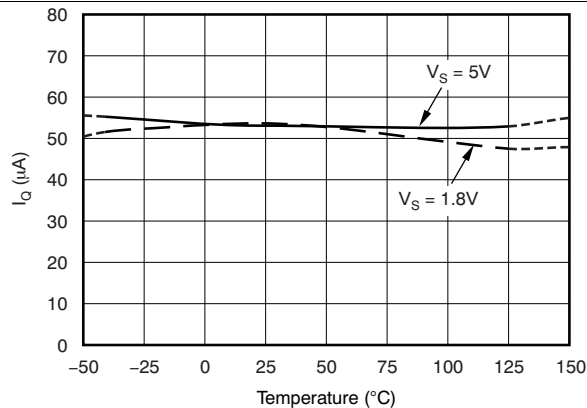


Figure 30. Quiescent Current vs Temperature

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{\text{REF}} = \text{midsupply}$, and $G = 1$ (unless otherwise noted)

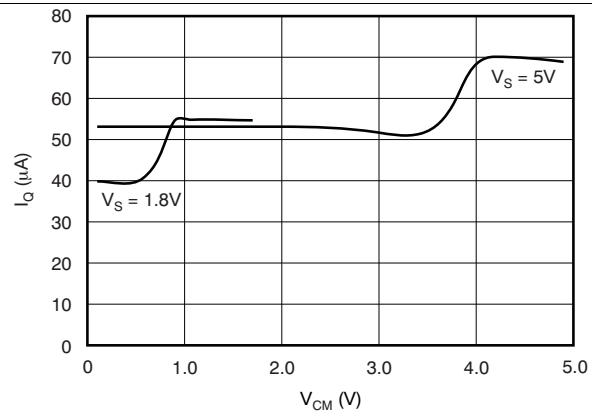


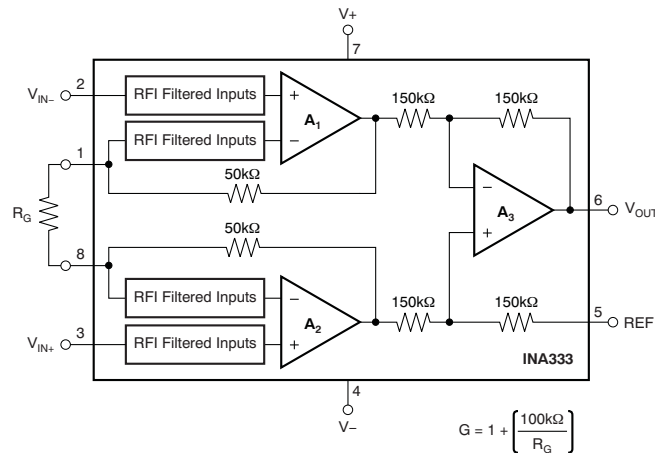
Figure 31. Quiescent Current vs Common-Mode Voltage

7 Detailed Description

7.1 Overview

The INA333 is a monolithic instrumentation amplifier (INA) based on the precision zero-drift OPA333 (operational amplifier) core. The INA333 also integrates laser-trimmed resistors to ensure excellent common-mode rejection and low gain error. The combination of the zero-drift amplifier core and the precision resistors allows this device to achieve outstanding DC precision and makes the INA333 ideal for many 3.3-V and 5-V industrial applications.

7.2 Functional Block Diagram



7.3 Feature Description

The INA333 is a low-power, zero-drift instrumentation amplifier offering excellent accuracy. The versatile three-operational-amplifier design and small size make the amplifiers ideal for a wide range of applications. Zero-drift chopper circuitry provides excellent DC specifications. A single external resistor sets any gain from 1 to 10,000. The INA333 is laser trimmed for very high common-mode rejection (100 dB at $G \geq 100$). This device operates with power supplies as low as 1.8 V, and quiescent current of 50 μ A, typically.

7.4 Device Functional Modes

7.4.1 Internal Offset Correction

INA333 internal operational amplifiers use an auto-calibration technique with a time-continuous 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8 μ s using a proprietary technique. Upon power up, the amplifier requires approximately 100 μ s to achieve specified VOS accuracy. This design has no aliasing or flicker noise.

7.4.2 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA333 is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A1 and A2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see [Figure 20](#).

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA333 is near 0 V even though both inputs are overloaded.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA333 measures small differential voltage with high common-mode voltage developed between the noninverting and inverting input. The high input impedance makes the INA333 suitable for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

8.2 Typical Application

Figure 32 shows the basic connections required for operation of the INA333 device. Good layout practice mandates the use of bypass capacitors placed close to the device pins as shown.

The output of the INA333 device is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to assure good common-mode rejection. Although 15 Ω or less of stray resistance can be tolerated while maintaining specified CMRR, small stray resistances of tens of Ω s in series with the REF pin can cause noticeable degradation in CMRR.

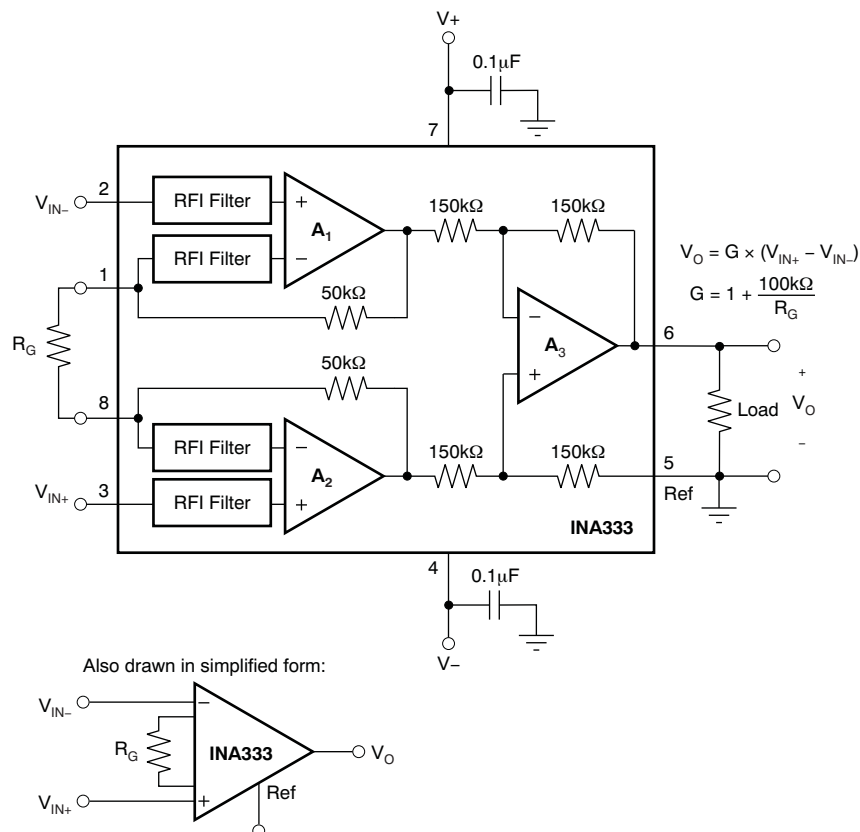


Figure 32. Basic Connections

Typical Application (continued)

8.2.1 Design Requirements

The device can be configured to monitor the input differential voltage when the gain of the input signal is set by the external resistor R_G . The output signal references to the Ref pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the Ref pin to ground. When the input signal increases, the output voltage at the OUT pin increases, too.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Gain

Gain of the INA333 device is set by a single external resistor, R_G , connected between pins 1 and 8. The value of R_G is selected according to [Equation 1](#):

$$G = 1 + (100 \text{ k}\Omega / R_G) \quad (1)$$

[Table 1](#) lists several commonly-used gains and resistor values. The 100 k Ω in [Equation 1](#) comes from the sum of the two internal feedback resistors of A_1 and A_2 . These on-chip resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA333 device.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from the gain [Equation 1](#). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at the R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency.

Table 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC ⁽¹⁾	NC
2	100k	100k
5	25k	24.9k
10	11.1k	11k
20	5.26k	5.23k
50	2.04k	2.05
100	1.01k	1k
200	502.5	499
500	200.4	200
1000	100.1	100

(1) NC denotes no connection. When using the SPICE model, the simulation will not converge unless a resistor is connected to the R_G pins; use a very large resistor value.

8.2.2.2 Internal Offset Correction

The INA333 device internal operational amplifiers use an auto-calibration technique with a time-continuous 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8 μ s using a proprietary technique. Upon power-up, the amplifier requires approximately 100 μ s to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

8.2.2.3 Offset Trimming

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF pin. [Figure 33](#) shows an optional circuit for trimming the output offset voltage. The voltage applied to REF pin is summed at the output. The operational amplifier buffer provides low impedance at the REF pin to preserve good common-mode rejection.

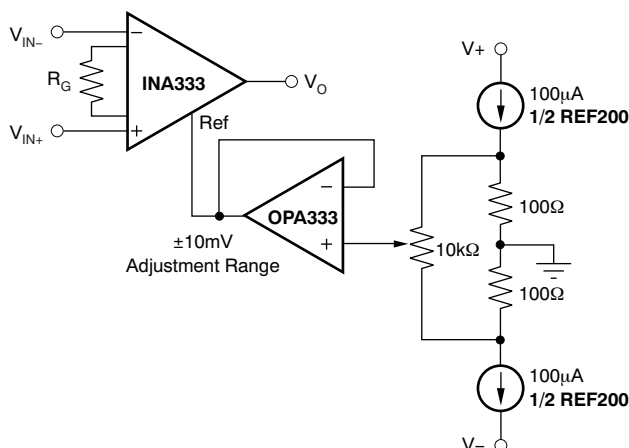


Figure 33. Optional Trimming of Output Offset Voltage

8.2.2.4 Noise Performance

The auto-calibration technique used by the INA333 device results in reduced low frequency noise, typically only 50 nV/√Hz, ($G = 100$). The spectral noise density can be seen in detail in [Figure 8](#). Low frequency noise of the INA333 device is approximately 1 μV_{PP} measured from 0.1 Hz to 10 Hz, ($G = 100$).

8.2.2.5 Input Bias Current Return Path

The input impedance of the INA333 device is extremely high—approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically ±70 pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. [Figure 34](#) shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA333 device, and the input amplifiers will saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in [Figure 34](#)). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

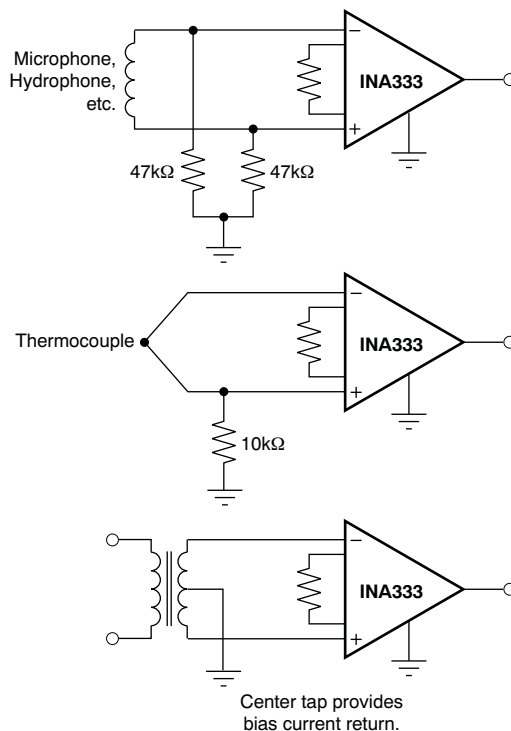


Figure 34. Providing an Input Common-Mode Current Path

8.2.2.6 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA333 device is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A₁ and A₂. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see Figure 20 to Figure 23 in the [Typical Characteristics](#) section.

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA333 is near 0 V even though both inputs are overloaded.

8.2.2.7 Operating Voltage

The INA333 operates over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the [Typical Characteristics](#) section of this data sheet.

8.2.2.8 Low Voltage Operation

The INA333 device can be operated on power supplies as low as ±0.9 V. Most parameters vary only slightly throughout this supply voltage range—see the [Typical Characteristics](#) section. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. [Figure 20](#) to [Figure 23](#) show the range of linear operation for various supply voltages and gains.

8.2.2.9 Single-Supply Operation

The INA333 device can be used on single power supplies of 1.8 V to 5.5 V. [Figure 35](#) shows a basic single-supply circuit. The output REF pin is connected to mid-supply. Zero differential input voltage demands an output voltage of mid-supply. Actual output voltage swing is limited to approximately 50 mV more than ground, when the load is referred to ground as shown. [Figure 29](#) shows how the output voltage swing varies with output current.

8.2.3 Application Curves

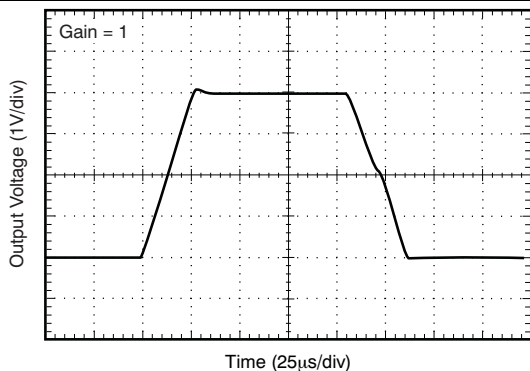


Figure 36. Large Signal Response

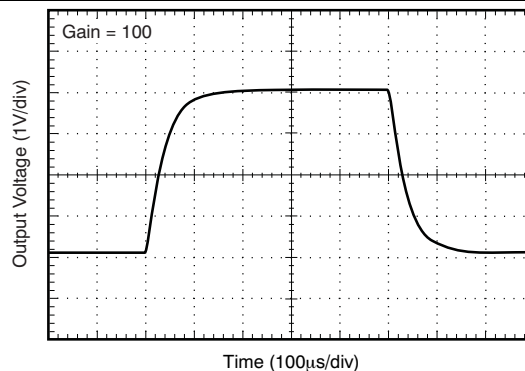


Figure 37. Large-Signal Step Response

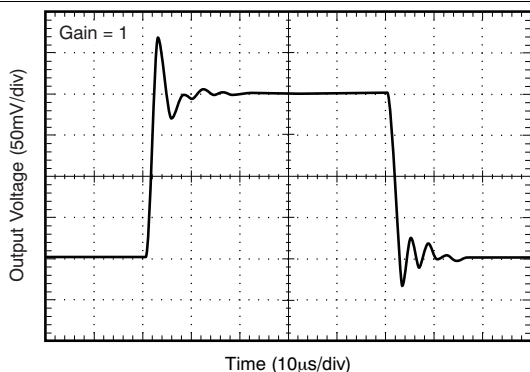


Figure 38. Small-Signal Step Response

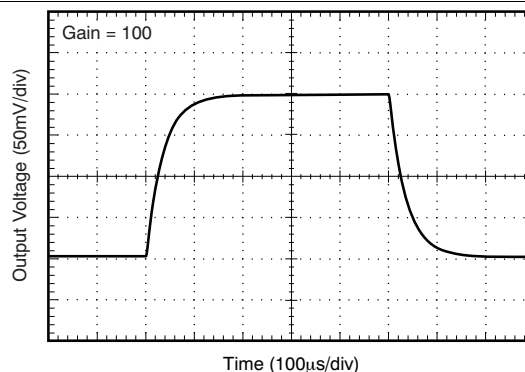


Figure 39. Small-Signal Step Response

9 Power Supply Recommendations

The minimum power supply voltage for INA333 is 1.8 V and the maximum power supply voltage is 5.5 V. For optimum performance, 3.3 V to 5 V is recommended. TI recommends adding a bypass capacitor at the input to compensate for the layout and power supply source impedance.

10 Layout

10.1 Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1- μ F bypass capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

Instrumentation amplifiers vary in the susceptibility to radio-frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The INA333 device has been specifically designed to minimize susceptibility to RFI by incorporating passive RC filters with an 8-MHz corner frequency at the V_{IN+} and V_{IN-} inputs. As a result, the INA333 device demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may continue to cause varying offset levels, however, and may require additional shielding.

10.2 Layout Example

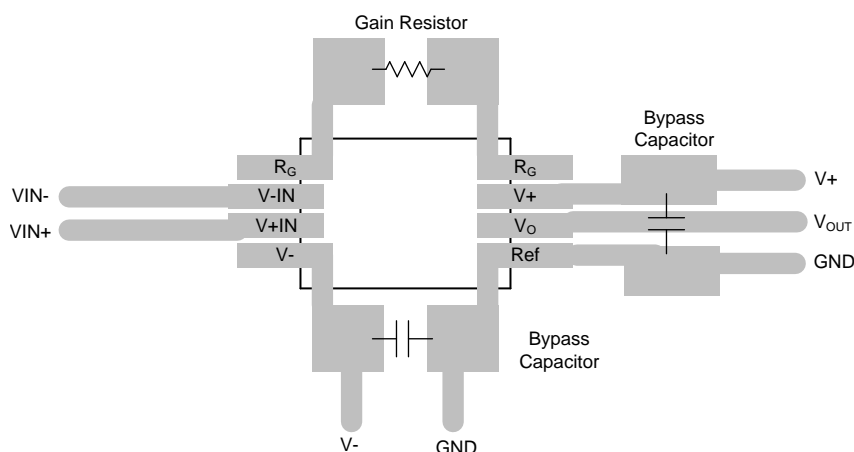


Figure 40. INA333 Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI (免费下载软件)

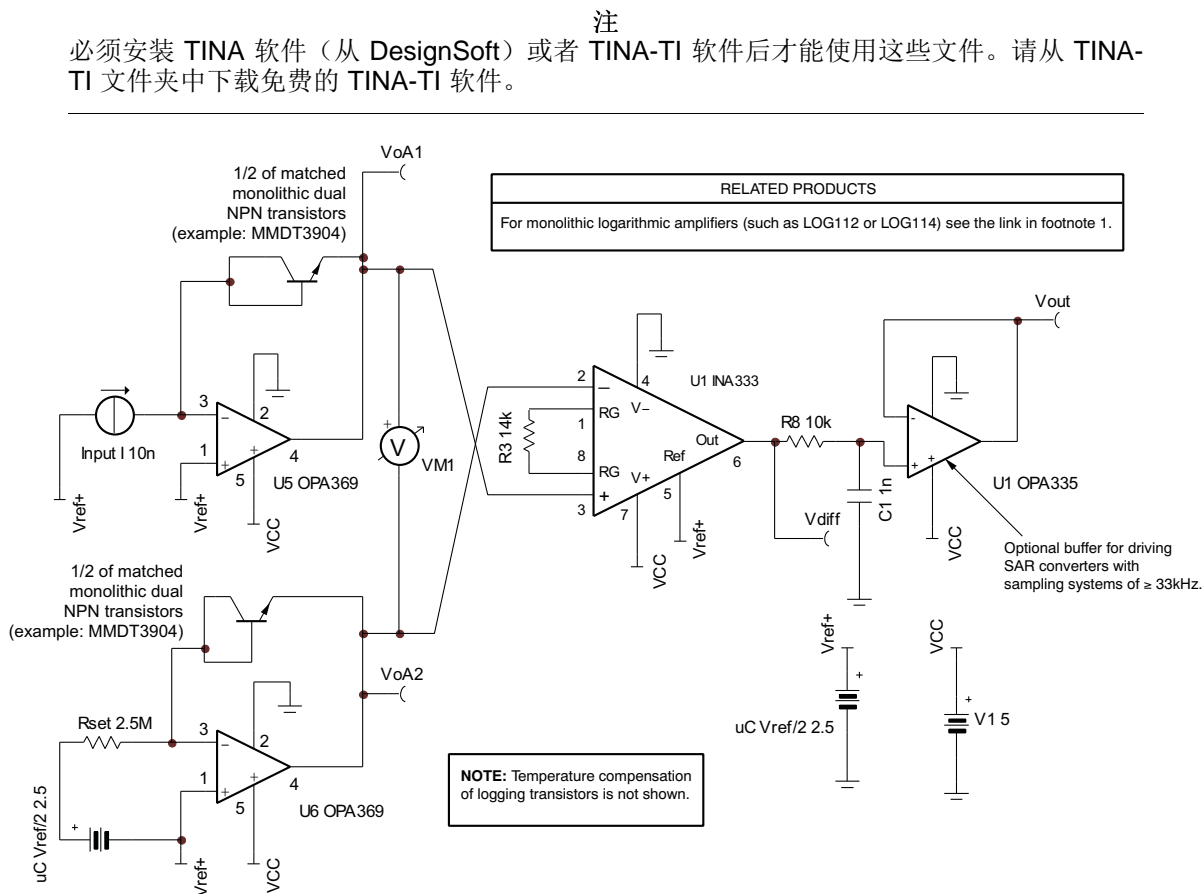
TINA-TI 基于 SPICE 的模拟仿真程序 (适用于 INA333)

TINA 是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。它提供所有传统的 SPICE 直流 (DC)、瞬态和频域分析以及其他设计功能。

TINA-TI 可从 [Analog eLab Design Center \(模拟电子实验室设计中心\)](#) 免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。

虚拟仪器为用户提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

图 41 和图 42 给出了适用于 INA333 器件的 TINA-TI 电路示例，这些电路可用于开发、修改和评估特定用途的电路设计。下面给出了这些仿真文件的下载链接。

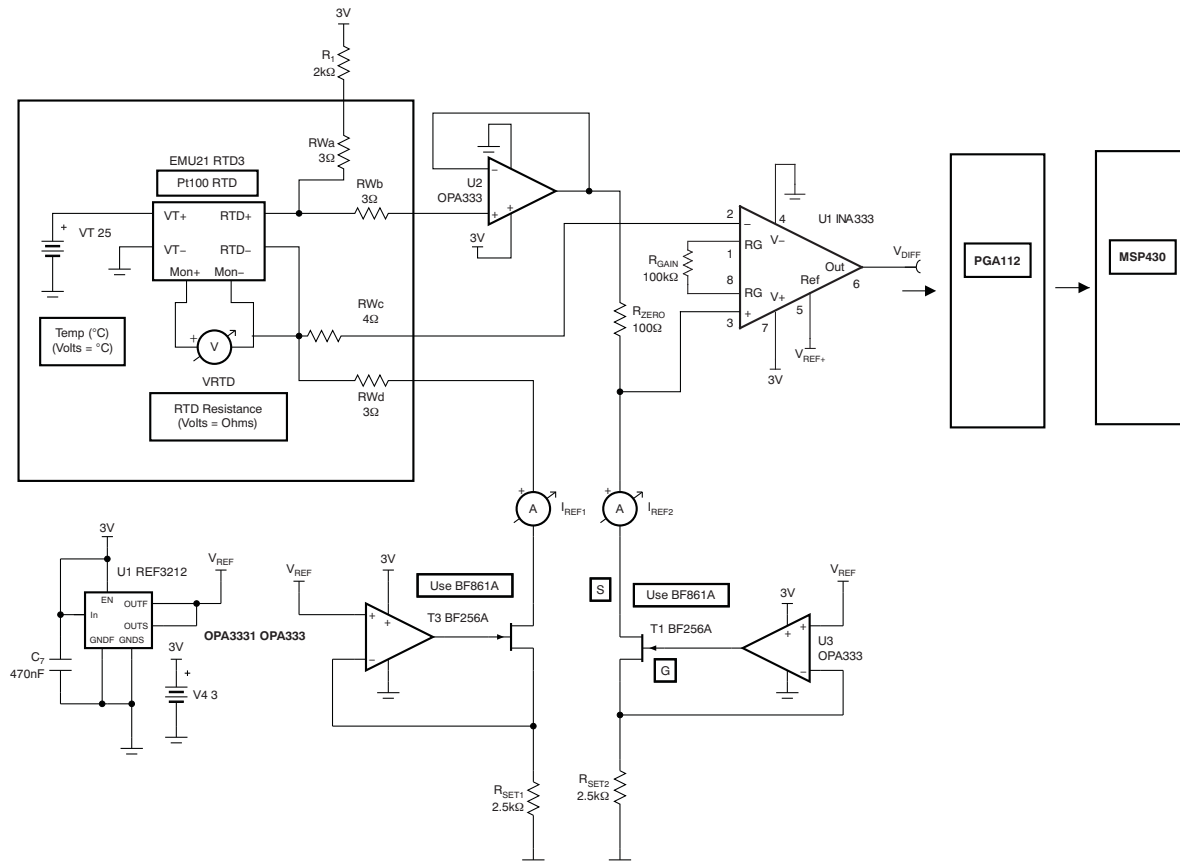


(1) 如下链接会打开 TI 对数放大器网页：对数放大器产品主页

图 41. 便携式电池供电类系统的低功耗对数函数电路 (例如血糖仪)

要下载包含此电路 TINA-TI 仿真文件的压缩文件，请点击如下链接：[对数电路](#)。

器件支持 (接下页)



RWa、RWb、RWc 和 RWd 用于仿真线电阻。包含这些电阻是为了展示四线传感技术对线不匹配问题的抗扰性。此方法假定使用四线 RTD。

图 42. 具有可编程增益采集系统的四线、3V PT100 RTD 调节器

要下载包含此电路 TINA-TI 仿真文件的压缩文件，请点击如下链接：[PT100 RTD](#)。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- 《高精度、低噪声、轨到轨输出、36V、零漂移运算放大器》，[SBOS642](#)
- 《50μV VOS、0.25μV/°C、35μA CMOS 运算放大器零漂移系列》，[SBOS432](#)
- 《4ppm/°C、100μA、SOT23-6 系列电压基准》，[SBVS058](#)
- 《电路板布局布线技巧》，[SLOA089](#)

11.3 商标

All trademarks are the property of their respective owners.

11.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA333AIDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDGKRG4	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDGKT.A	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDGKTG4	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDRGR	Active	Production	SON (DRG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A
INA333AIDRGR.A	Active	Production	SON (DRG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A
INA333AIDRGRG4	Active	Production	SON (DRG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A
INA333AIDRGRG4.A	Active	Production	SON (DRG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A
INA333AIDRGT	Active	Production	SON (DRG) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A
INA333AIDRGT.A	Active	Production	SON (DRG) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA333 :

- Automotive : [INA333-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA333AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA333AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA333AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA333AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA333AIDRGRG4	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA333AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA333AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
INA333AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA333AIDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
INA333AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA333AIDRGRG4	SON	DRG	8	3000	353.0	353.0	32.0
INA333AIDRGT	SON	DRG	8	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

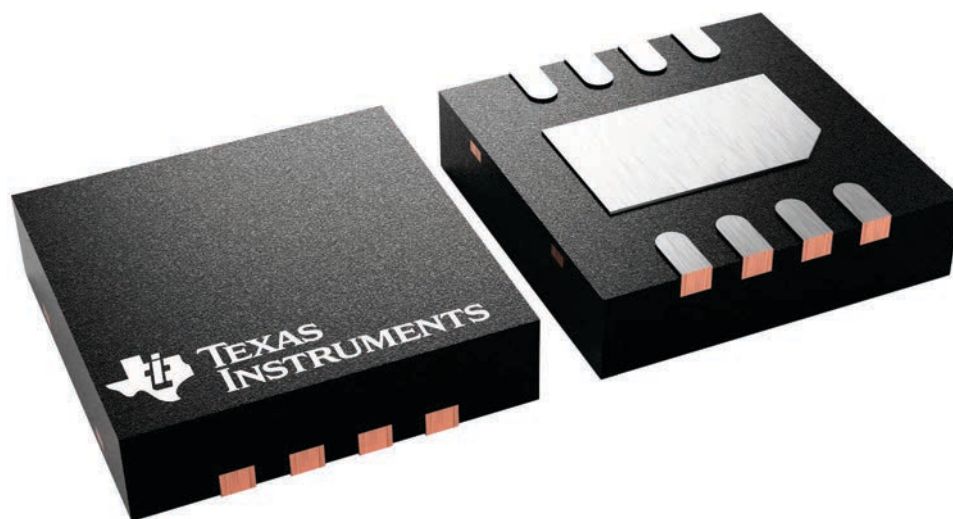
DRG 8

WSON - 0.8 mm max height

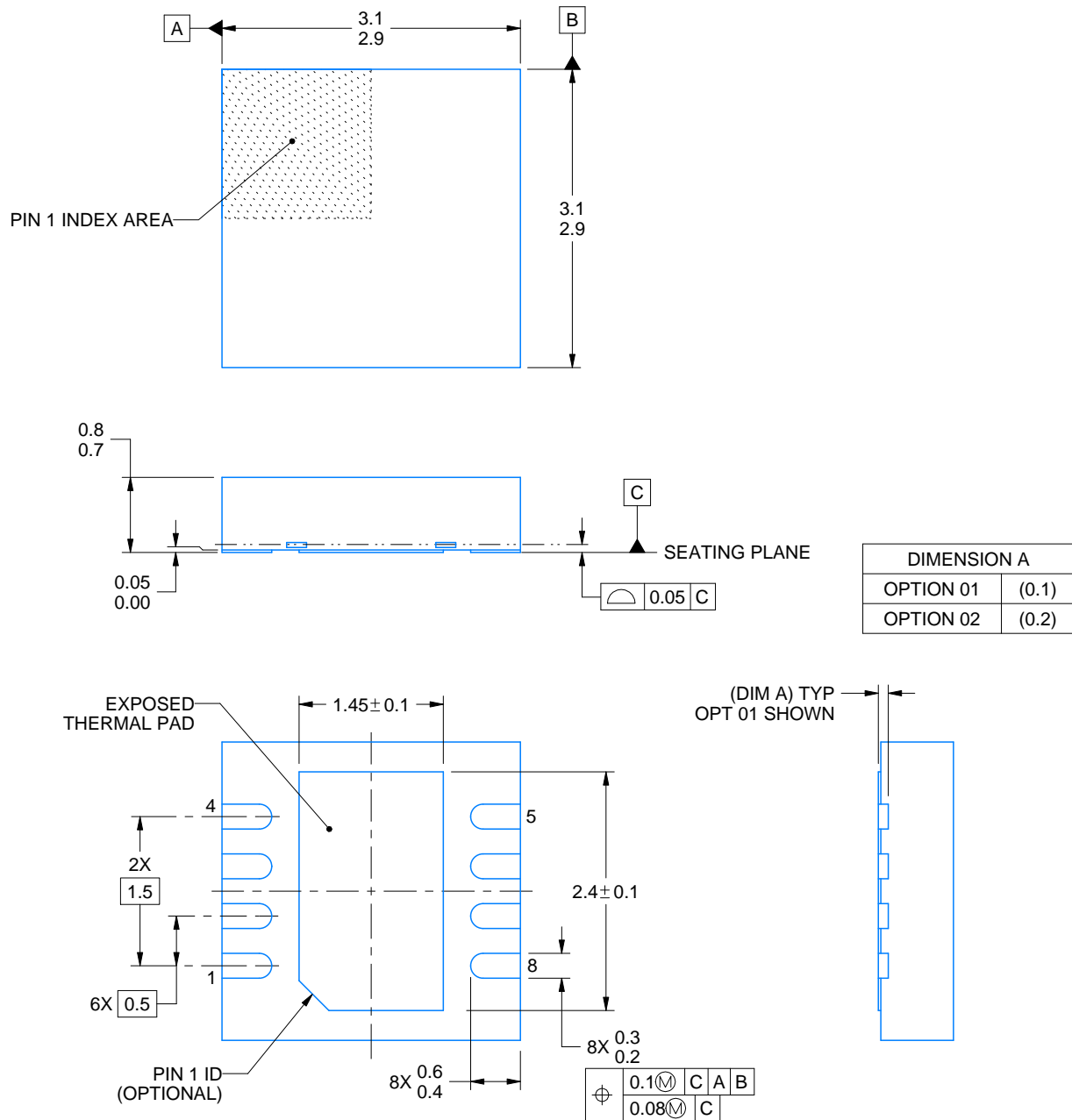
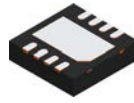
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225794/A



4218886/A 01/2020

NOTES:

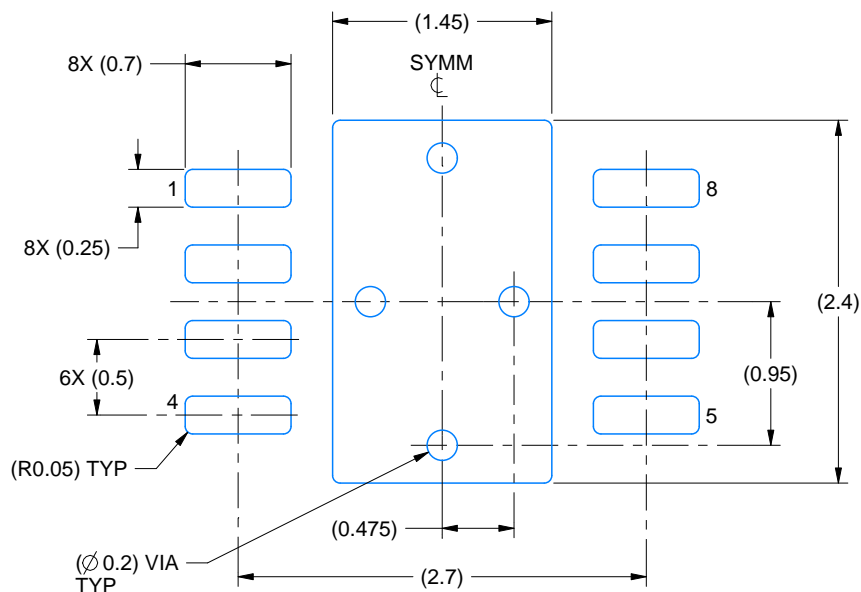
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

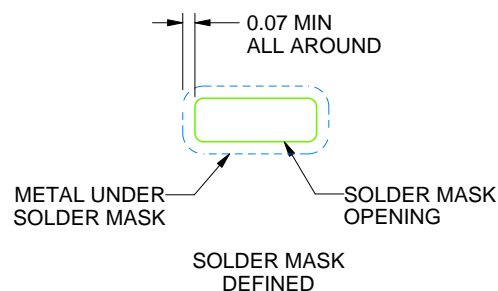
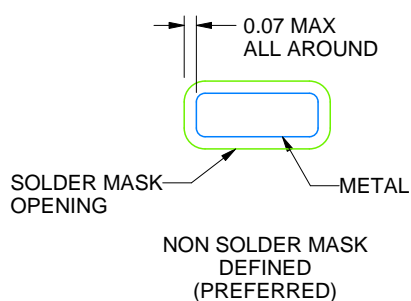
DRG0008B

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218886/A 01/2020

NOTES: (continued)

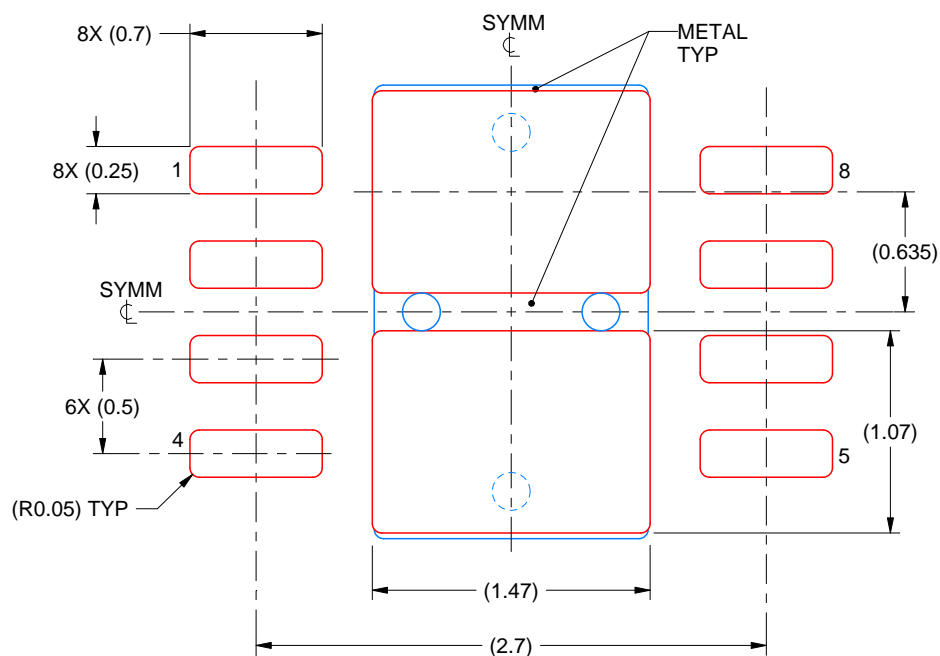
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRG0008B

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218886/A 01/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

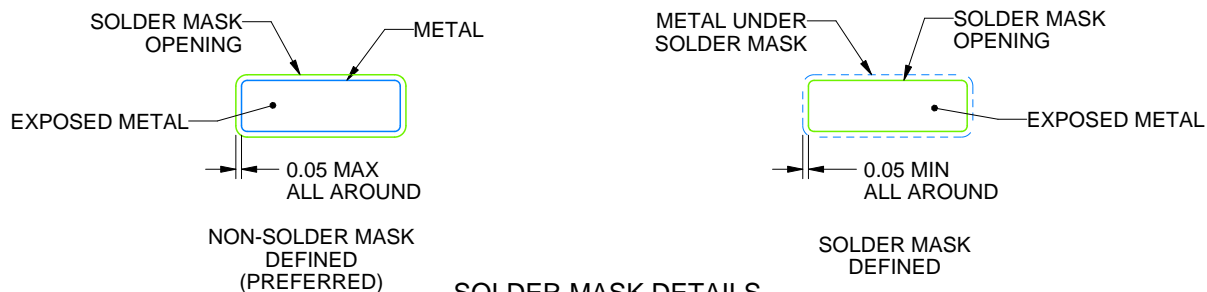
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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