# ESD321 采用 0402 和 SOD-523 封装的低电容（小于 1pF）单通道 30kV ESD 保护二极管

## 1 特性

- IEC 61000-4-2 4 级 ESD 保护：
  - ±30kV 接触放电
  - ±30kV 空气间隙放电
- IEC 61000-4-4 EFT 保护：
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护：
  - 6A (8/20μs)
- IO 电容：0.9pF（典型值）
- 直流击穿电压：4.5V（最小值）
- 低漏电流：0.1nA（典型值）
- 超低的 ESD 钳位电压：
  - 16A TLP 时为 6.8V（IO 至 GND）
  - $R_{DYN}$：0.13Ω（I/O 至 GND）
- 工业温度范围：-40°C 至 +125°C
- 业界通用的 0402 (DFN1006P2) 和 SOD-523 封装

## 2 应用

- 终端设备：
  - 可穿戴设备
  - 工业和服务机器人
  - 便携式计算机和台式机
  - 手机和平板电脑
  - 机顶盒
  - DVR 和 NVR
  - 电视和监视器
  - EPOS（电子销售点）
- 接口：
  - USB 2.0/1.1
  - GPIO
  - 以太网 10/100/1000Mbps
  - 按钮
  - 音频

## 3 说明

ESD321 是一款单向 TVS ESD 保护二极管，具有低动态电阻和低钳位电压。ESD321 的额定 ESD 冲击消散值高达 ±30kV，符合 IEC 61000-4-2 国际标准（高于 4 级）。

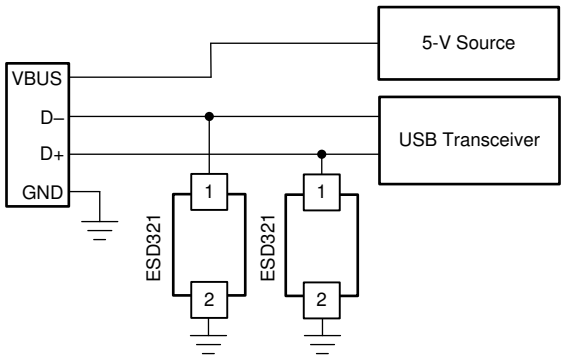
超低的动态电阻 (0.13Ω) 和极低的钳位电压（16A TLP 时为 6.8V）可确保针对瞬态事件提供系统级保护。该器件具有 0.9pF 的低 IO 电容，因此适用于保护 USB 2.0 和以太网 10/100/1000Mbps 等接口。

ESD321 采用业界通用的 0402 (DPY/DFN1006P2) 和 SOD-523 (DYA) 封装。

**封装信息**

| 器件型号 | 封装(1) | 封装尺寸(2) |
|---|---|---|
| ESD321 | DPY（X1SON，2） | 1mm × 0.6mm |
| | DYA（SOD-523，2） | 1.6mm × 0.8mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。




**USB 2.0 典型应用原理图**

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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# 4 Pin Configuration and Functions

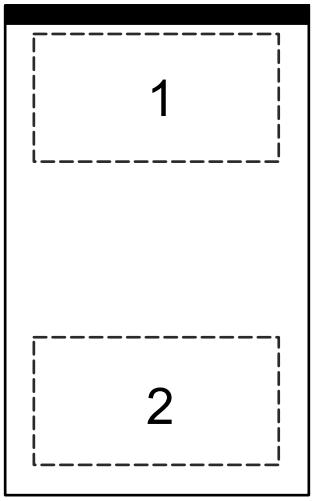



图 4-1. DPY Package, 2-Pin X1SON (Top View)

表 4-1. Pin Functions

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | DPY | | |
| IO | 1 | I/O | ESD Protected Channel. Connect to the line being protected. |
| GND | 2 | GND | Connect to ground. |

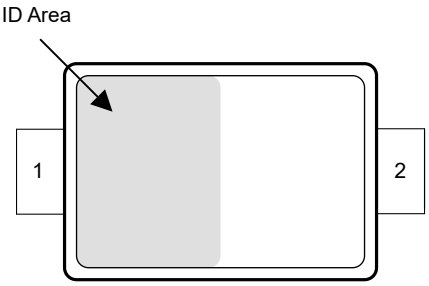



图 4-2. DYA Package, 2-Pin SOD-523 (Top View)

表 4-2. Pin Functions

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | DYA | | |
| IO | 2 | I/O | ESD Protected Channel. Connect to the line being protected. |
| GND | 1 | GND | Connect to ground. |

(1) I = input, O = output, GND = ground

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Electrical Fast Transient | IEC 61000-4-4 Peak Current at 25 °C | | 80 | A |
| Surge Pulse | IEC 61000-4-5 Surge (tp 8/20μs) Peak Power at 25 °C | | 40 | W |
| | IEC 61000-4-5 Surge (tp 8/20μs) Peak Current at 25 °C | | 6 | A |
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |
| $T_{stg}$ | Storage temperature | –65 | 155 | °C |

(1) Stresses beyond those listed under 节 5.1 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under 节 5.4. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings – JEDEC Specifications

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 ESD Ratings – IEC Specifications

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 Contact Discharge, all pins | ±30000 | V |
| | | IEC 61000-4-2 Air Discharge, all pins | ±30000 | |

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 0 | | 3.6 | V |
| $T_A$ | Operating Free Air Temperature | –40 | | 125 | °C |

## 5.5 Thermal Information

| THERMAL METRIC (1) | | ESD321 | | UNIT |
|---|---|---|---|---|
| | | DYA (SOD-523) | DPY (X1SON) | |
| | | 2 Pins | 2 Pins | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 774.7 | 437.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 462.3 | 249.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 541.1 | 169.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 164.4 | 99.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 534.6 | 168.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.


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## 5.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse stand-off voltage | $I_{IO}$ < 50nA, across operating temperature range | | | 3.6 | V |
| $I_{LEAKAGE}$ | Leakage current at 3.6V | $V_{IO}$ = 3.6V, I/O to GND | | 0.1 | 10 | nA |
| $V_{BRF}$ | Breakdown voltage, I/O to GND (1) | $I_{IO}$ = 1mA | 4.5 | | 7.5 | V |
| $V_{FWD}$ | Forward Voltage, GND to I/O (1) | $I_{IO}$ = 1mA | | 0.8 | | V |
| $V_{HOLD}$ | Holding voltage, I/O to GND (2) | $I_{IO}$ = 1mA | | 5.1 | | V |
| $V_{CLAMP}$ | Clamping voltage | $I_{PP}$ = 6A (8/20µs Surge), I/O to GND | | 6.3 | | V |
| | | $I_{PP}$ = 16A (100ns TLP), I/O to GND | | 6.8 | | V |
| | | $I_{PP}$ = 16A (100ns TLP), GND to I/O | | 4.7 | | V |
| $R_{DYN}$ | Dynamic resistance | I/O to GND, 100ns TLP, between 10 to 20A $I_{PP}$ | | 0.13 | | Ω |
| | | GND to I/O , 100ns TLP, between 10 to 20A $I_{PP}$ | | 0.2 | | Ω |
| $C_{LINE}$ | Line capacitance, IO to GND | $V_{IO}$ = 0V, $V_{p-p}$ = 30mV, f = 1MHz | | 0.9 | 1.1 | pF |

(1) $V_{BRF}$ and $V_{BRR}$ are defined as the voltage obtained at 1mA when sweeping the voltage up, before the device latches into the snapback state

(2) $V_{HOLD}$ is defined as the voltage when 1mA is applied, after the device has successfully latched into the snapback state.

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## 5.7 Typical Characteristics

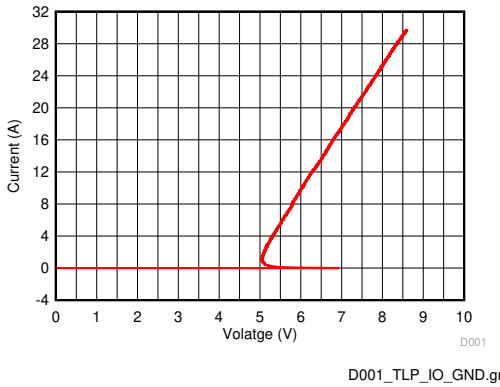



图 5-1. TLP I-V Curve, I/O Pin to GND ($t_p$ = 100ns)

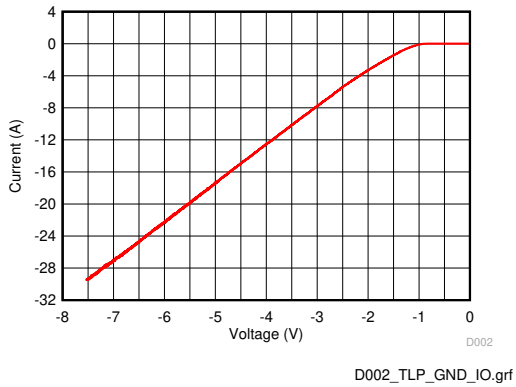



图 5-2. TLP I-V Curve, GND to I/O Pin ($t_p$ = 100ns)

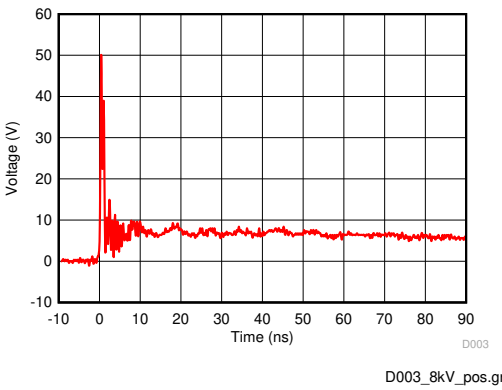



图 5-3. 8kV IEC 61000-4-2 Clamping Voltage Waveform, I/O Pin to GND

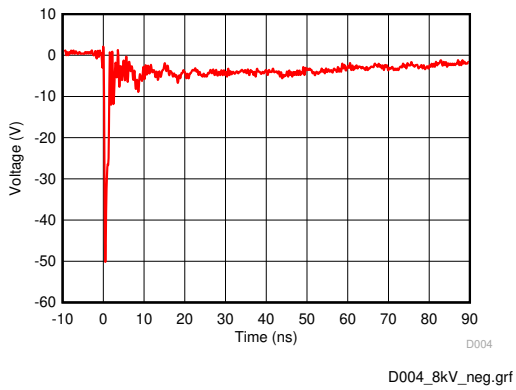



图 5-4. 8kV IEC 61000-4-2 Clamping Voltage Waveform, GND to I/O Pin

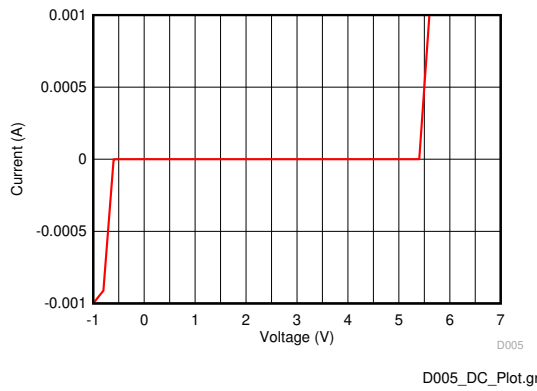



图 5-5. DC Voltage Sweep I-V Curve, I/O Pin to GND

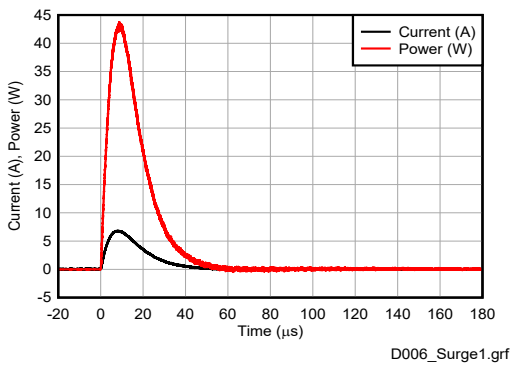



图 5-6. Surge Curve (IEC 61000-4-5, $t_p$=8/20µs), I/O Pin to GND


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## 5.7 Typical Characteristics (continued)

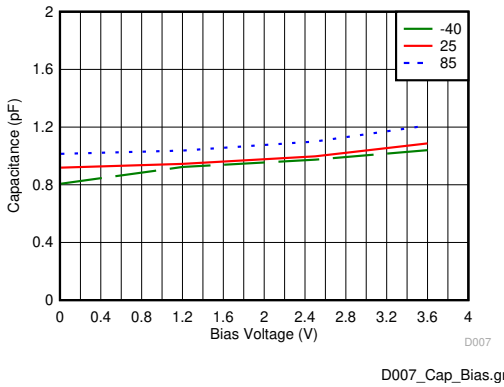



图 5-7. Capacitance vs. Bias Voltage For Different Temperatures (°C)

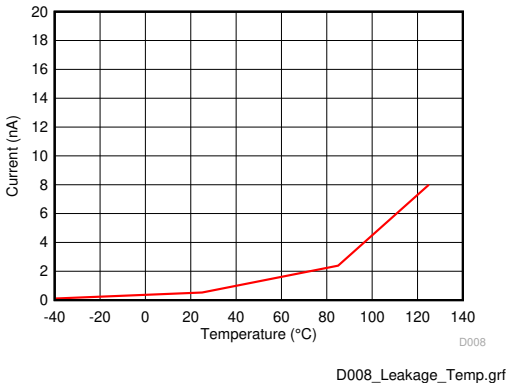



图 5-8. Leakage Current (at 3.6V Bias) Across Temperature, I/O Pin to GND

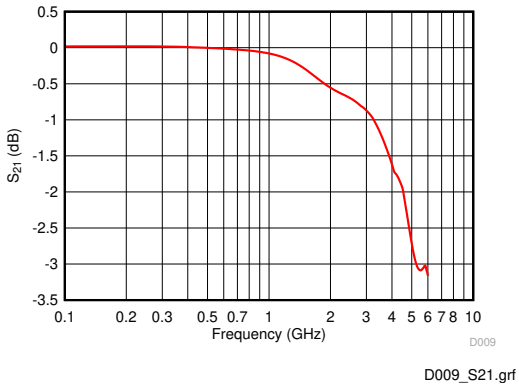



图 5-9. Insertion Loss vs. Frequency

# 6 Detailed Description

## 6.1 Overview

The ESD321 is a low capacitance uni-directional ESD Protection Diode with a low clamping voltage. This device can dissipate ESD strikes up to ±30kV (Contact and Air) per the IEC 61000-4-2 Standard. The low clamping makes this device suitable for protecting any ESD sensitive devices.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

ESD321 provides ESD protection up to ±30kV contact and ±30kV air gap per IEC 61000-4-2 standard. During an ESD event, ESD diode connected to the I/O pin turns on and diverts the current to ground. Additionally, ESD321 also provides protection against IEC 61000-4-5 Surge currents up to 6A (8/20µs waveform) and up to 80A per IEC 61000-4-4 (5/50ns waveform, 4kV with 50Ω impedance) electrical fast transient (EFT) standard. The capacitance between the I/O pin and ground is 0.9pF (typical) and 1.1pF (maximum). The device features a low leakage current of 0.1nA (typical) and 50nA (maximum, across operating temperature range) with a bias of 3.6V. The ESD diode at the I/O pin protects the ESD-sensitive devices by clamping the voltage to a low value of 6.8V ($I_{PP}$ = 16A 100ns TLP ). The layout makes adding protection to an existing layout simple. The package offers flow-through routing, requiring minimal modification to an existing layout.

## 6.4 Device Functional Modes

The ESD321 is a passive integrated circuit that triggers when voltages exceed $V_{BRF}$ or fall below $V_{FWD}$. During ESD events, voltages as high as ±30kV (contact or air) can be directed to ground through the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD321 (typically within 10ns) the device returns to passive.


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# 7 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 7.1 Application Information

The ESD321 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low $R_{DYN}$ of the triggered TVS holds this voltage, $V_{CLAMP}$, to a safe level for the protected IC.

## 7.2 Typical Application

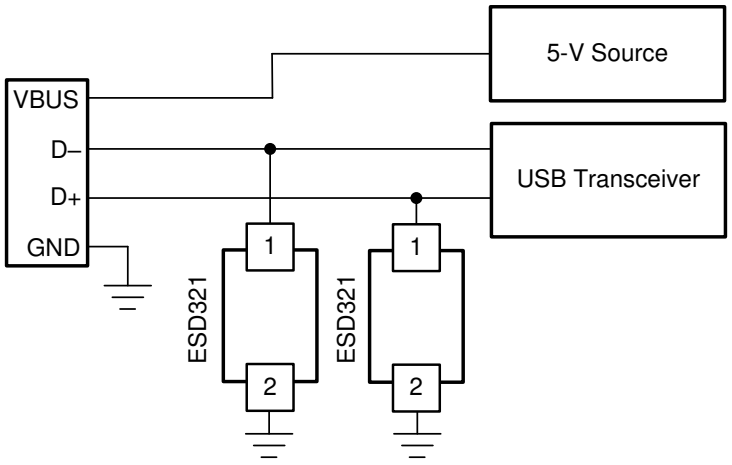



图 7-1. USB 2.0 ESD Schematic

### *7.2.1 Design Requirements*

For this design example, two ESD321 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in 表 7-1 are known.

表 7-1. Design Parameters

| DESIGN PARAMETER | VALUE |
|---|---|
| Signal range on DP-DM lines | 0V to 3.6V |
| Operating frequency on DP-DM lines | up to 240MHz |

### *7.2.2 Detailed Design Procedure*

#### 7.2.2.1 Signal Range

The ESD321 supports signal ranges between 0V and 3.6V, which supports the USB 2.0 signal pair on the USB 2.0 application.

#### 7.2.2.2 Operating Frequency

The ESD321 has a 0.9pF (typical) capacitance, which supports the USB 2.0 data rates of 480Mbps.

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### 7.2.3 Application Curve

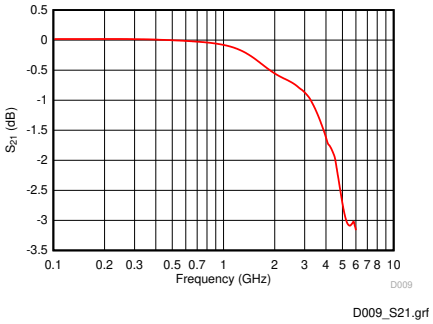



**图 7-2. Insertion Loss Vs. Frequency**

## 7.3 Power Supply Recommendations

Because the ESD321 is a passive ESD device, there is no need to power it. To help ensure the device functions properly, do not violate the recommended I/O specification (0V to 3.6V).

## 7.4 Layout

### 7.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, which increases EMI coupling.


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### 7.4.2 Layout Example

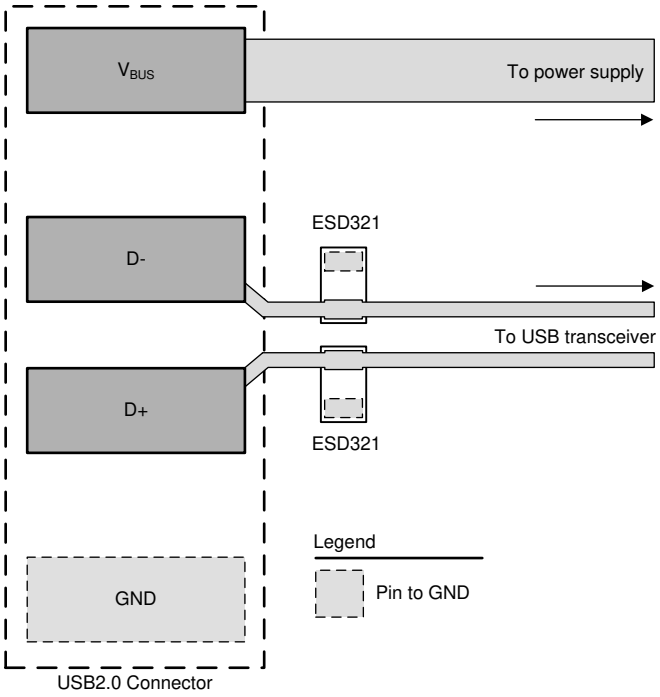



**图 7-3. USB 2.0 ESD Layout**

# 8 Device and Documentation Support

## 8.1 Documentation Support

### *8.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *Generic ESD Device Evaluation Module*

## 8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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## 8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision B (October 2023) to Revision C (June 2025) | Page |
|---|---|
| • Separated pinout information into two tables | 3 |

| Changes from Revision A (December 2022) to Revision B (October 2023) | Page |
|---|---|
| • 更新了*封装信息* 表以包含封装尺寸 | 1 |
| • Changed voltage to power in the *Surge Curve (IEC 61000-4-5, $t_p$=8/20µs), I/O Pin to GND* figure | 6 |

| Changes from Revision * (July 2018) to Revision A (December 2022) | Page |
|---|---|
| • 更新了整个文档中的表格、图和交叉参考的编号格式 | 1 |
| • 向数据表添加了 *DYA* 封装 | 1 |


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## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ESD321DPYR | Active | Production | X1SON (DPY) \| 2 | 10000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | DD |
| ESD321DPYR.B | Active | Production | X1SON (DPY) \| 2 | 10000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 150 | DD |
| ESD321DPYRG4 | Active | Production | X1SON (DPY) \| 2 | 10000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | DD |
| ESD321DPYRG4.B | Active | Production | X1SON (DPY) \| 2 | 10000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | DD |
| ESD321DYAR | Active | Production | SOT-5X3 (DYA) \| 2 | 3000 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -55 to 150 | 1L8 |
| ESD321DYAR.B | Active | Production | SOT-5X3 (DYA) \| 2 | 3000 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | 1L8 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

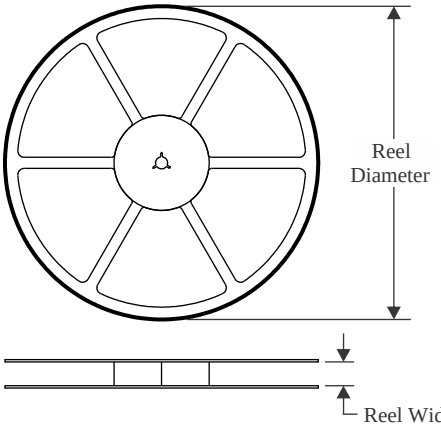
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

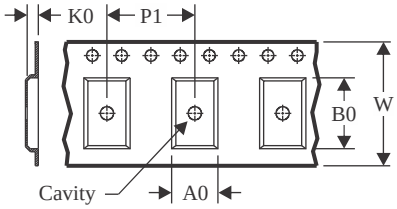
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

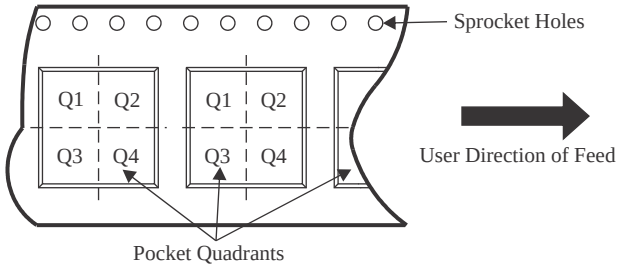



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

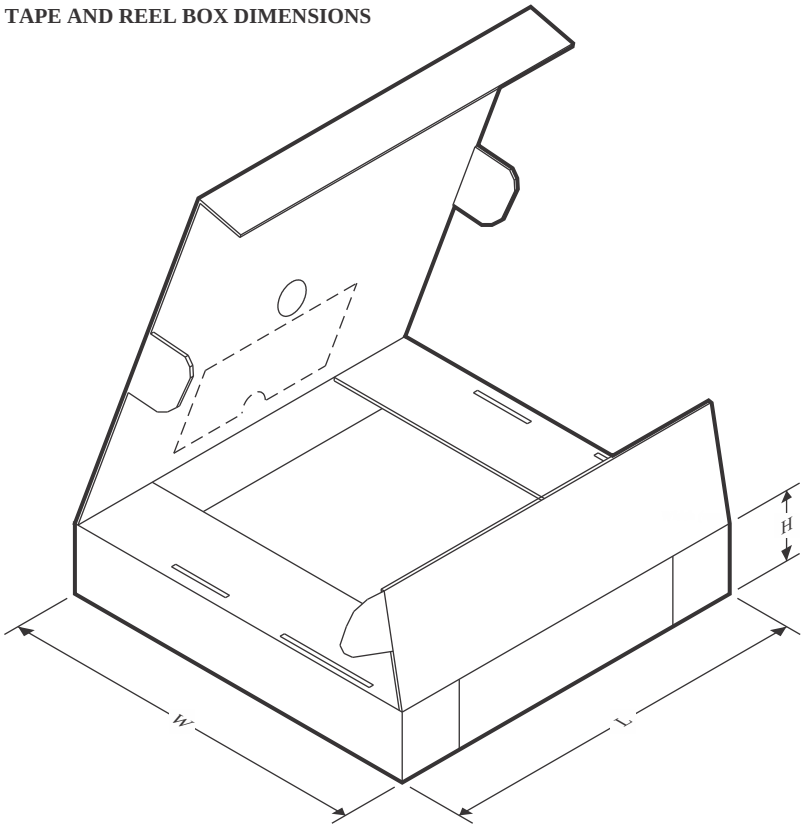
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ESD321DPYR | X1SON | DPY | 2 | 10000 | 178.0 | 8.4 | 0.7 | 1.15 | 0.47 | 2.0 | 8.0 | Q1 |
| ESD321DYAR | SOT-5X3 | DYA | 2 | 3000 | 178.0 | 9.5 | 0.5 | 1.94 | 0.73 | 2.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ESD321DPYR | X1SON | DPY | 2 | 10000 | 205.0 | 200.0 | 33.0 |
| ESD321DYAR | SOT-5X3 | DYA | 2 | 3000 | 210.0 | 200.0 | 42.0 |

# GENERIC PACKAGE VIEW

## DPY 2

## X1SON - 0.45 mm max height

**1 x 0.6 mm**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



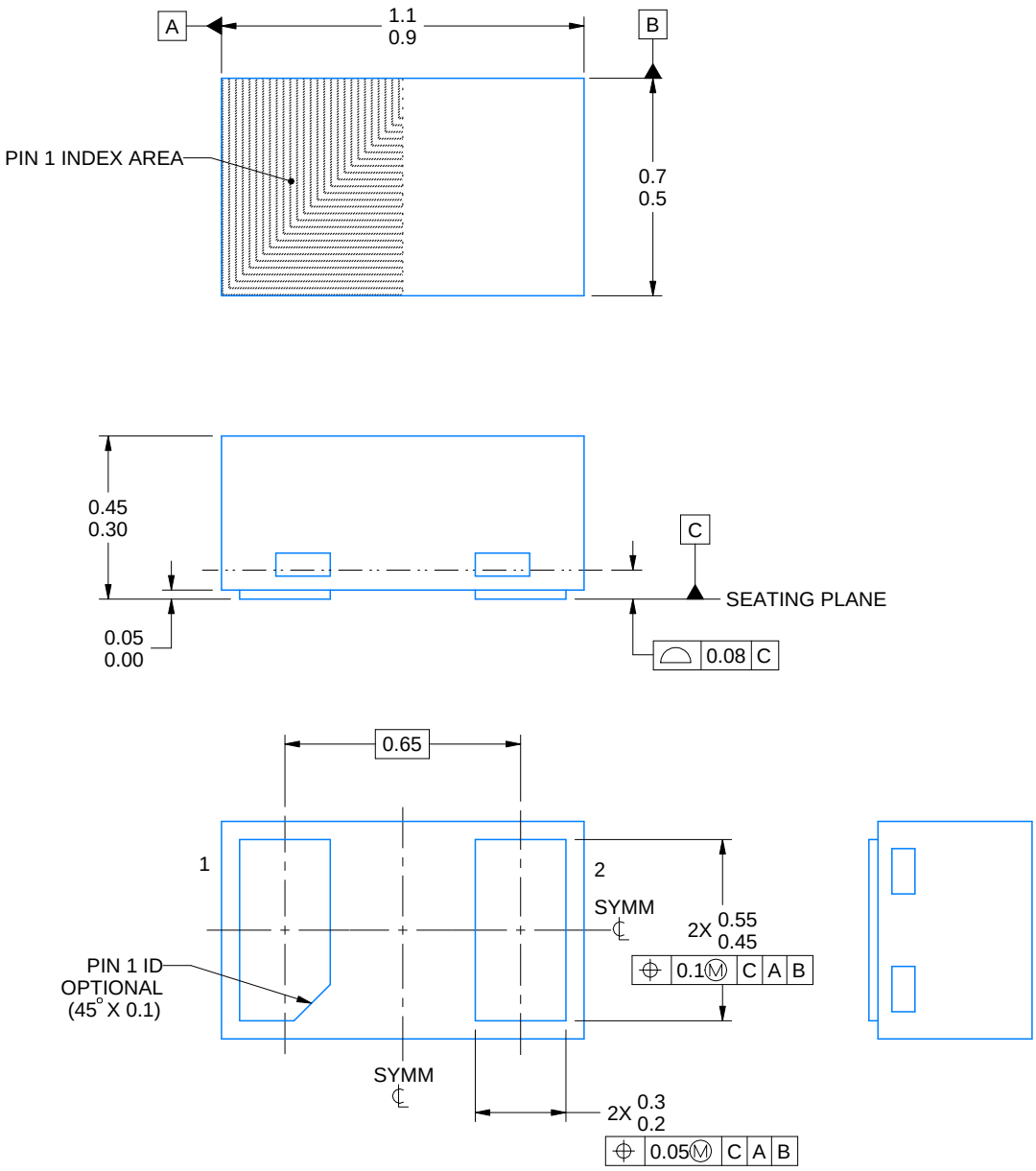

4231484/A

# PACKAGE OUTLINE

## DPY0002A

## X1SON - 0.45 mm max height

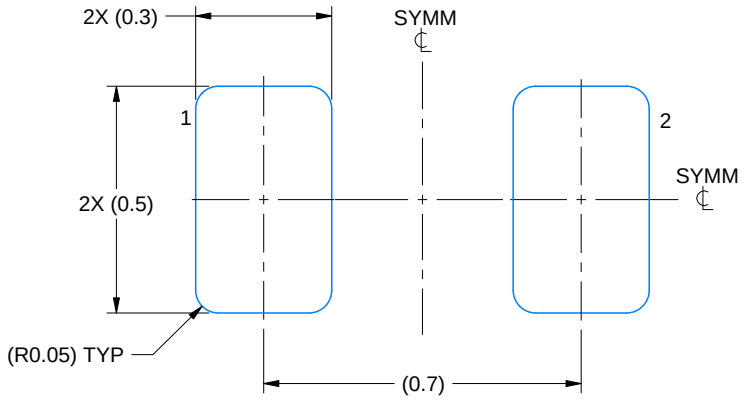
PLASTIC SMALL OUTLINE - NO LEAD



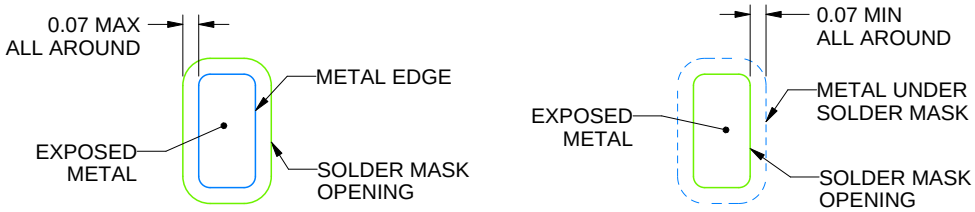

4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

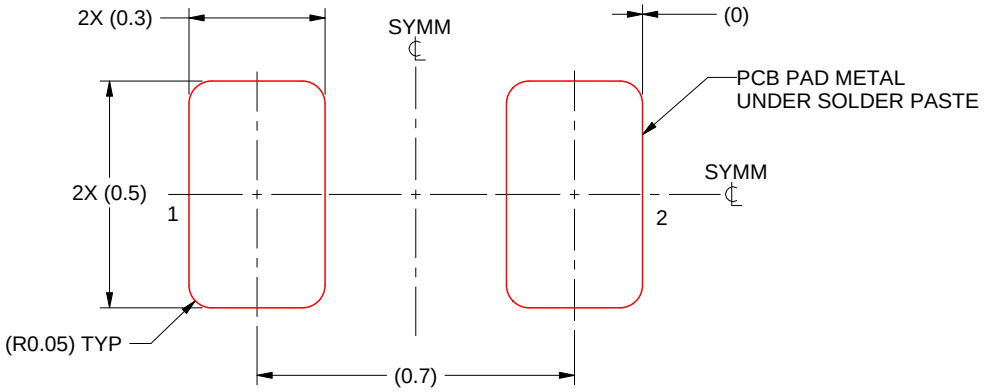



SOLDER MASK DETAILS

4224561/C 07/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

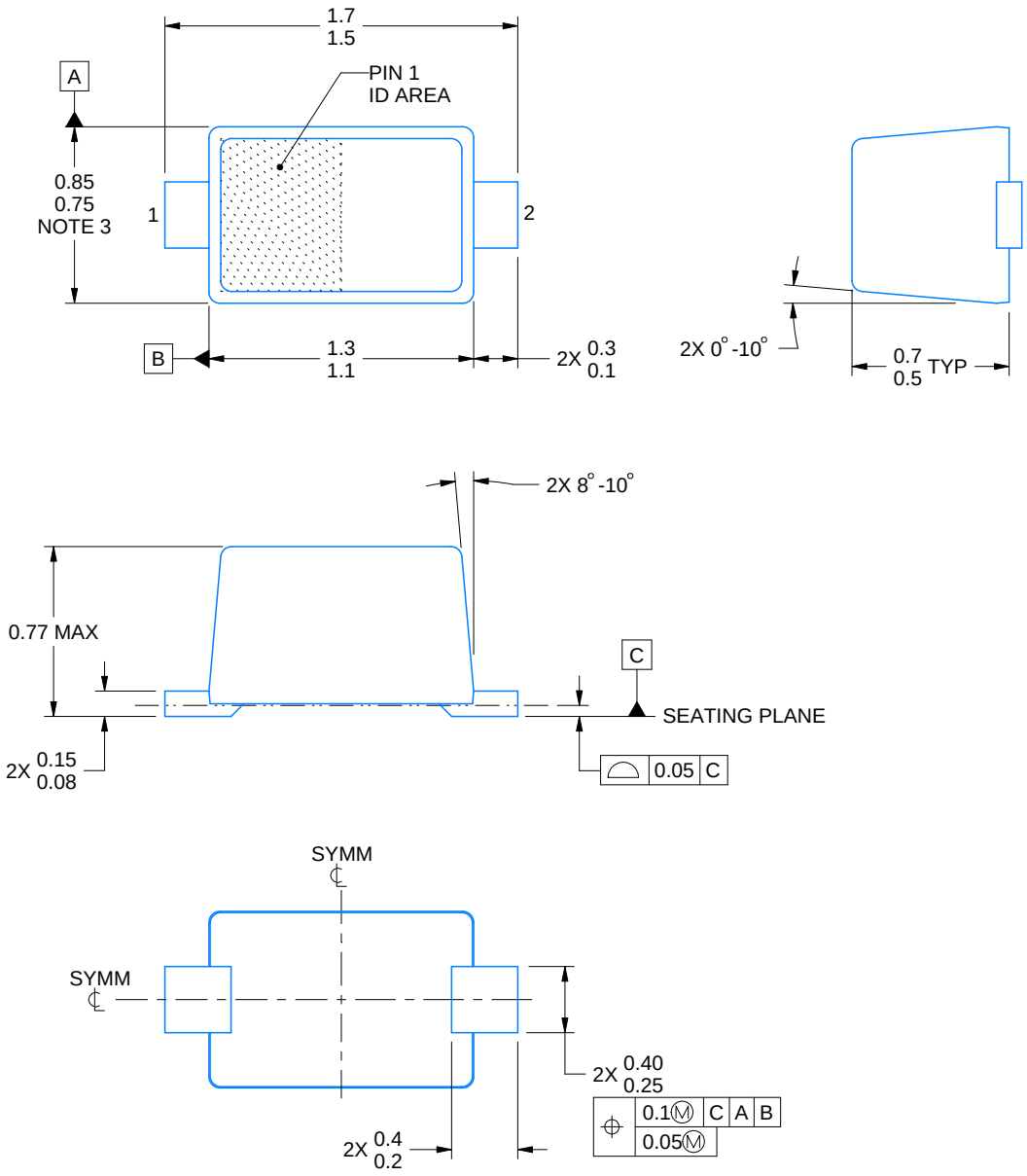
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DYA0002A

## SOT (SOD-523) - 0.77 mm max height

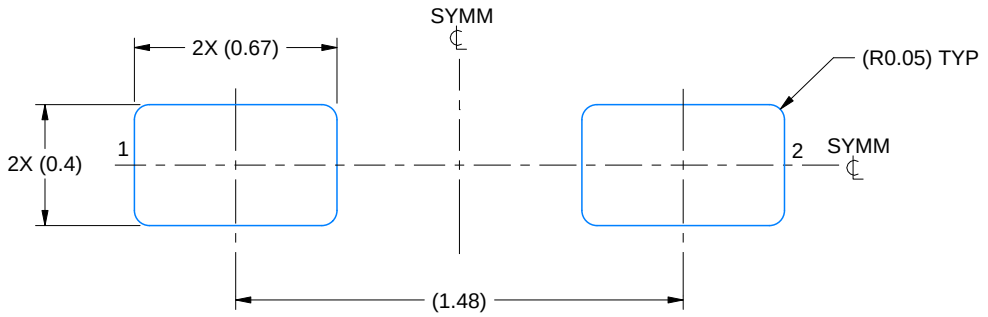
PLASTIC SMALL OUTLINE



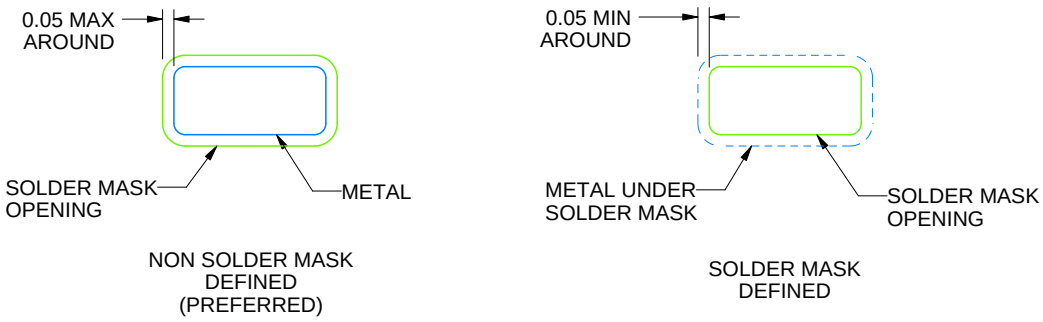

4224978/D 08/2026

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height




LAND PATTERN EXAMPLE
SCALE:40X

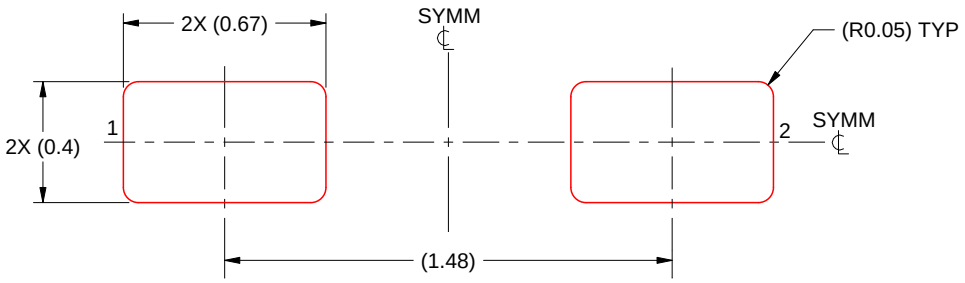



SOLDERMASK DETAILS

4224978/D 08/2026

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4224978/D 08/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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