

用于 HDMI 接口的 ESD224 低钳位 4 通道 ESD 保护器件

1 特性

- IEC 61000-4-2 4 级静电放电 (ESD) 保护
 - ±12kV 接触放电
 - ±15kV 气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
 - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
 - 2A (8/20µs)
- IO 电容:
 - 0.5pF (典型值)
- 符合 HDMI 2.0 标准
- 超低泄漏电流: 0.1nA (典型值)
- 超低 ESD 钳位电压: 在 16A TLP 下为 8V (系统侧)
- 支持速率最高达 6Gbps 的高速接口
- 工业温度范围: -40°C 至 +125°C
- 行业标准 DQA 封装

2 应用

- 终端设备
 - 机顶盒
 - 电视和监视器
 - 便携式计算机和台式机
 - DVD、蓝光、多媒体播放器
- 接口
 - HDMI 2.0/1.4
 - 以太网 10/100/1000Mbps
 - USB 3.0

3 说明

ESD224 是一款适用于高速应用 (如 USB 3.0 和 HDMI 2.0) 的双向 TVS ESD 保护二极管阵列。ESD224 的额定 ESD 冲击消散值达到了 IEC 61000-4-2 (4 级) 国际标准中规定的最高水平。ESD224 采用片上差分匹配的串联元件提高下行 ESD 钳位性能, 同时能够保持高速接口的信号符合性。ESD224 片上 ESD 保护网络提供超低钳位性能和高差分带宽, 使器件符合 HDMI 2.0 标准, 并且为下行 HDMI 器件提供稳健的保护。

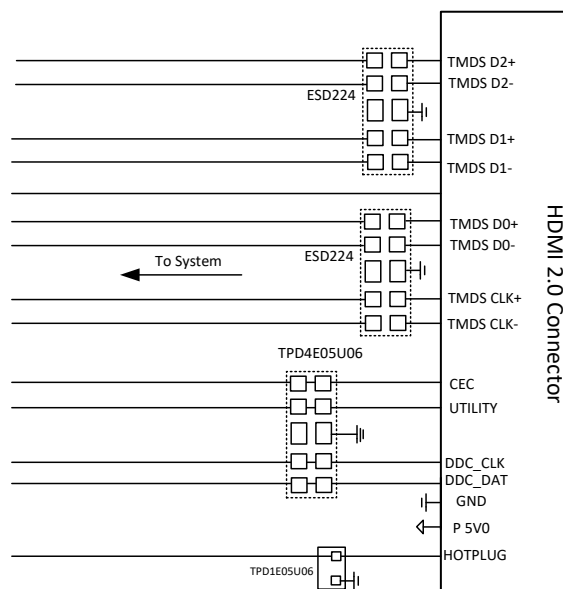
ESD224 采用符合行业标准的 USON-10 (DQA) 封装。该封装采用 0.5mm 引脚间距, 能够简化实现并缩短设计时间。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
ESD224	USON (10)	2.50mm x 1.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

典型应用原理图



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4 修订历史记录

Changes from Original (February 2018) to Revision A

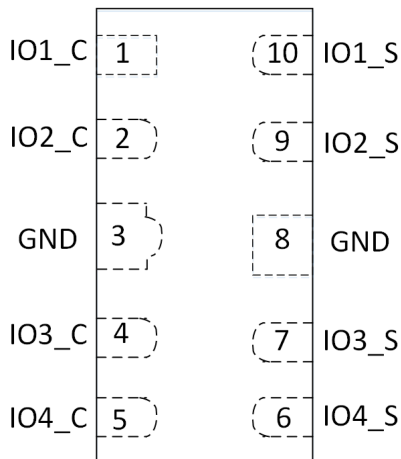
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• 已更改 将产品状态从“预告信息”更改成了“生产数据”	1
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5 Pin Configuration and Functions

**DQA Package
10-Pin USON
Top View**

Top View



USON-10 2.5 mm x 1.0 mm, 0.5 mm pitch

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	3	Ground	Ground. Connect to ground. These pins are shorted internally.
GND	8		
IO1_C	1	Connector Side I/O	ESD protected channel to be connected to the connector
IO2_C	2		
IO3_C	4		
IO4_C	5		
IO4_S	6	System Side I/O Pin corresponding to IO4_C	To be connected to the system side
IO3_S	7	System Side I/O Pin corresponding to IO3_C	
IO2_S	9	System Side I/O Pin corresponding to IO2_C	
IO1_S	10	System Side I/O Pin corresponding to IO1_C	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Electrical Fast Transient	IEC 61000-4-4 Peak Current at 25°C		80	A
Peak Pulse	IEC 61000-4-5 Surge (t _p 8/20 μs) Peak Power at 25°C		17	W
	IEC 61000-4-5 Surge (t _p 8/20 μs) Peak Current at 25°C		2	A
T _A	Operating free-air temperature	-40	125	°C
T _{stg}	Storage temperature	-65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings -JEDEC Specifications

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±12000
		IEC 61000-4-2 Air Discharge, all pins	±15000

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	-3.6		3.6	V
T _A	Operating Free Air Temperature	-40		125	°C

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾	ESD224		UNIT
	DQA (USON)		
	10 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	173.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	109.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	77.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	77.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

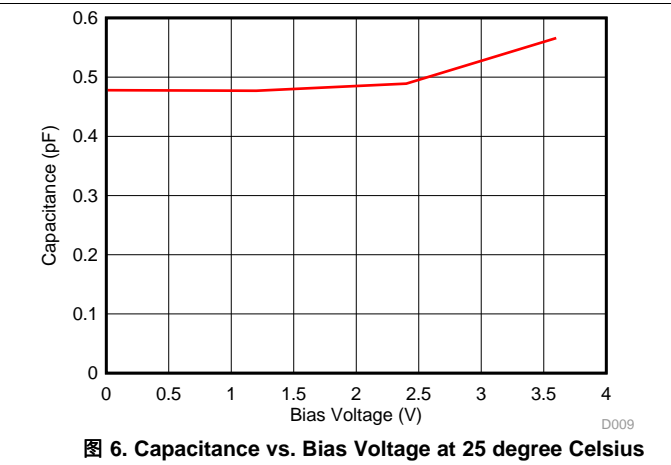
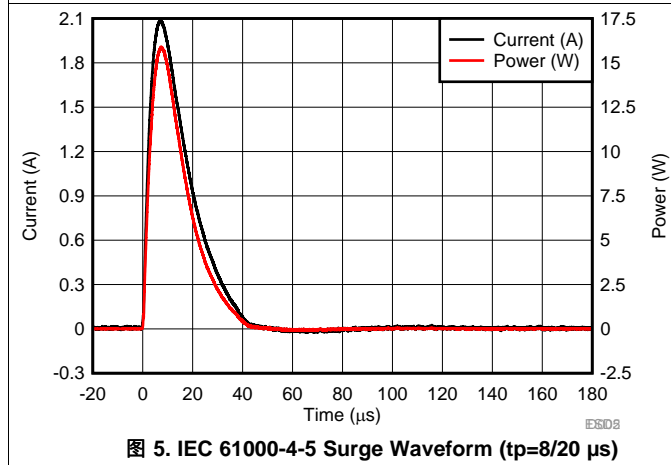
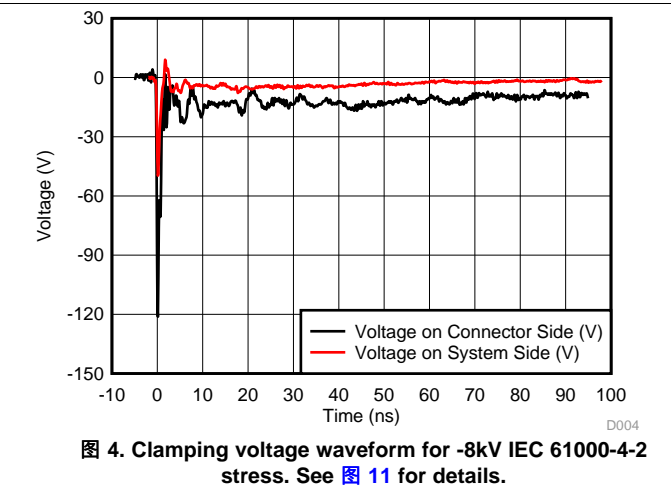
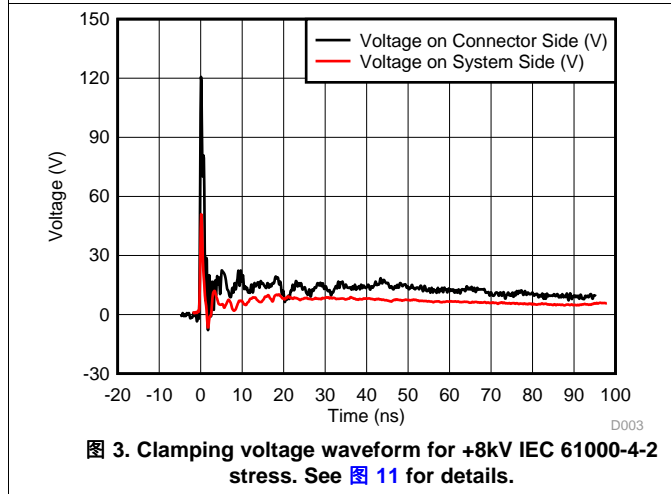
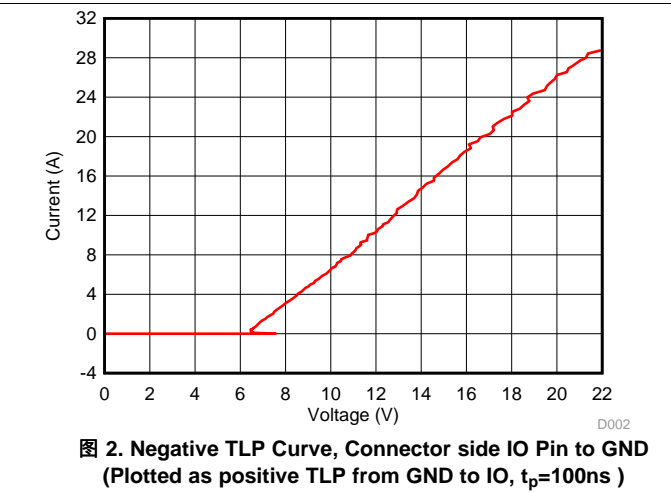
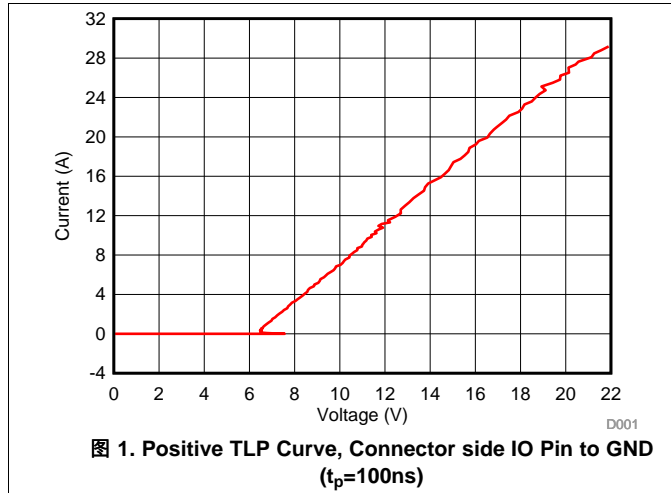
At $T_A = 25^\circ\text{C}$ unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	$I_{IO} < 10 \text{ nA}$, across operating temperature range	-3.6		3.6	V
V_{BRF}	Breakdown voltage, Pin 1, 2, 4, 5 to 3 (GND) ⁽¹⁾	$I_{IO} = 1 \text{ mA}$	5		7.9	V
V_{BRR}	Reverse breakdown voltage, pin 1, 2, 4, 5 to 3 (GND) ⁽¹⁾	$I_{IO} = -1 \text{ mA}$	-7.9		-5	V
V_{HOLD}	Holding voltage, pin1, 2, 4, 5 to 3 (GND) and 3 (GND) to pin 1, 2, 4, 5 ⁽²⁾	$I_{IO} = 1 \text{ mA}$		6.3		V
$V_{HOLD-NEG}$	Breakdown voltage, pin1, 2, 4, 5 to 3 (GND) ⁽²⁾	$I_{IO} = -1 \text{ mA}$		-6.3		V
V_{CLAMP}	TLP Clamping voltage (Intrinsic)	IPP = 1 A, pin 1, 2, 4, 5 to 3 or 8(GND), GND to pin 1, 2, 4, 5		7		V
		IPP = 5 A, pin 1, 2, 4, 5 to 3 or 8(GND), GND to pin 1, 2, 4, 5		9		V
		IPP = 16 A, pin 1, 2, 4, 5 to 3 or 8(GND), GND to pin 1, 2, 4, 5		14		V
$V_{CLAMP-IEC-SYS}$	IEC 61000-4-2 30 ns Clamping voltage (system side) assuming system draws at least 3 A of current at 8 V. See measurement setup.	8-kV Contact discharge on pin 1, 2, 4, 5 with pin3 grounded. Voltage waveform measured at pin 6, 7, 9, 10 with respect to GND		8		V
		-8-kV Contact discharge on pin 1, 2, 4, 5 with pin3 grounded. Voltage waveform measured at pin 6, 7, 9, 10 with respect to GND		-5		V
R_{DYN}	Dynamic resistance	Pin 1, 2, 4, 5 to GND, 100 ns TLP		0.5		Ω
		GND to Pin 1, 2, 4, 5, 100 ns TLP		0.5		
C_{LINE}	Line capacitance, any IO to GND	$V_{IO} = 0 \text{ V}$, $V_{p-p} = 30 \text{ mV}$, $f = 1 \text{ MHz}$		0.5	0.6	pF
ΔC_{LINE}	Variation of line capacitance	$C_{LINE1} - C_{LINE2}$, $V_{IO} = 0 \text{ V}$, $V_{p-p} = 30 \text{ mV}$, $f = 1 \text{ MHz}$		0.02	0.07	pF
C_{CROSS}	Line-to-line capacitance between one differential pair to another differential pair	$V_{IO} = 0 \text{ V}$, $V_{rms} = 30 \text{ mV}$, $f = 1 \text{ MHz}$		0.28		pF
S_{21DC}	DC Insertion Loss	DC insertion loss at Ch1, Ch2, Ch3, Ch4		0.3		dB
$I_{leakage}$	Leakage Current	$V_{IO} = \pm 3.6 \text{ V}$, Pin 1,2,4,5 to Pin 3		0.1	10	nA

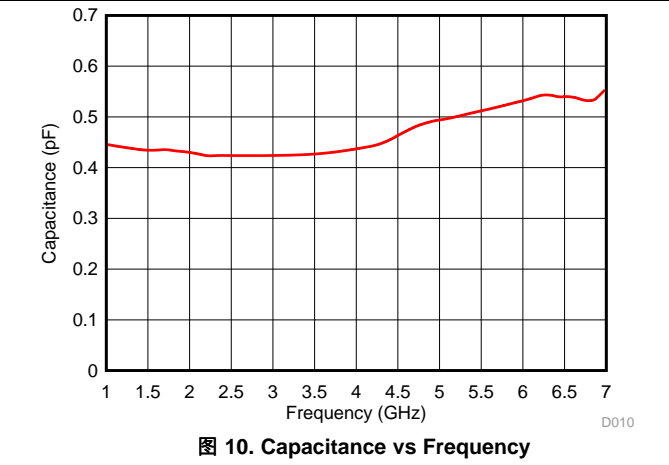
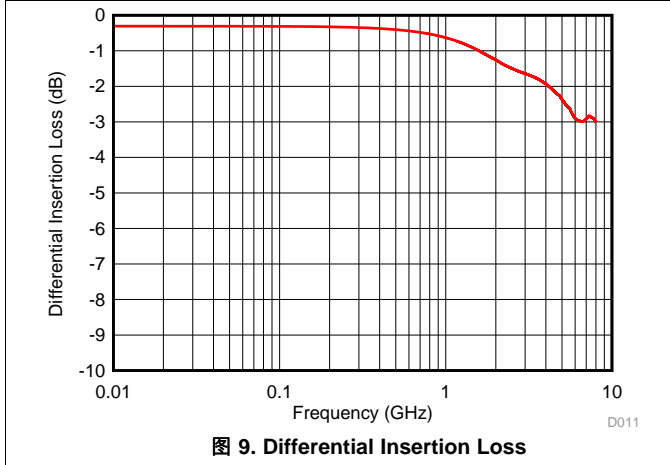
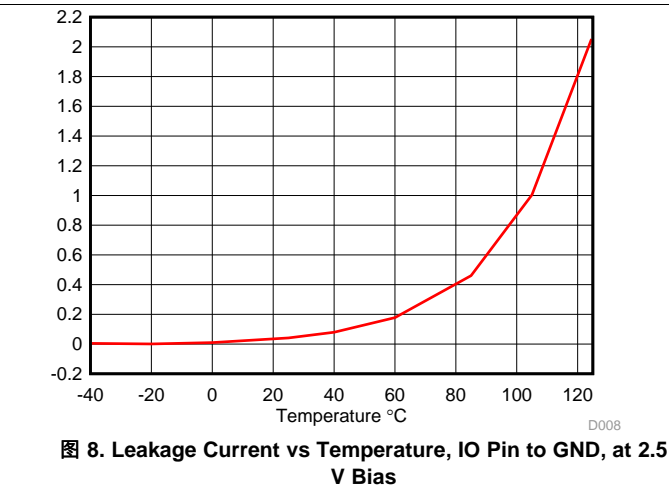
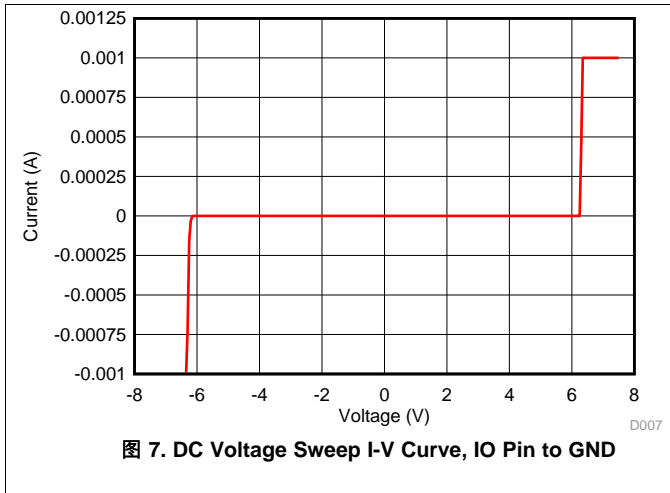
(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state

(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

6.7 Typical Characteristics



Typical Characteristics (接下页)



7 Parameter Measurement Setup

7.1 IEC 61000-4-2 System Level ESD Test Setup with HDMI Driver for Clamping Voltage Measurement

图 11 shows the setup used to perform System Level ESD test to evaluate the clamping performance of ESD224 in real-world applications where the device is protecting a downstream HDMI driver System-on-Chip. IEC 61000-4-2 8kV Contact stress was applied at the connector pin and the voltage waveform on the system-side pin was captured to look at the clamping voltage presented by ESD224 to the down stream HDMI driver.

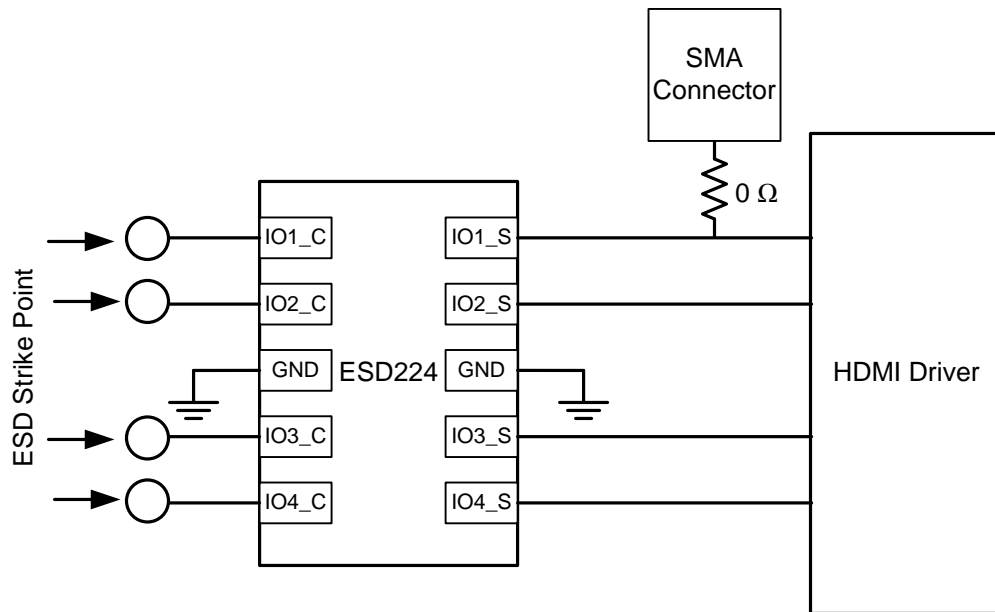


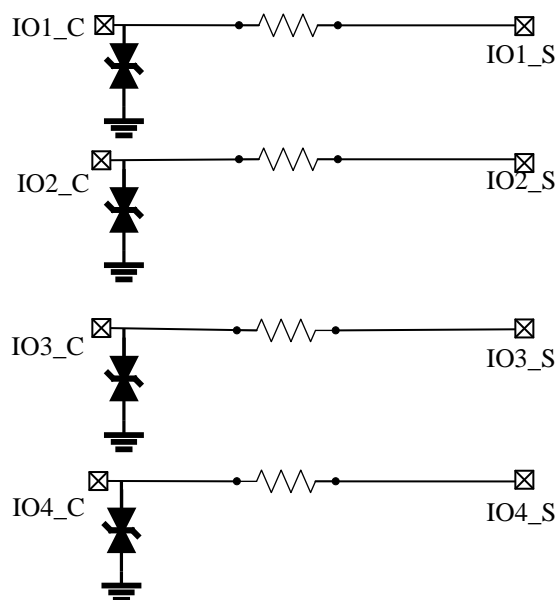
图 11. System Level IEC 61000-4-2 ESD Test Setup with ESD224 protecting an HDMI driver chip

8 Detailed Description

8.1 Overview

The ESD224 is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ± 12 -kV contact and ± 15 -kV air gap. The ESD-surge clamp diverts the current to ground.

8.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50- Ω impedance). The ESD-surge clamp diverts the current to ground.

8.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2 A and 17 W (8/20 μ s waveform). The ESD-surge clamp diverts this current to ground.

8.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.5 pF (typical). This device supports data rates up to 6 Gbps.

8.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of ± 5.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ± 3.6 V.

Feature Description (接下页)

8.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of ± 2.5 V.

8.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8 V ($I_{PP} = 16$ A TLP) on the system side pins when the system draws at least 3 A.

8.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 6 Gbps, because of the extremely low IO capacitance.

8.3.9 Industrial Temperature Range

This device features an industrial operating range of -40°C to $+125^{\circ}\text{C}$.

8.4 Device Functional Modes

The ESD224 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR} . During ESD events, voltages as high as ± 15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD224 (usually within 100s of nano-seconds) the device reverts to passive.

9 Application and Implementation

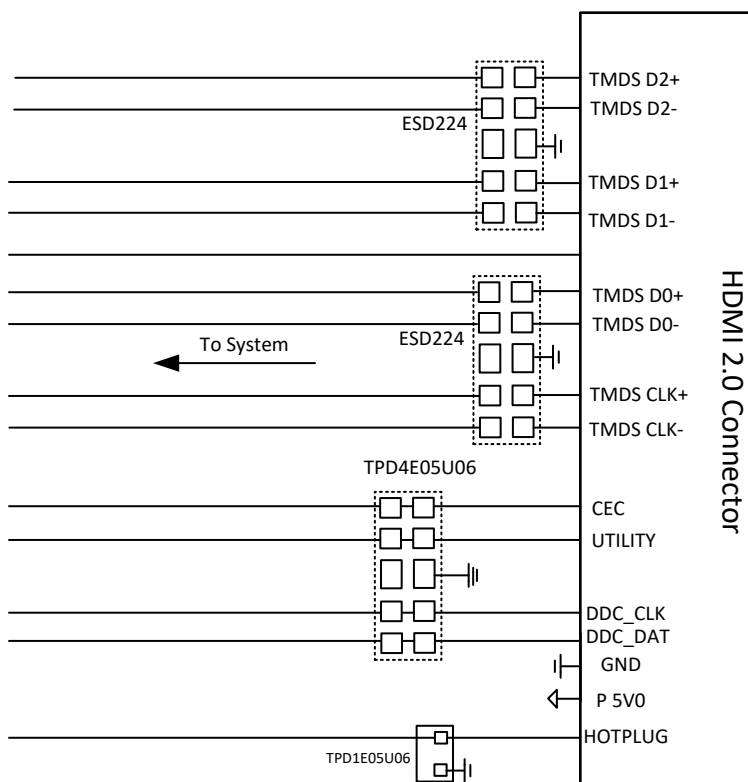
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ESD224 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. Part of this voltage drop across the diode drops across the series element between the connector side pin and the system-side pin. Therefore, the effective voltage drop across the protected IC is smaller than the voltage drop across the diode. It is recommended to avoid through-routing for this ESD diode (single trace connecting both the connector side pin and the system side pin) for the best ESD performance.

9.2 Typical Application



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图 12. ESD224 Protecting the HDMI Interface

Typical Application (接下页)

9.2.1 Design Requirements

In this design example, two ESD224 devices, one TPD4E05U06 and one TPD1E05U06 device are used to protect an HDMI 2.0 interface. For HDMI 2.0 application design parameters listed in 表 1 are known.

表 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on high speed differential data lines	0 to 3.6 V
Operating frequency of high speed data lines	3 GHz (First Harmonic)
Signal range on control lines (CEC, UTILITY, DDC_CLK and DDC_DAT)	0 to 5 V

9.2.2 Detailed Design Procedure

9.2.2.1 Signal Range

ESD224 supports signal ranges between -3.6 V and 3.6 V , which supports the high-speed lines on the HDMI 2.0 application. The TPD4E05U06 and TPD1E05U06 support signal ranges between 0 V and 5.5 V , which supports the HDMI control lines.

9.2.2.2 Operating Frequency

The ESD224 has a 0.5 pF (typical) capacitance, which supports the HDMI 2.0 rate of 6 Gbps . The TPD4E05U06 and TPD1E05U06 have a typical capacitance of 0.5 pF and 0.42 pF respectively, which easily support the control lines. The ESD224 has 4 identical protection channels for the differential HDMI high-speed signal lines. The symmetrical pin out of the device with a ground pin between the two differential signal pins makes it suitable for this application.

9.2.3 Application Curves

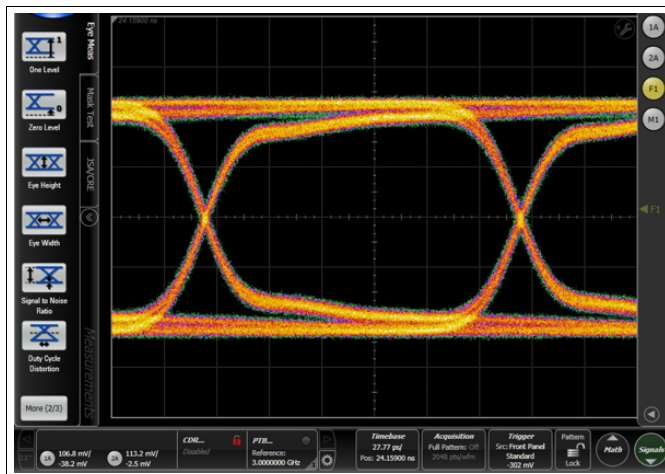


图 13. HDMI 2.0 6 Gbps Eye Diagram (Bare Board)

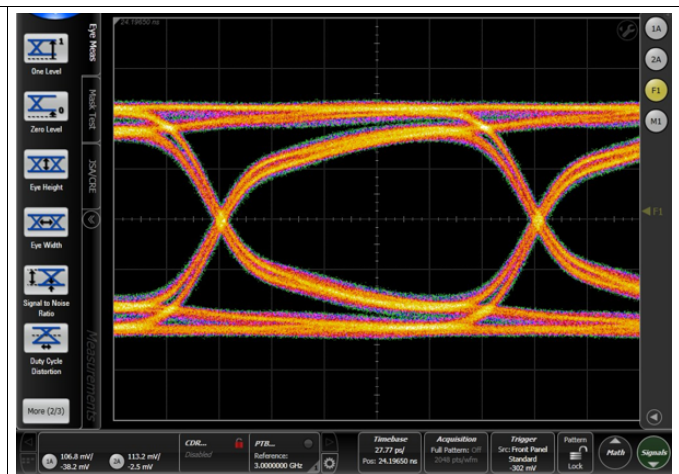


图 14. HDMI 2.0 6 Gbps Eye Diagram with ESD224

10 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- For the best ESD performance, do not use through-routing for the data channels. Connecting pins 1 and 10, 2 and 9, 4 and 7, 5 and 6 together with through routing will reduce the clamping voltage performance of ESD224.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Examples

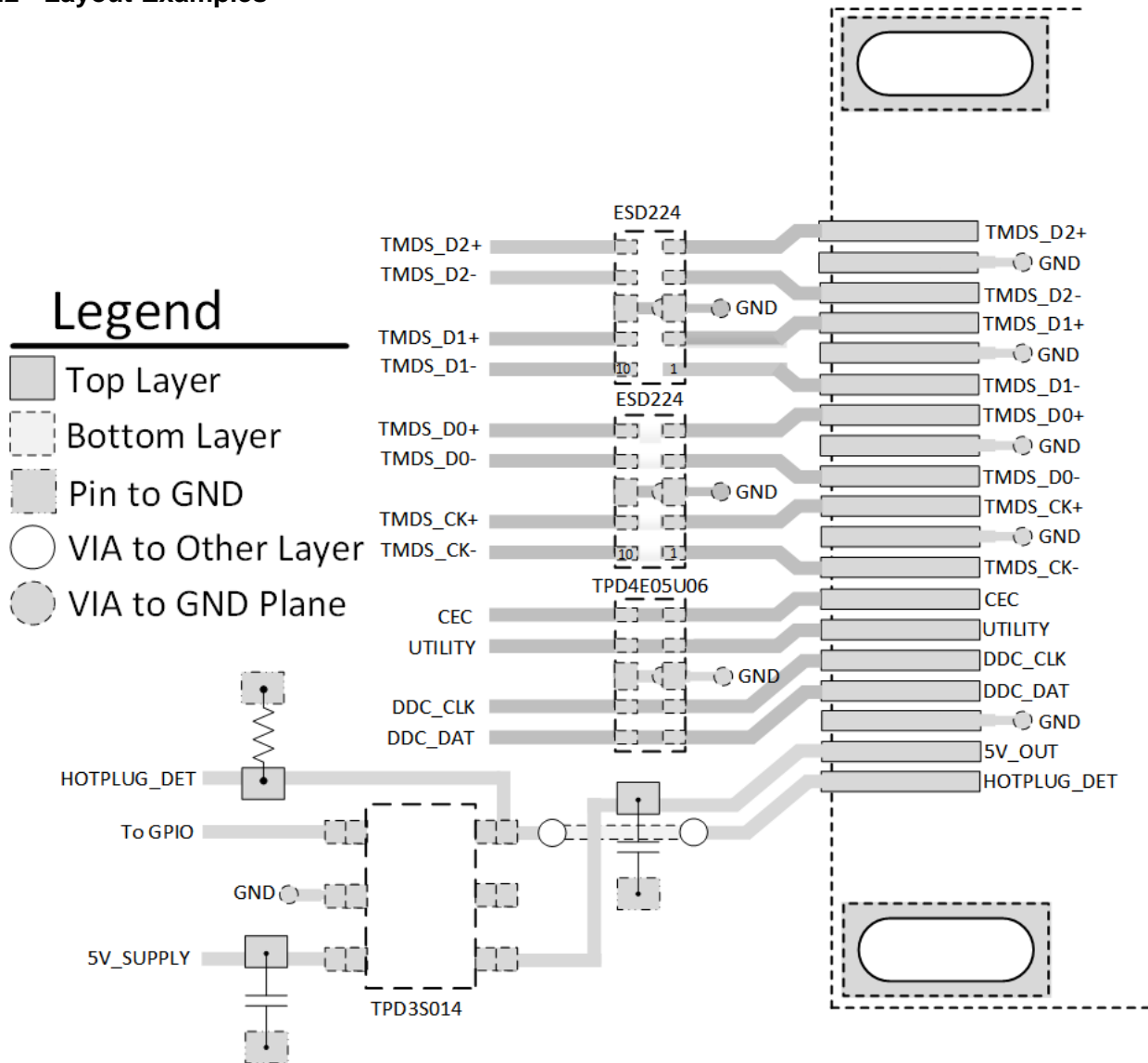


图 15. HDMI Type-A Transmitter Port Layout

注

There is no Through-Routing for the ESD224 Pins Connecting to the High Speed Data Lines.

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的 *通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.

12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD224DQAR	Active	Production	USON (DQA) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1AR
ESD224DQAR.B	Active	Production	USON (DQA) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1AR

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD224DQAR	USON	DQA	10	3000	180.0	8.4	1.2	2.7	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD224DQAR	USON	DQA	10	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

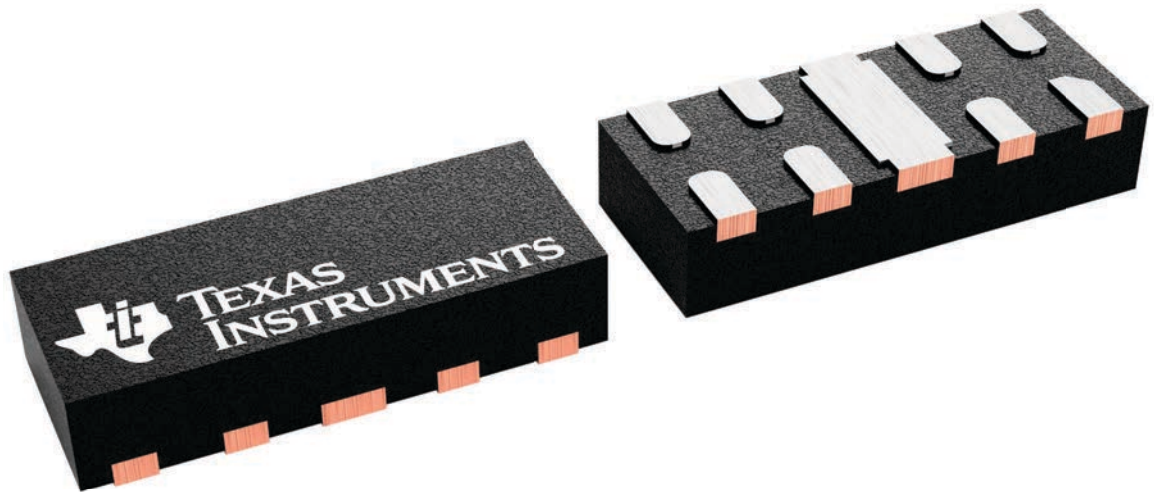
DQA 10

USON - 0.55 mm max height

1 x 2.5, 0.5 mm pitch

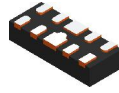
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230320/A

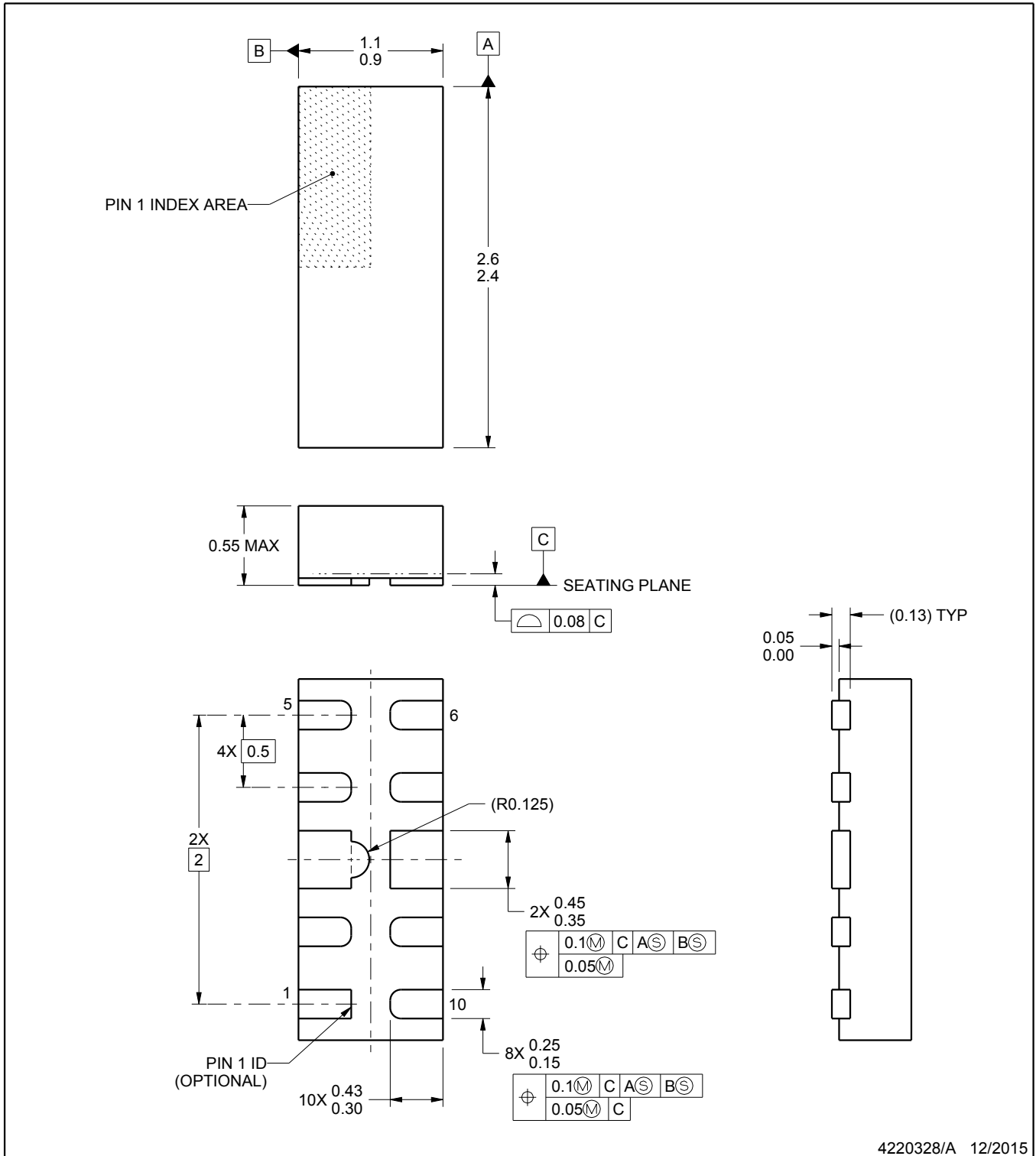
DQA0010A



PACKAGE OUTLINE

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220328/A 12/2015

NOTES:

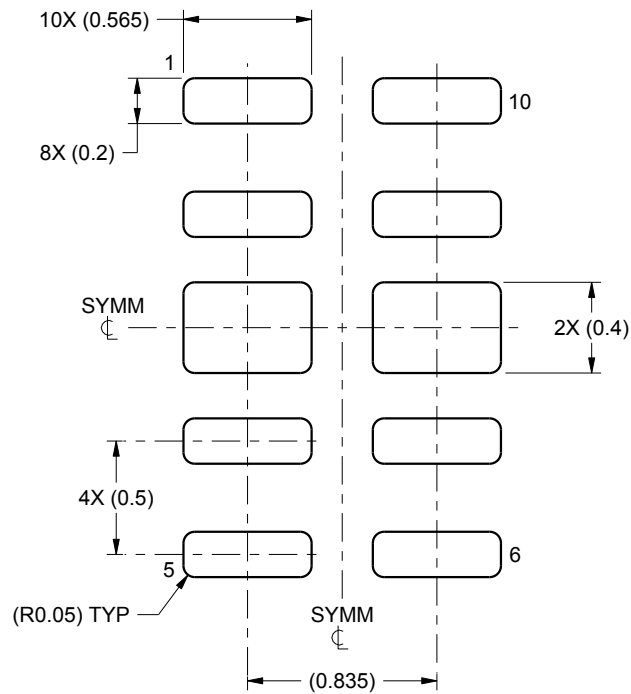
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

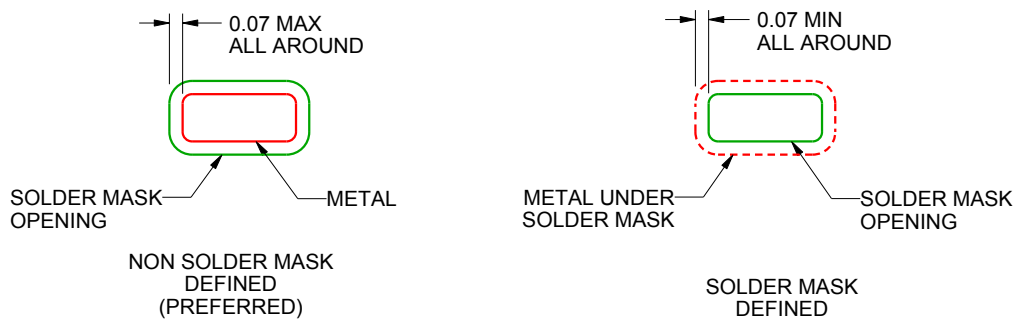
DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

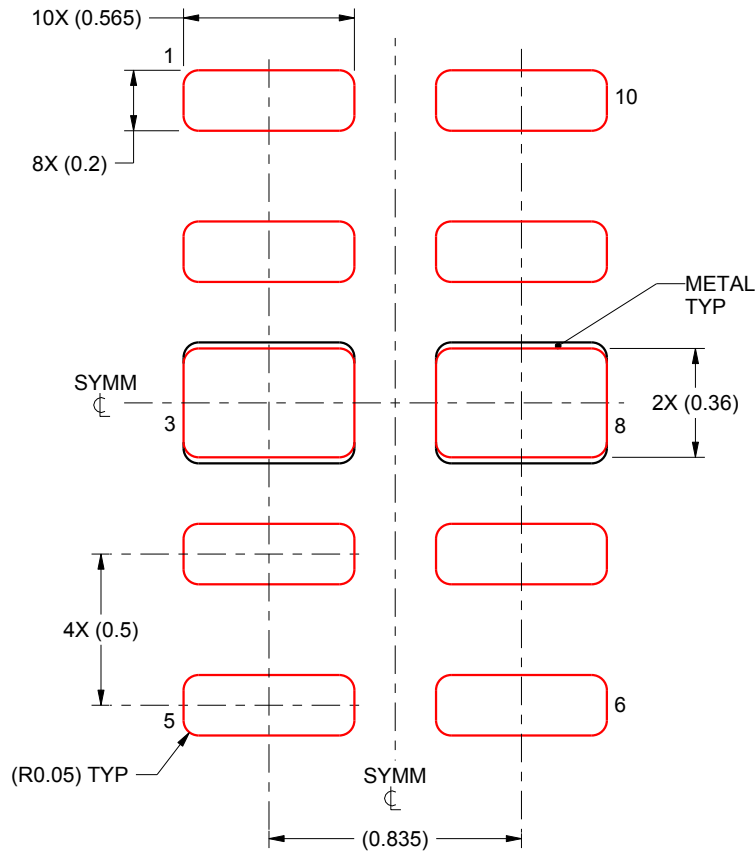
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220328/A 12/2015

NOTES: (continued)

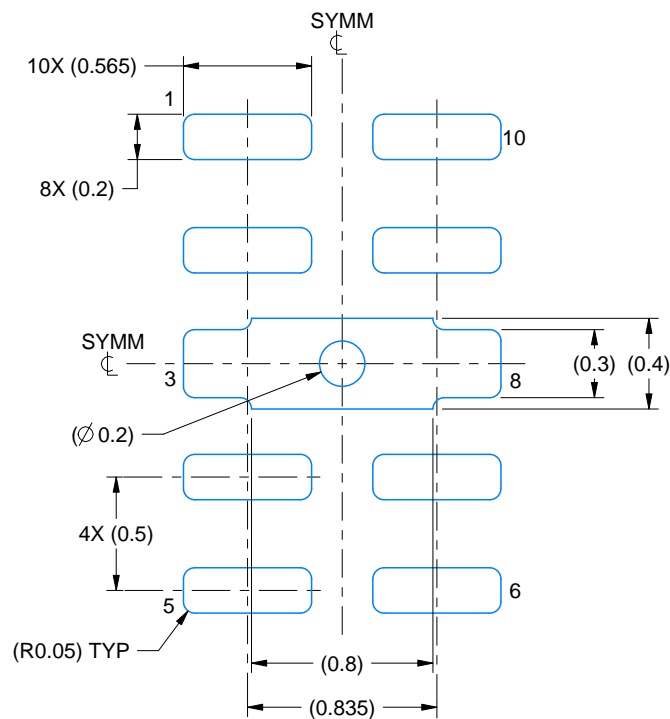
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

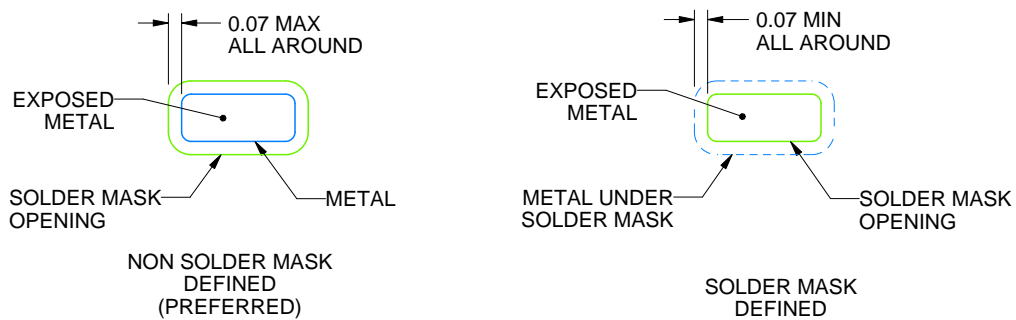
DQA0010B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

4230307/B 03/2026

NOTES: (continued)

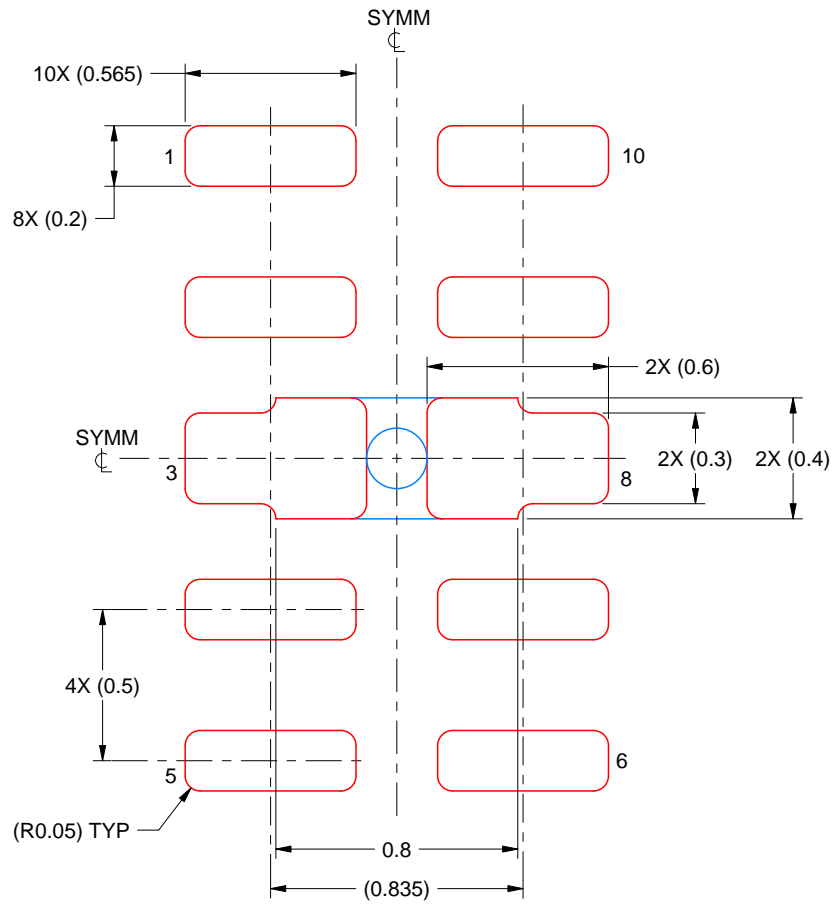
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4230307/B 03/2026

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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