

## ESD204 4 通道低电容浪涌和 ESD 保护二极管

### 1 特性

- IEC 61000-4-2 4 级静电放电 (ESD) 保护
  - $\pm 30\text{kV}$  接触放电
  - $\pm 30\text{kV}$  气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
  - 5.5A (8/20 $\mu\text{s}$ )
  - 低浪涌钳位电压  
在 5.5A  $I_{PP}$  下为 8.5V
- IO 电容:
  - 0.55pF (典型值)
- 符合 HDMI 2.0 标准
- 直流击穿电压: 5.5V (最小值)
- 超低泄漏电流: 10nA (最大值)
- 支持速率最高达 6Gbps 的高速接口
- 工业温度范围:  $-40^{\circ}\text{C}$  至  $+125^{\circ}\text{C}$
- 简易直通布线封装

### 2 应用

- 终端设备
  - IP 网络摄像机
  - 数字视频录像机 (DVR) 和网络视频录像机 (NVR)
  - 以太网交换机和路由器
  - 便携式计算机和台式机
  - 机顶盒
  - 电视和监视器
  - 手机和平板电脑
- 接口
  - HDMI 2.0
  - HDMI 1.4
  - USB 3.0
  - 显示端口 1.3
  - PCI Express 3.0 总线接口
  - 以太网 10/100/1000Mbps

### 3 说明

ESD204 是一种双向 TVS ESD 保护二极管阵列, 可为 HDMI 和 USB 提供高达 5.5A (8/20 $\mu\text{s}$ ) 的浪涌保护。ESD204 的额定 ESD 冲击消散值达到了 IEC 61000-4-2 (4 级) 国际标准中规定的最高水平。

ESD204 提供低钳位和高差分带宽, 使器件可干净地传输高速信号, 并且为下游器件提供强大的保护。该器件每通道具有 0.55pF 的低电容值, 这使其非常适合用于保护速率高达 6Gbps 的高速接口 (例如 HDMI 2.0、HDMI 1.4、USB 3.0 和以太网 1G)。低动态电阻和低钳位电压确保系统级抗瞬变事件保护。

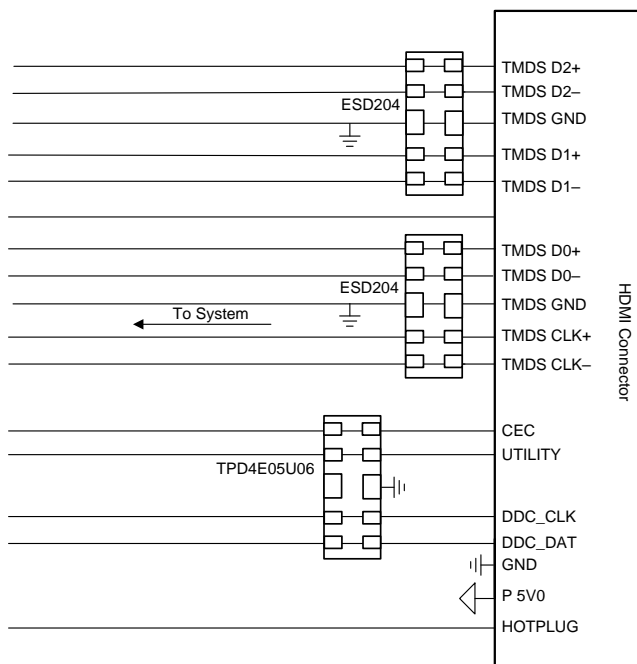
ESD204 采用符合行业标准的 USON-10 (DQA) 封装。该封装采用直通布线, 其引脚间距为 0.5mm, 能够简化实现并缩短设计时间。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
ESD204	USON (10)	2.50mm x 1.00mm

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

#### 典型应用原理图



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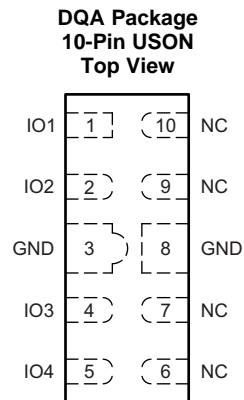
## 4 修订历史记录

### Changes from Original (February 2018) to Revision A

Page

<ul style="list-style-type: none"> <li>• 已更改 将“高级信息”更改为“生产数据” ..... 1</li> </ul>	1
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## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	3	Ground	Ground. Connect to ground
GND	8		
IO1	1	I/O	ESD protected channel. Connect to the line being protected.
IO2	2		
IO3	4		
IO4	5		
NC	6	NC	Not connected internally; Can be connected to line being protected for optional flow-through routing. Can also be left floating or grounded
NC	7		
NC	9		
NC	10		

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Electrical Fast Transient	IEC 61000-4-4 Peak Current at 25°C		80	A
Peak Pulse	IEC 61000-4-5 Surge ( $t_p$ 8/20 $\mu$ s) Peak Power at 25°C		50	W
	IEC 61000-4-5 Surge ( $t_p$ 8/20 $\mu$ s) Peak Current at 25°C		5.5	A
$T_A$	Operating free-air temperature	-40	125	°C
$T_{stg}$	Storage temperature	-65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings -JEDEC Specifications

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings - IEC Specifications

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000
		IEC 61000-4-2 Air Discharge, all pins	±30000

### 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	-3.6		3.6	V
$T_A$	Operating Free Air Temperature	-40		125	°C

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ESD204	UNIT
		DQA (USON)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	184.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	138.2	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	41.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	137.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RWM}$	Reverse stand-off voltage	$I_{IO} < 10 \text{ nA}$ , across operating temperature range	-3.6		3.6	V
$V_{BRF}$	Positive Breakdown Voltage, Each IO Pin to GND <sup>(1)</sup>	$I_{IO} = 1 \text{ mA}$	5		7.9	V
$V_{BRR}$	Negative Breakdown Voltage, Each IO Pin to GND <sup>(1)</sup>	$I_{IO} = -1 \text{ mA}$ ,	-7.9		-5	V
$V_{HOLD}$	Positive Holding Voltage, Each IO pin to GND <sup>(2)</sup>	$I_{IO} = 1 \text{ mA}$		6.2		V
$V_{HOLD-NEG}$	Negative Holding Voltage, Each IO pin to GND <sup>(2)</sup>	$I_{IO} = -1 \text{ mA}$		-6.2		V
$V_{CLAMP}$	Clamping voltage	Surge $I_{PP} = 5.5 \text{ A}$ , Each IO pin to GND, GND to Each IO pin, $t_p=8/20 \mu\text{s}$		8.5		V
		TLP $I_{PP} = 5 \text{ A}$ , Each IO pin to GND, GND to Each IO pin, $t_p=10/100 \text{ ns}$		8.2		V
		TLP $I_{PP} = 16 \text{ A}$ , Each IO pin to GND, GND to Each IO pin, $t_p=10/100 \text{ ns}$		11.5		V
$R_{DYN}$	Dynamic resistance	Each IO Pin to GND, TLP $t_p=10/100 \text{ ns}$		0.3		$\Omega$
		GND to Each IO Pin, TLP $t_p=10/100 \text{ ns}$		0.3		
$C_{LINE}$	Line capacitance, any IO to GND	$V_{IO} = 0 \text{ V}$ , $V_{p-p} = 30 \text{ mV}$ , $f = 1 \text{ MHz}$		0.55	0.65	pF
$\Delta C_{LINE}$	Variation of line capacitance	$C_{LINE1} - C_{LINE2}$ , $V_{IO} = 0 \text{ V}$ , $V_{p-p} = 30 \text{ mV}$ , $f = 1 \text{ MHz}$		0.02	0.07	pF
$C_{CROSS}$	Line-to-line capacitance	$V_{IO} = 0 \text{ V}$ , $V_{rms} = 30 \text{ mV}$ , $f = 1 \text{ MHz}$		0.25	0.35	pF

(1)  $V_{BRF}$  and  $V_{BRR}$  are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state

(2)  $V_{HOLD}$  is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

### 6.7 Typical Characteristics

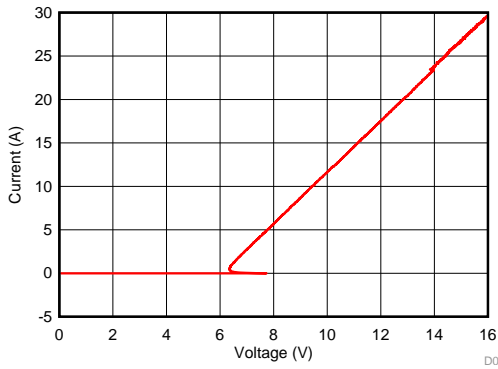


图 1. Positive TLP Curve, IO pin to GND ( $t_p = 100$  ns)

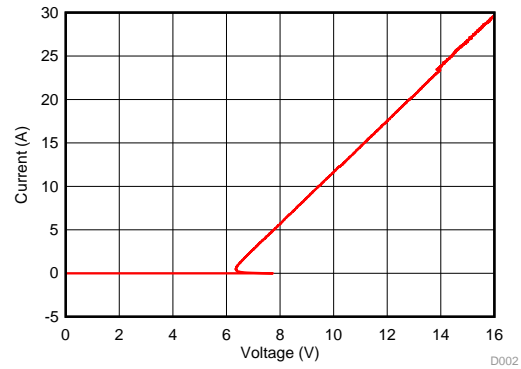


图 2. Negative TLP Curve, GND to IO pin ( $t_p=100$  ns; Plotted as Positive TLP Curve from GND to IO pin)

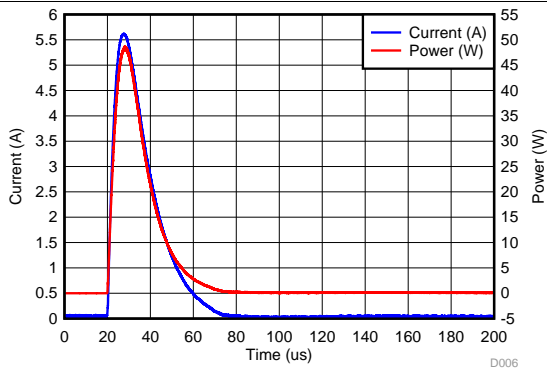


图 3. Surge Curve ( $t_p = 8/20$   $\mu$ s), any IO pin to GND

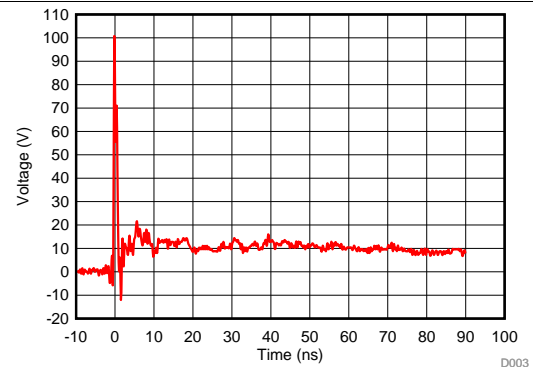


图 4. 8-kV IEC 61000-4-2 Clamping Voltage Waveform, IO pin to GND

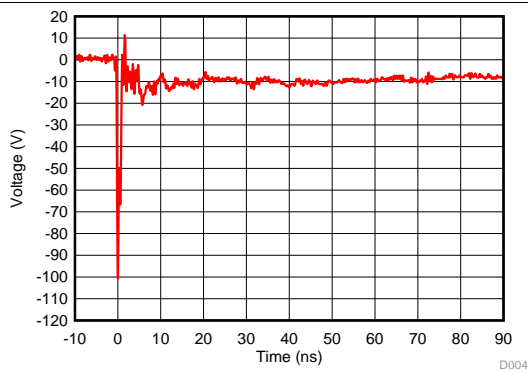


图 5. -8-kV IEC 61000-4-2 Clamping Voltage Waveform, GND pin to IO

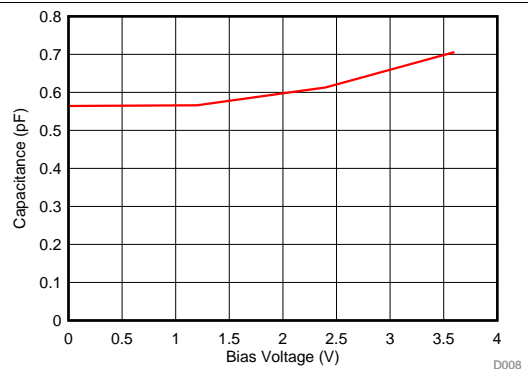


图 6. Capacitance vs Bias Voltage

Typical Characteristics (接下页)

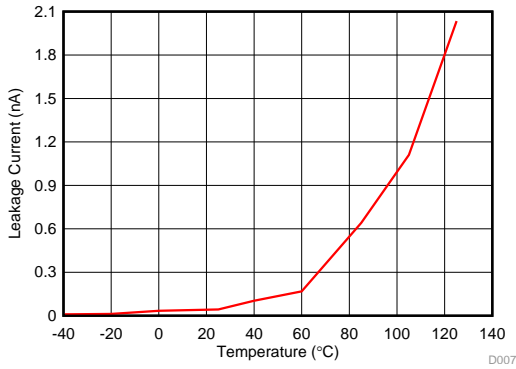


图 7. Leakage Current vs Temperature, IO pin to GND at 3.6 V Bias

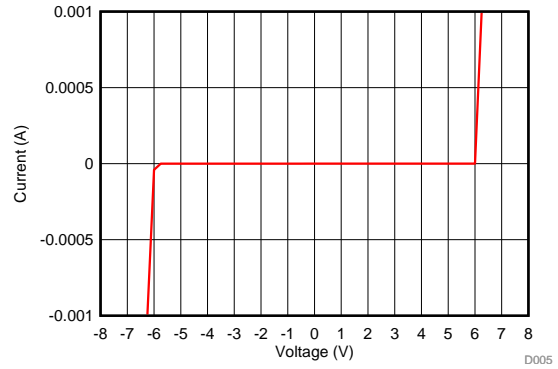


图 8. DC Voltage Sweep I-V Curve, IO pin to GND

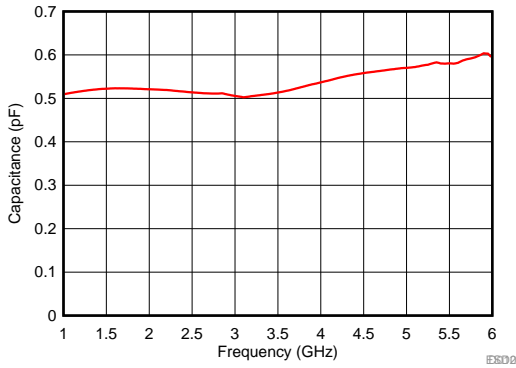


图 9. Capacitance vs Frequency

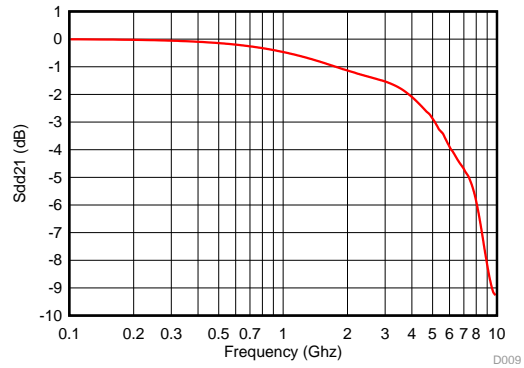


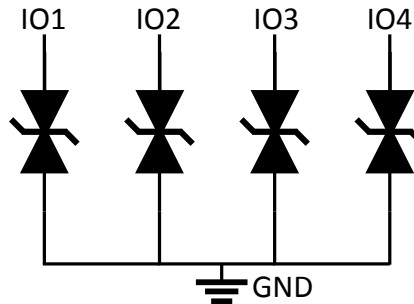
图 10. Differential Insertion Loss

## 7 Detailed Description

### 7.1 Overview

The ESD204 is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes up to 30kV (Contact/Air) level specified by the IEC 61000-4-2 International Standard. Additionally, ESD204 dissipates 5.5 A of surge current (8/20  $\mu$ s waveform) per IEC 61000-4-5 standard. The ultra-low capacitance makes this device capable of supporting any super high-speed signal pins.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

ESD204 provides ESD protection up to  $\pm 30$ -kV contact and  $\pm 30$ -kV air gap per IEC61000-4-2 standard. During an ESD event, ESD diode connected to the IO pin turns on and diverts the ESD current to ground. Additionally, ESD204 also provides protection against IEC 61000-4-5 surge currents up to 5.5 A (8/20  $\mu$ s waveform) and up to 80 A per IEC 61000-4-4 electrical fast transient (EFT) standard. Please see the [Application Note](#) on IEC61000-4-x standard based tests. ESD204 provides a very low clamping voltage of 11.5 V at 16 A 100 ns TLP current and 8.5 V at 5.5 A surge current (8/20  $\mu$ s waveform).

The capacitance between each I/O pin to ground is 0.55 pF (typical) and 0.65 pF (maximum). This device supports data rates up to 6 Gbps. The DC breakdown voltage of each I/O pin is a minimum of  $\pm 5$  V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of  $\pm 3.6$  V. The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of  $\pm 3.6$  V.

### 7.4 Device Functional Modes

The ESD204 is a passive integrated circuit that triggers when voltages are above  $V_{BRF}$  or below  $V_{BRR}$ . During ESD events, voltages as high as  $\pm 30$  kV (contact/air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD204 (usually within 10s of nano-seconds) the device reverts to passive.

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The ESD204 is a diode type TVS array which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between an interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage,  $V_{CLAMP}$ , to a safe level for the protected IC.

## 8.2 Typical Application

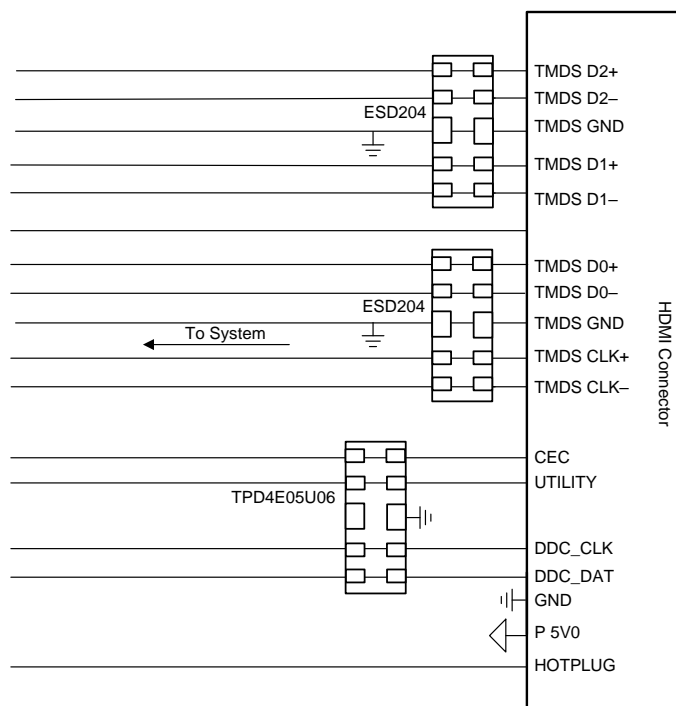


图 11. ESD204 Protecting the HDMI Interface

### 8.2.1 Design Requirements

In this design example, two ESD204 devices and one TPD4E05U06 device are used to protect an HDMI 2.0 interface. For HDMI 2.0 application design parameters listed in 表 1 are known.

表 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on high speed differential data lines	0 to 3.6 V
Operating frequency of high speed data lines	3 GHz (First Harmonic)
Signal range on control lines (CEC, UTILITY, DDC_CLK and DDC_DAT)	0 to 5 V

### 8.2.2 Detailed Design Procedure

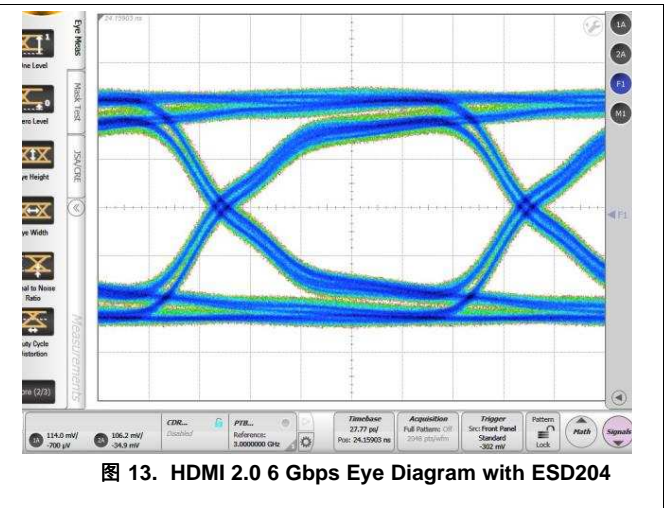
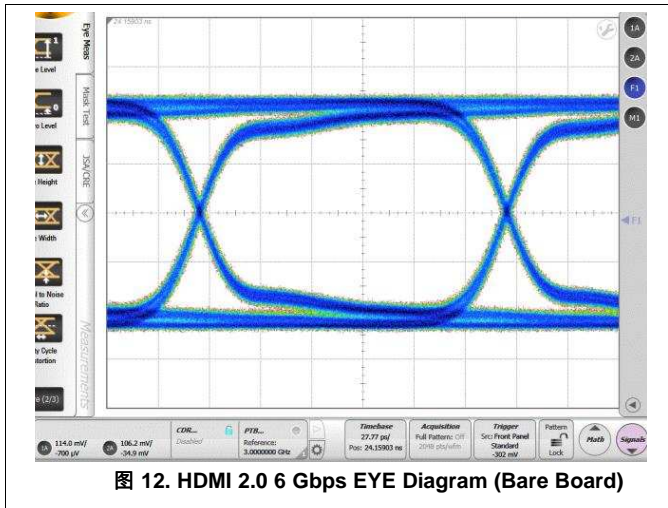
#### 8.2.2.1 Signal Range

ESD204 supports signal ranges between  $-3.6\text{ V}$  and  $3.6\text{ V}$ , which supports the high-speed lines on the HDMI 2.0 application. The TPD4E05U06 supports signal ranges between  $0\text{ V}$  and  $5.5\text{ V}$ , which supports the HDMI control lines.

#### 8.2.2.2 Operating Frequency

The ESD204 has a  $0.55\text{ pF}$  (typical) capacitance, which supports the HDMI 2.0 rate of  $6\text{ Gbps}$ . The TPD4E05U06 has a typical capacitance of  $0.5\text{ pF}$ , which easily support the control lines. The ESD204 has 4 identical protection channels for the differential HDMI high-speed signal lines. The symmetrical pin out of the device with a ground pin between the two differential signal pins makes it suitable for this application.

### 8.2.3 Application Curves



## 9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.






## 10 Layout

### 10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

## 10.2 Layout Examples

### Legend

-  Top Layer
-  Bottom Layer
-  Pin to GND
-  VIA to Other Layer
-  VIA to GND Plane

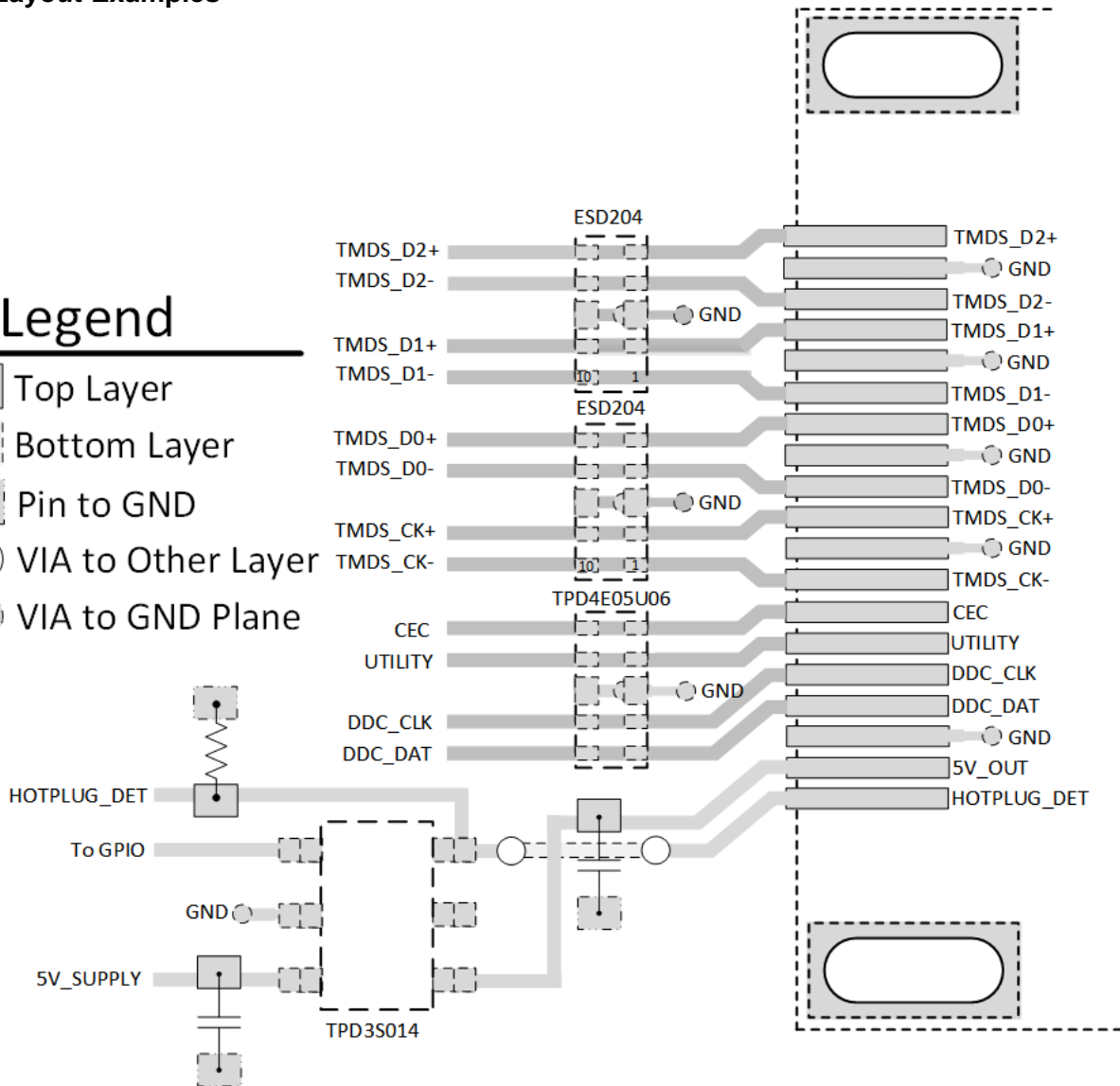


图 14. HDMI Type-A Transmitter Port Layout

## 11 器件和文档支持

### 11.1 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ 在线社区** [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 11.3 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.5 术语表

[SLYZ022](#) — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">ESD204DQAR</a>	Active	Production	USON (DQA)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CE5, CEG) CEY
ESD204DQAR.B	Active	Production	USON (DQA)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CE5, CEG) CEY
ESD204DQARG4	Active	Production	USON (DQA)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CE5
ESD204DQARG4.B	Active	Production	USON (DQA)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CE5

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD204DQAR	USON	DQA	10	3000	180.0	8.4	1.2	2.7	0.63	4.0	8.0	Q1
ESD204DQARG4	USON	DQA	10	3000	180.0	8.4	1.2	2.7	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD204DQAR	USON	DQA	10	3000	210.0	185.0	35.0
ESD204DQARG4	USON	DQA	10	3000	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

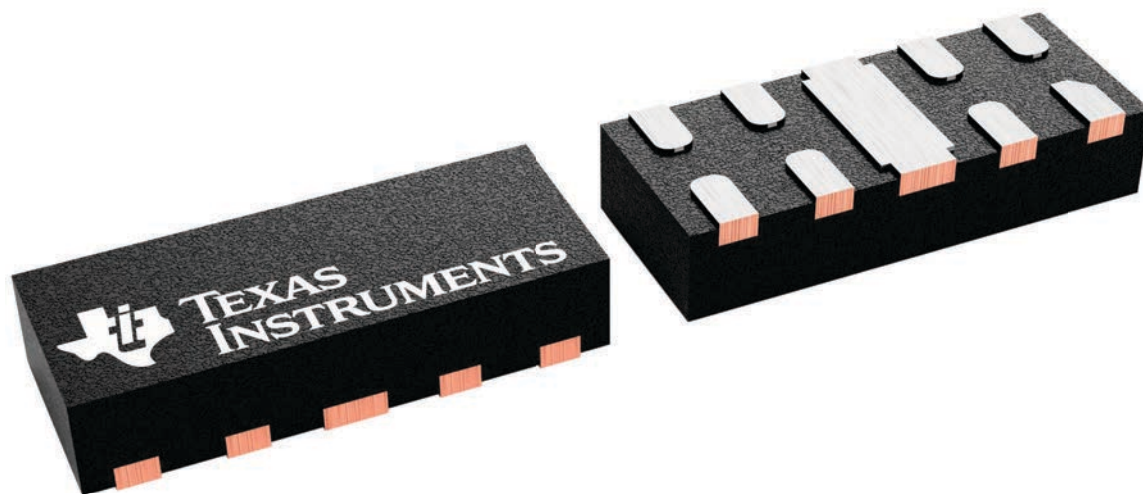
**DQA 10**

**USON - 0.55 mm max height**

1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4230320/A

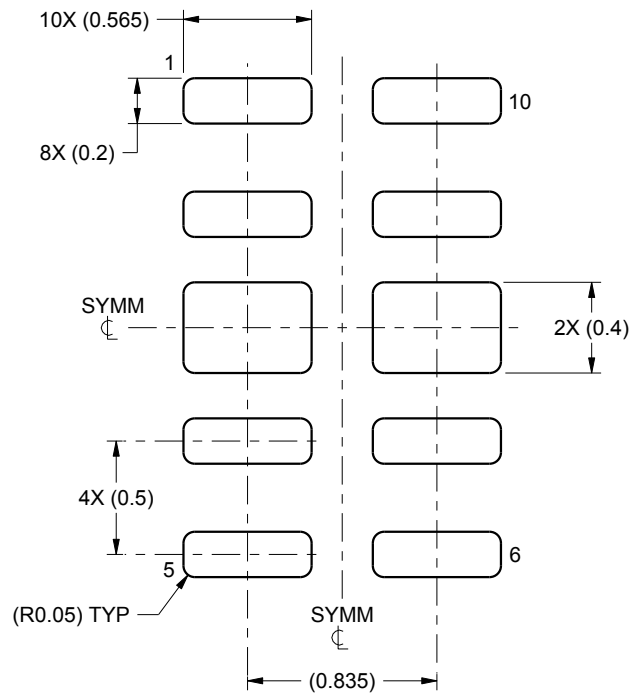


# EXAMPLE BOARD LAYOUT

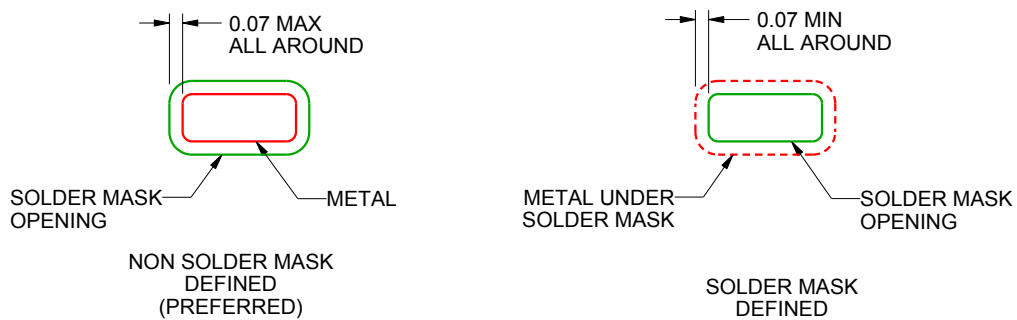
DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

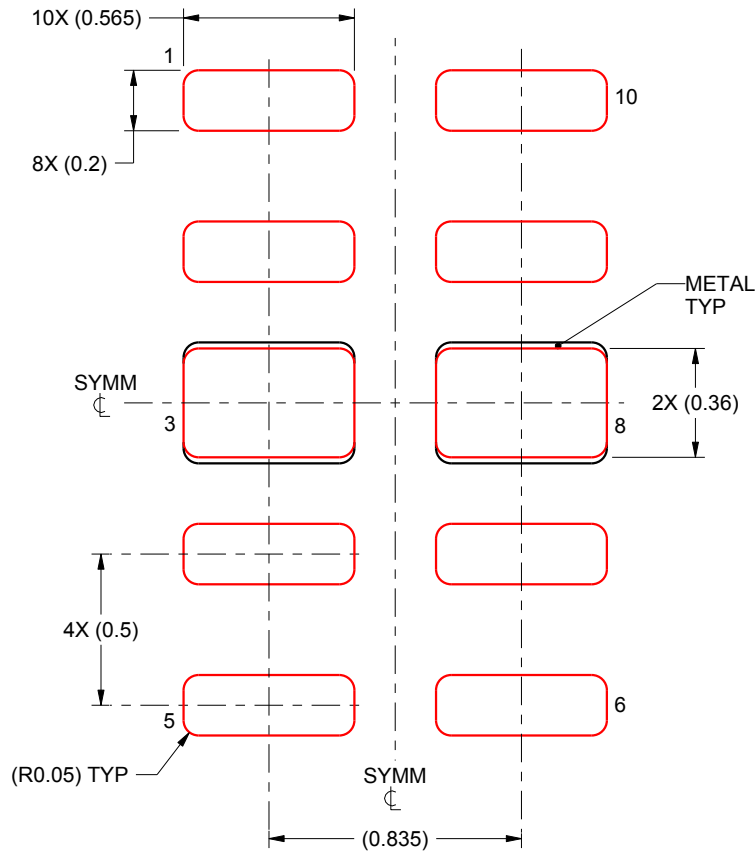
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:  
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

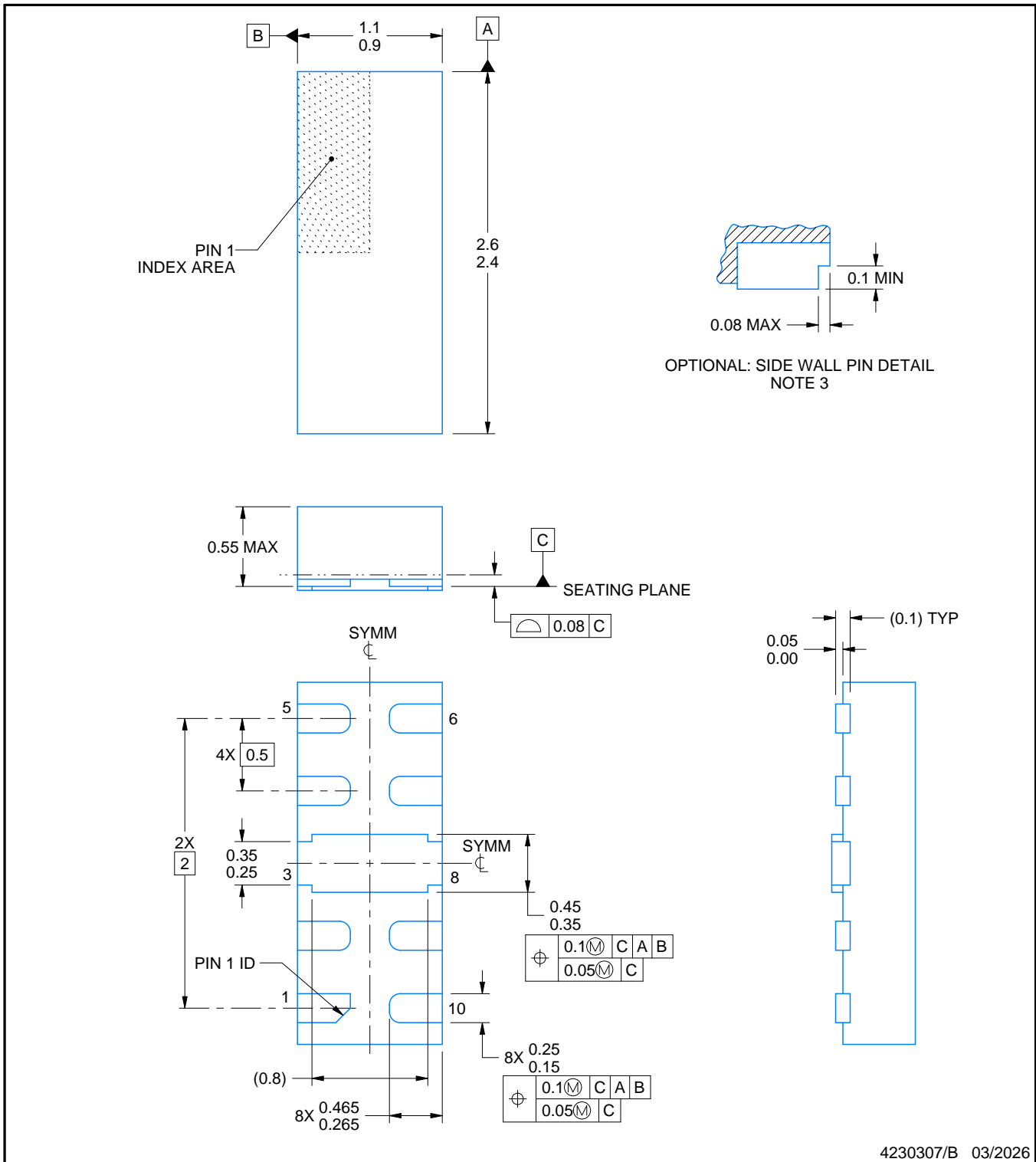
# DQA0010B



# PACKAGE OUTLINE

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4230307/B 03/2026

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.

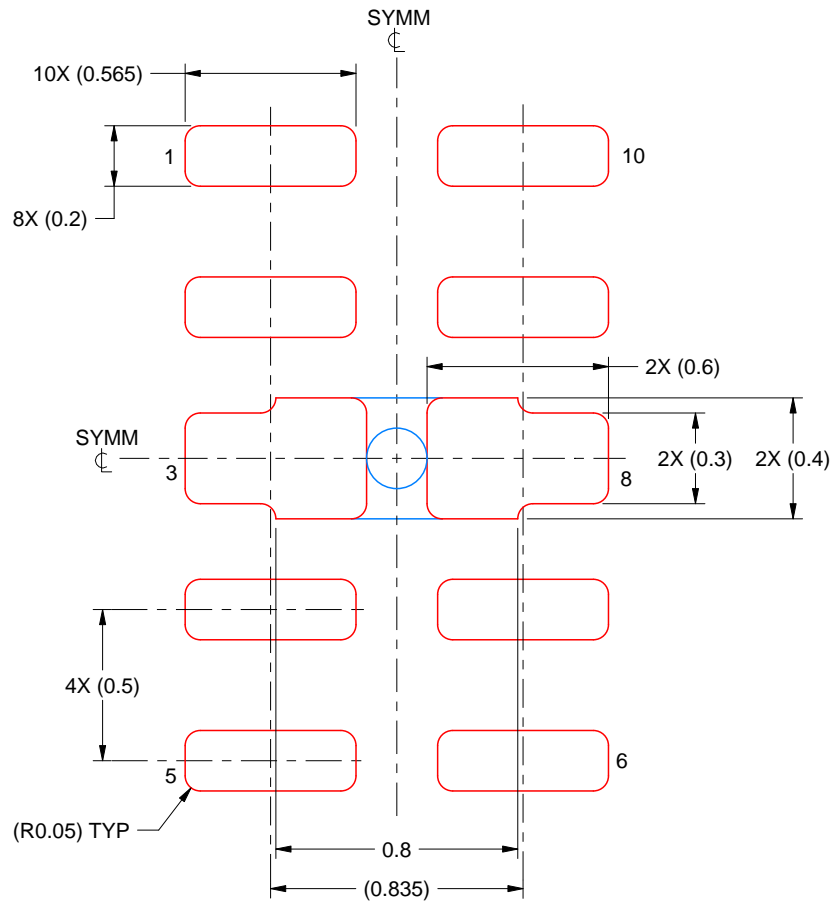


# EXAMPLE STENCIL DESIGN

DQA0010B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4230307/B 03/2026

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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