DS90UB91xQ-Q1 具有双向控制通道的 10MHz 至 100MHz、10 位和 12 位直流均衡 FPD-Link III 串行器和解串器

1 特性

- 10MHz 至 100MHz 输入像素时钟支持
- 单个差分对互连
- 可编程的数据有效载荷：
  - 10 位有效载荷，高达 100MHz
  - 12 位有效载荷，高达 75MHz
- 连续低延迟双向控制接口通道，支持 I^2C，频率达 400kHz
- 2:1 多路复用器，可在两个输入成像器之间进行选择
- 具有直流均衡编码的嵌入式时钟，支持交流耦合互连
- 能够驱动长达 25 米的屏蔽双绞线
- 接收均衡器自动适应电缆损耗的变化
- 串行器和解串器上均提供有 4 个专用通用输入/输出引脚 (GPIO)
- LOCK 输出报告引脚和 AT-SPEED BIST（全速内置自检）诊断特性，可验证链路完整性
- 串行器上提供 1.8V、2.8V 或 3.3V 兼容并行输入
- 1.8V 单电源
- 符合 ISO 10605 和 IEC 61000-4-2 静电放电 (ESD) 标准
- 汽车级产品：符合 AEC-Q100 2 级要求
- 温度范围：-40°C 至 +105°C
- 小尺寸串行器 (5mm × 5mm)
- 解串器上提供 EMI/EMC 缓解功能
  - 可编程扩频 (SSCG) 输出
  - 接收器交错输出

2 应用

- 前置摄像头或后置摄像头，实现碰撞缓解
- 停车辅助系统环视

3 说明

DS90UB91xQ-Q1 芯片组提供一个具有高速正向通道和双向控制通道的 FPD-Link III 接口，用来实现单一差分对上的数据传输。 DS90UB91xQ-Q1 芯片组的高速正向通道和双向控制通道数据路径上均包含差分信令。串行器和解串器对主要用于电子控制单元 (ECU) 中成像器与视频处理器的连接。 该芯片组非常适用于驱动需要高达 12 位像素深度、2 个同步信号以及双向控制通道总线的视频数据。

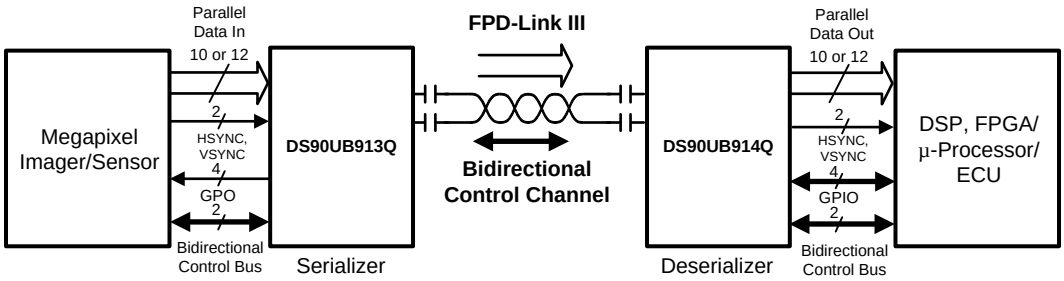
解串器上有一个多路复用器，可用于在两个输入成像器之间进行选择。 解串器只能激活一个输入成像器。 主视频传输将 10 位和 12 位数据转换为单条高速串行数据流，另外一个独立的低延迟双向控制通道传输负责接收来自 I^2C 端口的控制信息，与视频消隐期无关。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DS90UB913Q-Q1	WQFN (32)	5.00mm x 5.00mm
DS90UB914Q-Q1	WQFN (48)	7.00mm x 7.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2014) to Revision D — **Page**

- 已添加*引脚配置和功能*部分，*ESD 额定值表*，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 已更新数据表以符合新的 TI 布局 ... 1
- Added text and graphic to Power Up Requirements ... 39

Changes from Revision B (April 2013) to Revision C — **Page**

- Changed "PCLK from imager mode" value in DS90UB913Q Serializer MODE Resistor Value table from 0 kΩ to 100 kΩ ... 35
- Changed Falling to Rising in RRFB ... 47
- Changed Rising to Falling in RRFB ... 47

Changes from Revision A (April 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 61

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5 说明（续）

凭借德州仪器 (TI) 的嵌入式时钟技术，可在单一差分对上进行透明的全双工通信，两个方向上运载不对称的双向控制通道信息。 这种单一串行数据流通过消除并行数据与时钟路径间的偏差，简化了印刷电路板 (PCB) 走线和电缆上的宽数据总线传输。 这样，通过限制路径的宽度，大大节省了系统成本，相应地减少了 PCB 层数、电缆宽度以及连接器尺寸和引脚数量。 此外，解串器输入还提供自适应均衡功能来补偿较长距离介质上的损耗。 内部直流均衡编码和解码被用来支持交流耦合互连。 此串化器采用 32 引脚超薄型四方扁平无引线 (WQFN) 封装，而解串器采用 48 引脚 WQFN 封装。

6 器件比较表

器件编号	**FPD-III** 功能	封装	传输介质	**PCLK** 频率
DS90UB913Q-Q1	串行器	32 引脚 RTV (WQFN)	STP	10MHz 至 100MHz
DS90UB913A-Q1	串行器	32 引脚 RTV (WQFN)	同轴或屏蔽双绞线 (STP)	25MHz 至 100MHz
DS90UB914Q-Q1	解串器	48 引脚 RHS (WQFN)	STP	10MHz 至 100MHz
DS90UB914A-Q1	解串器	48 引脚 RHS (WQFN)	同轴或 STP	25MHz 至 100MHz

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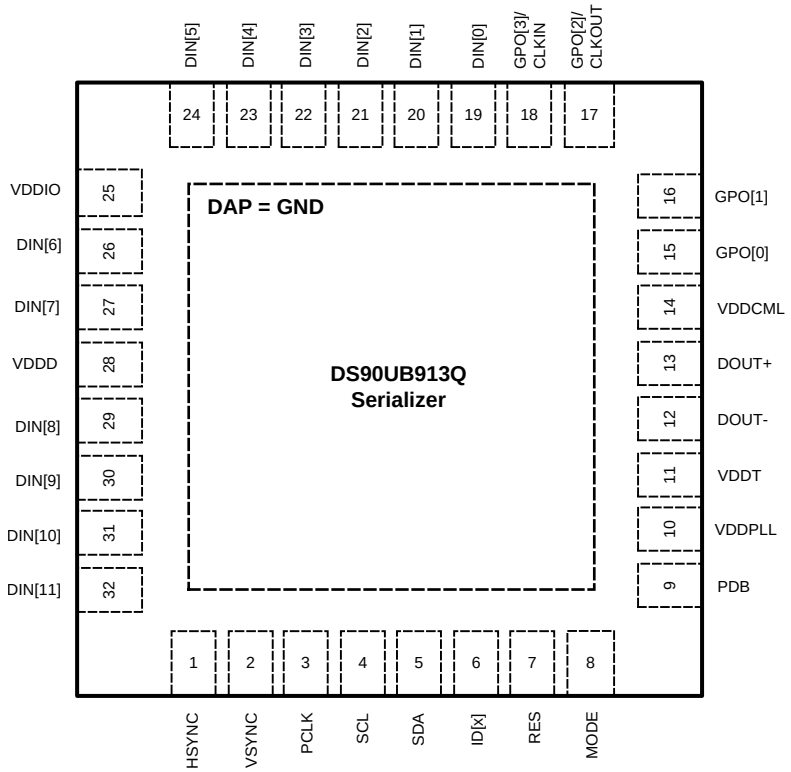
7 Pin Configuration and Functions

RTV Package
32-Pin WQFN
Top View



DS90UB913Q-Q1 Serializer Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
LVCMOS PARALLEL INTERFACE			
DIN[0:11]	19, 20, 21, 22, 23, 24, 26, 27, 29, 30, 31, 32	Inputs, LVCMOS with pulldown	Parallel data inputs
HSYNC	1	Inputs, LVCMOS with pulldown	Horizontal SYNC input
PCLK	3	Input, LVCMOS with pulldown	Pixel clock input pin Strobe edge set by TRFB control register.
VSYNC	2	Inputs, LVCMOS with pulldown	Vertical SYNC input

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DS90UB913Q-Q1 Serializer Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GENERAL-PURPOSE OUTPUT (GPO)			
GPO[1:0]	16, 15	Output, LVCMOS	General-purpose output pins can be configured as outputs; used to control and respond to various commands. GPO[0:1] can be configured to be the outputs for input signals coming from GPIO[0:1] pins on the deserializer or can be configured to be outputs of the local register on the serializer.
GPO[2]/ CLKOUT	17	Output, LVCMOS	GPO2 pin can be configured to be the output for input signal coming from the GPIO2 pin on the deserializer or can be configured to be the output of the local register on the serializer. It can also be configured to be the output clock pin when the DS90UB913Q-Q1 device is used in the External Oscillator mode. See *Applications Information* for a detailed description of the DS90UB91xQ-Q1 chipsets working with the external oscillator.
GPO[3]/ CLKIN	18	Input/Output, LVCMOS	GPO3 can be configured to be the output for input signals coming from the GPIO3 pin on the deserializer or can be configured to be the output of the local register setting on the serializer. It can also be configured to be the input clock pin when the DS90UB913Q-Q1 serializer is working with an external oscillator. See *Applications Information* section for a detailed description of the DS90UB91xQ-Q1 chipsets working with an external oscillator.
BIDIRECTIONAL CONTROL BUS - I^2C COMPATIBLE			
SCL	4	Input/Output, Open-Drain	Clock line for the bidirectional control bus communication SCL requires an external pullup resistor to V_{DDIO}.
SDA	5	Input/Output, Open-Drain	Data line for the bidirectional control bus communication SDA requires an external pullup resistor to V_{DDIO}.
MODE	8	Input, LVCMOS with pulldown	**Device mode select** Resistor to Ground and 10-kΩ pullup to 1.8-V rail. MODE pin on the serializer can be used to select whether the system is running off the PCLK from the imager or an external oscillator. See details in Table 3.
ID[x]	6	Input, analog	**Device ID address select** The ID[x] pin on the serializer is used to assign the I^2C device address. Resistor to Ground and 10-kΩ pullup to 1.8-V rail. See Table 1.
CONTROL AND CONFIGURATION			
PDB	9	Input, LVCMOS with pulldown	**Power down Mode Input Pin** PDB = H, serializer is enabled and is ON. PDB = L, Serailizer is in power-down mode. When the serializer is in power-down, the PLL is shutdown, and IDD is minimized. Programmed control register data are NOT retained and reset to default values
RES	7	Input, LVCMOS with pulldown	Reserved **This pin MUST be tied LOW.**
FPD-Link III INTERFACE			
DOUT+	13	Input/Output, CML	Noninverting differential output, bidirectional control channel input. The interconnect must be AC-coupled with a 100-nF capacitor.
DOUT–	12	Input/Output, CML	Inverting differential output, bidirectional control channel input. The interconnect must be AC-coupled with a 100-nF capacitor.
POWER AND GROUND			
VDDPLL	10	Power, Analog	PLL Power, 1.8 V ±5%
VDDT	11	Power, Analog	Tx Analog Power, 1.8 V ±5%
VDDCML	14	Power, Analog	CML and bidirectional channel driver power, 1.8 V ±5%
VDDD	28	Power, Digital	Digital power, 1.8 V ±5%
VDDIO	25	Power, Digital	Power for I/O stage. The single-ended inputs and SDA, SCL are powered from V_{DDIO}. V_{DDIO} can be connected to a 1.8 V ±5% or 2.8 V ±10% or 3.3 V ±10%
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connected to the ground plane (GND) with at least 9 vias.

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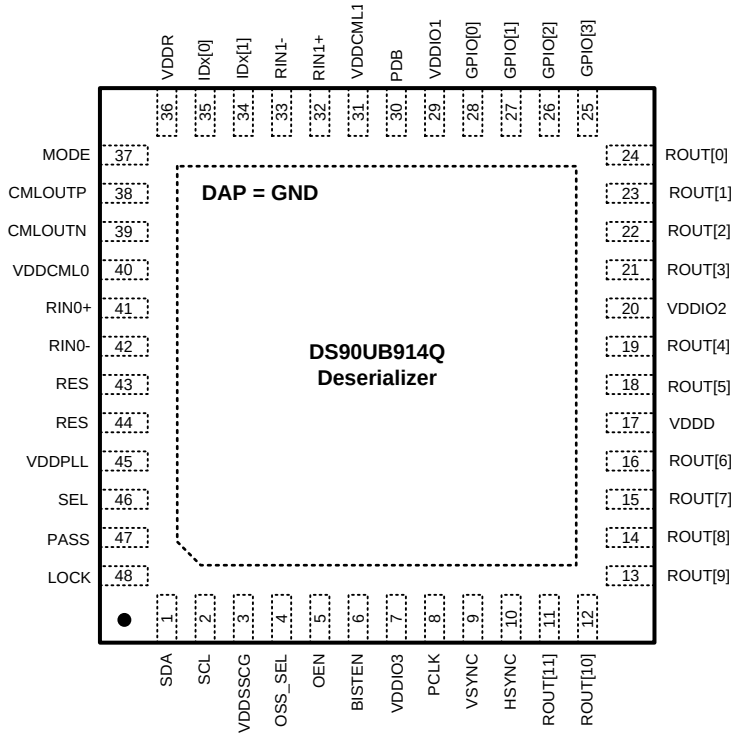
RHS Package
48-Pin WQFN
Top View



DS90UB914Q-Q1 Deserializer Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
LVCMOS PARALLEL INTERFACE			
ROUT[11:0]	11, 12, 13, 14, 15, 16, 18, 19, 21, 22, 23, 24	Outputs, LVCMOS	Parallel data outputs
HSYNC	10	Output, LVCMOS	Horizontal SYNC output
PCLK	8	Output, LVCMOS	Pixel clock output pin Strobe edge set by RRFB control register
VSYNC	9	Output, LVCMOS	Vertical SYNC output
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)			
GPIO[1:0]	27, 28	Digital Input/Output, LVCMOS	General-purpose input/output pins can be used to control and respond to various commands. They may be configured to be the input signals for the corresponding GPOs on the serializer or they may be configured to be outputs to follow local register settings.
GPIO[3:2]	25, 26	Digital Input/Output LVCMOS	General-purpose input/output pins GPO[2:3] can be configured to be input signals for GPOs on the serializer. In addition they can also be configured to be outputs to follow the local register settings. When the SerDes chipsets are working with an external oscillator, these pins can be configured only to be outputs to follow the local register settings.

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DS90UB914Q-Q1 Deserializer Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
BIDIRECTIONAL CONTROL BUS - I²C COMPATIBLE			
SCL	2	Input/Output, Open-Drain	Clock line for the bidirectional control bus communication SCL requires an external pullup resistor to V_{DDIO}.
SDA	1	Input/Output, Open-Drain	Data line for bidirectional control bus communication SDA requires an external pullup resistor to V_{DDIO}.
MODE	37	Input, LVCMOS with pullup	**Device mode select pin** Resistor-to-Ground and 10-kΩ pullup to 1.8-V rail. The MODE pin on the deserializer can be used to configure the serializer and deserializer to work in different input PCLK range. See details in Table 8. **12-bit low-frequency mode (10- to 50-MHz operation):** In this mode, the serializer and deserializer can accept up to 12 bits DATA+2 SYNC. Input PCLK range is from 10 MHz to 50 MHz. **12-bit high-frequency mode (15- to 75-MHz operation):** In this mode, the serializer and deserializer can accept up to 12 bits DATA + 2 SYNC. Input PCLK range is from 15 MHz to 75 MHz. **10-bit mode (20- to 100-MHz operation):** In this mode, the serializer and deserializer can accept up to 10 bits DATA + 2 SYNC. Input PCLK frequency can range from 20 MHz to 100 MHz. Refer to Table 4 in the *Applications Information* section on how to configure the MODE pin on the deserializer.
IDx[0:1]	35, 34	Input, analog	The IDx[0] and IDx[1] pins on the deserializer are used to assign the I²C device address. Resistor-to-Ground and 10-kΩ pullup to 1.8-V rail. See Table 2 Input pin to select the slave device address. Input is connect to external resistor divider to set programmable Device ID address.
CONTROL AND CONFIGURATION			
PDB	30	Input, LVCMOS with pulldown	**Power-down mode input pin** PDB = H, deserializer is enabled and is ON. PDB = L, deserializer is in sleep (power-down mode). When the deserializer is in sleep, programmed control register data are NOT retained and reset to default values.
LOCK	48	Output, LVCMOS	**LOCK status output pin** LOCK = H, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL control register. May be used as link status.
BISTEN	6	Input LVCMOS with pulldown	**BIST enable pin** **BISTEN=H**, BIST mode enabled **BISTEN=L**, BIST mode is disabled
PASS	47	Output, LVCOMS	**PASS output pin for BIST mode.** **PASS = H**, ERROR FREE transmission **PASS = L**, one or more errors were detected in the received payload. See Built-In Self Test section for more information. Leave open if unused. Route to test point (pad) recommended.
OEN	5	Input LVCMOS with pulldown	Output enable input Refer to Table 5
OSS_SEL	4	Input LVCMOS with pulldown	Output sleep state select pin Refer to Table 5
SEL	46	Input LVCMOS with pulldown	MUX select line **SEL = L**, RIN0± input. This selects input A as the active channel on the deserializer. **SEL = H**, RIN1± input. This selects input B as the active channel on the deserializer.

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DS90UB914Q-Q1 Deserializer Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
FPD-LINK III INTERFACE			
RIN0+	41	Input/Output, CML	Noninverting differential input, bidirectional control channel. The IO must be AC coupled with a 100-nF capacitor
RIN0-	42	Input/Output, CML	Inverting differential input, bidirectional control channel. The IO must be AC coupled with a 100-nF capacitor
RIN1+	32	Input/Output, CML	Noninverting differential input, bidirectional control channel. The IO must be AC coupled with a 100-nF capacitor
RIN1-	33	Input/Output, CML	Inverting differential input, bidirectional control channel. The IO must be AC coupled with a 100-nF capacitor
RES	43, 44	—	Reserved; **This pin must always be tied low**.
CMLOUTP/N	38, 39	—	Route to test point or leave open if unused
POWER AND GROUND			
VDDIO1/2/3	29, 20, 7	Power, Digital	LVCMOS I/O buffer power, The single-ended outputs and control input are powered from V_{DDIO}. V_{DDIO} can be connected to a 1.8 V ±5% or 3.3 V ±10%
VDDD	17	Power, Digital	Digital core power, 1.8 V ±5%
VDDSSCG	3	Power, Analog	SSCG PLL power, 1.8 V ±5%
VDDR	36	Power, Analog	RX analog power, 1.8 V ±5%
VDDCML0/1	40, 31	Power, Analog	CML and bidirectional control channel drive power, 1.8 V±5%
VDDPLL	45	Power, Analog	PLL Power, 1.8 V ±5%
VSS	DAP	Ground, DAP	DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connected to the ground plane (GND) with at least 16 vias.

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

	MIN	MAX	UNIT
Supply voltage – V_{DDn} (1.8 V)	−0.3	2.5	V
Supply voltage – V_{DDIO}	−0.3	4.0	V
LVCMOS input voltage	−0.3	VDDIO + 0.3	V
CML driver I/O voltage (V_{DD})	−0.3	V_{DD} + 0.3	V
CML receiver I/O voltage (V_{DD})	−0.3	V_{DD} + 0.3	V
Junction temperature		150	°C
Maximum package power dissipation capacity package		$1/\theta_{JA}$ above +25°	°C/W
Air discharge (DOUT+, DOUT–, RIN+, RIN–)	−25	25	kV
Contact discharge (DOUT+, DOUT–, RIN+, RIN–)	−7	7	kV
Storage temperature T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) For soldering specifications: see product folder at www.ti.com and SNOA549.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±8000	V
	Charged-device model (CDM), per AEC Q100-011		±1000	
	Machine model (MM)		±250	
	IEC 61000-4-2 (2)	Air Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±25 000	
		Contact Discharge (DOUT+, DOUT-, RIN+, RIN-)	≥±7000	
	ISO10605 (3) (4)	Air Discharge	≥±15 000	
		Contact Discharge	≥±8000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) R_D = 330 Ω, C_S = 150 pF
(3) R_D = 330 Ω, C_S = 150 / 330 pF
(4) R_D = 2 KΩ, C_S = 150 / 330 pF

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage (V_{DDn})		1.71	1.8	1.89	V
LVCMOS supply voltage (V_{DDIO}) OR		1.71	1.8	1.89	V
LVCMOS supply voltage (V_{DDIO}) OR		3.0	3.3	3.6	
LVCMOS supply voltage (V_{DDIO}) only serializer		2.52	2.8	3.08	
Supply noise (1)	V_{DDn} (1.8 V)			25	mVp-p
	V_{DDIO} (1.8 V)			25	
	V_{DDIO} (3.3 V)			50	
Operating free-air temperature (T_A)		–40	25	105	°C
PCLK clock frequency		10		100	MHz

(1) Supply noise testing was done with minimum capacitors (as shown on Figure 49 and Figure 48) on the PCB. A sinusoidal signal is AC coupled to the VDDn (1.8-V) supply with amplitude = 25 mVp-p measured at the device VDDn pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency on the serializer is less than 1 MHz. The deserializer on the other hand shows no error when the noise frequency is less than 750 kHz.

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8.4 Thermal Information

THERMAL METRIC[1]		DS90UB913Q-Q1 RTV (WQFN) 32 PINS	DS90UB914Q-Q1 RHS (WQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.4	26.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.9	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

over recommended operating supply and temperature ranges unless otherwise specified.[1] [2] [3]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS 3.3V I/O (SERIALIZER INPUTS, DESERIALIZER OUTPUTS, GPI, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High level input voltage	V_{IN} = 3 V to 3.6 V		2		V_{IN}	V
V_{IL}	Low level input voltage	V_{IN} = 3 V to 3.6 V		GND		0.8	V
I_{IN}	Input current	V_{IN} = 0 V or 3.6 V, V_{IN} = 3 V to 3.6 V		−20	±1	20	µA
V_{OH}	High level output voltage	V_{DDIO} = 3 V to 3.6 V, I_{OH} = −4 mA		2.4		V_{DDIO}	V
V_{OL}	Low level output voltage	V_{DDIO} = 3 V to 3.6 V, I_{OL} = +4 mA		GND		0.4	V
I_{OS}	Output short circuit current	V_{OUT} = 0 V	Serializer GPO outputs		–15		mA
			Deserializer LVCMOS outputs		–35		
I_{OZ}	TRI-STATE output current	PDB = 0 V, V_{OUT} = 0 V or V_{DD}	LVCMOS outputs	–20		20	µA
LVCMOS DC SPECIFICATIONS 1.8V I/O (SERIALIZER INPUTS, DESERIALIZER OUTPUTS, GPI, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High level input voltage	V_{IN} = 1.71 V to 1.89 V		0.65 V_{IN}		V_{IN}	V
V_{IL}	Low level input voltage	V_{IN} = 1.71 V to 1.89 V		GND		0.35 V_{IN}	
I_{IN}	Input current	V_{IN} = 0 V or 1.89 V, V_{IN} = 1.71 V to 1.89 V		–20	±1	20	µA
V_{OH}	High level output voltage	V_{DDIO} = 1.71 V to 1.89 V, I_{OH} = −4 mA		V_{DDIO} – 0.45		V_{DDIO}	V
V_{OL}	Low level output voltage	V_{DDIO} = 1.71 V to 1.89 V I_{OL} = 4 mA	Deserializer LVCMOS outputs	GND		0.45	V
I_{OS}	Output short circuit current	V_{OUT} = 0 V	Serializer GPO outputs		–11		mA
			Deserializer LVCMOS outputs		–17		
I_{OZ}	TRI-STATE output current	PDB = 0 V, V_{OUT} = 0 V or V_{DD}	LVCMOS outputs	–20		20	µA

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.
(3) Typical values represent most likely parametric norms at 1.8 V or 3.3 V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not specified.

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Electrical Characteristics (continued)

over recommended operating supply and temperature ranges unless otherwise specified.(1) (2) (3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS 2.8-V I/O (SERIALIZER INPUTS, GPI, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High level input voltage	V_{IN} = 2.52 V to 3.08 V		0.7 V_{IN}		V_{IN}	V
V_{IL}	Low level input voltage	V_{IN} = 2.52 V to 3.08 V		GND		0.3 V_{IN}	V
I_{IN}	Input current	V_{IN} = 0 V or 3.08 V, V_{IN} = 2.52 V to 3.08 V		−20	±1	20	µA
V_{OH}	High level output voltage	V_{DDIO} = 2.52 V to 3.08 V, I_{OH} = −4 mA		V_{DDIO} – 0.4		V_{DDIO}	V
V_{OL}	Low level output voltage	V_{DDIO} =2.52 V to 3.08 V I_{OL} = 4 mA	Deserializer LVCMOS outputs	GND		0.4	V
I_{OS}	Output short circuit current	V_{OUT} = 0 V	Serializer GPO outputs		−11		mA
			Deserializer LVCMOS outputs		−20		mA
I_{OZ}	TRI-STATE output current	PDB = 0 V, V_{OUT} = 0 V or V_{DD}	LVCMOS outputs	−20		20	µA
CML DRIVER DC SPECIFICATIONS (DOUT+, DOUT–)							
$\|V_{OD}\|$	Output differential voltage	R_L = 100 Ω (see Figure 9)		268	340	412	mV
ΔV_{OD}	Output differential voltage unbalance	R_L = 100 Ω			1	50	mV
V_{OS}	Output differential offset voltage	R_L = 100 Ω (see Figure 9)			V_{DD} – $V_{OD/2}$		V
ΔV_{OS}	Offset voltage unbalance	R_L = 100 Ω			1	50	mV
I_{OS}	Output short circuit current	DOUT± = 0 V			–26		mA
R_T	Differential internal termination resistance	Differential across DOUT+ and DOUT–		80	100	120	Ω
CML RECEIVER DC SPECIFICATIONS (RIN0+, RIN0–, RIN1+, RIN1–)							
I_{IN}	Input current	V_{IN} = V_{DD} or 0 V, V_{DD} = 1.89 V		−20	1	20	µA
R_T	Differential internal termination resistance	Differential across RIN+ and RIN-		80	100	120	Ω
CML RECEIVER AC SPECIFICATIONS (RIN0+, RIN0–, RIN1+, RIN1–)							
$\|V_{swing}\|$	Minimum allowable swing for 1010 pattern(4)	Line rate = 1.4 Gbps (see Figure 11)		135			mV
CML MONITOR OUTPUT DRIVER SPECIFICATIONS (CMLOUTP, CMLOUTN)							
E_W	Differential output eye opening	R_L = 100 Ω Jitter frequency > f / 40 (see Figure 20)			0.45		UI
E_H	Differential output eye height	R_L = 100 Ω Jitter frequency > f / 40 (see Figure 20)			200		mV

(4) Specification is ensured by characterization and is not tested in production.

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Electrical Characteristics (continued)

over recommended operating supply and temperature ranges unless otherwise specified.(1) (2) (3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SERIALIZER AND DESERIALIZER SUPPLY CURRENT *DIGITAL, PLL, AND ANALOG VDD							
I_{DDT}	Serializer (TX) V_{DDn} supply current (includes load current)	R_L = 100 Ω WORST CASE pattern (see Figure 6)	VDDn = 1.89 V VDDIO = 3.6 V f = 100 MHz, 10-bit mode default registers		61	80	mA
			VDDn = 1.89 V VDDIO = 3.6 V f = 75 MHz, 12-bit high-frequency mode default registers		61	80	mA
			VDDn = 1.89 V VDDIO = 3.6 V f = 50 MHz, 12-bit low-frequency mode default registers		61	80	
		R_L = 100 Ω RANDOM PRBS-7 pattern	VDDn = 1.89 V VDDIO = 3.6 V f = 100 MHz, 10-bit mode default registers		54		mA
			VDDn = 1.89 V VDDIO = 3.6 V f = 75 MHz, 12-bit high-frequency mode default registers		54		
			VDD = 1.89 V VDDIO = 3.6 V f = 50 MHz, 12-bit low-frequency mode default registers		54		
I_{DDIOT}	Serializer (TX) VDDIO supply current (includes load current)	R_L = 100 Ω WORST CASE pattern (see Figure 6)	VDDIO = 1.89 V f = 75 MHz, 12-bit high-freq mode default registers		1.5	3	mA
			VDDIO = 3.6 V f = 75 MHz, 12-bit high-frequency mode default registers		5	8	
I_{DDTZ}	Serializer (TX) supply current power-down	PDB = 0 V; all other LVCMOS inputs = 0 V	VDDIO = 1.89 V Default registers		300	900	µA
			VDDIO = 3.6 V Default registers		300	900	µA
I_{DDIOTZ}	Serializer (TX) VDDIO supply current power-down	PDB = 0 V; All other LVCMOS Inputs = 0 V	VDDIO = 1.89 V Default registers		15	100	µA
			VDDIO = 3.6 V Default registers		15	100	µA

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Electrical Characteristics (continued)

over recommended operating supply and temperature ranges unless otherwise specified.(1) (2) (3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DDIOR}	Deserializer (RX) total supply current (includes load current)	V_{DDIO} = 1.89 V C_L = 8 pF WORST CASE pattern	f = 100 MHz, 10-bit mode		22	42	mA
			f = 75 MHz, 12-bit high-freq mode		19	39	
			f = 50 MHz, 12-bit low-freq mode		21	32	
		V_{DDIO} = 1.89 V C_L=8pF Random pattern	f = 100 MHz, 10–bit mode		15		mA
			f = 75 MHz, 12-bit high-freq mode		12		
			f = 50 MHz, 12-bit low-freq mode		14		
		V_{DDIO} = 3.6 V C_L = 8 pF WORST CASE pattern	f = 100 MHz, 10-bit mode		42	55	mA
			f = 75 MHz, 12-bit high-freq mode		37	50	
			f = 50 MHz, 12-bit low-freq mode		25	38	
		V_{DDIO} = 3.6 V C_L = 8 pF Random pattern	f = 100 MHz, 10-bit mode		35		mA
			f = 75 MHz, 12-bit high-freq mode		30		
			f = 50 MHz, 12-bit low-freq mode		18		
		V_{DDIO} = 1.89 V C_L = 4 pF WORST CASE pattern	f = 100 MHz, 10-bit mode		15		mA
			f = 75 MHz, 12-bit high-freq mode		11		
			f = 50 MHz, 12-bit low-freq mode		16		
		V_{DDIO} = 1.89 V C_L = 4 pF Random pattern	f = 100 MHz, 10-bit mode		8		mA
			f = 75 MHz, 12-bit high-freq mode		4		
			f = 50 MHz, 12-bit low-freq mode		9		
		V_{DDIO} = 3.6 V C_L = 4 pF WORST CASE pattern	f = 100 MHz, 10-bit mode		36		mA
			f = 75 MHz, 12-bit high-freq mode		29		
			f = 50 MHz, 12-bit low-freq mode		20		
		V_{DDIO} = 3.6 V C_L = 4 pF Random pattern	f = 100 MHz, 10-bit mode		29		mA
			f = 75 MHz, 12-bit high-freq mode		22		
			f = 50 MHz, 12-bit low-freq mode		13		

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Electrical Characteristics (continued)

over recommended operating supply and temperature ranges unless otherwise specified.(1) (2) (3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DDR}	Deserializer (RX) VDDn supply current (includes load current)	V_{DDn} = 1.89 V C_L = 4 pF WORST CASE pattern	f = 100 MHz, 10-bit mode		64	110	mA
			f = 75 MHz, 12-bit high-frequency mode		67	114	
			f = 50 MHz, 12-bit low-frequency mode		63	96	
		V_{DDn} = 1.89 V C_L = 4 pF Random pattern	f = 100 MHz, 10-bit mode		57		
			f = 75 MHz, 12–bit high-frequency mode		60		
			f = 50 MHz, 12-bit low-frequency mode		56		
I_{DDRZ}	Deserializer (RX) supply current power-down	PBB = 0 V, all other LVCMOS Inputs=0 V	VDDIO = 1.89 V Default registers		42	400	µA
		PBB = 0 V, all other LVCMOS Inputs=0 V	VDDIO = 3.6 V Default registers		42	400	
I_{DDIORZ}	Deserializer (RX) VDD supply current power-down	PDB = 0 V, all other LVCMOS Inputs = 0 V	V_{DDIO} = 1.89 V		8	40	µA
			V_{DDIO} = 3.6 V		360	800	

8.6 Timing Requirements: Recommended for Serializer PCLK

over recommended operating supply and temperature ranges unless otherwise specified.(1)

		TEST CONDITIONS	PIN/FREQ	MIN	NOM	MAX	UNIT
t_{TCP}	Transmit clock period	10-bit mode		10	T	50	ns
		12-bit high-frequency mode		13.33	T	66.66	
		12-bit low-frequency mode		20	T	100	
t_{TCIH}	Transmit clock input high time			0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit clock input low time			0.4T	0.5T	0.6T	ns
t_{CLKT}	PCLK input transition time (Figure 12)	20 MHz–100 MHz, 10-bit mode		0.5T	2.5T	0.3T	ns
		15 MHz to 75 MHz, 12-bit high-frequency mode		0.5T	2.5T	0.3T	
		10 MHz to 50 MHz, 12-bit low-frequency mode		0.5T	2.5T	0.3T	
t_{JIT0}	PCLK input jitter (PCLK from imager mode)	Refer to jitter freq > f / 40	f = 10 to 100 MHz		0.1T		ns
t_{JIT1}	PCLK input jitter (external oscillator mode)	Refer to jitter freq > f / 40	f = 10 to 100 MHz		1T		ns
t_{JIT2}	External oscillator jitter				0.1		UI

(1) Recommended input timing requirements are input specifications and not tested in production.

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8.7 AC Timing Specifications (SCL, SDA) - I²C Compliant

over recommended supply and temperature ranges unless otherwise specified. (See Figure 5)

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
RECOMMENDED INPUT TIMING REQUIREMENTS						
f_{SCL}	SCL clock frequency	Standard mode	>0		100	kHz
		Fast mode	>0		400	
t_{LOW}	SCL low period	Standard mode	4.7			µs
		Fast mode	1.3			
t_{HIGH}	SCL high period	Standard mode	4.0			µs
		Fast mode	0.6			
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard mode	4			µs
		Fast mode	0.6			
$t_{SU:STA}$	Setup time for a start or a repeated start condition	Standard mode	4.7			µs
		Fast mode	0.6			
$t_{HD:DAT}$	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		900	
$t_{SU:DAT}$	Data setup time	Standard mode	250			ns
		Fast mode	100			
$t_{SU:STO}$	Setup time for STOP condition	Standard mode	4			µs
		Fast mode	0.6			
t_{BUF}	Bus free time between stop and start	Standard mode	4.7			µs
		Fast mode	1.3			
t_r	SCL and SDA rise time	Standard mode			1000	ns
		Fast mode			300	
t_f	SCL and SDA fall time	Standard mode			300	ns
		Fast mode			300	

8.8 Bidirectional Control Bus DC Timing Specifications (SCL, SDA) - I²C Compliant

over recommended supply and temperature ranges unless otherwise specified(1)

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
RECOMMENDED INPUT TIMING REQUIREMENTS						
V_{IH}	Input high level	SDA and SCL	0.7 × V_{DDIO}		V_{DDIO}	V
V_{IL}	Input low level	SDA and SCL	GND		0.3 × V_{DDIO}	V
V_{HY}	Input hysteresis			>50		mV
V_{OL}	Output low level	SDA, I_{OL} = 0.5 mA	0		0.4	V
I_{IN}	Input current	SDA or SCL, V_{IN} = V_{DDOP} OR GND	−10		10	µA
t_R	SDA rise time-READ	SDA, RPU = 10 kΩ, Cb ≤ 400 pF (see Figure 5)		430		ns
t_F	SDA fall time-READ			20		ns
$t_{SU;DAT}$		See Figure 5		560		ns
$t_{HD;DAT}$		See Figure 5		615		ns
t_{SP}				50		ns
C_{IN}		SDA or SCL		<5		pF

(1) Specification is ensured by design.

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8.9 Switching Characteristics: Serializer

over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LHT}	CML low-to-high transition time	R_L = 100 Ω (see Figure 7)		150	330	ps
t_{HLT}	CML high-to-low transition time	R_L = 100 Ω (see Figure 7)		150	330	ps
t_{DIS}	Data input setup to PCLK	Serializer data inputs (see Figure 13)	2			ns
t_{DIH}	Data input hold from PCLK	Serializer data inputs (see Figure 13)	2			ns
t_{PLD}	Serializer PLL lock time	R_L = 100 Ω(1) (2), (see Figure 14)		1	2	ms
t_{SD}	Serializer delay(2)	R_T = 100 Ω, 10-bit mode Register 0x03h b[0] (TRFB = 1) (see Figure 15)	32.5T	38T	44T	ns
		R_T = 100 Ω, 12-bit mode Register 0x03h b[0] (TRFB = 1) (see Figure 15)	11.75T	13T	15T	ns
t_{JIND}	Serializer output deterministic jitter	Serializer output intrinsic deterministic jitter. Measured (cycle-cycle) with PRBS-7 test pattern(3) (4)		0.13		UI
t_{JINR}	Serializer output random jitter	Serializer output intrinsic random jitter (cycle-cycle). Alternating-1,0 pattern.(3) (4)		0.04		UI
t_{JINT}	Peak-to-peak serializer output jitter	Serializer output peak-to-peak jitter includes deterministic jitter, random jitter, and jitter transfer from serializer input. Measured (cycle-cycle) with PRBS-7 test pattern.(3) (4)		0.396		UI
λ_{STXBW}	Serializer jitter transfer function –3-dB bandwidth(5)	PCLK = 100 MHz 10-bit mode. Default registers		2.2		MHz
		PCLK = 75 MHz 12-bit high-frequency mode. Default registers		2.2		MHz
		PCLK = 50 MHz 12-bit low-frequency mode. Default registers		2.2		MHz
δ_{STX}	Serializer jitter transfer function (peaking)(5)	PCLK = 100 MHz 10-bit mode. Default Registers		1.06		dB
		PCLK = 75 MHz 12-bit high-frequency mode. Default registers		1.09		dB
		PCLK = 50 MHz 12-bit low-frequency mode. Default registers		1.16		dB
δ_{STXf}	Serializer jitter transfer function (peaking frequency)(5)	PCLK = 100 MHz 10-bit mode. Default registers		400		kHz
		PCLK = 75 MHz 12-bit high-frequency mode. Default registers		500		kHz
		PCLK = 50 MHz 12-bit low-frequency mode. Default registers		600		kHz

(1) t_{PLD} and t_{DDLT} is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active PCLK
(2) Specification is ensured by design.
(3) Typical values represent most likely parametric norms at 1.8 V or 3.3 V, T_A = 25°C, and at the recommended operation conditions at the time of product characterization and are not specified.
(4) UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with PCLK frequency.
(5) Specification is ensured by characterization and is not tested in production.

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8.10 Switching Characteristics: Deserializer

over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ	MIN	TYP	MAX	UNIT
t_{RCP}	Receiver output clock period	10-bit mode	PCLK (see Figure 19)	10		50	ns
		12-bit high-frequency mode		13.33		66.66	
		12-bit low-frequency mode		10		100	
t_{PDC}	PCLK duty cycle	10-bit mode	PCLK	45%	50%	55%	
		12-bit high-frequency mode		40%	50%	60%	
		12-bit low-frequency mode		40%	50%	60%	
t_{CLH}	LVCMOS low-to-high transition time	V_{DDIO}: 1.71 V to 1.89 V or 3.0 V to 3.6 V, C_L = 8 pF (lumped load) Default registers (see Figure 17)(1)	PCLK	1.3	2	2.8	ns
t_{CHL}	LVCMOS high-to-low transition time			1.3	2	2.8	ns
t_{CLH}	LVCMOS low-to-high transition time	V_{DDIO}: 1.71 V to 1.89 V or 3.0 V to 3.6 V, C_L = 8 pF (lumped load) Default registers (see Figure 17)(1)	ROUT[11:0], HS, VS	1	2.5	4	ns
t_{CHL}	LVCMOS high-to-low transition time			1	2.5	4	ns
t_{ROS}	ROUT setup data to PCLK	V_{DDIO}: 1.71 V to 1.89 V or 3.0 V to 3.6 V, C_L = 8 pF (lumped load) Default registers (see Figure 19)	ROUT[11:0], HS, VS	0.38T	0.5T		ns
t_{ROH}	ROUT hold data to PCLK			0.38T	0.5T		ns
t_{DD}	Deserializer delay	Default registers Register 0x03h b[0] (RRFB = 1) (see Figure 18)(1)	10-bit mode	154T		158T	ns
			12-bit low-frequency mode	109T		112T	
			12-bit high-frequency mode	73T		75T	
t_{DDLT}	Deserializer data lock time	With Adaptive Equalization (see Figure 16)	10-bit mode		15	22	ms
			12-bit low-frequency mode		15	22	
			12-bit high-frequency mode		15	22	
t_{RCJ}	Receiver clock jitter	PCLK SSCG[3:0] = OFF(1)	10-bit mode PCLK = 100 MHz		20	30	ps
			12-bit low-frequency mode PCLK = 50 MHz		22	35	
			12-bit high-frequency mode PCLK = 75 MHz		45	90	
t_{DPJ}	Deserializer period jitter	PCLK SSCG[3:0] = OFF(1) (2)	10-bit mode PCLK = 100 MHz		170	815	ps
			12-bit low-frequency mode PCLK= 50 MHz		180	330	
			12-bit high-frequency mode PCLK= 75 MHz		300	515	

(1) Specification is ensured by characterization and is not tested in production.
(2) t_{DPJ} is the maximum amount the period is allowed to deviate measured over 30,000 samples.

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Switching Characteristics: Deserializer (continued)

over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ	MIN	TYP	MAX	UNIT
t_{DCCJ}	Deserializer cycle-to-cycle clock jitter	PCLK SSCG[3:0] = OFF (1) (3)	10-bit mode PCLK = 100 MHz		440	1760	ps
			12-bit low-frequency mode PCLK = 50 MHz		460	730	
			12-bit high-frequency mode PCLK = 75 MHz		565	985	
fdev	Spread spectrum clocking deviation frequency	LVCMOS output bus SSC[3:0] = ON (see Figure 24) (1)	10 MHz–100 MHz		±0.5 to ±1.5%		
fmod	Spread spectrum clocking modulation frequency		10 MHz–100 MHz		5 to 50		kHz

(3) t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles measured over 30,000 samples.

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8.11 Typical Characteristics

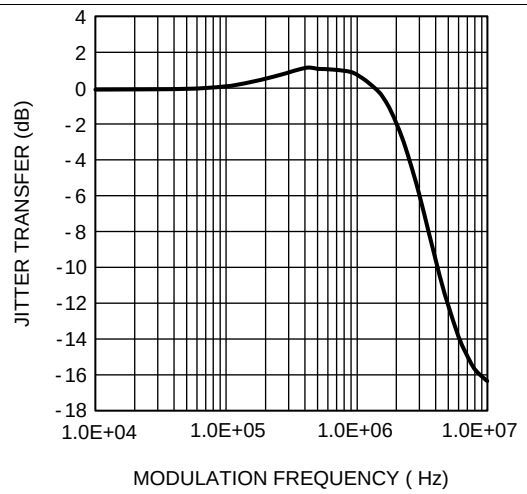

Figure 1. Typical Serializer Jitter Transfer Function at 100 MHz

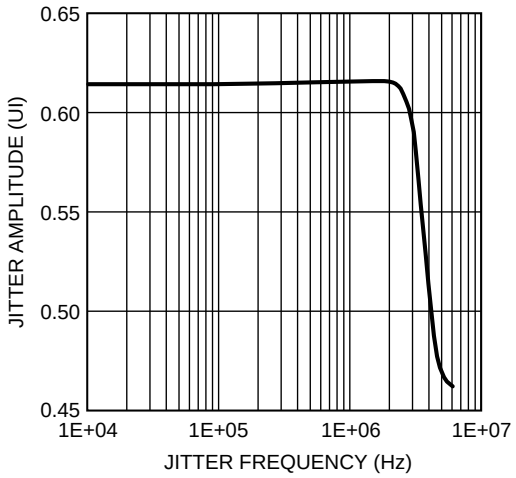

Figure 2. Typical Deserializer Input Jitter Tolerance Curve at 1.4-Gbps Line Rate

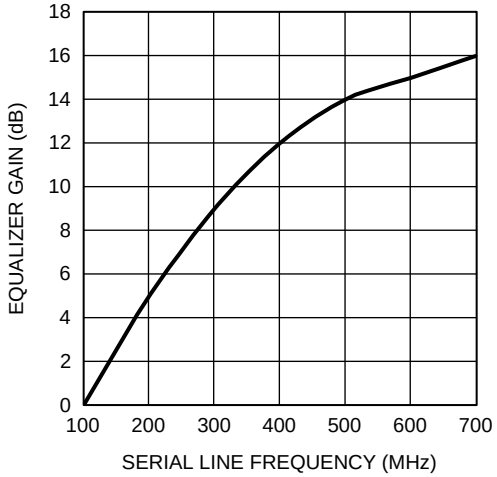

Figure 3. Maximum Equalizer Gain vs. Line Frequency

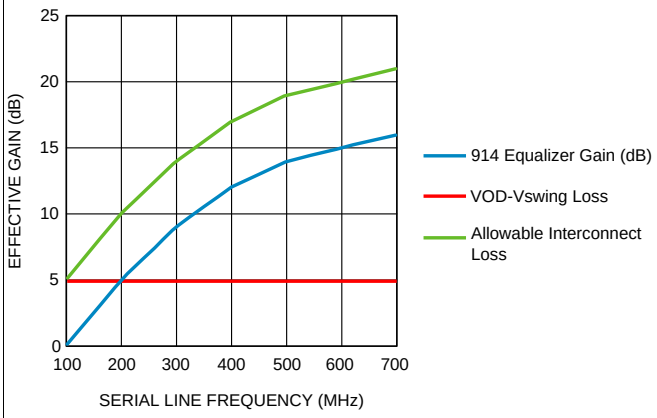

Figure 4. Adaptive Equalizer – Interconnect Loss Compensation

9 Parameter Measurement Information

9.1 AC Timing Diagrams and Test Circuits

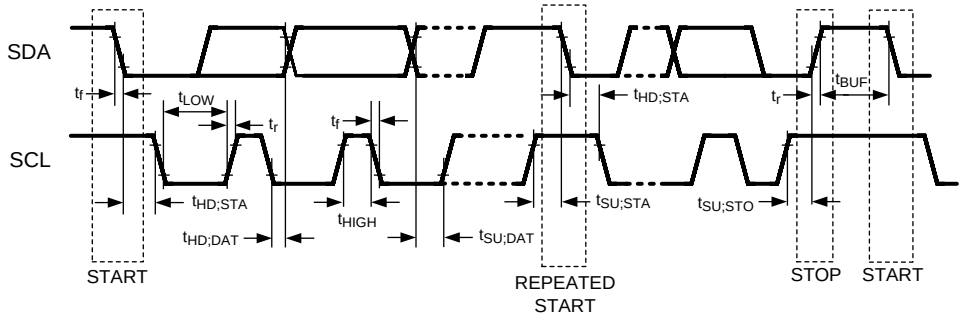

Figure 5. Bidirectional Control Bus Timing

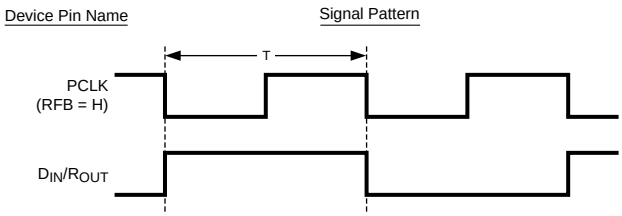

Figure 6. *Worst Case* Test Pattern

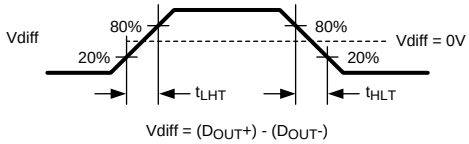

Figure 7. Serializer CML Output Load and Transition Times

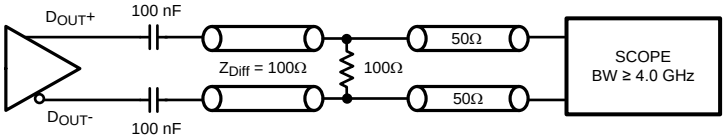

Figure 8. Serializer CML Output Load and Transition Times

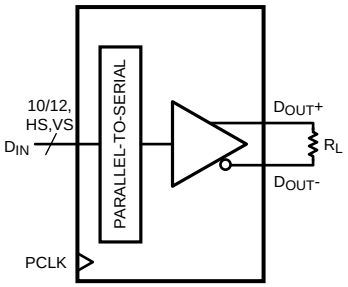

Figure 9. Serializer VOD Diagram

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AC Timing Diagrams and Test Circuits (continued)

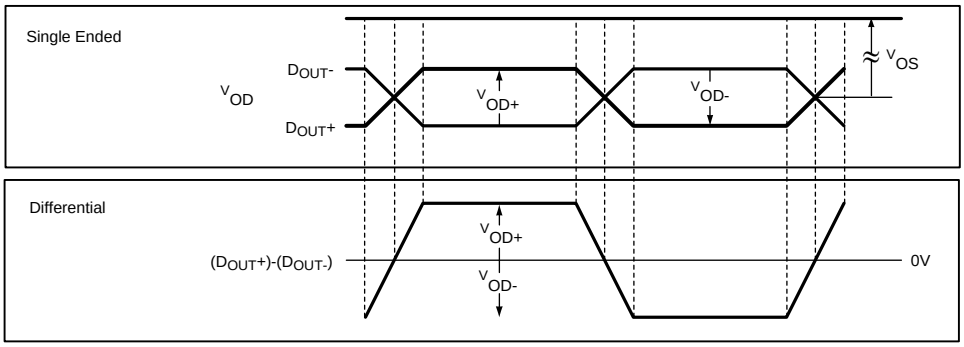

Figure 10. Serializer VOD Diagram

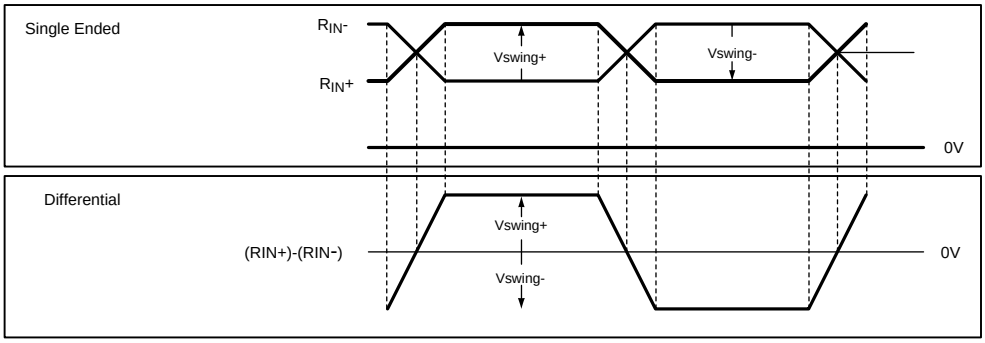

Figure 11. Differential Vswing Diagram

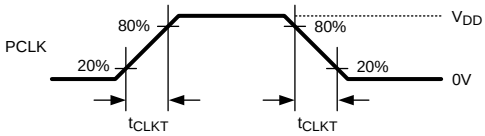

Figure 12. Serializer Input Clock Transition Times

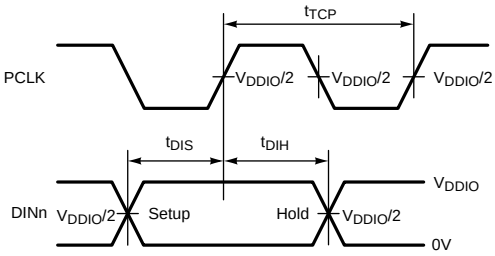

Figure 13. Serializer Set-Up and Hold Times

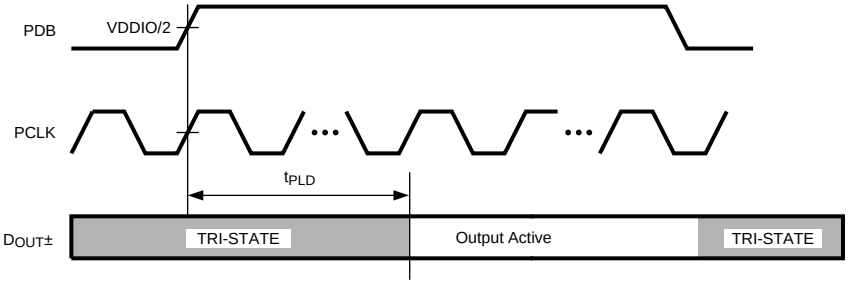

Figure 14. Serializer PLL Lock Time

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AC Timing Diagrams and Test Circuits (continued)

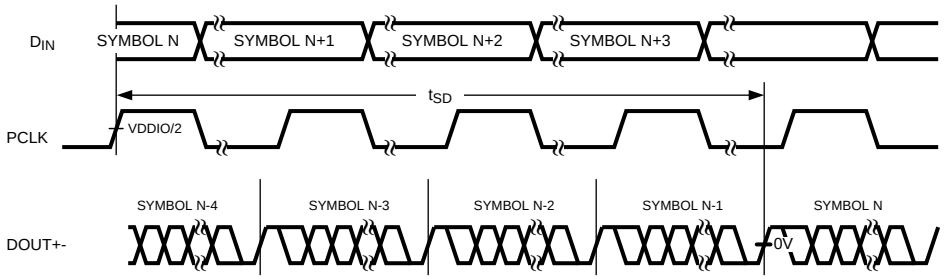

Figure 15. Serializer Delay

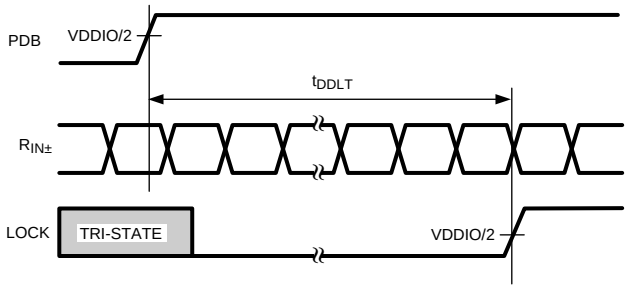

Figure 16. Deserializer Data Lock Time

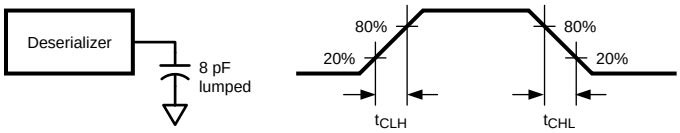

Figure 17. Deserializer LVCMOS Output Load and Transition Times

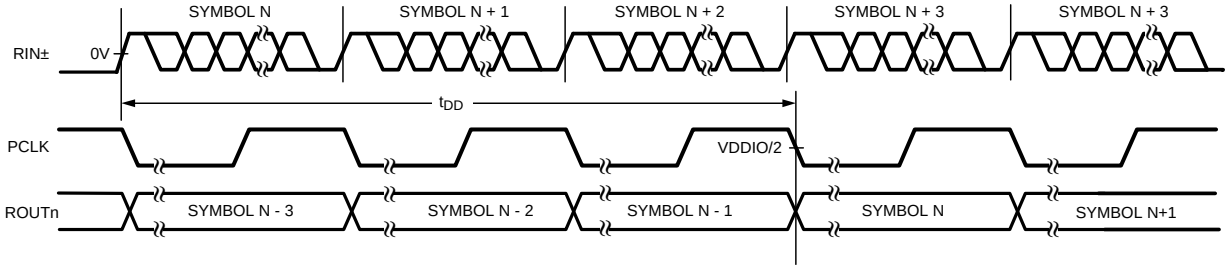

Figure 18. Deserializer Delay

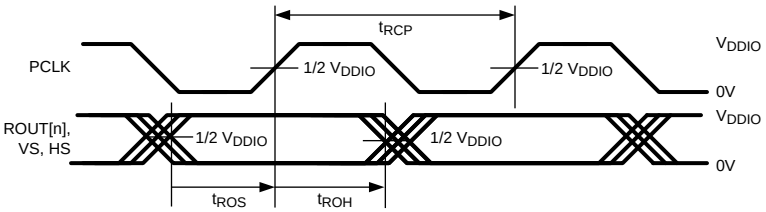

Figure 19. Deserializer Output Set-Up and Hold Times

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AC Timing Diagrams and Test Circuits (continued)

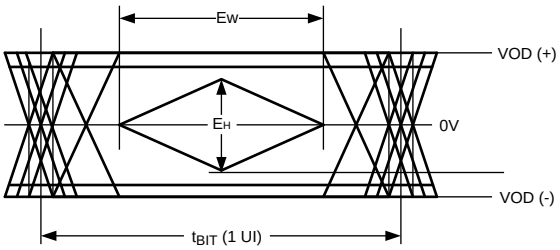

Figure 20. CML Output Driver

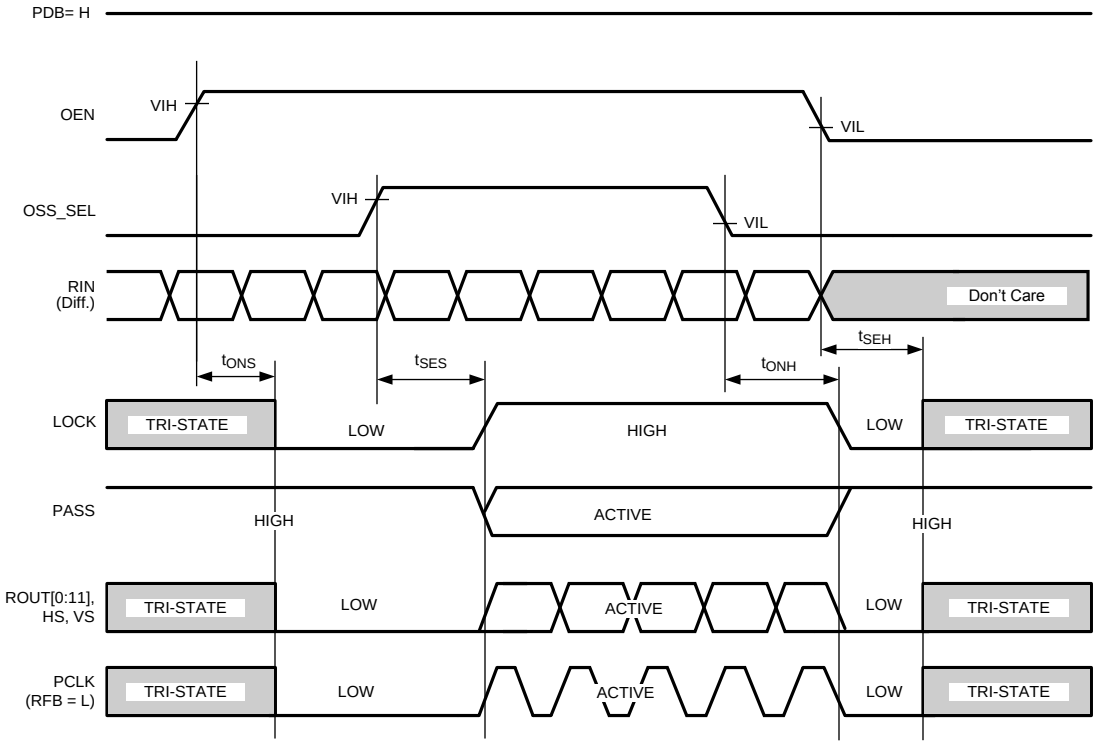

Figure 21. Output State (Set-Up and Hold) Times

AC Timing Diagrams and Test Circuits (continued)

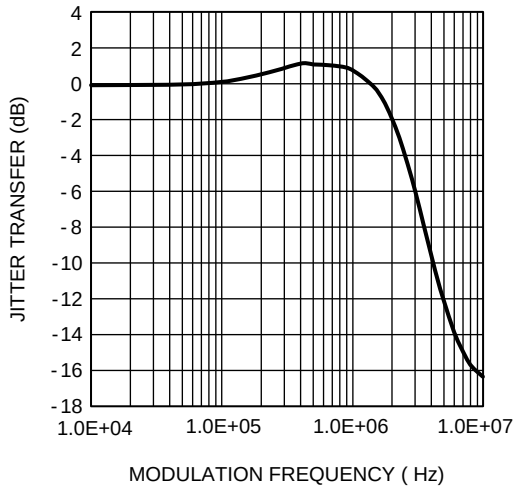

Figure 22. Typical Serializer Jitter Transfer Function at 100 MHz

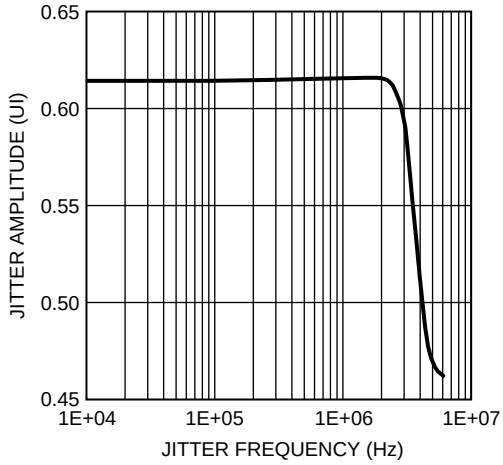

Figure 23. Typical Deserializer Input Jitter Tolerance Curve at 1.4-Gbps Line Rate

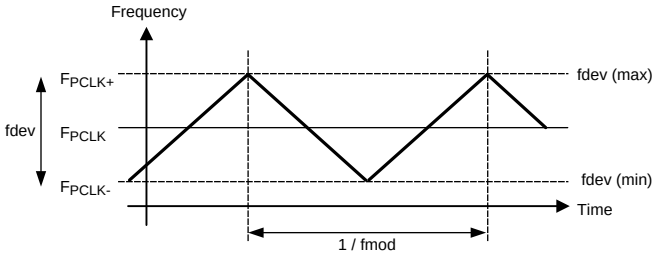

Figure 24. Spread Spectrum Clock Output Profile

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10 Detailed Description

10.1 Overview

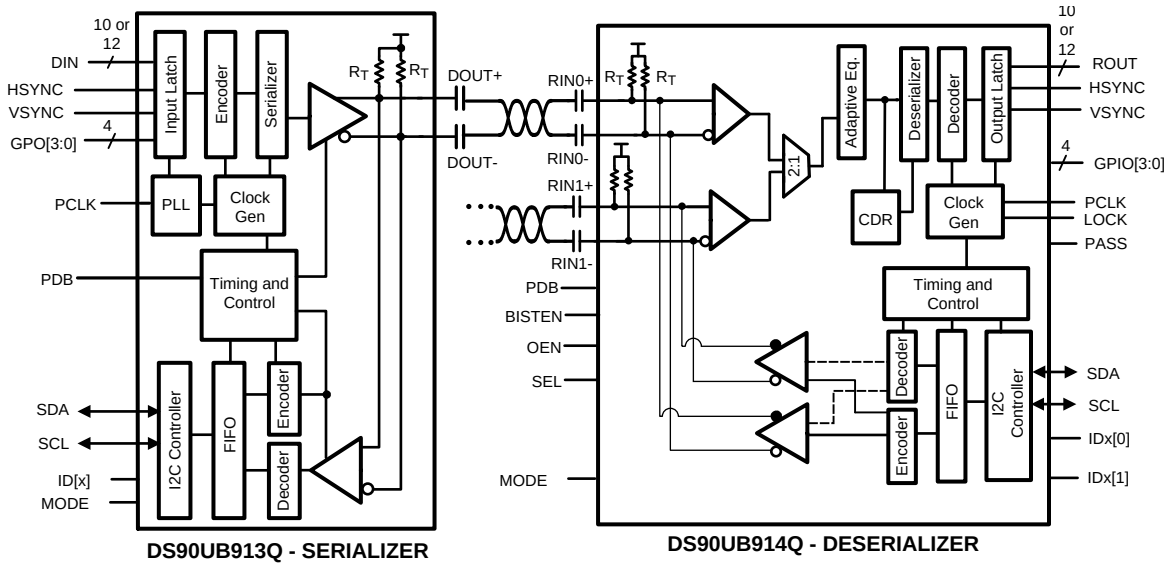
The DS90UB91xQ-Q1 FPD-Link III chipsets are intended to link megapixel camera imagers and video processors in ECUs. The serializer and deserializer chipset can operate from 10-MHz to 100-MHz pixel clock frequency. The DS90UB913Q-Q1 device transforms a 10- and 12-bit wide parallel LVCMOS data bus along with a bidirectional control channel control bus into a single high-speed differential pair. The high-speed serial bit stream contains an embedded clock and DC-balanced information which enhances signal quality to support AC coupling. The DS90UB914Q-Q1 device receives the single serial data stream and converts it back into a 10- and 12-bit wide parallel data bus together with the control channel data bus. The DS90UB91xQ-Q1 chipsets can accept up to:

- 12 bits of DATA+2 bits SYNC for an input PCLK range of 10 MHz-50 MHz in the 12-bit low-frequency mode
- 12 bits DATA + 2 SYNC bits for an input PCLK range of 15 MHz to 75 MHz in the 12-bit high-frequency mode
- 10 bits DATA + 2 SYNC bits for an input PCLK range of 20 MHz to 100 MHz in the 10-bit mode.

The DS90UB914Q-Q1 chipset has a 2:1 multiplexer that allows customers to select between two serializer inputs. The control channel function of the DS90UB91xQ-Q1 chipset provides bidirectional communication between the image sensor and ECUs. The integrated bidirectional control channel transfers data bidirectionally over the same differential pair used for video data interface. This interface offers advantages over other chipsets by eliminating the need for additional wires for programming and control. The bidirectional control channel bus is controlled through an I^2C port. The bidirectional control channel offers asymmetrical communication and is not dependent on video blanking intervals.

The DS90UB91xQ-Q1 chipset offer customers the choice to work with different clocking schemes. The DS90UB91xQ-Q1 chipsets can use an external oscillator as the reference clock source for the PLL or PCLK from the imager as primary reference clock to the PLL.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Serial Frame Format

The high-speed forward channel is composed of 28 bits of data containing video data, sync signals, I^2C and parity bits. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced and scrambled. The 28-bit frame structure changes in the 12-bit low-frequency mode, 12-bit high frequency mode and the 10-bit mode internally and is seamless to the customer. The bidirectional control channel data is transferred over the single serial link along with the high-speed forward data. This architecture provides a full duplex low-speed forward and backward path across the serial link together with a high-speed forward channel without the dependence on the video blanking phase.

10.3.2 Line Rate Calculations for the DS90UB91xQ

The DS90UB913Q-Q1 device divides the clock internally by divide-by-1 in the 12-bit low-frequency mode, by divide-by-2 in the 10-bit mode and by divide-by-1.5 in the 12-bit high-frequency mode. Conversely, the DS90UB914Q-Q1 multiplies the recovered serial clock to generate the proper pixel clock output frequency. Thus the maximum line rate in the three different modes remains 1.4 Gbps. The following are the formulae used to calculate the maximum line rate in the different modes.

- For 12-bit low-frequency mode, Line rate = f_{PCLK} × 28; that is, f_{PCLK}= 50 MHz, line rate = 50 × 28 = 1.4 Gbps
- For 10-bit mode, Line rate = f_{PCLK} / 2 × 28; that is, f_{PCLK}= 100 MHz, line rate = (100 / 2) × 28 = 1.4 Gbps
- For the 12-bit high-frequency mode, Line rate = f_{PCLK} × (2 / 3) × 28; that is, f_{PCLK}= 75 MHz, line rate = (75) × (2 / 3) × 28 = 1.4 Gbps

10.3.3 Deserializer Multiplexer Input

The DS90UB914Q-Q1 offers a 2:1 multiplexer that can be used to select which camera is used as the input. Figure 25 shows the operation of the 2:1 multiplexer in the deserializer. The selection of the camera can be pin controlled as well as register controlled. Both the deserializer inputs cannot be enabled at the same time. If the Serializer A is selected as the active serializer, the back-channel for Deserializer A turns ON and vice versa. To switch between the two cameras, first the Serializer B has to be selected using the SEL pin/register on the deserializer. After that the back channel driver for Deserializer B has to be enabled using the register in the deserializer.

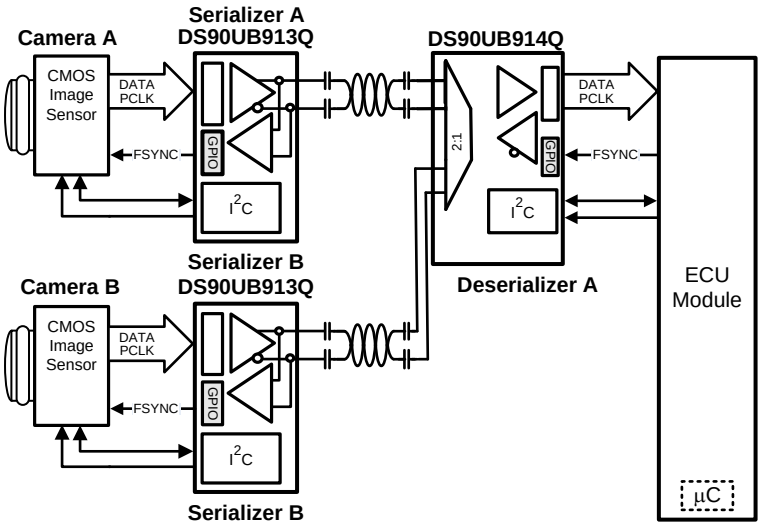


Figure 25. Using the Multiplexer on the Deserializer to Enable a Two-Camera System

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Feature Description (continued)

10.3.4 Error Detection

The chipset provides error detection operations for validating data integrity in long distance transmission and reception. The data error detection function offers users flexibility and usability of performing bit-by-bit data transmission error checking. The error detection operating modes support data validation of the following signals:

- Bidirectional control channel data across the serial link
- Parallel video/sync data across the serial link

The chipset provides one parity bit on the forward channel and 4 CRC bits on the back channel for error detection purposes. The DS90UB91xQ-Q1 chipset checks the forward and back channel serial links for errors and stores the number of detected errors in two 8-bit registers in the serializer and the deserializer respectively.

To check parity errors on the forward-channel, monitor registers 0x1A and 0x1B on the deserializer. If there is a loss of LOCK, then the counters on registers 0x1A and 0x1B are reset.

NOTE

Whenever there is a parity error on the forward channel, the PASS pin will go low.

To check CRC errors on the back-channel, monitor registers 0x0A and 0x0B on the serializer.

10.3.5 Description of Bidirectional Control Bus and I^{2}C Modes

The I^{2}C-compatible interface allows programming of the DS90UB913Q-Q1, DS90UB914Q-Q1, or an external remote device (such as image sensor) through the bidirectional control channel. Register programming transactions to/from the DS90UB913xQ-Q1 chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open-drain I/Os and both lines must be pulled up to VDDIO by an external resistor. Pullup resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic LOW is transmitted by driving the output low. Logic HIGH is transmitted by releasing the output and allowing it to be pulled up externally. The appropriate pullup resistor values will depend upon the total bus capacitance and operating speed. The DS90UB91xQ-Q1 I^{2}C bus data rate supports up to 400 kbps according to I^{2}C fast mode specifications.

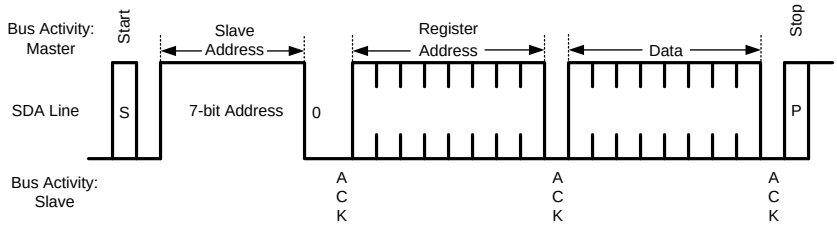

Figure 26. Write Byte

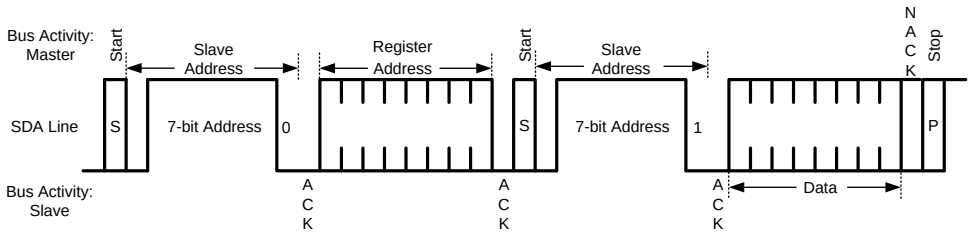

Figure 27. Read Byte

Feature Description (continued)

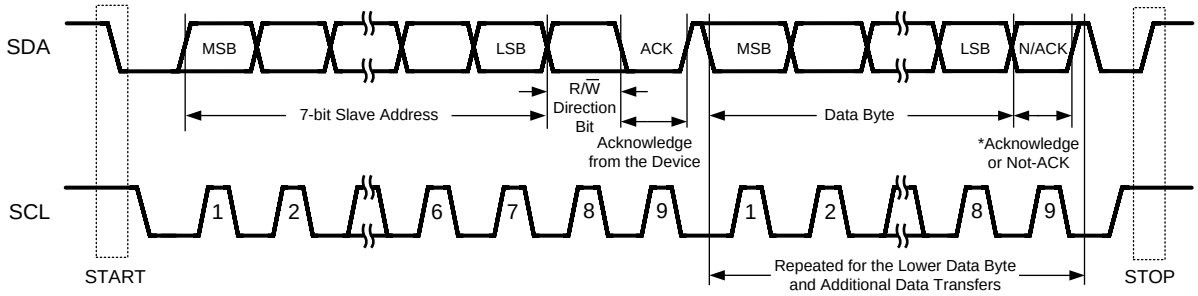

Figure 28. Basic Operation

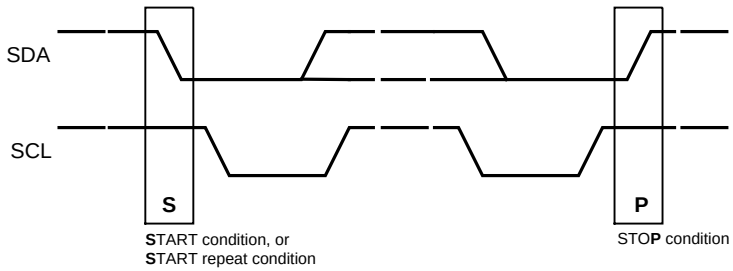

Figure 29. Start and Stop Conditions

10.3.6 Slave Clock Stretching

The I^{2}C-compatible interface allows programming of the DS90UB913Q-Q1, DS90UB914Q-Q1, or an external remote device (such as image sensor) through the bidirectional control.

NOTE

To communicate and synchronize with remote devices on the I^{2}C bus through the bidirectional control channel/MCU, the chipset utilizes bus clock stretching (holding the SCL line low) during data transmission where the I^{2}C slave pulls the SCL line low on the 9th clock of every I^{2}C transfer (before the ACK signal).

The slave device will not control the clock and only stretches it until the remote peripheral has responded. The I^{2}C master must support clock stretching to operate with the DS90UB91xQ-Q1 chipset.

10.3.7 I^{2}C Pass-Through

I^{2}C pass-through provides an alternative means to independently address slave devices. The mode enables or disables I^{2}C bidirectional control channel communication to the remote I^{2}C bus. This option is used to determine whether or not an I^{2}C instruction is to be transferred over to the remote I^{2}C device. When enabled, the I^{2}C bus traffic will continue to pass through, I^{2}C commands will be excluded to the remote I^{2}C device. The pass-through function also provides access and communication to only specific devices on the remote bus.

See Figure 30 for an example of this function.

If master controller transmits I^{2}C transaction for address 0xA0, the SER A with I^{2}C pass-through enabled will transfer I^{2}C commands to remote Camera A. The SER B with I^{2}C pass-through disabled, any I^{2}C commands will be bypassed on the I^{2}C bus to Camera B.

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Feature Description (continued)

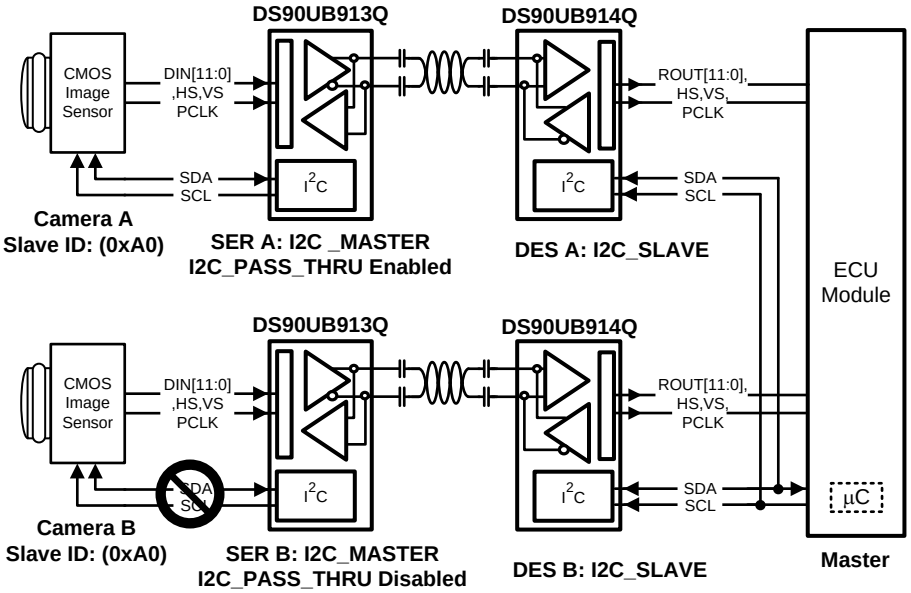

Figure 30. I²C Pass-Through

10.3.8 ID[x] Address Decoder on the Serializer

The ID[x] pin on the serializer is used to decode and set the physical slave address of the serializer (I^2C only) to allow up to five devices on the bus connected to the serializer using only a single pin. The pin sets one of the 5 possible addresses for each serializer device. The pin must be pulled to VDD (1.8 V, not VDDIO) with a 10-kΩ resistor and a pulldown resistor (RID) of the recommended value to set the physical device address. The recommended maximum resistor tolerance is 1%.

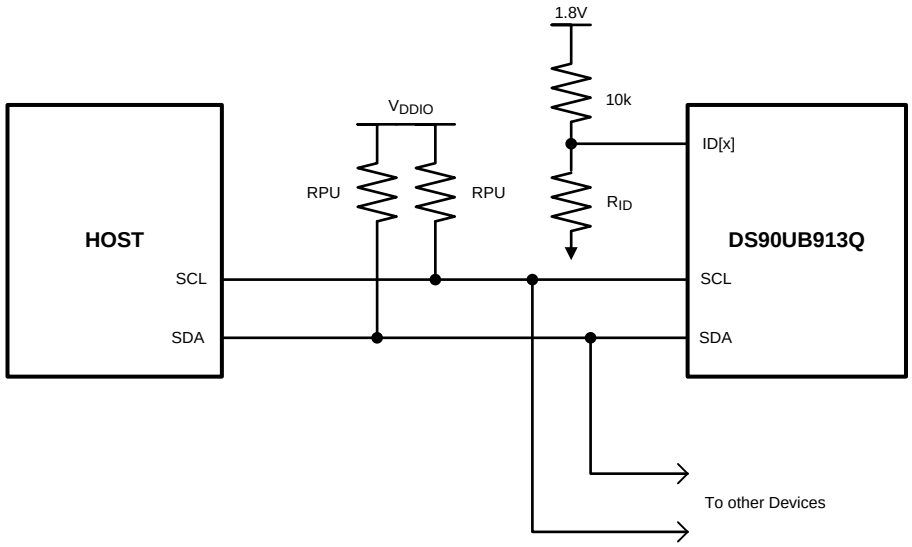

Figure 31. ID[x] Address Decoder on the Serializer

Table 1. ID[x] Resistor Value for DS90UB913Q-Q1 Serializer

ID[x] Resistor Value — DS90UB913Q-Q1 Serializer		
Resistor RID0 Ω (1% Tolerance)	**Address 7'b**	**Address 8'b 0 appended (WRITE)**
0 k	0x58	0xB0
2 k	0x59	0xB2
4.7 k	0x5A	0xB4
8.2 k	0x5B	0xB6
14 k	0x5C	0xB8
100 k	0x5D	0xBA

10.3.9 ID[x] Address Decoder on the Deserializer

The IDx[0] and IDx[1] pins on the deserializer are used to decode and set the physical slave address of the deserializer (I^2C only) to allow up to 16 devices on the bus using only two pins. The pins set one of 16 possible addresses for each deserializer device. As there will be more deserializer devices connected on the same board than serializers, more I^2C device addresses have been defined for the DS90UB914Q-Q1 deserializer than the DSDS90UB913Q-Q1 serializer. The pins must be pulled to VDD (1.8 V, not VDDIO) with a 10-kΩ resistor and two pulldown resistors (RID0 and RID1) of the recommended value to set the physical device address. The recommended maximum resistor tolerance is 1%.

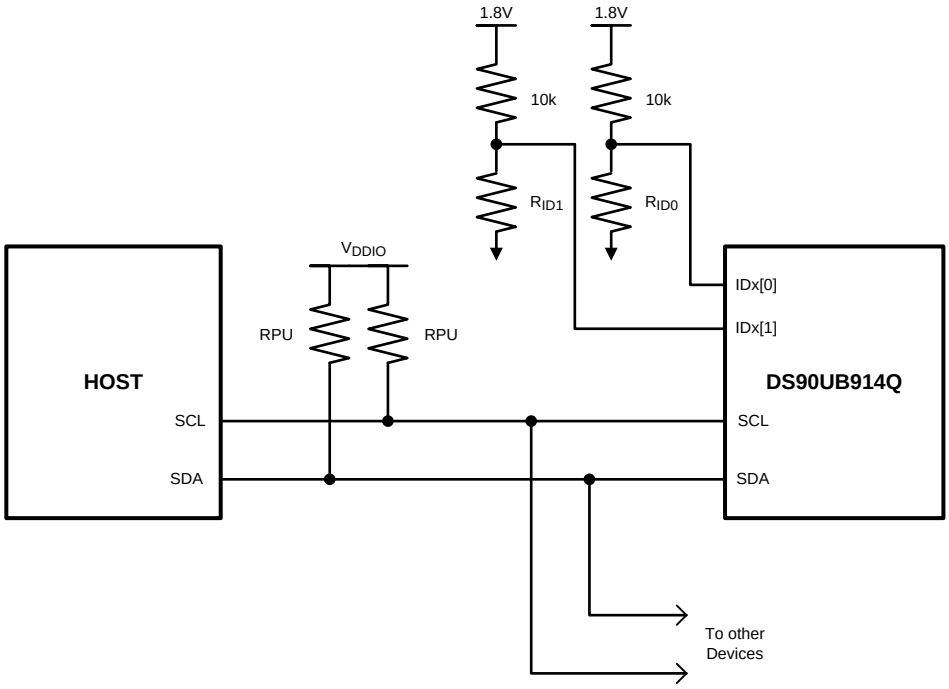

Figure 32. ID[x[Address Decoder on the Deserializer

Table 2. Resistor Values for IDx[0] and IDx[1] on DS90UB914Q-Q1 Deserializer

ID[X] RESISTOR VALUE — DS90UB913Q SERIALIZER			
RESISTOR RID1 Ω (1%TOLERANCE)	**RESISTOR RID0 Ω** (1%TOLERANCE)	**ADDRESS 7'b**	**ADDRESS 8'b 0 APPENDED (WRITE)**
0 k	0 k	0x60	0xC0
0 k	3 k	0x61	0xC2
0 k	11 k	0x62	0xC4
0 k	100 k	0x63	0xC6
3 k	0 k	0x64	0xC8

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Table 2. Resistor Values for IDx[0] and IDx[1] on DS90UB914Q-Q1 Deserializer (continued)

ID[X] RESISTOR VALUE — DS90UB913Q SERIALIZER			
3 k	3 k	0x65	0xCA
3 k	11 k	0x66	0XCC
3 k	100 k	0x67	0XCE
11 k	0 k	0x68	0XD0
11 k	3 k	0x69	0XD2
11 k	11 k	0x6A	0XD4
11 k	100 k	0x6B	0XD6
100 k	0 k	0x6C	0XD8
100 k	3 k	0x6D	0XDA
100 k	11 k	0x6E	0XDC
100 k	100 k	0x6F	0XDE

10.3.10 Programmable Controller

An integrated I^2C slave controller is embedded in the DS90UB913Q-Q1 serializer as well as the DS90UB914Q-Q1 deserializer. It must be used to configure the extra features embedded within the programmable registers or it can be used to control the set of programmable GPIOs.

10.3.11 Synchronizing Multiple Cameras

For applications requiring multiple cameras for frame-synchronization, TI recommends to utilize the General-Purpose Input/Output (GPIO) pins to transmit control signals to synchronize multiple cameras together. To synchronize the cameras properly, the system controller needs to provide a field sync output (such as a vertical or frame sync signal) and the cameras must be set to accept an auxiliary sync input. The vertical synchronize signal corresponds to the start and end of a frame and the start and end of a field.

NOTE

this form of synchronization timing relationship has a non-deterministic latency. After the control data is reconstructed from the bidirectional control channel, there will be a time variation of the GPIO signals arriving at the different target devices (between the parallel links). The maximum latency delta (t1) of the GPIO data transmitted across multiple links is 25 µs.

NOTE

The user must verify that the timing variations between the different links are within their system and timing specifications.

See Figure 33 for an example of synchronizing multiple cameras.

The maximum time (t1) between the rising edge of GPIO (that is, sync signal) arriving at Camera A and Camera B is 25 µs.

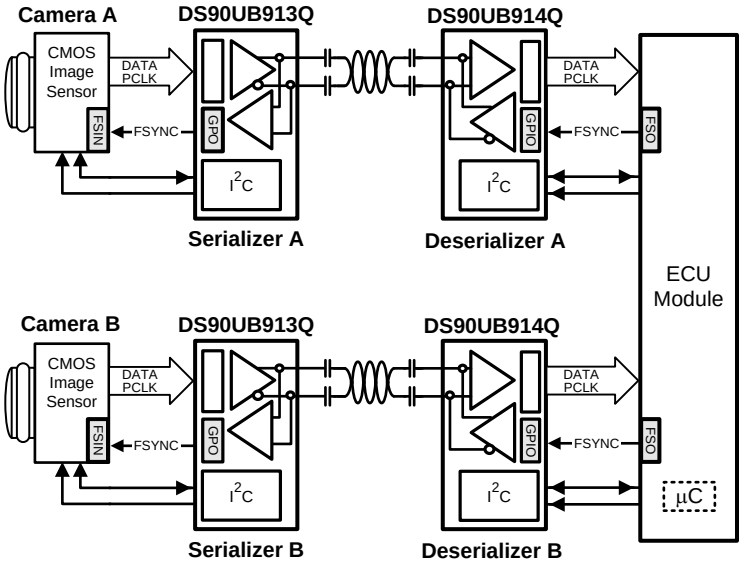

Figure 33. Synchronizing Multiple Cameras

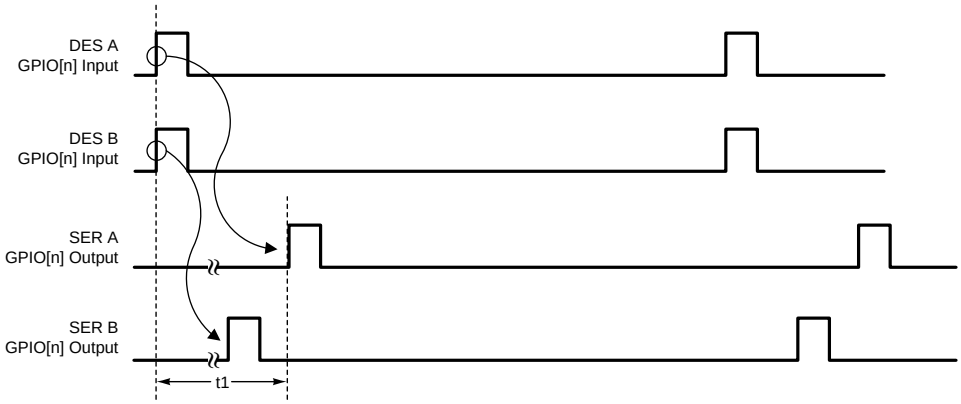

Figure 34. GPIO Delta Latency

10.3.12 General-Purpose I/O (GPIO) Descriptions

There are 4 GPOs on the serializer and 4 GPIOs on the deserializer when the DS90UB91xQ-Q1 chipsets are run off the pixel clock from the imager as the reference clock source. The GPOs on the serializer can be configured as outputs for the input signals that are fed into the deserializer GPIOs. In addition, the GPOs on the serializer can behave as outputs of the local register on the serializer. The GPIOs on the deserializer can be configured to be the input signals feeding the output of the GPOs on the serializer. In addition the GPIOs on the deserializer can be configured to behave as outputs of the local register on the deserializer. If the DS90UB91xQ-Q1 chipsets are run off the external oscillator source as the reference clock, then GPO3 on the serializer is automatically configured to be the input for the external clock and GPIO2 on the deserializer is configured to be the output of the divide-by-2 clock which is fed into the imager as its reference clock. In this case, the GPIO2 and GPIO3 on the deserializer can only behave as outputs of the local register on the deserializer. The GPIO maximum switching rate is up to 66 kHz when configured for communication between deserializer GPIO to serializer GPO.

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10.3.13 LVCMOS VDDIO Option

1.8-V, 2.8-V, and 3.3-V serializer inputs and 1.8-V and 3.3-V deserializer outputs are user configurable to provide compatibility with 1.8-V, 2.8-V and 3.3-V system interfaces.

10.3.14 Deserializer – Adaptive Input Equalization (AEQ)

The receiver inputs provide an adaptive input equalization filter in order to compensate for loss from the media. The level of equalization can also be manually selected through register controls. The fully-adaptive equalizer output can be seen using the CMLOUTP/CMLOUTN pins in the deserializer.

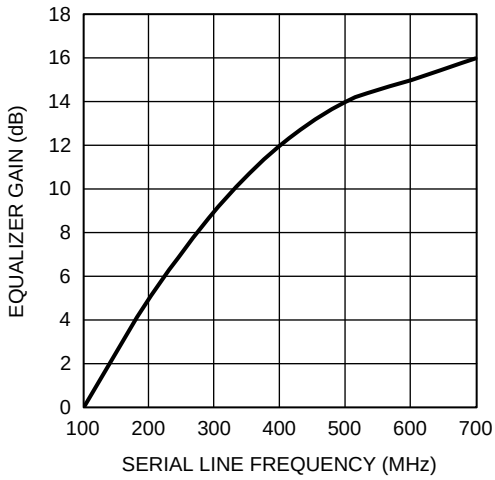

Figure 35. Maximum Equalizer Gain vs. Line Frequency

10.3.15 EMI Reduction

10.3.15.1 Deserializer Staggered Output

The receiver staggers output switching to provide a random distribution of transitions within a defined window. Outputs transitions are distributed randomly. This minimizes the number of outputs switching simultaneously and helps to reduce supply noise. In addition it spreads the noise spectrum out reducing overall EMI.

10.3.15.2 Spread Spectrum Clock Generation (SSCG) on the Deserializer

The DS90UB914Q-Q1 parallel data and clock outputs have programmable SSCG ranges from 10 MHz to 100 MHz. The modulation rate and modulation frequency variation of output spread is controlled through the SSC control registers on the DS90UB914Q-Q1 device. SSC profiles can be generated using bits [3:0] in register 0x02 in the deserializer.

10.4 Device Functional Modes

10.4.1 DS90UB91xQ-Q1 Operation With External Oscillator as Reference Clock

In some applications, the pixel clock that comes from the imager can have jitter which exceeds the tolerance of the DS90UB91xQ-Q1 chipsets. In this case, the DS90UB913Q-Q1 device should be operated by using an external clock source as the reference clock for the DS90UB91xQ-Q1 chipsets. This is the recommended operating mode. The external oscillator clock output goes through a divide-by-2 circuit in the DS90UB913Q-Q1 serializer and this divided clock output is used as the reference clock for the imager. The output data and pixel clock from the imager are then fed into the DS90UB913Q-Q1 device. Figure 36 shows the operation of the DS90UB1xQ-Q1 chipsets while using an external automotive grade oscillator.

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Device Functional Modes (continued)

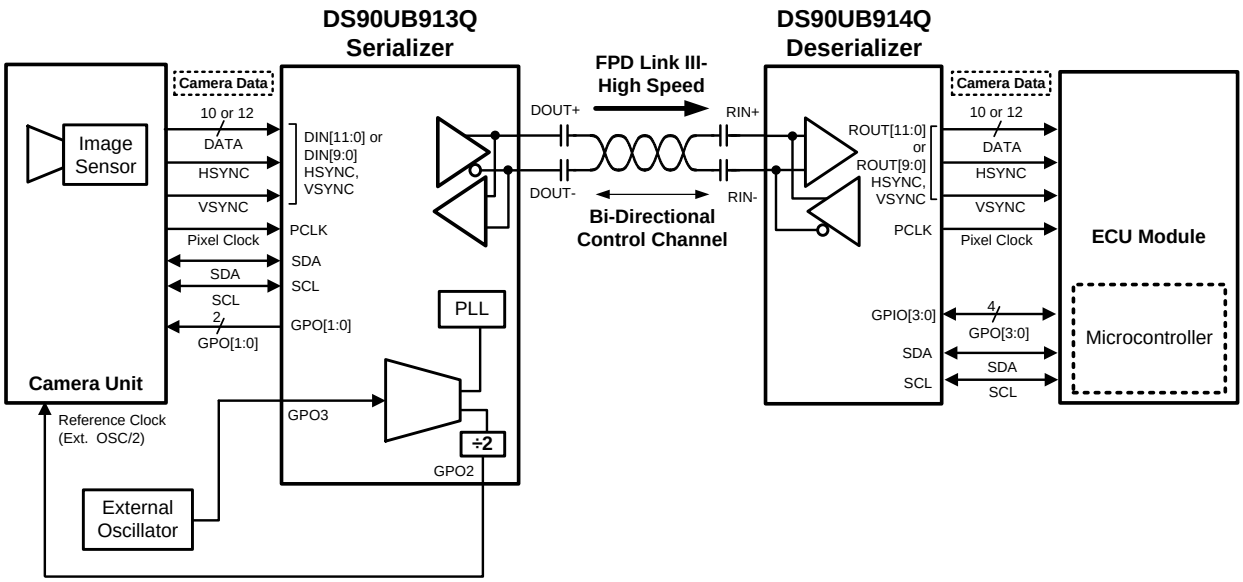

Figure 36. DS90UB91xQ-Q1 Operation in the External Oscillator Mode

When the DS90UB913Q-Q1 device is operated using an external oscillator, the GPO3 pin on the DS90UB913Q-Q1 is the input pin for the external oscillator. In applications where the DS90UB913Q-Q1 device is operated from an external oscillator, the divide-by-2 circuit in the DS90UB913Q-Q1 device feeds back the divided clock output to the imager device through GPO2 pin. The pixel clock to external oscillator ratios needs to be fixed for the 12-bit high-frequency mode and the 10-bit mode.

NOTE

In the 10-bit mode, the pixel clock frequency divided by the external oscillator frequency must be 2. In the 12-bit high-frequency mode, the pixel clock frequency divided by the external oscillator frequency must be 1.5.

For example, if the external oscillator frequency is 48 MHz in the 10-bit mode, the pixel clock frequency of the imager needs to be twice of the external oscillator frequency, that is, 96 MHz. If the external oscillator frequency is 48 MHz in the 12-bit high-frequency mode, the pixel clock frequency of the imager needs to be 1.5 times of the external oscillator frequency, that is, 72 MHz. In this mode, GPO2 and GPO3 on the serializer cannot act as the output of the input signal coming from GPIO2 or GPIO3 on the deserializer.

10.4.2 DS90UB91xQ-Q1 Operation With Pixel Clock from Imager as Reference Clock

The DS90UB91xQ-Q1 chipsets can be operated by using the pixel clock from the imager as the reference clock.Figure 37 shows the operation of the DS90UB91xQ-Q1 chipsets using the pixel clock from the imager. If the DS90UB913Q-Q1 device is operated using the pixel clock from the imager as the reference clock, then the imager uses an external oscillator as its reference clock. There are 4 GPIOs on the serializer and 4 GPIOs on the deserializer in this mode.

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Device Functional Modes (continued)

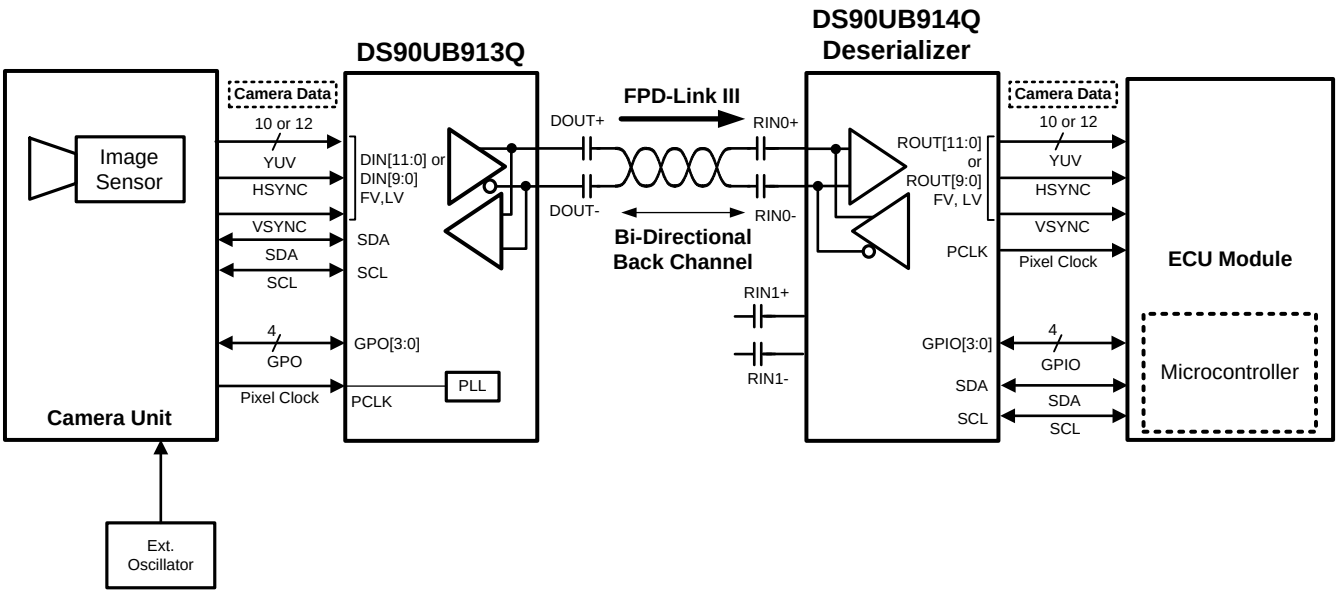

Figure 37. DS90UB91xQ-Q1 Operation in PCLK mode

10.4.3 MODE Pin on Serializer

The mode pin on the serializer can be configured to select if the DS90UB913Q-Q1 device is to be operated from the external oscillator or the PCLK from the imager. The pin must be pulled to V_{DD} (1.8 V, not V_{DDIO}) with a 10-kΩ resistor and a pulldown resistor (R_{MODE}) of the recommended value to set the modes shown in Figure 38. The recommended maximum resistor tolerance is 1%.

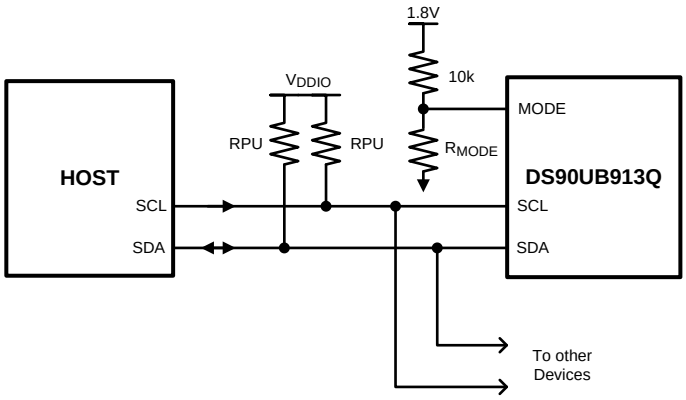

Figure 38. MODE Pin Configuration on DS90UB913Q-Q1

Table 3. DS90UB913Q-Q1 Serializer MODE Resistor Value

MODE SELECT	R_{MODE} RESISTOR VALUE
PCLK from imager mode	100 kΩ
External Oscillator mode	4.7 kΩ

10.4.4 MODE Pin on Deserializer

The mode pin on the deserializer can be used to configure the device to work in the 12-bit low-frequency mode, 12-bit high frequency mode or the 10-bit mode of operation. Internally, the DS90UB91xQ-Q1 chipset operates in a divide-by-1 mode in the 12-bit low-frequency mode, divide-by-2 mode in the 10-bit mode and a divide-by-1.5 mode in the 12-bit high-frequency mode. The pin must be pulled to V_{DD} (1.8 V, not V_{DDIO}) with a 10-kΩ resistor and a pulldown resistor (R_{MODE}) of the recommended value to set the different modes in the deserializer as mentioned in Table 4. The deserializer automatically configures the serializer to correct mode through the back-channel. The recommended maximum resistor tolerance is 1%

.

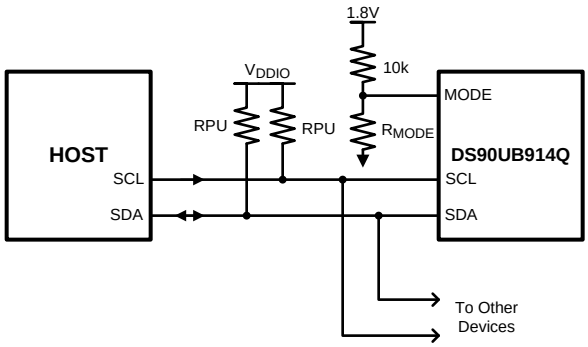

Figure 39. Mode Pin Configuration on DS90UB914Q-Q1 Deserializer

Table 4. DS90UB914Q-Q1 Deserializer MODE Resistor Value

DS90UB914Q-Q1 DESERIALIZER MODE RESISTOR VALUE	
MODE SELECT	**R_{MODE} RESISTOR VALUE**
12-bit low-frequency mode 10 to 50 MHz PCLK 10 to 12 bit DATA + 2 SYNC	0 Ω
12-bit low-frequency mode 15 to 75 MHz PCLK 10 to 12 bit DATA + 2 SYNC	3 kΩ
10-bit mode 20 to 100 MHz PCLK 10 to 10 bit DATA + 2 SYNC	11 kΩ

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10.4.5 Clock-Data Recovery Status Flag (LOCK), Output Enable (OEN) and Output State Select (OSS_SEL)

When PDB is driven HIGH, the CDR PLL of the deserializer begins locking to the serial input and LOCK is TRI-STATE or LOW (depending on the value of the OEN setting). After the DS90UB914Q-Q1 completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the parallel bus and PCLK outputs. The states of the outputs are based on the OEN and OSS_SEL setting (Table 3). See Figure 20.

Table 5. Output States

INPUTS				OUTPUTS			
SERIAI INPUTS	PDB	OEN	OSS	LOCK	PASS	DATA, GPIO, I2S	CLK
X	0	X	X	Z	Z	Z	Z
X	1	0	0	L or H	L	L	L
X	1	0	1	L or H	Z	Z	Z
Static	1	1	0	L	L	L	L/Osc (Register Bit Enable)
Static	1	1	1	H	Previous State	L	L
Active	1	1	0	H	L	L	L
Active	1	1	1	H	Valid	Valid	Valid

10.4.6 Multiple Device Addressing

Some applications require multiple camera devices with the same fixed address to be accessed on the same I^2C bus. The DS90UB91xQ-Q1 provides slave ID matching/aliasing to generate different target slave addresses when connecting more than two identical devices together on the same bus. This allows the slave devices to be independently addressed. Each device connected to the bus is addressable through a unique ID by programming of the SLAVE_ID_MATCH register on deserializer. This will remap the SLAVE_ID_MATCH address to the target SLAVE_ID_INDEX address; up to 8 ID indexes are supported. The ECU Controller must keep track of the list of I^2C peripherals in order to properly address the target device.

See Figure 40 for an example of multiple device addressing.

- ECU is the I^2C master and has an I^2C master interface
- The I^2C interfaces in DES A and DES B are both slave interfaces
- The I^2C protocol is bridged from DES A to SER A and from DES B to SER B
- The I^2C interfaces in SER A and SER B are both master interfaces

If master controller transmits I^2C slave 0xA0, the DES A address 0xC0 will forward the transaction to remote Camera A. If the controller transmits slave address 0xA4, the DES B 0xC2 will recognize that 0xA4 is mapped to 0xA0 and will be transmitted to the remote Camera B. If controller sends command to address 0xA6, the DES B 0xC2 will forward transaction to slave device 0xA2.

The Slave ID index/match is supported only in the camera mode (SER: MODE pin = L; DES: MODE pin = H). For Multiple device addressing in display mode (SER: MODE pin = H; DES: MODE pin = L), use the I^2C pass-through function.

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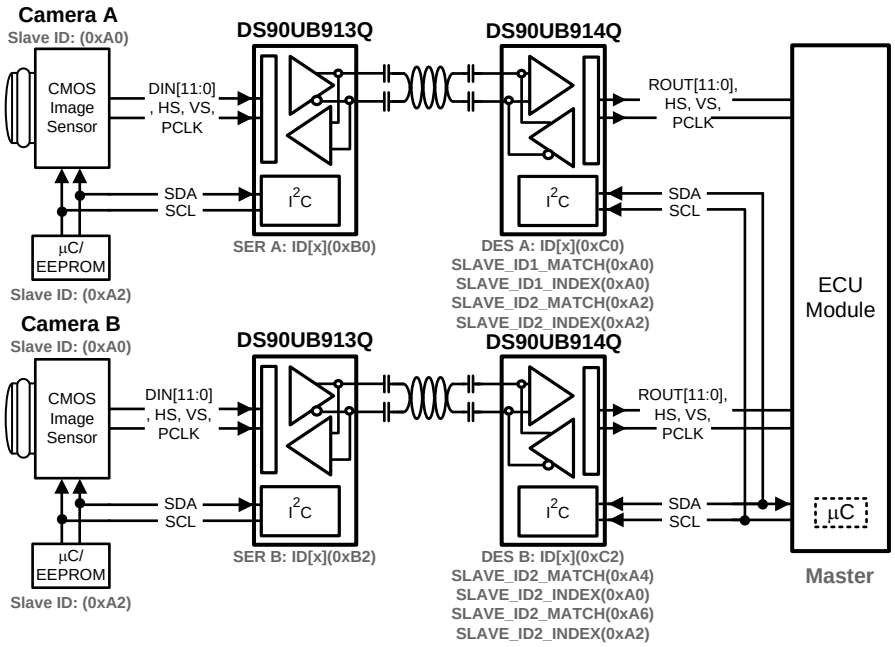

Figure 40. Multiple Device Addressing

10.4.7 Powerdown

The SER has a PDB input pin to ENABLE or Powerdown (SLEEP) the device. The modes can be controlled by the host and is used to disable the Link to save power when the remote device is not operational. In this mode, if the PDB pin is tied High and the SER will enter SLEEP when the PCLK stops. When the PCLK starts again, the SER will then lock to the valid input PCLK and transmit the data to the DES. In SLEEP mode, the high-speed driver outputs are static (High). The DES has a PDB input pin to ENABLE or Powerdown (SLEEP) the device. This pin can be controlled by the system and is used to disable the DES to save power. An auto mode is also available. In this mode, the PDB pin is tied High and the DES will enter SLEEP when the serial stream stops. When the serial stream starts up again, the DES will lock to the input stream and assert the LOCK pin and output valid data. In SLEEP mode, the Data and PCLK outputs are set by the OSS_SEL configuration.

10.4.8 Pixel Clock Edge Select (TRFB / RRFB)

The TRFB/RRFB selects which edge of the Pixel Clock is used. For the SER, this register determines the edge that the data is latched on. If TRFB register is 1, data is latched on the Rising edge of the PCLK. If TRFB register is 0, data is latched on the Falling edge of the PCLK. For the DES, this register determines the edge that the data is strobed on. If RRFB register is 1, data is strobed on the Rising edge of the PCLK. If RRFB register is 0, data is strobed on the falling edge of the PCLK.

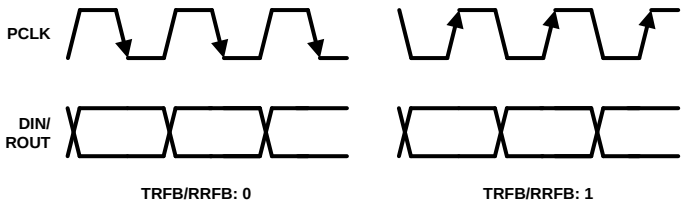

Figure 41. Programmable PCLK Strobe Select

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10.4.9 Power-Up Requirements and PDB Pin

When power is applied, the VDDIO supply needs to reach the expected operating voltage (1.8 V to 3.3 V) before the other supplies (VDDn) begin to ramp. It is required to delay and release the PDB Signal after VDD (VDDn and VDDIO) power supplies have settled to the recommended operating voltage. An external RC network can be connected to the PDB pin to ensure PDB arrives after all the VDD has stabilized.

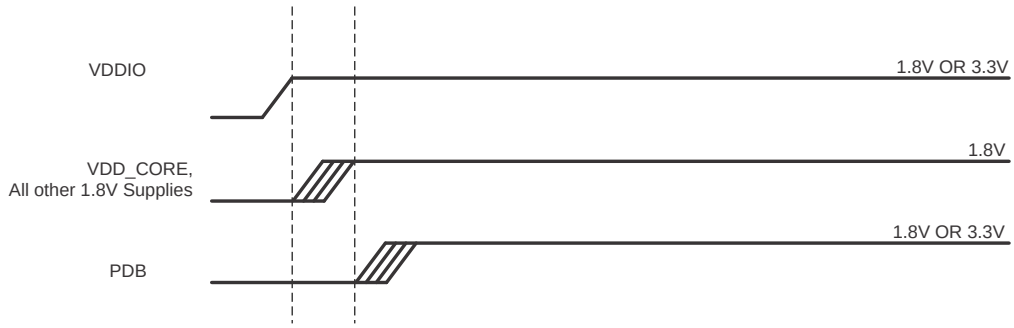

Figure 42. Power-Up Sequencing

10.4.10 Built-In Self Test

An optional AT-Speed, Built-In Self Test (BIST) feature supports the testing of the high-speed serial link and low-speed back channel. This is useful in the prototype stage, equipment production, and in-system test and also for system diagnostics.

10.4.11 BIST Configuration and Status

The chipset can be programmed into BIST mode using either pins or registers. By default BIST configuration is controlled through pins. BIST can be configured through registers using BIST Control register (0x24). Pin based configuration is defined as follows:

- BISTEN : Enable the BIST Process
- GPIO0 and GPIO1 : Defines the BIST clock source (PCLK vs. various frequencies of internal OSC

Table 6. BIST Configuration

DESERIALIZER GPIO[0:1]	OSCILLATOR SOURCE	BIST FREQUENCY (MHZ)
00	External PCLK	PCLK or External Oscillator
01	Internal	50
10	Internal	25
11	Internal	12.5

The BIST mode provides various options for source PCLK. Using external pins, GPIO0 and GPIO1 or using registers, customer can program the BIST mode to use external PCLK or various OSC frequencies. The BIST status can be monitored real time on PASS pin. For every frame with error(s), PASS pin toggles low for half PCLK period. If two consecutive frames have errors, PCLK will toggle twice to allow counting of frames with errors. Once the BIST is done, the PASS pin reflects the pass/fail status of the last BIST run. The status can also be read through I^2C for the number of frames in errors. BIST status on PASS pin remains until it is changed by a new BIST session or a reset. The BIST status on PASS pin is not maintained till RX loses LOCK after BISTEN is deassserted. To evaluate BIST in the external oscillator mode, both external oscillator and PCLK need to be present.

The BIST status on PASS pin is not maintained till RX loses LOCK after BISTEN is deassserted. So for all practical purposes, the BIST status can be monitored from register 0x25, that is, BIST Error Count on the DS90UB914Q-Q1 deserializer. To evaluate BIST in the external oscillator mode, both external oscillator and PCLK need to be present.

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10.4.11.1 Sample BIST Sequence

Step 1. For the DS90UB91xQ-Q1 FPD-Link III chipset, BIST Mode is enabled through the BISTEN pin of DS90UB914Q-Q1 FPD-Link III deserializer. The desired clock source is selected through the GPIO0 and GPIO1 pins as shown in Table 4.

Step 2. The DS90UB913Q-Q1 serializer is woken up through the back channel if it is not already on. The SSO pattern on the data pins is send through the FPD-Link III to the deserializer. Once the serializer and deserializer are in the BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking data stream. If an error in the payload is detected the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3. To stop the BIST mode, the deserializer BISTEN pin is set low. The deserializer stops checking the data. The final test result is not maintained on the PASS pin. To monitor the BIST status, check the BIST Error Count register, 0x25 on the deserializer.

Step 4. The link returns to normal operation after the deserailzer BISTEN pin is low. Figure 44 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission, and so forth), thus they may be introduced by greatly extending the cable length, faulting the interconnect, or by reducing signal condition enhancements (RX equalization).

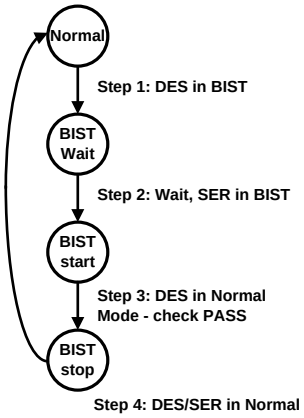

Figure 43. AT-Speed BIST System Flow Diagram

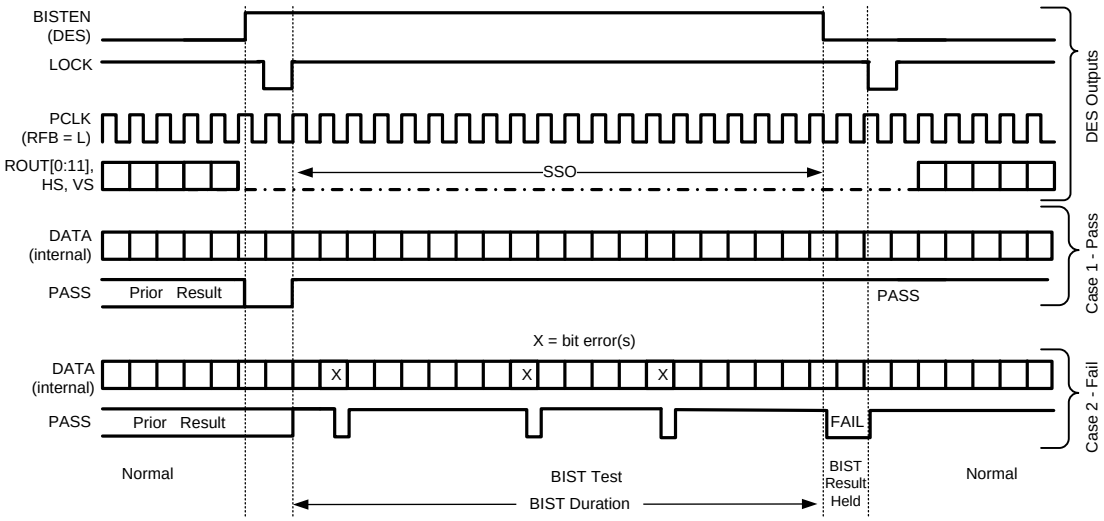

Figure 44. BIST Timing Diagram

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10.5 Register Maps

Table 7. DS90UB913Q-Q1 Control Registers

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x00	I^2C Device ID	7:1	DEVICE ID	RW	0x58'h	7-bit address of serializer; 0x58'h (0101_1000X'b) default
		0	SER ID SEL			0: Device ID is from ID[x] 1: Register I^2C Device ID overrides ID[x]
0x01	Power and Reset	7	RSVD			Reserved
		6	RDS	RW	0	Digital Output Drive Strength 1: High Drive Strength 0: Low Drive Strength
		5	VDDIO Control	RW	1	Auto Voltage Control 1: Enable 0: Disable
		4	VDDIO MODE	RW	1	V_{DDIO}Voltage set 0: 1.8V 1: 3.3V
		3	ANAPWDN	RW	0	This register can be set only through local I^2C access 1: Analog power-down : Powers Down the analog block in the serializer 0: No effect
		2	RSVD	RW	0	Reserved
		1	DIGITAL RESET1	RW	0	1: Resets the digital block except for register values values. Does not affect device I^2C Bus or Device ID. This bit is self-clearing. 0: Normal Operation
		0	DIGITAL RESET0	RW	1	1: Digital Reset, resets the entire digital block including all register values.This bit is self-clearing. 0: Normal Operation.
0x02	**RESERVED**					
0x03	General Configuration	7	RX CRC Checker Enable	RW	1	Back-channel CRC Checker Enable 1:Enabled 0:Disabled
		6	TX Parity Generator Enable	RW	1	Forward channel Parity Generator Enable 1: Enable 0: Disable
		5	CRC Error Reset	RW	0	Clear CRC Error Counters. This bit is NOT self-clearing. 1: Clear Counters 0: Normal Operation
		4	I^2C Remote Write Auto Acknowledge	RW	0	Automatically Acknowledge I^2C Remote Write The mode works when the system is LOCKed. 1: Enable: When enabled, I^2C writes to the deserializer (or any remote I^2C Slave, if I^2C PASS ALL is enabled) are immediately acknowledged without waiting for the deserializer to acknowledge the write. The accesses are then re-mapped to address specified in 0x06. 0: Disable
		3	I^2C Pass All	RW	0	1: Enable Forward Control Channel pass-through of all I^2C accesses to I^2C Slave IDs that do not match the Serializer I^2C Slave ID. **The I^2C accesses are then remapped to address specified in register 0x06.** 0: Enable Forward Control Channel pass-through only of I^2C accesses to I^2C Slave IDs matching either the remote Deserializer Slave ID or the remote Slave ID.
		2	I^2C PASSTHROUGH	RW	1	I^2C Pass-Through Mode 0: Pass-Through Disabled 1: Pass-Through Enabled

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Register Maps (continued)

Table 7. DS90UB913Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x03	General Configuration	1	OV_CLK2PLL	RW	0	1:Enabled : When enabled this registers overrides the clock to PLL mode (External Oscillator mode or Direct PCLK mode) defined through MODE pin and allows selection through register 0x35 in the serializer 0: Disabled : When disabled, Clock to PLL mode (External Oscillator mode or Direct PCLK mode) is defined through MODE pin on the serializer.
		0	TRFB	RW	1	Pixel Clock Edge Select 1: Parallel Interface Data is strobed on the Rising Clock Edge. 0: Parallel Interface Data is strobed on the Falling Clock Edge.
0x04	**RESERVED**					
0x05	Mode Select	7	RSVD	RW	0	Reserved
		6	RSVD	RW	0	Reserved.
		5	MODE_OVERRIDE	RW	0	Allows overriding mode select bits coming from back-channel 1: Overrides MODE select bits 0: Does not override MODE select bits
		4	MODE_UP To DATE	R	0	Indicates that the status of mode select from deserializer is up to date
		3	Pin_MODE_12–bit High Frequency	R	0	1: 12-bit high-frequency mode is selected. 0: 12-bit high-frequency mode is not selected.
		2	Pin_MODE_10–bit mode	R	0	1: 10-bit mode is selected. 0: 10-bit mode is not selected.
		1:0	RSVD			Reserved
0x06	DES ID	7:1	Desializer Device ID	RW	0x00	7-bit Deserializer Device ID configures the I^2C Slave ID of the remote deserializer. A value of 0 in this field disables I^2C access to the remote deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel.
		0	Freeze Device ID	RW	0	1: Prevents auto-loading of the Deserializer Device ID by the bidirectional control channel. The ID will be frozen at the value written. 0: Update
0x07	DESAlias	7:1	Deserializer ALIAS ID	RW	0	7-bit Remote Deserializer Device Alias ID Configures the decoder for detecting transactions designated for an I^2C deserializer device. The transaction will be remapped to the address specified in the DES ID register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved
0x08	SlaveID	7:1	SLAVE ID	RW	0x00	7-bit Remote Slave Device ID Configures the physical I^2C address of the remote I^2C Slave device attached to the remote deserializer. If an I^2C transaction is addressed to the Slave Alias ID, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the deserializer. A value of 0 in this field disables access to the remote I^2C slave.
		0	RSVD			Reserved

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Register Maps (continued)

Table 7. DS90UB913Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x09	SlaveAlias	7:1	SLAVE ALIAS ID	RW	0x00	7-bit Remote Slave Device Alias ID Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote deserializer. The transaction will be remapped to the address specified in the Slave ID register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved
0x0A	CRC Errors	7:0	CRC Error Byte 0	R	0	Number of back-channel CRC errors during normal operation. Least Significant byte
0x0B	CRC Errors	7:0	CRC Error Byte 1	R	0	Number of back-channel CRC errors during normal operation. Most Significant byte
0x0C	General Status	7:5	Rev-ID	R	0	Revision ID 0x00: Production
		4	RX Lock Detect	R	0	1: RX LOCKED 0: RX not LOCKED
		3	BIST CRC Error Status	R	0	1: CRC errors in BIST mode 0: No CRC errors in BIST mode
		2	PCLK Detect	R	0	1: Valid PCLK detected 0: Valid PCLK not detected
		1	DES Error	R	0	1: CRC error is detected during communication with deserializer. This bit is cleared upon loss of link or assertion of CRC ERROR RESET in register 0x04. 0: No effect
		0	LINK Detect	R	0	1: Cable link detected 0: Cable link not detected This includes any of the following faults — Cable Open — + and - shorted — Short to GND — Short to battery
0x0D	GPO[0] and GPO[1] Configuration	7	GPO1 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPO1 Remote Enable	RW	1	Remote GPIO Control 1: Enable GPIO control from remote deserializer. The GPIO pin needs to be an output, and the value is received from the remote deserializer. 0: Disable GPIO control from remote deserializer.
		5	GPO1 Direction	RW	0	1: Input 0: Output
		4	GPO0 Enable	RW	1	1: GPIO enable 0: Tri-state
		3	GPO0 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPO0 Remote Enable	RW	1	Remote GPIO Control 1: Enable GPIO control from remote deserializer. The GPIO pin needs to be an output, and the value is received from the remote deserializer. 0: Disable GPIO control from remote deserializer.
		1	GPO0 Direction	RW	0	1: Input 0: Output
		0	GPO0 Enable	RW	1	1: GPIO enable 0: Tri-state

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Register Maps (continued)

Table 7. DS90UB913Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x0E	GPO[2] and GPO[3] Configuration	7	GPO3 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		6	GPO3 Remote Enable	RW	0	Remote GPIO Control 1: Enable GPIO control from remote deserializer. The GPIO pin needs to be an output, and the value is received from the remote deserializer. 0: Disable GPIO control from remote deserializer.
		5	GPO3 Direction	RW	1	1: Input 0: Output
		4	GPO3 Enable	RW	1	1: GPIO enable 0: Tri-state
		3	GPO2 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
		2	GPO2 Remote Enable	RW	1	Remote GPIO Control 1: Enable GPIO control from remote deserializer. The GPIO pin needs to be an output, and the value is received from the remote deserializer. 0: Disable GPIO control from remote deserializer.
		1	GPO2 Direction	RW	0	1: Input 0: Output
		0	GPO2 Enable	RW	1	1: GPIO enable 0: Tri-state
0x0F	I^2C Master Config	7:5	RSVD			Reserved
		4:3	SDA Output Delay	RW	00	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50 ns. Nominal output delay values for SCL to SDA are: 00 : 350 ns 01: 400 ns 10: 450 ns 11: 500 ns
		2	Local Write Disable	RW	0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the serializer registers from an I^2C master attached to the deserializer. Setting this bit does not affect remote access to I^2C slaves at the serializer.
		1	I^2C Bus Timer Speed up	RW	0	Speed up I^2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
		0	I^2C Bus Timer Disable	RW	0	1. Disable I^2C Bus Watchdog Timer When the I^2C Watchdog Timer may be used to detect when the I^2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I^2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL 0: No effect

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Register Maps (continued)

Table 7. DS90UB913Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x10	I^2C Control	7	RSVD			Reserved
		6:4	SDA Hold Time	RW	0x1	Internal SDA Hold Time. This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 ns.
		3:0	I^2C Filter Depth	RW	0x7	I^2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 10 ns.
0x11	SCL High Time	7:0	SCL High Time	RW	0x82	I^2C Master SCL High Time This field configures the high pulse width of the SCL output when the serializer is the Master on the local I^2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4µs + 1µs of rise time for cases where rise time is very fast) SCL high time with the internal oscillator clock running at 26MHz rather than the nominal 20 MHz.
0x12	SCL LOW Time	7:0	SCL Low Time	RW	0x82	I^2C SCL Low Time This field configures the low pulse width of the SCL output when the serializer is the Master on the local I^2C bus. This value is also used as the SDA setup time by the I^2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4.7 µs + 0.3 µs of fall time for cases where fall time is very fast) SCL low time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.
0x13	General-Purpose Control	7:0	GPCR[7:0]	RW	0	1: High 0: Low
0x14	BIST Control	7:3	RSVD			Reserved
		2:1	Clock Source	RW	0x0	Allows choosing different OSC clock frequencies for forward channel frame. OSC Clock Frequency in Functional Mode when OSC mode is selected or when the selected clock source is not present, for example, missing PCLK/ External Oscillator. See Table 9 for oscillator clock frequencies when PCLK/ External Clock is missing.
		0	BIST Enable	RW	0	BIST Control: 1: Enable BIST mode 0: Disable BIST mode
0x15 - 0x1D	**RESERVED**					
0x1E	BCC Watchdog Control	7:1	BCC Watchdog Timer	RW	0x7F	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2ms. This field should not be set to 0.
		0	BCC Watchdog Timer Disable	RW	0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation
0x1F-0x29	**RESERVED**					
0x2A	CRC Errors	7:0	BIST Mode CRC Errors Count	R	0	Number of CRC Errors in the back channel when in BIST mode

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Register Maps (continued)

Table 7. DS90UB913Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x2B - 0x34	RESERVED					
0x35	PLL Clock Overwrite	7:4	RSVD			Reserved
		3	PIN_LOCK to External Oscillator	RW	0	Status of mode select pin 1: Indicates External Oscillator mode is selected by mode-resistor 0: External Oscillator mode is not selected by mode-resistor
		2	PIN_LOCK to Oscillator	RW	0	Status of mode select pin 1: Indicates PCLK mode is selected by mode-resistor 0: PCLK mode not selected by mode-resistor
		1	LOCK to External Oscillator	RW	0	Affects only when 0x03[1]=1 (OV_CLK2PLL) and 0x35[0]=0. 1: Routes GPO3 directly to PLL 0: Allows PLL to lock to PCLK"
		0	RSVD			Reserved

Table 8. DS90UB914Q-Q1 Control Registers

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x00	I^2C Device ID	7:1	DEVICE ID	RW	0x60'h	7-bit address of deserializer; 0x60h
		0	Deserializer ID Select	RW	0	0: Deserializer Device ID is set using address coming from CAD 1: Register I^2C Device ID overrides ID[x]
0x01	Reset	7:6	RSVD			Reserved
		5	ANAPWDN	RW	0	This register can be set only through local I^2C access 1: Analog power-down : Powers down the analog block in the serializer 0: No effect
		4:2	RSVD			Reserved
		1	Digital Reset 1	RW	0	Digital Reset Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: No effect
		0	Digital Reset 0	RW	0	Digital Reset Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: No effect

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Table 8. DS90UB914Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x02	General Configuration 0	7	RSVD			Reserved
		6	RSVD			Reserved
		5	Auto-Clock	RW	0	1: Output PCLK or OSC clock when not LOCKED 0: Only PCLK
		4	SSCG LFMODE	RW	0	1: Selects 8x mode for 10-18 MHz frequency range in SSCG 0: SSCG running at 4X mode
		3:0	SSCG	RW	0	SSCG Select 0000: Normal Operation, SSCG OFF 0001: fmod (kHz) PCLK/2168, fdev ±0.50% 0010: fmod (kHz) PCLK/2168, fdev ±1.00% 0011: fmod (kHz) PCLK/2168, fdev ±1.50% 0100: fmod (kHz) PCLK/2168, fdev ±2.00% 0101: fmod (kHz) PCLK/1300, fdev ±0.50% 0110: fmod (kHz) PCLK/1300, fdev ±1.00% 0111: fmod (kHz) PCLK/1300, fdev ±1.50% 1000: fmod (kHz) PCLK/1300, fdev ±2.00% 1001: fmod (kHz) PCLK/868, fdev ±0.50% 1010: fmod (kHz) PCLK/868, fdev ±1.00% 1011: fmod (kHz) PCLK/868, fdev ±1.50% 1100: fmod (kHz) PCLK/868, fdev ±2.00% 1101: fmod (kHz) PCLK/650, fdev ±0.50% 1110: fmod (kHz) PCLK/650, fdev ±1.00% 1111: fmod (kHz) PCLK/650, fdev ±1.50% Note: **This register should be changed only after disabling SSCG.**
0x03	General Configuration 1	7	RX Parity Checker Enable	RW	1	Forward-Channel Parity Checker Enable 1: Enable 0: Disable
		6	TX CRC Checker Enable	RW	1	Back-Channel CRC Generator Enable 1: Enable 0: Disable
		5	V_{DDIO} Control	RW	1	Auto voltage control 1: Enable (auto-detect mode) 0: Disable
		4	V_{DDIO} Mode	RW	0	VDDIO voltage set 1: 3.3 V 0: 1.8 V
0x03	General Configuration 1	3	I^2C Passthrough	RW	1	I^2C Pass-Through Mode 1: Pass-Through Enabled 0: Pass-Through Disabled
		2	AUTO ACK	RW	0	Automatically Acknowledge I^2C Remote Write When enabled, I^2C writes to the deserializer (or any remote I^2C Slave, if I^2C PASS ALL is enabled) are immediately acknowledged without waiting for the deserializer to acknowledge the write. The accesses are then remapped to address specified in 0x06. This allows I^2C bus without LOCK. 1: Enable 0: Disable
		1	Parity Error Reset	RW	0	Parity Error Reset, This bit is self-clearing. 1: Parity Error Reset 0: No effect
		0	RRFB	RW	1	Pixel Clock Edge Select 1: Parallel Interface Data is strobed on the Rising Clock Edge. 0: Parallel Interface Data is strobed on the Falling Clock Edge.

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Table 8. DS90UB914Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x04	EQ Feature Control 1	7:0	EQ level - when AEQ bypass is enabled EQ setting is provided by this register	RW	0x00	Equalization gain 0x00 = ~0.0 dB 0x01 = ~4.5 dB 0x03 = ~6.5 dB 0x07 = ~7.5 dB 0x0F = ~8.0 dB 0x1F = ~11.0 dB 0x3F = ~12.5 dB
0x05	**RESERVED**					
0x06	SER ID	7:1	Remote ID	RW	0x0C	Remote Serializer ID
		0	Freeze Device ID	RW	0	Freeze Serializer Device ID Prevent auto-loading of the serializer Device ID from the Forward Channel. The ID will be frozen at the value written.
0x07	SER Alias	7:1	Serializer Alias ID	RW	0x00	7-bit Remote Serializer Device Alias ID Configures the decoder for detecting transactions designated for an I^2C deserializer device. The transaction will be remapped to the address specified in the SER ID register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved
0x08	Slave ID[0]	7:1	Slave ID0	RW	0	7-bit Remote Slave Device ID 0 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote serializer. If an I^2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the serializer.
		0	RSVD			Reserved
0x09	Slave ID[1]	7:1	Slave ID1	RW	0	7-bit Remote Slave Device ID 1 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote serializer. If an I^2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the serializer.
		0	RSVD			Reserved
0x0A	Slave ID[2]	7:1	Slave ID2	RW	0x00	7-bit Remote Slave Device ID 2 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote serializer. If an I^2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the serializer.
		0	RSVD			Reserved
0x0B	Slave ID[3]	7:1	Slave ID3	RW	0	7-bit Remote Slave Device ID 3 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote serializer. If an I^2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the serializer.
		0	RSVD			Reserved

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Table 8. DS90UB914Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x0C	Slave ID[4]	7:1	Slave ID4	RW	0	7-bit Remote Slave Device ID 4 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote serializer. If an I^2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the serializer.
		0	RSVD			Reserved
0x0D	Slave ID[5]	7:1	Slave ID5	RW	0x00	7-bit Remote Slave Device ID 5 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote serializer. If an I^2C transaction is addressed to the Slave Alias ID5 , the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the serializer.
		0	RSVD			Reserved
0x0E	Slave ID[6]	7:1	Slave ID6	RW	0	7-bit Remote Slave Device ID 6 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote serializer. If an I^2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the serializer.
		0	RSVD			Reserved
0x0F	Slave ID[7]	7:1	Slave ID7	RW	0x00	7-bit Remote Slave Device ID 7 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote serializer. If an I^2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the serializer.
		0	RSVD			Reserved
0x10	Slave Alias[0]	7:1	Slave Alias ID0	RW	0x00	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved
0x11	Slave Alias[1]	7:1	Slave Alias ID1	RW	0x00	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote serializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved

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Table 8. DS90UB914Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x12	Slave Alias[2]	7:1	Slave Alias ID2	RW	0x00	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote serializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved
0x13	Slave Alias[3]	7:1	Slave Alias ID3	RW	0x00	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote serializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved
0x14	Slave Alias[4]	7:1	Slave Alias ID4	RW	0x00	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote serializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved
0x15	Slave Alias[5]	7:1	Slave Alias ID5	RW	0x00	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote serializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved
0x16	Slave Alias[6]	7:1	Slave Alias ID6	RW	0x00	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote serializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved
0x17	Slave Alias[7]	7:1	Slave Alias ID7	RW	0x00	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote serializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I^2C Slave.
		0	RSVD			Reserved
0x18	Parity Errors Threshold	7:0	Parity Error Threshold Byte 0	RW	0	Parity errors threshold on the Forward channel during normal information. This sets the maximum number of parity errors that can be counted using register 0x1A. Least significant Byte.

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Table 8. DS90UB914Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x19	Parity Errors Threshold	7:0	Parity Error Threshold Byte 1	RW	0	Parity errors threshold on the Forward channel during normal operation. This sets the maximum number of parity errors that can be counted using register 0x1B. Most significant Byte
0x1A	Parity Errors	7:0	Parity Error Byte 0	RW	0	Number of parity errors in the Forward channel during normal operation. Least significant Byte
0x1B	Parity Errors	7:0	Parity Error Byte 1	RW	0	Number of parity errors in the Forward channel during normal operation Most significant Byte
0x1C	General Status	7:4	Rev-ID	R	0	Revision ID 0x0000: Production
		3	RSVD			Reserved
		2	Parity Error	R	0	Parity Error detected 1: Parity Errors detected 0: No Parity Errors
		1	Signal Detect	R	0	1: Serial input detected 0: Serial input not detected
		0	Lock	R	0	Deserializer CDR, PLL's clock to recovered clock frequency 1: Deserializer locked to recovered clock 0: Deserializer not locked
0x1D	GPIO[1] and GPIO[0] Config	7	GPIO1 Output Vaue	RW	0	Local GPIO Output Value This value is the output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		6	RSVD			Reserved
		5	GPIO1 Direction	RW	1	Local GPIO Direction 1: Input 0: Output
		4	GPIO1 Enable	RW	1	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
		3	GPIO0 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
0x1D	GPIO[1] and GPIO[0] Config	2	RSVD			Reserved
		1	GPIO0 Direction	RW	1	Local GPIO Direction 1: Input 0: Output
		0	GPIO0 Enable	RW	1	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation

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Table 8. DS90UB914Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x1E	GPIO[3] and GPIO[2] Config	7	GPIO3 Output Vaue	RW	0	Local GPIO Output Value This value is the output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		6	RSVD			Reserved
		5	GPIO3 Direction	RW	1	Local GPIO Direction 1: Input 0: Output
		4	GPIO3 Enable	RW	1	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
		3	GPIO2 Output Value	RW	0	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output.
		2	RSVD			Reserved
		1	GPIO2 Direction	RW	1	Local GPIO Direction 1: Input 0: Output
		0	GPIO2 Enable	RW	1	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
0x1F	Mode and OSS Select	7	OEN_OSS Override	RW	0	Allows overriding OEN and OSS select coming from Pins 1: Overrides OEN/OSS_SEL selected by pins 0: Does NOT override OEN/OSS_SEL select by pins
		6	OEN Select	RW	0	OEN configuration from register
		5	OSS Select	R	0	OSS_SEL configuration from register
		4	MODE_OVERRIDE	RW	0	Allows overriding mode select bits coming from back-channel 1: Overrides MODE select bits 0: Does not override MODE select bits
		3	PIN_MODE_12–bit HF mode	R	0	Status of mode select pin
		2	PIN_MODE_10-bit mode	R	0	Status of mode select pin
		1	MODE_12–bit High Frequency	RW	0	Selects 12-bit high-frequency mode. This bit is automatically updated by the mode settings from RX unless MODE_OVERRIDE is SET 1: 12-bit high-frequency mode is selected. 0: 12-bit high-frequency mode is not selected.
		0	MODE_10–bit mode	RW	0	Selects 10-bit mode. This bit is automatically updated by the mode settings from RX unless MODE_OVERRIDE is SET 1: Enables 10-bit mode. 0: Disables 10-bit mode.
0x20	BCC Watchdog Control	7:1	BCC Watchdog timer	RW	0	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2ms. This field should not be set to 0.
		0	BCC Watchdog Timer Disable	RW	0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

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Table 8. DS90UB914Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x21	I^{2}C Control 1	7	I^{2}C pass-through all	RW	0	I^{2}C Pass-Through All Transactions 0: Disabled 1: Enabled
		6:4	I^{2}C SDA Hold	RW	0	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50ns.
		3:0	I^{2}C Filter Depth	RW	0	I^{2}C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 10ns.
0x22	I^{2}C Control 2	7	Forward Channel Sequence Error	R	0	Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in forward control channel. 1: If this bit is set, an error may have occurred in the control channel operation 0: No forward channel errors have been detected on the control channel
		6	Clear Sequence Error	RW	0	Clears the Sequence Error Detect bit
		5	RSVD			Reserved
		4:3	SDA Output Delay	RW	0	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50 ns. Nominal output delay values for SCL to SDA are: 00 : 350ns 01: 400ns 10: 450ns 11: 500ns
		2	Local Write Disable	RW	0	Disable Remote Writes to local registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the deserializer registers from an I^{2}C master attached to the serializer. Setting this bit does not affect remote access to I^{2}C slaves at the deserializer.
		1	I^{2}C Bus Timer Speed up	RW	0	Speed up I^{2}C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 µs 0: Watchdog Timer expires after approximately 1 s.
		0	I^{2}C Bus Timer Disable	RW	0	Disable I^{2}C Bus Watchdog Timer When the I^{2}C Watchdog Timer may be used to detect when the I^{2}C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I^{2}C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL
0x23	General-Purpose Control	7:0	GPCR	RW	0	Scratch Register
0x24	BIST Control	7:4	RSVD			Reserved
		3	BIST Pin Configuration	RW	1	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through register bit "reg_24[0]"
		2:1	BIST Clock Source	RW	00	BIST Clock Source See Table 10
		0	BIST Enable	RW	0	BIST Control 1: Enabled 0: Disabled

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Table 8. DS90UB914Q-Q1 Control Registers (continued)

ADDR (HEX)	NAME	BITS	FIELD	R/W	DEFAULT	DESCRIPTION
0x25	Parity Error Count	7:0	BIST Error Count	R	0	Number of Forward channel Parity errors in the BIST mode.
0x26 - 0x3B	**RESERVED**					
0x3C	Oscillator output divider select	7:2	RSVD			Reserved
		1:0	OSC OUT DIVIDER SEL	RW	0	Selects the divider for the OSC clock out on PCLK when system is not locked and selected by OEN/OSSSEL 0x02[5] 00: 50M (± 30%) 01: 25M (± 30%) 1X: 12.5M (± 30%)
0x3D - 0x3E	**RESERVED**					
0x3F	CML Output Enable	7:5	RSVD			Reserved
		4	CML OUT Enable	RW	1	0: CML Loop-through Driver is powered up 1: CML Loop-through Driver is powered down.
		3:0	RSVD			Reserved
0x40	SCL High Time	7:0	SCL High Time	RW	0x82	I^2C Master SCL High Time This field configures the high pulse width of the SCL output when the deserializer is the Master on the local I^2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4µs + 0.3µs of rise time for cases where rise time is very fast) SCL high time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
0x41	SCL Low Time	7:0	SCL Low Time	RW	0x82	I^2C SCL Low Time This field configures the low pulse width of the SCL output when the deserializer is the Master on the local I^2C bus. This value is also used as the SDA setup time by the I^2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum (4.7µs + 0.3µs of fall time for cases where fall time is very fast) SCL low time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
0x42	CRC Force Error	7:2	RSVD			Reserved
		1	Force Back Channel Error	RW	0	1: This bit introduces multiple errors into Back channel frame. 0: No effect
		0	Force One Back Channel Error	RW	0	1: This bit introduces ONLY one error into Back channel frame. Self clearing bit 0: No effect
0x43 - 0x4C	**RESERVED**					
0x4D	AEQ Test Mode Select	7	RSVD			Reserved
		6	AEQ Bypass	RW	0	Bypass AEQ and use set manual EQ value using register 0x04
		5:0	RSVD			Reserved
0x4E	EQ Value	7:0	AEQ / Manual Eq Readback	R	0	Read back the adaptive and manual Equalization value

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Table 9. Clock Sources for Forward Channel Frame on the Serializer During Normal Operation

DS90UB913Q REG 0x14 [2:1]	10-BIT MODE	12-BIT HIGH-FREQUENCY MODE	12-BIT LOW-FREQUENCY MODE
00	50 MHz	37.5 MHz	25 MHz
01	100 MHz	75 MHz	50 MHz
10	50 MHz	37.5 MHz	25 MHz
11	25MHz	18.75 MHz	12.5 MHz

Table 10. BIST Clock Sources

DS90UB914Q REG 0x24 [2:1]	10-BIT MODE	12-BIT HIGH-FREQUENCY MODE	12-BIT LOW-FREQUENCY MODE
00	PCLK	PCLK	PCLK
01	100 MHz	75 MHz	50 MHz
10	50 MHz	37.5 MHz	25 MHz
11	25MHz	18.75 MHz	12.5 MHz

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11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Applications Information

The serializer and deserializer support only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as illustrated in Figure 45.

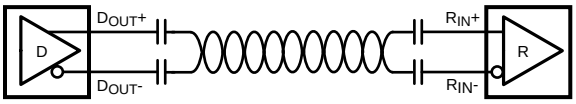

Figure 45. AC-Coupled Connection

For high-speed FPD-Link III transmissions, the smallest available package should be used for the AC-coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The I/Os require a 100-nF AC-coupling capacitors to the line.

11.2 Typical Application

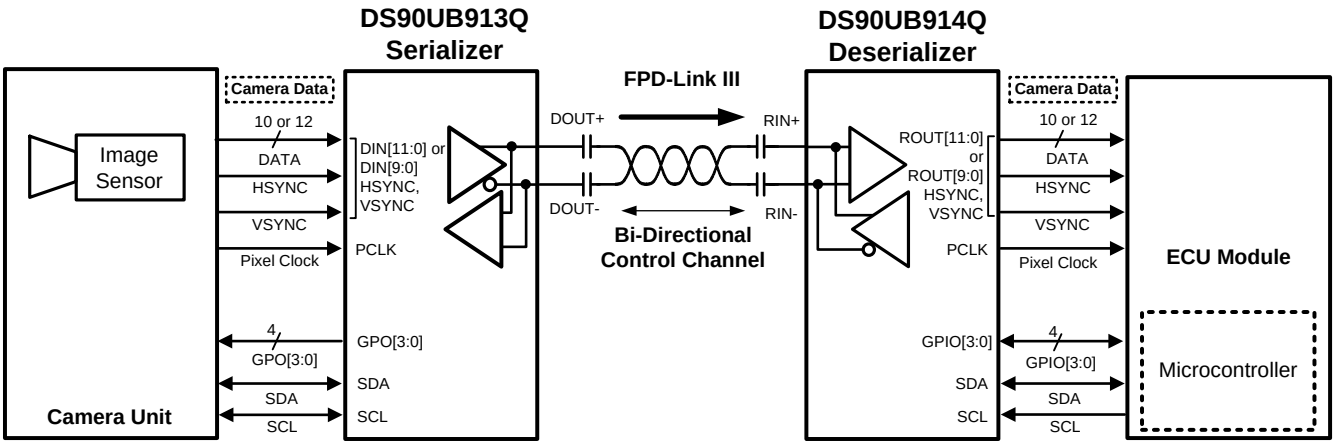

Figure 46. Application Block Diagram

11.2.1 Design Requirements

11.2.1.1 Transmission Media

The DS90UB91xQ-Q1 chipset is intended to be used in a point-to-point configuration through a shielded twisted pair cable. The serializer and deserializer provide internal termination to minimize impedance discontinuities. The interconnect (cable and connectors) should have a differential impedance of 100 Ω. The maximum length of cable that can be used is dependent on the quality of the cable (gauge, impedance), connector, board (discontinuities, power plane), the electrical environment (for example, power stability, ground noise, input clock jitter, PCLK frequency, and so forth). The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. A differential probe should be used to measure across the termination resistor at the CMLOUTP/N pins. Figure 20 illustrates the minimum eye width and eye height that is necessary for bit error free operation.

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Typical Application (continued)

11.2.1.2 Adaptive Equalizer – Loss Compensation

The adaptive equalizer is designed to compensate for signal degradation due to the differential insertion loss of the interconnect components. There are limits to the amount of loss that can be compensated – these limits are defined by the gain curve of the equalizer. In addition, there is an inherent tolerance for loss defined by the delta between the minimum VDO of the serializer and the input threshold (Vswing) of the deserializer. In order to determine the maximum cable reach, other factors that affect signal integrity such as jitter, skew, ISI, crosstalk, and so forth, need to be taken into consideration. Figure 49 illustrates the maximum allowable interconnect loss with the adaptive equalizer at its maximum gain setting (914 equalizer gain).

11.2.2 Detailed Design Procedure

Figure 47 shows the typical connection of a DS90UB913Q-Q1 serializer.

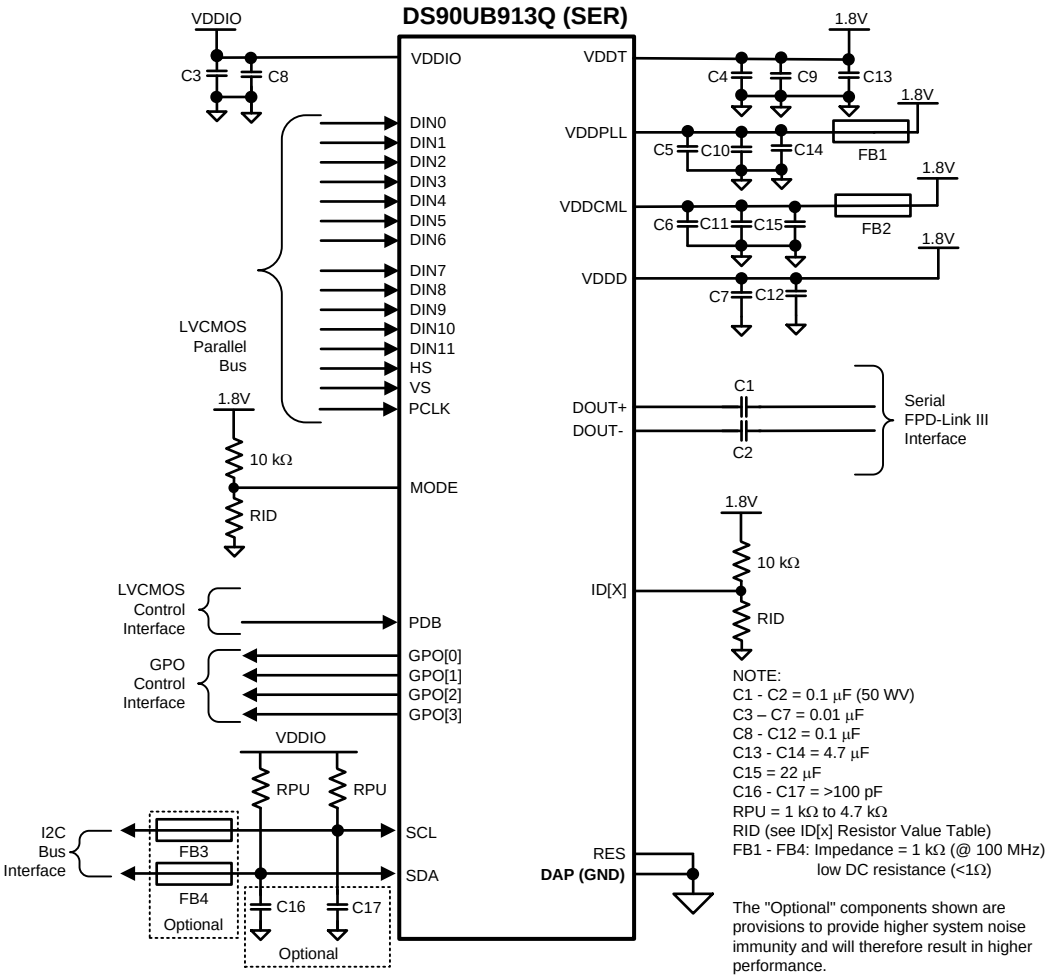

Figure 47. DS90UB913Q-Q1 Typical Connection Diagram — Pin Control

Typical Application (continued)

Figure 48 shows a typical connection of the DS90UB914Q-Q1 deserializer.

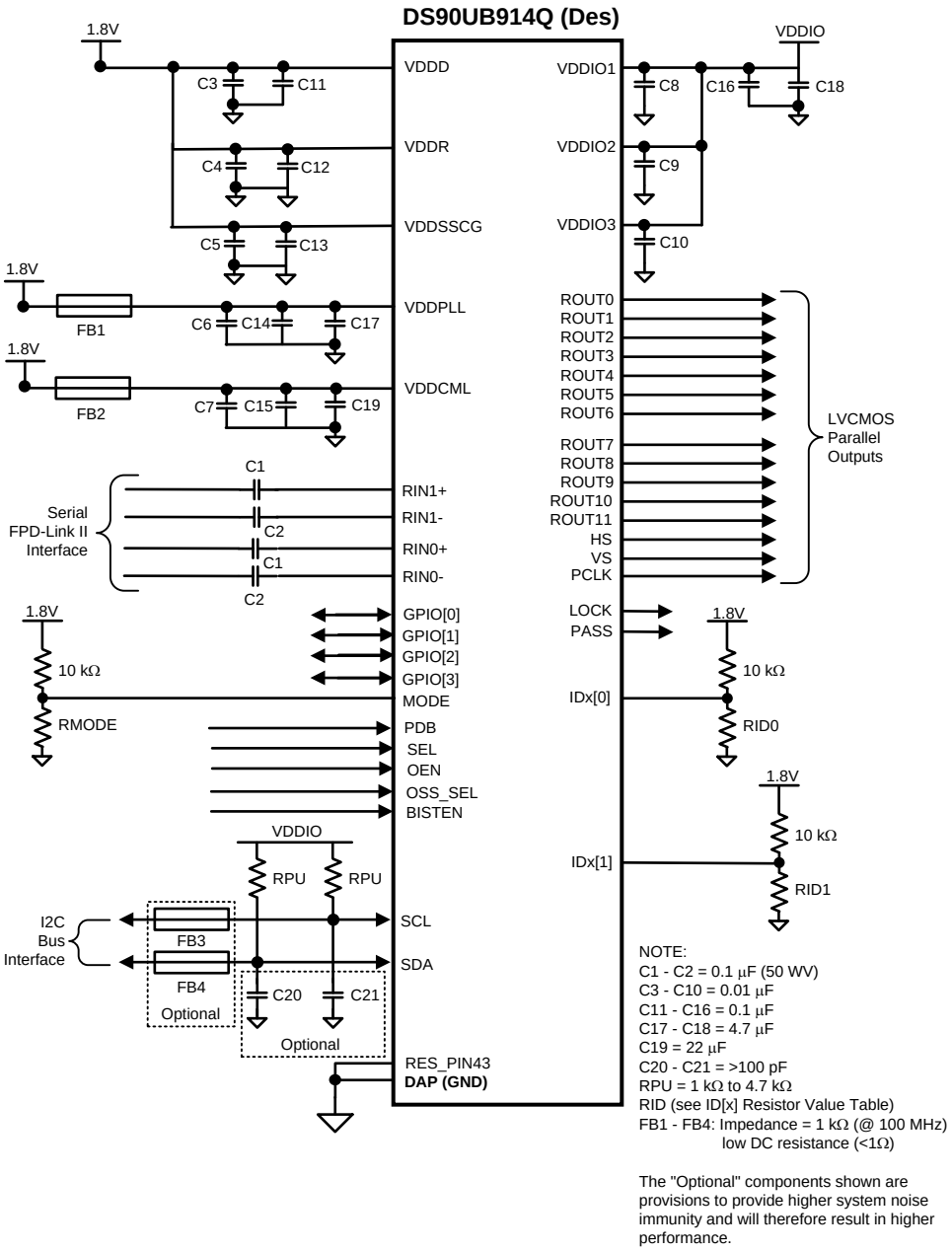

Figure 48. DS90UB914Q-Q1 Typical Connection Diagram — Pin Control

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Typical Application (continued)

11.2.3 Application Curve

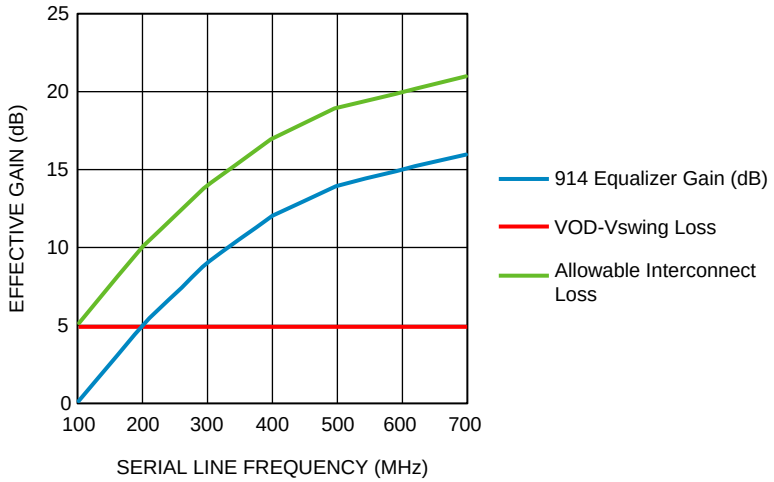

Figure 49. Adaptive Equalizer – Interconnect Loss Compensation

12 Power Supply Recommendations

This device is designed to operate from an input core voltage supply of 1.8 V. Some devices provide separate power and ground terminals for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Terminal description tables typically provide guidance on which circuit blocks are connected to which power terminal pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

13 Layout

13.1 Layout Guidelines

Printed-circuit-board layout and stack-up for the serializer and deserializer devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2-µF to 10-µF range. Voltage rating of the tantalum capacitors should be at least 5× the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50-µF to 100-µF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with a via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100 Ω are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in Texas Instruments' Application Note: AN-1187 (SNOA401).

See AN-1108 (SNLA008) and AN-905 (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S, 2S, and 3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

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Layout Guidelines (continued)

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instrument web site at: www.ti.com/lvds

13.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in Figure 50.

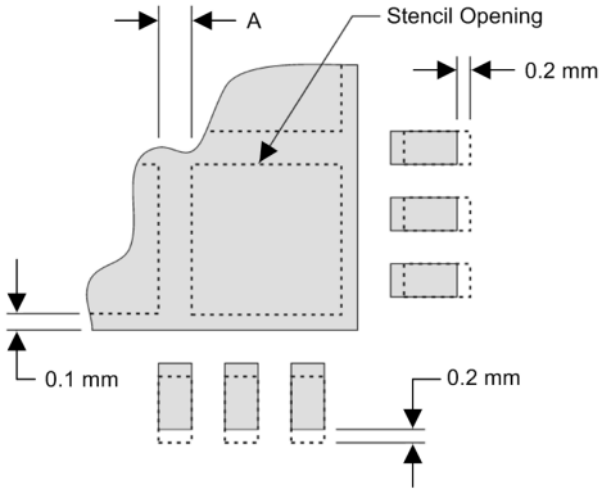

Figure 50. No Pullback WQFN, Single Row Reference Diagram

Figure 50 and Figure 51 PCB layout examples are derived from the layout design of the *DS90UB913Q-Q1 Serializer and DS90UB914Q-Q1 Deserializer Evaluation Kit* (SNLU110). These graphics and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in the serializer and deserializer.

Table 11. No Pullback WQFN Stencil Aperture Summary for DS90UB913Q-Q1 and DS90UB914Q-Q1

DEVICE	PIN COUNT	MKT DWG	PCB I/O PAD SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE (mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER OF DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS90UB913Q-Q1	32	RTV	0.25 x 0.6	0.5	3.1 x 3.1	0.25 x 0.7	1.4 x 1.4	4	0.2
DS90UB914Q-Q1	48	RHS	0.25 x 0.6	0.5	5.1 x 5.1	0.25 x 0.7	1.1 x 1.1	16	0.2

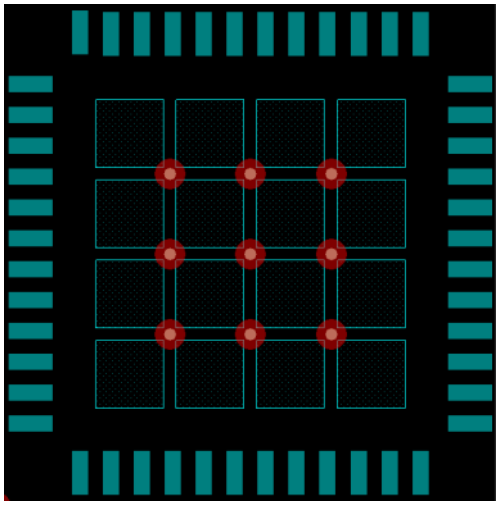

Figure 51. 48-Pin WQFN Stencil Example of Via and Opening Placement

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14 器件和文档支持

14.1 文档支持

14.1.1 相关文档

相关文档如下：

- *《焊接相关的最大绝对额定值》*，SNOA549
- *AN-1187《无引线框架封装 (LLP)》*，SNOA401
- *AN-1108《通道链路 PCB 和互连设计指南》*，SNLA008
- *《传输线路 RAPIDESIGNER 操作和应用指南》*，SNLA035
- *《DS90UB913Q-Q1 串行器和 DS90UB914Q-Q1 解串器评估套件》*，SNLU110

14.2 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **12.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
DS90UB913Q-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
DS90UB914Q-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

14.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

14.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB913QSQ/NOPB	ACTIVE	WQFN	RTV	32	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB913SQ	Samples
DS90UB913QSQE/NOPB	ACTIVE	WQFN	RTV	32	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB913SQ	Samples
DS90UB913QSQX/NOPB	ACTIVE	WQFN	RTV	32	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB913SQ	Samples
DS90UB914QSQ/NOPB	ACTIVE	WQFN	RHS	48	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB914QSQ	Samples
DS90UB914QSQE/NOPB	ACTIVE	WQFN	RHS	48	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB914QSQ	Samples
DS90UB914QSQX/NOPB	ACTIVE	WQFN	RHS	48	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB914QSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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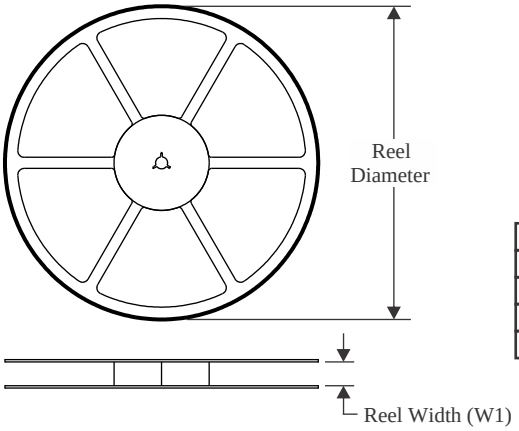
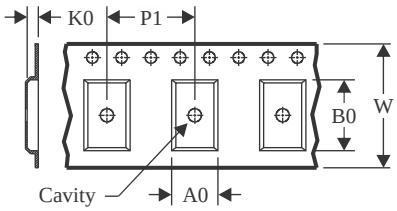
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

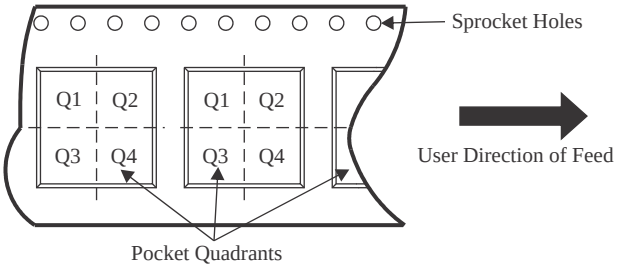


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

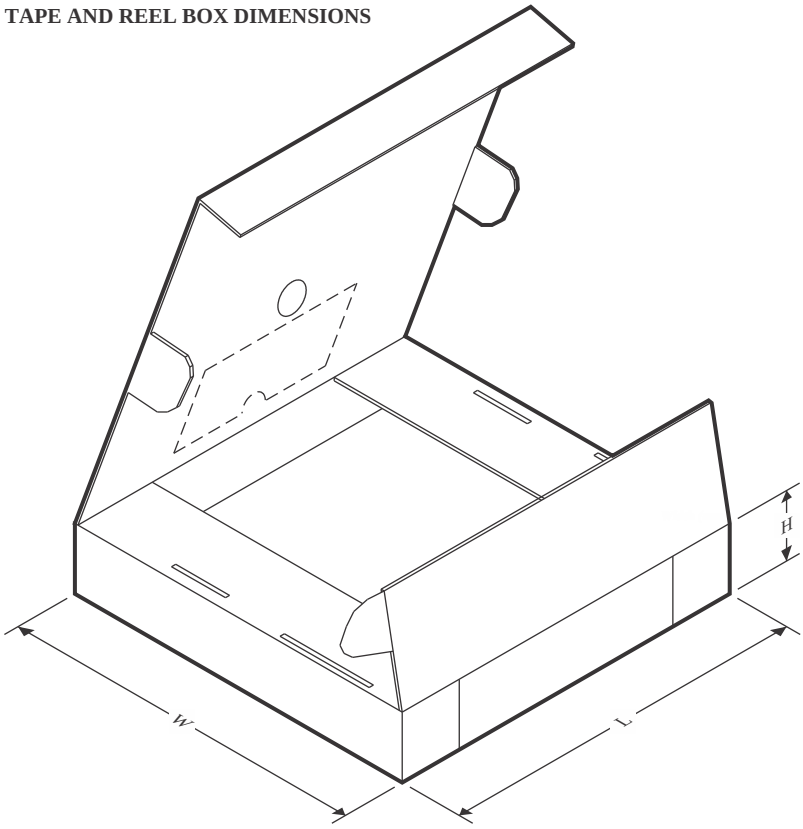
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

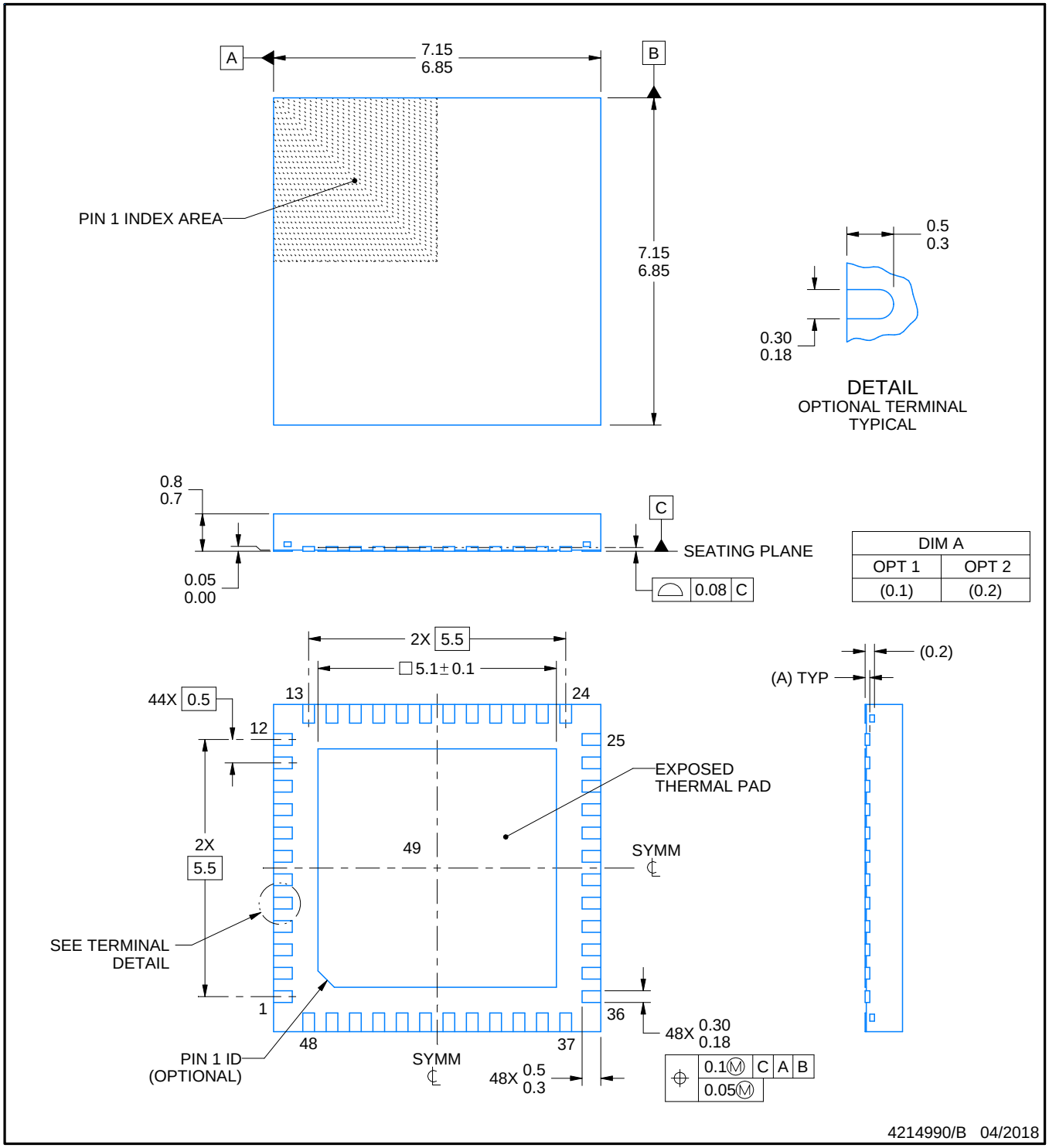
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB913QSQ/NOPB	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS90UB913QSQE/NOPB	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS90UB913QSQX/NOPB	WQFN	RTV	32	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS90UB914QSQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UB914QSQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UB914QSQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



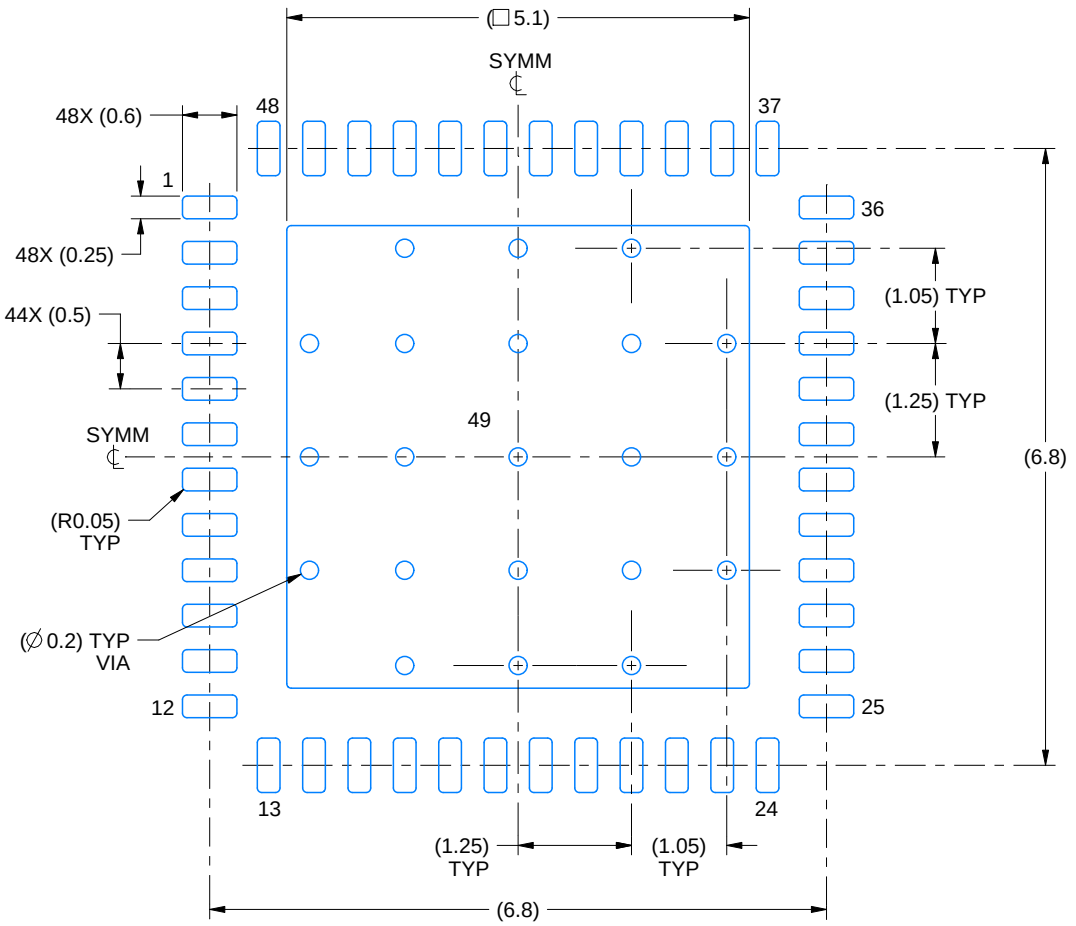
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB913QSQ/NOPB	WQFN	RTV	32	1000	208.0	191.0	35.0
DS90UB913QSQE/NOPB	WQFN	RTV	32	250	208.0	191.0	35.0
DS90UB913QSQX/NOPB	WQFN	RTV	32	4500	356.0	356.0	36.0
DS90UB914QSQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	35.0
DS90UB914QSQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
DS90UB914QSQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	35.0

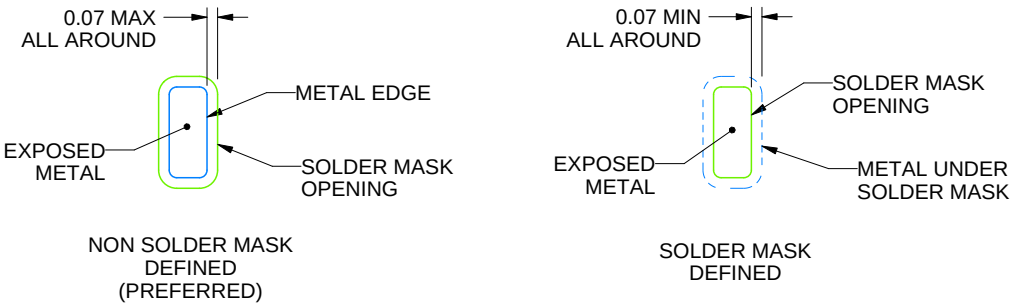


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

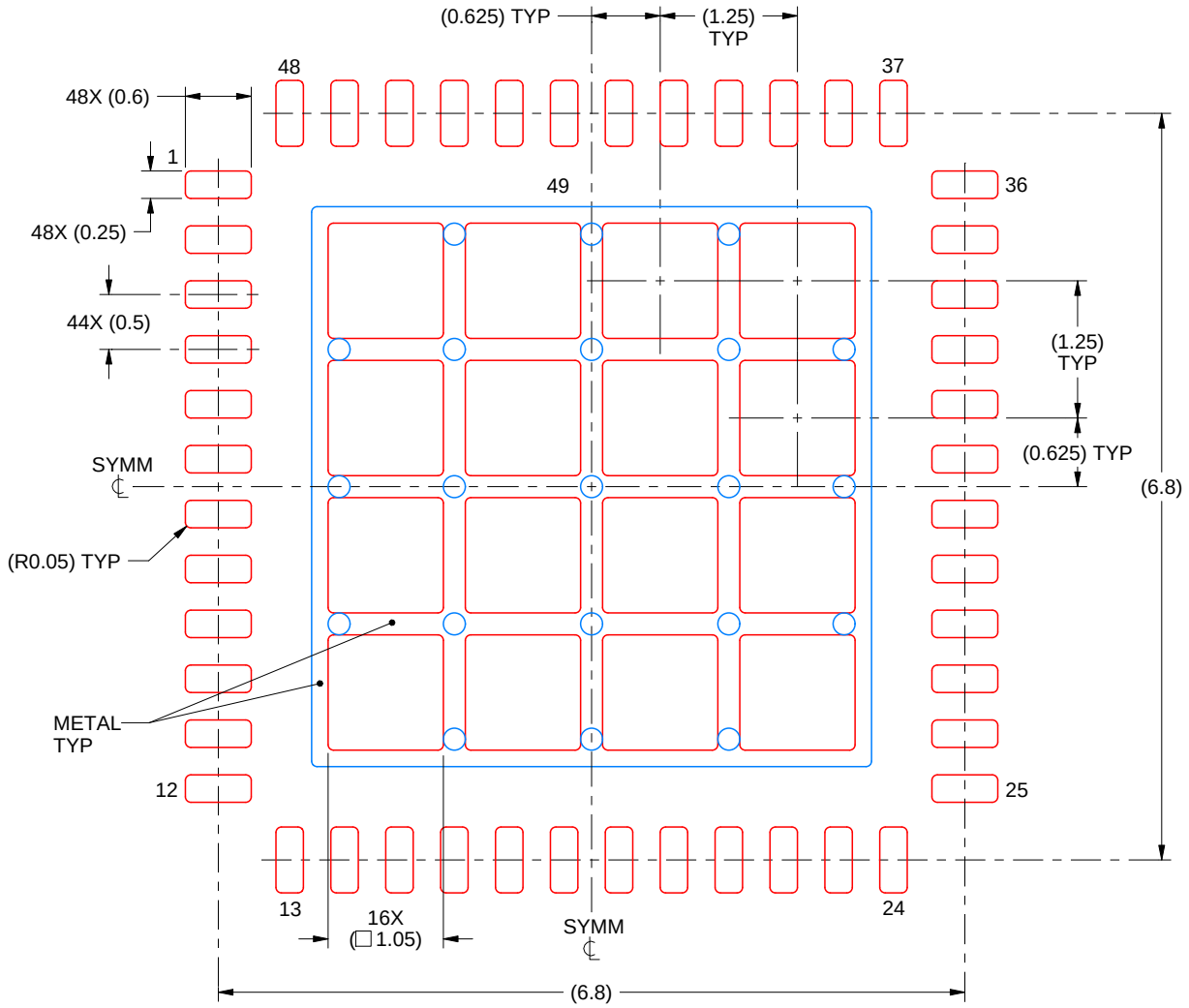


SOLDER MASK DETAILS

4214990/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

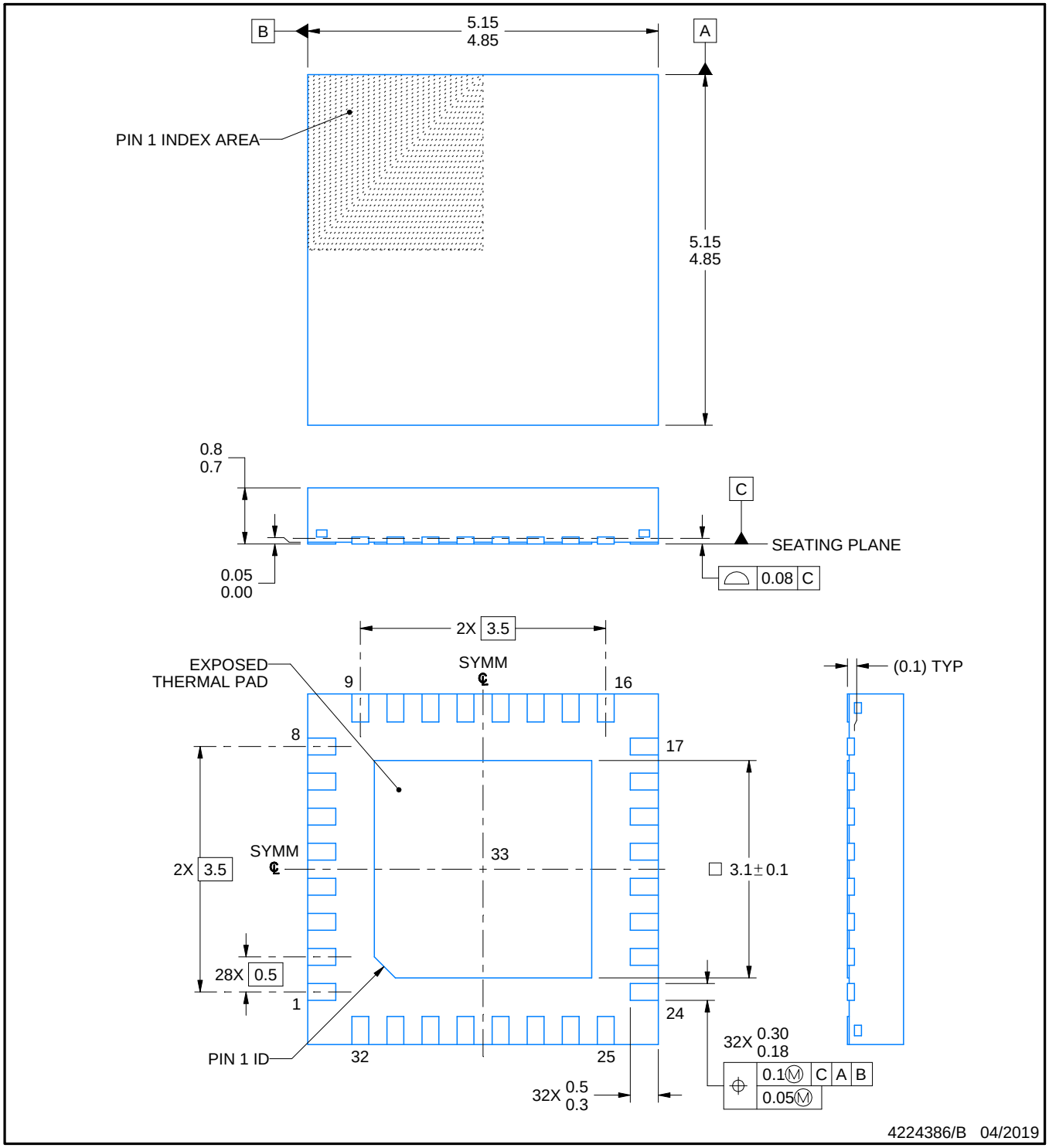
EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4214990/B 04/2018

NOTES: (continued)

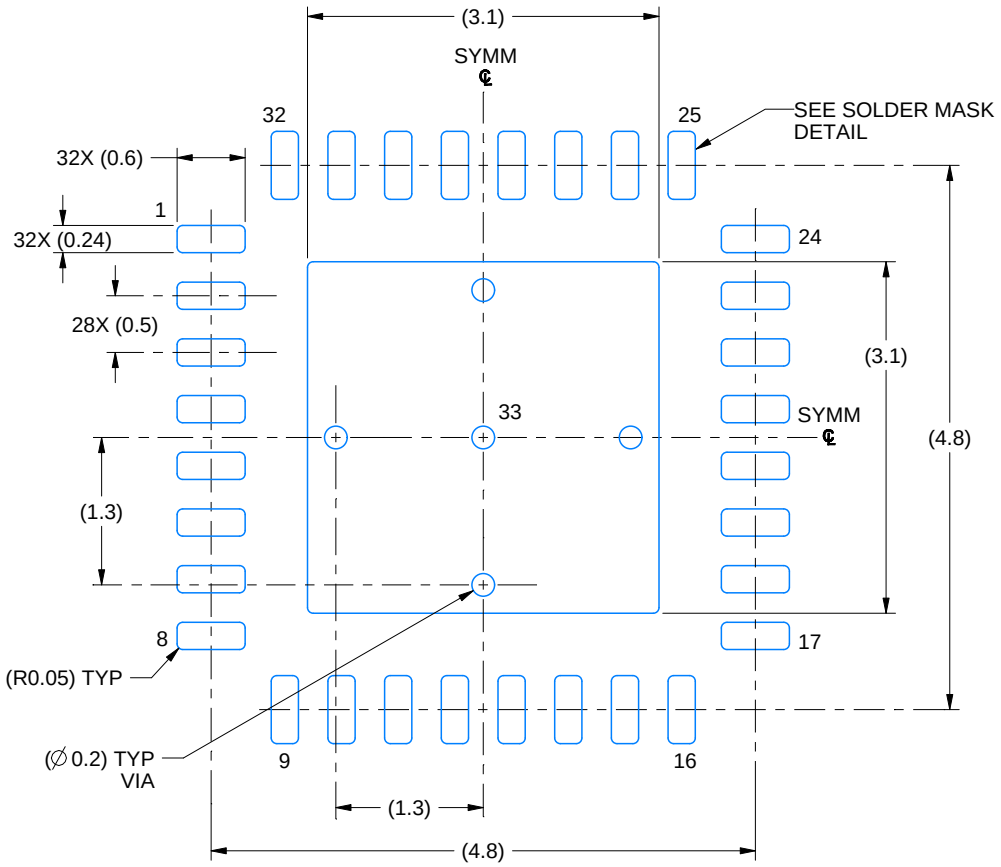
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PLASTIC QUAD FLATPACK - NO LEAD

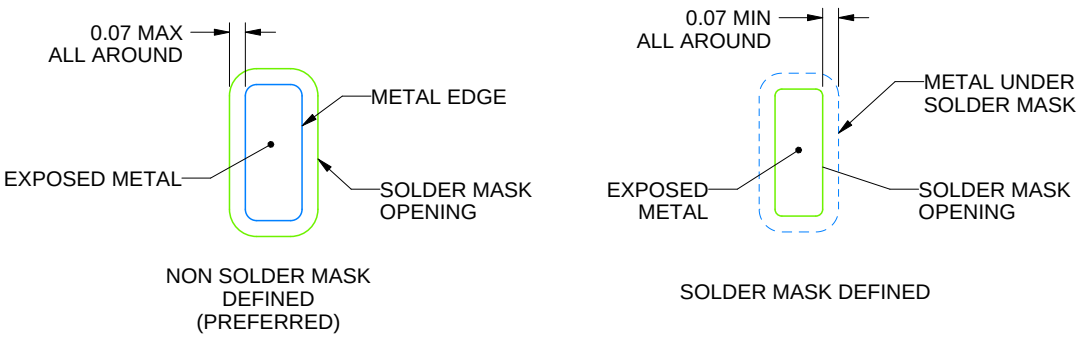


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

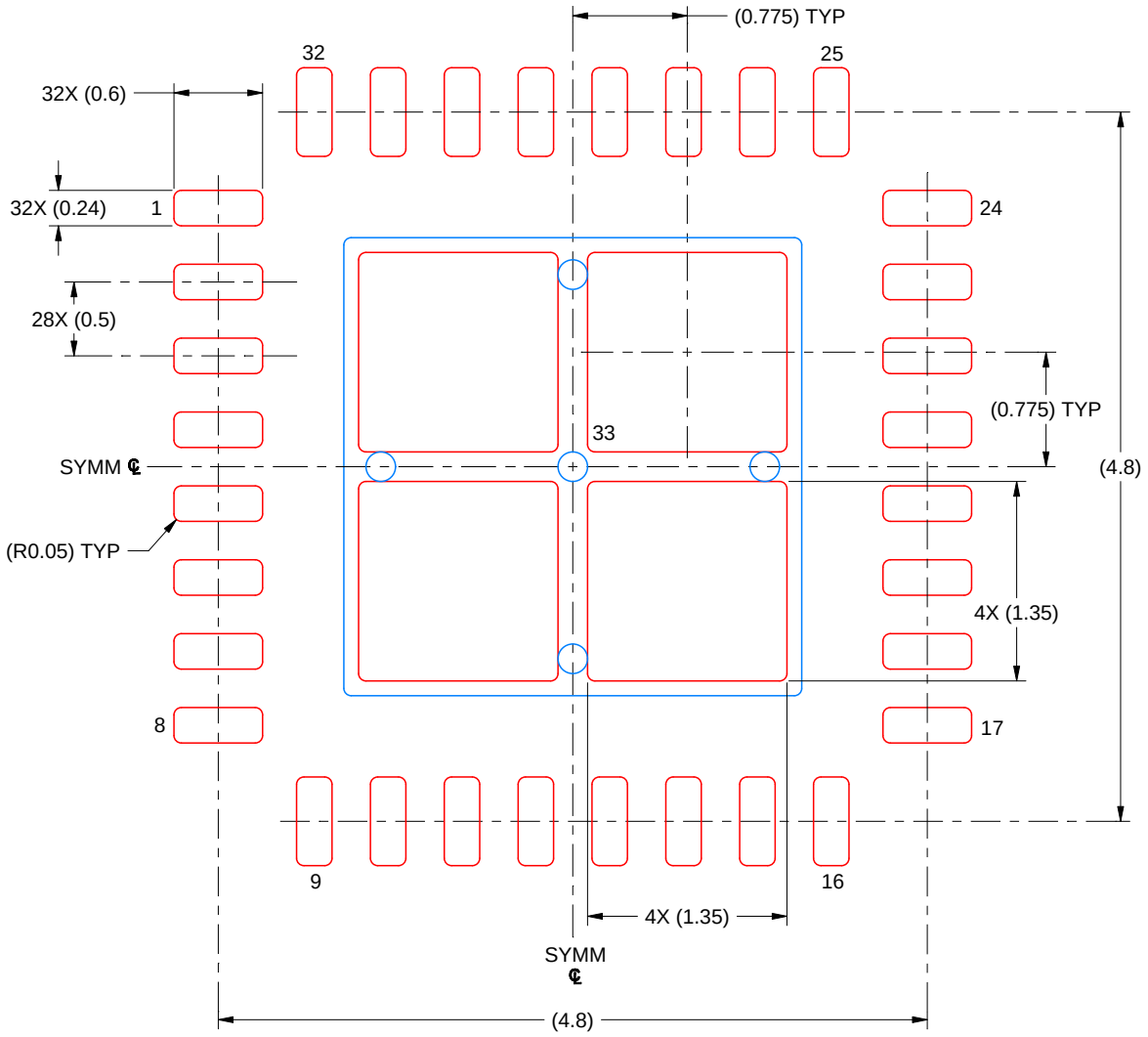


SOLDER MASK DETAILS

4224386/B 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224386/B 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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