DS25CP152Q Automotive 3.125 Gbps LVDS 2x2 Crosspoint Switch

Check for Samples: **DS25CP152Q**

## FEATURES

- **AECQ-100 Grade 3**
- **DC - 3.125 Gbps Low Jitter, Low Skew, Low Power Operation**
- **Pin Configurable, Fully Differential, Non-Blocking Architecture**
- **On-chip 100Ω Input and Output Terminations Minimize Return Losses, Reduce Component Count and Minimize Board Space**
- **8 kV ESD on LVDS I/O Pins Protects Adjoining Components**
- **Small 4 mm x 4 mm WQFN-16 Space Saving Package**

APPLICATIONS

- **Automotive Display Applications**
- **Clock and Data Buffering and Muxing**
- **OC-48 / STM-16**
- **SD/HD/3G HD SDI Routers**
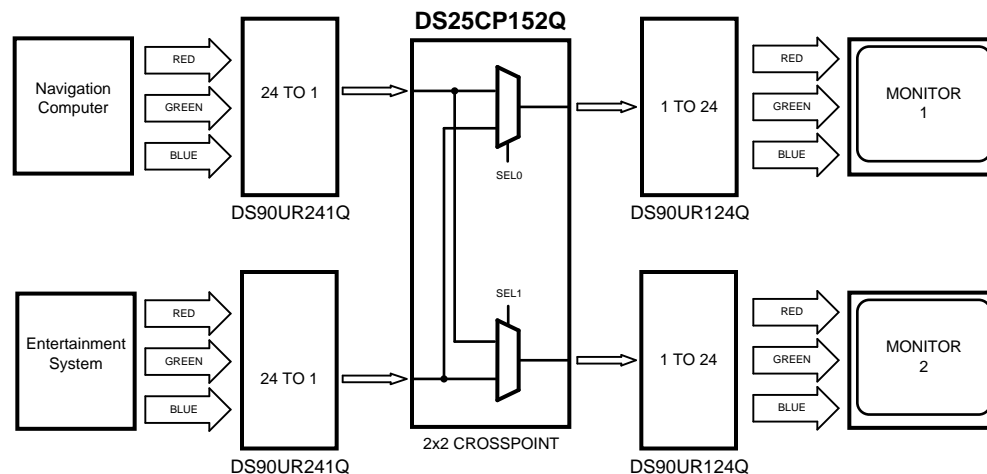
DESCRIPTION

The DS25CP152Q is a 3.125 Gbps 2x2 LVDS crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a 100Ω resistor to lower device return losses, reduce component count and further minimize board space.
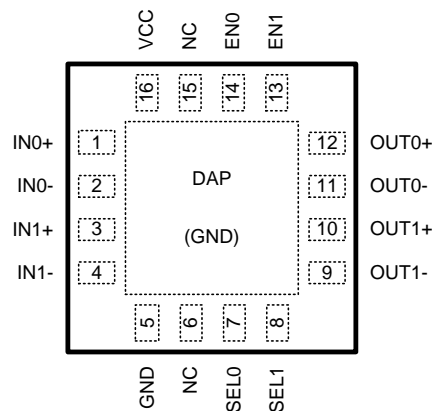
Typical Application

Block Diagram
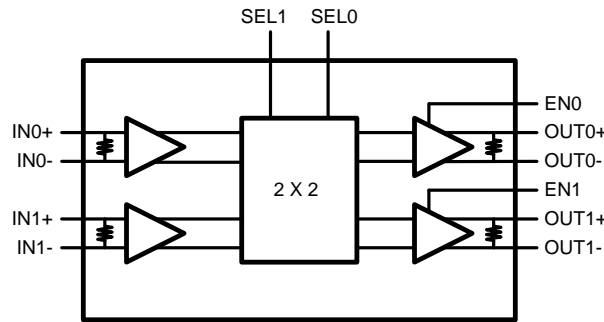
Connection Diagram

Figure 1. DS25CP152Q Pin Diagram

PIN DESCRIPTIONS

Pin Name	Pin Number	I/O, Type	Pin Description
IN0+, IN0- , IN1+, IN1-	1, 2, 3, 4	I, LVDS	Inverting and non-inverting high speed LVDS input pins.
OUT0+, OUT0-, OUT1+, OUT1-	12, 11, 10, 9	O, LVDS	Inverting and non-inverting high speed LVDS output pins.
SEL0, SEL1	7, 8	I, LVCMOS	Switch configuration pins. There is a 20 kΩ pulldown resistor on each pin.
EN0, EN1	14, 13	I, LVCMOS	Output enable pins. There is a 20 kΩ pulldown resistor on each pin.
NC	6, 15	I, LVCMOS	"NO CONNECT" pins.
VDD	16	Power	Power supply pin.
GND	5, DAP	Power	Ground pin and Device Attach Pad (DAP) ground.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)]

Supply Voltage	−0.3V to +4V
LVCMOS Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Input Voltage	−0.3V to +4V
Differential Input Voltage |VID|	1.0V
LVDS Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Differential Output Voltage	0V to 1.0V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+105°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
RGH0016A Package	1.91W
Derate RGH0016A Package	23.9 mW/°C above +25°C
Package Thermal Resistance	
θ_{JA}	+41.8°C/W
θ_{JC}	+6.9°C/W
ESD Susceptibility	
HBM [(3)]	≥8 kV
MM [(4)]	≥250V
CDM [(5)]	≥1250V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. [(1)(2)(3)]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V V_{CC} = 3.6V	40	175	250	µA
I_{IL}	Low Level Input Current	V_{IN} = GND V_{CC} = 3.6V		0	±10	µA

(1) The Electrical Characteristics tables list ensure specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not ensured.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. [(1)(2)(3)]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA, V_{CC} = 0V		−0.9	−1.5	V
LVDS INPUT DC SPECIFICATIONS						
V_{ID}	Input Differential Voltage		0		1	V
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V or V_{CC}-0.05V		0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100 mV	0.05		V_{CC} - 0.05	V
I_{IN}	Input Current	V_{IN} = +3.6V or 0V V_{CC} = 3.6V or 0V		±1	±10	µA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R_{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω
LVDS OUTPUT DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	R_L = 100Ω	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current [(4)]	OUT to GND		-35	-55	mA
		OUT to V_{CC}		7	55	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
SUPPLY CURRENT						
I_{CC}	Supply Current	EN0 = EN1 = High		64	77	mA
I_{CCZ}	Supply Current with Outputs Disabled	EN0 = EN1 = Low		23	29	mA

(4)   Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified [(1)(2)(3)]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS						
t_{PLHD}	Differential Propagation Delay Low to High	R_L = 100Ω		340	500	ps
t_{PHLD}	Differential Propagation Delay High to Low			344	500	ps
t_{SKD1}	Pulse Skew |$t_{PLHD} - t_{PHLD}$| [(4)]			4	35	ps
t_{SKD2}	Channel to Channel Skew [(5)]			12	40	ps
t_{SKD3}	Part to Part Skew [(6)]			50	150	ps

(1)   The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2)   Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(3)   Specification is ensured by characterization and is not tested in production.
(4) t_{SKD1}, |$t_{PLHD} - t_{PHLD}$|, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) t_{SKD2}, Channel to Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Broadcast mode (any one input to all outputs).
(6) t_{SKD3}, Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Product Folder Links: DS25CP152Q

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified [1][2][3]

| Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{LHT}	Rise Time	$R_L = 100\Omega$			65	120	ps
t_{HLT}	Fall Time				65	120	ps
t_{ON}	Output Enable Time	ENn = LH to output active			7	20	μs
t_{OFF}	Output Disable Time	ENn = HL to output inactive			5	12	ns
t_{SEL}	Select Time	SELn LH or HL to output			3.5	12	ns
JITTER PERFORMANCE [3]							
t_{RJ1}	Random Jitter (RMS Value) [7]	$V_{ID} = 350$ mV $V_{CM} = 1.2$V Clock (RZ)	2.5 Gbps		0.5	1	ps
t_{RJ2}			3.125 Gbps		0.5	1	ps
t_{DJ1}	Deterministic Jitter (Peak to Peak) [8]	$V_{ID} = 350$ mV $V_{CM} = 1.2$V K28.5 (NRZ)	2.5 Gbps		8	25	ps
t_{DJ2}			3.125 Gbps		3	19	ps
t_{TJ1}	Total Jitter (Peak to Peak) [9]	$V_{ID} = 350$ mV $V_{CM} = 1.2$V PRBS-23 (NRZ)	2.5 Gbps		0.04	0.08	UI_{P-P}
t_{TJ2}			3.125 Gbps		0.03	0.09	UI_{P-P}

(7)   Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
(8)   Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
(9)   Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC Test Circuits
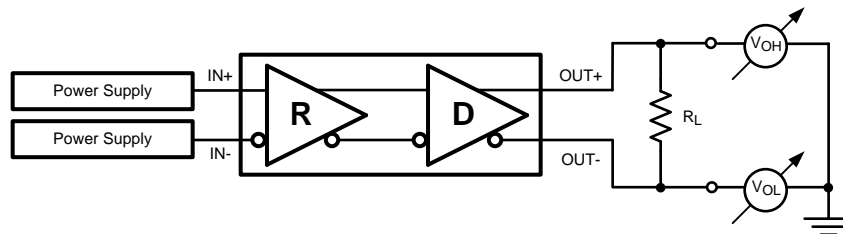
AC Test Circuits and Timing Diagrams

Product Folder Links: DS25CP152Q
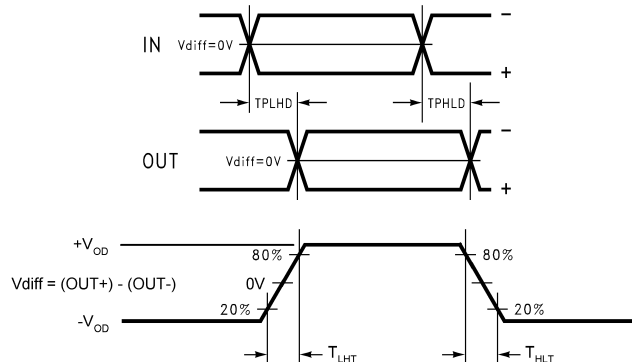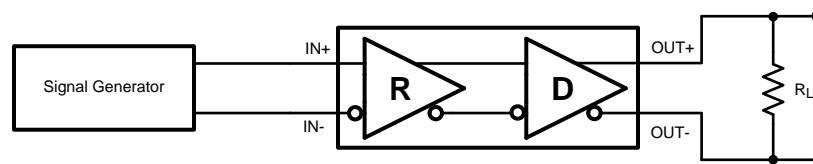
FUNCTIONAL DESCRIPTION

The DS25CP152Q is a 3.125 Gbps 2x2 LVDS digital crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables.

Switch Configuration Truth Table

S1	S0	OUT1	OUT0
0	0	IN0	IN0
0	1	IN0	IN1
1	0	IN1	IN0
1	1	IN1	IN1

Output Enable Truth Table

EN1	EN0	OUT1	OUT0
0	0	Disabled	Disabled
0	1	Disabled	Enabled
1	0	Enabled	Disabled
1	1	Enabled	Enabled

Input Interfacing

The DS25CP152Q accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25CP152Q can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25CP152Q inputs are internally terminated with a 100Ω resistor.
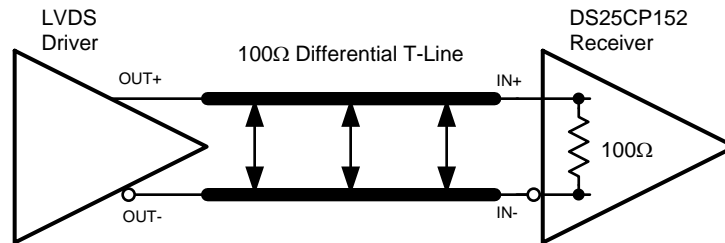

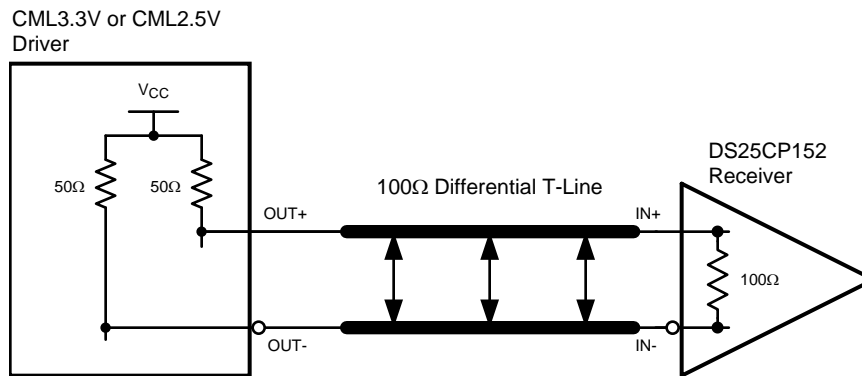**Figure 2. Typical LVDS Driver DC-Coupled Interface to DS25CP152Q Input**

Figure 3. Typical CML Driver DC-Coupled Interface to DS25CP152Q Input
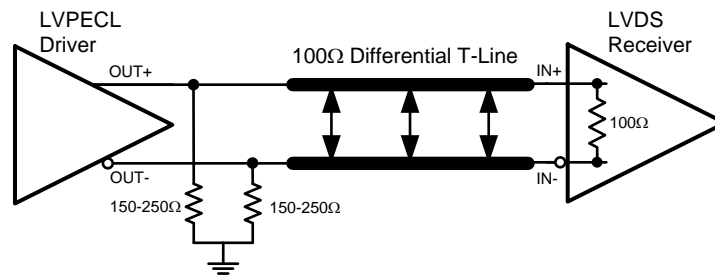
Product Folder Links: *DS25CP152Q*

Figure 4. Typical LVPECL Driver DC-Coupled Interface to DS25CP152Q Input

Output Interfacing

The DS25CP152Q outputs signals that are compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check the respective receiver's data sheet prior to implementing the suggested interface implementation.
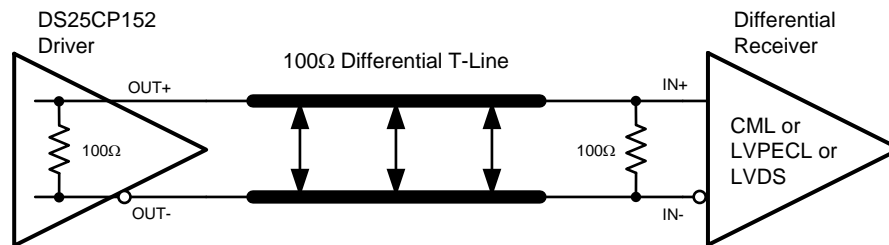

Figure 5. Typical DS25CP152Q Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver
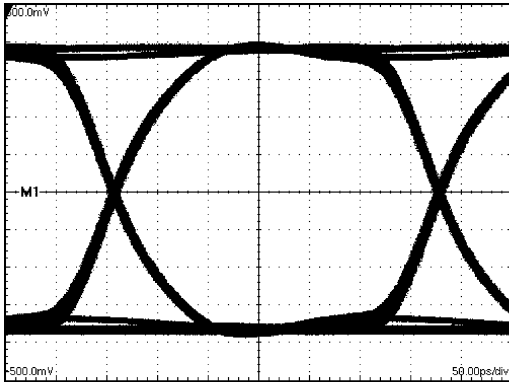
Typical Performance Characteristics

Figure 6. A 3.125 Gbps NRZ PRBS-7 After 2"
Differential FR-4 Stripline
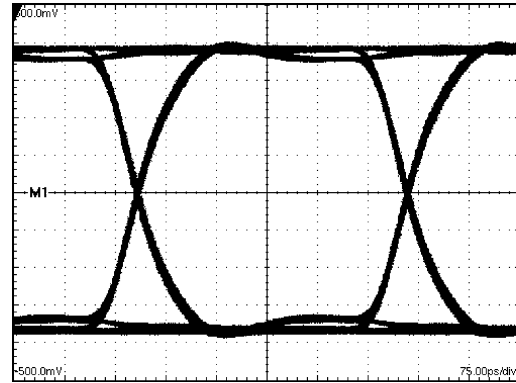V:100 mV / DIV, H:50 ps / DIV

Figure 7. A 2.5 Gbps NRZ PRBS-7 After 2"
Differential FR-4 Stripline
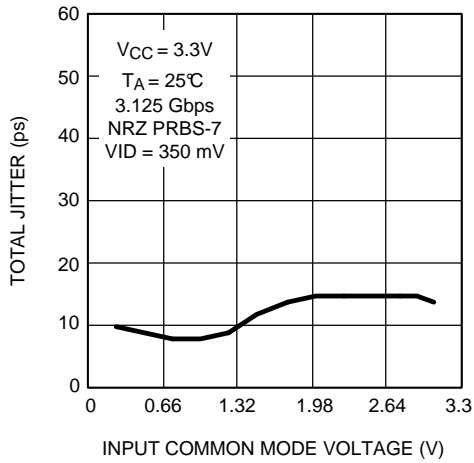V:100 mV / DIV, H:75 ps / DIV

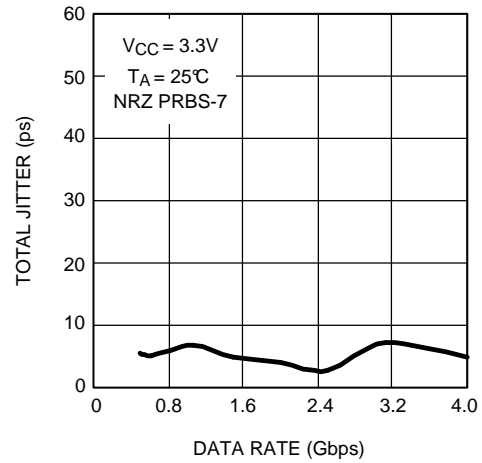Figure 8. Total Jitter as a Function of Input Common Mode
Voltage

Figure 9. Total Jitter as a Function of Data Rate

Product Folder Links: *DS25CP152Q*

REVISION HISTORY

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS25CP152QSQ/NOPB	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2C152QS
DS25CP152QSQ/NOPB.A	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2C152QS
DS25CP152QSQ/NOPB.B	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
DS25CP152QSQX/NOPB	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2C152QS
DS25CP152QSQX/NOPB.A	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2C152QS
DS25CP152QSQX/NOPB.B	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

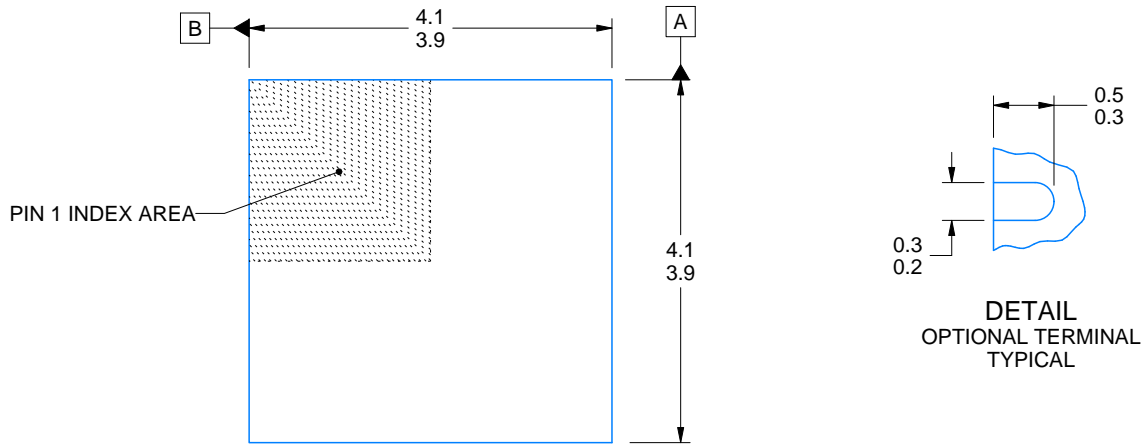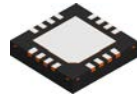**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

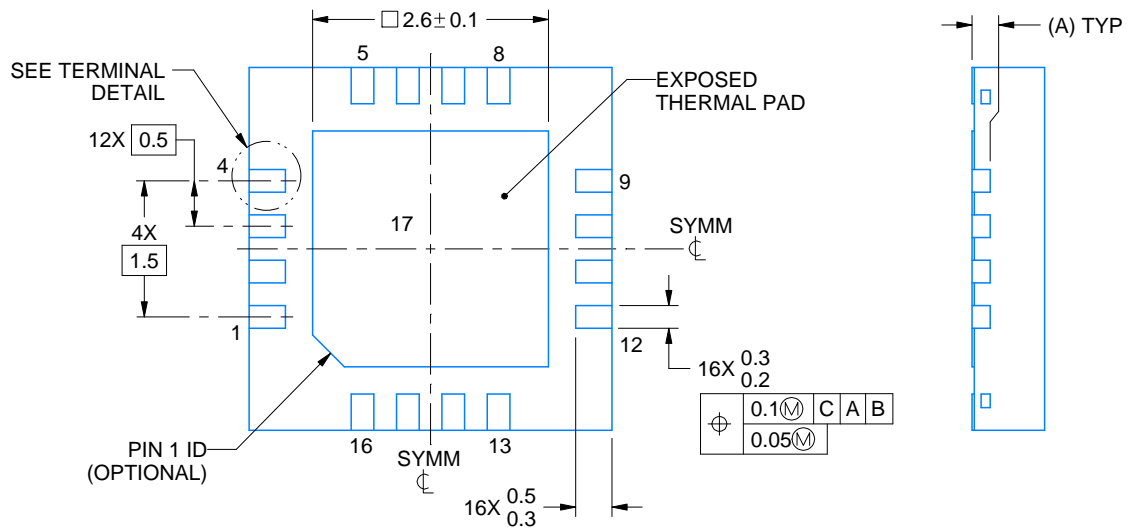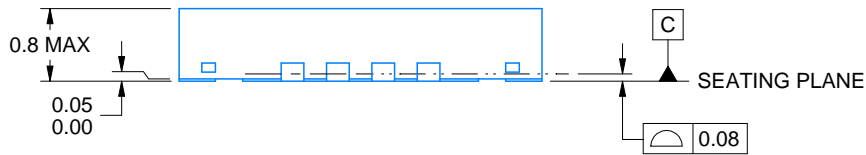| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25CP152QSQ/NOPB	WQFN	RGH	16	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS25CP152QSQX/NOPB	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25CP152QSQ/NOPB	WQFN	RGH	16	1000	210.0	185.0	35.0
DS25CP152QSQX/NOPB	WQFN	RGH	16	4500	367.0	367.0	35.0

B

4.1
3.9

A

PIN 1 INDEX AREA

4.1
3.9

0.5
0.3

0.3
0.2

DETAIL
OPTIONAL TERMINAL
TYPICAL

DIM A	
OPT 1	OPT 1
(0.1)	(0.2)

0.8 MAX

0.05
0.00

C

SEATING PLANE

| △ | 0.08 |

□ 2.6 ± 0.1

(A) TYP

SEE TERMINAL
DETAIL

5   8

EXPOSED
THERMAL PAD

12X | 0.5 |

4

9

17

SYMM
₵

4X
| 1.5 |

1

12

16X 0.3
0.2

⊕	0.1 Ⓜ	C	A	B
	0.05 Ⓜ			

PIN 1 ID
(OPTIONAL)

16   SYMM   13
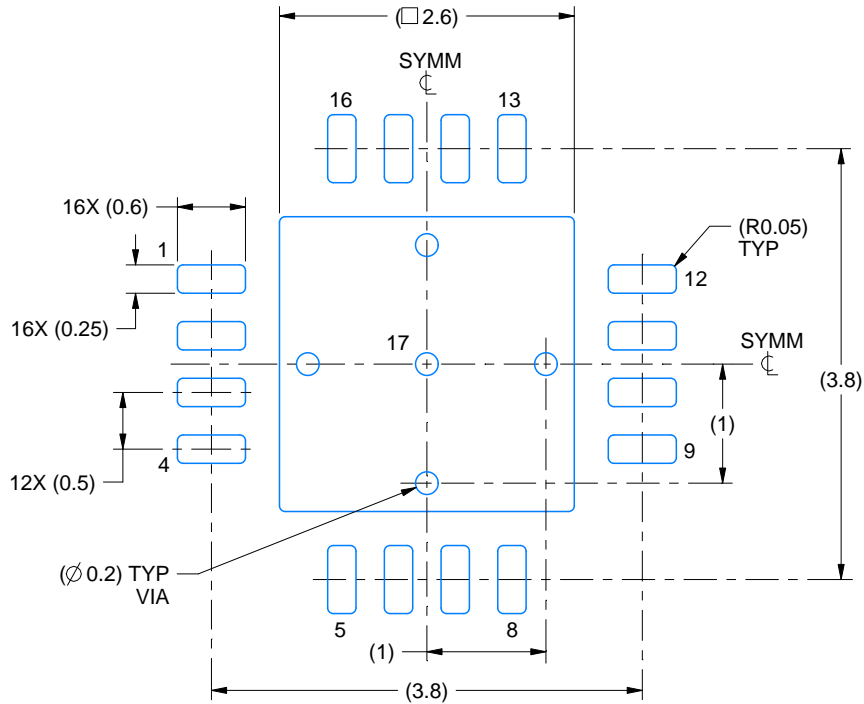₵

16X 0.5
0.3

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

(□2.6)

SYMM

16   13
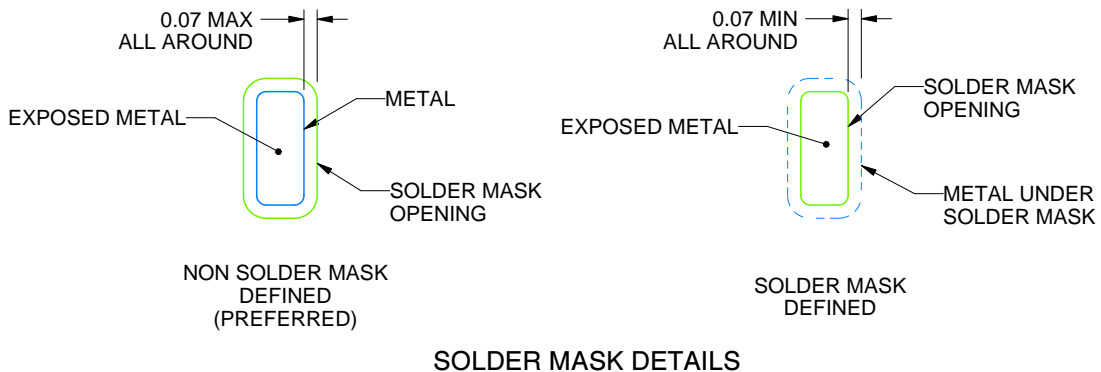
16X (0.6)

1

16X (0.25)

17   (R0.05) TYP

12

SYMM

(3.8)

4

(1)

9

12X (0.5)

(⌀ 0.2) TYP VIA

5   8

(1)

(3.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

0.07 MAX
ALL AROUND

METAL

EXPOSED METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

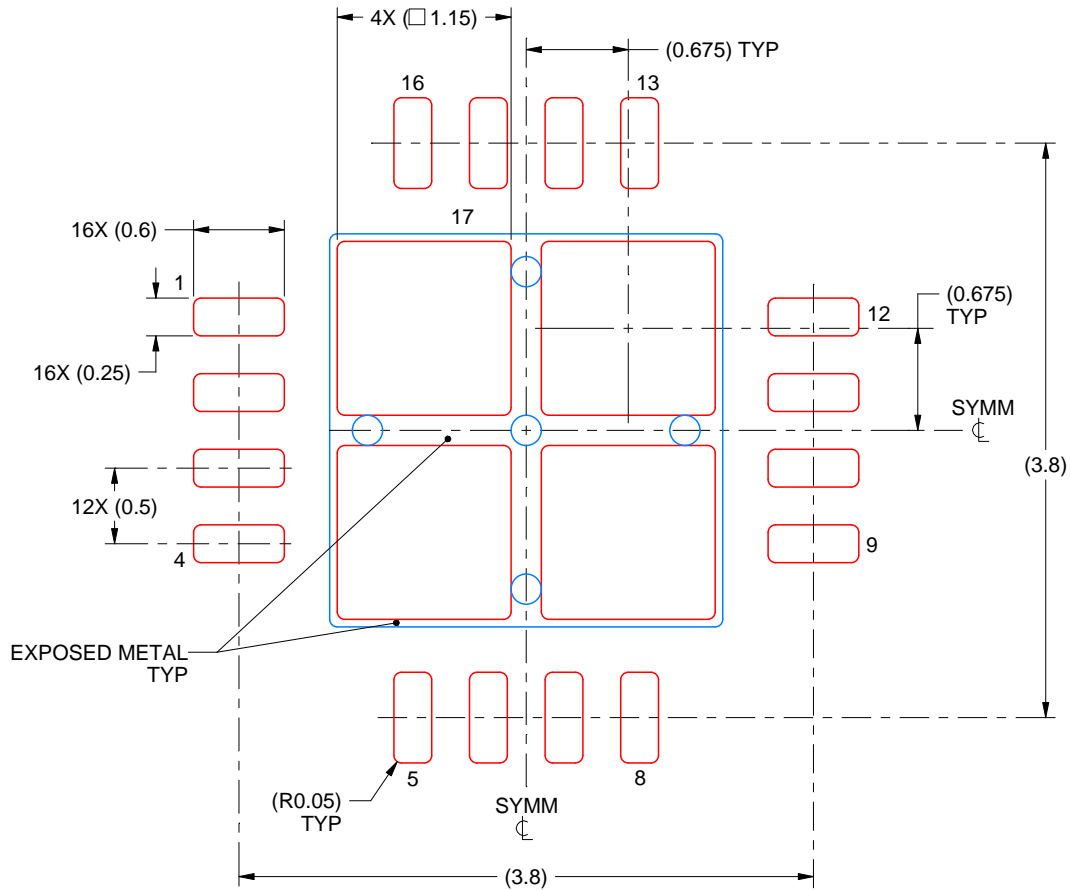SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

4X (□ 1.15)

(0.675) TYP

16

13

16X (0.6)

17

1

16X (0.25)

12

(0.675) TYP

SYMM ₵

12X (0.5)

(3.8)

4

9

EXPOSED METAL TYP

(R0.05) TYP

5

SYMM ₵

8

(3.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

TEXAS INSTRUMENTS
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