具有高性能传感、保护和诊断功能的DRV3245E-Q1三相 0 级汽车栅极驱动器单元 (GDU)

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 0：
    –40°C 至 +150°C，T_A
- SafeTI™半导体组件
  - 根据 ISO 26262 标准的相应要求开发
- 4.5V 至 45V 工作电压范围
- 可编程峰值栅极驱动电流高达 1A
- 支持 100% 占空比的电荷泵栅极驱动器
- 电流分流放大器和相位比较器
  - A 器件：3 个电流分流放大器和三相比较器，具有状态，通过 SPI
  - B 器件：2 个电流分流放大器和三相比较器，具有实时监控器，通过数字引脚
- 高达 20kHz 的 3 PWM 或 6 PWM 输入控制
- 能够进行单 PWM 模式换向
- 支持 3.3V 和 5V 数字接口
- 串行外设接口 (SPI)
- 耐热增强型 48 引脚 HTQFP 封装
- 保护 功能：
  - 内部稳压器、电池电压监控器
  - SPI CRC
  - 时钟监控器
  - 模拟内置自检
  - 可编程的死区时间控制
  - MOSFET 击穿保护
  - MOSFET V_{DS} 过流监视器
  - 栅源电压实时监控器
  - 过热警告

2 应用

- 高温 12V 汽车应用
  - 手自一体变速器和双离合器变速器
  - 线控换档
  - 分动箱和泵

3 说明

DRV3245E-Q1 器件是一款适用于三相电机驱动 应用。此器件适用于高温汽车 应用 ，根据 ISO 26262 标准中有关功能安全应用的相应要求设计 而成。该器件具有三个半桥驱动器，每个驱动器都能够驱动高侧和低侧 N 沟道 MOSFET，同时还具有先进的 FET 保护和监控功能。电荷泵驱动器可在冷启动运行期间实现 100% 占空比并支持低电池电压。凭借所集成的电流检测放大器、相位比较器和基于 SPI 的配置省去了大多数外部和无源组件，从而减少了所需物料并减小了印刷电路板 (PCB) 空间。

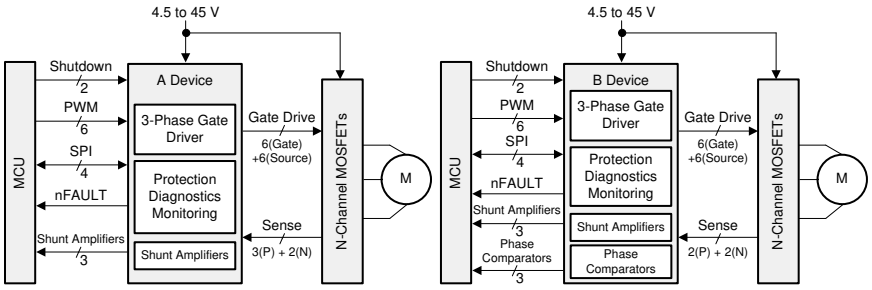
DRV3245E-Q1 器件还为内部时钟集成了诊断和保护功能，并可提供常用系统诊断检查支持，二者皆可进行实例化并通过 SPI 进行报告。这种集成 特性 的灵活性使得该器件能够无缝集成到各种安全架构中。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
DRV3245E-Q1	HTQFP (48)	7.00mm × 7.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



4 器件和文档支持

4.1 器件支持

4.1.1 器件命名规则

图 1 显示了 DRV3245E-Q1 器件的完整可订购器件名称的解读图例

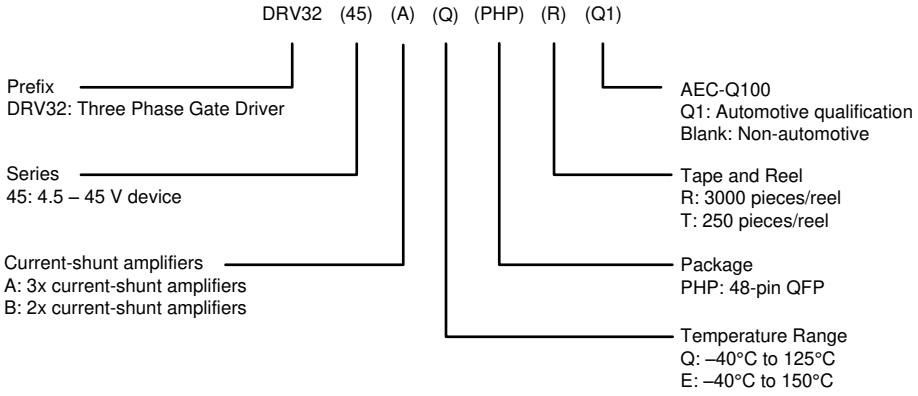


图 **1.** 器件命名规则

4.2 文档支持

相关文档请参见以下部分：

- 德州仪器 (TI)，《*PowerPAD™ 热增强型封装*》应用报告
- 德州仪器 (TI)，《*PowerPAD™ 速成*》应用报告
- 德州仪器 (TI)，《*使用 MSP430 的传感器式三相 BLDC 电机控制*》应用报告
- 德州仪器 (TI)，《*了解 TI 电机栅极驱动器中的 IDRIVE 和 TDRIVE*》应用报告

4.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

4.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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4.5 商标

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4.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

4.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

5 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV3245AEPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	D3245AE
DRV3245AEPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	D3245AE
DRV3245BEPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	D3245BE
DRV3245BEPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	D3245BE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

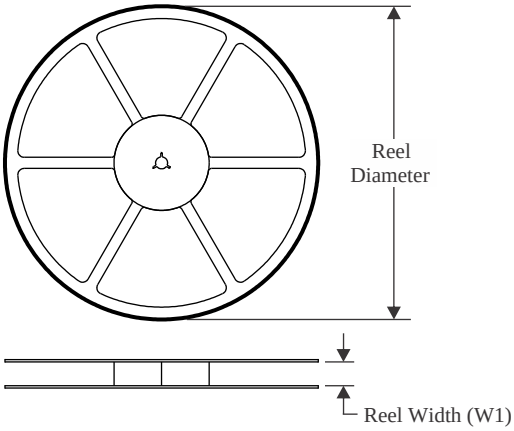
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

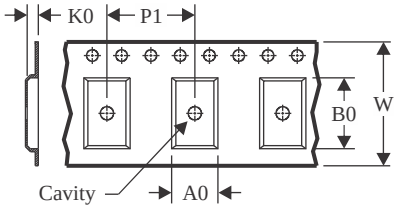
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

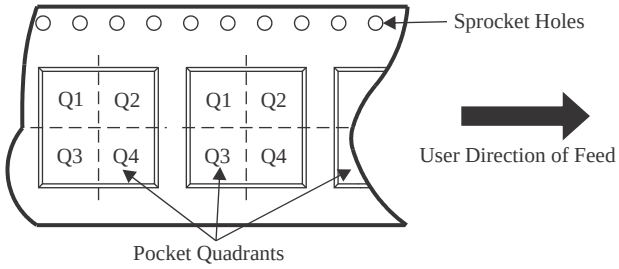


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

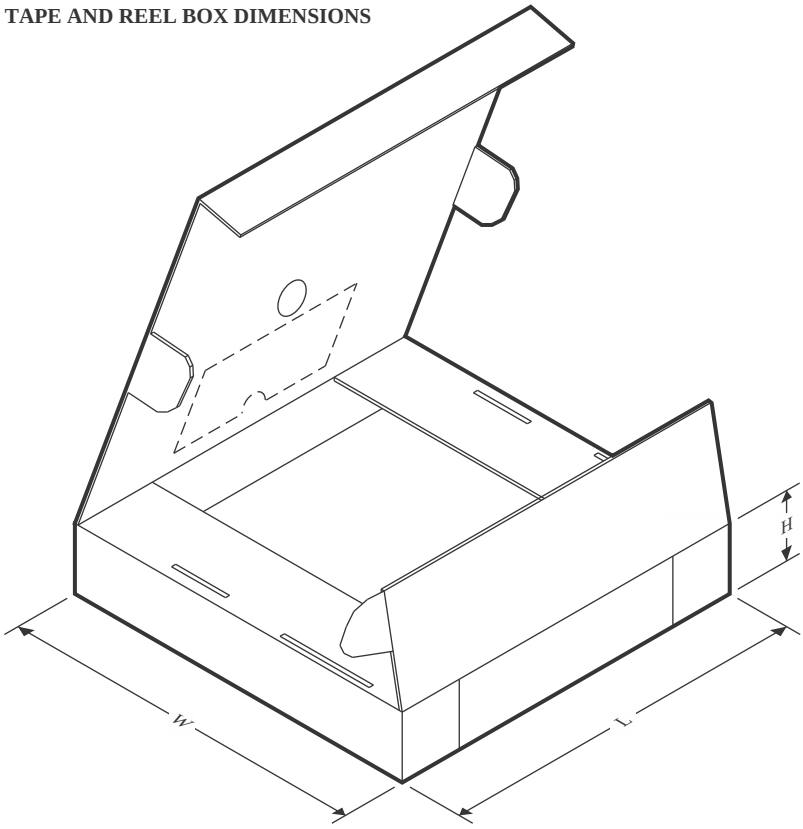
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3245AEPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DRV3245BEPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3245AEPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8
DRV3245BEPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

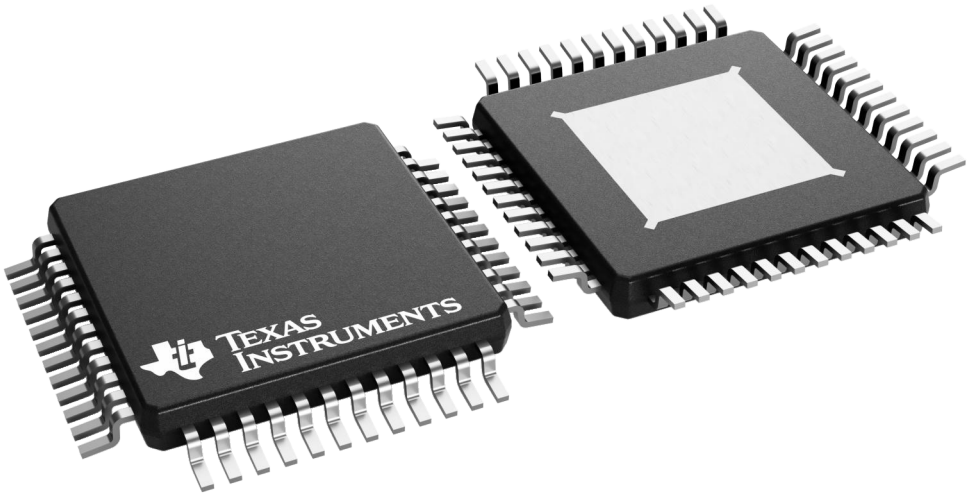
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



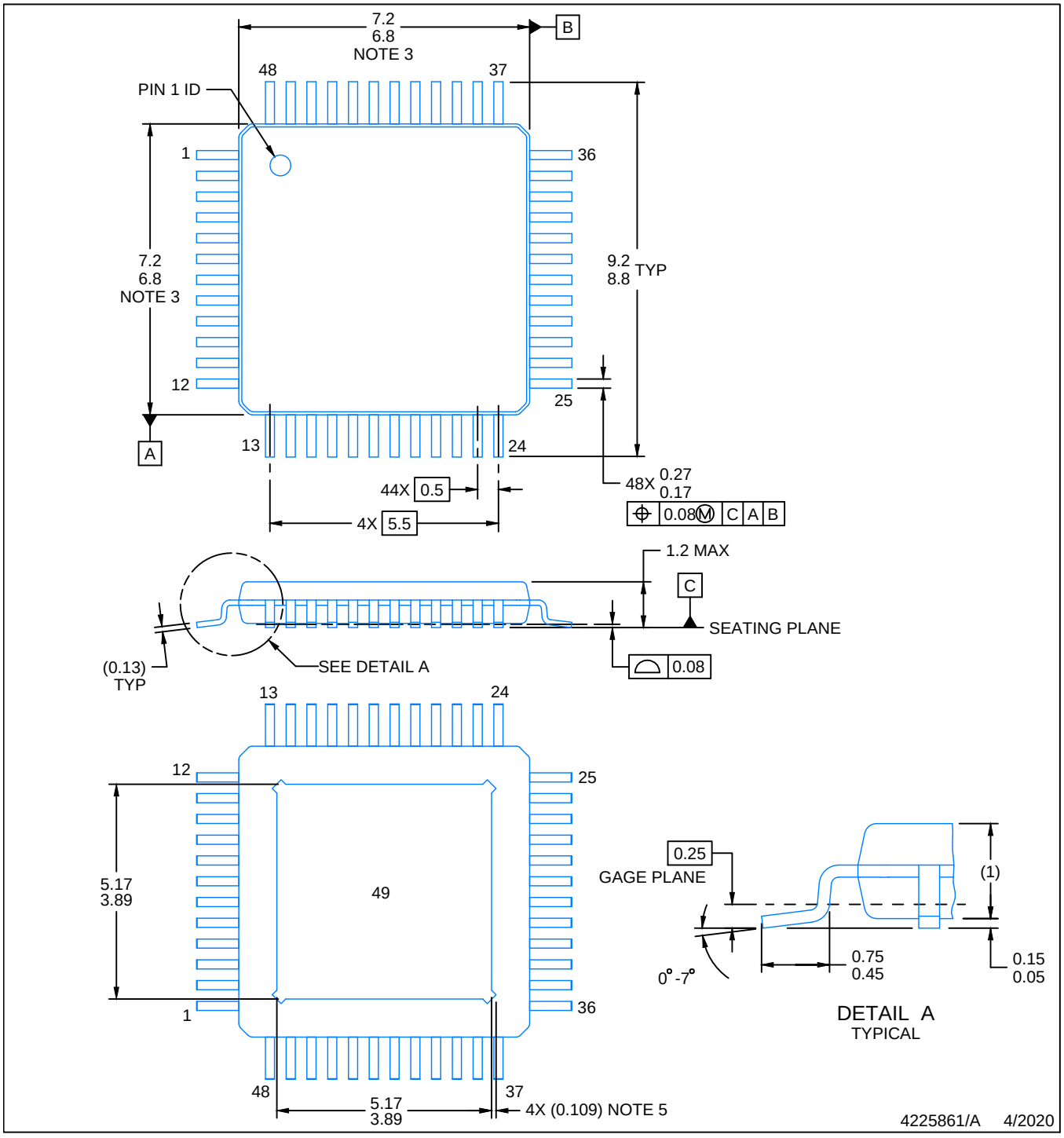
4226443/A

PACKAGE OUTLINE

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

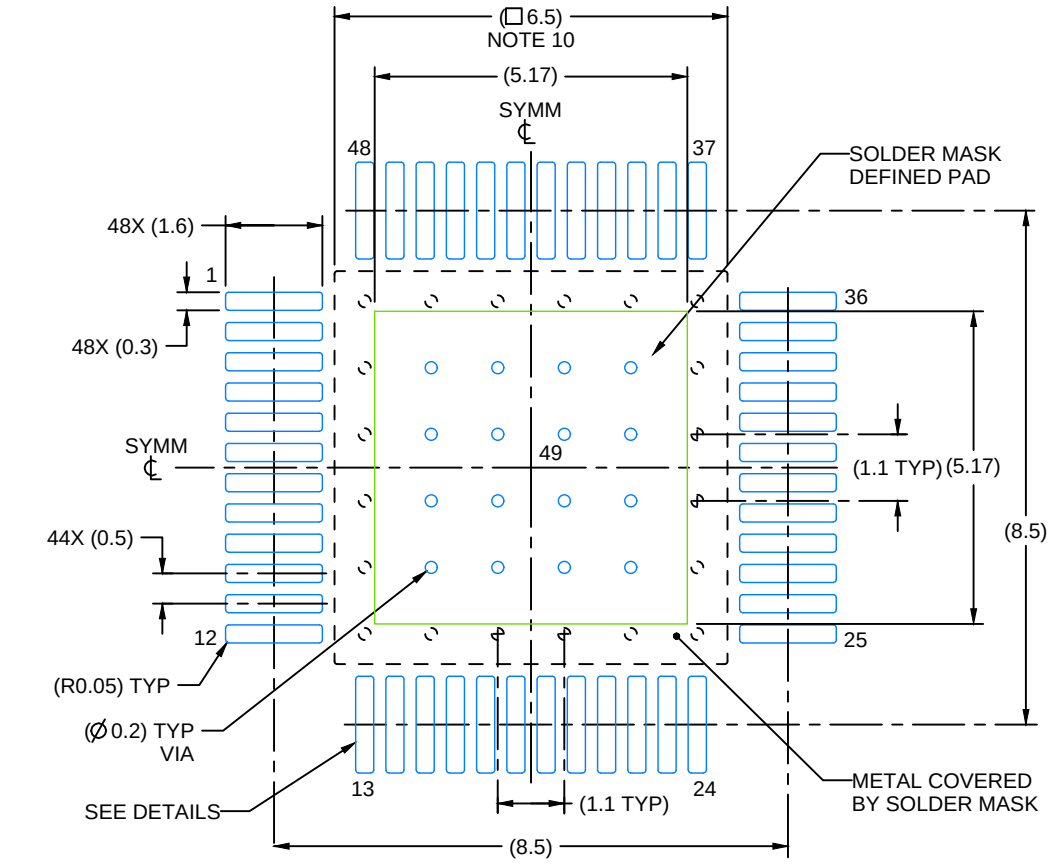
PLASTIC QUAD FLATPACK



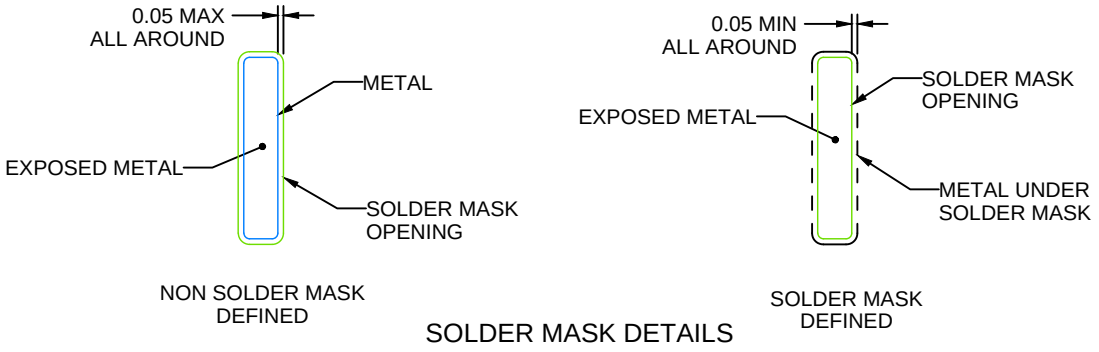
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

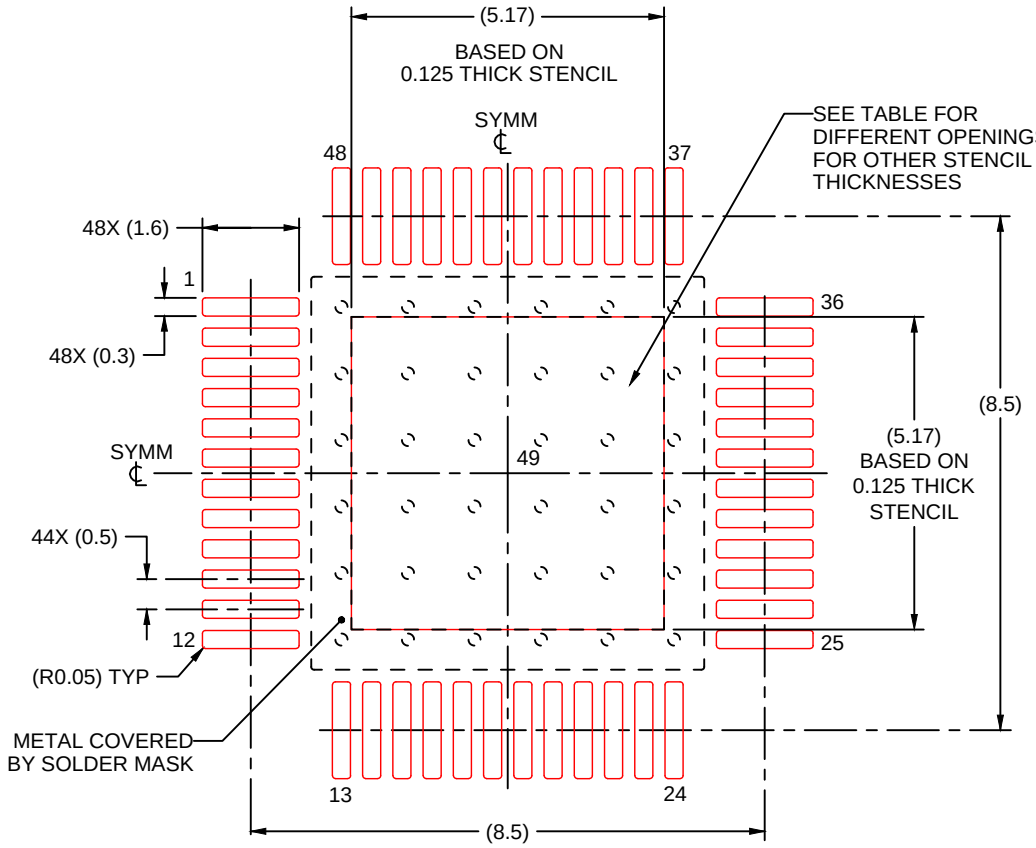


SOLDER MASK DETAILS

4225861/A 4/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

4225861/A 4/2020

NOTES: (continued)

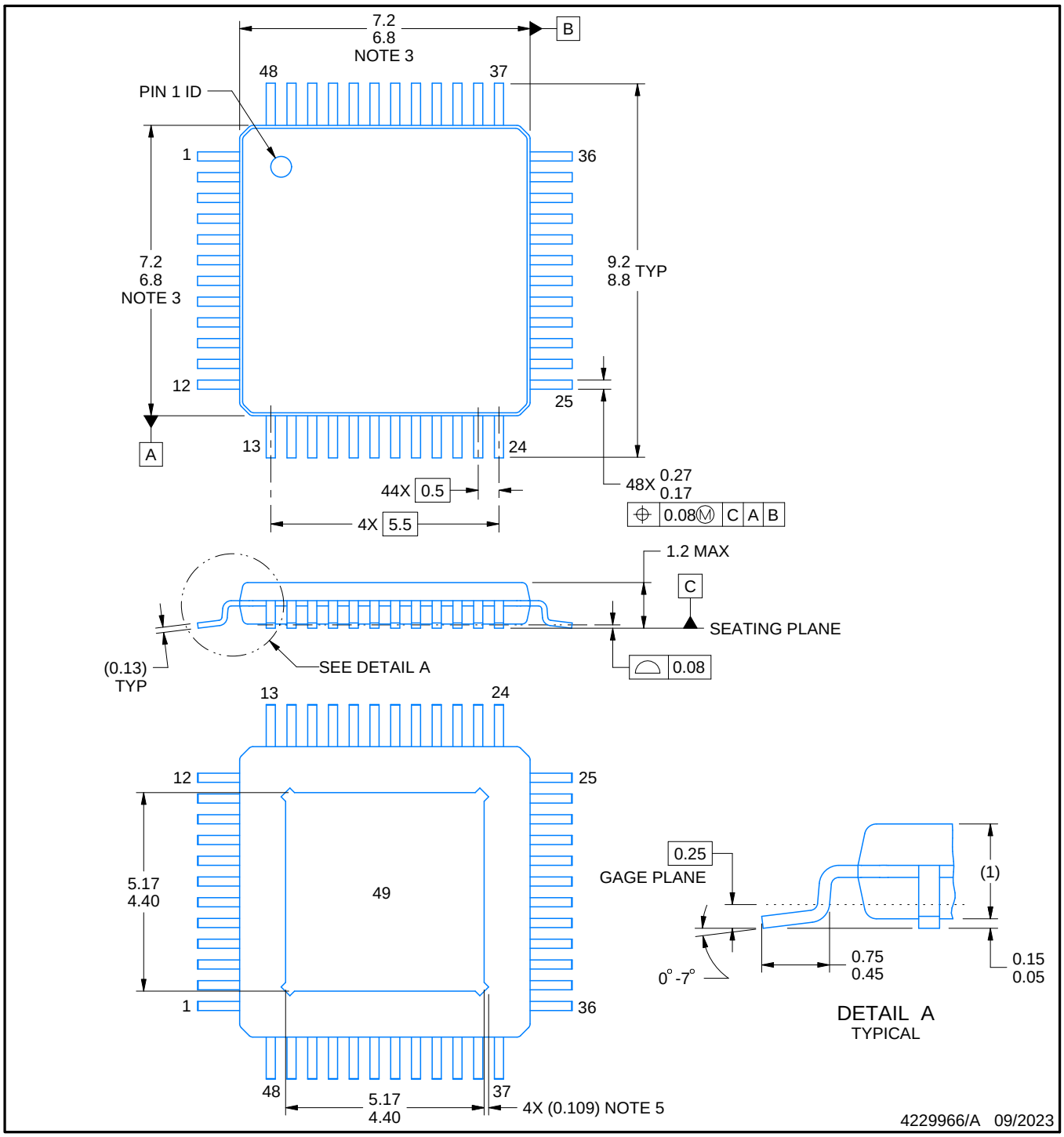
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PHP0048N

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

NOTES:

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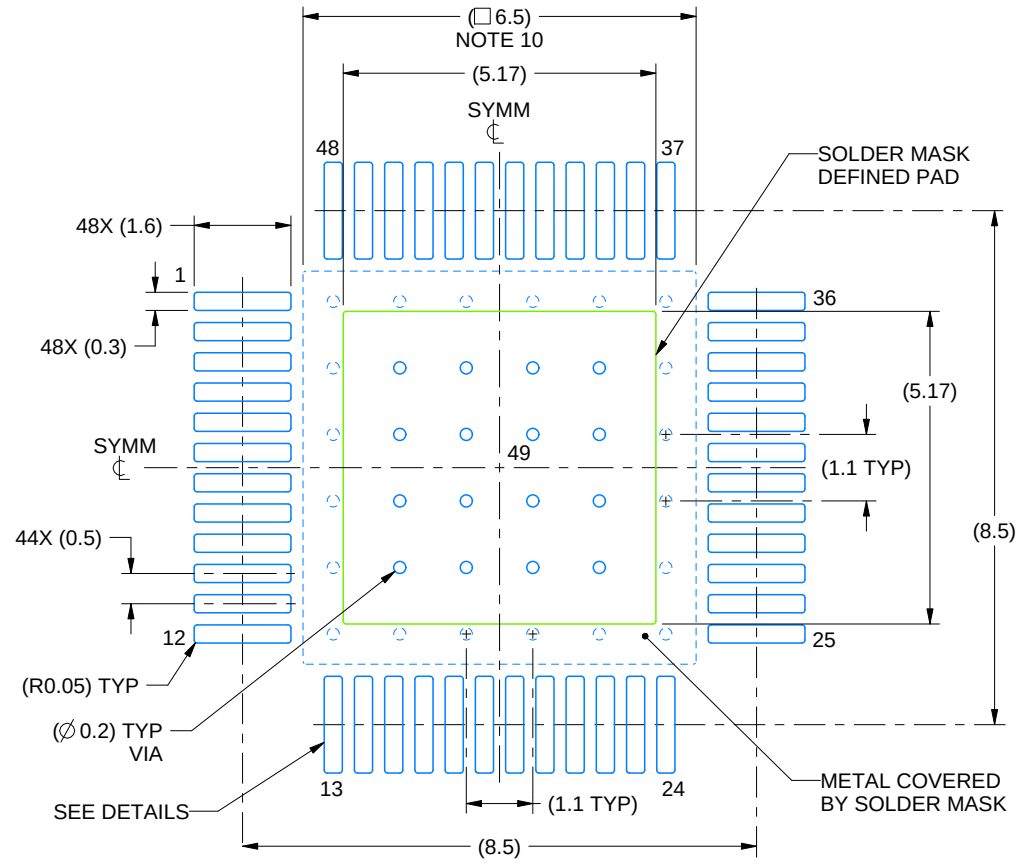
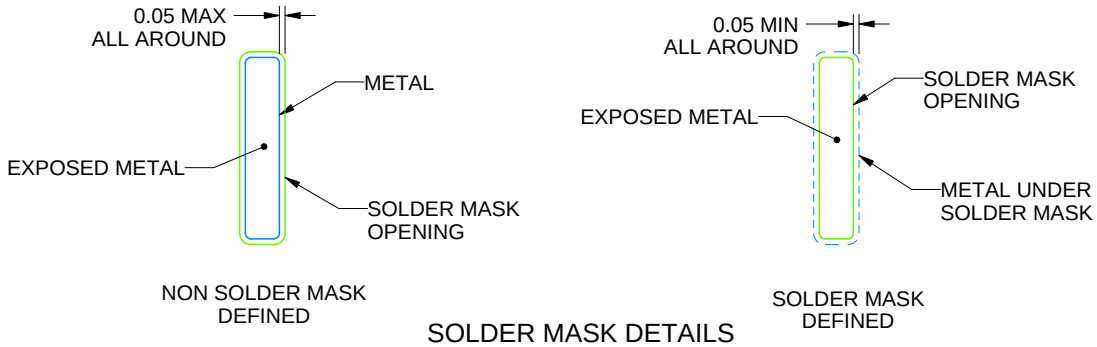
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

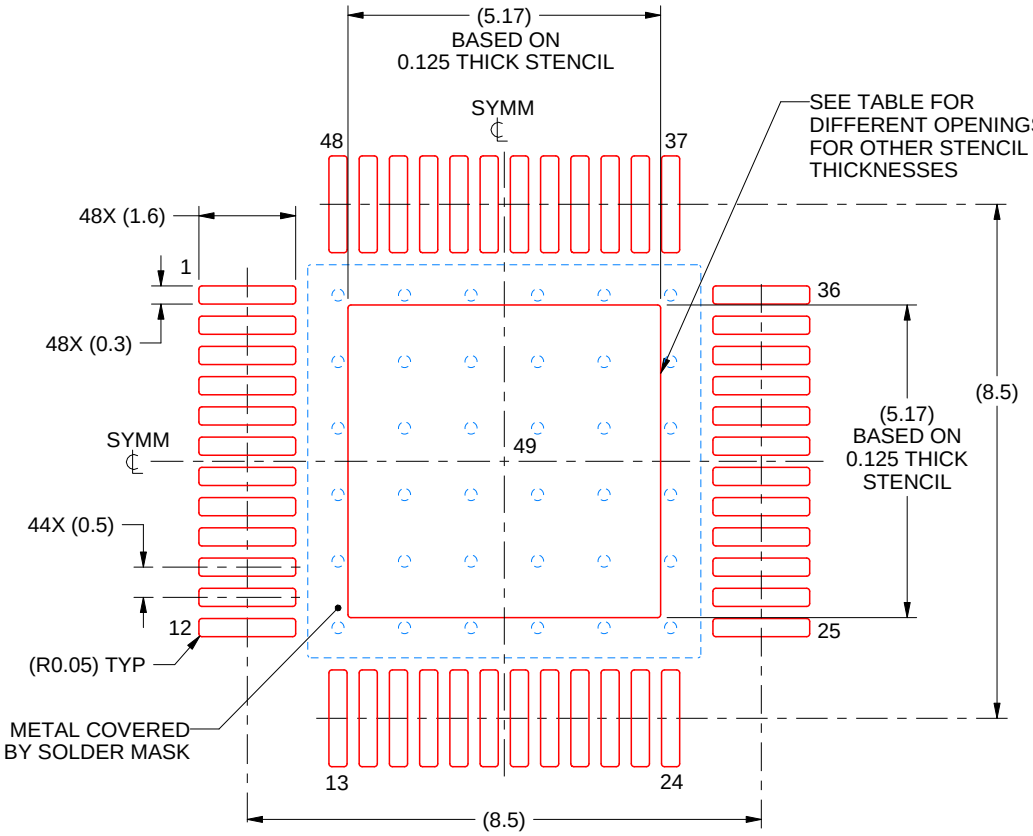


SOLDER MASK DETAILS

4229966/A 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

4229966/A 09/2023

NOTES: (continued)

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12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月