DLP651LE 0.65 WXGA 数字微镜器件

1 特性

- 0.65 英寸对角线微镜阵列
  - WXGA (1280 × 800) 显示分辨率
  - 10.8µm 微镜间距
  - ±12° 微镜倾斜角（相对于平面）
  - 角落照明
- 2×LVDS 输入数据总线
- DLP651LE 芯片组包括：
  - DLP651LE DMD
  - DLPC4430 控制器
  - DLPA100 控制器电源管理和电机驱动器 IC
  - DLPA200 DMD 电源管理 IC

2 应用

- 智能照明
- 企业投影仪
- 教育投影仪

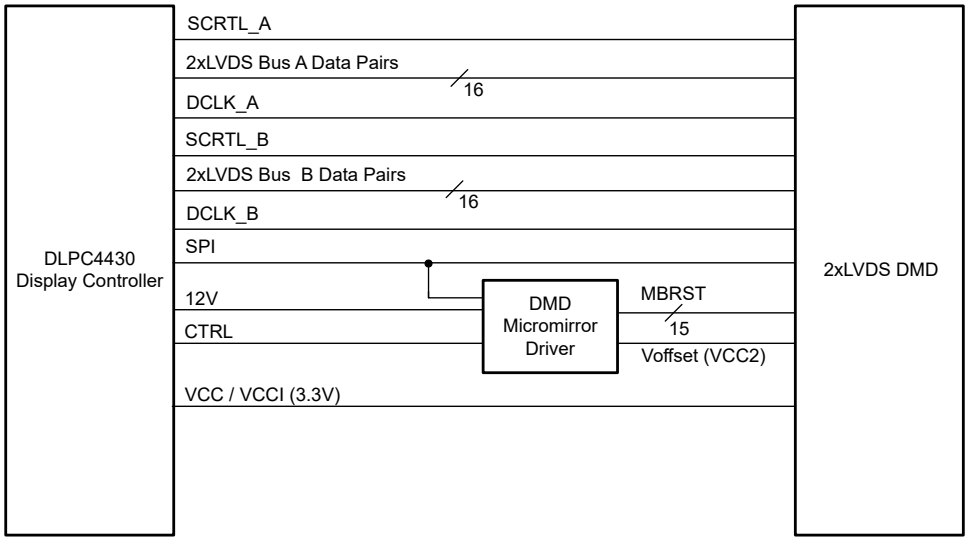
3 说明

DLP651LE 数字微镜器件 (DMD) 是一款数控微机电系统 (MEMS) 空间光调制器 (SLM)，可用于实现经济实惠的 WXGA 显示解决方案。该芯片组由 DLP651LE DMD、DLPC4430 显示控制器、DLPA100 电源和电机驱动器以及 DLPA200 微镜驱动器组成。该芯片组是 -DLP650LE 的成本优化版本，采用-性能增强型密封封装，专为实现需要 16:10 宽高比和出色亮度的应用而设计。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
DLP651LE	FYM (149)	22.30mm × 32.20mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



DLP651LE 简化原理图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Revision History

DATE	REVISION	NOTES
October 2023	*	Initial release

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5 Pin Configuration and Functions

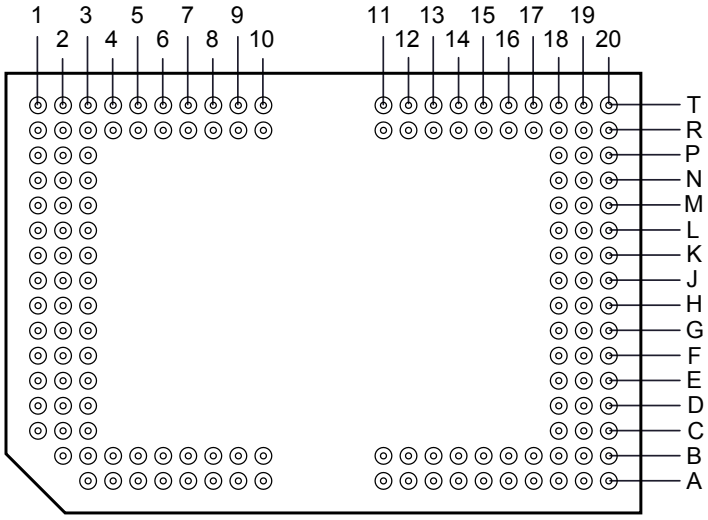


图 5-1. FYM Package 149-Pin CLGA Bottom View

表 5-1. Pin Functions

PIN		NET LENGTH (mils)	SIGNAL	TYPE[1]	DESCRIPTION
NAME	NO.				
DATA INPUTS					
D_AN(1)	G20	711.64	LVDS	I	LVDS pair for Data Bus A
D_AN(3)	H19	711.60			
D_AN(5)	F18	711.60			
D_AN(7)	E18	711.60			
D_AN(9)	C20	711.60			
D_AN(11)	B18	711.60			
D_AN(13)	A20	711.60			
D_AN(15)	B19	711.58			
D_AP(1)	H20	711.66			
D_AP(3)	G19	711.61			
D_AP(5)	G18	711.59			
D_AP(7)	D18	711.60			
D_AP(9)	D20	711.59			
D_AP(11)	A18	711.58			
D_AP(13)	B20	711.59			
D_AP(15)	A19	711.59			

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表 5-1. Pin Functions（续）

PIN		NET LENGTH (mils)	SIGNAL	TYPE[1]	DESCRIPTION
NAME	NO.				
D_BN(1)	K20	711.61	LVDS	I	LVDS pair for Data Bus B
D_BN(3)	J19	711.59			
D_BN(5)	L18	711.59			
D_BN(7)	M18	711.6			
D_BN(9)	P20	711.6			
D_BN(11)	R18	711.59			
D_BN(13)	T20	711.59			
D_BN(15)	R19	711.59			
D_BP(1)	J20	711.61			
D_BP(3)	K19	711.6			
D_BP(5)	K18	711.58			
D_BP(7)	N18	711.58			
D_BP(9)	N20	711.6			
D_BP(11)	T18	711.61			
D_BP(13)	R20	711.59			
D_BP(15)	T19	711.6			
DCLK_AN	D19	711.59		I	LVDS pair for Data Clock A
DCLK_AP	E19	711.59			
DCLK_BN	N19	711.6		I	LVDS pair for Data Clock B
DCLK_BP	M19	711.61			
DATA CONTROL INPUTS					
SCTRL_AN	F20	711.62		I	LVDS pair for Serial Control (Sync) A
SCTRL_AP	E20	711.6			
SCTRL_BN	L20	711.59		I	LVDS pair for Serial Control (Sync) B
SCTRL_BP	M20	711.59			

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表 5-1. Pin Functions（续）

PIN		NET LENGTH (mils)	SIGNAL	TYPE[1]	DESCRIPTION
NAME	NO.				
MICROMIRROR BIAS RESET INPUTS					
MBRST(0)	C3	507.20		I	Non-logic compatible Micromirror Bias Reset signals. Connected directly to the array of pixel micromirrors. Used to hold or release the micromirrors. The bond pads connect to an internal pulldown resistor.
MBRST(1)	D2	576.83			
MBRST(2)	D3	545.78			
MBRST(3)	E2	636.33			
MBRST(4)	G3	618.42			
MBRST(5)	E1	738.25			
MBRST(6)	G2	718.82			
MBRST(7)	G1	777.04			
MBRST(8)	N3	543.29			
MBRST(9)	M2	612.93			
MBRST(10)	M3	580.97			
MBRST(11)	L2	672.43			
MBRST(12)	J3	653.61			
MBRST(13)	L1	764.00			
MBRST(14)	J2	764.37			
MBRST(15)	J1	813.14			
SCP CONTROL					
SCPCLK	A8			I	Serial Communications Port Clock. The bond pad connects to an internal pulldown circuit.
SCPDI	A5			I	Serial Communications Port Data. The bond pad connects to an internal pulldown circuit.
SCPENZ	B7			I	Active low serial communications port enable. The bond pad connects to an internal pulldown circuit.
SCPDO	A9			O	Serial communications port output
OTHER SIGNALS					
EVCC	A3			P	Do not connect on the DLP system board.
MODE_A	A4	415.1		I	Data Bandwidth Mode Select. The bond pad connects to an internal pulldown circuit. Refer to the table for DLP system board connection information.
PWRDNZ	B9	110.38		I	Active Low Device Reset. The bond pad connects to an internal pulldown circuit.
POWER					
V_{CC} [2]	B11, B12, B13, B16, R12, R13, R16, R17			P	Power supply for low voltage CMOS logic. Power supply for normal high voltage at micromirror address electrodes.
V_{CCI} [2]	A12, A14, A16, T12, T14, T16			P	Power supply for low voltage CMOS LVDS interface
V_{OFFSET} [2]	C1, D1, M1, N1			P	Power supply for high voltage CMOS logic. Power supply for stepped high voltage at micromirror address electrodes

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表 5-1. Pin Functions（续）

PIN		NET LENGTH (mils)	SIGNAL	TYPE[1]	DESCRIPTION
NAME	NO.				
V_{SS} (Ground)[3]	A6, A11, A13, A15, A17, B4, B5, B8, B14, B15, B17, C2, C18, C19, F1, F2, F19, H1, H2, H3, H18, J18, K1, K2, L19, N2, P18, P19, R4, R9, R14, R15, T7, T13, T15, T17			P	Common return for all power
RESERVED SIGNALS					
RESERVED_FC	R7	40.64		I	Connect to GND on the DLP system board. The bond pad connects to an internal pulldown circuit.
RESERVED_FD	R8	94.37		I	Connect to GND on the DLP system board. The bond pad connects to an internal pulldown circuit.
RESERVED_PFE	T8	50.74		I	Connect to ground on the DLP system board. The bond pad connects to an internal pulldown circuit.
RESERVED_STM	B6			I	Connect to GND on the DLP system board. The bond pad connects to an internal pulldown circuit.
RESERVED_TP0	R10	93.3		I	Do not connect on the DLP system board.
RESERVED_TP1	T11	263.74		I	Do not connect on the DLP system board.
RESERVED_TP2	R11	281.47		I	Do not connect on the DLP system board.
RESERVED_BA	T10	148.85		O	Do not connect on the DLP system board.
RESERVED_BB	A10	105.28		O	Do not connect on the DLP system board.
RESERVED_RA1	T9			O	Do not connect on the DLP system board.
RESERVED_RB1	A7			O	Do not connect on the DLP system board.
RESERVED_TS	B10	145.42		O	Do not connect on the DLP system board.
RESERVED_A(0)	T2			NC	Do not connect on the DLP system board.
RESERVED_A(1)	T3				
RESERVED_A(2)	R3				
RESERVED_A(3)	T4				
RESERVED_M(0)	R2			NC	Do not connect on the DLP system board.
RESERVED_M(1)	P1			NC	Do not connect on the DLP system board.
RESERVED_S(0)	T1			NC	Do not connect on the DLP system board.
RESERVED_S(1)	R1			NC	Do not connect on the DLP system board.
RESERVED_IRQZ	T6			NC	Do not connect on the DLP system board.
RESERVED_OEZ	R5			NC	Do not connect on the DLP system board.
RESERVED_RSTZ	R6			NC	Do not connect on the DLP system board.
RESERVED_STR	T5			NC	Do not connect on the DLP system board.

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表 5-1. Pin Functions（续）

PIN		NET LENGTH (mils)	SIGNAL	TYPE(1)	DESCRIPTION
NAME	NO.				
RESERVED_STR	T5			NC	Do not connect on the DLP system board.
RESERVED_VB	E3, F3, K3, L3			NC	Do not connect on the DLP system board.
RESERVED_VR	B2, B3, P2, P3			NC	Do not connect on the DLP system board.

(1) I = Input, O = Output, G = Ground, A = Analog, P = Power, NC = No Connect.
(2) Power supply pins required for all DMD operating modes are V_{SS}, V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET}.
(3) V_{SS} must be connected for proper DMD operation.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{CC}	Supply voltage for LVCMOS core logic(2)	–0.5	4	V
V_{CCI}	Supply voltage for LVDS interface(2)	–0.5	4	V
V_{OFFSET}	Micromirror electrode and HVCMOS voltage(2) (3)	–0.5	9	V
V_{MBRST}	Input voltage for MBRST(15:0)(2)	–28	28	V
$\lvert V_{CCI} - V_{CC} \rvert$	Supply voltage delta (absolute value)(4)		0.3	V
INPUT VOLTAGES				
	Input voltage for all other input pins(2)	–0.5	V_{CC} + 0.3	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(5)		700	mV
CLOCKS				
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_A		400	MHz
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_B		400	MHz
ENVIRONMENTAL				
T_{ARRAY}	Temperature, operating(6)	0	90	°C
	Temperature, non-operating(6)	–40	90	°C
T_{DP}	Dew point temperature, operating and non-operating (noncondensing)		81	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET} power supplies are all required for all DMD operating modes.
(3) V_{OFFSET} supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable voltage difference between V_{CC} and V_{CCI} may result in excessive current draw.
(5) The maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(6) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), shown in the figure in 节 7.5 .
(7) V_{OFFSET} supply transients must fall within specified voltages.
(8) Excludes micromirror bias reset inputs MBRST(15:0).

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6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	– 40	80	°C
T_{DP-AVG}	Average dew point temperature (non-condensing) (1)		28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

SYMBOL	PARAMETER	DESCRIPTION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	V
$V_{(ESD)}$	Electrostatic discharge (MBRST PINS)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±150	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	Supply voltage for LVCMOS core logic(1)	3.0	3.3	3.6	V
V_{CCI}	Supply voltage for LVDS Interface(1)	3.0	3.3	3.6	V
V_{OFFSET}	Micromirror Electrode and HVCMOS voltage(1) (2)	8.25	8.5	8.75	V
V_{MBRST}	Micromirror Bias / Reset Voltage(1)	– 27		26.5	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage delta (absolute value)(3)		0	0.3	V
LVCMOS INTERFACE					
V_{IH}	Input High Voltage	1.7	2.5	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	– 0.3		0.7	V
I_{OH}	High Level Output Current			– 20	mA
I_{OL}	Low Level Output Current			15	mA
t_{PWRDNZ}	PWRDNZ pulse width(4)	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency(5)	50		500	kHz
t_{SCP_PD}	Propagation delay, clock to Q, from rising-edge of SCPCLK to valid SCPDO(6)	0		900	ns
t_{SCP_DS}	SCPDI clock setup time (before SCPCLK falling-edge)(6)	800			ns
t_{SCP_DH}	SCPDI hold time (after SCPCLK falling-edge)(6)	900			ns
$t_{SCP_NEG_ENZ}$	Time between falling-edge of SCPENZ and the rising-edge of SCPCLK(5)	1			us
SCP_POS_ENZ	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			us

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6.4 Recommended Operating Conditions（续）

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
$t_{SCP_OUT_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tristate)			192/f_{DCLK}	s
$t_{SCP_PW_ENZ}$	SCPENZ inactive pulse width (high level)	1			1/f_{scpclk}
t_r	Rise time (20% to 80%)			200	ns
t_f	Fall time (80% to 20%)			200	ns
LVDS INTERFACE					
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK(7)		320	330	MHz
$\|V_{ID}\|$	Input differential voltage (absolute value)(8)	100	400	600	mV
V_{CM}	Common mode voltage(8)		1200		mV
V_{LVDS}	LVDS voltage(8)	0		2000	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			10	ns
Z_{IN}	Internal differential termination resistance	95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operational(9) (10) (11)	10		40 to 70(12)	°C
	Array temperature, short-term operational(10) (13)	0		10	°C
$T_{DP\ -AVG}$	Average dew point average temperature (non-condensing)(14)			28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(15)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
Q_{AP-ILL}	Window aperture illumination overfill (16)			17	W/cm^2
SOLID STATE ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 410 nm(9) (18)			10	mW/cm^2
ILL_{VIS}	Illumination power at wavelengths ⩾ 410 nm and ⩽800 nm (17) (18)			33.5	W/cm^2
ILL_{IR}	Illumination power at wavelengths > 800 nm (18)			10	mW/cm^2
ILL_{BLU}	Illumination power at wavelengths ⩾ 410 nm and ⩽ 475 nm (17) (18)			10.6	W/cm^2
ILL_{BLU1}	Illumination power at wavelengths ⩾ 410 nm and ⩽ 440 nm (17) (18)			1.7	W/cm^2
LAMP ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 395 nm(9) (18)			2	mW/cm^2
ILL_{VIS}	Illumination power at wavelengths ⩾ 395 nm and ⩽ 800 nm (17) (18)			23.5	W/cm^2
ILL_{IR}	Illumination power at wavelengths > 800 nm (18)			10	mW/cm^2

(1) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(2) V_{OFFSET} supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta $|V_{CCI} - V_{CC}|$ must be less than the specified limit. See 节 10 and 图 10-1.
(4) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.
(5) The SCP clock is a gated clock. Duty cycle must be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(6) See 图 6-3.
(7) See LVDS Timing Requirements in 节 6.7 and 图 6-7.
(8) See 图 6-6 LVDS Waveform Requirements.
(9) Simultaneous exposure of the DMD to the maximum 节 6.4 for temperature and UV illumination will reduce device lifetime.

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(10) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 图 7-1 and the package thermal resistance using 节 7.5.
(11) Long-term is defined as the usable life of the device.
(12) Per 图 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See 节 7.8 for a definition of micromirror landed duty cycle.
(13) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
(14) The average over time (including storage and operating) that the device is not in the "elevated dew point temperature range."
(15) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(16) Light illuminating the critical area on the window aperture shown in 图 6-2 should be limited to a maximum of Q_{AP-ILL}.
(17) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
(18) To calculate, see Micromirror Power Density Calculation.

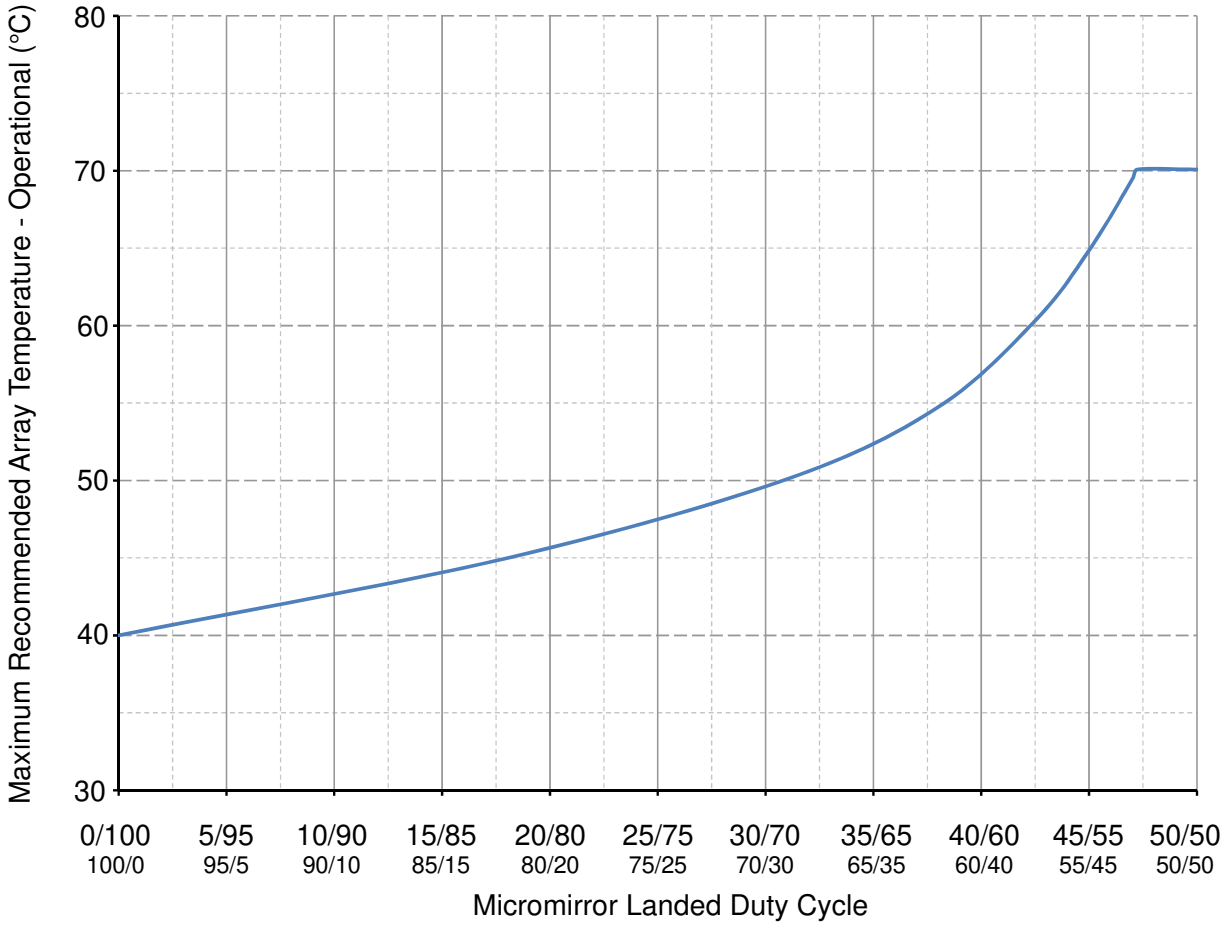


图 6-1. Maximum Recommended Array Temperature—Derating Curve

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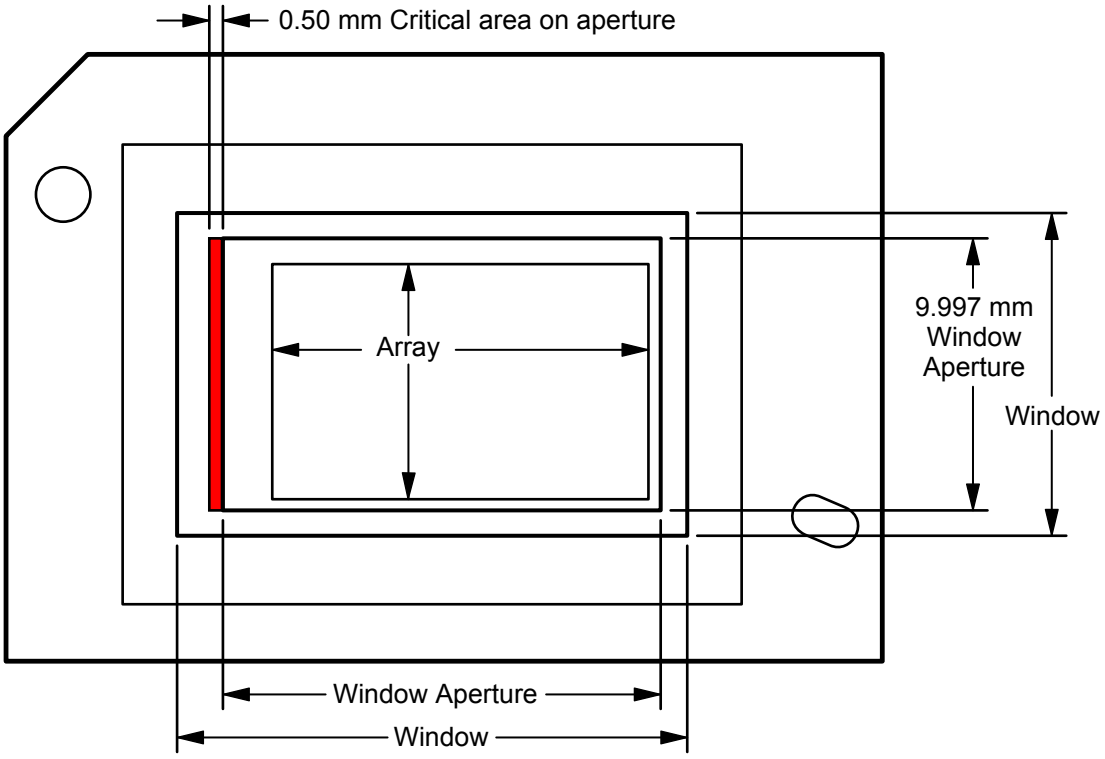


图 6-2. Illumination Overfill Diagram—Critical Area

6.5 Thermal Information

THERMAL METRIC	DLP651LE FYM Package 149 PINS	UNIT
Thermal resistance, active area to test point 1 (TP1)(1)	0.50	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the 节 6.4.
The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.
Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

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6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	V_{CC} = 3 V, I_{OH} = – 20 mA	2.4			V
V_{OL}	Low level output voltage	V_{CC} = 3.6 V, I_{OL} = 15 mA			0.4	V
I_{OZ}	High impedance output current	V_{CC} = 3.6 V			10	µA
I_{IL}	Low level input current	V_{CC} = 3.6 V, VI = 0			– 60	µA
I_{IH}	High level input current (1)	V_{CC} = 3.6 V, VI = V_{CC}			200	µA
I_{CC}	Supply current VCC (2)	V_{CC} = 3.6 V			479	mA
I_{CCI}	Supply current VCCI (2)	V_{CCI} = 3.6 V			309	mA
I_{OFFSET}	Supply current VOFFSET (3)	V_{OFFSET} = 8.75 V			25	mA
Z_{IN}	Internal differential termination resistance		95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)		90	100	110	Ω
C_I	Input capacitance(1)	f = 1 MHz			10	pF
C_O	Output capacitance(1)	f = 1 MHz			10	pF
C_{IM}	Input capacitance for MBRST[0:15] pins	f = 1 MHz	200		330	pF

(1) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins
(2) To prevent excess current, the supply voltage delta $|V_{CCI} - V_{CC}|$ must be less than the specified limit in 节 6.4.
(3) To prevent excess current, the supply voltage delta $|V_{BIAS} - V_{OFFSET}|$ must be less than the specified limit in 节 6.4.

6.7 Timing Requirements

Over Recommended Operating Conditions (unless otherwise noted).

PARAMETER DESCRIPTION		SIGNAL	MIN	TYP	MAX	UNIT
LVDS (1)						
t_C	Clock cycle duration for DCLK_A	LVDS	3.03			ns
t_C	Clock cycle duration for DCLK_B	LVDS	3.03			ns
t_W	Pulse duration for DCLK_A	LVDS	1.36	1.52		ns
t_W	Pulse duration for DCLK_B	LVDS	1.36	1.52		ns
t_{SU}	Setup time for D_A(15:0) before DCLK_A	LVDS	0.35			ns
t_{SU}	Setup time for D_A(15:0) before DCLK_B	LVDS	0.35			ns
t_{SU}	Setup time for SCTRL_A before DCLK_A	LVDS	0.35			ns
t_{SU}	Setup time for SCTRL_B before DCLK_B	LVDS	0.35			ns
t_H	Hold time for D_A(15:0) after DCLK_A	LVDS	0.35			ns
t_H	Hold time for D_B(15:0) after DCLK_B	LVDS	0.35			ns
t_H	Hold time for SCTRL_A after DCLK_A	LVDS	0.35			ns
t_H	Hold time for SCTRL_B after DCLK_B	LVDS	0.35			ns
t_{SKEW}	Channel B relative to Channel A(2) (3)	LVDS	– 1.51		1.51	ns

(1) See *Timing Requirements* for timing requirements for LVDS.
(2) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15:0) and D_AP(15:0)
(3) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15:0) and D_BP(15:0)

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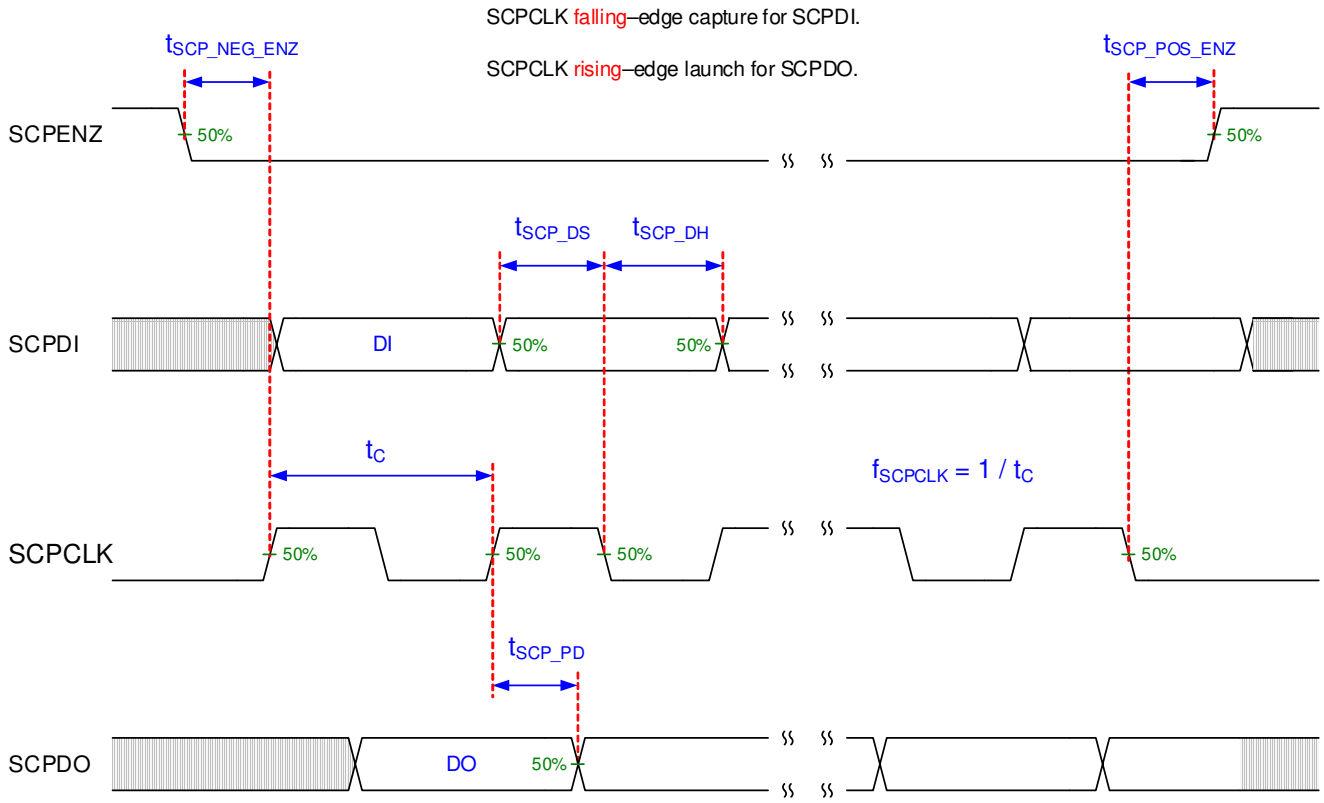
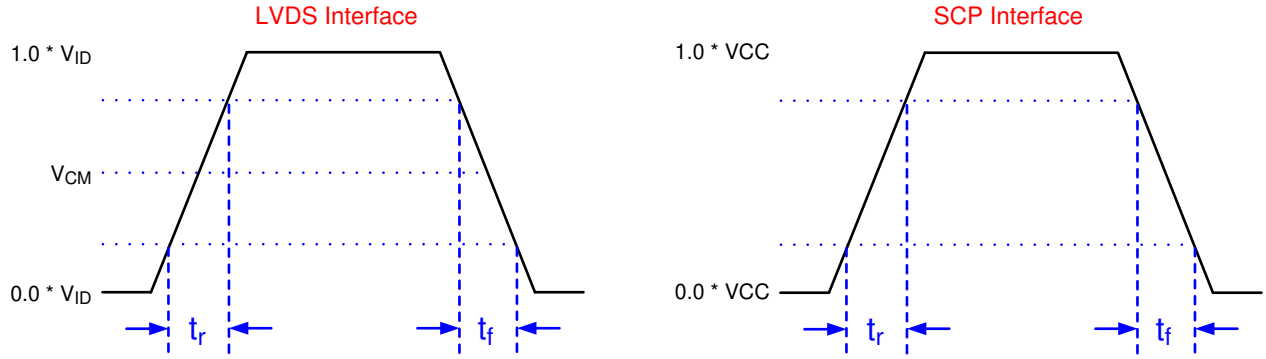


图 6-3. SCP Timing Requirements

See *Recommended Operating Conditions* for f_{SCPCLK}, t_{SCP_DS}, t_{SCP_DH}, and t_{SCP_PD} specifications.

See *Recommended Operating Conditions* for t_r and t_f specifications and conditions.



Not to scale.

Refer to the *Timing Requirements*.

Refer to the *Pin Functions* for list of LVDS pins and SCP pins.

图 6-4. Rise Time and Fall Time

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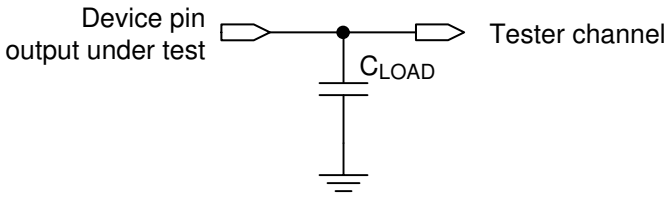


图 6-5. Test Load Circuit for Output Propagation Measurement

For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. See Test Load Circuit for Output Propagation Measurement.

Not to Scale

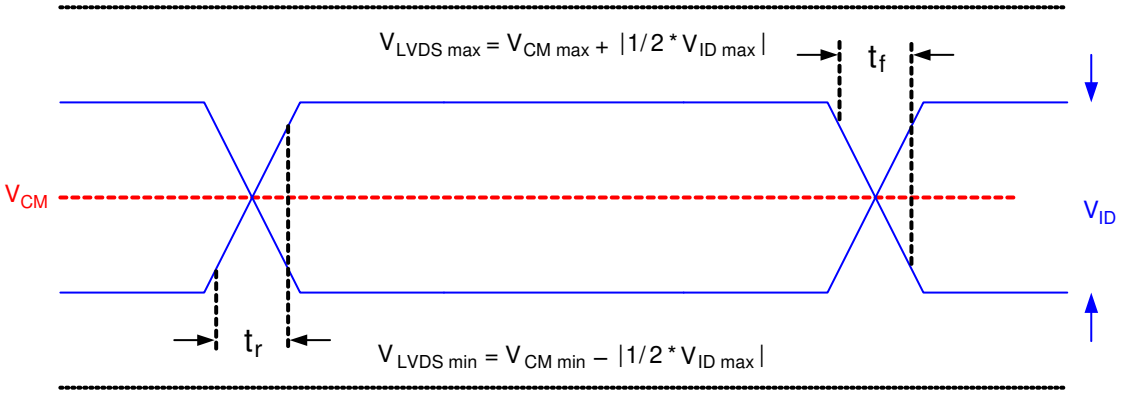


图 6-6. LVDS Waveform Requirements

See *Recommended Operating Conditions* for V_{CM}, V_{ID}, and V_{LVDS} specifications and conditions.

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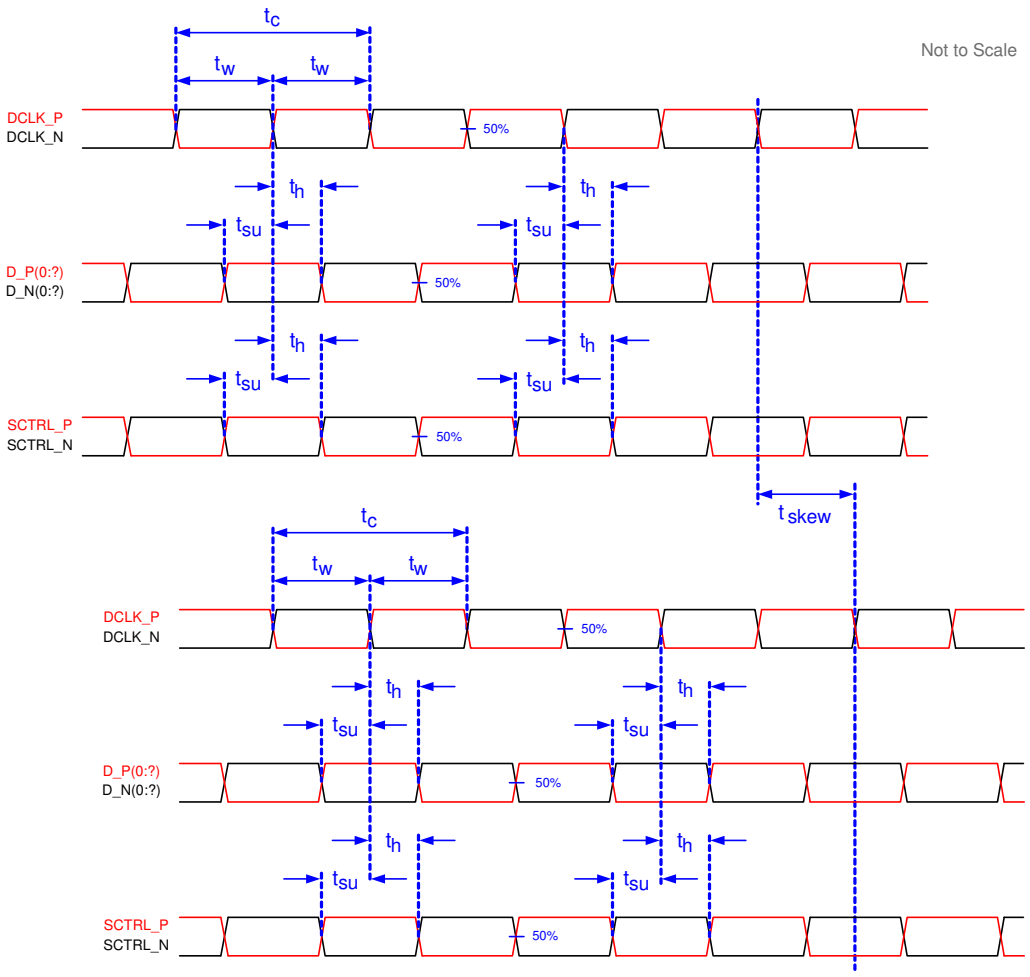


图 6-7. Timing Requirements

See *Timing Requirements* for timing requirements and LVDS pairs per channel (bus) defining D_P(0:x) and D_N(0:x).

6.8 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
When loads are applied on both electrical and thermal interface areas				
Maximum load to be applied to the electrical interface area(1)			111	N
Maximum load to be applied to the thermal interface area(1)			111	N
When load is applied on the electrical interface area only				
Maximum load to be applied to the electrical interface area(1)			222	N
Maximum load to be applied to the thermal interface area(1)			0	N

(1) The load must be uniformly applied in the corresponding areas shown in the figure below.

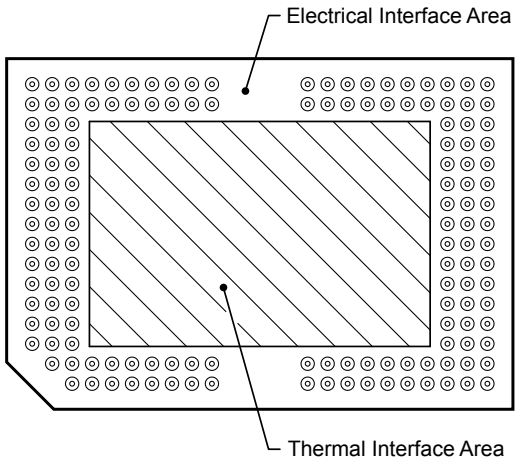


图 6-8. System Mounting Interface Loads

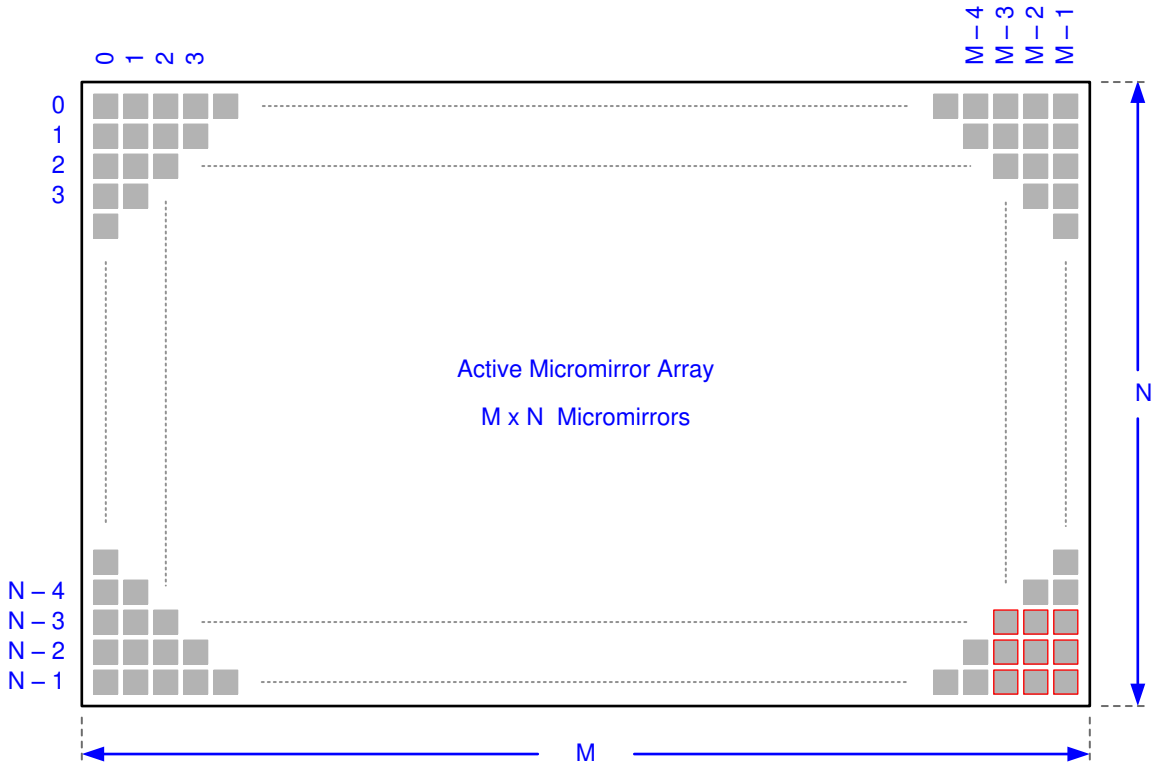
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6.9 Micromirror Array Physical Characteristics

表 6-1. Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns (1)	M	1280	micromirrors
Number of active rows (1)	N	800	
Micromirror (pixel) pitch (1)	P	10.8	µm
Micromirror active array width (1)	Micromirror pitch × number of active columns	13.824	mm
Micromirror active array height (1)	Micromirror pitch × number of active rows	8.640	mm
Micromirror active border size(2)	Pond of Micromirror (POM)	10	micromirrors / side

(1) See 图 6-9.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the *Pond Of Mirrors* (POM). These micromirrors are structurally or electrically prevented from tilting toward the bright or “on” state but still require an electrical bias to tilt toward “off.”



Pond Of Micromirrors (POM) omitted for clarity.

Details omitted for clarity. Not to scale.

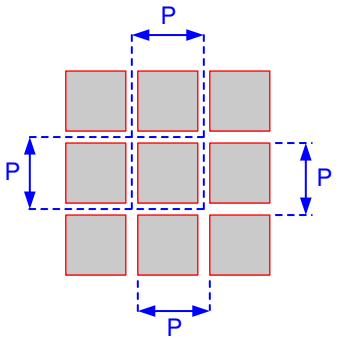


图 6-9. Micromirror Array Physical Characteristics

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Refer to 节 6.9 table for M, N, and P specifications.

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6.10 Micromirror Array Optical Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micromirror tilt angle (2) (3) (4) (5)		landed state (1)	11	12	13	Degrees
Micromirror crossover time (6)		typical performance		3		µs
Micromirror switching time (7)		typical performance	10			µs
DMD Efficiency (420 nm – 680 nm) (8)				68		%
Image performance	Bright pixel(s) in active area (9)	Gray 10 screen (12)			0	Micromirrors
	Bright pixel(s) in the POM (9) (11)	Gray 10 screen (12)			1	
	Dark pixel(s) in the active area (10)	White screen (13)			4	
	Adjacent pixel(s) (14)	Any screen			0	
	Unstable pixel(s) in active area (15)	Any screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(4) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(5) Refer to 图 6-10.
(6) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(7) The minimum time between successive transitions of a micromirror.
(8) Efficiency numbers assume 24-degree illumination angle, F/2.4 illumination and collection cones, uniform source spectrum, and uniform pupil illumination. Efficiency numbers assume 100% electronic micromirror duty cycle and do not include optical overfill loss. The efficiency is measured photopically. Note that this number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.
(9) Bright pixel definition: a single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(10) Dark pixel definition: a single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(11) POM definition: rectangular border of off-state mirrors surrounding the active area
(12) Gray 10 screen definition: a full screen with RGB values set to R = 10/255, G = 10/255, B = 10/255
(13) White screen definition: a full screen with RGB values set to R=255/255, G = 255/255, B = 255/255
(14) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
(15) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

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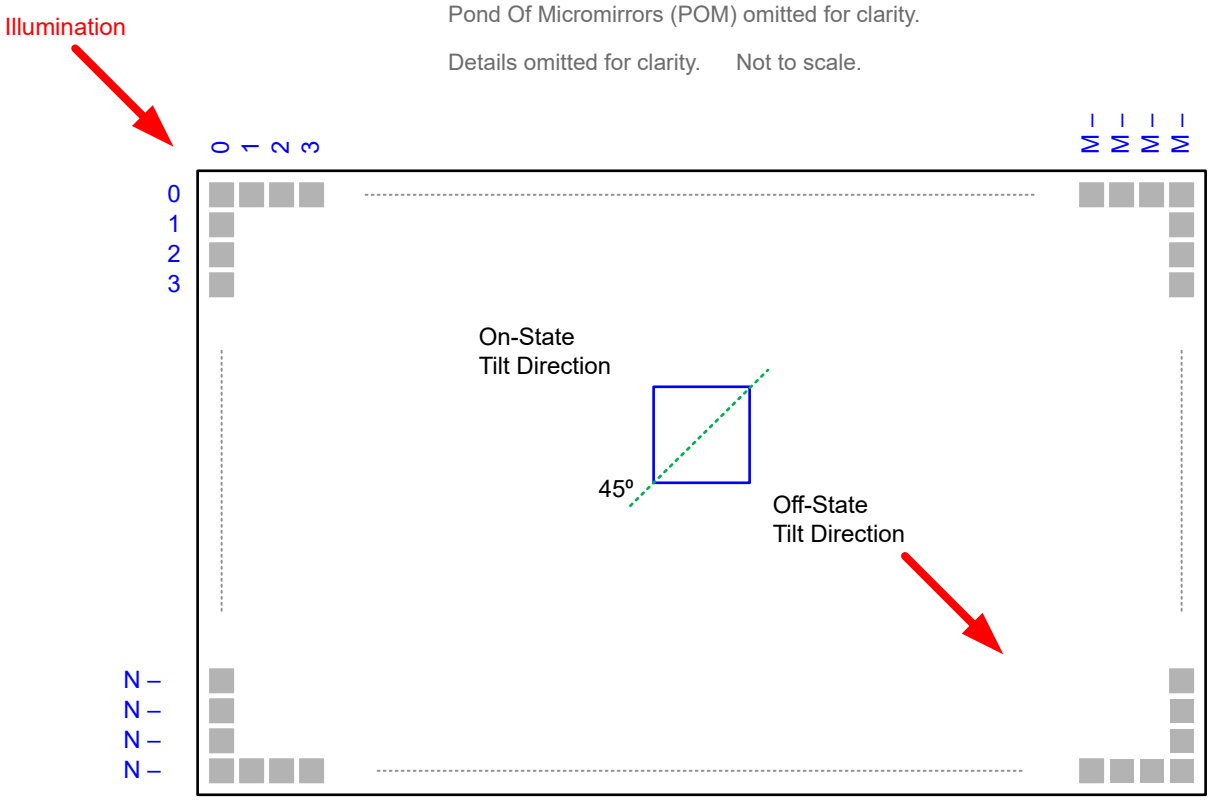


图 6-10. Micromirror Landed Orientation and Tilt

Refer to 节 6.9 table for M, N, and P specifications.

6.11 Window Characteristics

表 6-2. DMD Window Characteristics

PARAMETER	NOM
Window material	Corning Eagle XG
Window Refractive Index at 546.1 nm	1.5119

6.12 Chipset Component Usage Specification

Reliable function and operation of the DLP651LE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

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7 Detailed Description

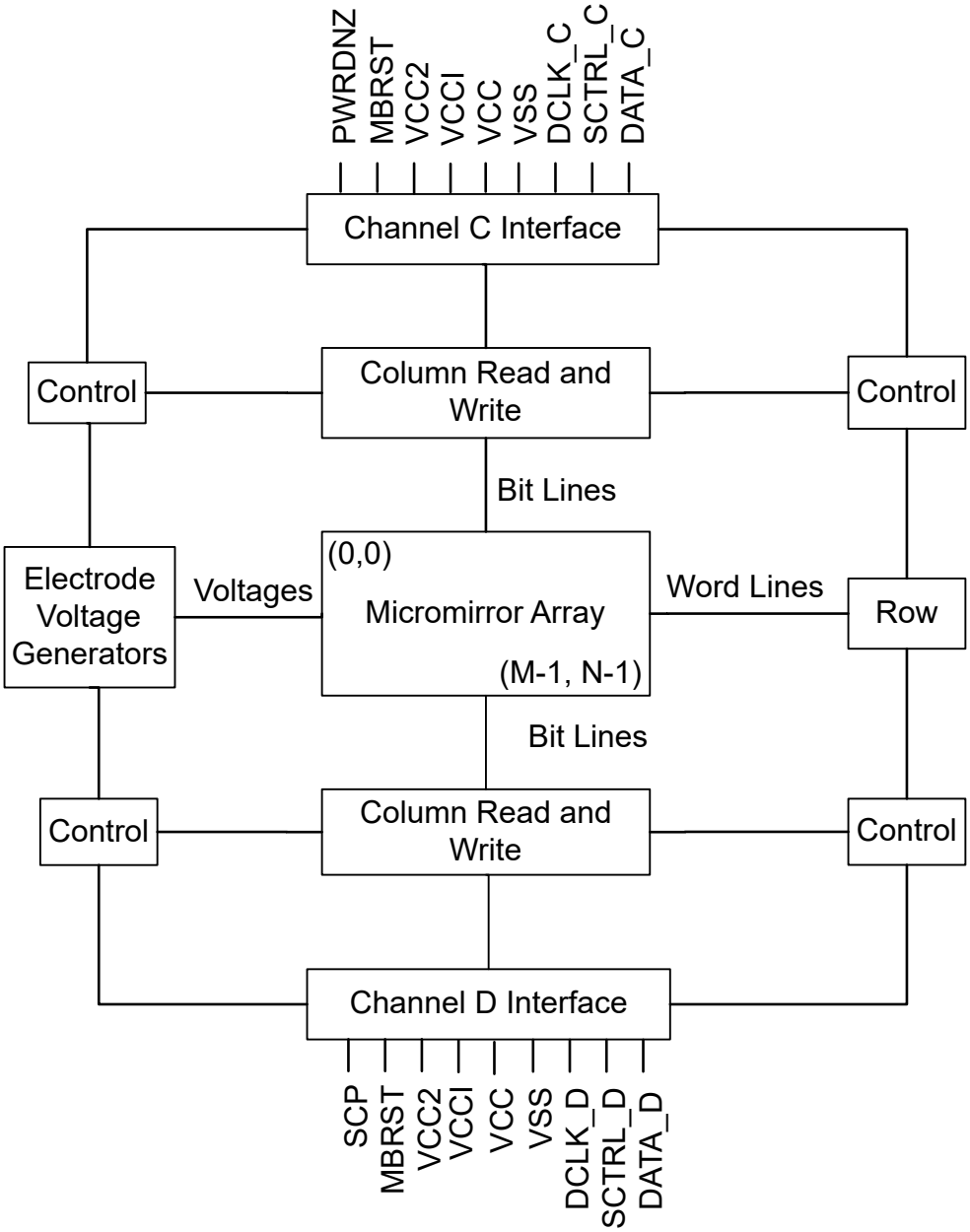
7.1 Overview

The DMD is a 0.65-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the 节 7.2. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP651LE DMD is part of the chipset comprising of the DLP651LE DMD, the DLPC4430 display controller, the DLPA100 power and motor driver and the DLPA200 micromirror driver. To ensure reliable operation, the DLP651LE DMD must always be used with the DLPC4430 display controller, the DLPA100 power and motor driver and the DLPA200 micromirror driver.

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7.2 Functional Block Diagram



For pin details on Channels A, B refer to *Pin Configuration and Functions* and LVDS Interface section of *Timing Requirements*.

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7.3 Feature Description

7.3.1 Power Interface

The DMD requires 3 DC voltages: DMD_P3P3V, V_{OFFSET}, and MBRST. DMD_P3P3V is created by the DLPA100 power and motor driver and the DLPA200 DMD micromirror driver. Both the DLPA100 and DLPA200 create the main DMD voltages, as well as powering various peripherals (TMP411, I^2C, and TI level translators). DMD_P3P3V provides the V_{CC} voltage required by the DMD. V_{OFFSET} (8.5V) and MBRST are made by the DLPA200 and are supplied to the DMD to control the micromirrors.

7.3.2 Timing

This data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. 图 6-5 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. System optical performance and image quality strongly relate to optical system design parameter trade offs. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.4.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation, and objectionable artifacts in the display’s border and/or active area could occur.

7.4.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display’s border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.4.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

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7.5 Micromirror Array Temperature Calculation

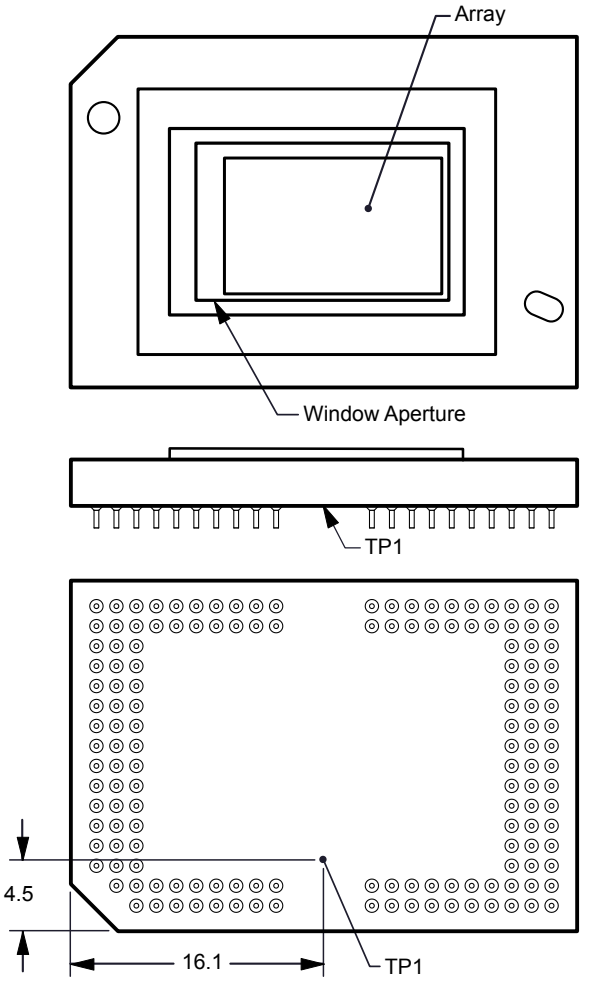


图 7-1. DMD Thermal Test Points

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Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in 图 7-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in 节 6.5 from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal Electrical Power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.42

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 1.5 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{INCIDENT} = 45 \text{ W (measured)} \quad (3)$$

$$T_{CERAMIC} = 55.0°C$$

$$Q_{ELECTRICAL} = 1.5 \text{ W}$$

$$Q_{ARRAY} = 1.5 \text{ W} + (0.42 \times 45 \text{ W}) = 20.4 \text{ W}$$

$$T_{ARRAY} = 55.0°C + (20.4 \text{ W} \times 0.50°C/W) = 65.2 °C$$

7.6 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL}$ (mW/cm^2)
- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL}$ (mW/cm^2)
- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})$ (cm^2)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)

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- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm^2) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV\text{-}RATIO}$ = ratio of the optical power for wavelengths <410 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS\text{-}RATIO}$ = ratio of the optical power for wavelengths ⩾410 and ⩽800 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR\text{-}RATIO}$ = ratio of the optical power for wavelengths >800 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU\text{-}RATIO}$ = ratio of the optical power for wavelengths ⩾410 and ⩽475 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1\text{-}RATIO}$ = ratio of the optical power for wavelengths ⩾410 and ⩽440 nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$$Q_{INCIDENT} = 45 \text{ W (measured)} \quad (4)$$

$$A_{ARRAY} = (13.824 \text{ mm} \times 8.640 \text{ mm}) \div 100 = 1.1944 \text{ cm}^2 \text{ (data sheet)} \quad (5)$$

$$OV_{ILL} = 16.3\% \text{ (optical model)} \quad (6)$$

$$OP_{UV\text{-}RATIO} = 0.00017 \text{ (spectral measurement)} \quad (7)$$

$$OP_{VIS\text{-}RATIO} = 0.99977 \text{ (spectral measurement)} \quad (8)$$

$$OP_{IR\text{-}RATIO} = 0.00006 \text{ (spectral measurement)} \quad (9)$$

$$OP_{BLU\text{-}RATIO} = 0.28100 \text{ (spectral measurement)} \quad (10)$$

$$OP_{BLU1\text{-}RATIO} = 0.03200 \text{ (spectral measurement)} \quad (11)$$

$$A_{ILL} = 1.1944 \text{ cm}^2 \div (1 - 0.163) = 1.4270 \text{ cm}^2 \quad (12)$$

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$$ILL_{UV} = [0.00017 \times 45\ W] \times 1000 \div 1.4270\ cm^2 = 5.361\ mW/cm^2 \quad (13)$$

$$ILL_{VIS} = [0.99977 \times 45\ W] \div 1.4270\ cm^2 = 31.53\ W/cm^2 \quad (14)$$

$$ILL_{IR} = [0.00006 \times 45\ W] \times 1000 \div 1.4270\ cm^2 = 1.892\ mW/cm^2 \quad (15)$$

$$ILL_{BLU} = [0.28100 \times 45\ W] \div 1.4270\ cm^2 = 8.86\ W/cm^2 \quad (16)$$

$$ILL_{BLU1} = [0.03200 \times 45\ W] \div 1.4270\ cm^2 = 1.01\ W/cm^2 \quad (17)$$

7.7 Window Aperture Illumination Overfill Calculation

The amount of optical overfill on the critical area of the window aperture cannot be measured directly. For systems with uniform illumination on the array the amount is determined using the total measured incident optical power on the DMD, and the ratio of the total optical power on the DMD that is on the defined critical area. The optical model is used to determine the percent of optical power on the window aperture critical area and estimate the size of the area.

- $Q_{AP\text{-}ILL} = [Q_{INCIDENT} \times OP_{AP_ILL_RATIO}] \div A_{AP_ILL}\ (W/cm^2)$

where:

- $Q_{AP\text{-}ILL}$ = window aperture illumination overfill (W/cm^2)
- $Q_{INCIDENT}$ = total incident optical power on the DMD (Watts) (measured)
- $OP_{AP_ILL_RATIO}$ = ratio of the optical power on the critical area of the window aperture to the total optical power on the DMD (optical model)
- $A_{AP\text{-}ILL}$ = size of the window aperture critical area (cm^2) (datasheet)
- OP_{CA_RATIO} = percent of the window aperture critical area with incident optical power (%) (optical model)

Sample calculation:

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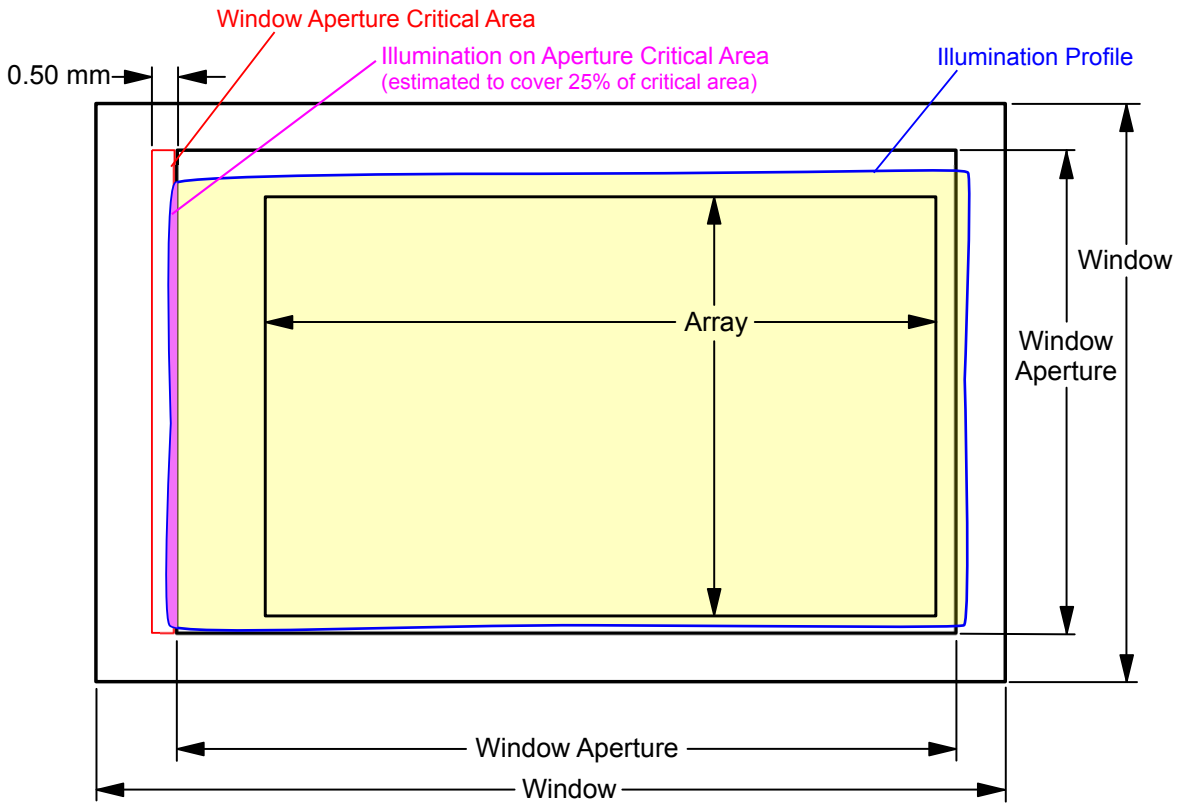


图 7-2. Window Aperture Overfill Example

See the figure for the length of the critical aperture.

$Q_{INCIDENT}$ = 45 W (measured) (18)

$OP_{AP_ILL_RATIO}$ = 0.312% (optical model) (19)

OV_{CA_RATIO} = 25% (optical model) (20)

Length of the window aperture for critical area = 0.9997 (data sheet) (21)

Width of critical area = 0.050 cm (data sheet) (22)

$A_{AP\text{-}ILL}$ = 0.99977 cm × 0.050 cm = 0.049989 (cm^2) (23)

$Q_{AP\text{-}ILL}$ = (45 × 0.00312) ÷ (0.049989 × 0.25) = 11.2 (W/cm^2) (24)

7.8 Micromirror Landed-On/Landed-Off Duty Cycle

7.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

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As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time (and in the Off state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in 图 6-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature at a given long-term average Landed Duty Cycle.

7.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

表 7-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30

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表 7-1. Grayscale Value and Landed Duty Cycle
（续）

GRAYSCALE VALUE	LANDED DUTY CYCLE
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

- Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

Where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point. (1)

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, and blue color intensities would be as shown in 表 7-2 and 表 7-3.

表 7-2. Example Landed Duty Cycle for Full-Color, Color Percentage

RED CYCLE	GREEN CYCLE	BLUE CYCLE
50%	20%	30%

表 7-3. Example Landed Duty Cycle for Full-Color

RED SCALE	GREEN SCALE	BLUE SCALE	LANDED DUTY CYCLE
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

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8 Application and Implementation

备注

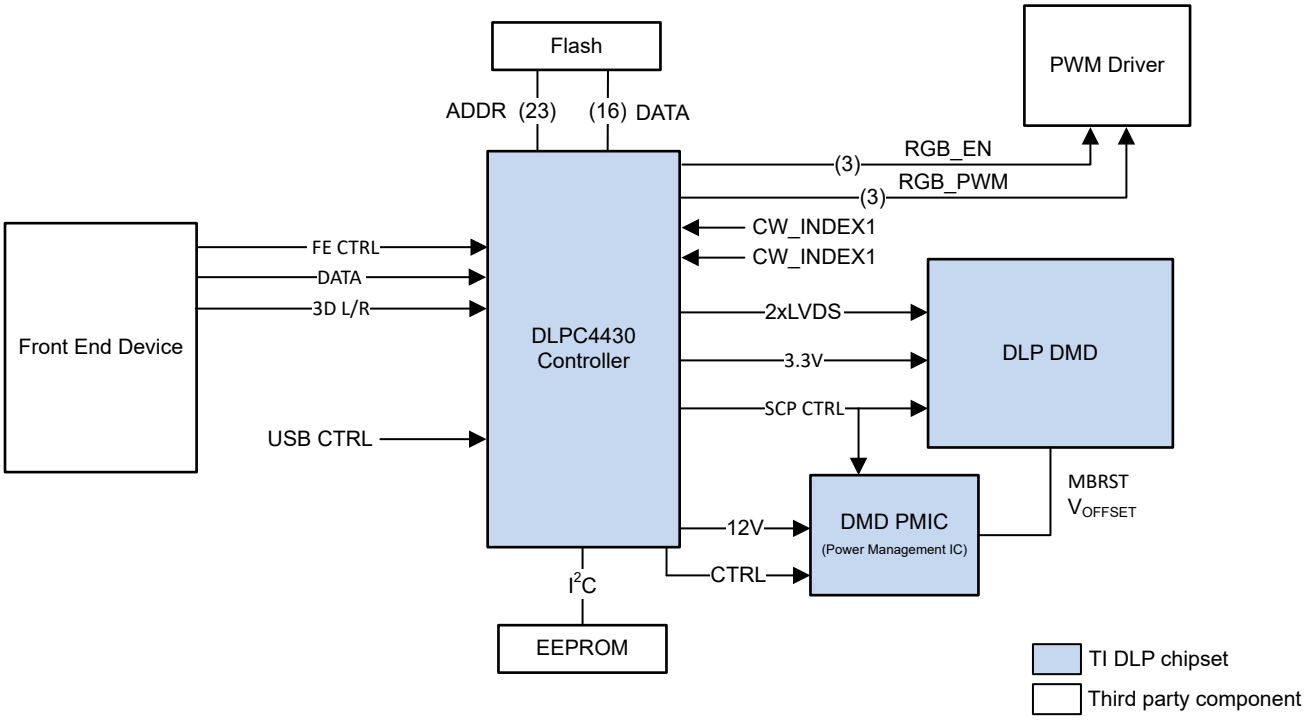
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8.1 Application Information

Texas Instruments DLP technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, either towards the projection optics, or the collection optics. The large micromirror array size and ceramic package provides great thermal performance for bright display applications. Typical applications using the DLP651LE include education projectors, and business projectors.

8.2 Typical Application

The DLP651LE digital micromirror device (DMD), combined with a DLPC4430 digital controller, DLPA100 power management device, and DLPA200 micromirror driver provides WXGA resolution for bright, colorful display applications. A typical display system that uses the DLP651LE and additional system components is shown in 图 8-1.



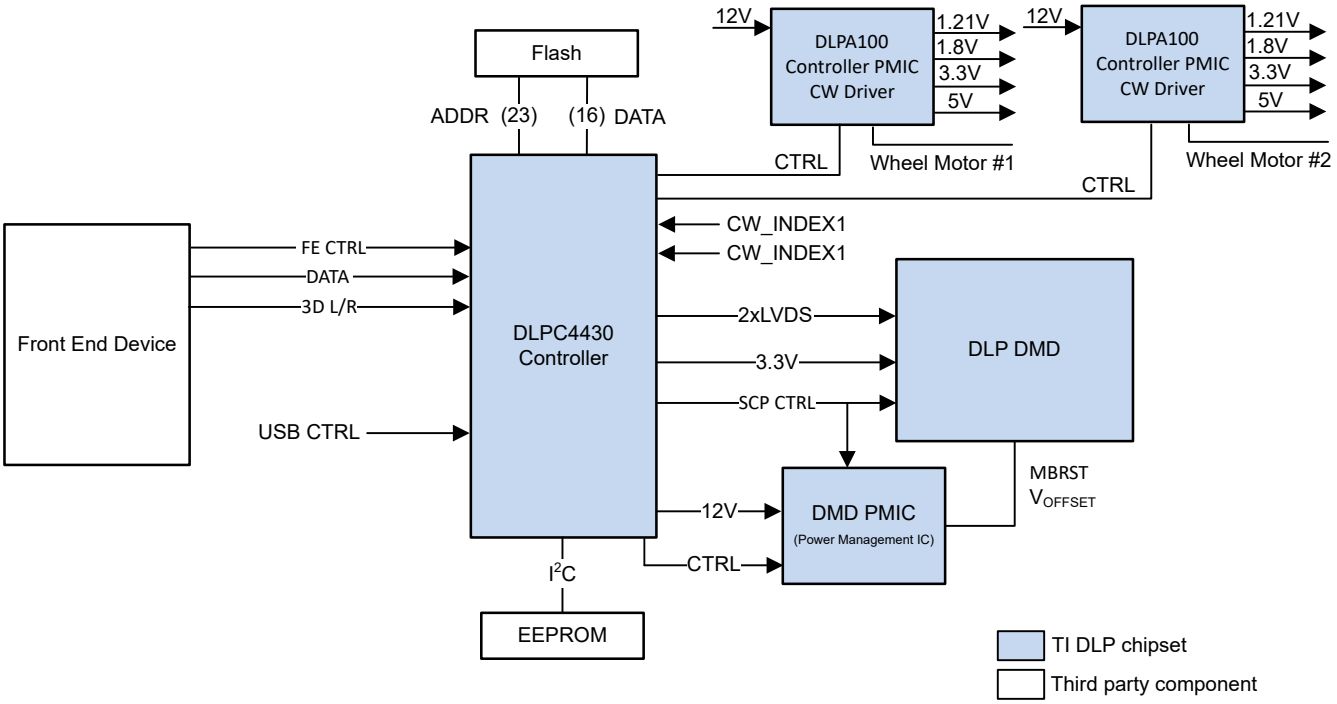


图 8-1. Typical DLPC4430 Application (LED, Top; LPCW, Bottom)

8.2.1 Design Requirements

The DLP 0.65 WXGA chipset can be used to create an efficient projection system. This chipset includes the DLP651LE, DLPC4430, DLPA100, and the DLPA200. The DLP651LE is used as the core imaging device in the display system and contains a 0.65-inch array of micromirrors. The DLPC4430 controller is the digital interface between the DMD and the rest of the system. The controller drives the DMD by taking the converted source data from the front end receiver and transmitting it to the DMD over a high speed interface. The DLPA100 power management device provides voltage regulators for the controller and colorwheel motor control. The DLPA200 provides the power and sequencing to drive the DLP651LE. To ensure reliable operation, the DLP651LE DMD must always be used with the DLPC4430 display controller, a DLPA100 PMIC driver, and a DLPA200 DMD micromirror driver.

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The illumination source options include lamp, LED, laser, or laser phosphor. The type of illumination used and desired brightness will have a major effect on the overall system design and size.

8.2.2 Detailed Design Procedure

For help connecting the DLPC4430 display controller and the DLP651LE DMD, see the reference design schematic. For a complete DLP system, an optical module or light engine is required that contains the DLP651LE DMD, associated illumination sources, optical elements, and necessary mechanical components. The optical module is typically supplied by an optical OMM (optical module manufacturer) who specializes in designing optics for DLP projectors.

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8.2.3 Application Curves

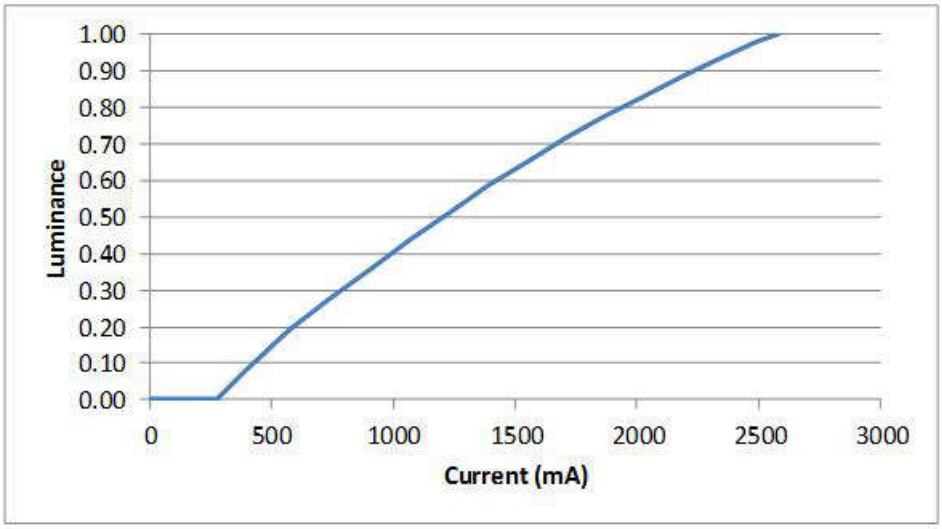


图 8-2. Luminance vs. Current

9 Layout

9.1 Layout Guidelines

The DLP651LE DMD is part of a chipset controlled by the DLPC4430 display controller in conjunction with the DLPA100 power and motor driver. These guidelines help to design a PCB board with the DLP651LE DMD. The DLP651LE DMD board is a high-speed multilayer PCB, with primarily high-speed digital logic with dual edge clock rates up to 400 MHz for DMD LVDS signals. The remaining traces comprise low-speed digital LVTTL signals. Use mini power planes for VOFFSET and MBRST[0:15]. Solid planes are required for DMD_P3P3V (3.3 V) and ground. The target impedance for the PCB is 50 Ω ±10% with the LVDS traces being 100 Ω ±10% differential. Use an 8-layer stack-up as described in 表 9-1.

9.2 Layout Example

9.2.1 Layers

表 9-1 shows the layer stack-up and copper weight for each layer. Small subplanes are allowed on signal routing layers to connect components to major subplanes on top/bottom layers if necessary.

表 9-1. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT.	COMMENTS
1	Side A—DMD only	1.5 oz	DMD, escapes, low frequency signals, power subplanes
2	Ground	1 oz	Solid ground plane (net GND)
3	Signal	0.5 oz	50-Ω and 100-Ω differential signals
4	Ground	1 oz	Solid ground plane (net GND)
5	DMD_P3P3V	1 oz	+3.3-V power plane (net DMD_P3P3V)
6	Signal	0.5 oz	50-Ω and 100-Ω differential signals
7	Ground	1 oz	Solid ground plane (net GND)
8	Side B—all other components	1.5 oz	Discrete components, low frequency signals, power subplanes

9.2.2 Impedance Requirements

TI recommends the board have matched impedance of 50 Ω ±10% for all signals. The following table lists the exceptions.

表 9-2. Special Impedance Requirements

SIGNAL TYPE	SIGNAL NAME	IMPEDANCE (Ω)
A channel LVDS differential pairs	D_AP(0:15), D_AN(0:15)	100 ±10% differential across each pair
	DCLK_AP, DCLK_AN	
	SCTRL_AP, SCTRL_AN	
B channel LVDS differential pairs	D_BP(0:15), D_BN(0:15)	100 ±10% differential across each pair
	DCLK_BP, DCLK_BN	
	SCTRL_BP, SCTRL_BN	

9.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends all signals follow the 0.005-inch/0.005-inch design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1-inch minimum. Actual trace widths and clearances will be determined based on an analysis of impedance and stack-up requirements.

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10 Power Supply Recommendations

The following power supplies are all required to operate the DMD: V_{SS}, V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET}. DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

备注

CAUTION: For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See 图 10-1—DMD Power Supply Sequencing Requirements.

V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Common ground V_{SS} must also be connected.

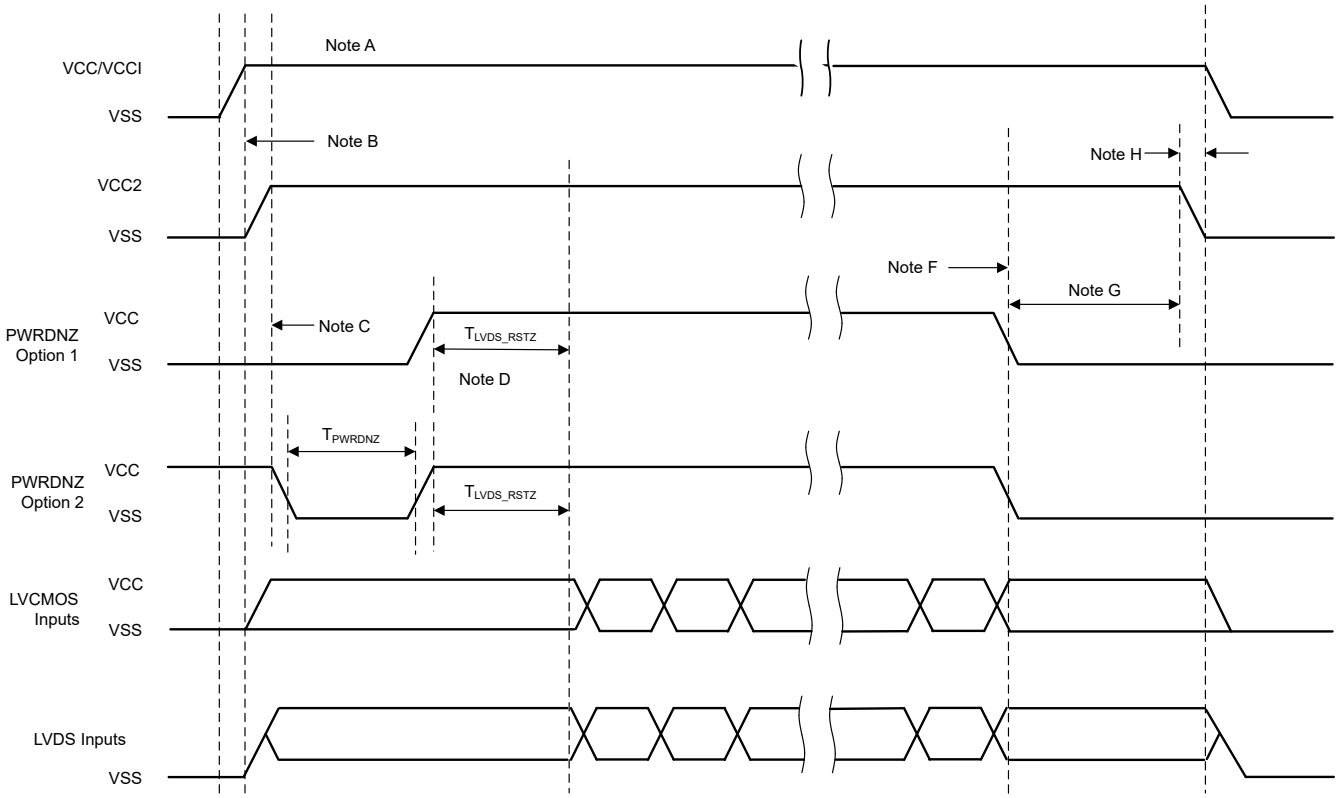
10.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{CC} and V_{CCI} must always start and settle before V_{OFFSET} plus the first time delay period (t_{D1}). V_{BIAS} and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in 节 6.4.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in 节 6.1, in 节 6.4, and in 图 10-1.
- During power-up, LVCMOS input pins must not be driven high until after V_{CC} and V_{CCI} have settled at operating voltages listed in 节 6.4.

10.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{CC} and V_{CCI} must be supplied until after V_{CC2} is discharged to within the specified limit of ground. Refer to 节 6.4.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in 节 6.1 and 节 6.4.
- During power-down, LVCMOS input pins must be less than specified in 节 6.4.

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A. See *Pin Configuration and Functions* for pin functions.
B. V_{CC} must be up and stable prior to V_{CC2} powering up.
C. PWRDNZ has two turn on options. Option 1: PWRDNZ does not go high until V_{CC} and V_{CC2} are up and stable, or Option 2: PWRDNZ must be pulsed low for a minimum of T_{PWRDNZ}, or 10 ns after V_{CC} and V_{CC2} are up and stable.
D. There is a minimum of T_{LVDS_ARSTZ}, or 2 μs, wait time from PWRDNZ going high for the LVDS receiver to recover.
E. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates the PWRDNZ and disables V_{CC2}.
F. Under power-loss conditions, where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, PWRDNZ goes low.
G. V_{CC} must remain high until after V_{CC2} goes low.
H. To prevent excess current, the supply voltage delta $|V_{CCI} - V_{CC}|$ must be less than specified limit in 节 6.4.

图 10-1. Power Supply Timing(1)

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

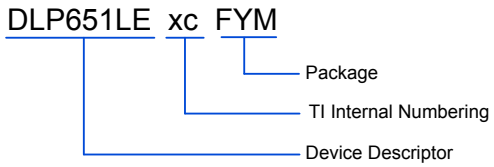


图 11-1. Device Number Description

11.1.2 Device Markings

The device marking will include both human-readable information and a two-dimensional matrix code. The human-readable information is described in 图 11-2. The two-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

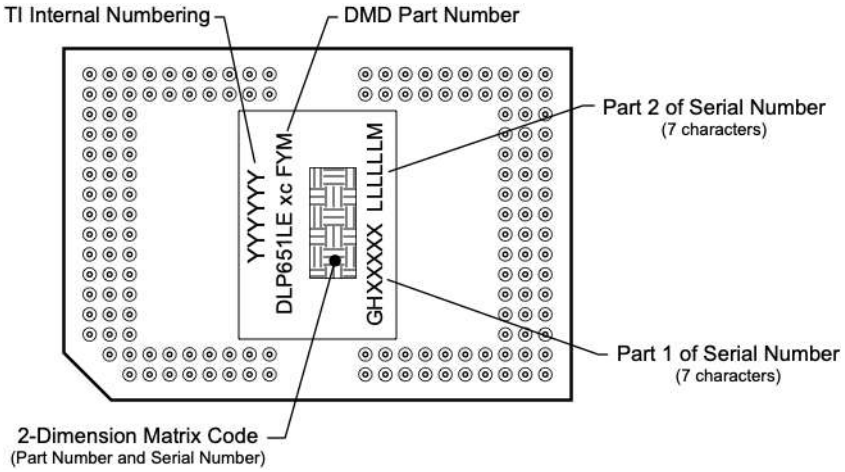


图 11-2. DMD Marking Locations

11.2 Documentation Support

11.2.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP651LE:

- *DLPC4430 Display Controller Data Sheet*
- *DLPA100 Power and Motor Driver Data Sheet*
- *DLPA200 Micromirror Driver Data Sheet*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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11.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP651LEA0FYM	Active	Production	CPGA (FYM) | 149	33 | JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 90	
DLP651LEA0FYM.A	Active	Production	CPGA (FYM) | 149	33 | JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 90	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

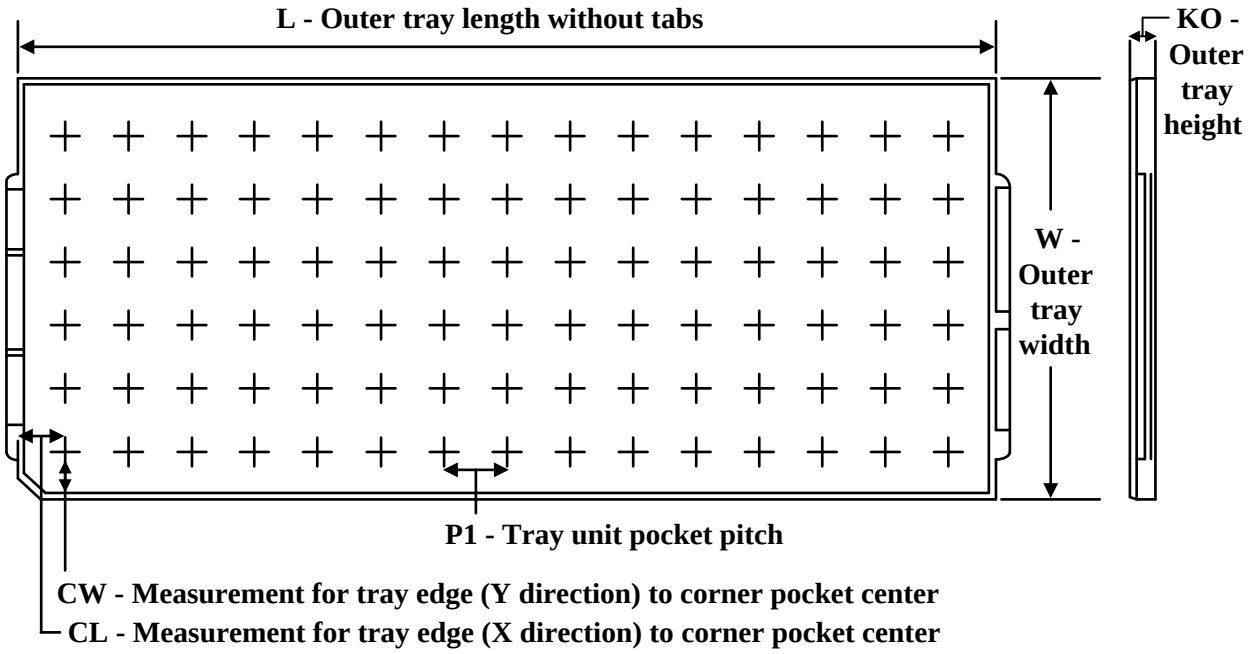
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP651LEA0FYM	FYM	CPGA	149	33	3 x 11	150	315	135.9	12190	27.5	20	27.45
DLP651LEA0FYM.A	FYM	CPGA	149	33	3 x 11	150	315	135.9	12190	27.5	20	27.45

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