DLP650LNIR 0.65 NIR WXGA S450 DMD

1 特性

- 具有超过 100 万个微镜的 1280 × 800 (WXGA) 阵列
  - 10.8µm 微镜间距
  - ±12° 微镜倾斜角（相对于平面）
  - 用于角落照明的 0.65 英寸对角线阵列
  - 0.5°C/W 耐热高效封装
- 高效控制近红外光（800nm 到 2000nm）
  - DMD 上的高达 160W 的入射功率
  - 窗透射率 >98%（950nm 至 1150nm，单通道，两个窗面）
  - 窗透射率 >93%（850nm 至 2000nm，单通道，两个窗面）
  - 偏振无关型铝制微镜
- 16 位 2xLVDS 400MHz 输入数据总线
- 专用 DLPC410 控制器、DLPR410 PROM 和 DLPA200 微镜驱动器可确保可靠的高速运行
  - 二进制模式速率高达 12,500Hz
  - 全局、单块、双块和四块反射镜时钟脉冲（复位）运行模式

2 应用

- 3D 打印、选择性激光烧结 (SLS)
- 动态灰度激光打标和编码
- 工业印刷、柔性版印刷、数字制版
- 修复和消融
- 光谱分析
- 3D 机器视觉和 3D 生物识别
- 红外场景投影
- 高光谱成像
- 光学开关

3 说明

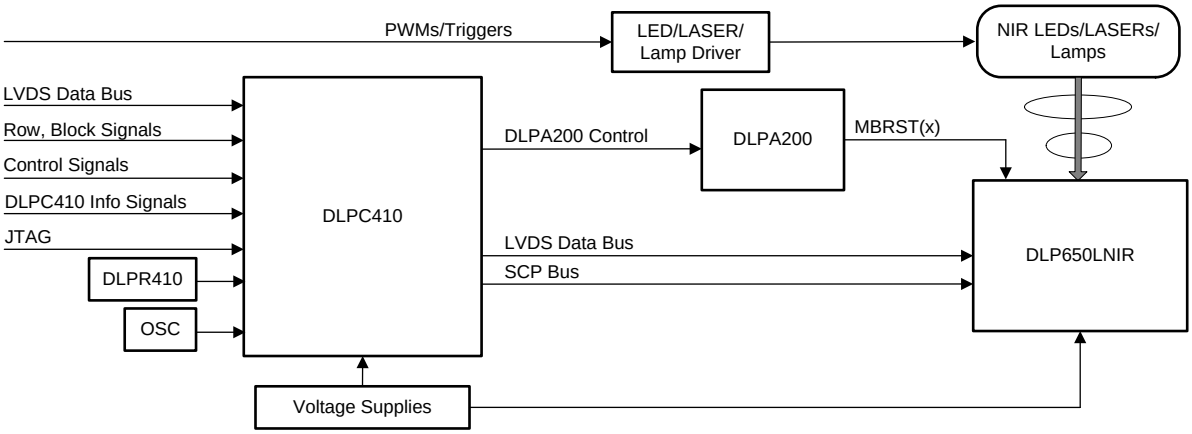
DLP650LNIR 数字微镜器件可作为空间光线调制器 (SLM)，在工业设备中控制近红外 (NIR) 光并生成用于实现高级成像的高速图形。该器件采用了高效散热型封装，允许客户将 DMD 与高功率 NIR 激光照明相结合，从而提供动态数字印刷、烧结和打标解决方案。DLP650LNIR、DLPC410、DLPR410 和 DLPA200 芯片组可提供高达 12,500Hz 的 1 位图形速率及像素精确控制，因此设计人员可以设计出比传统控制激光器所允许的更加创新和精确的光学系统。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLP650LNIR	FYL (149)	22.30mm × 32.20mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

日期	修订版本	说明
2018 年 11 月	*	最初发布版本。

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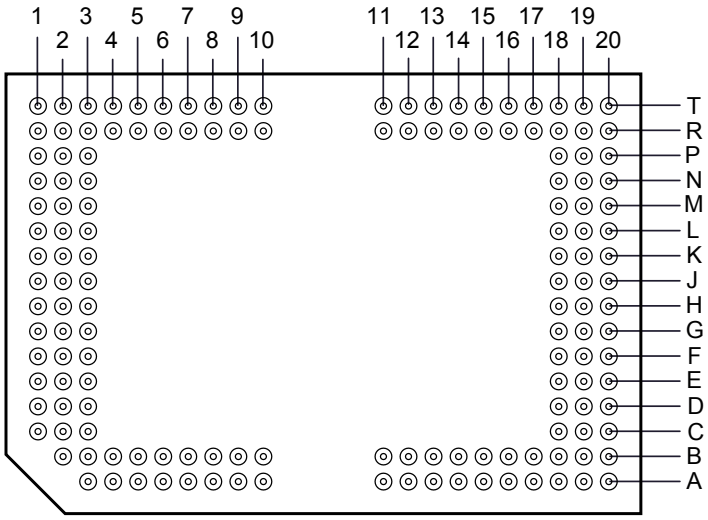
5 Pin Configuration and Functions

FYL Package
149-Pin CLGA
Bottom View



Pin Functions

PIN		NET LENGTH (mils)	SIGNAL	TYPE(1)	DESCRIPTION
NAME	NO.				
DATA INPUTS					
D_AN(1)	G20	711.64	LVDS	I	LVDS pair for Data Bus A
D_AN(3)	H19	711.60			
D_AN(5)	F18	711.60			
D_AN(7)	E18	711.60			
D_AN(9)	C20	711.60			
D_AN(11)	B18	711.60			
D_AN(13)	A20	711.60			
D_AN(15)	B19	711.58			
D_AP(1)	H20	711.66			
D_AP(3)	G19	711.61			
D_AP(5)	G18	711.59			
D_AP(7)	D18	711.60			
D_AP(9)	D20	711.59			
D_AP(11)	A18	711.58			
D_AP(13)	B20	711.59			
D_AP(15)	A19	711.59			
D_BN(1)	K20	711.61	LVDS	I	LVDS pair for Data Bus B
D_BN(3)	J19	711.59			
D_BN(5)	L18	711.59			
D_BN(7)	M18	711.6			
D_BN(9)	P20	711.6			
D_BN(11)	R18	711.59			
D_BN(13)	T20	711.59			
D_BN(15)	R19	711.59			
D_BP(1)	J20	711.61			
D_BP(3)	K19	711.6			
D_BP(5)	K18	711.58			
D_BP(7)	N18	711.58			
D_BP(9)	N20	711.6			
D_BP(11)	T18	711.61			
D_BP(13)	R20	711.59			
D_BP(15)	T19	711.6			
DCLK_AN	D19	711.59		I	LVDS pair for Data Clock A
DCLK_AP	E19	711.59			
DCLK_BN	N19	711.6		I	LVDS pair for Data Clock B
DCLK_BP	M19	711.61			
DATA CONTROL INPUTS					
SCTRL_AN	F20	711.62		I	LVDS pair for Serial Control (Sync) A
SCTRL_AP	E20	711.6			
SCTRL_BN	L20	711.59		I	LVDS pair for Serial Control (Sync) B
SCTRL_BP	M20	711.59			

(1) I = Input, O = Output, G = Ground, A = Analog, P = Power, NC = No Connect.

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Pin Functions (continued)

PIN		NET LENGTH (mils)	SIGNAL	TYPE(1)	DESCRIPTION
NAME	NO.				
MICROMIRROR BIAS RESET INPUTS					
MBRST(0)	C3	507.20		I	Non–logic compatible Micromirror Bias Reset signals. Connected directly to the array of pixel micromirrors. Used to hold or release the micromirrors. Bond Pads connect to an internal pull–down resistor.
MBRST(1)	D2	576.83			
MBRST(2)	D3	545.78			
MBRST(3)	E2	636.33			
MBRST(4)	G3	618.42			
MBRST(5)	E1	738.25			
MBRST(6)	G2	718.82			
MBRST(7)	G1	777.04			
MBRST(8)	N3	543.29			
MBRST(9)	M2	612.93			
MBRST(10)	M3	580.97			
MBRST(11)	L2	672.43			
MBRST(12)	J3	653.61			
MBRST(13)	L1	764.00			
MBRST(14)	J2	764.37			
MBRST(15)	J1	813.14			
SCP CONTROL					
SCPCLK	A8			I	Serial Communications Port Clock. Bond Pad connects to an internal pulldown circuit.
SCPDI	A5			I	Serial Communications Port Data. Bond Pad connects to an internal pulldown circuit.
SCPENZ	B7			I	Active low serial communications port enable. Bond pad connects to an internal pulldown circuit.
SCPDO	A9			O	Serial communications port output.
OTHER SIGNALS					
EVCC	A3			P	Do Not Connect on the DLP system board.
MODE_A	A4	415.1		I	Data Bus Width Select. Bond Pad connects to an internal pull–down circuit, but for this DMD the PCB also ties this signal to GND.
PWRDNZ	B9	110.38		I	Active Low Device Reset. Bond Pad connects to an internal pull–down circuit.
POWER					
V_{CC}(2)	B11, B12, B13, B16, R12, R13, R16, R17			P	Power supply for low voltage CMOS logic. Power supply for normal high voltage at micromirror address electrodes.
V_{CCI}(2)	A12, A14, A16, T12, T14, T16			P	Power supply for low voltage CMOS LVDS interface.
V_{CC2}(2)	C1, D1, M1, N1			P	Power supply for high voltage CMOS logic. Power supply for stepped high voltage at micromirror address electrodes.

(2) Power supply pins required for all DMD operating modes are V_{SS}, V_{CC}, V_{CCI}, V_{CC2}.

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Pin Functions (continued)

PIN		NET LENGTH (mils)	SIGNAL	TYPE(1)	DESCRIPTION
NAME	NO.				
V_{SS} (Ground)(3)	A6, A11, A13, A15, A17, B4, B5, B8, B14, B15, B17, C2, C18, C19, F1, F2, F19, H1, H2, H3, H18, J18, K1, K2, L19, N2, P18, P19, R4, R9, R14, R15, T7, T13, T15, T17			P	Common Return for all power.
RESERVED SIGNALS					
RESERVED_FC	R7	40.64		I	Connect to GND on the DLP system board. Bond Pad connects to an internal pull–down circuit.
RESERVED_FD	R8	94.37		I	Connect to GND on the DLP system board. Bond Pad connects to an internal pull–down circuit.
RESERVED_PFE	T8	50.74		I	Connect to ground on the DLP system board. Bond Pad connects to an internal pull-down circuit.
RESERVED_STM	B6			I	Connect to GND on the DLP system board. Bond Pad connects to an internal pull–down circuit.
RESERVED_TP0	R10	93.3		I	Do not connect on the DLP system board.
RESERVED_TP1	T11	263.74		I	Do not connect on the DLP system board.
RESERVED_TP2	R11	281.47		I	Do not connect on the DLP system board.
RESERVED_BA	T10	148.85		O	Do not connect on the DLP system board.
RESERVED_BB	A10	105.28		O	Do not connect on the DLP system board.
RESERVED_RA1	T9			O	Do not connect on the DLP system board.
RESERVED_RB1	A7			O	Do not connect on the DLP system board.
RESERVED_TS	B10	145.42		O	Do not connect on the DLP system board.
RESERVED_A(0)	T2			NC	Do not connect on the DLP system board.
RESERVED_A(1)	T3				
RESERVED_A(2)	R3				
RESERVED_A(3)	T4				
RESERVED_M(0)	R2			NC	Do not connect on the DLP system board.
RESERVED_M(1)	P1			NC	Do not connect on the DLP system board.
RESERVED_S(0)	T1			NC	Do not connect on the DLP system board.
RESERVED_S(1)	R1			NC	Do not connect on the DLP system board.
RESERVED_IRQZ	T6			NC	Do not connect on the DLP system board.
RESERVED_OEZ	R5			NC	Do not connect on the DLP system board.
RESERVED_RSTZ	R6			NC	Do not connect on the DLP system board.
RESERVED_STR	T5			NC	Do not connect on the DLP system board.

(3) V_{SS} must be connected for proper DMD operation.

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Pin Functions (continued)

PIN		NET LENGTH (mils)	SIGNAL	TYPE(1)	DESCRIPTION
NAME	NO.				
RESERVED_STR	T5			NC	Do not connect on the DLP system board.
RESERVED_VB	E3, F3, K3, L3			NC	Do not connect on the DLP system board.
RESERVED_VR	B2, B3, P2, P3			NC	Do not connect on the DLP system board.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{CC}	Supply voltage for LVCMOS core logic(2)	–0.5	4	V
V_{CCI}	Supply voltage for LVDS Interface(2)	–0.5	4	V
V_{CC2}	Micromirror Electrode and HVCMOS voltage(2)(3)	–0.5	9	V
V_{MBRST}	Input voltage for MBRST(15:0)(2)	–28	28	V
$\lvert V_{CCI} - V_{CC} \rvert$	Supply voltage delta (absolute value)(4)		0.3	V
INPUT VOLTAGES				
	Input voltage for all other input pins(2)	–0.5	V_{CC} + 0.3	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(5)		700	mV
ENVIRONMENTAL				
T_{MIRROR} and T_{WINDOW}	Temperature, operating(6)	0	90	°C
	Temperature, non–operating(6)	–40	90	°C
$\lvert T_{DELTA} \rvert$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1(7)		30	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to common ground V_{SS}. V_{CC}, V_{CCI}, V_{CC2} power supplies are all required for all DMD operating modes. V_{MBRST}signals are also required to be at the appropriate voltage at the appropriate time as controlled by the DLPC410 and DLPA200.
(3) V_{CC2} supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable voltage difference between V_{CC} and V_{CCI} may result in excessive current draw.
(5) The maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(6) The highest micromirror temperature (as calculated using *Micromirror Temperature Calculations*) or of any point along the window edge as defined in Figure 20. The locations of thermal test points TP2, TP3, TP4, and TP5 in Figure 20 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, use that point.
(7) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 20. The window test points TP2, TP3, TP4, and TP5 shown in Figure 20 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, then use that point.

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6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	80	°C
T_{DP-AVG}	Average dew point temperature (non-condensing) (1)		28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Limit exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except MBRST(15:0)	±2000	V
			Pins MBRST(15:0)	< 250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	Supply voltage for LVCMOS core logic (1)	3.0	3.3	3.6	V
V_{CCI}	Supply voltage for LVDS Interface (1)	3.0	3.3	3.6	V
V_{CC2}	Micromirror Electrode and HVCMOS voltage (1) (2)	8.25	8.5	8.75	V
V_{MBRST}	Micromirror Bias / Reset Voltage (1)	–27		26.5	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage delta (absolute value) (3)		0	0.3	V
LVCMOS INTERFACE					
V_{IH}	Input High Voltage	1.7	2.5	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	–0.3		0.7	V
I_{OH}	High Level Output Current			–20	mA
I_{OL}	Low Level Output Current			15	mA
t_{PWRDNZ}	PWRDNZ pulse width (4)	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency (5)	50		500	kHz
t_{SCP_PD}	Propagation delay, clock to Q, from rising-edge of SCPCLK to valid SCPDO. (6)	0		900	ns
t_{SCP_DS}	SCPDI clock setup time (before SCPCLK falling-edge) (6)	800			ns
t_{SCP_DH}	SCPDI hold time (after SCPCLK falling-edge) (6)	900			ns
$t_{SCP_NEG_ENZ}$	Time between falling–edge of SCPENZ and the rising–edge of SCPCLK. (5)	1			us
$_{SCP_POS_ENZ}$	Time between falling-edge of SCPCLK and the rising–edge of SCPENZ	1			us
$t_{SCP_OUT_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tri-state).			192/f_{DCLK}	s

(1) All voltages are referenced to V_{SS} (common ground). V_{CC}, V_{CCI}, V_{CC2}, and V_{MBRST} power supplies are all required for proper DMD operation. V_{SS} must also be connected to common ground.
(2) V_{CC2} supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta $\lvert V_{CCI} - V_{CC} \rvert$ must be less than the specified limit.
(4) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.
(5) The SCP clock is a gated clock. Duty cycle must be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(6) See Figure 3.

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Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
$t_{SCP_PW_ENZ}$	SCPENZ inactive pulse width (high level)	1			$1/f_{scpclk}$
t_r	Rise Time (20% to 80%). See (6)			200	ns
t_f	Fall time (80% to 20%). See (6)			200	ns
LVDS INTERFACE					
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK (7)	395	400	405	MHz
$\|V_{ID}\|$	Input differential voltage (absolute value) (8)	100	400	600	mV
V_{CM}	Common mode voltage (8)		1200		mV
V_{LVDS}	LVDS voltage (8)	0		2000	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			10	ns
Z_{IN}	Internal differential termination resistance	95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL					
T_{MIRROR}	Micromirror temperature, long–term operational (9) (10) (11)	10		40 to 70 (12)	°C
	Micromirror temperature, short–term operational (10) (13)	0		10	°C
T_{WINDOW}	Window temperature–operational (14)	10		85	°C
$T_{\|DELTA\ \|}$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1. (15)			26	°C
$T_{DP\ -AVG}$	Average dew point temperature (non–condensing) (16)			28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) (17)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
ILL_{UV}	Illumination Power Density < 420 nm (9)			10	mW/cm^2
$ILL_{VIS-NIR}$	Illumination Power Density between 420 nm and 950 nm			40	W/cm^2
ILL_{NIR2A}	Illumination Total Power between 950 nm and 1150 nm (18)			160	W
ILL_{NIR2B}	Illumination Power Density between 950 nm and 1150 nm (18)			500	W/cm^2
ILL_{NIR3}	Illumination Power Density between 1150 nm and 2000 nm			40	W/cm^2
ILL_{IR}	Illumination Power Density > 2000 nm			10	mW/cm^2

(7) See LVDS Timing Requirements in *Timing Requirements* and Figure 7.
(8) See Figure 6 LVDS Waveform Requirements.
(9) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination reduces device lifetime.
(10) The mirror temperatures cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 20 and the DMD package and mirror *thermal resistances* using the *Micromirror Temperature Calculations*.
(11) Long-term is defined as the usable life of the device.
(12) Per Figure 2, derate the maximum operational micromirror temperature based on the micromirror landed duty cycle that the DMD experiences in the end application. See *Micromirror Landed-On/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(13) Mirror temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
(14) The locations of thermal test points TP2, TP3, TP4, and TP5 in Figure 20 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, add test points to those locations.
(15) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 20. The window test points TP2, TP3, TP4, and TP5 shown in Figure 20 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, use that point.
(16) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
(17) Limit exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.
(18) See Figure 1 for allowable combinations of illumination power vs illumination power density. 160W total power is achievable only by full array illumination. 500 W/cm^2 is only achievable through partial array illumination. Some combinations of illumination power and power density require cooling of the window with forced air as defined by Figure 1. Refer to the application note DLP® High Power Thermal Design Guide: Focus on High Power NIR Laser Illumination for additional details.

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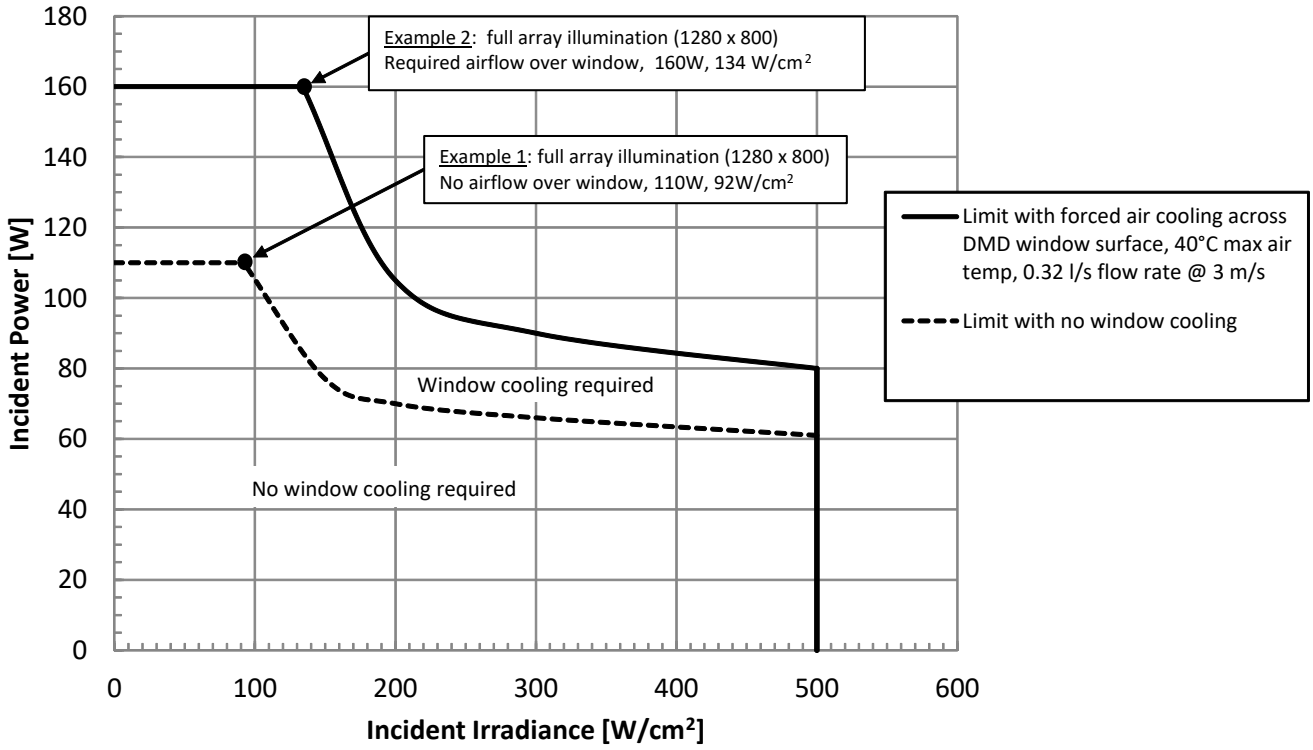

Figure 1. Maximum Recommended Illumination Incident Power vs Incident Irradiance

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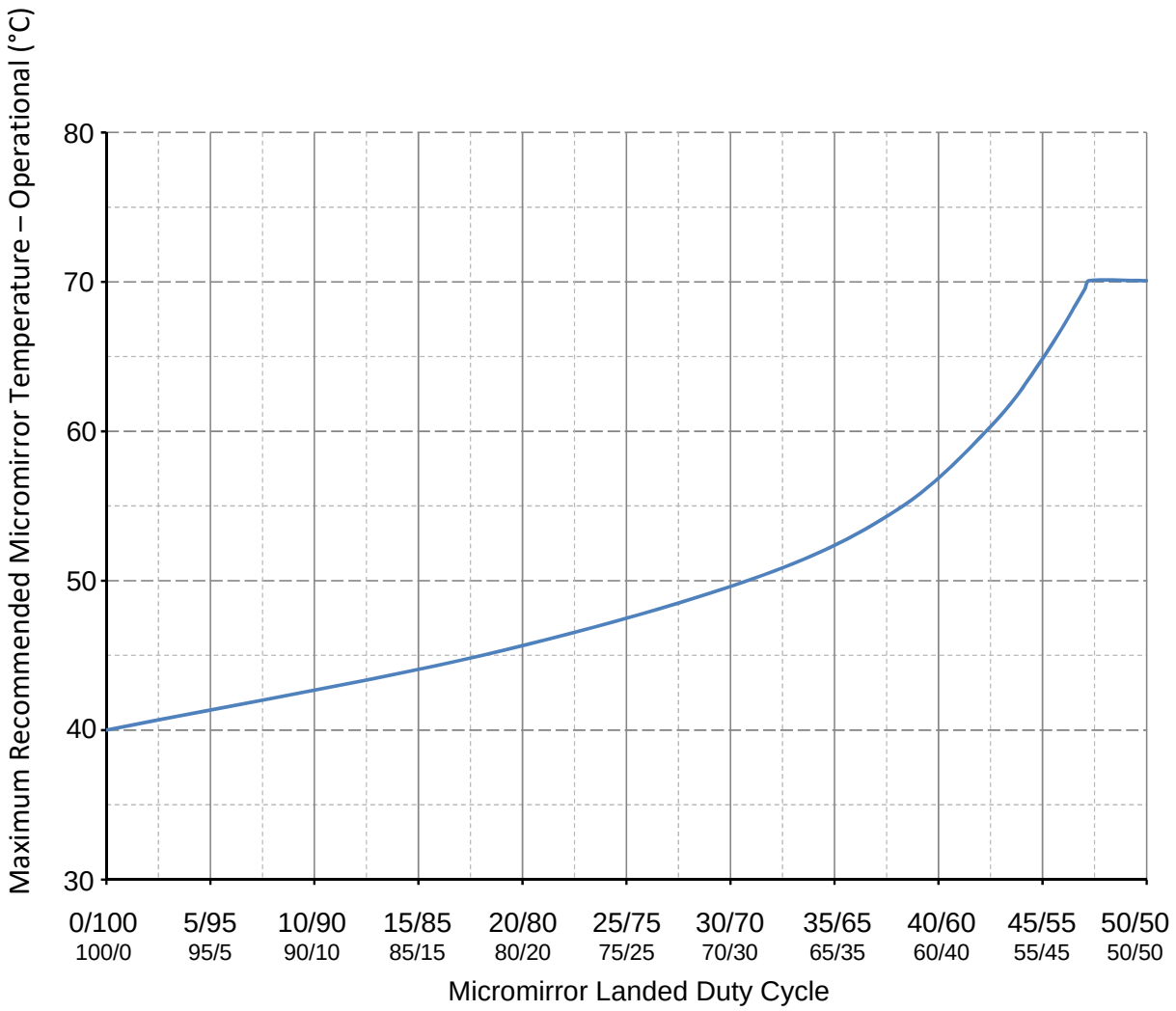

Figure 2. Maximum Recommended Micromirror Temperature - Derating Curve (see Landed Duty Cycle and Operational DMD Temperature)

6.5 Thermal Information

THERMAL METRIC	DLP650LNIR FYL Package 149 PINS	UNIT
$R_{SILICON\text{-}TO\text{-}CERAMIC}$: Thermal resistance, silicon to ceramic, as measured at test point 1 (TP1) (1)	0.5	°C/W
$R_{MIRROR\text{-}TO\text{-}SILICON}$: Thermal resistance, mirror to silicon, per individual mirror (1)	3.39×10^5	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*.
The total heat load on the DMD is largely driven by the incident light absorbed by the micromirrror array, although other contributions include light energy outside of the active mirror array and electrical power dissipation of the silicon.
Design the optical system to minimized light outside of the active micromirror array because light outside of this area gets highly absorbed by the optical border and increases DMD heat load.
Design the optical system to minimize the light energy falling outside the window clear aperture. Aditional thermal load in this area contributes to window heating and significantly degrades the reliability of the device.

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6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	V_{CC} = 3 V, I_{OH} = – 20 mA	2.4			V
V_{OL}	Low level output voltage	V_{CC} = 3.6 V, I_{OL} = 15 mA			0.4	V
I_{OZ}	High impedance output current	V_{CC} = 3.6 V			10	µA
I_{IL}	Low level input current	V_{CC} = 3.6 V, VI = 0			–60	µA
I_{IH}	High level input current (1)	V_{CC} = 3.6 V, VI = V_{CC}			200	µA
I_{CC}	Supply current VCC (2)	V_{CC} = 3.6 V			650	mA
I_{CCI}	Supply current VCCI (2)	V_{CCI} = 3.6 V			350	mA
I_{CC2}	Supply current VCC2	V_{CC2} = 8.75 V			25	mA
Z_{IN}	Internal differential termination resistance		95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)		90	100	110	Ω
C_I	Input capacitance (1)	f = 1 MHz			10	pF
C_O	Output capacitance (1)	f = 1 MHz			10	pF
C_{IM}	Input capacitance for MBRST[0:15] pins	f = 1 MHz	160		210	pF

(1) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins.
(2) To prevent excess current, the supply voltage delta $|V_{CCI} – V_{CC}|$ must be less than the specified limit in *Recommended Operating Conditions*.

6.7 Timing Requirements

Over *Recommended Operating Conditions* (unless otherwise noted).

PARAMETER DESCRIPTION		SIGNAL	MIN	TYP	MAX	UNIT
LVDS (1)						
t_C	Clock Cycle Duration for DCLK_A	LVDS	2.46			ns
t_C	Clock Cycle Duration for DCLK_B	LVDS	2.46			ns
t_W	Pulse Duration for DCLK_A	LVDS	1.07	1.23		ns
t_W	Pulse Duration for DCLK_B	LVDS	1.07	1.23		ns
t_{SU}	Setup Time for D_A(15:0) before DCLK_A	LVDS	0.35			ns
t_{SU}	Setup Time for D_A(15:0) before DCLK_B	LVDS	0.35			ns
t_{SU}	Setup Time for SCTRL_A before DCLK_A	LVDS	0.35			ns
t_{SU}	Setup Time for SCTRL_B before DCLK_B	LVDS	0.35			ns
t_H	Hold time for D_A(15:0) after DCLK_A	LVDS	0.50			ns
t_H	Hold time for D_B(15:0) after DCLK_B	LVDS	0.50			ns
t_H	Hold Time for SCTRL_A after DCLK_A	LVDS	0.50			ns
t_H	Hold Time for SCTRL_B after DCLK_B	LVDS	0.50			ns
t_{SKEW}	Channel B relative to Channel A (2) (3)	LVDS	–1.23		1.23	ns

(1) See Figure 7 for timing requirements for LVDS.
(2) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15,13,11,9,7,5,3,1) and D_AP(15,13,11,9,7,5,3,1).
(3) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15,13,11,9,7,5,3,1) and D_BP(15,13,11,9,7,5,3,1).

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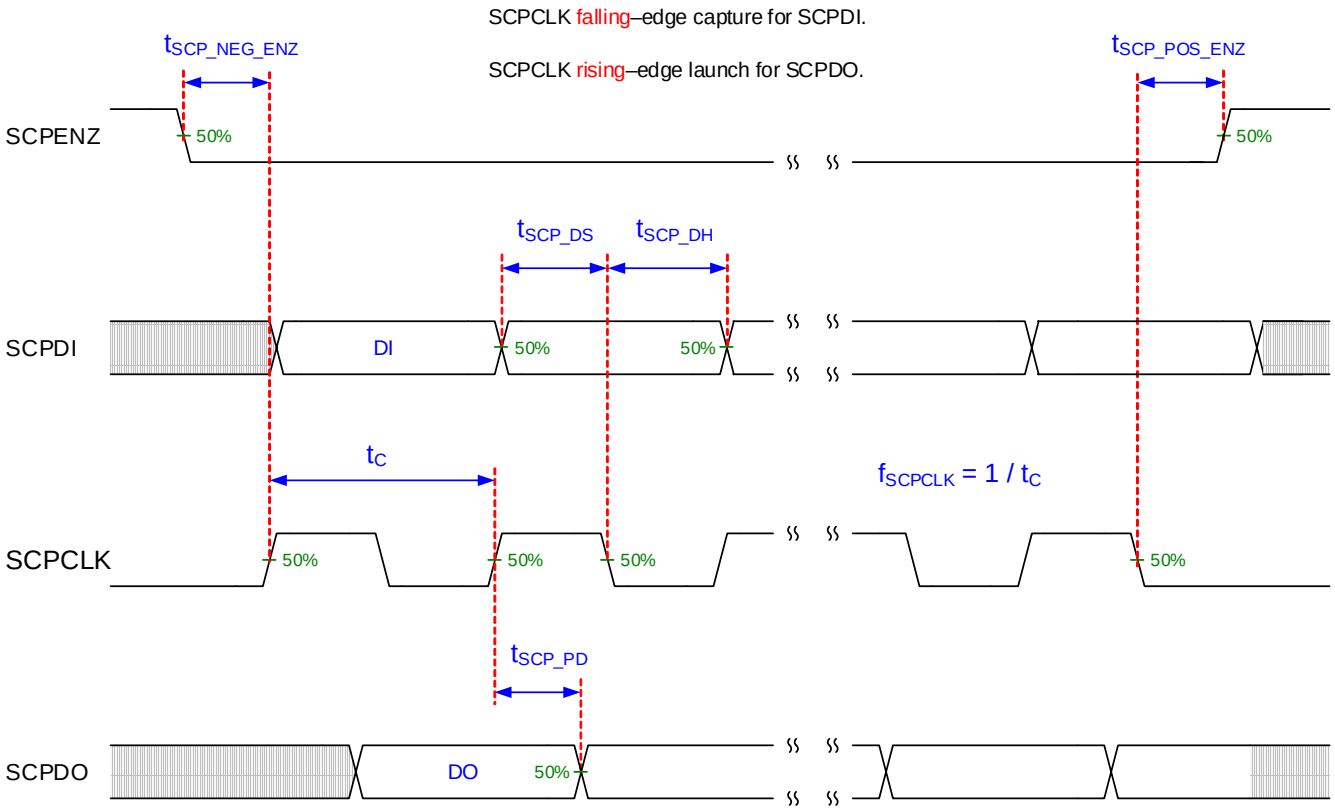
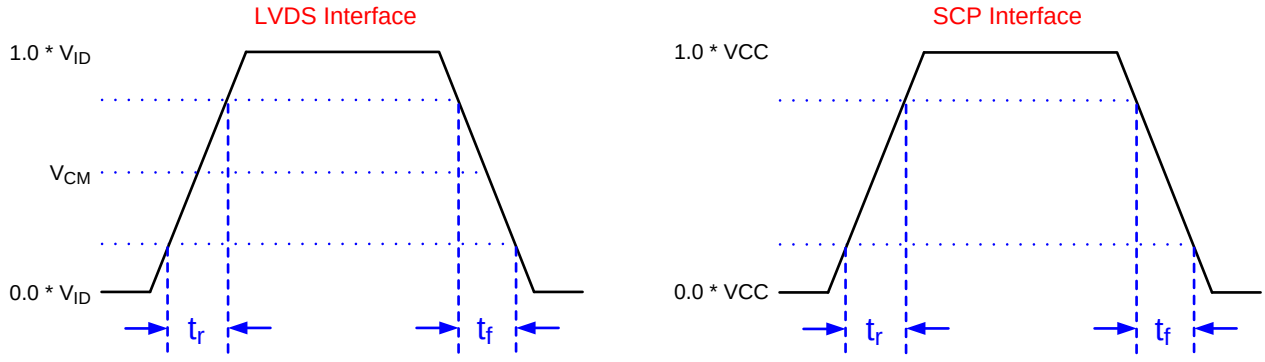


Figure 3. SCP Timing Requirements

See *Recommended Operating Conditions* for f_{SCPCLK}, t_{SCP_DS}, t_{SCP_DH}, and t_{SCP_PD} specifications.

See *Recommended Operating Conditions* for t_r and t_f specifications and conditions.



Not to scale.

Refer to the *Timing Requirements*.

Refer to for list of LVDS pins and SCP pins.

Figure 4. Rise Time and Fall Time

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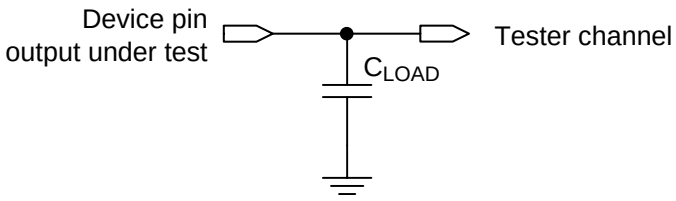

Figure 5. Test Load Circuit for Output Propagation Measurement

For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Use IBIS or other simulation tools to correlate the timing reference load to a system environment. See Figure 5.

Not to Scale

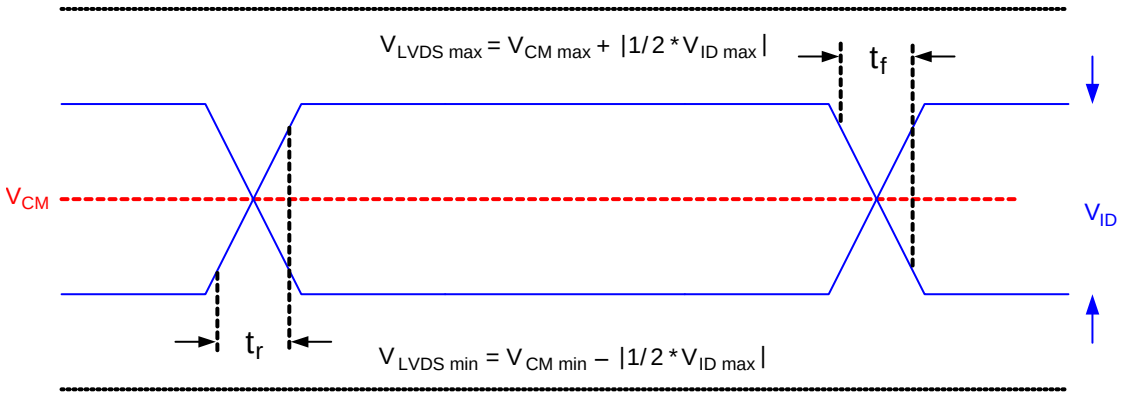

Figure 6. LVDS Waveform Requirements

See *Recommended Operating Conditions* for V_{CM}, V_{ID}, and V_{LVDS} specifications and conditions.

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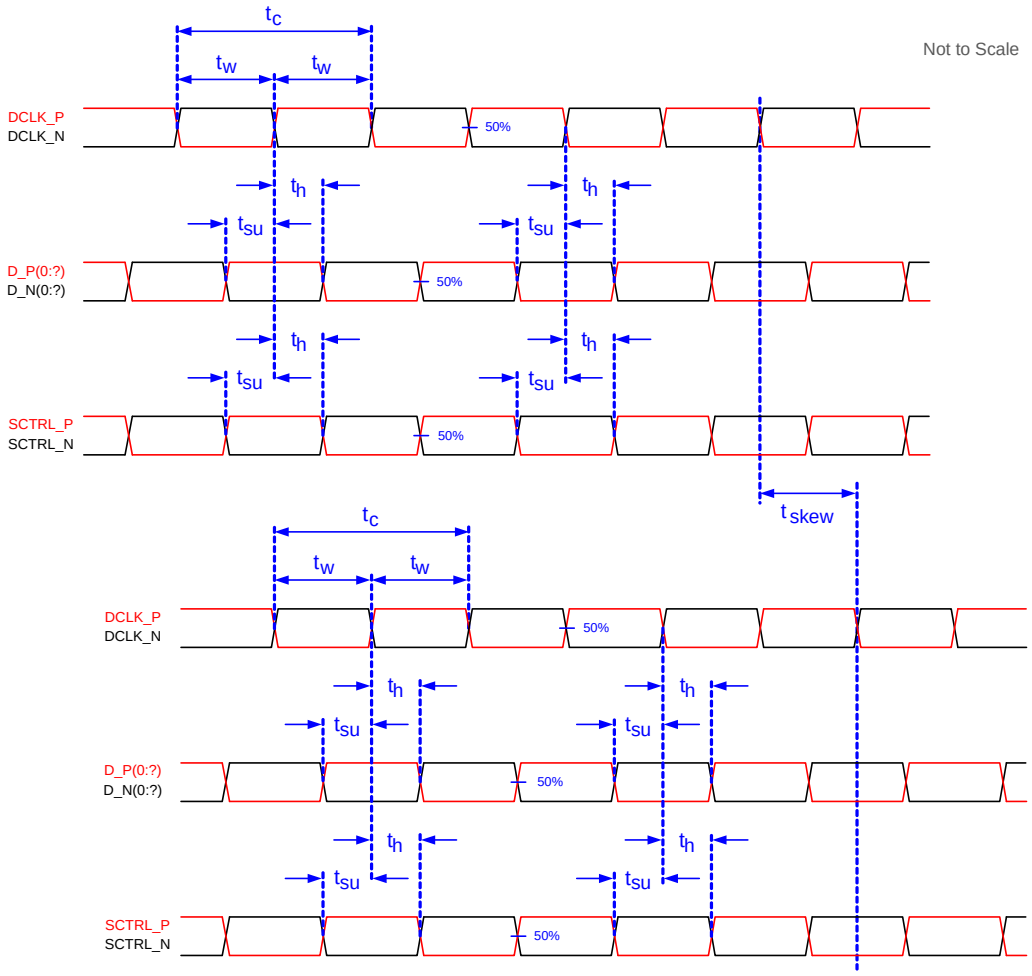

Figure 7. Timing Requirements

See *Timing Requirements* for timing requirements and LVDS pairs per channel (bus) defining D_P(0:x) and D_N(0:x).

6.8 System Mounting Interface Loads

Table 1. System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Condition 1:				
• Thermal Interface area(1)			11.3	kg
• Electrical Interface area(1)			11.3	kg
Condition 2:				
• Thermal Interface area(1)			0	kg
• Electrical Interface area(1)			22.6	kg

(1) Uniformly distributed within area shown in Figure 8.

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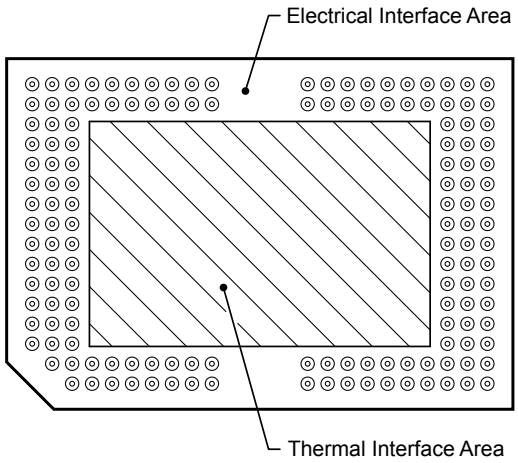

Figure 8. System Mounting Interface Loads

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6.9 Micromirror Array Physical Characteristics

Table 2. Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns (1)	M	1280	micromirrors
Number of active rows (1)	N	800	
Micromirror (pixel) pitch (1)	P	10.8	µm
Micromirror active array width (1)	Micromirror pitch × number of active columns	13.824	mm
Micromirror active array height (1)	Micromirror pitch × number of active rows	8.640	mm
Micromirror active border size (2)	Pond of Micromirror (POM)	10	micromirrors / side

(1) See Figure 9.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the *Pond Of Mirrors* (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or "on" state but the requirement of an electrical bias to tilt toward "off remains."

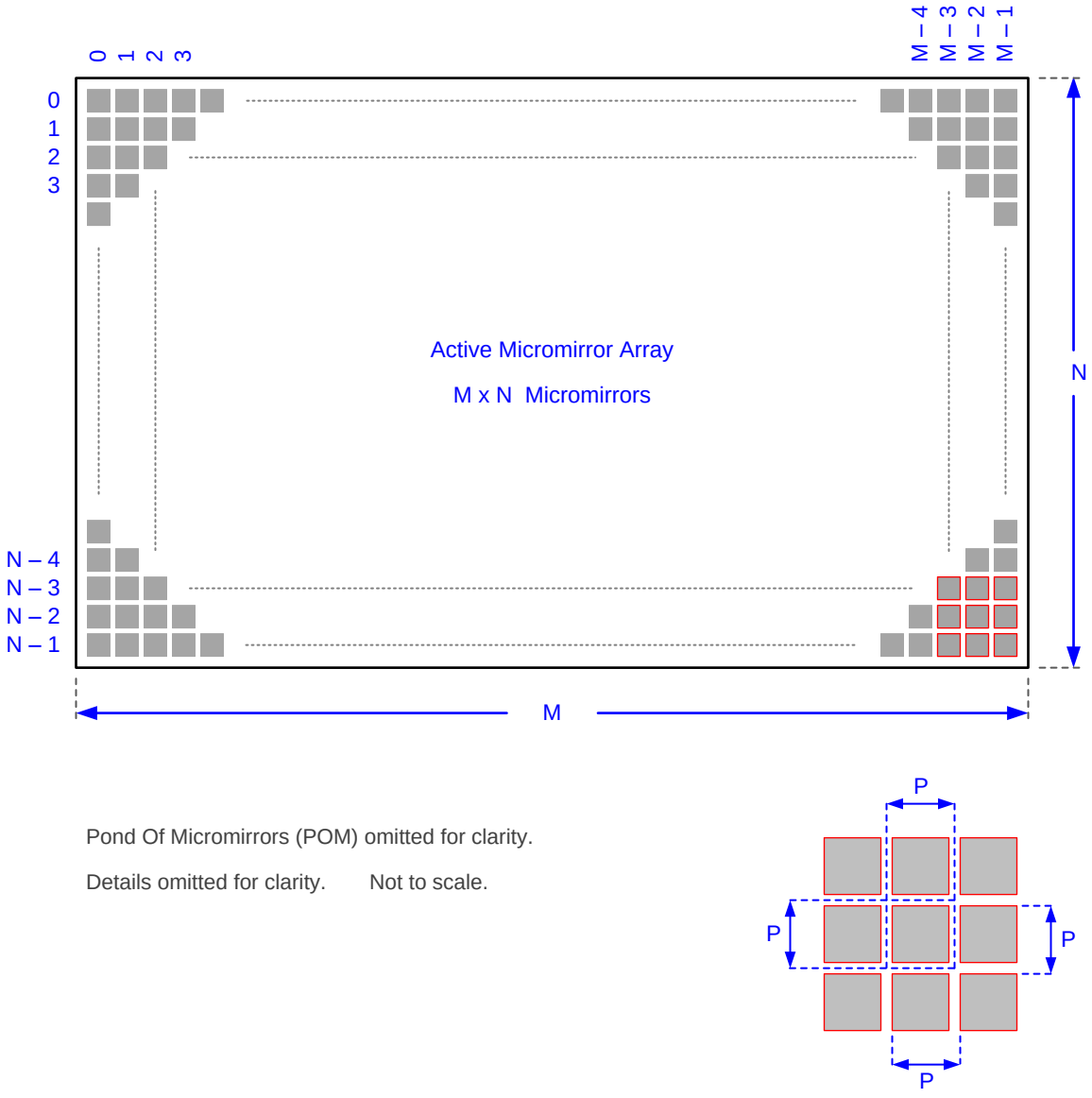

Figure 9. Micromirror Array Physical Characteristics

Refer to the *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

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6.10 Micromirror Array Optical Characteristics

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. See the additional details, considerations, and guidelines: DLP System Optics Application Report (listed in DLPS022) for guidelines.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
a	Micromirror tilt angle	DMD parked state (1) (2), See Figure 15		0		degrees
		DMD landed state (1) (3) (4) See Figure 15		12		
β	Micromirror tilt angle variation (1) (3) (5) (6) (7)	See Figure 15	–1		1	degrees
	Micromirror crossover time (8)			3		µs
	Micromirror switching time (9)			13	22	µs
	Array switching time at 400 MHz with global reset (10)		92.5			µs
	Non-operating micromirrors (11)	Non-adjacent micromirrors			10	micromirrors
		Adjacent micromirrors			0	
	Orientation of the micromirror axis-of-rotation (12)	See Figure 15	44	45	46	degrees
	Micromirror array optical efficiency (13) (14)	@1064 nm, with all micromirrors in the ON state		75%		

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Parking the micromirror array returns all of the micromirrors to an essentially flat (0˚) state (as measured relative to the plane formed by the overall micromirror array).
(3) Additional variation exists between the micromirror array and the package datums- see the *机械、封装和可订购信息*
(4) When the micromirror array is landed, the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in an nominal angular position of +12°. A binary value of 0 results in a micromirror landing in an nominal angular position of –12°.
(5) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(6) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(7) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast variation.
(8) Micromirror crossover time is the transition time from landed to landed during a crossover transition and primarily a function of the natural response time of the micromirrors.
(9) Micromirror switching time is the time after a micromirror clocking pulse until the micromirrors can be addressed again. It includes the micromirror settling time.
(10) Array switching is controlled and coordinated by the DLPC410 (DLPS024) and DLPA200 (DLPS015). Nominal switching time depends on the system implementation and represents the time for the entire micromirror array to be refreshed (array loaded plus reset and mirror settling time).
(11) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the –12° position to +12° or vice versa.
(12) Measured relative to the package datums 'B' and 'C', shown in the *机械、封装和可订购信息*.
(13) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:
  (a) Illumination wavelength, bandwidth/line-width, degree of coherence
  (b) Illumination angle, plus angle tolerance
  (c) Illumination and projection aperture size, and location in the system optical path
  (d) Illumination overfill of the DMD micromirror array
  (e) Aberrations present in the illumination source and/or path
  (f) Aberrations present in the projection path

  The specified nominal DMD optical efficiency is based on the following use conditions:
  (a) NIR illumination (1064nm selected as reference example)
  (b) Input illumination optical axis oriented at 24° relative to the window normal
  (c) Projection optical axis oriented at 0° relative to the window normal
  (d) *ƒ* / 3 illumination aperture
  (e) *ƒ* / 2.4 projection aperture

  Based on these use conditions, the nominal DMD optical efficiency at 1064 nm results from the following four components:
  (a) Micromirror array fill factor: nominally 94%
  (b) Micromirror array diffraction efficiency: nominally 88%
  (c) Micromirror surface reflectivity: nominally 94%
  (d) Window transmission: nominally 98% (single pass, through two surface transitions)
(14) Does not account for the effect of micromirror switching duty cycle, which is application dependent. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.

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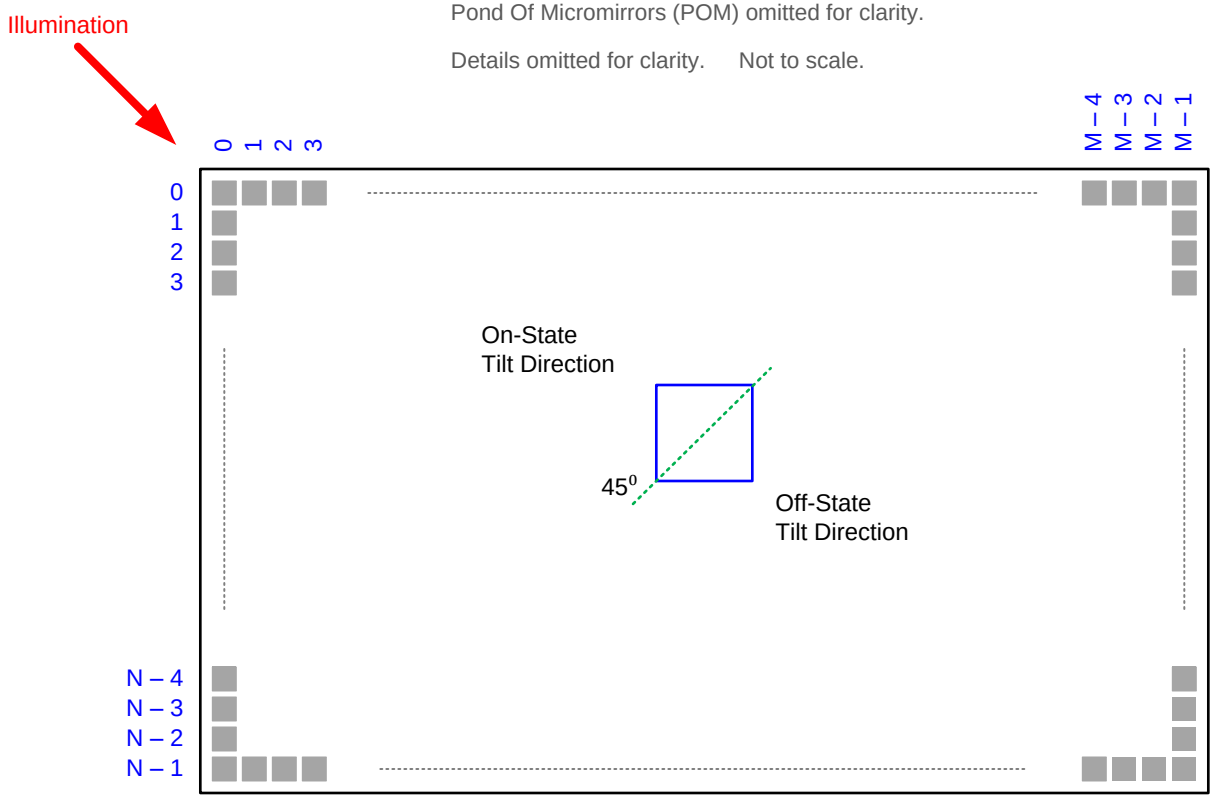

Figure 10. Micromirror Landed Orientation and Tilt

Refer to the *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

6.11 Window Characteristics

PARAMETER (1)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Window material designation	Corning Eagle XG				
Window refractive index	At wavelength 1060 nm		1.4996		
Window aperture	See (2)				
Illumination overfill	Refer to *Illumination Overfill*				
Window transmittance, single–pass through both surfaces and glass (3)	At wavelength 1050 nm. Applies to 0° AOI only.		99%		
	Minimum within the wavelength range 850 nm to 2000 nm. Applies to 0° AOI only.	90%	93%		
	Minimum within the wavelength range 950 nm to 1150 nm. Applies to 0° AOI only.	98%	98.4%		

(1) See *Optical Interface and System Image Quality Considerations* for more information.
(2) For details regarding the size and location of the window aperture, see the package mechanical characteristics listed in the Mechanical ICD in the Mechanical, Packaging, and Orderable Information section.
(3) See the TI application report DLPA031, *Wavelength Transmittance Considerations for DLP DMD Window*.

6.12 Chipset Component Usage Specification

Reliable function and operation of the DLP650LNIR DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

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7 Detailed Description

7.1 Overview

Optically, the DLP650LNIR consists of 1,024,000 highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors), organized in a two-dimensional array of 1280 micromirror columns by 800 micromirror rows. Each aluminum micromirror is approximately 10.8 microns in size (see the *Micromirror Pitch* in) and is switchable between two discrete angular positions: –12° and 12°. The angular positions are measured relative to a 0° flat state, which is parallel to the array plane (see Figure 15). The tilt direction is perpendicular to the hinge-axis, which is positioned diagonally relative to the overall array. The On State landed position is directed toward row 0, column 0 (upper left) corner of the device package (see the *Micromirror Hinge-Axis Orientation* in). In the field of visual displays, the 1280 × 800 pixel resolution is referred to as WXGA or WXGA-800.

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror clocking pulse is applied. The angular position (–12° or +12°) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being synchronous with the CMOS memory cell data update. Therefore, writing a logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a 12° position. Writing a logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a –12° position.

Updating the angular position of the micromirror array consists of two steps. First, updating the contents of the CMOS memory. Second, application of a micromirror clocking pulse to all or a portion of the micromirror array (depending upon the configuration of the system). Micromirror clocking pulses are generated externally by the DLPA200 device, with application of the pulses being coordinated by the DLPC410 controller.

Around the perimeter of the 1280 by 800 array of micromirrors is a uniform band of border micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 1280 by 800 active array.

Figure 11 shows a DLPC410 and DLP650LNIR chipset block diagram. The DLPC410 and DLPA200 control and coordinate the data loading and micromirror switching for reliable DLP650LNIR operation. The DLPR410 is the programmed PROM required to properly configure the DLPC410 controller. For more information on the chipset components, see *Feature Description*. For a typical system application using the DLPC410 and chipset components including a DLP650LNIR DMD, see Figure 21.

7.2 System Functional Block Diagram

Figure 11 shows a simplified system block diagram with the use of the DLPC410 with the following chipset components:

DLPC410 Xilinx [XC5VLX30] FPGA configured to provide high-speed DMD data and control, and DLPA200 timing and control

DLPR410 [XCF16PFSG48C] serial flash PROM contains startup configuration information (EEPROM)

DLPA200 DMD micromirror driver for the DLP650LNIR DMD

DLP650LNIR Spatial light modulator (DMD)

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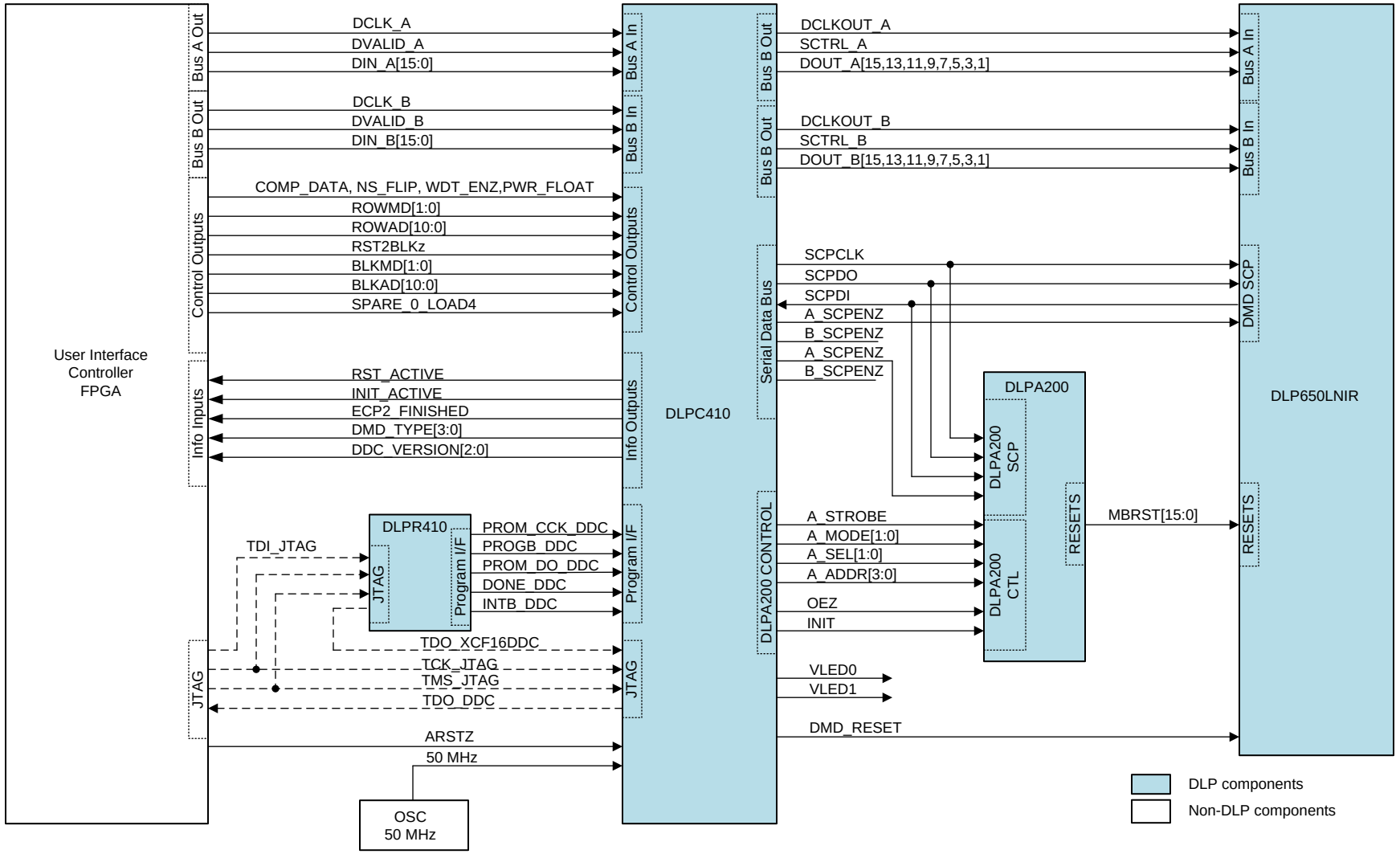

Figure 11. DLPC410, DLPA200, DLPR410, and DLP650LNIR Functional Block Diagram

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7.3 Feature Description

Table 3. DMD Overview

DMD	ARRAY	QUAD BLOCK MODE (Patterns/s)	GLOBAL RESET MODE (Patterns/s)	DATA RATE (Giga Pixels/s)	MIRROR PITCH
DLP650LNIR - 0.65" WXGA NIR	1280 × 800	12,500	10,811	12	10.8 µm

7.3.1 DLPC410: Digital Controller for DLP Discovery 4100 Chipset

The DLPC410 chipset includes the DLPC410 controller which provides a high-speed LVDS data and control interface for DMD control. This interface is also connected to a second FPGA used to drive applications (not included in the chipset). The DLPC410 generates DMD and DLPA200 initialization and control signals in response to the inputs on the control interface.

For more information, see the DLPC410 data sheet (DLPS024).

7.3.2 DLPA200: DMD Micromirror Driver

DLPA200 micromirror driver provides the micromirror clocking pulse driver functions for the DMD. A single driver is required for DLP650LNIR DMD.

The DLPA200 is designed to work with multiple DLP chipsets. The DLPA200 contains 16 MBSRT output pins and all 16 are used with the DLP650LNIR chipset. For more information see the DLPC410 (DLPS024) and the DLPA200 data sheets (DLPS015).

7.3.3 DLPR410: PROM for DLP Discovery 4100 Chipset

The DLPC410 controller is configured at startup from the DLPR410 PROM. The contents of this PROM are fixed and cannot be altered. For more information, see the DLPR410 data sheet (DLPS027) and the DLPC410 data sheet (DLPS024).

7.3.4 DLP650LNIR: DLP 0.65 WXGA NIR 2xLVDS Series 450 DMD

7.3.4.1 DLP650LNIR Chipset Interfaces

This section describes the interface between the different components included in the chipset. For more information on component interfacing, see *Application Information*.

7.3.4.1.1 DLPC410 Interface Description

7.3.4.1.1.1 DLPC410 IO

Table 4 describes the inputs and outputs of the DLPC410 related to the control of the DLP650LNIR DMD. For more details on these signals, see the DLPC410 data sheet (DLPS024).

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Table 4. Input/Output Description

PIN NAME	DESCRIPTION	I/O
$\overline{\text{ARST}}$	Asynchronous active low reset	I
CLKIN_R	Reference clock, 50 MHz	I
DIN_[A,B,C,D](15:0)	LVDS DDR input for data bus A,B,C,D (15:0)	I
DCLKIN[A,B,C,D]	LVDS inputs for data clock (400 MHz) on bus A, B, C, and D	I
DVALID[A,B,C,D]	LVDS input signals used to start write sequence for bus A, B, C, and D	I
ROWMD(1:0)	DMD row address and row counter control	I
ROWAD(10:0)	DMD row address pointer	I
BLK_AD(3:0)	DMD mirror block address pointer	I
BLK_MD(1:0)	DMD mirror block reset and clear command modes	I
PWR_FLOAT	Used to float DMD mirrors before complete loss of power	I
LOAD4	Load4 mode enable [uses DLPC410 SPARE_0 input pin (AB21)]	I
DMD_TYPE(3:0)	DMD type in use	O
RST_ACTIVE	Indicates DMD mirror reset in progress	O
INIT_ACTIVE	Initialization in progress.	O
VLED0	System “heartbeat” signal	O
VLED1	Denotes initialization complete	O

7.3.4.1.1.2 Initialization

The *INIT_ACTIVE* (Table 4) signal indicates that the DLP650LNIR, DLPA200, and DLPC410 are in an initialization state after power is applied. During this initialization period, the DLPC410 is initializing the DLP650LNIR and DLPA200 by setting all internal registers to their correct states. When this signal goes low, the system has completed initialization. System initialization takes approximately 220 ms to complete. Data and command write cycles should not be asserted during the initialization.

During initialization the user must send a training pattern to the DLPC410 on all data and DVALID lines to correctly align the data inputs to the data clock. For more information, see the interface training pattern information in the DLPC410 data sheet.

7.3.4.1.1.3 DMD Device Detection

The DLPC410 automatically detects the DMD type and device ID. DMD_TYPE (Table 4) is an output from the DLPC410 that contains the DMD information.

7.3.4.1.1.4 Power Down

To ensure long term reliability of the DLP650LNIR DMD, a shutdown procedure must be executed. Prior to power removal, assert the PWR_FLOAT (Table 4) signal and allow approximately 300 µs to assure the mirrors are in a flat state prior to power removal.

NOTE

Use PWR_FLOAT only when DC power is going to be removed from the DMD. When not powering down but it is desired to place the system in an idle (non-functioning) state, all applications benefit from operating the DMD near 50% landed on/off duty cycle. See section 3 (Duty Cycle Considerations) in application note DLPA052 - System Design Considerations Using TI DLP® Technology down to 400 nm.

7.3.4.1.2 DLPC410 to DMD Interface

7.3.4.1.2.1 DLPC410 to DMD IO Description

Table 5 lists the available controls and status pin names and their corresponding signal type, along with a brief functional description.

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Table 5. DLPC410 to DMD I/O Pin Descriptions

PIN NAME	DESCRIPTION	I/O
DOUT_A[15,13,11,9,7,5,3,1]	2xLVDS DDR output to DMD data bus A[15,13,11,9,7,5,3,1]	O
DOUT_B[15,13,11,9,7,5,3,1]	2xLVDS DDR output to DMD data bus B[15,13,11,9,7,5,3,1]	O
DCLKOUT_[A,B]	2xLVDS output to DMD data clock DCLKA and DCLKB	O
SCTRL_[A,B]	2xLVDS DDR output to DMD data control buses A, and B	O

7.3.4.1.2.2 Data Flow

Figure 12 shows the data traffic through the DLPC410. Special considerations are necessary when laying out the DLPC410 to allow best signal flow.

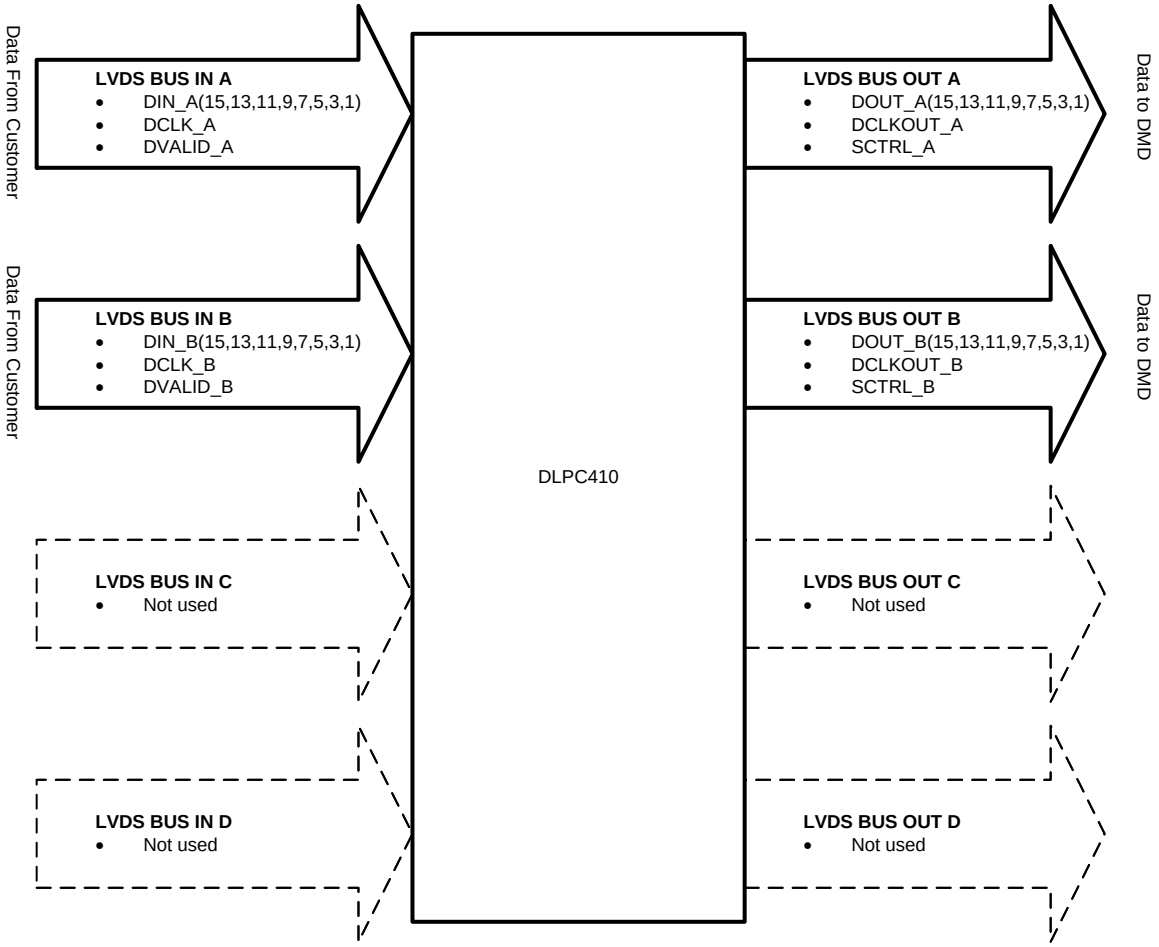

Figure 12. DLPC410 Data Flow

Two LVDS buses A and B transfer the data from the user to the DLPC410. Each bus has its own data clock that is input edge aligned with the data (DCLK). Each bus also has its own validation signal that qualifies the data input to the DLPC410 (DVALID).

Output LVDS buses A and B transfer data from the DLPC410 to the DLP650LNIR. The DLP650LNIR uses only the odd input signals of the output buses A and B.

Buses C and D are used with DMDs which have 64-bit wide data inputs only.

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7.3.4.1.3 DLPC410 to DLPA200 Interface

7.3.4.1.3.1 DLPA200 Operation

The DLPA200 DMD micromirror driver is a mixed-signal application-specific integrated circuit (ASIC) that combines the necessary high-voltage power supply generation and micromirror clocking pulse functions for a family of DMDs. The DLPA200 is programmable and controllable to meet all current and anticipated DMD requirements.

The DLPA200 operates from a 12-V power supply input. For more detailed information on the DLPA200, see the DLPA200 data sheet.

7.3.4.1.3.2 DLPC410 to DLPA200 IO Description

The Serial Communications Port (SCP) is a full duplex, synchronous, character-oriented (byte) port that allows exchange of commands from the DLPC410 to the DLPA200. One SCP bus is used for the DLP650LNIR.

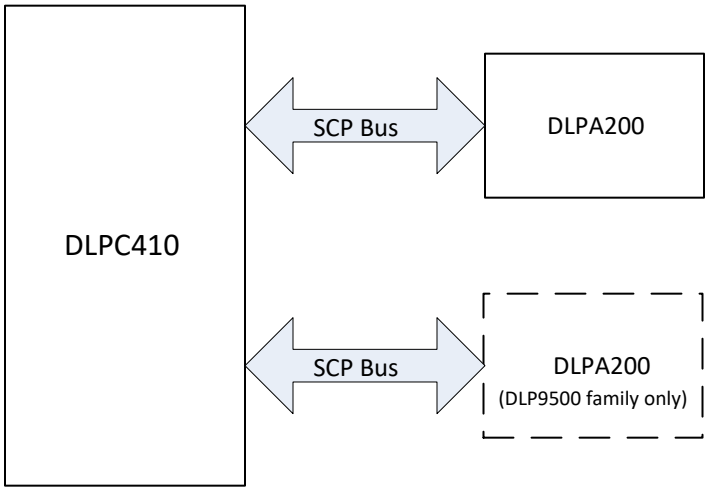

Figure 13. Serial Port System Configuration

Five signal lines are associated with the SCP bus: $\overline{\text{SCPEN}}$, SCPCK, SCPDI, SCPDO, and $\overline{\text{IRQ}}$.

Table 6 lists the available controls and status pin names and their corresponding signal type, along with a brief functional description.

Table 6. DLPC410 to DLPA200 I/O Pin Descriptions

PIN NAME	DESCRIPTION	I/O
$\overline{\text{A_SCPEN}}$	Active-low chip select for DLPA200 serial bus	O
A_STROBE	DLPA200 control signal strobe	O
A_MODE(1:0)	DLPA200 mode control	O
A_SEL(1:0)	DLPA200 select control	O
A_ADDR(3:0)	DLPA200 address control	O
$\overline{\text{B_SCPEN}}$	Active-low chip select for DLPA200 serial bus (2)	O
B_STROBE	DLPA200 control signal strobe (2)	O
B_MODE(1:0)	DLPA200 mode control	O
B_SEL(1:0)	DLPA200 select control	O
B_ADDR(3:0)	DLPA200 address control	O

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The DLPA200 provides a variety of output options to the DMD by selecting logic control inputs: MODE[1:0], SEL[1:0] and reset group address A[3:0] (Table 6). The MODE[1:0] input determines whether a single output, two outputs, four outputs, or all outputs, are selected. Output levels (VBIAS, VOFFSET, or VRESET) are selected by SEL[1:0] pins. Selected outputs are tri-stated on the rising edge of the STROBE signal and latched to the selected voltage level after a break-before-make delay. Outputs remain latched at the last micromirror clocking pulse waveform level until the next micromirror clocking pulse waveform cycle.

7.3.4.1.4 DLPA200 to DLP650LNIR Interface

7.3.4.1.4.1 DLPA200 to DLP650LNIR Interface Overview

The DLPA200 generates three voltages: VBIAS, VRESET, and VOFFSET that are supplied to the DMD MBRST lines in various sequences through the micromirror clocking pulse driver function. VOFFSET is also supplied directly to the DMD as VCC2. A fourth DMD power supply, VCC, is supplied directly to the DMD by regulators.

The function of the micromirror clocking pulse driver is to switch selected outputs in patterns between the three voltage levels (VBIAS, VRESET and VOFFSET) to generate one of several micromirror clocking pulse waveforms. The order of these micromirror clocking pulse waveform events is controlled externally by the logic control inputs and timed by the STROBE signal. DLPC410 automatically detects the DMD type and then uses the DMD type to determine the appropriate micromirror clocking pulse waveform.

A direct micromirror clocking pulse operation causes a mirror to transition directly from one latched state to the next. The address must already be set up on the mirror electrodes when the micromirror clocking pulse is initiated. Where the desired mirror display period does not allow for time to set up the address, a micromirror clocking pulse with release can be performed. This operation allows the mirror to go to a relaxed state regardless of the address while a new address is set up, after which the mirror can be driven to a new latched state.

A mirror in the relaxed state typically reflects light into a system collection aperture and can be thought of as *off* although the light is likely to be more than a mirror latched in the *off* state. Carefully evaluate the impact of relaxed mirror conditions on optical performance.

7.3.5 Measurement Conditions

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 14 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the DMD is capable of driving. All rise and fall transition timing parameters are referenced to $V_{IL(max)}$ and $V_{IH(min)}$ for input clocks, $V_{OL(max)}$ and $V_{OH(min)}$ for output clocks.

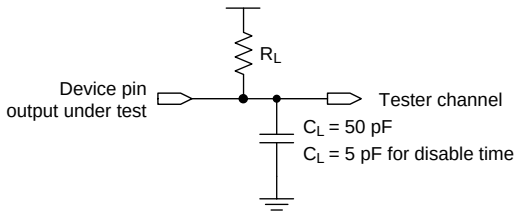

Figure 14. Test Load Circuit for AC Timing Measurements

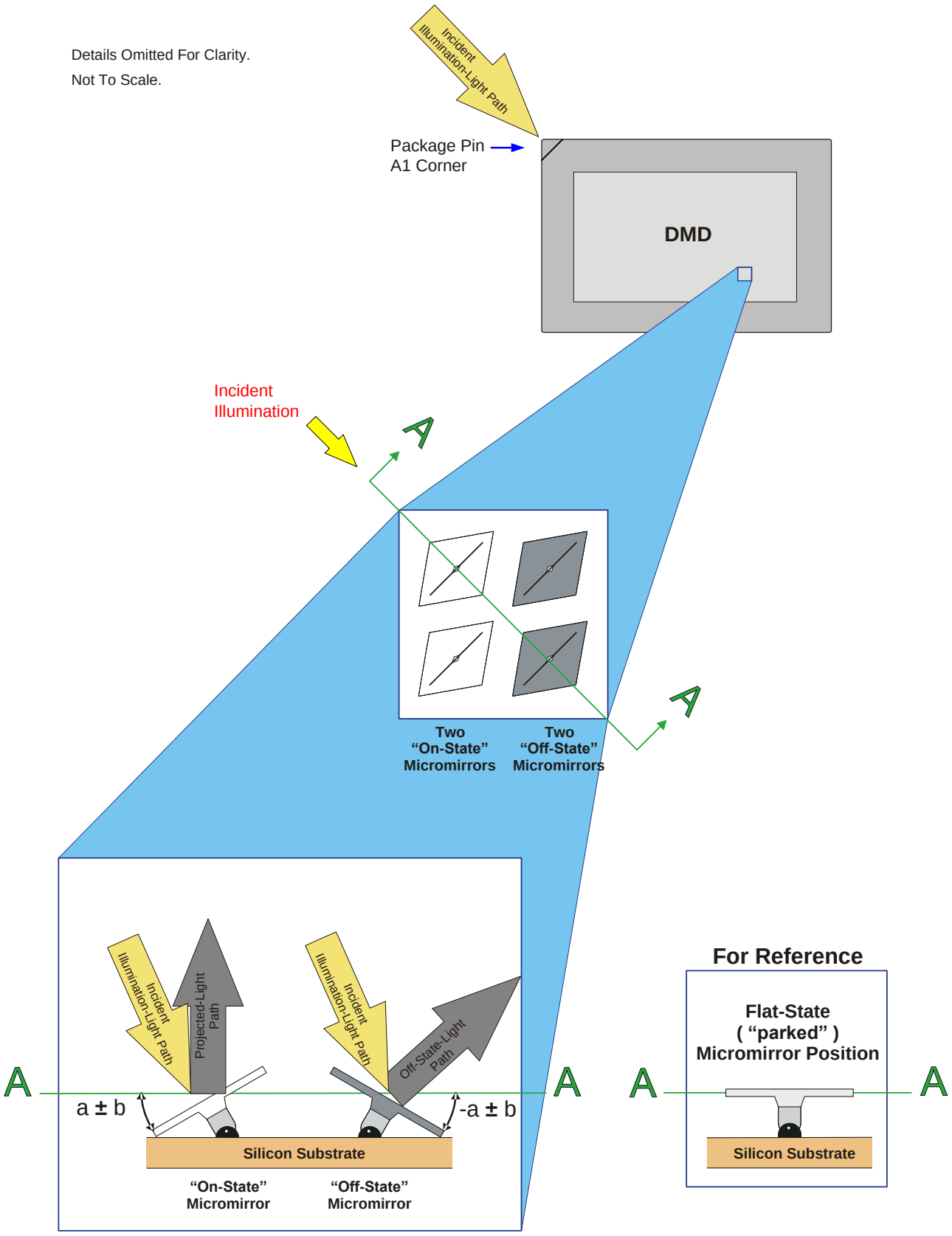

Figure 15. Micromirror Landed Positions and Light Paths

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7.4 Device Operational Modes

7.4.1 DMD Block Modes

When controlled by the DLPC410 controller in conjunction with the DLPA200 driver, the DLP650LNIR can be operated in four unique Block Modes. The DLP650LNIR is vertically segmented into 16 horizontal blocks, each 50 rows tall. Figure 16, Figure 17, Figure 18, and Figure 19 show how the DLPC410 can load and display an image using the different DMD Block Modes.

There are four Block Modes that determine which blocks are "reset" when a Micromirror Clocking Pulse command is issued:

- Single block mode
- Dual block mode
- Quad block mode
- Global mode

7.4.1.1 Single Block Mode

In Single Block Mode, any single block can be loaded with new data and then "reset" to its new mirror mechanical state when a Mirror Clocking Pulse is issued. This can be performed in any block order as long as the certain timing restrictions are met.

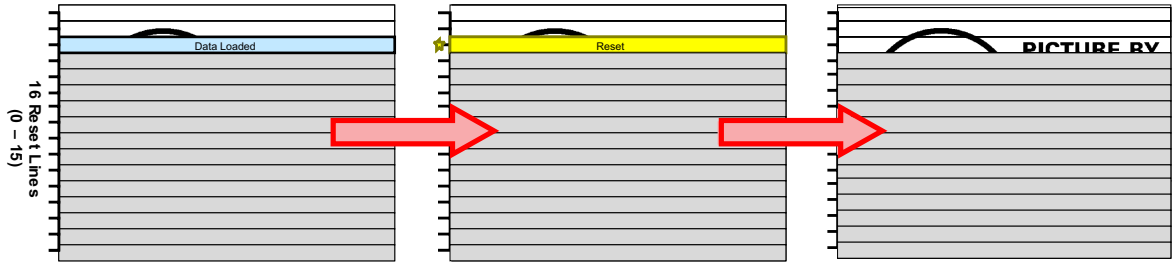

Figure 16. Single Block Mode Diagram

7.4.1.2 Dual Block Mode

In Dual Block Mode, the reset blocks of the DMD are grouped in to pairs such that the Mirror Clocking Pulse causes a pair of the DMD blocks to transition to their new states. In this mode, there are eight dual reset blocks paired together as follows (0-1), (2-3), (4-5), (6-7), (8-9), (10-11), (12-13), (14-15). Each dual group can be randomly addressed and reset. These pairs can be reset in any order by presenting the correct block mode commands to the DLPC410. After data is loaded into both groups, a pair can be reset to transfer the information to the mechanical state of the mirrors. Then another pair can be loaded and reset, etc.

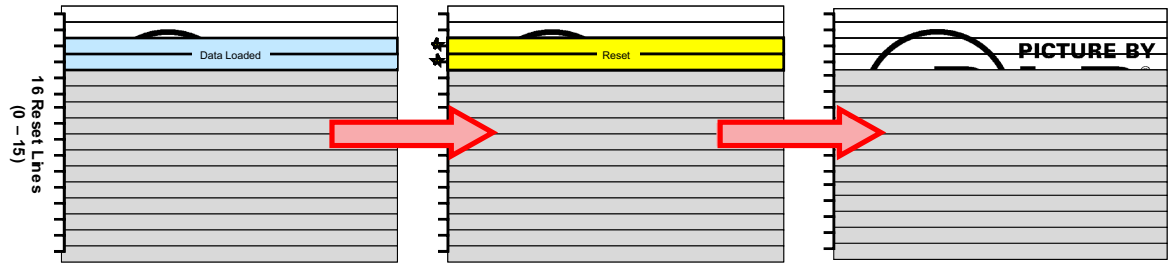

Figure 17. Dual Block Mode Diagram

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Device Operational Modes (continued)

7.4.1.3 Quad Block Mode

In Quad Block Mode, blocks of four are grouped together to receive the Mirror Clocking Pulse at the same time. In this mode, there are be 4 groups of four block each as follows (0-3), (4-7), (8-11) and (12-15). Each quad group can be randomly addressed and reset. After a quad group is loaded, it can be reset to transfer the information to the mechanical state of the mirrors.

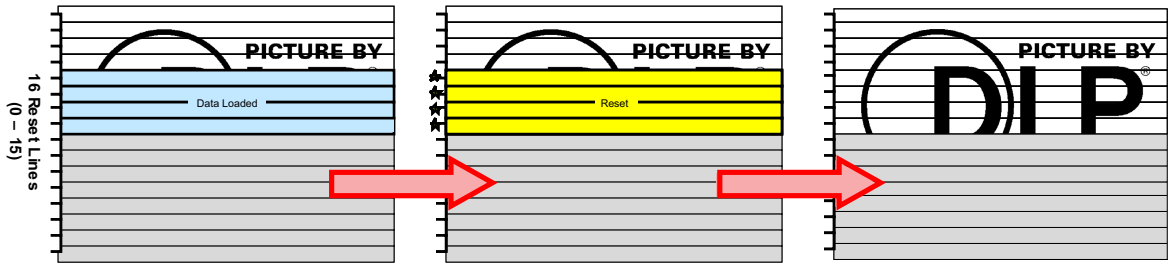

Figure 18. Quad Block Mode Diagram

7.4.1.4 Global Mode

In global mode, all 16 reset blocks are grouped into a single large group and reset together. The entire DMD must be loaded with the desired data before issuing a Global Reset to transfer the information to the mechanical state of the mirrors.

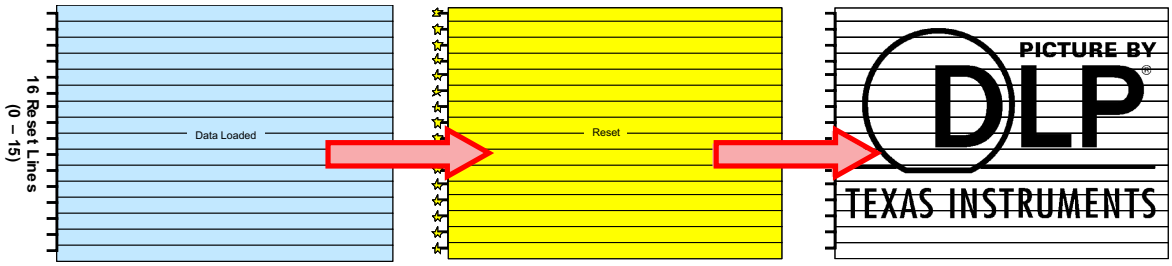

Figure 19. Global Mode Diagram

7.4.2 DMD Load4 Mode

Load4 Mode is a special data loading function of the DLP650LNIR DMD which is supported by the DLPC410 Controller. This mode allows the DLPC410 (an hence, the end user) to load the DMD faster at the expense of vertical resolution. In Load4 Mode, the device loads each horizontal line of data presented by the DLPC410 to the DLP650LNIR into 4 consecutive rows of the DMD. For example, assuming the DLPC410 presents the first row of new data to row 0 of the DMD, If Load4 is enabled then the device loads this single row of new input data into each of the first 4 rows (0-3) of the DMD. The device loads the next row presented to the DMD into the next 4 rows of the DMD (4-7), and so on.

Take precautions when using Load4 mode with the DLP650LNIR DMD, as each reset block of this DMD is 50 rows which is not evenly divisible by 4. Therefore, loading the last two rows of an even number block concurrently loads the first two rows in the subsequent odd number block. Conversely, to load an odd block, the last two rows of the preceding even number block need to be loaded first. See the DLPC410 datasheet for more information on how Load4 mode operates.

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7.5 Feature Description

7.5.1 Power Interface

The DLP650LNIR DMD requires three DC input voltages: V_{CC}, V_{CCI}, and V_{CC2}. It is typically allowable for V_{CC} and V_{CCI} to be provided by the same 3.3VDC power source. V_{CC2} is created by the DLPA200 DMD micromirror driver. The DLPA200 also creates other voltages (V_{BIAS}, V_{OFFSET}, and V_{RESET}) which it uses internally in creating the Mirror Clocking Pulses provided to the DMD on the MBRST signals inputs. The Mirror Clocking Pulses (resets) are provided to the DMD to facilitate the micromirror transitions from one state to the next state.

7.5.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 5 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. Use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.6 Optical Interface and System Image Quality Considerations

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.6.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.6.2 Numerical Aperture and Stray Light Control

Maintain the angle defined by the numerical aperture of the illumination optics at the DMD optical area to be the same angle implemented for the projection optics. Do not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination, projection pupils, or both to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the *ON* optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

7.6.3 Pupil Match

TI recommends the exit pupil of the illumination is nominally centered within 2° (two degrees) of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

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Optical Interface and System Image Quality Considerations (continued)

7.6.4 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be included in the projected image. To reduce DMD heating when applying high incident flux levels to the DMD in high power applications, design the illumination optics to limit light flux incident anywhere outside the active array to nearly zero percent. For lower incident power levels, depending on the optical architecture of a particular system, the acceptability levels of overfill light must be determined by the user as it relates to a specific application. In most cases it is almost always held to zero.

7.7 Micromirror Temperature Calculations

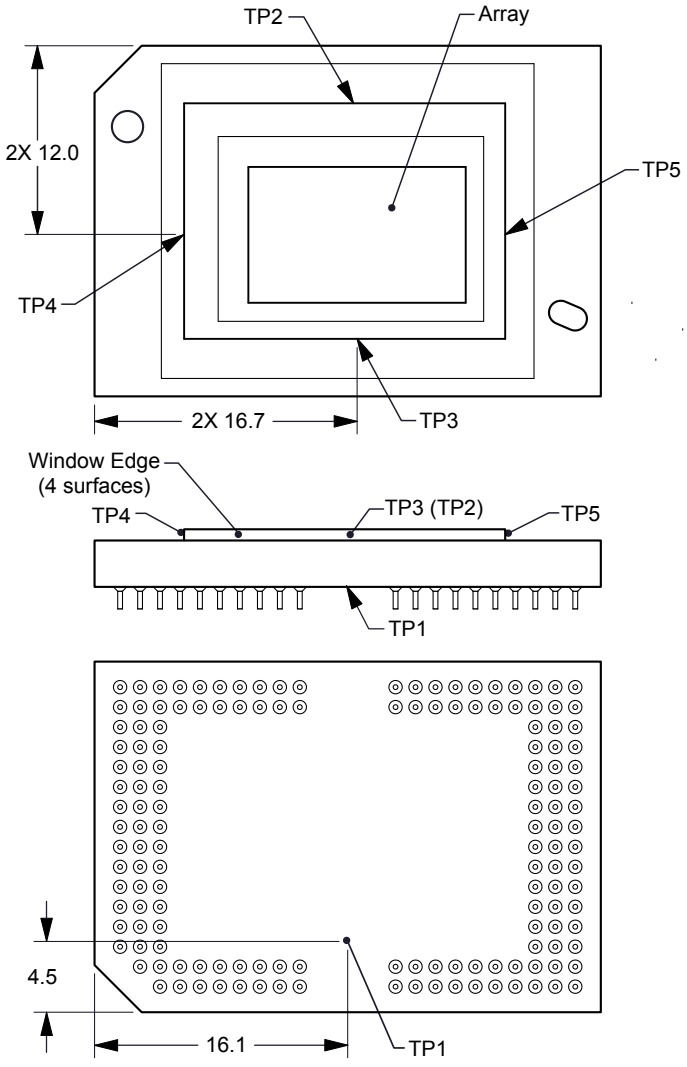

Figure 20. DMD Thermal Test Points

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Micromirror Temperature Calculations (continued)

The DMD Micromirror temperature cannot be measured directly, therefore it must be computed analytically from:

- the measurement point on the outside of the package
- the silicon-to-ceramic thermal resistance
- the mirror-to-silicon thermal resistance
- the internally generated electrical power
- and the illumination heat load

The relationship between mirror temperature and the reference ceramic temperature (thermal test TP1 in Figure 20) is provided by the following equations:

$$T_{MIRROR} = T_{CERAMIC} + Delta_T_{SILICON\text{-}TO\text{-}CERAMIC} + Delta_T_{MIRROR\text{-}TO\text{-}SILICON}$$

$$Delta_T_{SILICON\text{-}TO\text{-}CERAMIC} = Q_{SILICON} \times R_{SILICON\text{-}TO\text{-}CERAMIC}$$

$$Delta_T_{MIRROR\text{-}TO\text{-}SILICON} = Q_{MIRROR} \times R_{MIRROR\text{-}TO\text{-}SILICON}$$

$$Q_{SILICON} = Q_{ELECTRICAL} + (\alpha_{DMD} \times Q_{INCIDENT})$$

$$Q_{MIRROR} = Q_{INCIDENT_MIRROR} \times [FF_{OFF\text{-}STATE_MIRROR} \times (1 - MR)] \quad (1)$$

$$\alpha_{DMD} = [FF_{OFF\text{-}STATE_MIRROR} \times (1\text{-}MR)] + [1\text{-}FF_{OFF\text{-}STATE\text{-}MIRROR}] + [2 \times \alpha_{WINDOW}] \quad (2)$$

where:

- T_{MIRROR} = computed micromirror temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature (°C) (TP1 location)
- $Delta_T_{SILICON\text{-}TO\text{-}CERAMIC}$ = temperature rise of silicon above ceramic test point TP1
- $Delta_T_{MIRROR\text{-}TO\text{-}SILICON}$ = temperature rise of an individual mirror above the silicon (°C)
- $R_{SILICON\text{-}TO\text{-}CERAMIC}$ = thermal resistance, silicon die to ceramic TP1 (°C/Watt) as specified in Thermal Information
- $R_{MIRROR\text{-}TO\text{-}SILICON}$ = thermal resistance, individual mirror to silicon die (°C/Watt) as specified in Thermal Information
- $Q_{SILICON}$ = total DMD power (electrical + absorbed) on the silicon (Watts)
- Q_{MIRROR} = absorbed heat load on a single mirror (Watts)
- $Q_{ELECTRICAL}$ = nominal electrical power (Watts)
- $Q_{INCIDENT}$ = total incident optical power to DMD (Watts)
- $Q_{INCIDENT_MIRROR}$ = Incident optical power on an individual mirror (Watts)
- α_{DMD} = absorptivity of DMD
- α_{WINDOW} = absorptivity of DMD window (single pass)
- $FF_{OFF\text{-}STATE\text{-}MIRROR}$ = DMD off-state mirror fill factor
- MR = DMD mirror reflectivity

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a system operating at 1064 nm with 100% of the illumination contained within the 1280 × 800 active array mirrors. Silicon-to-ceramic thermal resistance assumes the entire active micromirror array is uniformly illuminated.

NOTE

Incident irradiation that concentrates on a subset of the micromirror array, results in an increase in effective package thermal resistance.

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Micromirror Temperature Calculations (continued)

7.7.1 Sample Calculation 1: Uniform Illumination of Entire DMD Active Array (1280 × 800 pixels)

This calculation assumes that the entire DMD active array (1280 × 800) mirrors is uniformly illuminated with zero overfill falling outside the Pond of Mirrors pixel border. The highest DMD temperatures typically occur when the DMD mirrors are in the off-state (–12° landed) position. Therefore, the off-state fill factor calculates the worst case mirror temperature. Calculate the mirror temperatures to assess the viability of the illumination conditions.

- $FF_{OFF\text{-}STATE\text{-}MIRROR}$ = 75.3%
- MR @ 1064 nm = 94%
- α_{WINDOW}@ 1064 nm = 0.7%
- $R_{MIRROR\text{-}TO\text{-}SILICON}$ = 3.39E5 °C/Watt
- $R_{SILICON\text{-}TO\text{-}CERAMIC}$ = 0.5 °C/Watt
- Array Resolution = 1280 × 800
- $T_{CERAMIC}$ = 30.0°C (measured)
- $Q_{INCIDENT}$ = 160 W (measured)
- $Q_{ELECTRICAL}$ = 1.8 W

α_{DMD} = [0.753 × (1-0.94)] + (1 - 0.753) + (2 × 0.007) = 0.31

$Q_{SILICON}$ = 1.8 W + (0.31 × 160 W) = 51.4 W

Q_{MIRROR} = [(160W / (1280 × 800)] × 0.753 × (1 - 0.94) = 7.06E-6 W

$Delta_T_{SILICON\text{-}TO\text{-}CERAMIC}$ = 51.4 W × 0.5°C/W= 25.7°C

$Delta_T_{MIRROR\text{-}TO\text{-}SILICON}$ = 7.06E-6 W × 3.39E5 °C/W= 2.4°C

T_{MIRROR} = 30.0°C + 25.7 + 2.4°C = **58.1°C**

7.7.2 Sample Calculation 2: Partial DMD Active Array Illumination with Non-uniform Illumination Peak

This calculation assumes that only a subsection of the DMD active array 960 × 475 pixels in size is (non-uniformly) illuminated. This calculation assumes the illuminated area is in the center of the DMD. Non-centered area can affect the value of $R_{SILICON\text{-}TO\text{-}CERAMIC}$. If the application requires offsetting the illumination on the DMD, contact TI for more information on how to assess $R_{SILICON\text{-}TO\text{-}CERAMIC}$. As in Sample Calculation 1, the off-state fill factor can be used to assess the highest temperatures that can occur. Calculate the mirror temperatures which occur at the highest illumination intensities to assess the viability of the illumination conditions.

- $FF_{OFF\text{-}STATE\text{-}MIRROR}$ = 75.3%
- MR @ 1064 nm = 94%
- α_{WINDOW}@ 1064 nm = 0.7%
- $R_{MIRROR\text{-}TO\text{-}SILICON}$ = 3.39E5 °C/Watt
- $R_{SILICON\text{-}TO\text{-}CERAMIC}$ = 0.9 °C/Watt (higher than previous example due to reduced illumination area)
- Pixel Size = 10.8 µm = 0.00108 cm (square)
- $T_{CERAMIC}$ = 30.0°C (measured)
- $Q_{INCIDENT}$ = 60 W (measured)
- $Q_{ELECTRICAL}$ = 1.8 W
- Peak Irradiance = 500 W/cm^2 (measured)

α_{DMD} = [0.753 × (1 - 0.94)] + (1 - 0.753) + (2 × 0.007) = 0.31

$Q_{SILICON}$ = 1.8 W + (0.31 × 60 W) =20.4 W

$Q_{INCIDENT_MIRROR}$ = Peak Irradiance (W/cm^2) × Pixel Area (cm^2) = [500 W/cm^2 × (0.00108 cm)^2] = 5.832E-4 W

Q_{MIRROR} = 5.832E-4 W × 0.753 × (1 - 0.94) = 2.64E-5 W

$Delta_T_{SILICON\text{-}TO\text{-}CERAMIC}$ = 20.4 W × 0.9°C/W = 18.4°C

$Delta_T_{MIRROR\text{-}TO\text{-}SILICON}$ = 2.64E-5 W × 3.39E5°C/W= 8.9°C

T_{MIRROR} = 30.0°C + 18.4°C + 8.9°C = **57.3°C**

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7.8 Micromirror Landed-On/Landed-Off Duty Cycle

7.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time (and in the Off state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Because a micromirror can be landed in only one of the two available states (on or off), the two numbers (percentages) always add to 100.

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Micromirror Landed-On/Landed-Off Duty Cycle (continued)

7.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce usable life of the DMD.

Note that it is the symmetry and asymmetry of the landed duty cycle that are of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the useable life of the DMD, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the useable life of the DMD. This is quantified in the de-rating curve shown in Figure 2. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature at a given long-term average Landed Duty Cycle.

7.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel experiences a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel experiences a 0/100 Landed Duty Cycle.

Between the two extremes, the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 7.

Table 7. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLP650LNIR devices require they be coupled with the DLPC410 controller to provide a reliable solution for many different applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC410. Applications of interest include 3D Printing, Selective Laser Sintering (SLS), Dynamic Grayscale Laser Marking, Industrial Printing, Flexographic Printing, Digital Plate making, and Repair and Ablation.

8.1.1 Device Description

The DLP650LNIR WXGA chipset offers developers a convenient way to design a wide variety of industrial, medical, telecom and advanced display applications by delivering maximum flexibility in formatting data, sequencing data, and light patterns.

The DLP650LNIR WXGA chipset includes the following four components: DMD Digital Controller (DLPC410), EEPROM (DLPR410), DMD Micromirror Driver (DLPA200), and a DMD (DLP650LNIR).

DLPC410 Digital Controller for DLP Discovery 4100 chipset

- Provides high speed LVDS data and control interface to the DLP650LNIR.
- Drives mirror clocking pulse and timing information to the DLPA200.
- Supports random row addressing.

DLPR410 PROM for DLP Discovery 4100 chipset

- Contains startup configuration information for the DLPC410.

DLPA200 DMD Micromirror Driver

- Generates Micromirror Clocking Pulse control (sometimes referred to as a "Reset") of DMD mirrors.

DLP650LNIR DLP 0.65 WXGA NIR 2xLVDS DMD

- Steers light in two digital positions (+12º and -12º) using 1280 × 800 micromirror array of aluminum mirrors.

Table 8. DLPC410 Chipset Configuration for 0.65 WXGA NIR Chipset

QUANTITY	TI PART	DESCRIPTION
1	DLP650LNIR	DLP 0.65 WXGA NIR 2xLVDS DMD
1	DLPC410	Digital Controller for DLP Discovery 4100 chipset
1	DLPR410	PROM for DLP Discovery 4100 chipset
1	DLPA200	DMD Micromirror Driver

Reliable function and operation of DLP650LNIR WXGA chipsets require the components be used in conjunction with each other. This document describes the proper integration and use of the DLP650LNIR WXGA chipset components.

The DLP650LNIR WXGA chipset can be combined with a user programmable Application FPGA (not included) to create high performance systems.

8.2 Typical Application

A typical embedded system application using the DLPC410 controller and DLP650LNIR is shown in Figure 21. In this configuration, the DLPC410 controller supports input from an FPGA. The FPGA sends low-level data to the controller, enabling the system to be highly optimized for low latency and high speed.

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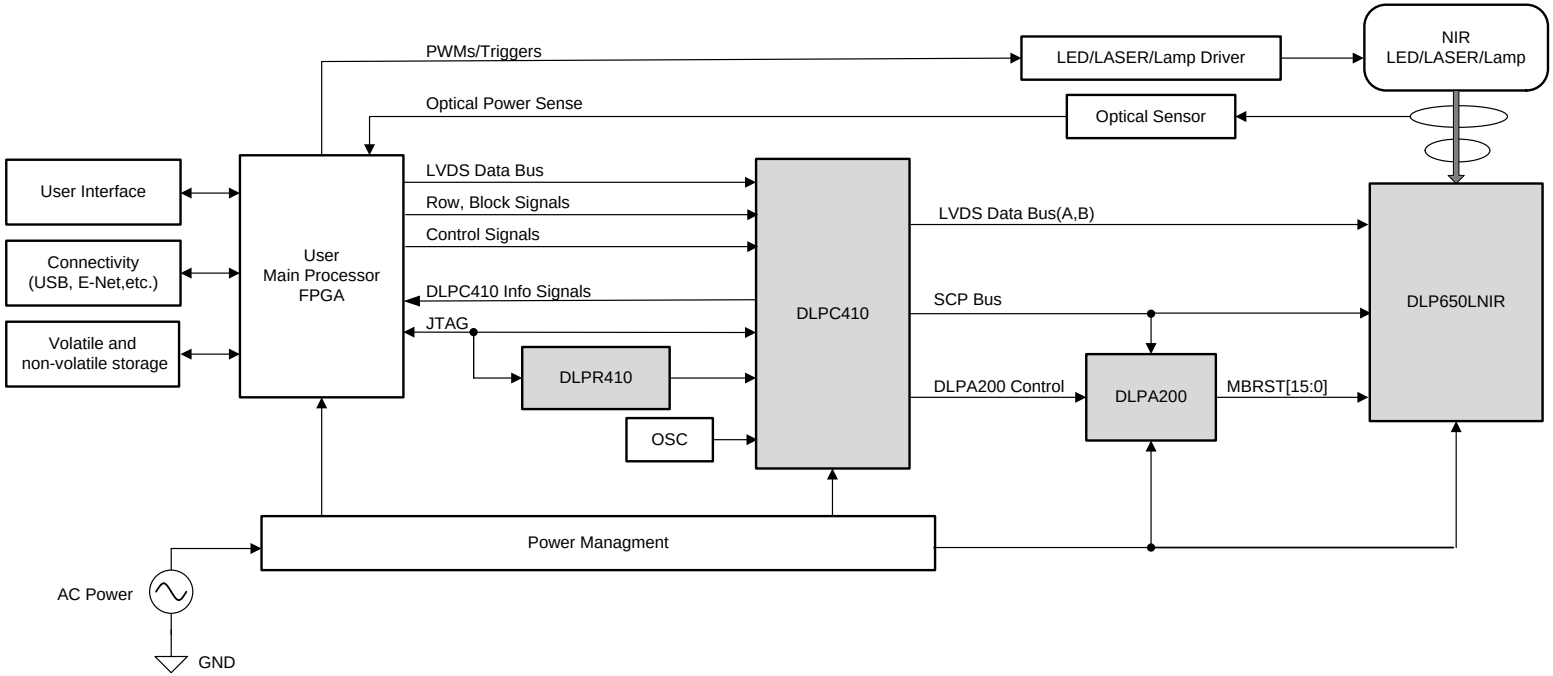

Figure 21. DLPC410 and DLP650LNIR Embedded Example Block Diagram

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8.2.1 Design Requirements

All applications using the DLP650LNIR WXGA chipset require both the controller and the DMD components for operation. The system also requires an external parallel flash memory device loaded with the DLPC410 Configuration and Support Firmware. The chipset has several system interfaces and requires some support circuitry. The following interfaces and support circuitry are required:

- DLPC410 System Interfaces:
  - Control Interface
  - Trigger Interface
  - Input Data Interface
  - Illumination Interface
  - Reference Clock
- DLP650LNIR Interfaces:
  - DLPC410 to DLP650LNIR Digital Data
  - DLPC410 to DLP650LNIR Control Interface
  - DLPC410 to DLP650LNIR Micromirror Reset Control Interface
  - DLPC410 to DLPA200 Micromirror Driver
  - DLPA200 to DLP650LNIR Micromirror Reset

8.2.2 Detailed Design Procedure

The DLP650LNIR DMD is well suited for Near-Infrared (NIR) light applications requiring fast, spatially programmable light patterns using the micromirror array. See the to see the connections between the DLP650LNIR DMD, the DLPC410 digital controller, the DLPR410 EEPROM, and the DLPA200 DMD micromirror drivers. See the Figure 21 for an application example. Follow the *Layout Guidelines* for reliability.

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9 Power Supply Recommendations

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. The DLP650LNIR power-up and power-down procedures are defined by the DLPC410 data sheet (DLPS024). These procedures must be followed to ensure reliable operation of the device.

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10 Layout

10.1 Layout Guidelines

The DLP650LNIR is a component of a chipset that is controlled by the DLPC410 in conjunction with the DLPA200. These guidelines refer to a PCB board with these components.

A target impedance of 50 Ω for single-ended signals and 100 Ω between LVDS signals is specified for all signal layers.

10.1.1 Impedance Requirements

Make sure to route signals to have a matched impedance of 50 Ω ±10% except for LVDS differential pairs (D_Xnn, DCLK_Xn, and SCTRL_Xn). Match the differential pairs to 100 Ω ±10% across each pair.

10.1.2 PCB Signal Routing

When designing a PCB for the DLP650LNIR controlled by the DLPC410 in conjunction with the DLPA200, the following are recommended:

Make sure that signal trace corners are no sharper than 45°. Make sure that adjacent signal layers have the predominate traces routed orthogonal to each other. TI recommends that critical signals be hand routed in the following order: DMD (LVDS signals), then DLPA200 signals.

TI does not recommend signal routing on power or ground planes.

TI does not recommend ground plane slots.

Make sure that high-speed signal traces do not cross over slots in adjacent power and/or ground planes.

Table 9. Important Signal Trace Constraints

SIGNAL	CONSTRAINTS
LVDS (D_Xnn, DCLK_xn, and SCTRL_xn)	P-to-N data, clock, and SCTRL: <10 mils (0.25 mm); Pair-to-pair <10 mils (0.25 mm); Bundle-to-bundle <2000 mils (50 mm, for example D_Ann to D_Bnn) Trace width: 4 mil (0.1 mm) Trace spacing: In ball field – 4 mil (0.11 mm); PCB etch – 14 mil (0.36 mm) Maximum recommended trace length <6 inches (150 mm)

Table 10. Power Trace Widths and Spacing

SIGNAL NAME	MINIMUM TRACE WIDTH	MINIMUM TRACE SPACING	LAYOUT REQUIREMENTS
GND	Maximize	5 mil (0.13 mm)	Maximize trace width to connecting pin as a minimum
VCC, VCC2	20 mil (0.51 mm)	10 mil (0.25 mm)	
MBRST[15:0]	11 mil (0.23 mm)	15 mil (0.38 mm)	

10.1.3 Fiducials

Make sure that the fiducials for automatic component insertion are 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

10.1.4 DMD Interface

The digital interface from the DLPC410 to the DMD are LVDS signals that run at clock rates up to 400 MHz. Data is clocked into the DMD on both the rising and falling edge of the clock, so the data rate is 800 MHz. Make sure the LVDS signals have 100 Ω differential impedance. Make sure the differential signals are length-matched and are as short as possible. Parallel termination at the LVDS receiver is in the DMD; therefore, on board termination is not necessary.

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10.1.4.1 Trace Length Matching

The DLPC410 DMD data signals require precise length matching. Make sure differential signals have impedance of 100 Ω (with 5% tolerance). It is important that the propagation delays are matched. The maximum differential pair uncoupled length is 100 mils with a relative propagation delay of ±25 mil between the p and n. Matching all signals exactly maximizes the channel margin. The signal path through all boards, flexible cables and internal DMD routing must be considered in this calculation.

10.1.5 DLP650LNIR Decoupling

Make sure to distribute general decoupling capacitors for the DLP650LNIR around the PCB and place them to minimize the distance from device voltage and ground pads. Each decoupling capacitor (0.1 µF recommended) needs vias directly to the ground and power planes. Via sharing between components (discreet or integrated) is discouraged. Tie the power and ground pads of the DLP650LNIR to the voltage and ground planes with their own vias.

10.1.5.1 Decoupling Capacitors

Place decoupling capacitors so that they minimize the distance from the decoupling capacitor to the supply and ground pin of the component. Follow these specific guidelines:

- Locate the supply voltage pin of the capacitor close to the DMD supply voltage pin(s). The decoupling capacitor needs vias to ground and voltage planes. The DMD can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1 inch. Otherwise, tie the component to the voltage or ground plane through separate vias.
- Make sure that the trace lengths of the voltage and ground connections for decoupling capacitors and components is less than 0.1 inch to minimize inductance.
- Make the trace width of the power and ground connection to decoupling capacitors and components as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.

10.1.6 VCC and VCC2

Connect the VCC pins of the DMD directly to the DMD VCC plane. Distribut the decoupling for the VCC around the DMD and placed to minimize the distance from the voltage and ground pads. Each decoupling capacitor needs vias directly connected to the ground and power planes. Tie the VCC and GND pads of the DMD to the VCC and ground planes with their own vias.

The VCC2 voltage can be routed to the DMD as a wide trace. Place decoupling capacitors to minimize the distance from the VCC2 and ground pads of the DMD. Use wide etch from the decoupling capacitors to the DMD connection to reduce inductance and improves decoupling performance.

10.1.7 DMD Layout

See the respective sections in this data sheet for package dimensions, timing and pin out information.

10.1.8 DLPA200

The DLPA200 driver generates the micromirror clocking pulses for the DMD. Route the DMD-drive outputs from the DLPA200 (MBRST[15:0] with a minimum trace width of 11 mil and a minimum spacing of 15 mil. Route the VCC and VCC2 traces from the output capacitors to the DLPA200 with a minimum trace width and spacing of 11 mil and 15 mil, respectively. See the DLPA200 customer data sheet for mechanical package and layout information.

10.2 Layout Example

For LVDS (and other differential signal) pairs and groups, it is important to match trace lengths. In the area of the dashed lines, Figure 22 shows correct matching of signal pair lengths with serpentine sections to maintain the correct impedance.

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Layout Example (continued)

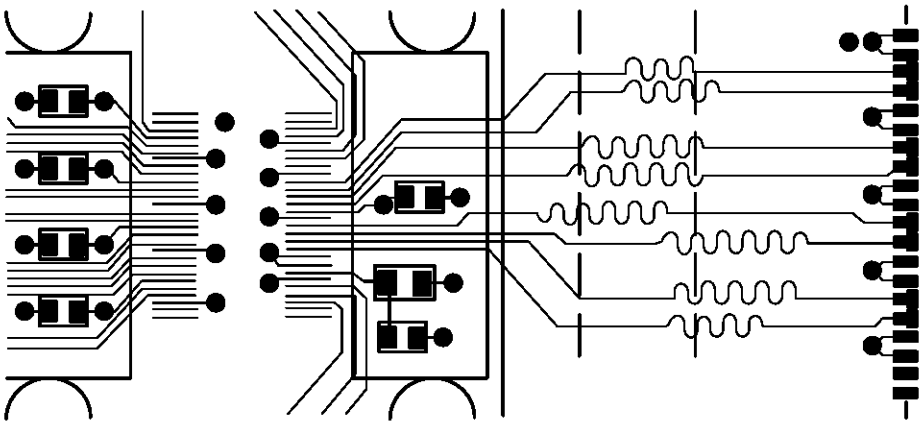

Figure 22. Mitering LVDS Traces to Match Lengths

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

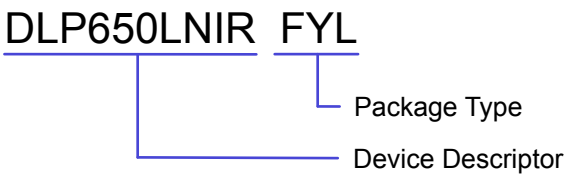

图 **23.** 器件型号 说明

11.1.2 器件标记

器件标记包括人类可读的信息和二位条码。图 24 中显示了人类可读信息。二维矩阵码是一个字母数字字符串，其中包含 DMD 部件号、序列号的第 1 部分和序列号的第 2 部分。DMD 序列号（第 1 部分）的首字符为制造年份。DMD 序列号（第 1 部分）的第二个字符为制造月份。

示例：DLP650LNIRFYL GHXXXXX LLLLLLM

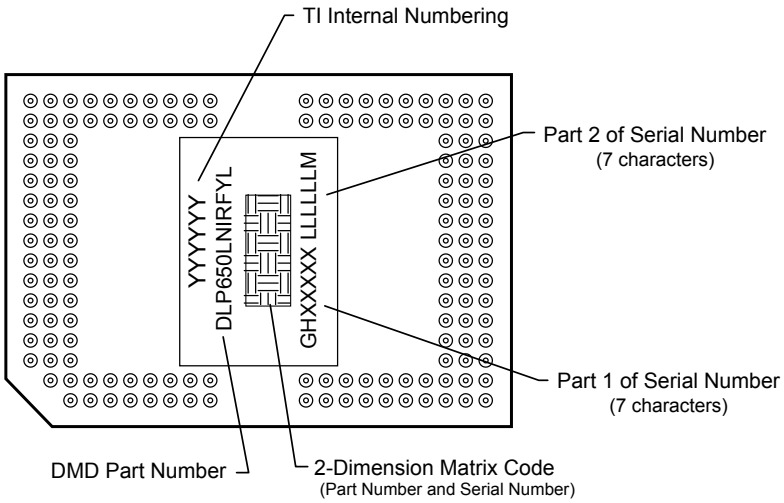

图 **24. DMD** 标记位置

11.2 文档支持

11.2.1 相关文档

以下文档包含与 DLP650LNIR 一起使用的芯片组组件相关的更多信息：

- 《DLPC410 DMD 数字控制器数据表》
- 《DLPR410 配置 PROM 数据表》
- 《DLPA200 DMD 微镜驱动器数据表》

11.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

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相关链接 **(**接下页**)**

表 **11.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
DLP650LNIR	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
DLPA200	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
DLPC410	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
DLPR410	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.6 商标

E2E is a trademark of Texas Instruments.

11.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP650LNIRFYL	Active	Production	CLGA (FYL) | 149	33 | JEDEC TRAY (5+1)	Yes	NIPDAU	N/A for Pkg Type	0 to 70	
DLP650LNIRFYL.B	Active	Production	CLGA (FYL) | 149	33 | JEDEC TRAY (5+1)	Yes	NIPDAU	N/A for Pkg Type	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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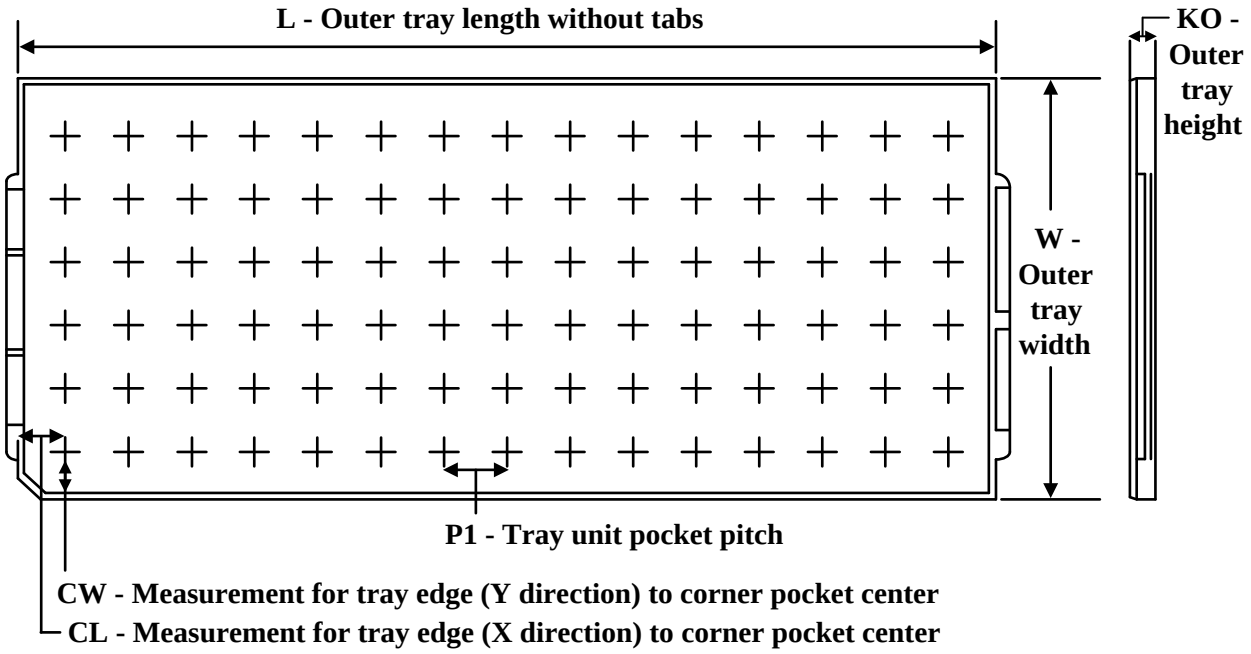
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP650LNIRFYL	FYL	CLGA	149	33	3 x 11	150	315	135.9	12190	27.5	20	27.45
DLP650LNIRFYL.B	FYL	CLGA	149	33	3 x 11	150	315	135.9	12190	27.5	20	27.45

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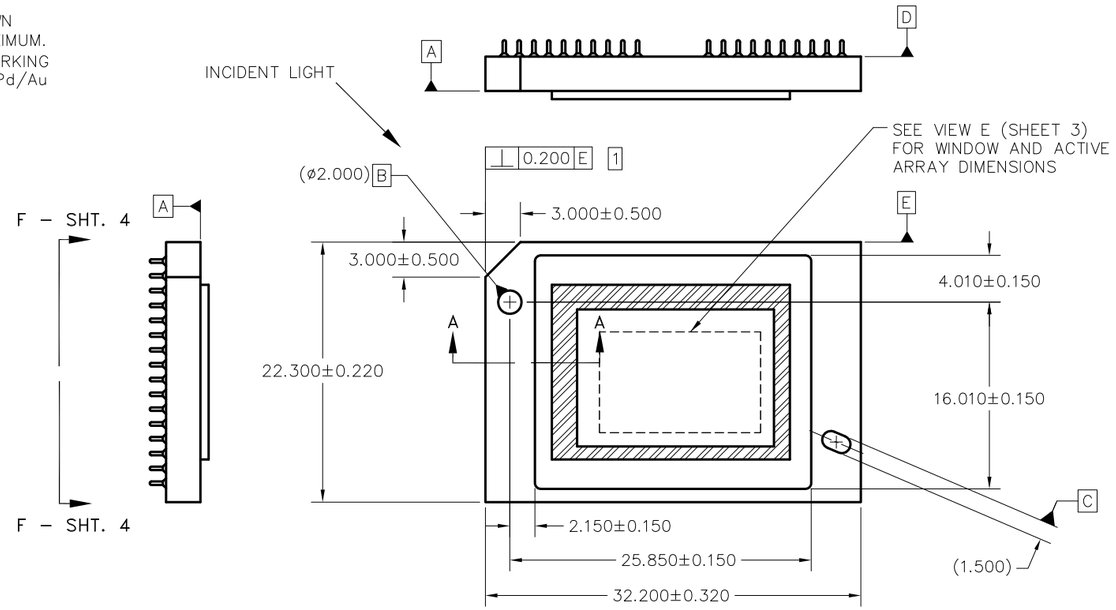
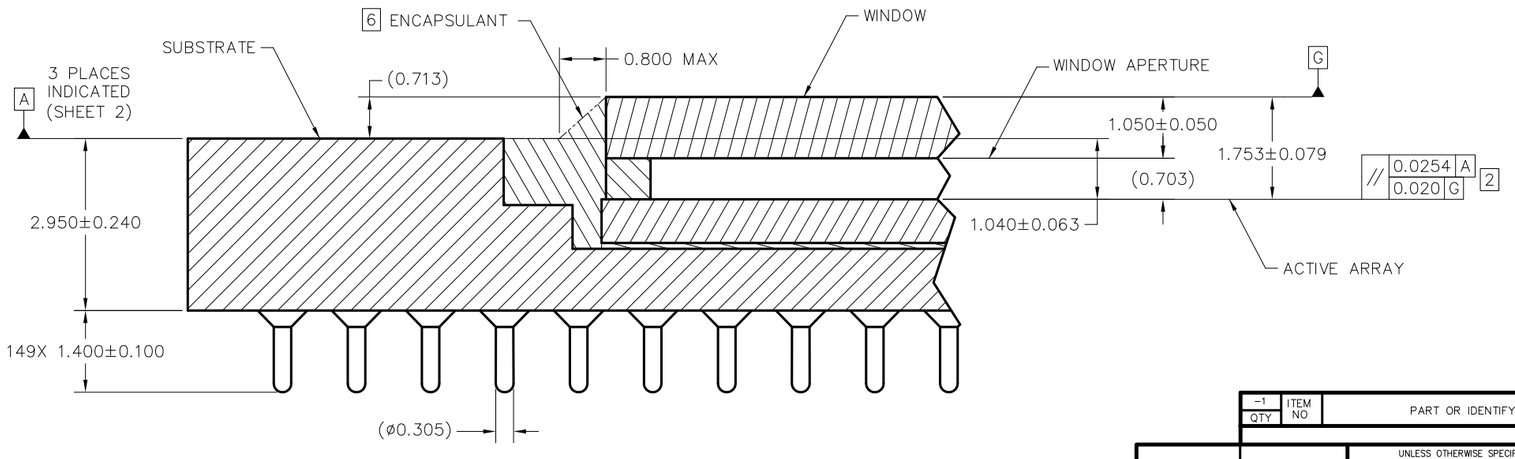
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2022283, INITIAL RELEASE	02/07/12	F. ARMSTRONG
B	ECO 2123271, CHG TO LARGE SYMBOLIZATION PAD	03/16/12	F. ARMSTRONG
C	ECO 2135104, ADD NOTE 8 TO SHEETS 1 & 4	08/02/13	F. ARMSTRONG
D	ECO 2168423, ADD FYL PACKAGE TO TITLE	08/17/17	M. AVERY

NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
5. MAXIMUM ENCAPSULANT PROFILE SHOWN
6. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
7. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.





SECTION A–A
SCALE 20/1

–1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5–1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

DWN F. ARMSTRONG DATE 02/07/12
ENGR F. ARMSTRONG 02/07/12
QA P. KONRAD
CQE M. DORAK

TEXAS INSTRUMENTS
Dallas, Texas

ICD, MECHANICAL, DMD
.65 WXGA–800 2xLVDS V2
SERIES 450 (FYL PACKAGE)

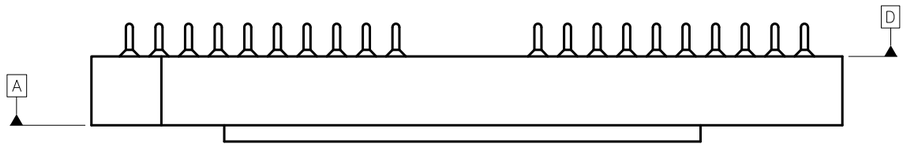
THIRD ANGLE PROJECTION

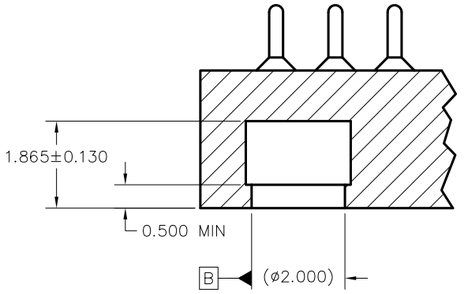
NEXT ASSY	USED ON
NONE	0314DA

APPLICATION

SIZE D | DRAWING NO 2512372 | REV D
SCALE 4/1 | SHEET 1 OF 4

ACED1g





SECTION C–C
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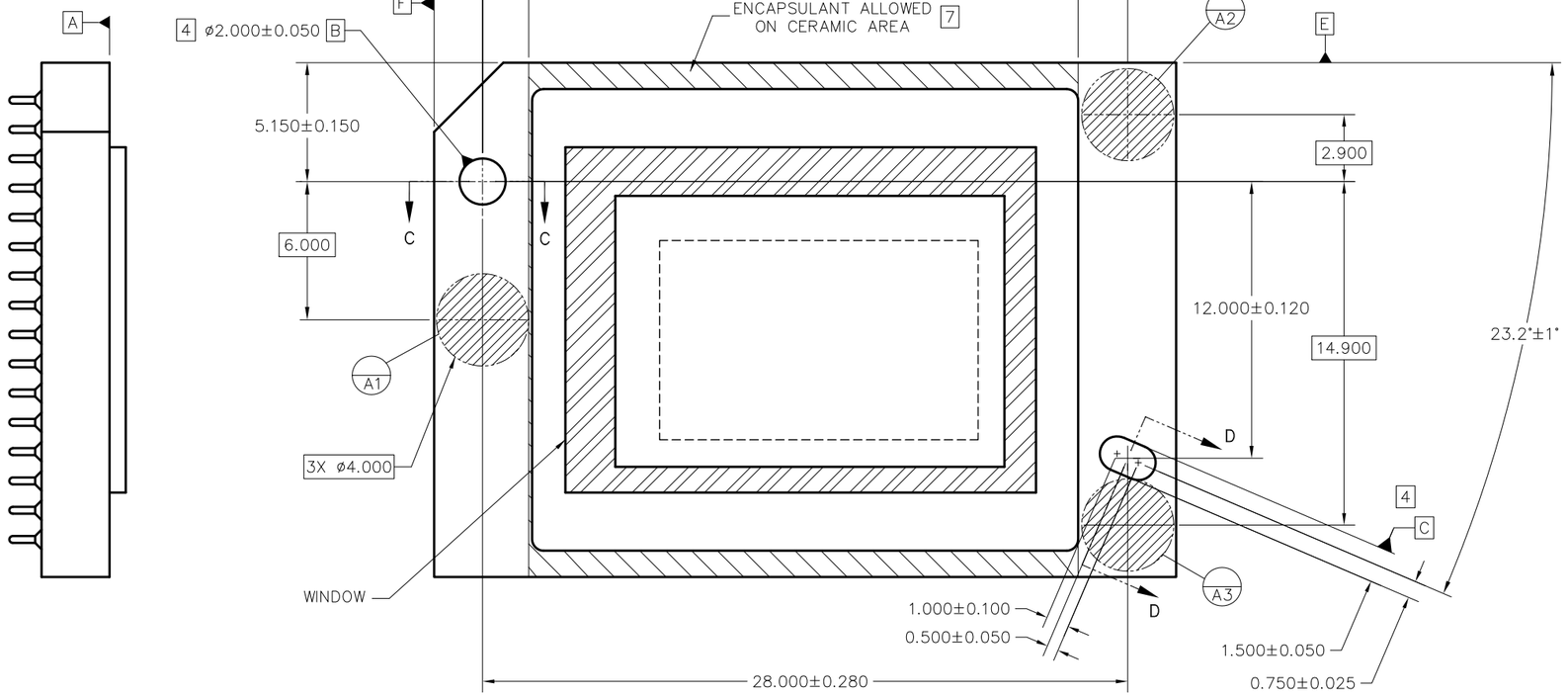
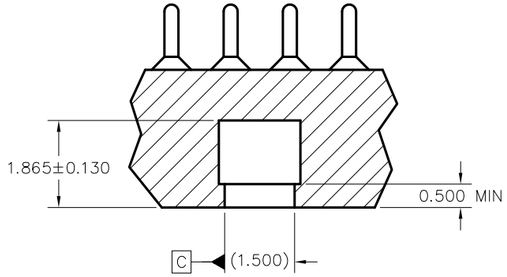
SCALE 16/1



VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION D–D
DATUM C
SCALE 16/1

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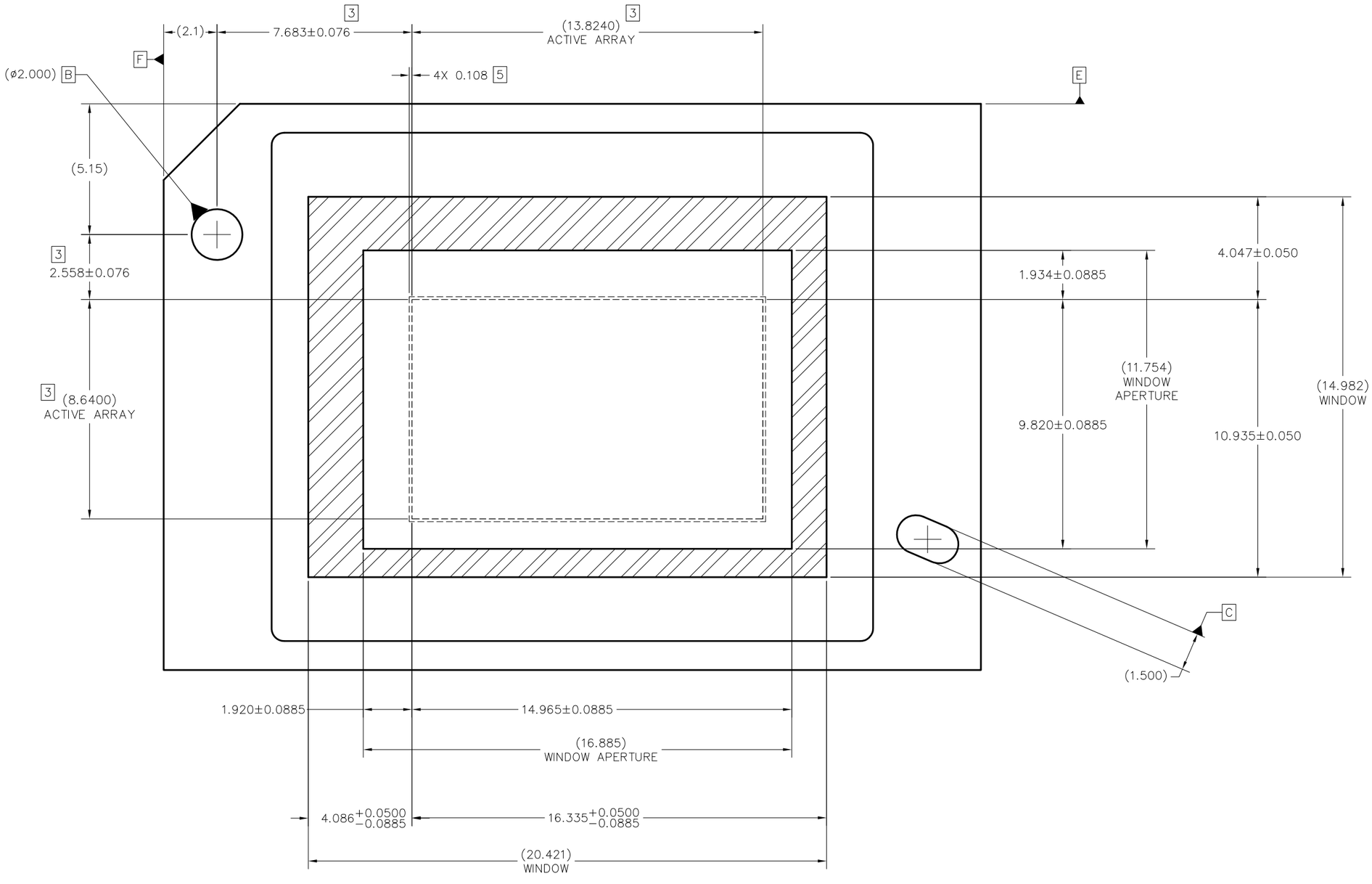
		SCALE 4/1	SHEET 2	

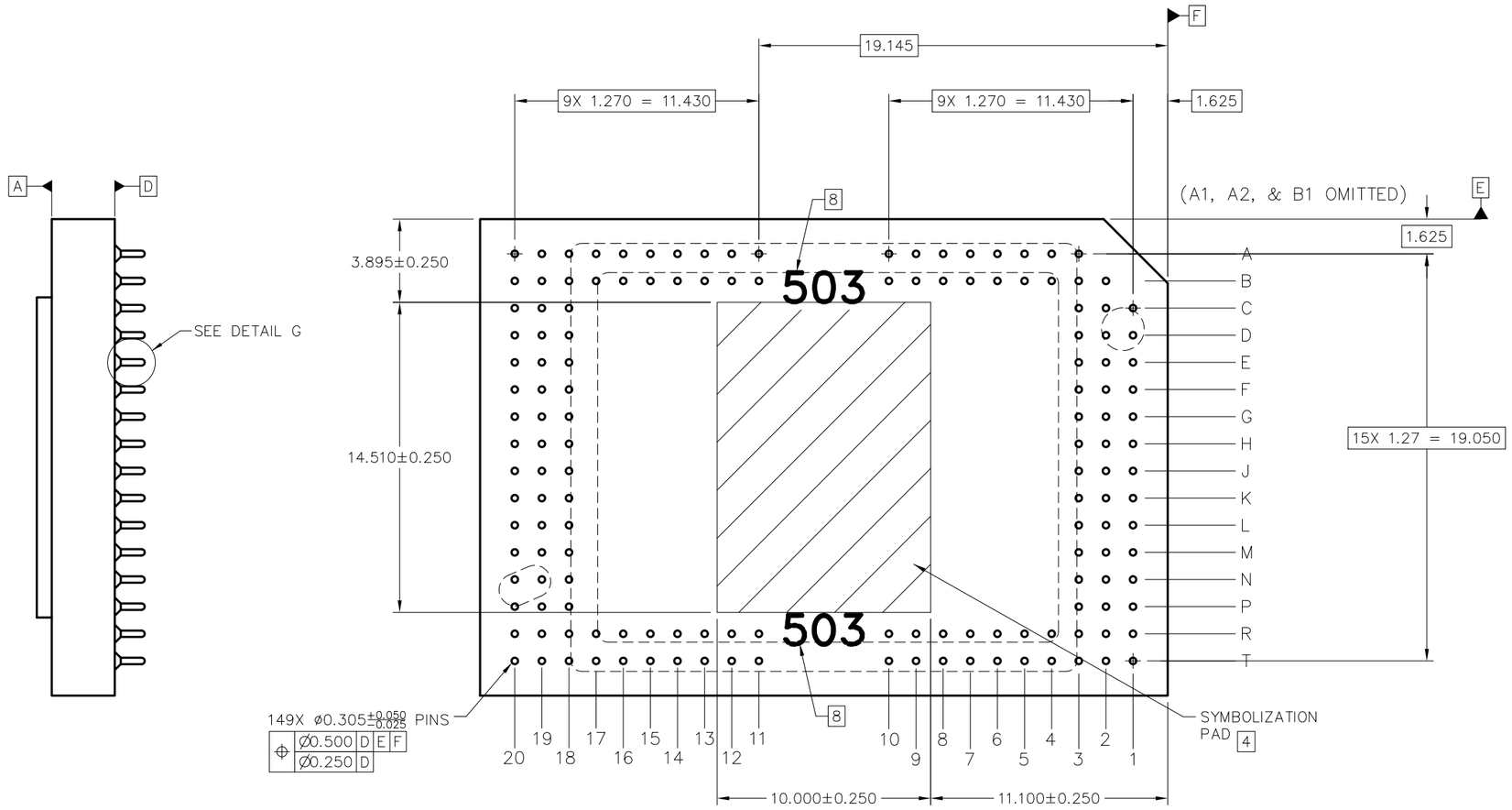
ACED2c



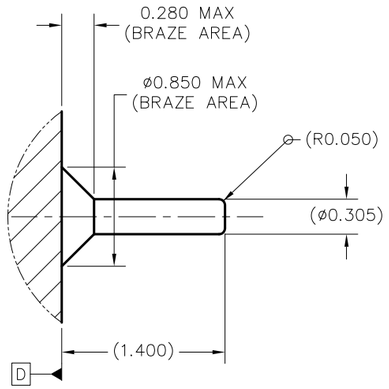
VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

Texas Instruments, Dallas, Texas	DWN DATE	SIZE D	DRAWING NO 2512372	REV D
	ISSUE DATE	SCALE 4/1	SHEET 3	

ACED2c



VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1



DETAIL G (149 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

Texas Instruments, Dallas, Texas	DWN	DATE	SIZE D	DRAWING NO 2512372 REV D
	ISSUE DATE		SCALE 4/1	SHEET 4

ACED2c

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最后更新日期：2025 年 10 月