16-Channel, Current-Input Analog-to-Digital Converter

FEATURES

- **SINGLE-CHIP SOLUTION TO MEASURE 16 LOW-LEVEL CURRENTS**
- **INTEGRATING I-TO-V CONVERSION FRONT-END**
- **PROGRAMMABLE FULL-SCALE : 3pC to 12pC**
- **ADJUSTABLE SPEED:**
  - **Data Rate Up To 100kSPS**
  - **Integration Time Down To 10μs**
- **ANALOG SUPPLY: +5V**
- **DIGITAL SUPPLY: +3.3V**

APPLICATIONS

- **CT SCANNER DAS**
- **PHOTODIODE SENSORS**
- **X-RAY DETECTION SYSTEMS**

Protected by US Patent #5841310

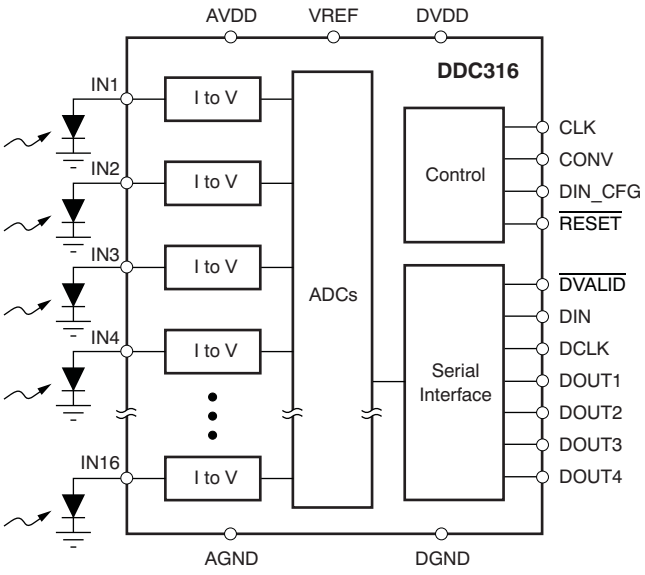
DESCRIPTION

The DDC316 is a 16-bit, 16-channel, current-input analog-to-digital converter (ADC). It combines both current-to-voltage and analog-to-digital (A/D) conversion so that 16 separate low-level current output devices (such as photodiodes) can be directly connected to its inputs and digitized.

For each of the 16 inputs, the DDC316 provides a dual-switched integrator front-end. This configuration allows for continuous current integration: while one integrator is being digitized by the on-chip ADC, the other is integrating the input current. Adjustable integration times range from 10μs to 1ms.

The DDC316 provides a serial interface of the output data, either multiplexed onto a single data output pin or parallel on four output pins. The output mode can be selected based on the available integration time.

The DDC316 uses a +5V analog supply and a +3.3V digital supply. Operating over the temperature range of 0°C to +70°C, the DDC316 is offered in a BGA-64 package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

AVDD to AGND	–0.3V to +6V
DVDD to DGND	–0.3V to +3.6V
AGND to DGND	±0.2V
VREF Input to AGND	2.0V to AVDD + 0.3V
Analog Input to AGND	–0.3V to +0.7V
Digital Input Voltage to DGND	–0.3V to DVDD + 0.3V
Digital Output Voltage to DGND	–0.3V to AVDD + 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	–60°C to +150°C
Junction Temperature (T_J)	+150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

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ELECTRICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +5V, DVDD = +3.3V, VREF = +4.096V, t_{INT} = 20µs, Range = 12pC, Format = 16 bits, CLK = 40MHz, and $\overline{HI_SPEED}$ Bit = 1, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DDC316 MIN	DDC316 TYP	DDC316 MAX	UNIT
ANALOG INPUT RANGE					
Range 1		2.4	3	3.6	pC
Range 2		4.8	6	7.2	pC
Range 3		9.6	12	14.4	pC
Negative Full-Scale Range		–1.786% of Positive Full-Scale Range			pC
DYNAMIC CHARACTERISTICS					
Data Rate				100	kSPS
Integration Time, t_{INT}	$\overline{HI_SPEED}$ Bit = 1	20		1,000	µs
	$\overline{HI_SPEED}$ Bit = 0	10		20	µs
System Clock Input		1		40	MHz
Data Clock (DCLK)				40	MHz
	Daisy-Chain Readback			20	MHz
ACCURACY					
Resolution		12		16	Bits
Noise, Low-Level Input(1)	C_{SENSOR}(2) = 10pF		3.5	6.0	LSB(3)
Integral Linearity Error(4)			8	16	LSB(3)
Input Bias Current	T_A = +25°C		±2	±10	pA
Range Error Match(5)			0.2	1	% of FSR(6)
Range Sensitivity to VREF	VREF = 4.096 ± 0.1V		1:1		
Offset Error			±50	±200	LSB(3)
Offset Error Match(5)			±75	±400	LSB(3)
DC Bias Voltage(7)	Low-Level Input (< 1% FSR)		±2	±10	mV
Power-Supply Rejection Ratio	at DC		40		LSB(3)/V
PERFORMANCE OVER TEMPERATURE					
Offset Drift			±1		LSB/°C
Offset Drift Stability	Continuous Readings Over 1-Minute Intervals After a 10-Minute Warm-Up		<1		LSB
DC Bias Voltage Drift(7)			±10		µV/°C
Input Bias Current Drift	Doubles Every +10°C				
Range Drift(8)			25		ppm/°C
Range Drift Match(5)			±10		ppm/°C
REFERENCE					
Voltage		4.000	4.096	4.200	V
DIGITAL INPUT/OUTPUT					
Logic Levels					
V_{IH}		0.8DVDD		DVDD + 0.1	V
V_{IL}		–0.1		0.2DVDD	V
V_{OH}	I_{OH} = –100µA	DVDD – 0.4			V
V_{OL}	I_{OL} = 100µA			0.4	V
Input Current (I_{IN})	0 < V_{IN} < DVDD			±10	µA
Data Format(9)			Straight Binary		

(1) Input is less than 1% of full-scale.
(2) C_{SENSOR} is the capacitance seen at the DDC316 inputs from wiring, photodiode, etc.
(3) LSB refers to 16-bit resolution.
(4) A best-fit line is used in measuring nonlinearity.
(5) Matching between side A and side B of the same input.
(6) FSR is full-scale range.
(7) Voltage produced by the DDC316 at its input that is applied to the sensor.
(8) Range drift does not include external reference drift.
(9) Data format is Straight Binary with a small offset. The number of bits in the output word is controlled by the Format bit.

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ELECTRICAL CHARACTERISTICS (continued)

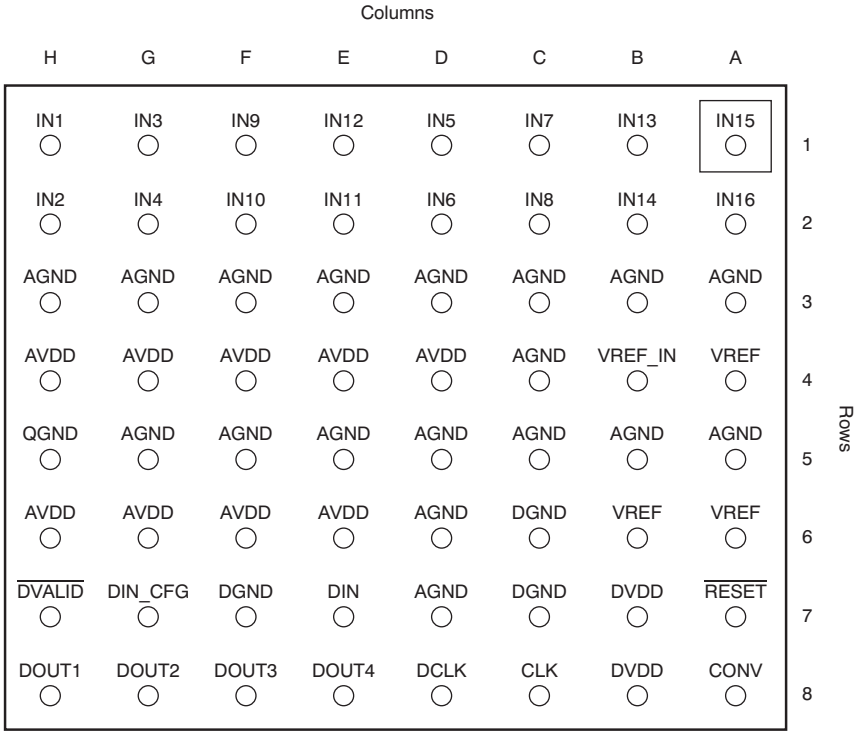
At T_A = +25°C, AVDD = +5V, DVDD = +3.3V, VREF = +4.096V, t_{INT} = 20µs, Range = 12pC, Format = 16 bits, CLK = 40MHz, and $\overline{HI_SPEED}$ Bit = 1, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DDC316			UNIT
		MIN	TYP	MAX	
POWER-SUPPLY REQUIREMENTS					
Analog Power-Supply Voltage (AVDD)		4.75	5.0	5.25	V
Digital Power-Supply Voltage (DVDD)		3	3.3	3.6	V
Supply Current					
Analog Current					
Internal Reference Buffer	BUFDIS Bit = 0		95		mA
External Reference Buffer	BUFDIS Bit = 1		85		mA
Digital Current	DVDD = +3.3V		5		mA
Total Power Dissipation					
Internal Reference Buffer	BUFDIS Bit = 0, DVDD = +3.3V		540		mW
External Reference Buffer	BUFDIS Bit = 1, DVDD = +3.3V		440	640	mW
Per Channel Power Dissipation					
Internal Reference Buffer	BUFDIS Bit = 0, DVDD = +3.3V		31		mW/channel
External Reference Buffer	BUFDIS Bit = 1, DVDD = +3.3V		28	40	mW/channel

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PIN CONFIGURATION

GXG AND ZXG PACKAGES
BGA-64
(TOP VIEW)

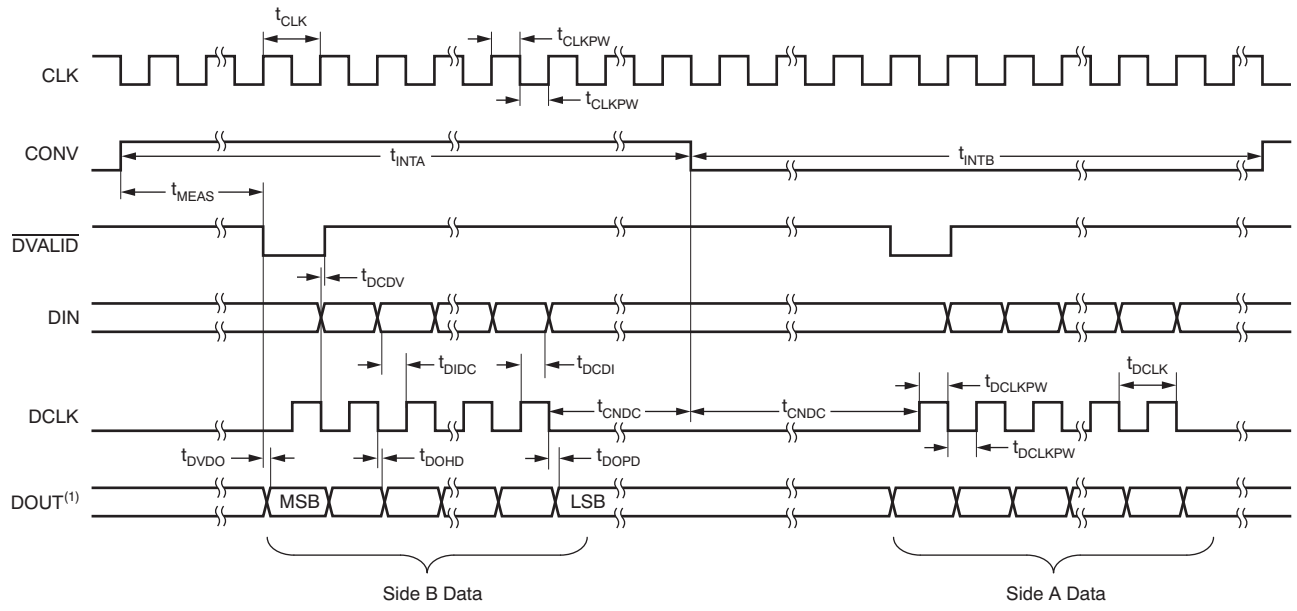


PIN DESCRIPTIONS

PIN	LOCATION	FUNCTION	DESCRIPTION
IN1–16	1A-1H, 2A-2H	Analog Input	Analog Inputs for Channels 1 to 16
AGND	3A-3H, 4C, 5A-5G, 6D, 7D	Analog	Analog Ground
VREF	4A, 6A, 6B	Analog Input	Voltage Reference for Internal Reference Buffer Mode
VREF_IN	4B	Analog Input	Voltage Reference for External Reference Buffer Mode
AVDD	4D-4H, 6E, 6F, 6G, 6H	Analog	Analog Power Supply, +5V Nominal
QGND	5H	Analog	Quiet Analog Ground
DGND	6C, 7C, 7F	Digital	Digital Ground
$\overline{\text{RESET}}$	7A	Digital Input	Digital Reset, Active Low
DVDD	7B, 8B	Digital	Digital Power Supply, +3V Nominal
DIN	7E	Digital Input	Serial Data Input for Daisy-Chain
DIN_CFG	7G	Digital Input	Configuration Register Data Input
$\overline{\text{DVALID}}$	7H	Digital Output	Data Valid Output, Active Low
CONV	8A	Digital Input	Conversion Control Input; 0 = Integrate on Side B, 1 = Integrate on Side A
CLK	8C	Digital Input	Master Clock Input
DCLK	8D	Digital Input	Serial Data Clock Input
DOUT4-1	8E-8H	Digital Output	Serial Data Output

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TIMING DIAGRAMS



NOTE: (1) DOUT1 in TDM data output mode; DOUT1 through DOUT4 in parallel data output mode.

Figure 1. Serial Interface Timing

TIMING REQUIREMENTS FOR Figure 1

At T_A = 0°C to +70°C and DVDD = 3V to 3.6V, unless otherwise noted.

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)		25		1000	ns
t_{CLKPW}	CLK pulse width, positive or negative		0.4			t_{CLK} periods
$t_{INTA,B}$	Integration time for sides A and B	$\overline{HI_SPEED}$ bit = 0	400		1000	t_{CLK} periods
		$\overline{HI_SPEED}$ bit = 0, CLK = 40MHz	10		25	µs
		$\overline{HI_SPEED}$ bit = 1	800		40,000	t_{CLK} periods
		$\overline{HI_SPEED}$ bit = 1, CLK = 40MHz	20		1000	µs
t_{MEAS}	Time required to perform measurement	$\overline{HI_SPEED}$ bit = 0		274		t_{CLK} periods
		$\overline{HI_SPEED}$ bit = 1		544		t_{CLK} periods
t_{DIDC}	Setup time from DIN to rising edge of DCLK		2			ns
t_{DCDI}	Hold time for DIN after rising edge of DCLK		0			ns
t_{DVDO} (1)	Falling edge of $\overline{DVALID}$ to valid DOUT			6	10	ns
t_{DCDV} (1)	Falling edge of first DCLK to rising edge of $\overline{DVALID}$			19		ns
t_{DCLK}	DCLK period ($1/f_{DCLK}$)		25			ns
t_{DCLKPW}	DCLK pulse width, positive or negative		0.4			t_{DCLK} periods
t_{DOPD} (1)	Propagation delay from the falling edge of DCLK to valid DOUT1				21	ns
t_{DOHD} (1)	Hold time during which previous DOUT1 is valid after falling edge of DCLK		5			ns
t_{CNDC}	Time between CONV toggle and data retrieval		5			ns

(1) Output load = 100kΩ || 10pF

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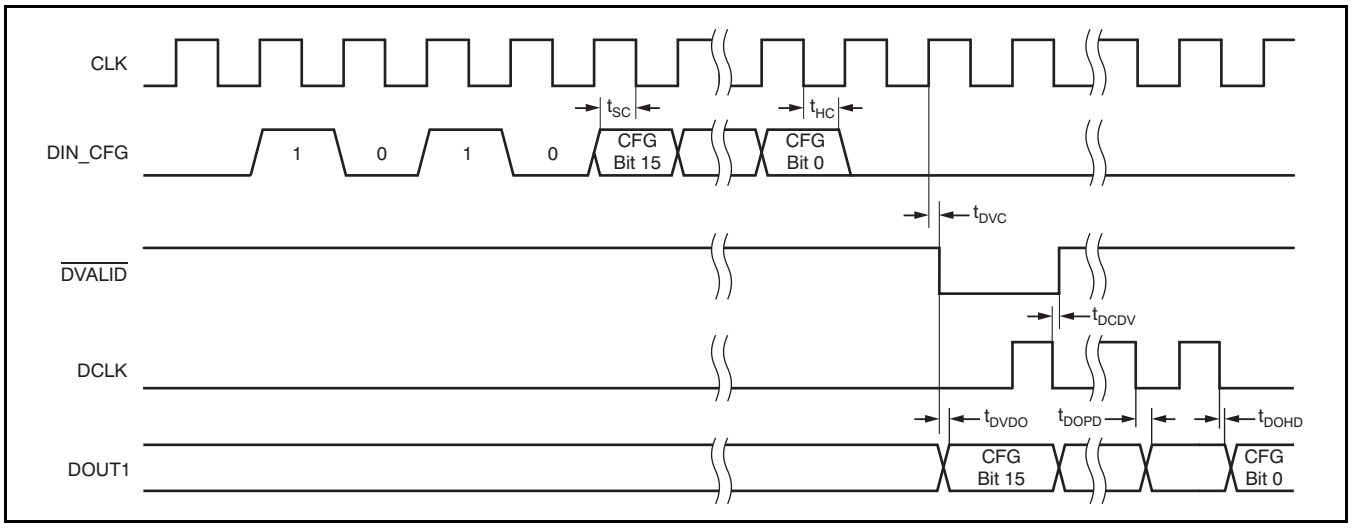


Figure 2. Configuration Register Read/Write Timing

TIMING REQUIREMENTS FOR Figure 2

At T_A = 0°C to +70°C and DVDD = 3.0V to 3.6V, unless otherwise noted.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SC}	Valid DIN_CFG to CLK falling edge; setup time	1	12		ns
t_{HC}	Valid DIN_CFG to CLK falling edge; hold time	3	12		ns
t_{DVC} (1)	Delay of $\overline{\text{DVALID}}$ from falling edge of CLK		18		ns
t_{DCDV} (1)	Falling edge of first DCLK to rising edge of $\overline{\text{DVALID}}$		19		ns
t_{DVDO} (1)	Delay from $\overline{\text{DVALID}}$ falling edge to valid CFG bit 15 on DOUT1		6	10	ns
t_{DOPD} (1)	Propagation delay from the falling edge of DCLK to valid DOUT1			21	ns
t_{DOHD} (1)	Hold time during which previous DOUT1 is valid after falling edge of DCLK	5			ns

(1) Output load = 100kΩ || 10pF

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TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise indicated.

NOISE vs C_{SENSOR}

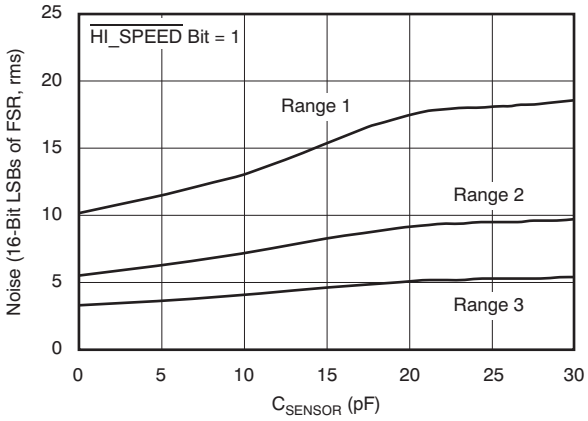


Figure 3.

NOISE vs C_{SENSOR}

C_{SENSOR} (pF)	Noise (16-Bit LSBs of FSR, rms)		
	Range 1	Range 2	Range 3
0	10.2	5.6	3.3
10	13.1	7.2	4.1
20	17.5	9.2	5.1
30	18.6	9.7	5.4
50	22.3	11.6	6.4
100	34.3	17.8	9.4

NOTE: $\overline{\text{HI_SPEED}}$ bit = 1.

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THEORY OF OPERATION

GENERAL DESCRIPTION

The DDC316 contains 16 identical input channels that perform the function of current-to-voltage integration, followed by a multiplexed A/D conversion. Integration time is directly controlled via the CONV pin. Each input uses a dual-switched integrator so that the current-to-voltage integration can be continuous over time. The 16 integrators from one side of the inputs are digitized, while the other 16 are integrating to achieve continuous charge collection. The results from the conversion are stored in a serial output shift register. The $\overline{\text{DVALID}}$ output goes low when the shift register contains valid data. A block diagram of the DDC316 is shown in Figure 4.

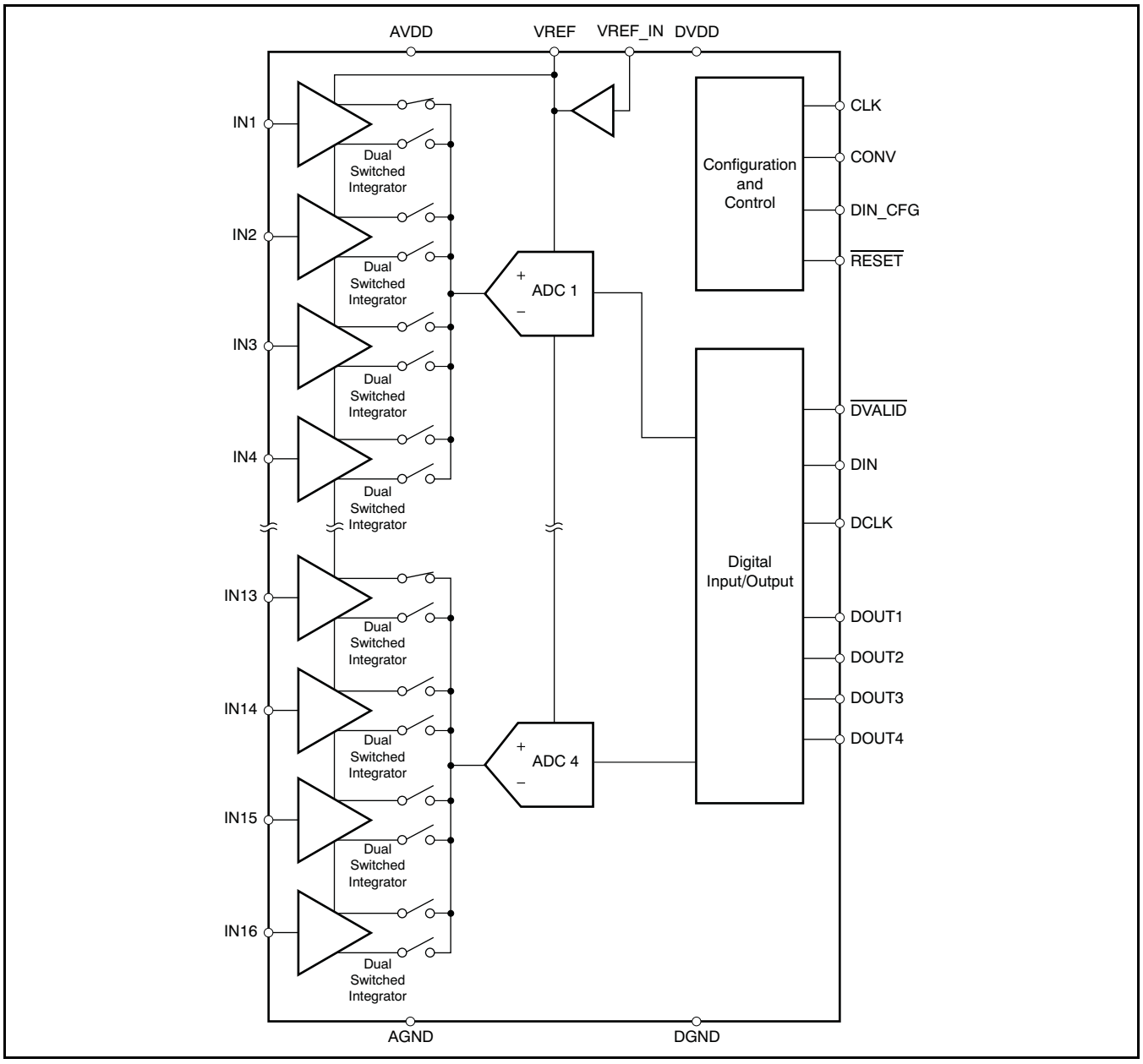


Figure 4. DDC316 Block Diagram

BASIC INTEGRATION CYCLE

The topology of the front-end of the DDC316 is an analog integrator, as shown in Figure 5. In this diagram, only input IN1 is shown. The input stage consists of an operational amplifier, a selectable feedback capacitor network (C_F), and several switches that implement the integration cycle.

The timing relationships of all of the switches shown in Figure 5 are illustrated in Figure 6. Note that Figure 6 conceptualizes the operation of the integrator input stage of the DDC316 and should not be used as an exact timing tool for design.

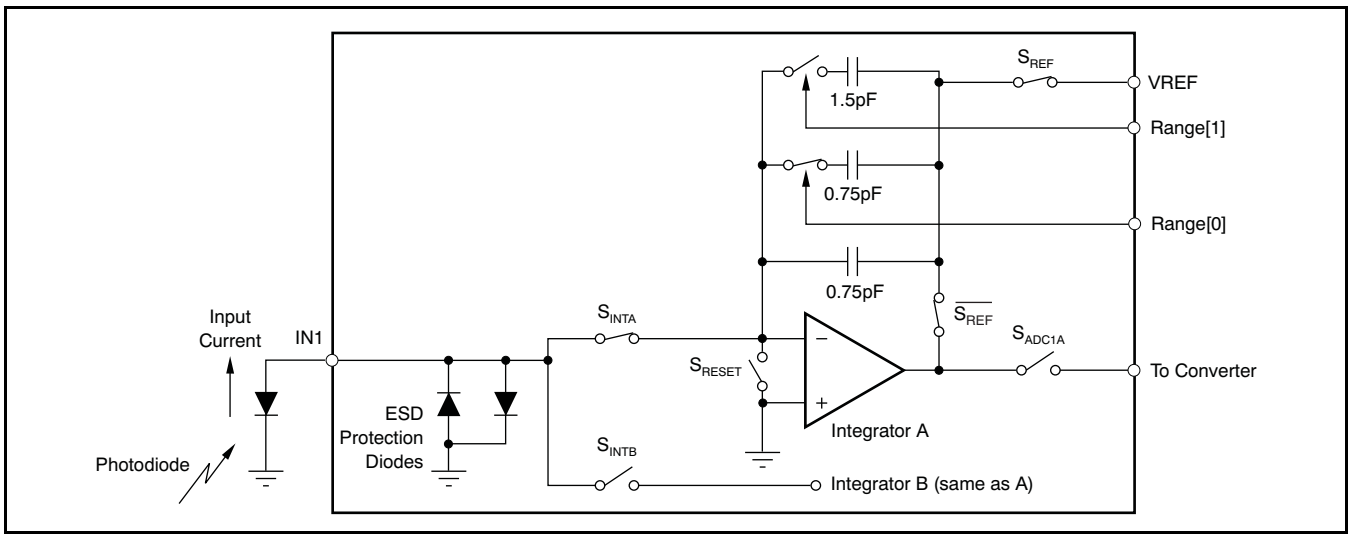


Figure 5. Basic Integration Configuration for Input 1

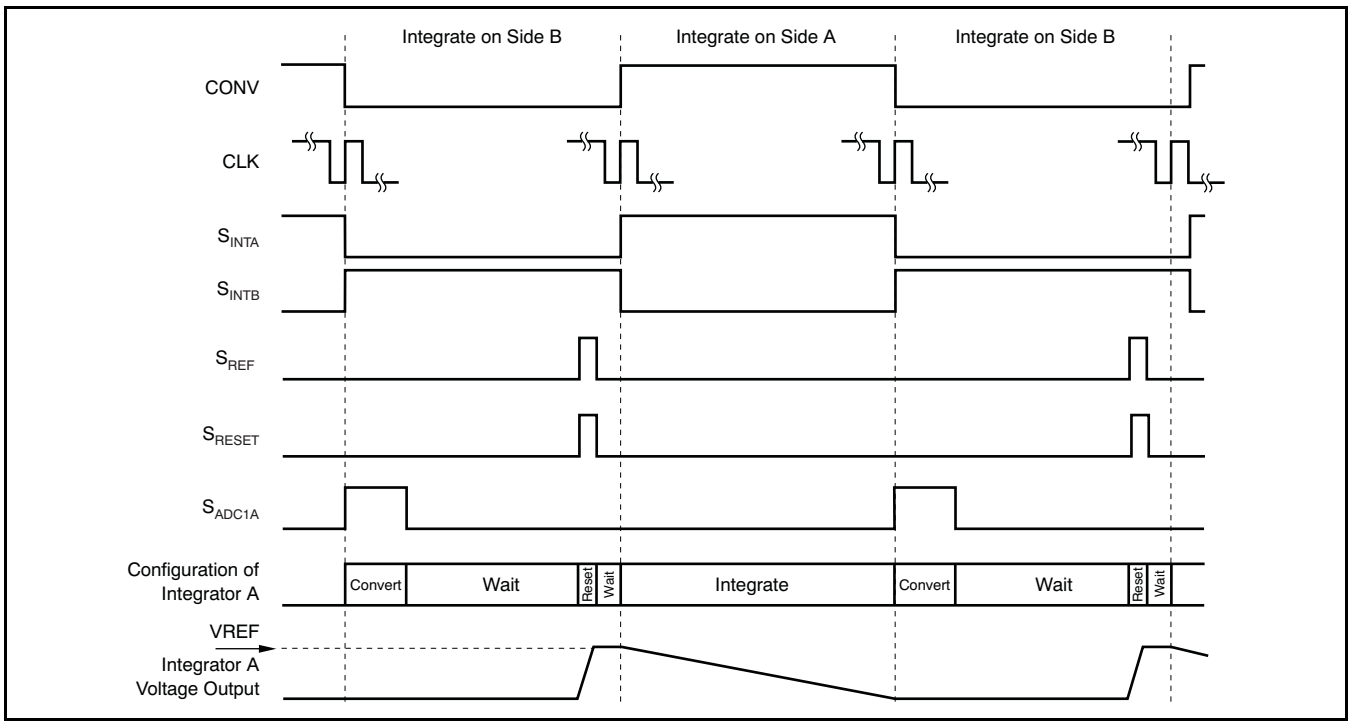


Figure 6. Conceptual Basic Integration Timing Diagram of Integrator A (as Illustrated in Figure 5)

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Figure 7 shows the block diagrams of the five states of the front end integrator. The conversion starts with the integrator being configured as shown in Figure 7a. In this state, the ADC converts the integrated value of side A of the previous phase. Once the conversion is done, the integrator waits until the ADC finishes converting the other three integrated values (Figure 7b). At the completion of all four A/D conversions, the charge on the integrator capacitor (C_F) is reset with S_{REF} and S_{RESET} (see Figure 7c). In this manner, the selected capacitor is charged to the reference voltage, VREF. Once the integration capacitor is charged, S_{REF} and S_{RESET} are switched so that VREF is no longer connected to the amplifier circuit while it waits to begin integrating (see Figure 7d). With the rising edge of CONV, S_{INTA} closes, which begins the integration of side A. This process puts the integrator stage into Integrate mode (see Figure 7e).

Charge from the input signal is collected on the integration capacitor, causing the voltage output of the amplifier to decrease. The falling edge of CONV stops the integration by switching the input signal from side A to side B (S_{INTA} and S_{INTB}). Before the falling edge of CONV, the signal on side B was converted by the ADC and reset during the time that side A was integrating. With the falling edge of CONV, side B starts integrating the input signal. At this point, the output voltage of the side A operational amplifier is presented to the input of the ADC, and the entire cycle repeats.

This internal switching network is controlled externally with the convert pin (CONV) and the system clock (CLK). For the best noise performance, CONV must be synchronized with the rising edge of CLK. It is recommended that CONV toggle within ±5ns of the rising edge of CLK. The noninverting inputs of the integrators are connected to ground. Consequently, the DDC316 analog ground should be as clean as possible.

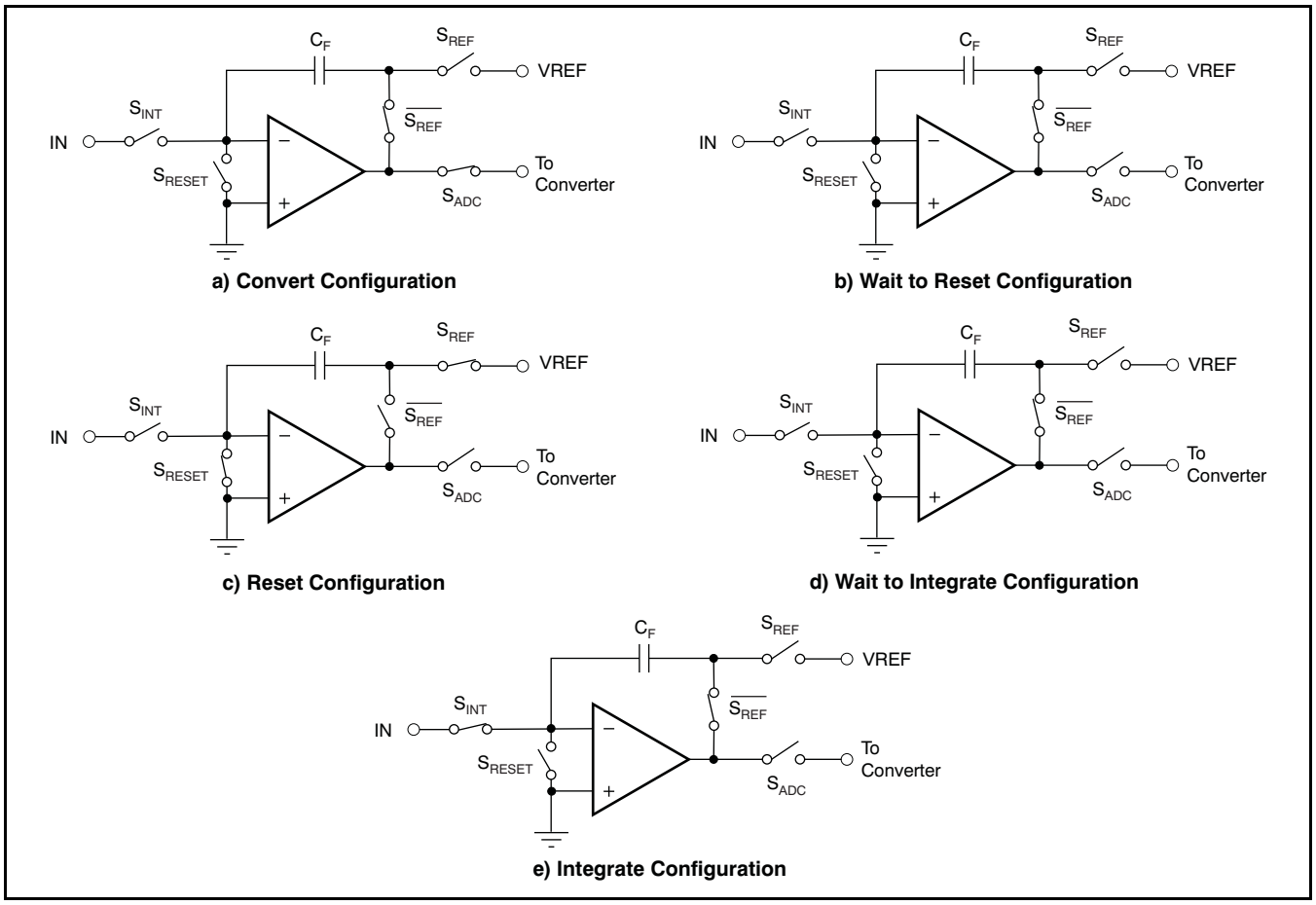


Figure 7. Diagrams for the Five Configurations of DDC316 Front-End Integrators

FREQUENCY RESPONSE

The frequency response of the DDC316 is set by the front-end integrators and is consistent with a traditional continuous time integrator, as shown in Figure 8. By adjusting t_{INT}, the user can change the 3dB bandwidth and the location of the notches in the response. The frequency response of the ADC that follows the front-end integrator is of no consequence because the converter samples a held signal from the integrators. That is, the input to the ADC is always a DC signal. Aliasing can occur because the output of the front-end integrators are sampled. Whenever the frequency of the input signal exceeds one-half of the sampling rate, the signal folds back down to lower frequencies.

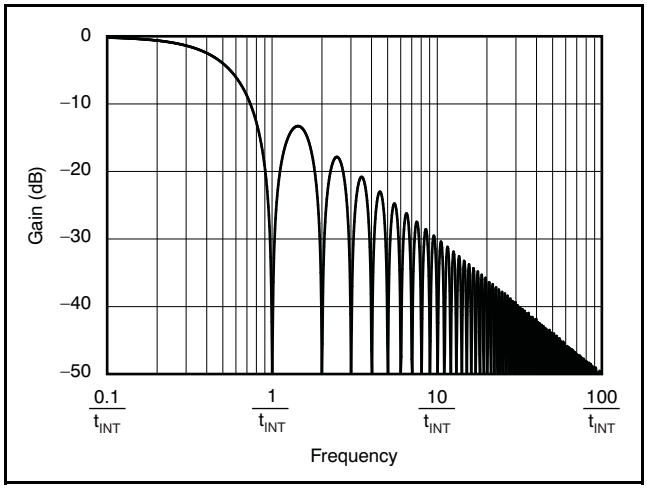


Figure 8. DDC316 Frequency Response

OPERATION SETTINGS

The DDC316 provides different settings of operation to provide flexibility in terms of range, resolution, etc. The settings are programmable using an on-chip register and are described in the following sections.

Ranges

There are three different capacitors available on-chip for both sides of every channel in the DDC316. The range control bits (Range[1:0]) change the capacitor value for all integrators. Consequently, all inputs and both sides of each input always have the same full-scale (FS) range. Table 1 shows the capacitor value selected for each range selection.

Table 1. Range Selection

RANGE	RANGE[1:0] BITS	C_F (pF, typ)	INPUT RANGE (pC, typ)
1	00	0.75	–0.0469 to 3
2	01	1.5	–0.0938 to 6
3	10	3	–0.1876 to 12

Resolution

The DDC316 provides three different resolutions for the convenience of the user. The user can select the resolution needed for the application and the time available for data retrieval. The three available resolutions are 16-bit, 14-bit, and 12-bit. The serial output data from the DDC316 are provided in an offset binary code, as shown in Table 2. The RES bits in the configuration register select how many bits are used in the output word. When 12-bits are selected, the last four bits are truncated; when 14-bits are chosen, the last two bits are truncated. Note that an offset is included in the output to allow slightly negative inputs (for example, from board leakages) from clipping the reading. The offset is approximately 1.8% of the positive full-scale.

Data Format

The DDC316 outputs 12 to 16 bits of data depending on the selected resolution. The format is straight binary with an offset to help prevent leakage currents from the printed circuit board (PCB), or the sensors forcing a clipping on the negative full-scale. Table 2 summarizes the ideal output codes for the different resolutions.

Table 2. Ideal Output Code(1) vs Input Signal

INPUT SIGNAL	IDEAL OUTPUT CODE RESOLUTION = 16 BITS	IDEAL OUTPUT CODE RESOLUTION = 14 BITS	IDEAL OUTPUT CODE RESOLUTION = 12 BITS
≥ 100% FS	1111 1111 1111 1111	1111 1111 1111 11	1111 1111 1111
0.07019% FS	0000 0100 1100 0000	0000 0100 1100 00	0000 0100 1100
0.02136% FS	0000 0100 1010 0000	0000 0100 1010 00	0000 0100 1010
0.00305% FS	0000 0100 1001 0100	0000 0100 1001 01	0000 0100 1001
0.001525% FS	0000 0100 1001 0011	0000 0100 1001 00	0000 0100 1001
0% FS	0000 0100 1001 0010	0000 0100 1001 00	0000 0100 1001
–1.7857% FS	0000 0000 0000 0000	0000 0000 0000 00	0000 0000 0000

(1) Excludes the effects of noise, INL, offset, and gain errors.

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Data Output Modes

The DDC316 provides two data output modes: time division multiplexed (TDM) and parallel. In TDM mode, data from all 16 channels are output on a single data output line, DOUT1, as shown in Figure 9. In this mode, DOUT2 through DOUT4 are not used and forced to logic low.

In parallel output mode, as shown in Figure 10, four channels of data are output on the four DOUT lines, DOUT1 thorough DOUT4.

In either mode, the most significant bit (MSB) is shifted out first.

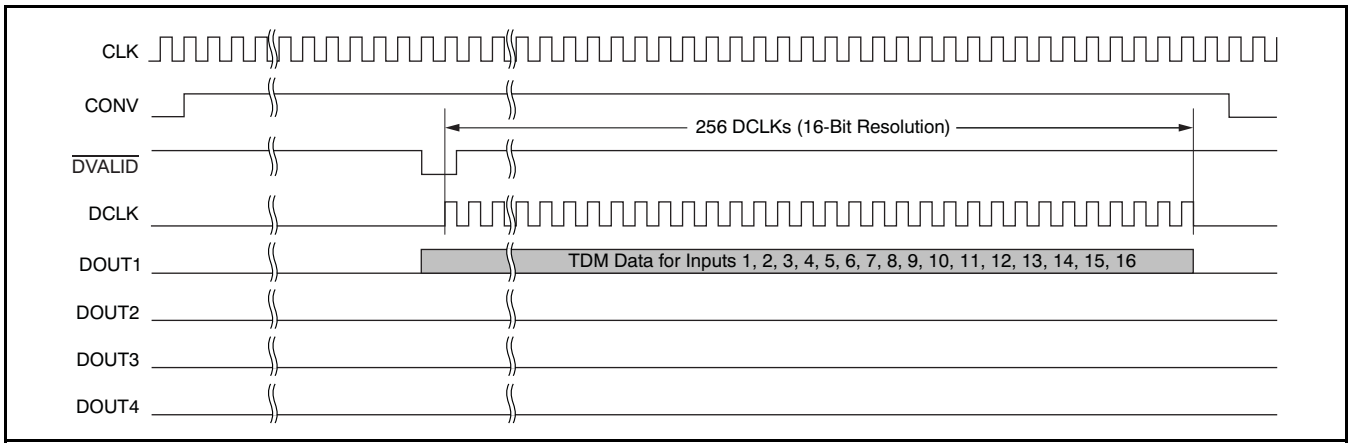


Figure 9. TDM Data Output

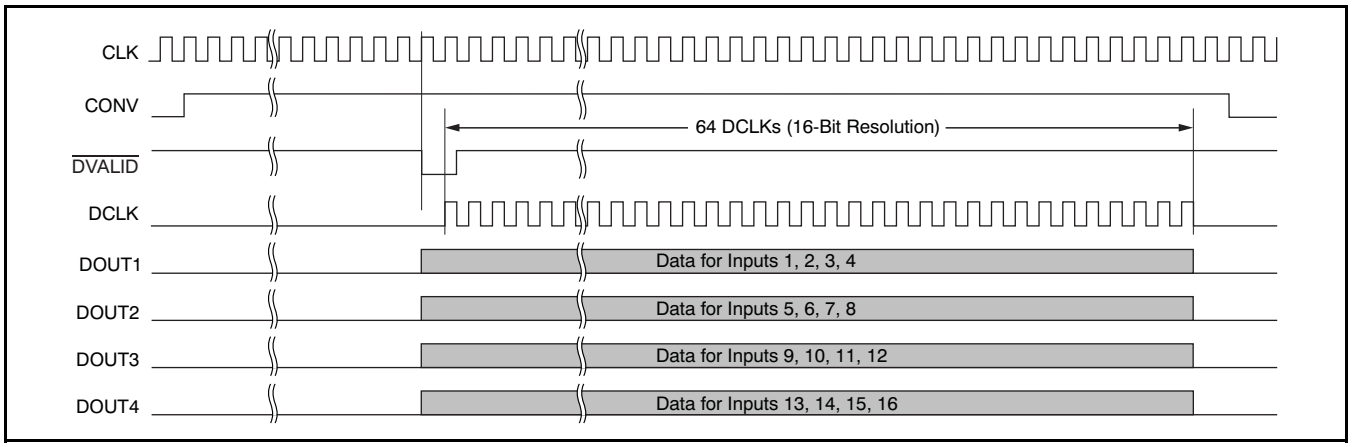


Figure 10. Parallel Data Output

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MINIMUM INTEGRATION TIME

The minimum integration time of the DDC316 is set by the master clock (CLK) and the HI_SPEED bit, as shown in Table 3. The integration time specification must always be met for both side A and side B integrations (t_{INTA} and t_{INTB}). Failure to meet integration time specifications gives invalid conversion results.

Table 3. Minimum Integration Times

HI_SPEED BIT	VALID RESOLUTIONS	MINIMUM INTEGRATION TIME (MINIMUM t_{INT})	
0	12-bit only	400 t_{CLK} periods	10µs (for CLK = 40MHz)
1	12-bit to 16-bit	800 t_{CLK} periods	20µs (for CLK = 40MHz)

When operating with the HI_SPEED bit set to 0, the DDC316 operates internally at a higher speed and the performance is reduced to fundamentally 12 bits. It is recommended, therefore, that the RES[1:0] bits should be set to 12-bit resolution when HI_SPEED = 0. This will provide more flexibility in retrieving data, because the time required to read back the conversion results is shorter.

DATA RETRIEVAL TIME

The available time for retrieving the conversion data (t_{RETRV}) from the DDC316 is the difference between the integration time (t_{INT}) and the measurement time (t_{MEAS}), as shown in Figure 11. Retrieval begins after DVALID goes low, and must complete before CONV toggles, for optimal noise performance (see the t_{CNDC} timing specification).

Sometimes, it is not possible to retrieve all of the data in time when using the TDM data output mode; for example, when integration times are short and DCLK is slow. In these cases, using the parallel data output mode will help because the required time for retrieval decreases by a factor of four.

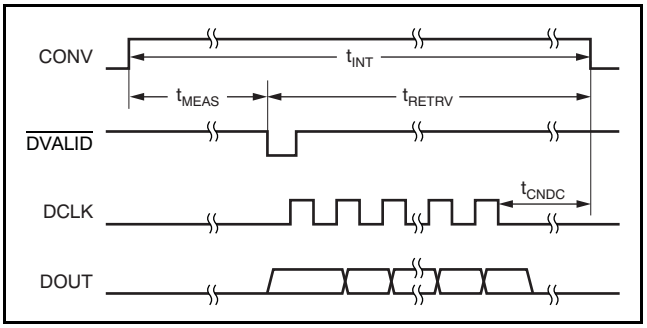


Figure 11. Data Retrieval Time

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CONFIGURATION REGISTER

The DDC316 configuration shown in Table 4 is controlled by and configured with an on-chip, 16-bit configuration register.

Table 4. Configuration Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	MODE	RES[1]	RES[0]	RANGE[1]	RANGE[0]	0	$\overline{\text{HI_SPEED}}$
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
TM[1]	TM[0]	0	BUFDIS	0	0	0	0

The following section gives a brief description of the programmable bits and the method to program the bits. Note that in the event of an external reset or a power-on reset, all the configuration bits are set to default values. The bits need to be reprogrammed as needed after a reset.

Bit Descriptions

Bit 15 Unused bit. This bit must always be set to one.
During a power-up or reset event, this bit is set to zero and must be programmed to one.

Bit 14 **MODE**—Data Output Mode.
This bit selects between the parallel and serial data output (time division multiplexing, or TDM) modes, as shown in Table 5.

Table 5. Data Output Mode

MODE	DATA OUTPUT MODE
0	Parallel, using DOUT1, DOUT2, DOUT3, and DOUT4 (default)
1	Serial, time division multiplexed (TDM) on DOUT1

Bits 13-12 **RES[1:0]**—Output Data resolution.
These bits set the output data resolution. The value of the output resolution is the same for RES[1:0] = '10' and RES[1:0] = '11'.

Table 6. Output Data Resolution

RES[1:0]	OUTPUT RESOLUTION
00	16 Bits (default)
01	14 Bits
10	12 Bits
11	

Bits 11-10 **RANGE[1:0]**—Full-Scale Input Range.
These range bits set the value of the integration capacitors that are used in the dual-switched integrators. Table 7 shows the three different capacitor values available. The value of the maximum input charge is the same for RANGE = '10' and RANGE = '11'.

Table 7. Full-Scale Range

RANGE[1:0]	MAXIMUM INPUT CHARGE
00	3pC (default)
01	6pC
10	12pC
11	

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Bit 9 Unused bit. This bit is reset to zero and must always be set to zero.

Bit 8 **$\overline{\text{HI_SPEED}}$**—High-Speed Operation Selection.
This bit sets which speed (normal or high) will be used. The default is normal speed, and is the generally recommended operating condition. However, if shorter integration times are needed than are supported during normal operation, then high-speed mode is available. Note that performance reduces to the 12-bit level during high-speed mode.

Table 8. High-Speed Mode Selection

$\overline{\text{HI_SPEED}}$	SPEED
0	High speed
1	Normal speed (default)

Bits 7-6 **TM[1:0]**—Test Mode Selection.
Test mode (TM) bits allow for configuration of the device to operate in either normal mode or test modes for verification purposes, as shown in Table 9. The test modes are provided as a means of evaluating the DDC316 noise.
In test mode 1, the inputs (IN1 through IN16) are disconnected from the DDC316 integrators to enable the user to measure a zero input signal, regardless of the current supplied to the DDC316 by the external sensor.
In test mode 2, the inputs (IN1 through IN16) are disconnected from the DDC316 integrators and at the same time a 10pF capacitor is added to the input to emulate the sensor capacitance.
In test mode 3, the inputs are disconnected from the DDC316 integrators. Each time a new conversion begins (CONV toggles), a fixed amount of charge (approximately 1.5pC) is dumped into the integrator.

Table 9. Test Mode Decoding

TM[1:0]	TEST MODE FUNCTION
00	Normal mode (default)
01	Test mode 1 (inputs opened)
10	Test mode 2 (inputs opened and 10pF internal capacitor connected to integrators)
11	Test mode 3 (inputs opened and 1.5pC charge dumped into the integrators during each conversion)

Bit 5 Unused bit. This bit is reset to zero and must always be set to zero.

Bit 4 **BUFDIS**—Internal Reference Buffer Disable.
This bit is used to turn the internal reference buffer off, as shown in Table 10. See the Voltage Reference section for more details.

Table 10. Internal Reference Buffer Disable

BUFDIS	INTERNAL REFERENCE BUFFER STATUS
0	Internal buffer enabled
1	Internal buffer disabled (default)

Bits 3-0 Unused bits. These bits are reset to zero and must always be set to zero.

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Writing and Reading of the Configuration Register

Figure 2 shows the timing diagram for writing to and reading from the configuration register. Writing and reading must be done before or after CONV toggles. The data on pin DIN_CFG are latched on the falling edge of CLK. The first four bits are used as preamble; only when these bits equal '1010' are the contents of the following 16 bits loaded into the configuration register. Once the content is loaded, the shift register immediately clears so that a new configuration can be written, if needed. It is recommended to leave the DIN_CFG pin to logic '0' when not programming the register.

Once the configuration register updates, it is loaded into the data shift register to be output on DOUT1. When DVALID is goes low, the configuration register is available to be read. If the data are not read back, then the register is overwritten by the conversion data on the following conversion. Data are shifted out on the falling edge of DCLK.

SYSTEM AND DATA CLOCKS (CLK AND DCLK)

The system clock is supplied to CLK and the data clock is supplied to DCLK. Make sure the clock signals are clean; avoid overshoot or ringing. DCLK should be held low after the data have been shifted out, or while CONV is transitioning; DCLK should not be left free-running.

The integration and conversion process is fundamentally independent of the data retrieval process. Consequently, the CLK and DCLK frequencies need not be the same, although for best performance, it is highly recommended that they be derived from the same clocking source to keep their phase relationship constant.

When using multiple DDC316s, pay close attention to the DCLK distribution on the printed circuit board (PCB). In particular, make sure to minimize skew in the DCLK signal because the skew can lead to timing violations in the serial interface specifications.

DATA VALID ($\overline{\text{DVALID}}$)

The $\overline{\text{DVALID}}$ signal indicates that data are ready. Data retrieval may begin after $\overline{\text{DVALID}}$ goes low. This signal goes low on the rising edge of the system clock (CLK), and goes high on the first falling edge of DCLK during the data retrieval process. Data retrieval from the DDC316 can be done either by polling the $\overline{\text{DVALID}}$ signal or by counting the number of clock cycles after a transition of the CONV signal. While using the counting method, the number of clock cycles to wait depends on the mode of operation, either the low power or the high speed mode. The exact number of CLK cycles to wait for the two different modes is given in Table 3.

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READBACK WITH MULTIPLE DDC316s

The serial interface supports daisy-chaining to simplify connections when using multiple DDC316s together. Figure 12 shows an example of a 64-channel system. The DIN pin is used to shift data into the DDC316s. Additional DCLK pulses must then be given during readback to ensure all the data have shifted through, as shown in Figure 13.

Note that daisy-chaining is only supported in TDM output mode, and will not work when using parallel data output mode. When the daisy-chaining function is not used, connect DIN to digital ground.

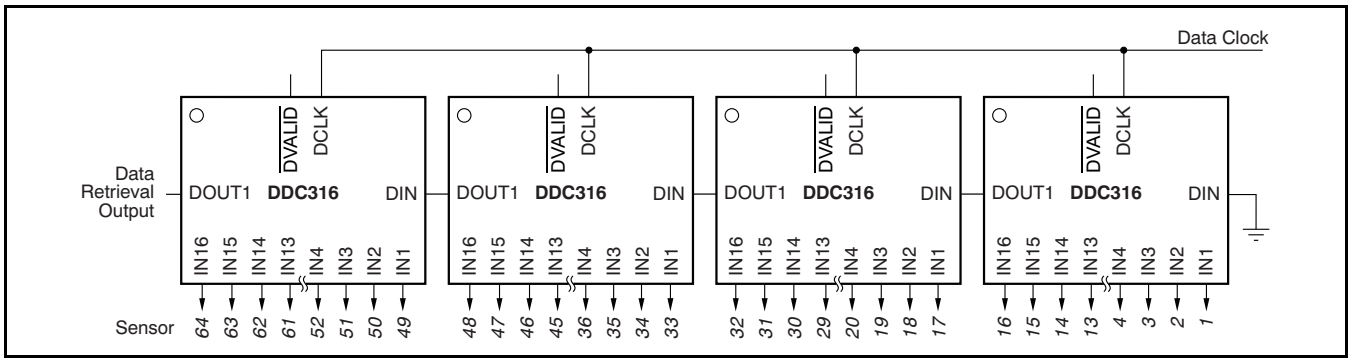


Figure 12. Daisy-Chain Configuration of a 64-Channel System

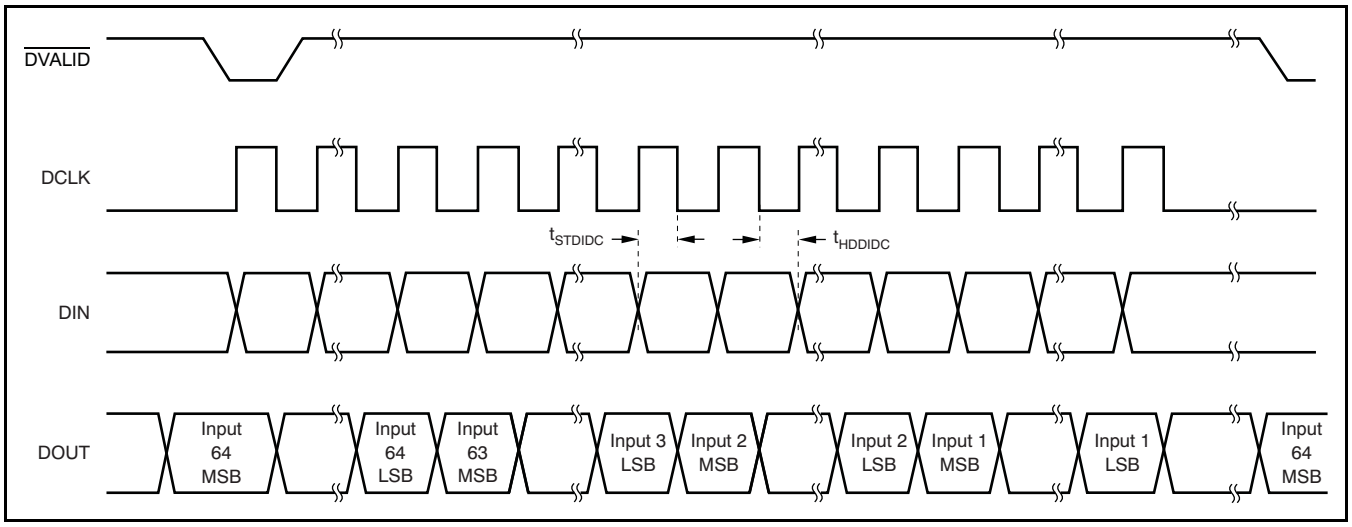


Figure 13. Daisy-Chain Readback of Four Devices (64 Channels)

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VOLTAGE REFERENCE

The reference voltage is used to reset the integration capacitors before an integration cycle begins. It is also used by the ADCs when they measure the voltage stored on the integrators after an integration cycle ends. During this sampling, the external reference must supply the charge needed by the ADCs. For an integration time of 20µs, this charge translates to an average VREF current of approximately 270µA. The amount of charge needed by the ADC is independent of the integration time; therefore, increasing the integration time lowers the average current. For example, an integration time of 40µs lowers the average VREF current to 135µA.

It is critical that VREF be stable during the different modes of operation (see Figure 7). The ADC measures the voltage on the integrator with respect to VREF. Since the integrator capacitors are initially reset to VREF, any drop in VREF, from the time the capacitors are reset to the time when the converter measures the integrator output, introduces an offset. It is also important that VREF be stable over longer periods of time because changes in VREF correspond directly to changes in the full-scale range. Finally, VREF should introduce as little additional noise as possible. For these reasons, it is strongly recommended that the external reference source be buffered with an operational amplifier.

The DDC316 offers two options for driving the reference voltage: through an external buffer or through an internal buffer. In both the cases, the reference voltage is generated external to the chip using an accurate reference, such as the REF3140.

Internal VREF Buffer

The DDC316 provides an internal VREF buffer to drive the four on-chip ADCs. The reference voltage must be provided at VREF_IN (pin 4B), as shown in Figure 14. The external capacitors at the VREF pins are necessary to stabilize the internal buffer. It is recommended that these capacitors be placed as close as possible to the device under test. Also, good quality capacitors with low ESR (< 1Ω) are necessary for optimum performance. High ESR capacitors will lead to oscillation of the internal buffer. Ceramic capacitors with ESR < 1Ω at 100kHz are recommended.

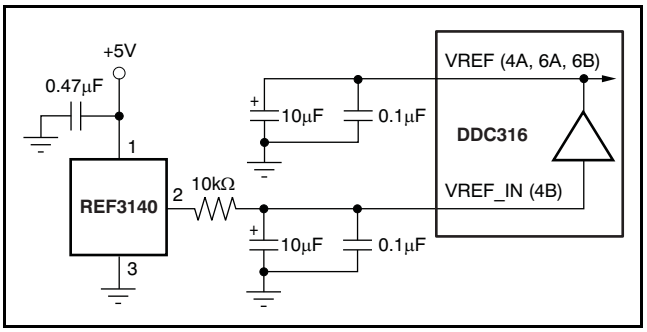


Figure 14. Recommended Circuit when Using the Internal VREF Buffer

External VREF Buffer

The internal buffer can be turned off using the control bits as explained in the Configuring the Modes section under Bit 4 and Table 10. For this option, configure the driving circuit as illustrated in Figure 15. The voltage reference is generated by a +4.096V reference. A low-pass filter to reduce noise connects the reference to an operational amplifier configured as a buffer. The VREF_IN pin must be left disconnected.

This amplifier used as buffer should have low noise and input/output common-mode ranges that support VREF. Even though the circuit in Figure 15 might appear to be unstable as a result of the large output capacitors, it works well for most operational amplifiers. It is ***not*** recommended that series resistance be placed in the output lead to improve stability because it can cause a drop in VREF and produce large offsets.

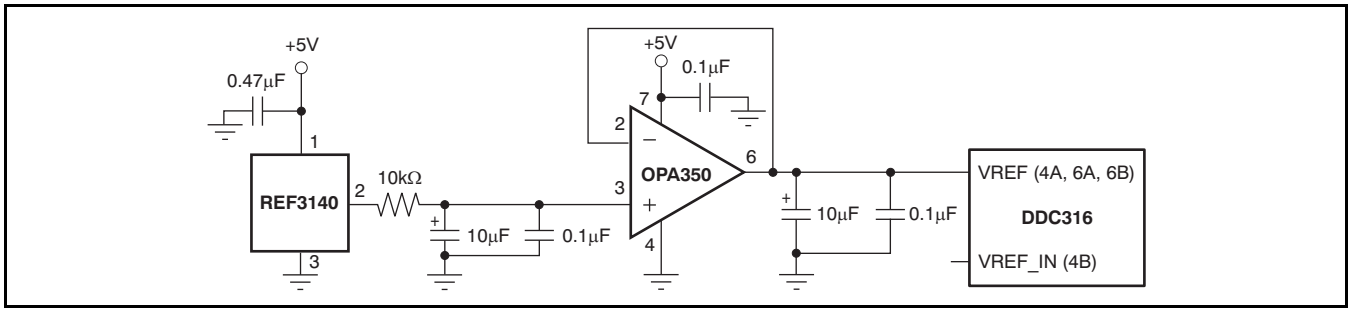


Figure 15. Recommended Circuit when Using an External VREF Buffer

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RESET ($\overline{\text{RESET}}$)

The DDC316 can be reset asynchronously by taking the $\overline{\text{RESET}}$ input low. Make sure the reset pulse is at least two CLK cycles wide. Once the $\overline{\text{RESET}}$ signal is pulled high, the internal reset is released t_{RST} later, after which the configuration register can be written. It is very important that $\overline{\text{RESET}}$ is glitch-free to avoid unintentional resets.

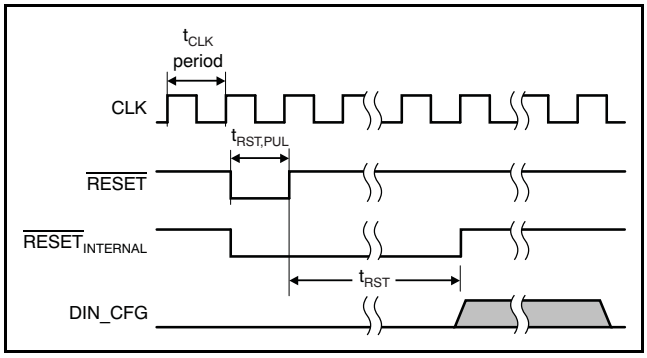


Figure 16. Reset Timing

POWER-UP SEQUENCING

Figure 17 shows the internal timing after the part powers up. Once the digital supply is above the threshold voltage, the internal power-on reset circuit releases the $\overline{\text{POR}}$ signal. The internal reset signal to the digital logic is released t_{POR} time after the $\overline{\text{POR}}_{\text{INTERNAL}}$, after which the configuration register can be written.

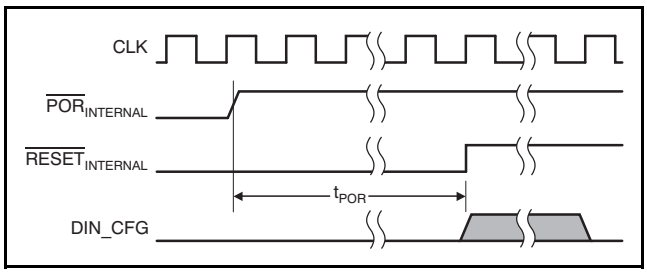


Figure 17. Power-Up Timing

LAYOUT

Power Supplies and Grounding

Both AVDD and DVDD should be as quiet as possible. It is particularly important to eliminate noise from AVDD that is nonsynchronous with the DDC316 operation. For this reason, switching-supplies are not recommended. Figure 18 illustrates how to supply power to the DDC316. Each supply of the DDC316 should be bypassed with 10µF solid ceramic capacitors. It is recommended that both the analog and digital grounds (AGND and DGND) be connected to a single ground plane on the PCB.

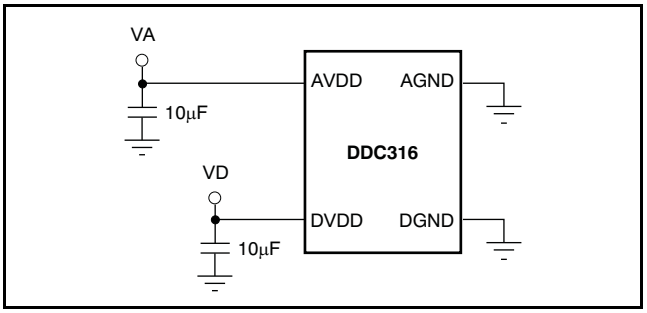


Figure 18. Power-Supply Connections

Shielding Analog Signal Paths

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance, particularly at the analog input pins and QGND. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The QGND pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the input bias current of the DDC316 if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

Table 11. Timing Figure 16 and Figure 17

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{RST,PUL}$	$\overline{\text{RESET}}$ pin low width	2			t_{CLK} periods
t_{RST}	Wait from $\overline{\text{RESET}}$ high to beginning of configuration register write	20			t_{CLK} periods
t_{POR}	Wait from power-up to power-on reset release	40,000			t_{CLK} periods

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Revision History

NOTE: Page numbers for previous revisions may be differ from page numbers in the current version.

Changes from Original (March 2008) to Revision A **Page**

- Changed test condition for Offset Drift Stability specification 3
- Changed Figure 1 6
- Changed Figure 2 7
- Added missing text 9
- Deleted duplicate mechanical package drawing 20

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DDC316CGXGR	Active	Production	NFBGA (GXG) | 64	1000 | LARGE T&R	No	SNPB	Level-3-240C-168 HR	0 to 70	DDC316
DDC316CGXGR.A	Active	Production	NFBGA (GXG) | 64	1000 | LARGE T&R	No	SNPB	Level-3-240C-168 HR	0 to 70	DDC316
DDC316CGXGT	Active	Production	NFBGA (GXG) | 64	250 | SMALL T&R	No	SNPB	Level-3-240C-168 HR	0 to 70	DDC316
DDC316CGXGT.A	Active	Production	NFBGA (GXG) | 64	250 | SMALL T&R	No	SNPB	Level-3-240C-168 HR	0 to 70	DDC316
DDC316CZXGR	Active	Production	NFBGA (ZXG) | 64	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 70	DDC316
DDC316CZXGR.A	Active	Production	NFBGA (ZXG) | 64	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	0 to 70	DDC316

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

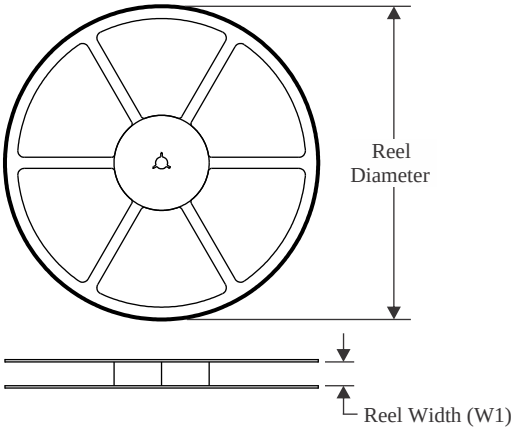
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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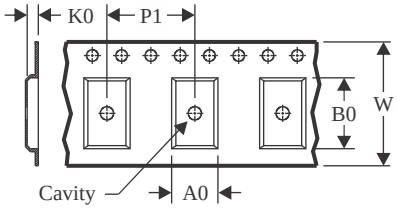
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

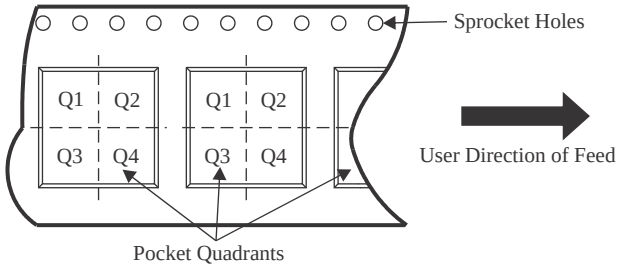


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

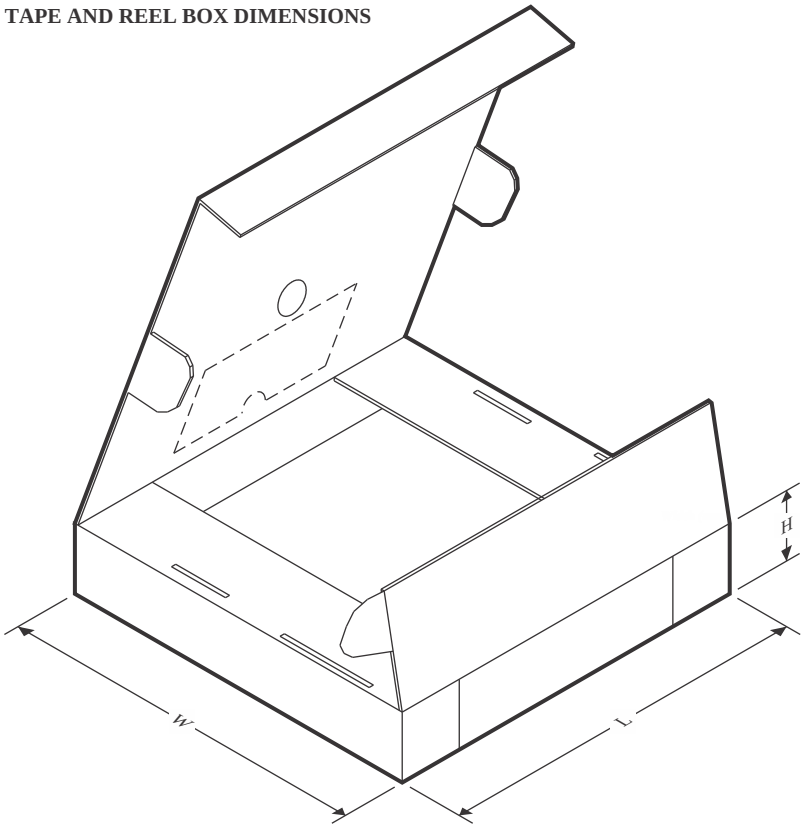
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DDC316CGXGR	NFBGA	GXG	64	1000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q1
DDC316CZXGR	NFBGA	ZXG	64	1000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q1
DDC316CZXGR	NFBGA	ZXG	64	1000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

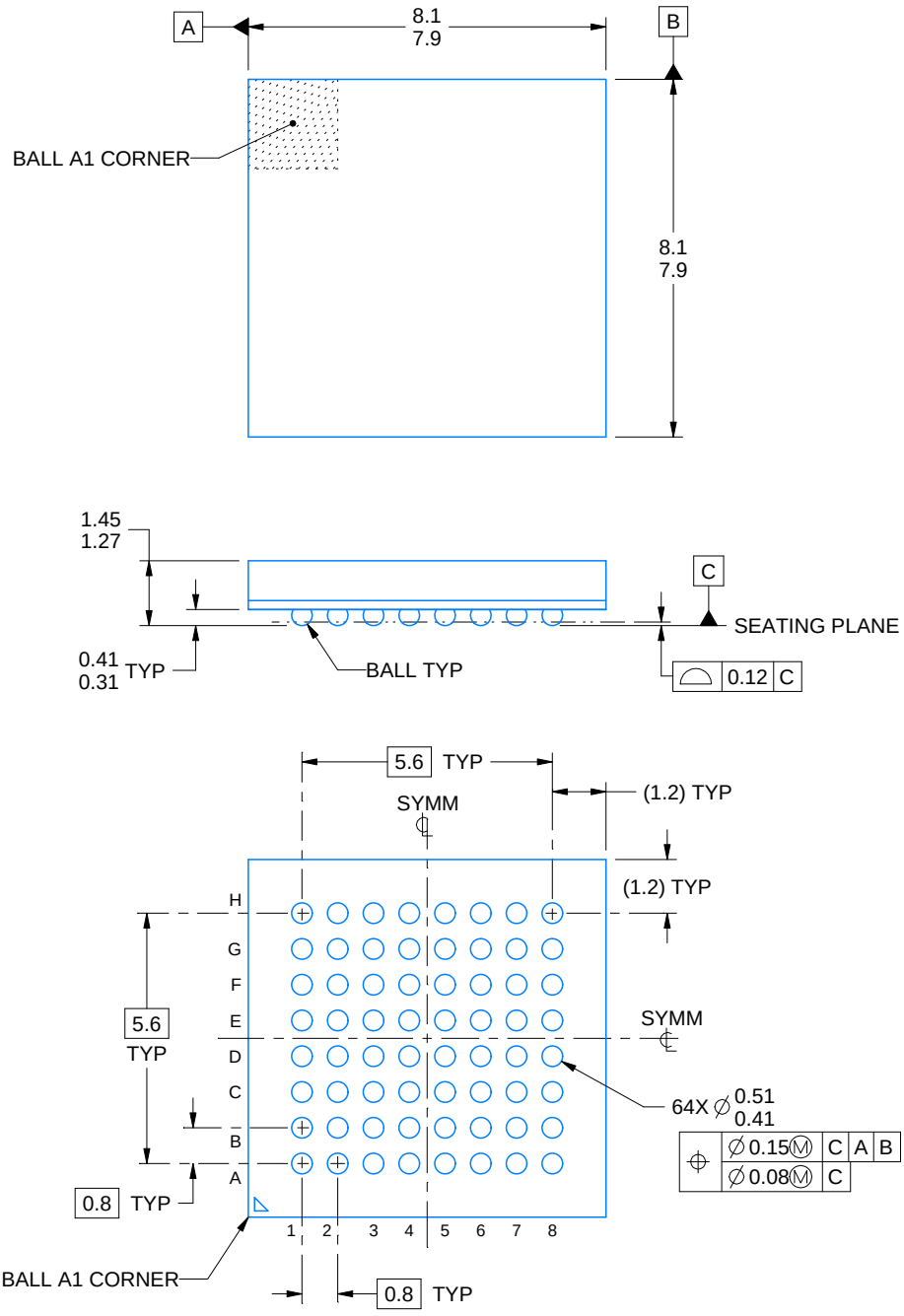
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DDC316CGXGR	NFBGA	GXG	64	1000	350.0	350.0	43.0
DDC316CZXGR	NFBGA	ZXG	64	1000	336.6	336.6	31.8
DDC316CZXGR	NFBGA	ZXG	64	1000	350.0	350.0	43.0

PACKAGE OUTLINE

GXG0064A

NFBGA - 1.45 mm max height

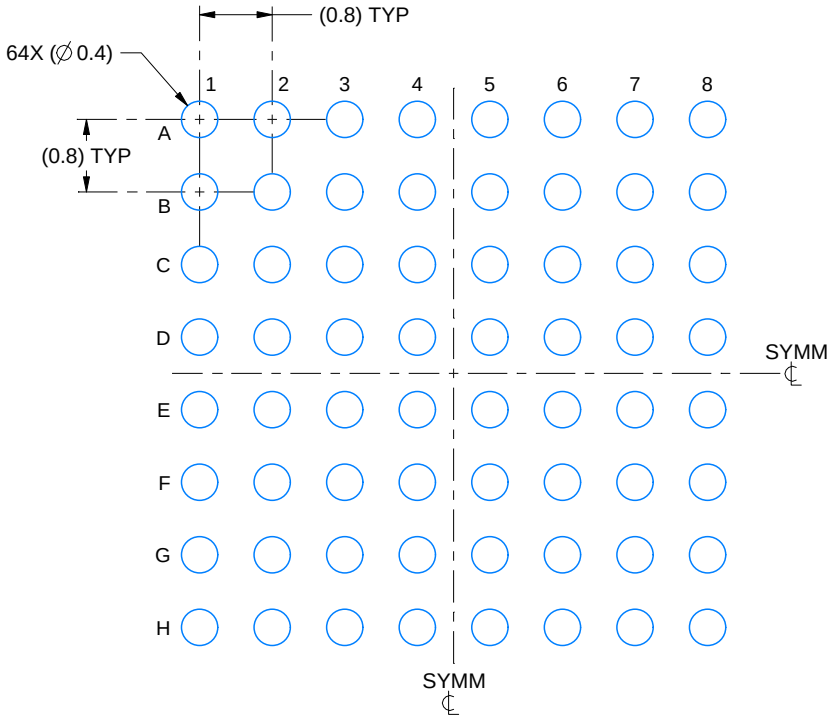
PLASTIC BALL GRID ARRAY



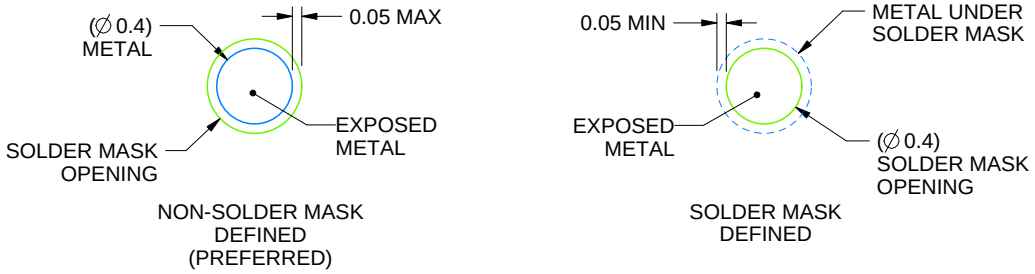
4220524/A 12/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

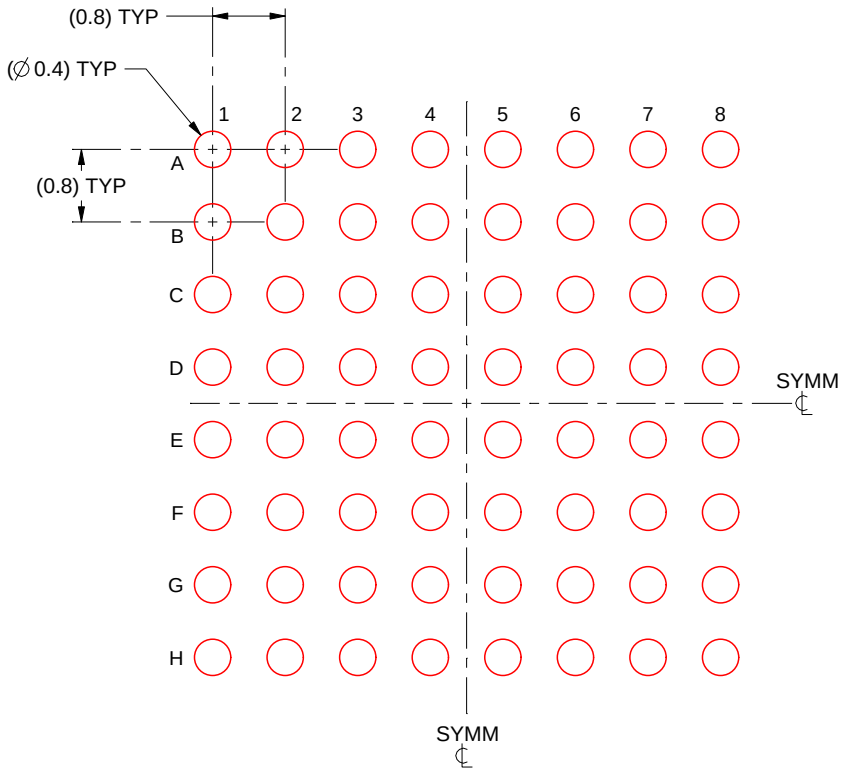


SOLDER MASK DETAILS
NOT TO SCALE

4220524/A 12/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:12X

4220524/A 12/2018

NOTES: (continued)

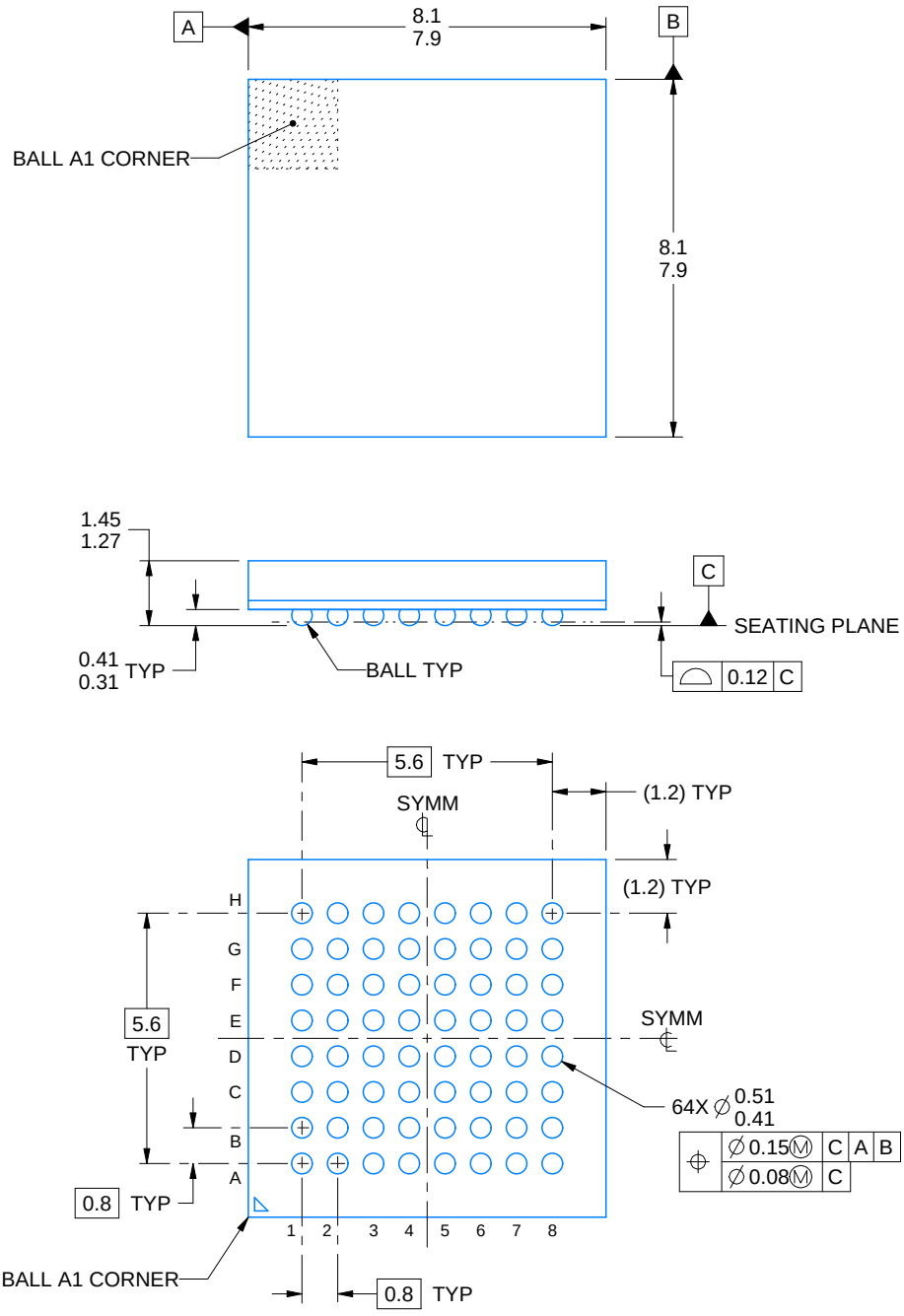
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ZXG0064A

NFBGA - 1.45 mm max height

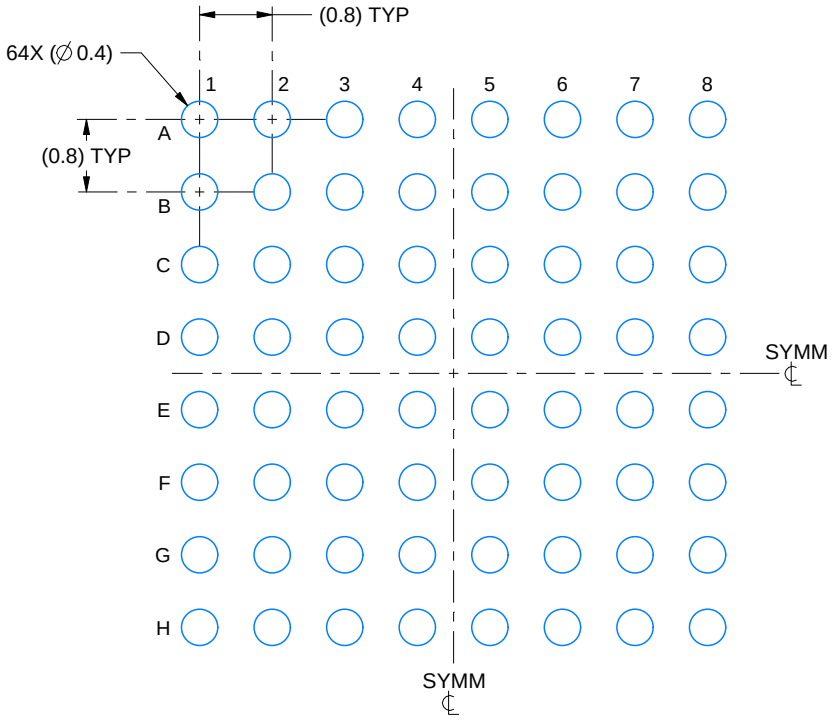
PLASTIC BALL GRID ARRAY



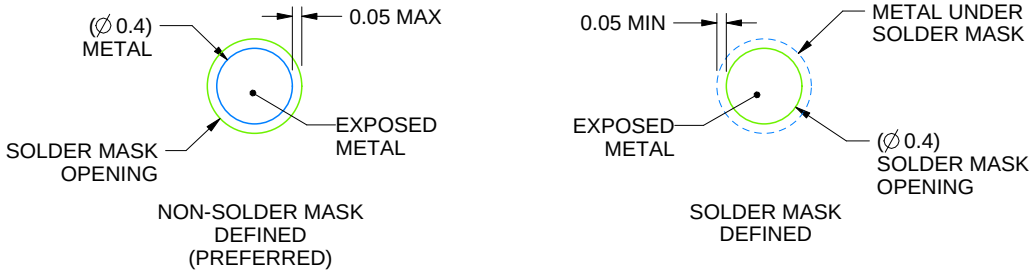
4220377/A 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is lead-free.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

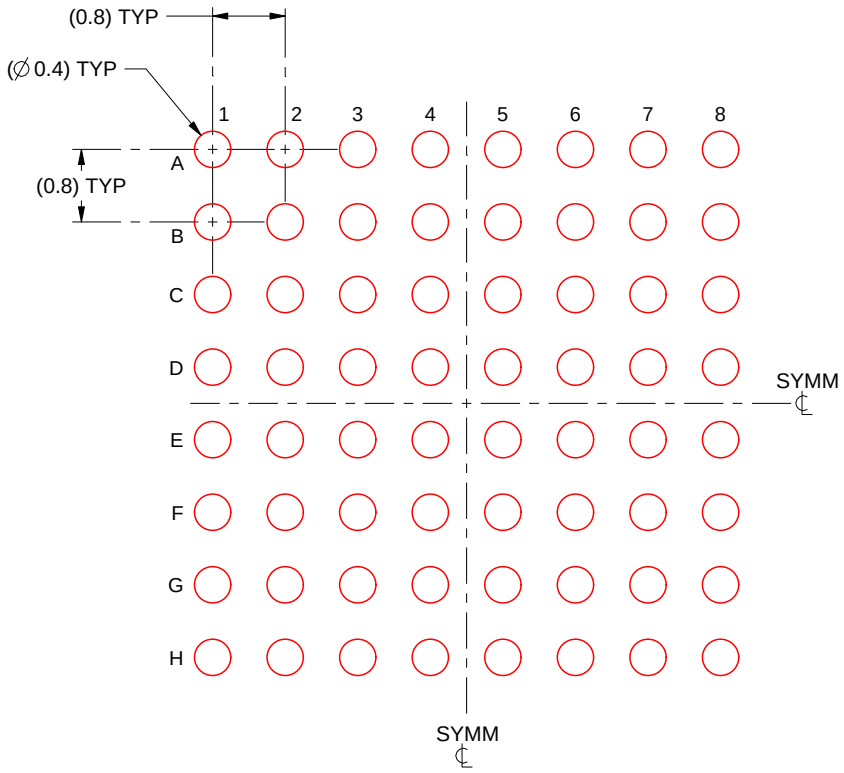


SOLDER MASK DETAILS
NOT TO SCALE

4220377/A 03/2023

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:12X

4220377/A 03/2023

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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