具有 JESD204B 接口、片上 PLL 和宽带插值的 DAC38RF8x 双通道、差分输出、14 位、9GSPS、射频采样 DAC

1 特性

- 具有多模式运行方式的 14 位分辨率、9GSPS DAC
  - 16 位、双通道数据模式
    - 最大输入速率：2.5GSPS
    - 宽带数字上变频器
      - 插值：1、2、4、6、8、10、12、16、18、20、24x
  - 12 位、双通道数据模式
    - 最大输入速率：3.33GSPS
    - 宽带数字上变频器
      - 插值：1、2、24x
  - 8 位、单通道数据模式
    - 最大输入速率：9GSPS
- JESD204B 接口
  - 子类 1 支持多芯片同步
  - 最大通道速率：12.5Gbps
- 差分输出
  - 支持直流耦合
  - 射频满量程输出功率（采用 2:1 平衡-非平衡变压器）：2.14GHz 时为 3dBm
- 具有旁路功能的内部 PLL 和 VCO
  - DAC38RF82：$f_{C(VCO)}$ = 5.9 或 8.9GHz
  - DAC38RF89：$f_{C(VCO)}$ = 5 或 7.5GHz
- 电源：-1.8V、1.0V、1.8V
- 封装：10mm x 10mm BGA，间距为 0.8mm，144 个焊球

2 应用

- 任意波形发生器
- 雷达和电子战
- 通信测试设备
- 符合 DOCSIS 3.0/3.1 要求的直接射频合成
- 微波回程

3 说明

DAC38RF82 和 DAC38RF89 是高性能的宽带宽型射频采样数模转换器 (DAC)，能够实现高达 3.33GSPS 的双通道输入数据速率或高达 9GSPS 的 8 位单通道运行状态。这些器件具有一个多达 8 通道的低功耗 JESD204B 接口，最大比特率为 12.5Gbps。

在双通道运行状态下，无插值时输入接口的数据速率高达 3.33GSPS（12 位分辨率）和 2.5GSPS（16 位分辨率）。当用作具有 2x 至 24x 插值模式的复合基带发送器时，DAC38RF82 或 DAC38RF89 可以合成具有 16 位输入分辨率的高达 2GHz 带宽的宽带信号和具有 12 位输入分辨率的 2.66GHz 带宽的宽带信号。

8 位模式允许以 9GSPS 的最大 DAC 采样率进行输入，并可合成 0 至 4.5GHz 的宽带信号。

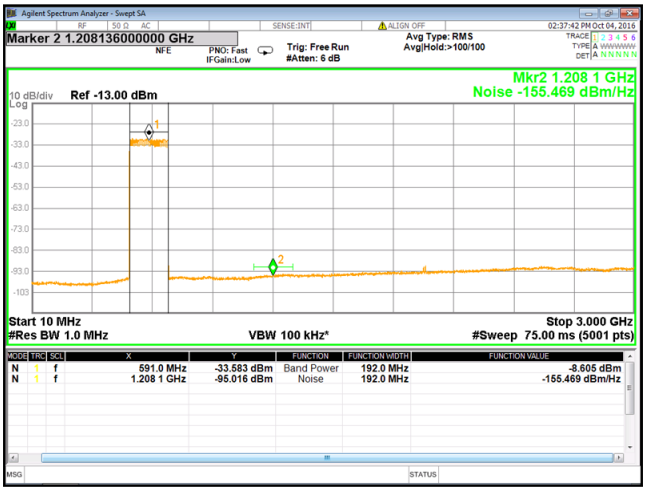
可选的低抖动 PLL/VCO 通过允许使用频率较低的参考时钟来简化 DAC 时钟的生成。DAC38RF82 和 DAC38RF89 支持不同的 VCO 频率范围，如*器件比较表* 所示。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DAC38RF82	FCBGA (144)	10.0mm x 10.0mm
DAC38RF89		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

32x6MHz 256QAM 载波



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (August 2017) to Revision C — **Page**

- Changed the t_r NOM value from 50 ns To 50 ps in the Anaolog Output of the *Timing Requirements* table ... 17
- Changed the t_f NOM value from 50 ns To 50 ps in the Anaolog Output of the *Timing Requirements* table ... 17
- Changed the MPY values in Table 4 ... 27
- Changed The title From: SerDes PLL Modes Selection To: SerDes PLL Multiplier (MPY) Values in in Table 4 ... 27
- Added section: *Digital Quadrature Modulator* ... 53
- Added section: *Low Power Coarse Resolution Mixing Modes* ... 54
- Added cross reference to MPY values in Table 132 ... 124
- Changed the enable/disable description for bit [15:13] of Table 134 ... 126

Changes from Revision A (April 2017) to Revision B — **Page**

- 已删除 将特性 中的“插值：1、2、4、24x”更改为“插值：1、2、24x” ... 1
- Changed the ALARM pin From: alarm_out_pol To: alm_out_pol in the *Pin Functions* table ... 5
- Changed the Description of pins A3, A4, A7, A6, A9, A10, A12, E12, F11, F7, G6, H5, H7, J6, J11 in the *Pin Functions* table ... 5
- Changed description of TXENABLE pin in the *PIN Functions* table ... 6
- Changed the MAX value of VEE18N rail From: 0.5 V To 0.3 V in the *Absolute Maximum Ratings* table ... 7
- Added "Supply Voltage Range" to the *Recommended Operating Conditions* table ... 7
- Changed DNL typical value From: ±0.5 to ±3 LSB in *Electrical Characteristics - DC Specifications* table ... 8
- Changed INL typical value From: ±1 To: ±4 LSB in *Electrical Characteristics - DC Specifications* table ... 8
- Added "Reference voltage drift" to the *Electrical Characteristics - DC Specifications* table ... 8
- Changed Power Dissipation Test Condition From: MODE 5: dual channel, 8-bit input mode, 2x Interpolation To: MODE 5: dual channel, 8-bit input mode, 1x Interpolation in the *Electrical Characteristics - DC Specifications* ... 9
- Changed the ILOAD values to negative for CMOS interface parameter, low-level output voltage, in the *Electrical*

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Characteristics - Digital Specifications table 10
- Added 0 dBFS to the condition statement for the *Electrical Characteristics - AC Specifications* table 13
- Added MIN and TYP value to maximum DAC sample rate for DAC38RF89 only in the *Electrical Characteristics - AC Specifications* table 13
- Added NSD values for DAC38RF82 with on-chip PLL enabled to *Electrical Characteristics - AC Specifications* table 15
- Changed the Isolation values in the TEST CONDITIONS, TYP value From: 74 dBc To: 82 dBc and 56 dBc To 73 dBc in the *Electrical Characteristics - AC Specifications* table 15
- Added Figure 16 19
- Added MPY value for 16.5x in the Table 4 27
- Changed input rate max and fdac max for 6x interpolation mode in Table 9 30
- Changed input data rate From: 6666 MSPS To: 3333 MSPS for LMFSHd=41380, 2x interpolation in Table 9 31
- Changed Table 12, JESD204B frame format for LMFSHd=84111 31
- Changed Table 14, JESD204B frame format for LMFSHd=44210 32
- Changed Table 16, JESD204B frame format for LMFSHd = 24410 32
- Changed Table 17, JESD204B frame format for LMFSHd = 44210 32
- Changed Table 18, JESD204B frame format for LMFSHd = 88210 33
- Changed Table 19, JESD204B frame format for LMFSHd = 24410 33
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- Changed Table 22, JESD204B frame format for LMFSHd = 48310 33
- Changed *Table 23, JESD204B frame format for LMFSHd = 81180* 34
- Changed Table 24, JESD204B frame format for LMFSHd = 41380 34
- Changed Table 26, JESD204B frame format for LMFSHd = 41121 35
- Added Table 27, JESD204B frame format for LMFSHd = 41121 36
- Changed Table 38 47
- Changed register field programming values for LMFSHd=24410, 41380, 41121 and 24310 in the *Register Programming for JESD and Interpolation Mode* table 52
- Changed the bit positions of N_M1 register field From: 12-8 To: 4-0 in the Table 42 table 53
- Changed the bit positions of N_M1' (NPRIME_M1) register field From: 4-0 To: 12-0 in the Table 42 table 53
- Changed the description of DAC PLL alarm in *Alarm Monitoring* 58
- Changed from BIST_ENA to Reserved in Table 61 78
- Changed from BIST_ZERO to Reserved in Table 61 78
- Changed the description of OUTSUM_SEL field in Table 69 84
- Changed the Description of Bit 11 From "dummy data generation" to "distortion enhancement" in Table 116 114
- 已更改 the junction temp and loop filter voltage range for PLL tuning in 图 142 128

Changes from Original (February 2017) to Revision A **Page**

- Corrected the NSD values for -9dBFS in *Electrical Characteristics - AC Specifications* table 15
- Added PLL/VCO characteristics table to PLL/VCO Electrical Characteristics 16
- Added JESD204B clock phase register setting to Table 41 52
- Removed descriptions for CLKJESD_DIV register from Table 41 52
- Added JESD204B clock phase register setting to Table 42 52
- Added information about the DAC output total current for various full scale current settings in DAC Fullscale Output Current 60
- Changed Bit 0 of Table 128 From: Enables the GSM PLL To: Reserved 121
- Changed Table 130 123
- Changed description of SERDES_REFCLK_DIV register field in Table 131 124

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• Changed Bit 12:11, 6:5 and 4:2 of Table 134 126

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5 Device Comparison Table

PART NUMBER	ANALOG OUTPUT TYPE	VCO0 CENTER FREQUENCY	VCO1 CENTER FREQUENCY
DAC38RF82	Differential	5.9 GHz	8.9 GHz
DAC38RF89	Differential	5 GHz	7.5 GHz

6 Pin Configuration and Functions

AAV Package
144-Pin (FCBGA)
Top View

	A	B	C	D	E	F	G	H	J	K	L	M
12	DACCLKSE	VSSCLK	AGND	VOUT2+	VOUT2-	AGND	VDDOUT18	VDDOUT18	AGND	VOUT1-	VOUT1+	AGND
11	VSSCLK	VSSCLK	AGND	AGND	AGND	VDDA1	VDDA18	VDDA18	VDDA1	AGND	AGND	AGND
10	DACCLK+	VDDAPLL18	EXTIO	VEE18N	VEE18N	VSSCLK	VDDL2_1	VDDL2_1	VSSCLK	VEE18N	VEE18N	SDIO
9	DACCLK-	VDDAPLL18	RBIAS	VDDAVCO18	VDDAVCO18	VSSCLK	VDDCLK1	VDDCLK1	VSSCLK	$\overline{\text{RESET}}$	SCLK	SDO
8	VSSCLK	VSSCLK	ATEST	VDDPLL1	VDDPLL1	VSSCLK	VDDL1_1	VDDL1_1	VSSCLK	ALARM	SLEEP	$\overline{\text{SDEN}}$
7	CLKTX+	VDDTX18	$\overline{\text{SYNC1+}}$	VDDDIG1	DGND	VDDE1	DGND	VDDE1	DGND	GPI0	GPO0	GPI1
6	CLKTX-	VDDTX1	$\overline{\text{SYNC1-}}$	DGND	VDDDIG1	DGND	VDDE1	DGND	VDDE1	TXENABLE	GPO1	DGND
5	VDDDIG1	VDDDIG1	VDDDIG1	VDDDIG1	VDDDIG1	VDDDIG1	VDDDIG1	VDDIO18	$\overline{\text{TRST}}$	TMS	DGND	RX3+
4	SYSREF-	VDDS18	$\overline{\text{SYNC0+}}$	VSENSE	VDDDIG1	VDDDIG1	VDDDIG1	TDI	TDO	TCLK	DGND	RX3-
3	SYSREF+	VDDS18	$\overline{\text{SYNC0-}}$	IFORCE	VDDDIG1	AMUX1	AMUX0	VDDT1	VDDT1	TESTMODE	DGND	RX2-
2	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDR18	VDDR18	DGND	DGND	RX2+
1	RX7+	RX7-	RX6-	RX6+	RX5+	RX5-	RX4-	RX4+	RX0+	RX0-	RX1-	RX1+

Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
C11, C12, D11, E11, F12, J12, K11, L11, M11, M12	AGND	–	Analog ground.
K8	ALARM	O	CMOS output for ALARM condition. Default polarity is active low, but can be changed to active high via RESET_CONFIG alm_out_pol control bit..
G3	AMUX0	O	Analog test pin for SerDes, Lane 0 to Lane 3. Can be left floating.
F3	AMUX1	O	Analog test pin for SerDes, Lane 4 to Lane 7. Can be left floating.
C8	ATEST	O	Analog test pin for DAC, references and PLL. Can be left floating.
A7	CLKTX+	O	Divided output clock, internal 100 Ω differential termination, self-biased, positive terminal.
A6	CLKTX-	O	Divided output clock, internal 100 Ω differential termination, self-biased, negative terminal.
A10	DACCLK+	I	Device clock, internal 100 Ω differential termination, self-biased, positive terminal.
A9	DACCLK-	I	Device clock, internal 100 Ω differential termination, self-biased, negative terminal.
A12	DACCLKSE	I	Single ended device clock optional input. Can be left floating if not used, internal 50 Ω termination.
A2, B2, C2, D2, D6, E2, E7, F2, F6, G2, G7, H6, J7, K2, L2, L3, L4, L5, M6	DGND	-	Digital ground.
C10	EXTIO	I/O	Requires a 0.1 μF decoupling capacitor to AGND.
K7	GPI0	-	Factory use only. User should GND.
M7	GPI1	-	Factory use only. User should GND.
L7	GPO0	O	Used for CMOS SYNC0\ signal.
L6	GPO1	O	Used for CMOS SYNC1\ signal.
D3	IFORCE	O	Test pin for on chip parametrics. Can be left floating.
C9	RBIAS	O	Full-scale output current bias. Change the full-scale output current through DACFS in register DACFS (8.5.72). Expected to be 3.6 kΩ to GND for 40 mA full scale output.
K9	$\overline{\text{RESET}}$	I	Active low input for chip RESET, which resets all the programming registers to their default state. Internal pull-up.
J1	RX0+	I	CML SerDes interface lane 0 input, positive
K1	RX0-	I	CML SerDes interface lane 0 input, negative
M1	RX1+	I	CML SerDes interface lane 1 input, positive
L1	RX1-	I	CML SerDes interface lane 1 input, negative
M2	RX2+	I	CML SerDes interface lane 2 input, positive
M3	RX2-	I	CML SerDes interface lane 2 input, negative
M5	RX3+	I	CML SerDes interface lane 3 input, positive
M4	RX3-	I	CML SerDes interface lane 3 input, negative
H1	RX4+	I	CML SerDes interface lane 4 input, positive
G1	RX4-	I	CML SerDes interface lane 4 input, negative
E1	RX5+	I	CML SerDes interface lane 5 input, positive
F1	RX5-	I	CML SerDes interface lane 5 input, negative
D1	RX6+	I	CML SerDes interface lane 6 input, positive
C1	RX6-	I	CML SerDes interface lane 6 input, negative
A1	RX7+	I	CML SerDes interface lane 7 input, positive
B1	RX7-	I	CML SerDes interface lane 7 input, negative
L9	SCLK	I	Serial interface clock. Internal pull-down.
M8	$\overline{\text{SDEN}}$	I	Active low serial data enable, always an input to the DAC38RFxx. Internal pull-up.
M10	SDIO	I/O	Serial interface data. Bi-directional in 3-pin mode (default) and uni-directional input 4-pin mode. Internal pull-down.
M9	SDO	O	Uni-directional serial interface data output in 4-pin mode. The SDO pin is tri-stated in 3-pin interface mode (default).
L8	SLEEP	I	Active high asynchronous hardware power-down input. Internal pull-down.
C4	$\overline{\text{SYNC0+}}$	O	Synchronization request to transmitter for JESD204B link 0, LVDS positive output.
C3	$\overline{\text{SYNC0-}}$	O	Synchronization request to transmitter for JESD204B link 0, LVDS negative output.
C7	$\overline{\text{SYNC1+}}$	O	Synchronization request to transmitter for JESD204B link 1, LVDS positive output.
C6	$\overline{\text{SYNC1-}}$	O	Synchronization request to transmitter for JESD204B link 1, LVDS negative output.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
A3	SYSREF+	I	LVPECL SYSREF positive input, internal 100 Ω differential termination, self biased. This positive/negative pair is captured with the rising edge of DACCLKP/N. It is used for multiple DAC synchronization.
A4	SYSREF-	I	LVPECL SYSREF negative input, self biased, internal 100 Ω differential termination. (See the SYSREF+ description)
K4	TCLK	I	JTAG test clock. Internal pull-down
H4	TDI	I	JTAG test data in. Internal pull-up
J4	TDO	O	JTAG test data out. Internal pull-up
K3	TESTMODE	-	This pin is used for factory testing. Recommended to connect to ground for normal operation.
K5	TMS	I	JTAG test mode select. Internal pull-up
J5	$\overline{\text{TRST}}$	I	JTAG test reset. Internal pull-up. Must be connected to ground if not used
K6	TXENABLE	I	Transmit enable active high input. Internal pull-down. This pin is ORed with spi_txenable bit in JESD_FIFO register to enable analog output data transmission. To enable analog output data transmission, pull CMOS TXENABLE pin to high. To disable analog output, pull CMOS TXENABLE pin to low. The DAC output is forced to midscale.
F11, J11	VDDA1	I	Analog 1 V supply voltage. Must be separated from VDDDIG1 supply for best performance.
G11, H11	VDDA18	I	Analog 1.8 V supply voltage. (1.8 V)
D8, E8	VDDPLL1	I	Analog 1 V supply for PLL.
B9, B10	VDDAPLL18	I	PLL analog supply voltage. (1.8 V)
D9, E9	VDDAVCO18	I	Analog supply voltage for VCO (1.8 V)
G9, H9	VDDCLK1	I	Internal clock buffer supply voltage (1 V). It is recommended to isolate this supply from VDDDIG1 and VDDA1.
G8, H8	VDDL1_1	I	DAC core supply voltage. (1 V)
G10, H10	VDDL2_1	I	DAC core supply voltage. (1 V)
A5, B5, C5, D5, D7, E3, E4, E5, E6, F4, F5, G4, G5	VDDDIG1	I	Digital supply voltage. (1 V). It is recommended to isolate this supply from VDDCLK1 and VDDA1.
F7, H7, G6, J6	VDDE1	I	Digital Encoder supply voltage (1 V). Must be separated from VDDDIG1 supply
H5	VDDIO18	I	Supply voltage for all digital I/O and CMOS I/O. (1.8 V)
G12, H12	VDDOUT18	I	DAC output supply. (1.8 V)
H2, J2	VDDR18	I	Supply voltage for SerDes. (1.8 V)
B3, B4	VDDS18	I	Supply voltage for LVDS $\overline{\text{SYNC0+/-}}$ and $\overline{\text{SYNC1+/-}}$ (1.8 V)
H3, J3	VDDT1	I	Supply voltage for SerDes termination. (1 V)
B6	VDDTX1	I	Supply voltage for divided clock output. (1 V)
B7	VDDTX18	I	Supply voltage for divided clock output . (1.8 V)
D10, E10, K10, L10	VEE18N	I	Analog supply voltage. (-1.8 V)
L12	VOUT1+	O	DAC channel 1 output.
K12	VOUT1-	O	DAC channel 1 complementary output.
D12	VOUT2+	O	DAC channel 2 output.
E12	VOUT2-	O	DAC channel 2 complementary output.
D4	VSENSE	O	Test pin for on chip parametrics. Can be left floating.
A8, A11, B8, B11, B12, F8, F9, F10, J8, J9, J10	VSSCLK	-	Clock ground.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply Voltage Range[2]	VDDDAC1, VDDDIG1, VDDL1_1, VDDL2_1, VDDCLK1, VDDT1, VDDCLK1, VDDTX1, VDDE1	–0.3	1.3	V
	VDDR18, VDDIO18, VDDS18, VDDAPLL18, VDDAREF18, VDDAOUT18, VDDA18, VDDAVCO18, VDDTX18	–0.3	2.45	V
	VEE18N	–2	0.3	V
Voltage between AGND and DGND		–0.3	0.3	V
Pin Voltage Range[2]	RX[0..7]+/-	–0.5	VDDDIG1 + 0.5 V	V
	$\overline{\text{SDEN}}$, SCLK, SDIO, SDO, TXENABLE, ALARM, $\overline{\text{RESET}}$, SLEEP, TMS, TCLK, TDI, TDO, $\overline{\text{TRST}}$, TESTMODE, GPI0, GPI1, GPO0, GPO1	–0.5	VDDIO + 0.5 V	V
	CLKOUT+/-	–0.5	VDDTX18 + 0.5 V	V
	DACCLK+/-, SYSREF+/-, DACCLKSE	–0.5	VDDCLK1 + 0.5 V	V
	$\overline{\text{SYNC0+/-}}$, $\overline{\text{SYNC1+/-}}$	–0.5	VDDS18 + 0.5 V	V
	IOUT1+/-, IOUT2+/-	–0.5	VDDAOUT18 + 0.5 V	V
	RBIAS, EXTIO, ATEST	–0.5	VDDAOUT18 + 0.5 V	V
	IFORCE, VSENSE	–0.5	VDDDIG1 + 0.5 V	V
	AMUX1, AMUX0	–0.5	VDDT1 + 0.5 V	V
Peak input current (any input)			20	mA
Peak total input current (all inputs)		–30		mA
Junction temperature T_J			150	°C
Operating free-air temperature, T_A		–40	85	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND or DGND.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
T_J	Recommended operating temperature				105	°C
	Maximum rated operating junction temperature[1]		125			°C
T_A	Recommended free-air temperature		–40		85	°C
Supply Voltage Range		VDDA18, VDDAPLL18, VDDS18, VDDIO18, VDDR18, VDDAPLL18, VDDOUT18, VDDAVCO18	1.71	1.8	1.89	V
		VDDDIG1 VDDA1, VDDT1, VDDAPLL1, VDDCLK1, VDDL1_1, VDDL2_1, VDDTX1, VDDE1	0.95	1	1.05	
		VEE18N	–1.89	–1.8	–1.71	

(1) Prolonged use at this junction temperature may increase the device failure-in-time (FIT) rate

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7.4 Thermal Information

THERMAL METRIC[1]		DAC38RF82 DAC38RF89 AAV (FCBGA) 144 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics - DC Specifications

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, nominal supplies, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
	Digital Input Resolution	8-bit Input Mode	8			bits
		12-bit Input Mode	12			
		16-bit Input Mode	16			
	DAC Core Resolution		14			bits
	DNL Differential nonlinearity			±3		LSB
	INL Integral nonlinearity			±4		LSB
Analog Output						
	Gain Error			±2		%FSR
	Full scale output current		10	30	40	mA
$P_{(OUTFS)}$	Full scale output power	2:1 transformer coupled into 50 Ω- load. Transformer (TCM2-452X-2+) loss not de-embedded 2.1 GHz output frequency		3		dBm
	Output Compliance Range		1.3		2.3	V
	Output capacitance	Single ended to ground		1.5		pF
	Output resistance	Differential		100		ohms
Reference Output: EXTIO						
V_{REF}	Reference output voltage			0.9		V
	Reference output current			100		nA
	Reference voltage drift			±8		ppm/°C
Power Supply Current and consumption						
	1 V Digital supplies: VDDDIG1	MODE 1: dual channel, 12-bit input mode, 2x Interpolation, Sin(x)/x enabled, f_{DAC} = 6 GHz, CLKTX Disabled		815	1300	mA
	1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1144	1250	mA
	1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			218	270	mA
	-1.8 V Supply: VEE18N			159	180	mA
P_{DIS}	Power Dissipation			2638	3360	mW
	1 V Digital supplies: VDDDIG1	MODE 2: dual channel, 16-bit input mode, 2x Interpolation, Sin(x)/x enabled, f_{DAC} = 5 GHz, CLKTX Disabled		798		mA
	1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1026		mA
	1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			222		mA
	-1.8 V Supply: VEE18N			159		mA
P_{DIS}	Power Dissipation			2510		mW

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Electrical Characteristics - DC Specifications (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, nominal supplies, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	1V Digital supplies: VDDDIG1	MODE 3: dual channel, 12-bit input mode, 2x Interpolation, Sin(x)/x enabled, f_{DAC} = 3 GHz, CLKTX Disabled		500		mA
	1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			751		mA
	1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			218		mA
	-1.8V Supply: VEE18N			159		mA
P_{DIS}	Power Dissipation			1930		mW
	1 V Digital supplies: VDDDIG1	MODE 4: dual channel, 16-bit input mode, 2x Interpolation, Sin(x)/x enabled, f_{DAC} = 2.5 GHz, CLKTX Disabled		517		mA
	1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			708		mA
	1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			222		mA
	-1.8 V Supply: VEE18N			159		mA
P_{DIS}	Power Dissipation			1911		mW
	1 V Digital supplies: VDDDIG1	MODE 5: dual channel, 8-bit input mode, 1x Interpolation, Sin(x)/x enabled, f_{DAC} = 9 GHz, CLKTX Disabled		624		mA
	1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			1469		mA
	1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			218		mA
	-1.8 V Supply: VEE18N			159		mA
P_{DIS}	Power Dissipation			2772		mW
	1 V Digital supplies: VDDDIG1	MODE 6: Power down mode, no clock, DAC in sleep, SerDes in sleep, CLKTX Disabled		63	568	mA
	1 V Analog supplies: VDDA1 VDDACLK1 VDDTX1 VDDAPLL1 VDDT1 VDDE1			18	105	mA
	1.8 V Supplies: VDDA18 VDDOUT18 VDDAVCO18 VDDAPLL18 VDDR18 VDDIO18 VDDS18 VDDTX18			47	51	mA
	-1.8 V Supply: VEE18N			23	28	mA
P_{DIS}	Power Dissipation			208	815	mW
	VDDTX1	f_{DAC} = 8847 MSPS, Clock Out Divider Enabled		25		mA
		f_{DAC} = 5898 MSPS, Clock Out Divider Enabled		19		mA
	VDDTX18	Clock Out Enabled		16		mA

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7.6 Electrical Characteristics - Digital Specifications

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, external differential clock mode at 9 GSPS, 12x Interpolation, f_{OUT} = 2.14 GHz, $I_{(OUTFS)}$ = 40 mA, nominal supplies, LMFSHd = 84111, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs: RX[7:0]+/-						
V_{DIFF}	Receiver input amplitude		50		1200	mV
V_{COM}	Input Common Mode Voltage	TERM = 111		600		mV
		TERM = 001		700		
		TERM = 100		0		
		TERM = 101		250		
Z_{DDIFF}	Internal differential termination		85	100	115	Ω
f_{SerDes}	SerDes bit rate		0.78125		12.5	Gbps
Differential Clock Inputs: SYSREF±, DACCLK±						
f_{DACCLK}	DACCLK input frequency		0.1		9	GHz
V_{COM}	Input common mode voltage			0.5		V
$V_{I(DPP)}$	Differential input peak-to-peak voltage			800	2000	mV
Z_T	Internal termination			100		Ω
C_L	Input capacitance			2		pF
	Duty cycle (DACCLK only		40%		60%	
LVDS Output: $\overline{\text{SYNC0}}$±, $\overline{\text{SYNC1}}$±						
V_{COM}	Output common mode voltage			1.2		V
Z_T	Internal termination			100		Ω
V_{OD}	Differential output voltage swing			500		mV
CML Output: DIVCLKOUT±						
V_{OD}	CML OUTPUT: CLKTX+/-			1300		mV
CMOS Interface: $\overline{\text{SDEN}}$, SCLK, SDIO, SDO, TXENABLE, ALARM, $\overline{\text{RESET}}$, SLEEP, TMS, TCLK, TDI, TDO, $\overline{\text{TRST}}$, TESTMODE, SYNCSE1, $\overline{\text{SYNCSE2}}$						
V_{IH}	High-level input voltage		0.7 x VDDIO			V
V_{IL}	Low-level input voltage				0.3 x VDDIO	V
I_{IH}	High-level input current		–40		40	µA
I_{IL}	Low-level input current		–40		40	µA
C_I	CMOS input capacitance			2		pF
V_{OH}	High-level output voltage	I_{LOAD} = –100 µA	VDDIO – 0.2			V
		I_{LOAD} = –2 mA	0.8 x VDDIO			
V_{OL}	Low-level output voltage	I_{LOAD} = 100 µA			0.2	V
		I_{LOAD} = 2 mA			0.5	
Latency						
	RX SerDes Digital Delay	full rate, RATE = “00”		34		UI
		half rate, RATE = “01”		29		
		quarter rate, RATE = “10”		26.5		
		eighth rate, RATE = “11”		26.25		
	SerDes output to JED204B elastic buffer input latency			21 -39		JESD clock cycles

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Electrical Characteristics - Digital Specifications (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, external differential clock mode at 9 GSPS, 12x Interpolation, f_{OUT} = 2.14 GHz, $I_{(OUTFS)}$ = 40 mA, nominal supplies, LMFSHd = 84111, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Latency: JESD Buffer to DAC Output	LMFSHD = 41121 or 82121, 1x Interpolation		269		DAC clock cycles
	LMFSHD = 41121 or 82121, 2x Interpolation		417		
	LMFSHD = 41121 or 82121, 4x Interpolation		717		
	LMFSHD = 41380 or 82380, 1x Interpolation		293		
	LMFSHD = 41380 or 82380, 2x Interpolation		465		
	LMFSHD = 81180, 1x Interpolation		289		
	LMFSHD = 82121, 6x Interpolation		269		
	LMFSHD = 82121, 8x Interpolation		1120		
	LMFSHD = 82121, 12x Interpolation		1602		
	LMFSHD = 82121, 16x Interpolation		2091		
	LMFSHD = 42111 or 84111, 6x Interpolation		817		
	LMFSHD = 42111 or 84111, 8x Interpolation		1057		
	LMFSHD = 42111 or 84111, 10x Interpolation		1184		
	LMFSHD = 42111 or 84111, 12x Interpolation		1532		
	LMFSHD = 42111 or 84111, 16x Interpolation		1997		
	LMFSHD = 42111 or 84111, 18x Interpolation		2142		
	LMFSHD = 42111 or 84111, 24x Interpolation		2941		
	LMFSHD = 22210 or 44210, 8x Interpolation		1020		
	LMFSHD = 22210 or 44210, 12x Interpolation		1473		
	LMFSHD = 22210 or 44210, 16x Interpolation		1917		
	LMFSHD = 22210 or 44210, 18x Interpolation		2050		
	LMFSHD = 22210 or 44210, 20x Interpolation		2275		
	LMFSHD = 22210 or 44210, 24x Interpolation		2821		
	LMFSHD = 12410 or 24410, 16x Interpolation		1912		
	LMFSHD = 12410 or 24410, 24x Interpolation		2786		
	LMFSHD = 44210 or 88210, 8x Interpolation		916		
	LMFSHD = 44210 or 88210, 12x Interpolation		1317		
	LMFSHD = 44210 or 88210, 16x Interpolation		1709		
	LMFSHD = 44210 or 88210, 24x Interpolation		2509		
	LMFSHD = 24410 or 48410, 16x Interpolation		1672		
	LMFSHD = 24410 or 48410, 24x Interpolation		1593		

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Electrical Characteristics - Digital Specifications (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, external differential clock mode at 9 GSPS, 12x Interpolation, f_{OUT} = 2.14 GHz, $I_{(OUTFS)}$ = 40 mA, nominal supplies, LMFSHd = 84111, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSREF TO JESD LMFC RESET	LMFSHD = 41121 or 82121, 1x Interpolation		13		JESD clock cycles
	LMFSHD = 41121 or 82121, 2x Interpolation		9		
	LMFSHD = 41121 or 82121, 4x Interpolation		6		
	LMFSHD = 41380 or 82380, 1x Interpolation		15		
	LMFSHD = 41380 or 82380, 2x Interpolation		10		
	LMFSHD = 81180, 1x Interpolation		6		
	LMFSHD = 82121, 6x Interpolation		5		
	LMFSHD = 82121, 8x Interpolation		5		
	LMFSHD = 82121, 12x Interpolation		5		
	LMFSHD = 82121, 16x Interpolation		5		
	LMFSHD = 42111 or 84111, 6x Interpolation		16		
	LMFSHD = 42111 or 84111, 8x Interpolation		16		
	LMFSHD = 42111 or 84111, 10x Interpolation		15		
	LMFSHD = 42111 or 84111, 12x Interpolation		15		
	LMFSHD = 42111 or 84111, 16x Interpolation		13		
	LMFSHD = 42111 or 84111, 18x Interpolation		15		
	LMFSHD = 42111 or 84111, 24x Interpolation		15		
	LMFSHD = 22210 or 44210, 8x Interpolation		8		
	LMFSHD = 22210 or 44210, 12x Interpolation		7		
	LMFSHD = 22210 or 44210, 16x Interpolation		6		
	LMFSHD = 22210 or 44210, 18x Interpolation		7		
	LMFSHD = 22210 or 44210, 20x Interpolation		5		
	LMFSHD = 22210 or 44210, 24x Interpolation		4		
	LMFSHD = 12410 or 24410, 16x Interpolation		9		
	LMFSHD = 12410 or 24410, 24x Interpolation		7		
	LMFSHD = 44210 or 88210, 8x Interpolation		29		
	LMFSHD = 44210 or 88210, 12x Interpolation		27		
	LMFSHD = 44210 or 88210, 16x Interpolation		26		
	LMFSHD = 44210 or 88210, 24x Interpolation		25		
	LMFSHD = 24410 or 48410, 16x Interpolation		8		
	LMFSHD = 24410 or 48410, 24x Interpolation		6		

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7.7 Electrical Characteristics - AC Specifications

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, external differential clock mode at 9 GSPS, 12x Interpolation, 0 dBFS, f_{OUT} = 2.14 GHz, $I_{(OUTFS)}$ = 40 mA, nominal supplies, LMFSHd = 84111, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Output						
f_{DAC}	Maximum DAC sample rate	DAC38RF82 only	9			GSPS
		DAC38RF89 only	8.4	9		
AC Performance - CW						
SFDR	Spurious Free Dynamic Range 0 – $f_{DAC}/2$	f_{CLK} = 6 GHz , f_{OUT} = 501 MHz		63		dBc
		f_{CLK} = 6 GHz , f_{OUT} = 951 MHz		62		
		f_{CLK} = 6 GHz , f_{OUT} = 1851 MHz		58		
		f_{CLK} = 6 GHz , f_{OUT} = 2651 MHz		57		
		f_{CLK} = 9 GHz , f_{OUT} = 501 MHz		62		
		f_{CLK} = 9 GHz , f_{OUT} = 951 MHz		61		
		f_{CLK} = 9 GHz , f_{OUT} = 1851 MHz		61		
		f_{CLK} = 9 GHz , f_{OUT} = 2651 MHz		54		
		f_{CLK} = 9 GHz , f_{OUT} = 3651 MHz		51		
SFDR	Spurious Free Dynamic Range within 500 MHz f_{OUT} ± 250 MHz	f_{CLK} = 6 GHz , f_{OUT} = 501 MHz		97		dBc
		f_{CLK} = 6 GHz , f_{OUT} = 951 MHz		93		
		f_{CLK} = 6 GHz , f_{OUT} = 1851 MHz		88		
		f_{CLK} = 6 GHz , f_{OUT} = 2651 MHz		77		
		f_{CLK} = 9 GHz , f_{OUT} = 501 MHz		94		
		f_{CLK} = 9 GHz , f_{OUT} = 951 MHz		90		
		f_{CLK} = 9 GHz , f_{OUT} = 1851 MHz		85		
		f_{CLK} = 9 GHz , f_{OUT} = 2651 MHz		82		
		f_{CLK} = 9 GHz , f_{OUT} = 3651 MHz		79		
SFDR	Spurious Free Dynamic Range excluding HD2, HD3 and CMP2 0 – $f_{DAC}/2$	f_{CLK} = 6 GHz , f_{OUT} = 501 MHz		72		dBc
		f_{CLK} = 6 GHz , f_{OUT} = 951 MHz		71		
		f_{CLK} = 6 GHz , f_{OUT} = 1851 MHz		74		
		f_{CLK} = 6 GHz , f_{OUT} = 2651 MHz		71		
		f_{CLK} = 9 GHz , f_{OUT} = 501 MHz		69		
		f_{CLK} = 9 GHz , f_{OUT} = 951 MHz		69		
		f_{CLK} = 9 GHz , f_{OUT} = 1851 MHz		72		
		f_{CLK} = 9 GHz , f_{OUT} = 2651 MHz		71		
		f_{CLK} = 9 GHz , f_{OUT} = 3651 MHz		67		
HD2	2nd Order Harmonic	f_{CLK} = 6 GHz , f_{OUT} = 501 MHz		72		dBc
		f_{CLK} = 6 GHz , f_{OUT} = 951 MHz		65		
		f_{CLK} = 6 GHz , f_{OUT} = 1851 MHz		57		
		f_{CLK} = 6 GHz , f_{OUT} = 2651 MHz		57		
		f_{CLK} = 9 GHz , f_{OUT} = 501 MHz		71		
		f_{CLK} = 9 GHz , f_{OUT} = 951 MHz		65		
		f_{CLK} = 9 GHz , f_{OUT} = 1851 MHz		62		
		f_{CLK} = 9 GHz , f_{OUT} = 2651 MHz		54		
		f_{CLK} = 9 GHz , f_{OUT} = 3651 MHz		51		

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Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, external differential clock mode at 9 GSPS, 12x Interpolation, 0 dBFS, f_{OUT} = 2.14 GHz, $I_{(OUTFS)}$ = 40 mA, nominal supplies, LMFSHd = 84111, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Order Harmonic	f_{CLK} = 6 GHz , f_{OUT} = 501 MHz		63		dBc
		f_{CLK} = 6 GHz , f_{OUT} = 951 MHz		62		
		f_{CLK} = 6 GHz , f_{OUT} = 1851 MHz		71		
		f_{CLK} = 6 GHz , f_{OUT} = 2651 MHz		69		
		f_{CLK} = 9 GHz , f_{OUT} = 501 MHz		62		
		f_{CLK} = 9 GHz , f_{OUT} = 951 MHz		61		
		f_{CLK} = 9 GHz , f_{OUT} = 1851 MHz		66		
		f_{CLK} = 9 GHz , f_{OUT} = 2651 MHz		65		
		f_{CLK} = 9 GHz , f_{OUT} = 3651 MHz		67		
CMP2	Fs/2 clock mixing product (Fs/2 – f_{OUT})	f_{CLK} = 6 GHz , f_{OUT} = 501 MHz		85		dBc
		f_{CLK} = 6 GHz , f_{OUT} = 951 MHz		85		
		f_{CLK} = 6 GHz , f_{OUT} = 1851 MHz		82		
		f_{CLK} = 6 GHz , f_{OUT} = 2651 MHz		79		
		f_{CLK} = 9 GHz , f_{OUT} = 501 MHz		78		
		f_{CLK} = 9 GHz , f_{OUT} = 951 MHz		76		
		f_{CLK} = 9 GHz , f_{OUT} = 1851 MHz		73		
		f_{CLK} = 9 GHz , f_{OUT} = 2651 MHz		74		
		f_{CLK} = 9 GHz , f_{OUT} = 3651 MHz		68		
CMP4+	Fs/N (N = 4, 8, 16) clock mixing product (f_{OUT} ± Fs/N)	f_{CLK} = 6 GHz , f_{OUT} = 501 MHz		92		dBc
		f_{CLK} = 6 GHz , f_{OUT} = 951 MHz		87		
		f_{CLK} = 6 GHz , f_{OUT} = 1851 MHz		81		
		f_{CLK} = 6 GHz , f_{OUT} = 2651 MHz		78		
		f_{CLK} = 9 GHz , f_{OUT} = 501 MHz		95		
		f_{CLK} = 9 GHz , f_{OUT} = 951 MHz		89		
		f_{CLK} = 9 GHz , f_{OUT} = 1851 MHz		84		
		f_{CLK} = 9 GHz , f_{OUT} = 2651 MHz		79		
		f_{CLK} = 9 GHz , f_{OUT} = 3651 MHz		74		
IMD3	Third-order two-tone intermodulation distortion	f_{CLK} = 6 GHz , f_{OUT} = 501 ± 5 MHz, –6 dBFS each tone		80		dBc
		f_{CLK} = 6 GHz , f_{OUT} = 951 ± 5 MHz, –6 dBFS each tone		76		
		f_{CLK} = 6 GHz , f_{OUT} = 1851 ± 5 MHz, –6 dBFS each tone		73		
		f_{CLK} = 6 GHz , f_{OUT} = 2651 ± 5 MHz, –6 dBFS each tone		72		
		f_{CLK} = 9 GHz , f_{OUT} = 501 ± 5 MHz, –6 dBFS each tone		80		
		f_{CLK} = 9 GHz , f_{OUT} = 951 ± 5 MHz, –6 dBFS each tone		75		
		f_{CLK} = 9 GHz , f_{OUT} = 1851 ± 5 MHz, –6 dBFS each tone		70		
		f_{CLK} = 9 GHz , f_{OUT} = 2651 ± 5 MHz, –6 dBFS each tone		70		
		f_{CLK} = 9 GHz , f_{OUT} = 3651 ± 5 MHz, –6 dBFS each tone		68		

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Electrical Characteristics - AC Specifications (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, external differential clock mode at 9 GSPS, 12x Interpolation, 0 dBFS, f_{OUT} = 2.14 GHz, $I_{(OUTFS)}$ = 40 mA, nominal supplies, LMFSHd = 84111, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Spectral Density > 50 MHz offset[(1)]	f_{CLK} = 6 GHz , f_{OUT} = 501 MHz		–170		dBFS/Hz
		f_{CLK} = 6 GHz , f_{OUT} = 951 MHz		–163		
		f_{CLK} = 6 GHz , f_{OUT} = 1851 MHz		–157		
		f_{CLK} = 6 GHz , f_{OUT} = 2651 MHz		–155		
		f_{CLK} = 9 GHz , f_{OUT} = 501 MHz		–172		
		f_{CLK} = 9 GHz , f_{OUT} = 951 MHz		–166		
		f_{CLK} = 9 GHz , f_{OUT} = 1851 MHz		–157		
		f_{CLK} = 9 GHz , f_{OUT} = 2651 MHz		–156		
		f_{CLK} = 9 GHz , f_{OUT} = 3651 MHz		–153		
		f_{CLK} = 6 GHz , f_{OUT} = 501 MHz, –9 dBFS		–172		
		f_{CLK} = 6 GHz , f_{OUT} = 951 MHz, –9 dBFS		–164		
		f_{CLK} = 6 GHz , f_{OUT} = 1851 MHz, –9 dBFS		–162		
		f_{CLK} = 9 GHz , f_{OUT} = 2651 MHz, –9 dBFS		–162		
		f_{CLK} = 9 GHz , f_{OUT} = 3651 MHz, –9 dBFS		–159		
NSD (on-chip PLL)	Noise Spectral Density > 50 MHz offset On-chip PLL enabled	f_{CLK} = 5 GHz , f_{OUT} = 501 MHz		–172		dBFS/Hz
		f_{CLK} = 5 GHz , f_{OUT} = 951 MHz		–166		
		f_{CLK} = 5 GHz , f_{OUT} = 1851 MHz		–157		
		f_{CLK} = 7.5 GHz , f_{OUT} = 501 MHz		–173		
		f_{CLK} = 7.5 GHz , f_{OUT} = 951 MHz		–167		
		f_{CLK} = 7.5 GHz , f_{OUT} = 1851 MHz		–159		
		f_{CLK} = 7.5 GHz , f_{OUT} = 2651 MHz		–155		
		f_{CLK} = 7.5 GHz , f_{OUT} = 3651 MHz		–151		
		f_{CLK} = 5 GHz , f_{OUT} = 501 MHz, –9 dBFS		–169		
		f_{CLK} = 5 GHz , f_{OUT} = 951 MHz, –9 dBFS		–167		
		f_{CLK} = 5 GHz , f_{OUT} = 1851 MHz, –9 dBFS		–162		
		f_{CLK} = 7.5 GHz , f_{OUT} = 2651 MHz, –9 dBFS		–162		
		f_{CLK} = 7.5 GHz , f_{OUT} = 3651 MHz, –9 dBFS		–157		
Isolation	Isolation between DAC A and DAC B analog output	f_{OUT} = 1856 MHz		82		dBc
		f_{OUT} = 3105 MHz		73		

(1) Also valid for on-chip PLL enabled in DAC38RF82

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7.8 PLL/VCO Electrical Characteristics

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, internal PLL/VCO clock mode, 12x Interpolation, f_{OUT} = 1.8 GHz, $I_{(OUTFS)}$ = 40 mA, nominal supplies, LMFSHd = 84111, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DAC38RF82			DAC38RF89			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
PLL/VCO									
f_{ref}	Reference clock frequency		100		f_{VCO} /4	100		f_{VCO} /4	MHz
f_{PFD}	Frequency of phase & frequency detector		100		500	100		500	MHz
f_{vcoL}	Low VCO operating frequency		5240		6720	4500		5600	MHz
f_{vcoH}	High VCO operating frequency		7960		9000	6600		8400	MHz
f_{BW}	Loop filter bandwidth			500			500		KHz
Low VCO Phase Noise									
Frequency Offset	600 KHz	f_{vco} = 6 GHz,CP=5, f_{PFD} = 500 MHz, measured at output frequency = 1.8 GHz		-123					dBc/Hz
	1.2 MHz			-132					
	1.8 MHz			-135					
	6.0 MHz			-146					
Frequency Offset	600 KHz	f_{vco} = 5 GHz,CP=5, f_{PFD} = 312.5 MHz, measured at output frequency = 1.8 GHz					-123		
	1.2 MHz						-132		
	1.8 MHz						-136		
	6.0 MHz						-147		
High VCO Phase Noise									
Frequency Offset	600 kHz	f_{vco} = 9 GHz, CP=5, f_{PFD} = 500 MHz, measured at output frequency = 1.8 GHz		-123					dBc/Hz
	1.2 MHz			-131					
	1.8 MHz			-135					
	6.0 MHz			-148					
Frequency Offset	600 kHz	f_{vco} = 7.5 GHz, CP=5, f_{PFD} = 468.75 MHz, measured at output frequency = 1.8 GHz					-124		
	1.2 MHz						-132		
	1.8 MHz						-136		
	6.0 MHz						-148		

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7.9 Timing Requirements

			MIN	NOM	MAX	UNIT
Digital Input Timing Specifications						
Timing: SYSREF+/-						
$t_{s(SYSREF)}$	Setup time, SYSREF+/- valid to rising edge of DACCLK+/-	SYSREF Capture assist disabled		50		ps
$t_{h(SYSREF)}$	Hold time, SYSREF+/- valid after rising edge of DACCLK+/-	SYSREF Capture assist disabled		50		ps
Timing: Serial Port						
$t_{s(/SDEN)}$	Setup time, $\overline{SDEN}$ to rising edge of SCLK			20		ns
$t_{s(SDIO)}$	Setup time, SDIO valid to rising edge of SCLK			10		ns
$t_{h(SDIO)}$	Hold time, SDIO valid after rising edge of SCLK			5		ns
$t_{(SCLK)}$	Period of SCLK	temperature sensor read		1		µs
		All other registers		100		ns
$t_{d(Data)}$	Data output delay after falling edge of SCLK			25		ns
t_{RESET}	Minimum $\overline{RESET}$ pulse width			25		ns
Analog Output						
$t_{s(DAC)}$	Output settling time to 0.1%			1		ns
t_r	Output rise time 10% to 90%			50		ps
t_f	Output fall time 90% to 10%			50		ps
Latency						
	RX SerDes AnalogDelay			250		ps
	DAC wake-up time	I_{OUT} current settling to 1% of I_{OUTFS} from deep sleep		90		µs
	DAC sleep time	I_{OUT} current settling to less than 1% of I_{OUTFS} in deep sleep		90		µs

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7.10 Typical Characteristics

Unless otherwise noted, all plots are at T_A = 25°C, nominal supply voltages, f_{DAC} = 8847.36MSPS, 12x interpolation, 0dBFS digital input, 40 mA full scale output current , LMFSHd = 84111 and PLL is disabled.

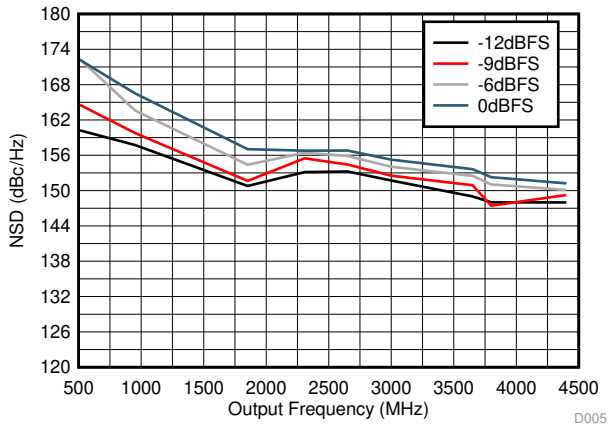

Figure 1. NSD vs Output Frequency Over Input Scale

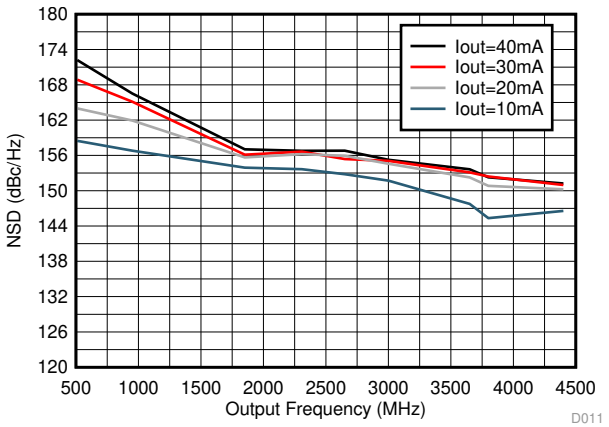

Figure 2. NSD vs Output Frequency Over Output Current $I_{out}FS$

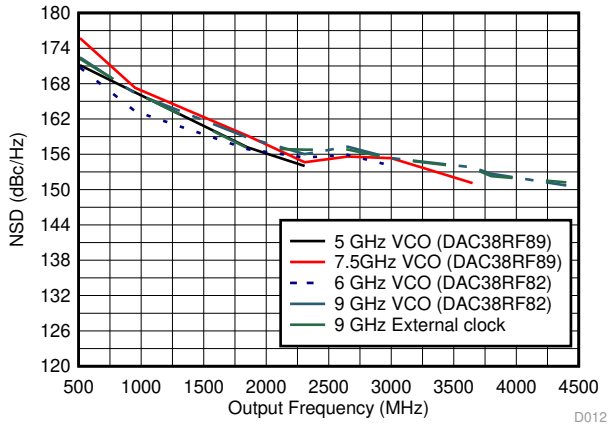

Figure 3. NSD vs Output Frequency Over Clocking Option

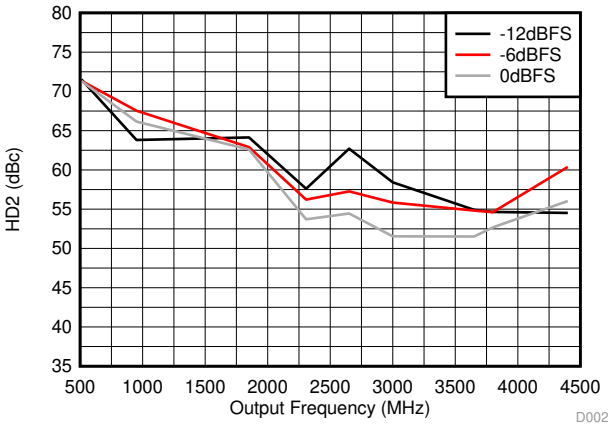

Figure 4. HD2 vs Output Frequency Over Input Scale

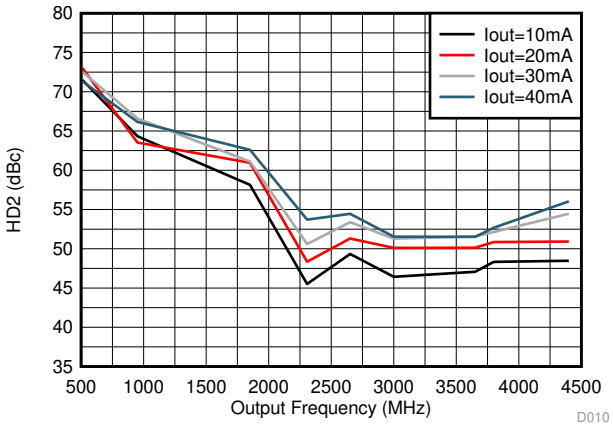

Figure 5. HD2 vs Output Frequency Over Output Current $I_{out}FS$

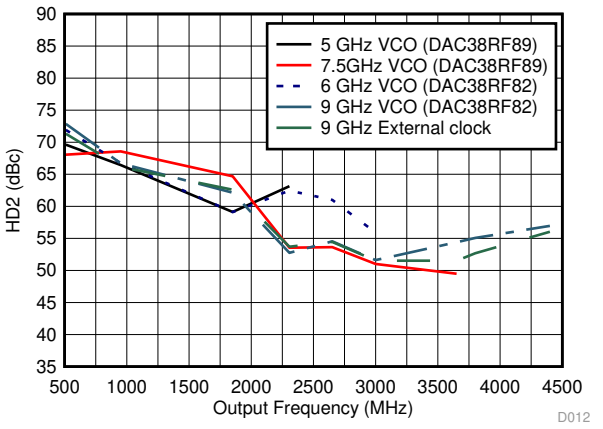

Figure 6. HD2 vs Output Frequency Over Clocking Option

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Typical Characteristics (continued)

Unless otherwise noted, all plots are at T_A = 25°C, nominal supply voltages, f_{DAC} = 8847.36MSPS, 12x interpolation, 0dBFS digital input, 40 mA full scale output current , LMFSHd = 84111 and PLL is disabled.

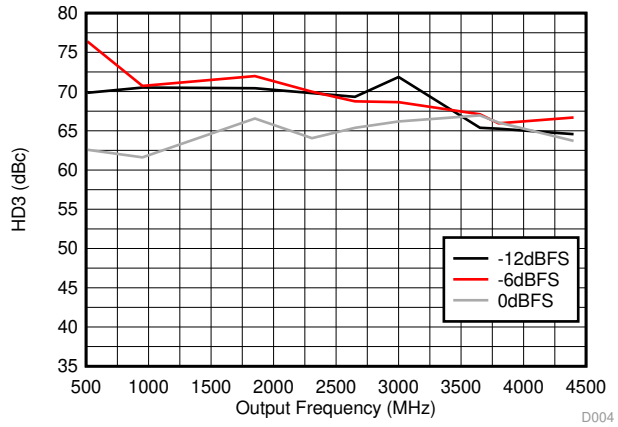

Figure 7. HD3 vs Output Frequency Over Input Scale

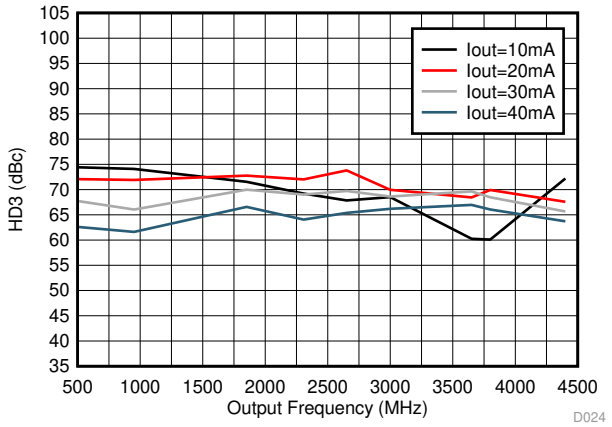

Figure 8. HD3 vs Output Frequency Over Output Current $I_{out}FS$

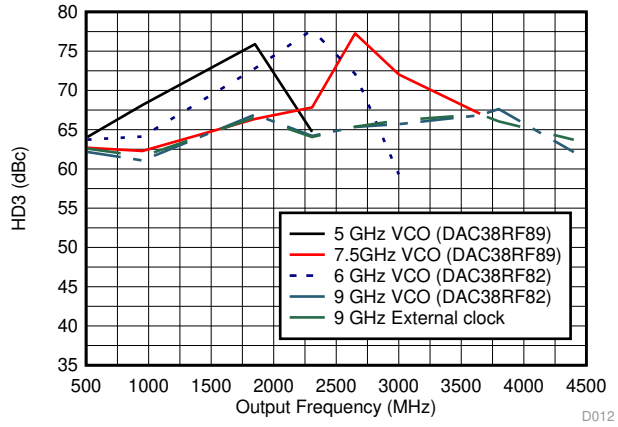

Figure 9. HD3 vs Output Frequency Over Clocking Option

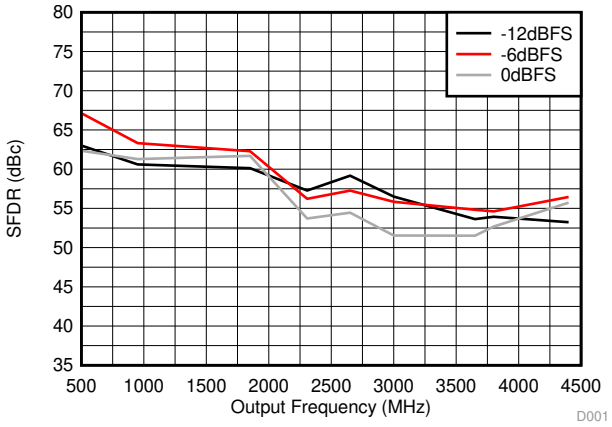

Figure 10. SFDR vs Output Frequency Over Input Scale

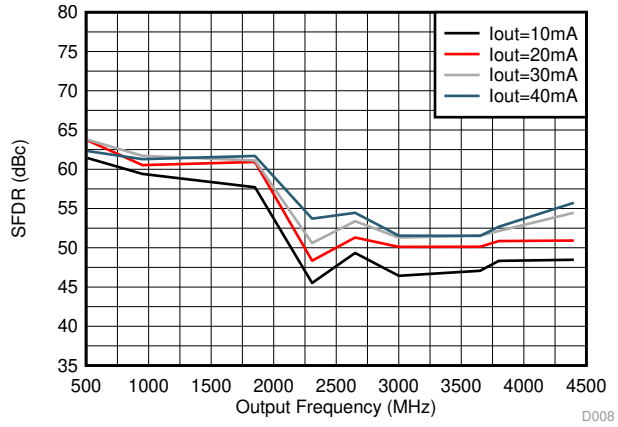

Figure 11. SFDR vs Output Frequency Over Output Current $I_{out}FS$

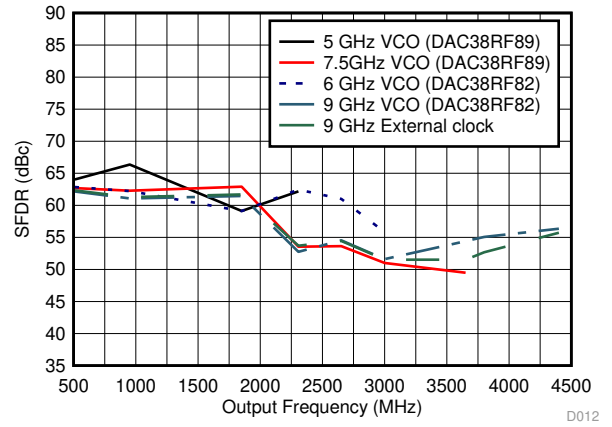

Figure 12. SFDR vs Output Frequency Over Clocking Option

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Typical Characteristics (continued)

Unless otherwise noted, all plots are at T_A = 25°C, nominal supply voltages, f_{DAC} = 8847.36MSPS, 12x interpolation, 0dBFS digital input, 40 mA full scale output current , LMFSHd = 84111 and PLL is disabled.

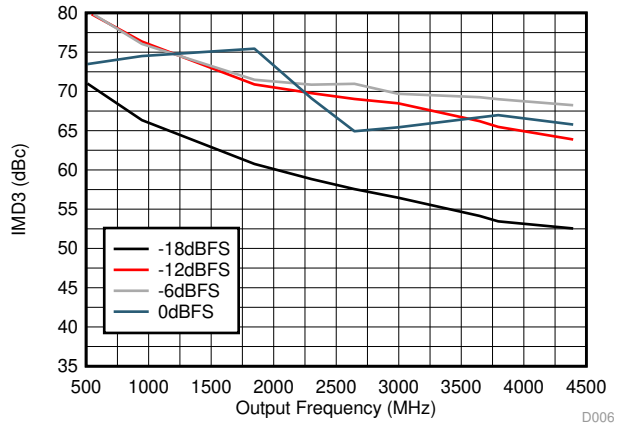
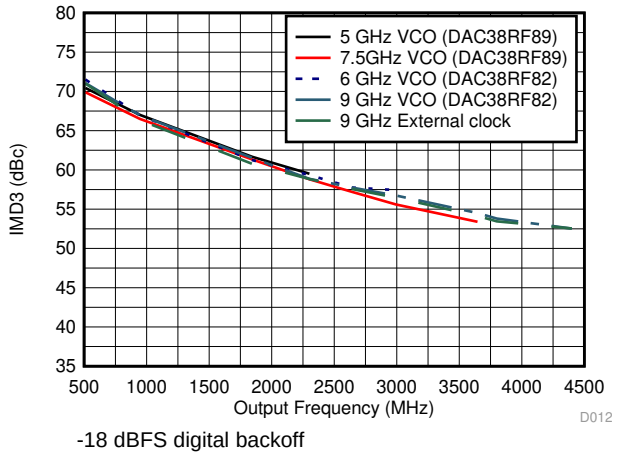


Figure 13. IMD3 vs Output Frequency Over Input Scale



-18 dBFS digital backoff

Figure 14. IMD3 vs Output Frequency Over Clocking Option

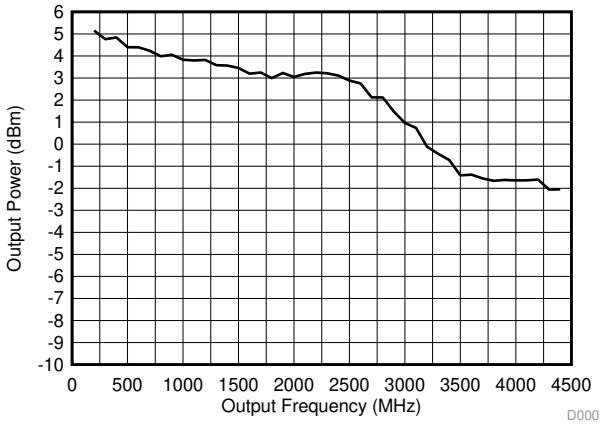


Figure 15. Power vs Output Frequency

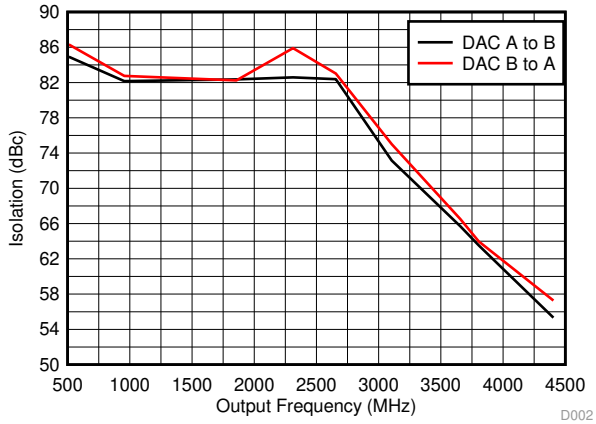
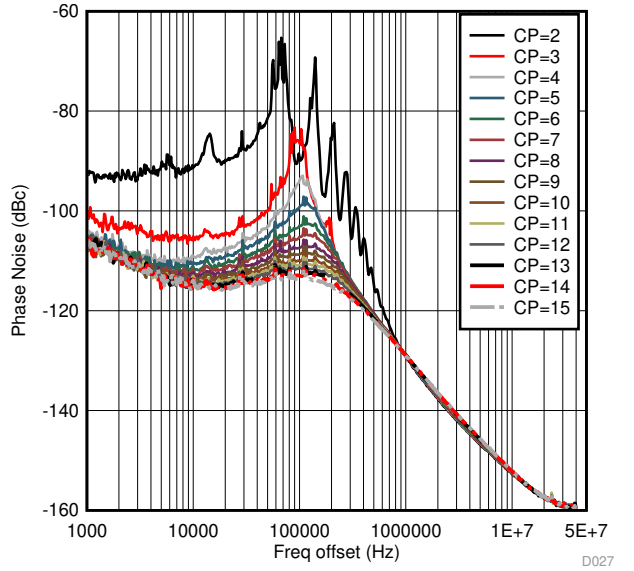


Figure 16. Isolation vs Output Frequency

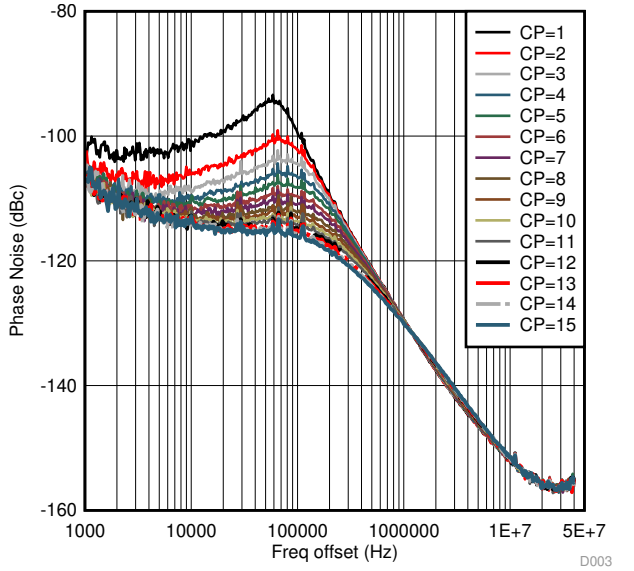
Typical Characteristics (continued)

Unless otherwise noted, all plots are at T_A = 25°C, nominal supply voltages, f_{DAC} = 8847.36MSPS, 12x interpolation, 0dBFS digital input, 40 mA full scale output current , LMFSHd = 84111 and PLL is disabled.



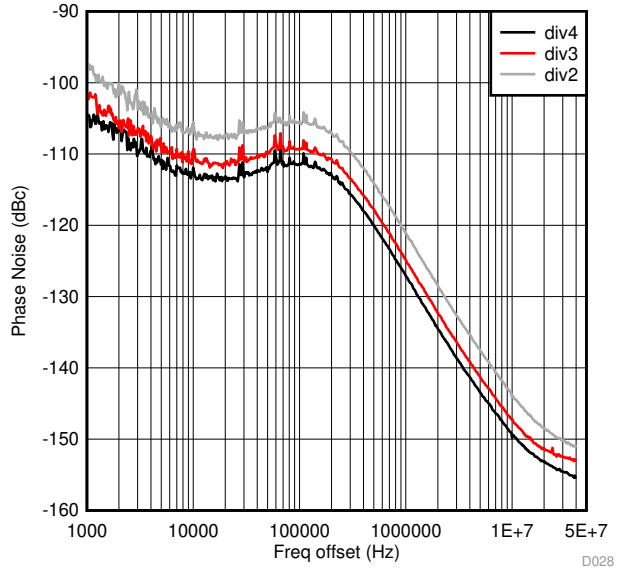
VCO frequency = 8.85 GHz Measured at 1.8 GHz

Figure 17. DAC38RF82 VCO1 Phase Noise vs Offset Frequency Over Charge pump current



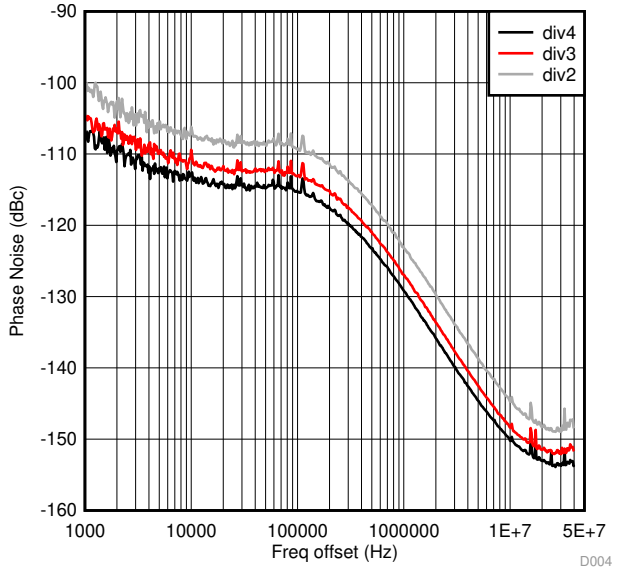
VCO frequency = 7.5 GHz Measured at 1.8 GHz

Figure 18. DAC38RF89 VCO1 Phase Noise vs Offset Frequency Over Charge pump current



VCO frequency = 8.85 GHz

Figure 19. DAC38RF82 VCO1 Output Clock Phase Noise vs Offset frequency Over Divider Ratio



VCO frequency = 7.5 GHz

Figure 20. DAC38RF89 VCO1 Output Clock Phase Noise vs Offset frequency Over Divider Ratio

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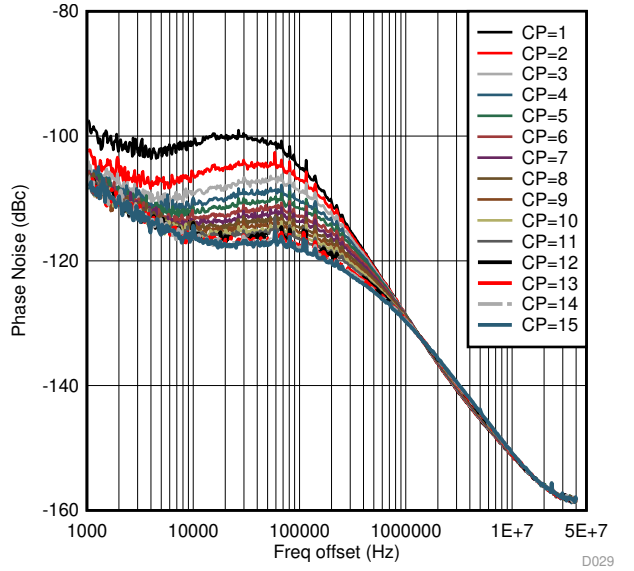
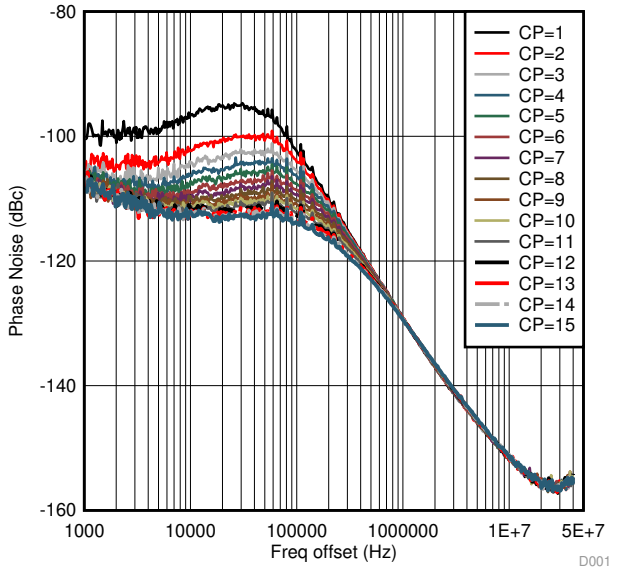
Typical Characteristics (continued)

Unless otherwise noted, all plots are at T_A = 25°C, nominal supply voltages, f_{DAC} = 8847.36MSPS, 12x interpolation, 0dBFS digital input, 40 mA full scale output current , LMFSHd = 84111 and PLL is disabled.



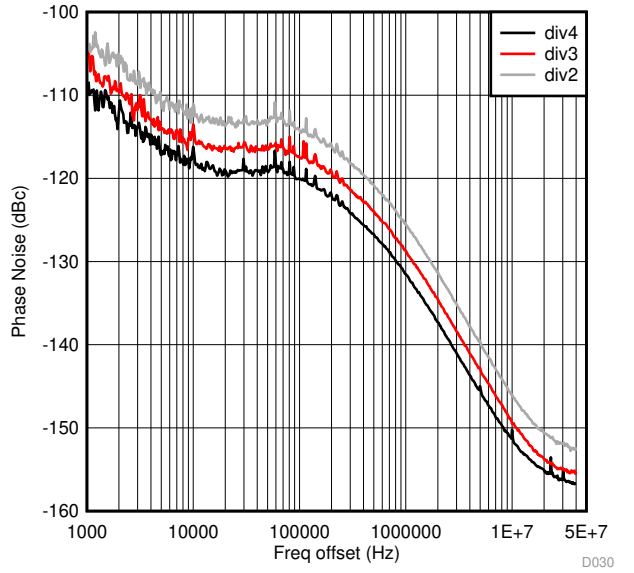
VCO frequency = 5.9 GHz Measured at 1.8 GHz

Figure 21. DAC38RF82 VCO0 Phase Noise vs Offset Frequency Over Charge Pump Current



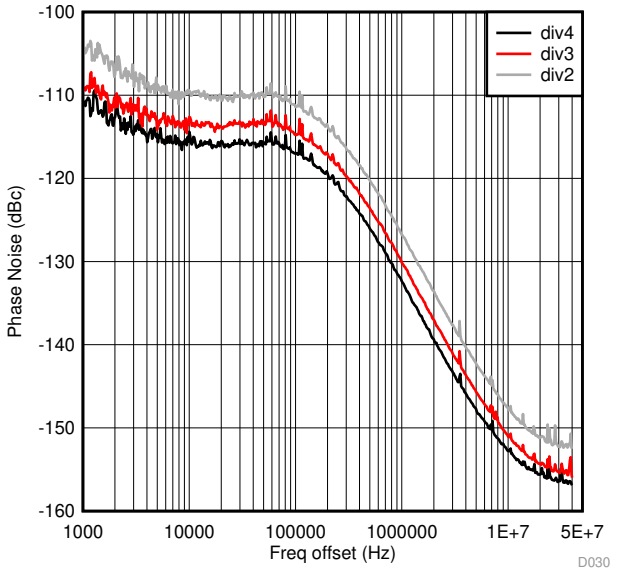
VCO frequency = 5.0 GHz Measured at 1.8 GHz

Figure 22. DAC38RF89 VCO0 Phase Noise vs Offset Frequency Over Charge Pump Current



VCO frequency = 5.9 GHz

Figure 23. DAC38RF82 VCO0 Output clock Phase Noise vs Offset Frequency Over Divider Ratio



VCO frequency = 5.0 GHz

Figure 24. DAC38RF89 VCO0 Output clock Phase Noise vs Offset Frequency Over Divider Ratio

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8 Detailed Description

8.1 Overview

The DAC38RF82 and DAC38RF89 are high performance, wide bandwidth RF-sampling digital-to-analog (DACs) that are capable of dual channel input data rate up to 3.33 GSPS or single-channel operation with 8-bits up to 9-GSPS. The devices have a low power JESD204B Interface with up to 8 lanes, with a maximum bit rate of 12.5 Gbps. In dual channel operation, the input interface is capable of data rates up to 3.33 GSPS at 12-bits and 2.5 GSPS at 16-bits resolution without interpolation. When used as a complex baseband transmitter with interpolation modes from 2x to 24x, the DAC38RF82 (or DAC38RF89) is capable of synthesizing wideband signals up to 2 GHz bandwidth with 16-bit input resolution and 2.66 GHz bandwidth with 12-bit input resolution. The 8-bit mode allows an input at the full 9 GSPS maximum DAC sample rate and can synthesize wideband signals from 0 to 4.5 GHz. An optional low jitter PLL/VCO simplifies the DAC clock generation by allowing use of a lower frequency reference clock. DAC38RF82 and DAC38RF89 support different VCO frequency ranges, summarized in Device Comparison Table.

8.2 Functional Block Diagrams

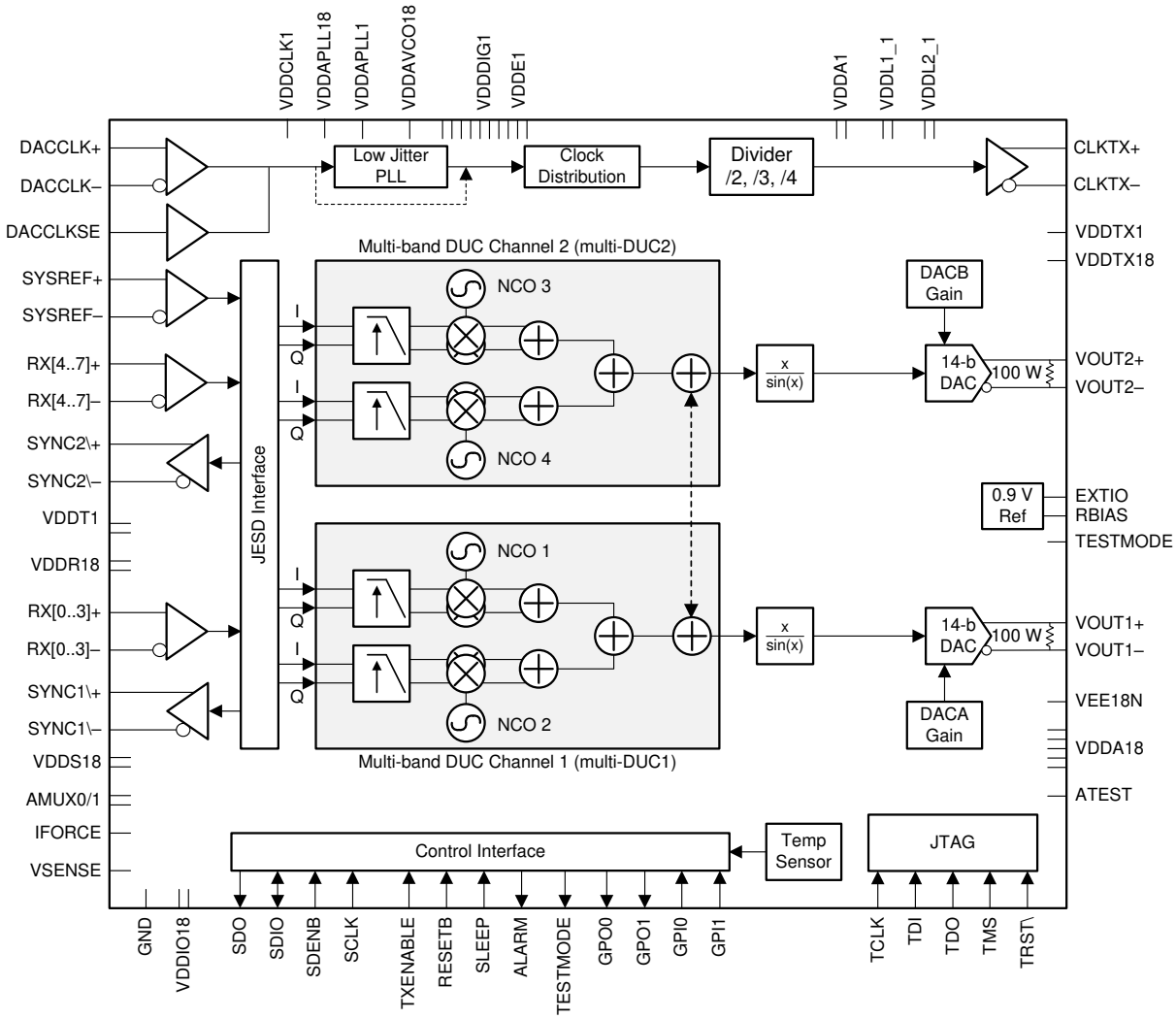

Figure 25. 12-, 16-Bit Input Mode Block Diagram

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Functional Block Diagrams (continued)

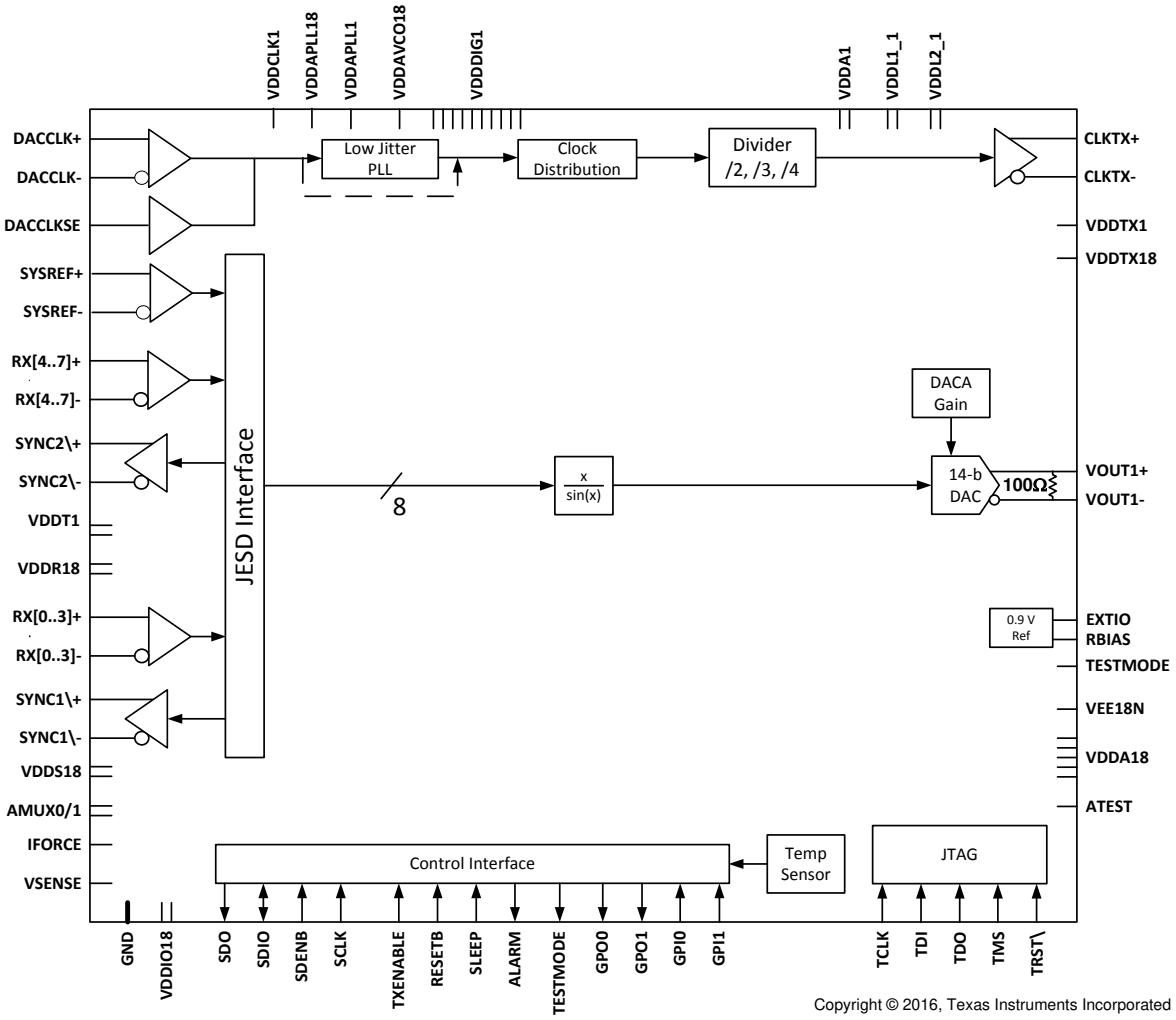

Figure 26. 8-Bit Input Mode Block Diagram

8.3 Feature Description

8.3.1 SerDes Inputs

The DAC38RF82 (or DAC38RF89) RX [0..7]+/- differential inputs are each internally terminated to a common point via 50 Ω, as shown in Figure 27.

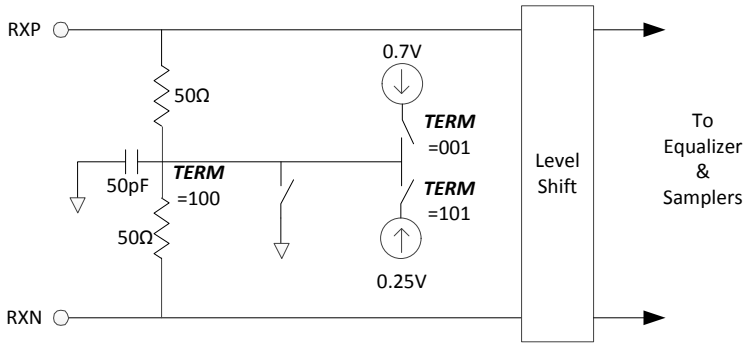

Figure 27. Serial Lane Input Termination

Common mode termination is via a 50 pF capacitor to GND. The common mode voltage and termination of the differential signal can be controlled in a number of ways to suit a variety of applications via field TERM in register SRDS_CFG2 (8.5.87), as described in Table 1.

NOTE

AC coupling is recommended for JESD204B compliance.

Table 1. Receiver Termination Selection

TERM	EFFECT
000	Reserved
001	Common point set to 0.7 V. This configuration is for AC coupled systems. The transmitter has no effect on the receiver common mode, which is set to optimize the input sensitivity of the receiver. Note: this mode is not compatible with JESD204B.
01x	Reserved
100	Common point set to GND. This configuration is for applications that require a 0 V common mode.
101	Common point set to 0.25 V. This configuration is for applications that require a low common mode.
110	Reserved
111	Common point floating. This configuration is for DC coupled systems in which the common mode voltage is set by the attached transmit link partner to 0 and 0.6 V. Note: this mode is not compatible with JESD204B

Input data is sampled by the differential sensing amplifier using clocks derived from the clock recovery algorithm. The polarity of RX+ and RX- can be inverted by setting the bit of the corresponding lane in field INVPAIR in register SRDS_POL (8.5.88) to “1”. This can potentially simplify PCB layout and improve signal integrity by avoiding the need to swap over the differential signal traces.

Due to processing effects, the devices in the RX+ and RX- differential sense amplifiers will not be perfectly matched and there will be some offset in switching threshold. The DAC38RF82 (or DAC38RF89) contains circuitry to detect and correct for this offset. This feature can be enabled by setting ENOC in register SRDS_CFG1 (8.5.86) to “1”. It is anticipated that most users will enable this feature.

8.3.2 SerDes Rate

The DAC38RF82 (or DAC38RF89) has eight configurable JESD204B serial lanes. The highest speed of each SerDes lane is 12.5 Gbps. Because the primary operating frequency of the SerDes is determined by its reference clock and PLL multiplication factor, there is a limit on the lowest SerDes rate supported. To support lower speed application, each receiver should be configured to operate at half, quarter or eighth of the full rate via field RATE in register SRDS_CFG2 (8.5.87). Refer to Table 2 for details.

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Table 2. Lane Rate Selection

RATE	EFFECT
00	Full rate. Four data samples taken per SerDes PLL output clock cycle.
01	Half rate. Two data samples taken per SerDes PLL output clock cycle.
10	Quarter rate. One data samples taken per SerDes PLL output clock cycle.
11	Eighth rate. One data samples taken every two SerDes PLL output clock cycles.

8.3.3 SerDes PLL

The DAC38RF82 (or DAC38RF89) has two integrated PLLs, one PLL is to provide the clocking of DAC, refer to the *DAC PLL* section; the other PLL is to provide the clocking for the high speed SerDes. The reference frequency of the SerDes PLL can be in the range of 100-800 MHz nominal, and 300-800 MHz optimal. The reference frequency is derived from DACCLK divided down by the value in field SerDes_REFCLK_DIV in register SRDS_CLK_CFG (8.5.84), as shown in Figure 28. Field SerDes_CLK_SEL in register SRDS_CLK_CFG (8.5.84) determines if the DACCLK input or DAC PLL output is used as the source of the SerDes PLL reference. If the DACCLK input is used, a pre-divider set by field SerDes_REFCLK_PREDIV in register SRDS_CLK_CFG (8.5.84) should be used to reduce the frequency of the DACCLK.

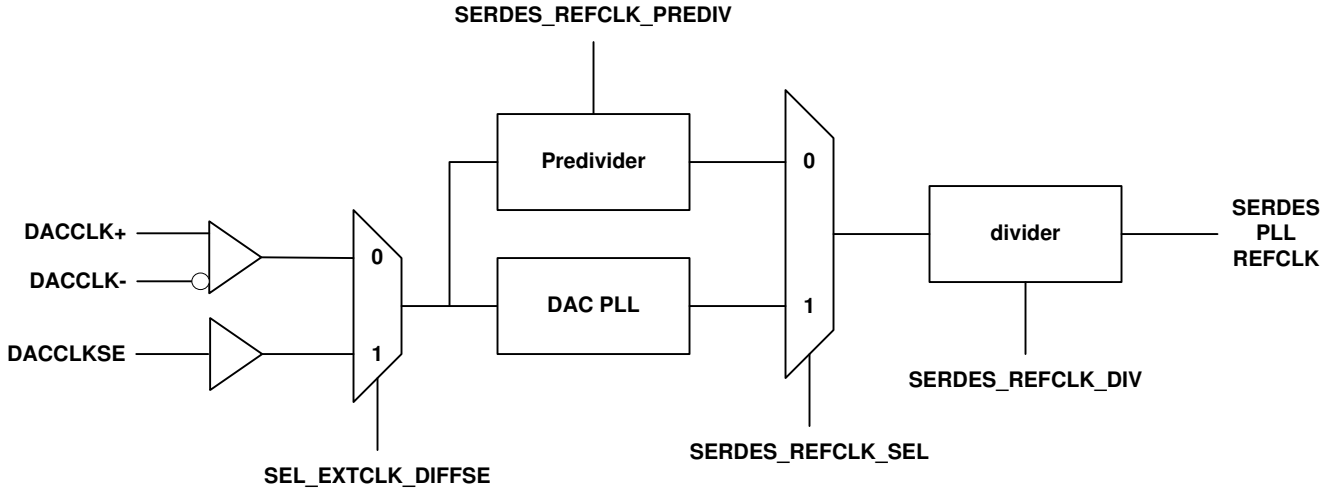

Figure 28. Reference Clock of SerDes PLL

During normal operation, the clock generated by PLL is 4-25 times the reference frequency, according to the multiply factor selected via the field MPY] in register SRDS_PLL_CFG (8.5.85). In order to select the appropriate multiply factor and reference clock frequency, it is first necessary to determine the required PLL output clock frequency. The relationship between the PLL output clock frequency and the lane rate is determined by field RATE in register SRDS_CFG2 (8.5.87) is shown in Table 3. Having computed the PLL output frequency, the reference frequency can be obtained by dividing this by the multiply factor specified via MPY.

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Table 3. Relationship Between Lane Rate and SerDes PLL Output Frequency

RATE	LINE RATE	PLL OUTPUT FREQUENCY
00	x Gbps	0.25x GHz
01	x Gbps	0.5x GHz
10	x Gbps	1x GHz
11	x Gbps	2x GHz

Table 4. SerDes PLL Multiplier (MPY) Values

MPY	EFFECT
0x10	4x
0x14	5x
0x18	6x
0x20	8x
0x21	8.25x
0x28	10x
0x30	12x
0x32	12.5x
0x3C	15x
0x40	16x
0x42	16.5x
0x50	20x
0x58	22x
0x64	25x
Other codes	Reserved

The wide range of multiply factors combined with the different rate modes means it is often possible to achieve a given line rate from multiple different reference frequencies. The configuration which utilizes the highest reference frequency achievable is always preferable.

The SerDes PLL VCO must be in the nominal range of 1.5625 - 3.125 GHz. It is necessary to adjust the loop filter depending on the operating frequency of the VCO. If the PLL output frequency is below 2.17 GHz, VRANGE in register SRDS_PLL_CFG (8.5.84) should be set high.

Performance of the integrated PLL can be optimized according to the jitter characteristics of the reference clock by setting the appropriate loop bandwidth via field LB in register SRDS_PLL_CFG (8.5.84). The loop bandwidth is obtained by dividing the reference frequency by BWSCALE, where the BWSCALE is a function of both LB and PLL output frequency as shown in Table 5.

Table 5. SerDes PLL Loop Bandwidth Selection

LB	EFFECT	BWSCALE vs PLL OUTPUT FREQUENCY		
		3.125 GHz	2.17 GHz	1.5625 GHz
00	Medium loop bandwidth	13	14	16
01	Ultra high loop bandwidth	7	8	8
10	Low loop bandwidth	21	23	30
11	High loop bandwidth	10	11	14

An approximate loop bandwidth of 8 – 30 MHz is suitable and recommended for most systems where the reference clock is via low jitter clock input buffer. For systems where the reference clock is via a low jitter input cell, but of low quality, an approximate loop bandwidth of less than 8 MHz may offer better performance. For systems where the reference clock is cleaned via an ultra-low jitter LC-based cleaner PLL, a high loop bandwidth up to 60 MHz is more appropriate. Note that the use of ultra-high loop bandwidth setting is not recommended for PLL multiply factor of less than 8.

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A free running clock output is available when field ENDIVCLK in register SRDS_PLL_CFG (8.5.85) is set high. It runs at a fixed divided-by-80 of the PLL output frequency and can be output on the ALARM pin by setting field DTEST to “0001” (lanes 0 – 3) or “0010” (lanes 4 – 7) in register DTEST (8.5.76).

8.3.4 SerDes Equalizer

All channels of the DAC38RF82 (or DAC38RF89) incorporate an adaptive equalizer, which can compensate for channel insertion loss by attenuating the low frequency components with respect to the high frequency components of the signal, thereby reducing inter-symbol interference. Figure 29 shows the response of the equalizer, which can be expressed in terms of the amount of low frequency gain and the frequency up to which this gain is applied (i.e., the frequency of the ’zero’). Above the zero frequency, the gain increases at 6 dB/octave until it reaches the high frequency gain.

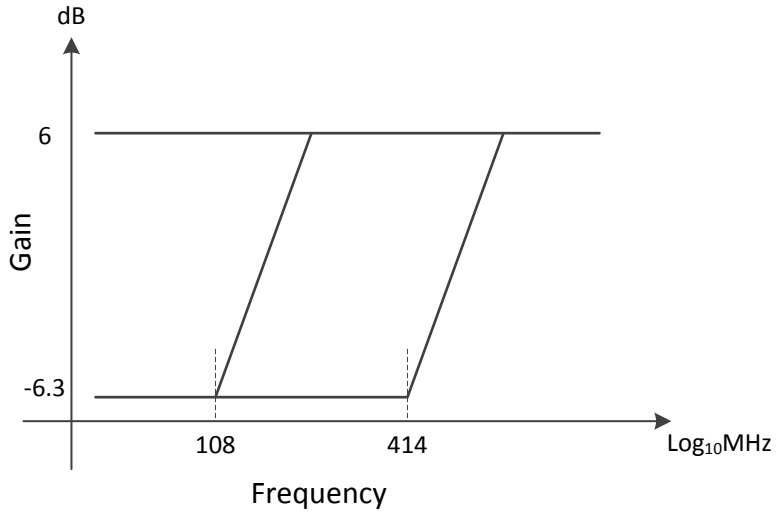

Figure 29. Equalizer Frequency Response

The equalizer can be configured via fields EQ and EQHLD in register SRDS_CFG1 (8.5.86). Table 6 and Table 7 summarize the options. When enabled, the receiver equalization logic analyzes data patterns and transition times to determine whether the low frequency gain should be increased or decreased. The decision logic is implemented as a voting algorithm with a relatively long analysis interval. The slow time constant that results reduces the probability of incorrect decisions but allows the equalizer to compensate for the relatively stable response of the channel. The lock time for the adaptive equalizer is data dependent, and so it is not possible to specify a generally applicable absolute limit. However, assuming random data, the maximum lock time will be 6x106 divided by the CDR activity level. For field CDR in register SRDS_CFG1 (8.5.86) = 110, the activity level is 1.5 x 10^6 UI.

When EQ[2] = 0, finer control of gain boost is available using the EQBOOST IEEE1500 tuning chain field, as shown in Table 6.

Table 6. Receiver Equalization Configuration

EQ		EFFECT
[1-0]	00	No equalization. The equalizer provides a flat response at the maximum gain. This setting may be appropriate if jitter at the receiver occurs predominantly as a result of crosstalk rather than frequency dependent loss.
	01	Fully adaptive equalization. The zero position is determined by the selected operating rate, and the low frequency gain of the equalizer is determined algorithmically by analyzing the data patterns and transition positions in the received data. This setting should be used for most applications.
	10	Precursor equalization analysis. The data patterns and transition positions in the received data are analyzed to determine whether the transmit link partner is applying more or less precursor equalization than necessary.
	11	Postcursor equalization analysis. The data patterns and transition positions in the received data are analyzed to determine whether the transmit link partner is applying more or less post-cursor equalization than necessary.

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Table 6. Receiver Equalization Configuration (continued)

EQ		EFFECT
[2]	0	Default
	1	Boost. Equalizer gain boosted by 6 dB, with a 20% reduction in bandwidth, and an increase of 5mW power consumption. May improve performance over long links.

Table 7. Receiver Equalizer Hold

EQHOLD	EFFECT
0	Equalizer adaption enabled. The equalizer adaption and analysis algorithm is enabled. This should be the default state.
1	Equalizer adaption held. The equalizer is held in its current state. Additionally, the adaption and analysis algorithm is reset.

Table 8. Relationship Between Lane Rate and SerDes PLL Output Frequency

EQBOOST	GAIN BOOST (dB)	BANDWIDTH CHANGE (%)	POWER INCREASE (mW)
00	0	0	0
01	2	-30	0
01	4	10	5
11	6	-20	5

When EQ is set to 010 or 011, the equalizer is reconfigured to provide analytical data about the amount of pre and post cursor equalization respectively present in the received signal. This can in turn be used to adjust the equalization settings of the transmitting link partner, where a suitable mechanism for communicating this data back to the transmitter exists. Status information is provided by setting field DTEST in register DTEST (8.5.76) to “0111” for EQOVER and “0110” for EQUNDER. The procedure is as follows:

1. Enable the equalizer by setting fields EQHLD low and EQ to “001” (register SRDS_CFG1 8.5.86). Allow sufficient time for the equalizer to adapt;
2. Set EQHLD to 1 to lock the equalizer and reset the adaption algorithm. This also causes both EQOVER and EQUNDER to become low;
3. Wait at least 48 UI, and proportionately longer if the CDR activity is less than 100%, to ensure the 1 on EQHLD is sampled and acted upon;
4. Set EQ to “010” or “011”, and EQHLD to 0. The equalization characteristics of the received signal are analysed (the equalizer response will continue to be locked);
5. Wait at least 150×103 UI to allow time for the analysis to occur, proportionately longer if the CDR activity is less than 100%;
6. Examine EQOVER and EQUNDER for results of analysis
   - If EQOVER is high, it indicates the signal is over equalized;
   - If EQUNDER is high, it indicates the signal is under equalized;
7. Set EQHLD to 1;
8. Repeat items 3–7 if required;
9. Set EQ to “001”, and EQHLD to 0 to exit analysis mode and return to normal adaptive equalization.

NOTE

When changing EQ from one non-zero value to another, EQHLD must already be 1. If this is not the case, there is a chance the equalizer could be reset by a transitory input state (i.e., if EQ is momentarily 000). EQHLD can be set to 0 at the same time as EQ is changed.

As the equalizer adaption algorithm is designed to equalize the post cursor, EQOVER or EQUNDER will only be set during post cursor analysis if the amount of post cursor equalization required is more or less than the adaptive equalizer can provide.

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8.3.5 JESD204B Descrambler

The descrambler is a 16-bit parallel self-synchronous descrambler based on the polynomial 1 + x14 + x15. From the JESD204B specification, the scrambling/descrambling process only occurs on the user data, not on the code group synchronization or the ILA sequence. Each multi-DUC has a separate descrambler that can be enabled independently. The descrambler is enabled by field SCR in the multi-DUC paged register JESD_N_HD_SCR (8.5.49).

8.3.6 JESD204B Frame Assembly

The DAC38RF82 (or DAC38RF89) may be programmed as a single or dual DAC device, with one JESD RX block designated for each DAC. The two JESD RX blocks can be programmed to operate as two separate links or as a single link.

The JESD204B defines the following parameters:

- L is the number of lanes
- M is the number of I or Q streams per device (2 = 1 IQ pair, 4 = 2 IQ pairs, 8 = 4 IQ pairs)
- F is the number of octets per frame clock period
- S is the number of samples per frame
- HD is the High-Density bit which controls whether a sample may be divided over more lanes
- N = NPRIME is the number of bits per sample (12 or 16 - bits)

Fields K and L are found in multi-DUC paged register JESD_K_L (8.5.46), M and S in multi-DUC paged register JESD_M_S (8.5.48), and N, NPRIME and HD in multi-DUC paged register JESD_N_HD_SCR (8.5.49).

Table 9 lists the available JESD204B formats, interpolation rates and sample rate limits for the DAC38RF82 (or DAC38RF89). The ranges are limited by the SerDes PLL VCO frequency range, the SerDes PLL reference clock range, the maximum SerDes line rate, and the maximum DAC sample frequency. Table 10 through Table 27 lists the frame formats for each mode. In the frame format tables, i CH (N) [x:y] and q CH (N) [x:y] are bits x through y of the I and Q samples at time N of DUC channel CH. If [x..y] is not listed, the full sample is assumed. For example, i0(0)[15:8] are bits 15 – 8 of the I sample at time 0, and q(1) is the full Q sample at time 1.

Table 9. JESD204B Formats for DAC38RF82 and DAC38RF89

L-M-F-S-Hd 1 TX	L-M-F-S-Hd 2 TX	Frame Format	Input Resolution	IQ pairs per DAC	Interp	Input rate max (MSPS)	f_{DAC} Max (MSPS)
82121	NA	1 TX: Table 10	16	1	6	1500	9000
			16	1	8	1125	9000
			16	1	12	750	9000
			16	1	16	562.5	9000
42111	84111	1 TX: Table 11 2 TX: Table 12	16	1	6	1250	7500
			16	1	8	1125	9000
			16	1	10	900	9000
			16	1	12	750	9000
			16	1	16	562.5	9000
			16	1	18	500	9000
			16	1	24	375	9000
22210	44210	1 TX: Table 13 2 TX: Table 14	16	1	8	625	5000
			16	1	12	625	7500
			16	1	16	562.5	9000
			16	1	18	500	9000
			16	1	20	450	9000
			16	1	24	375	9000
12410	24410	1 TX: Table 15 2 TX: Table 16	16	1	16	312.5	5000
			16	1	24	312.5	7500

Table 9. JESD204B Formats for DAC38RF82 and DAC38RF89 (continued)

L-M-F-S-Hd 1 TX	L-M-F-S-Hd 2 TX	Frame Format	Input Resolution	IQ pairs per DAC	Interp	Input rate max (MSPS)	f_{DAC} Max (MSPS)
44210	88210	1 TX: Table 17 2 TX: Table 18	16	2	8	625	5000
			16	2	12	625	7500
			16	2	16	562.5	9000
			16	2	24	375	9000
24410	48410	1 TX: Table 19 2 TX: Table 20	16	2	16	312.5	5000
			16	2	24	312.5	7500
24310	48310	1 TX: Table 21 2 TX: Table 22	12	2	24	375	9000
81180	NA	1 TX: Table 23	8	real input	1	9000	9000
41380	82380	1 TX: Table 24 2 TX: Table 25	12	real input (1)	1	3333	3333
					2	3333	6666
41121	82121	1 TX: Table 26 2 TX: Table 27	16	real input (1)	1	2500	2500
					2	2500	5000
					4	2250	9000

(1) Can also be used as I-Q pair per 2 DACs. See description in Wideband DUC (wide-DUC)

Table 10. JESD204B Frame Format for LMFSHd = 82121

# un bits	4	8
# en bits	5	10
Nibble	1	2
lane RX0	i0[15:8]	
lane RX1	i0[7:0]	
lane RX2	i1[15:8]	
lane RX3	i1[7:0]	
lane RX4	q0[15:8]	
lane RX5	q0[7:0]	
lane RX6	q1[15:8]	
lane RX7	q1[7:0]	

Table 11. JESD204B Frame Format for LMFSHd = 42111

# un bits	4	8
# en bits	5	10
Nibble	1	2
lane RX0	i0[15:8]	
lane RX1	i0[7:0]	
lane RX2	q0[15:8]	
lane RX3	q0[7:0]	

Table 12. JESD204B Frame Format for LMFSHd = 84111

# un bits	4	8
# en bits	5	10
Nibble	1	2
lane RX0	A-i0[15:8] (1)	
lane RX1	A-i0[7:0] (2)	

(1) DAC A, I sample 0, MSB byte
(2) DAC A, I sample 0, LSB byte

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Table 12. JESD204B Frame Format for LMFSHd = 84111 (continued)

lane RX2	A-q0[15:8]
lane RX3	A-q0[7:0]
lane RX4	B-i0[15:8]
lane RX5	B-i0[7:0]
lane RX6	B-q0[15:8]
lane RX7	B-q0[7:0]

Table 13. JESD204B Frame Format for LMFSHd = 22210

# un bits	4	8	12	16
# en bits	5	10	15	20
Nibble	1	2	3	4
lane RX0	i0			
lane RX1	q0			

Table 14. JESD204B Frame Format for LMFSHd = 44210

# un bits	4	8	12	16
# en bits	5	10	15	20
Nibble	1	2	3	4
lane RX0	A-i0 (1)			
lane RX1	A-q0			
lane RX2	B-i0			
lane RX3	B-q0			

(1) DAC A, I sample 0

Table 15. JESD204B Frame Format for LMFSHd = 12410

# un bits	4	8	12	16	20	24	28	32
# en bits	5	10	15	20	25	30	35	40
Nibble	1	2	3	4	5	6	7	8
lane RX0	i0				q0			

Table 16. JESD204B Frame Format for LMFSHd = 24410

# un bits	4	8	12	16	20	24	28	32
# en bits	5	10	15	20	25	30	35	40
Nibble	1	2	3	4	5	6	7	8
lane RX0	A-i0 (1)				A-q0			
lane RX1	B-i0				B-q0			

(1) DAC A, I sample 0

Table 17. JESD204B Frame Format for LMFSHd = 44210

# un bits	4	8	12	16
# en bits	5	10	15	20
Nibble	1	2	3	4
lane RX0	A1-i0 (1)			
lane RX1	A1-q0 (2)			
lane RX2	A2-i0			

(1) DAC A, MultiDUC 1, I sample 0
(2) DAC A, MultiDUC 2, I sample 0

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Table 17. JESD204B Frame Format for LMFSHd = 44210 (continued)

lane RX3	A2-q0

Table 18. JESD204B Frame Format for LMFSHd = 88210

# un bits	4	8	12	16
# en bits	5	10	15	20
Nibble	1	2	3	4
lane RX0	A1-i0 (1)			
lane RX1	A1-q0			
lane RX2	A2-i0			
lane RX3	A2-q0			
lane RX4	B1-i0			
lane RX5	B1-q0			
lane RX6	B2-i0			
lane RX7	B1-q0			

(1) DAC A, MultiDUC 1, I sample 0

Table 19. JESD204B Frame Format for LMFSHd = 24410

# un bits	4	8	12	16	20	24	28	32
# en bits	5	10	15	20	25	30	35	40
Nibble	1	2	3	4	5	6	7	8
lane RX0	A1-i0 (1)				A1-q0			
lane RX1	A2-i0				A2-q0			

(1) DAC A, MultiDUC 1, I sample 0

Table 20. JESD204B Frame Format for LMFSHd = 48410

# un bits	4	8	12	16	20	24	28	32
# en bits	5	10	15	20	25	30	35	40
Nibble	1	2	3	4	5	6	7	8
lane RX0	A1-i0 (1)				A1-q0			
lane RX1	A2-i0				A2-q0			
lane RX2	B1-i0				B1-q0			
lane RX3	B2-i0				B2-q0			

(1) DAC A, MultiDUC 1, I sample 0

Table 21. JESD204B Frame Format for LMFSHd = 24310

# un bits	4	8	12	16	20	24
# en bits	5	10	15	20	25	30
Nibble	1	2	3	4	5	6
lane RX0	A1-i0 (1)			A1-q0		
lane RX1	A2-i0			A2-q0		

(1) DAC A, MultiDUC 1, I sample 0

Table 22. JESD204B Frame Format for LMFSHd = 48310

# un bits	4	8	12	16	20	24
# en bits	5	10	15	20	25	30

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Table 22. JESD204B Frame Format for LMFSHd = 48310 (continued)

Nibble	1	2	3	4	5	6
lane RX0	A1-i0 (1)			A1-q0		
lane RX1	A2-i0			A2-q0		
lane RX2	B1-i0			B1-q0		
lane RX3	B2-i0			B2-q0		

(1) DAC A, MultiDUC 1, I sample 0

Table 23. JESD204B Frame Format for LMFSHd = 81180

# un bits	4	8
# en bits	5	10
Nibble	1	2
lane RX0	A0 (1)	
lane RX1	A1	
lane RX2	A2	
lane RX3	A3	
lane RX4	A4	
lane RX5	A5	
lane RX6	A6	
lane RX7	A7	

(1) DAC A, sample 0

Table 24. JESD204B Frame Format for LMFSHd = 41380

# un bits	4	8	12	16	20	24
# en bits	5	10	15	20	25	30
Nibble	1	2	3	4	5	6
lane 0	A-0 (1)			A-1		
lane 1	A-2			A-3		
lane 2	A-4			A-5		
lane 3	A-6			A-7		

(1) DAC A, sample 0

Table 25. JESD204B Frame Format for LMFSHd = 82380

# un bits	4	8	12	16	20	24
# en bits	5	10	15	20	25	30
Nibble	1	2	3	4	5	6
lane 0	i(0)			i(1)		
lane 1	i(2)			i(3)		
lane 2	i(4)			i(5)		
lane 3	i(6)			i(7)		
lane 4	q(0)			q(1)		
lane 5	q(2)			q(3)		
lane 6	q(4)			q(5)		
lane 7	q(6)			q(7)		

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Table 26. JESD204B Frame Format for LMFSHd = 41121

# un bits	4	8
# en bits	5	10
Nibble	1	2
lane 0	A-0[15:8] (1)	
lane 1	A-0[7:0] (2)	
lane 2	A-1[15:8]	
lane 3	A-1[7:0]	

(1) DAC A, sample 0, MSB byte
(2) DAC A, sample 0, LSB byte

Table 27. JESD204B Frame Format for LMFSHd = 82121

# un bits	4	8
# en bits	5	10
Nibble	1	2
lane RX0	A-0[15:8] (1)	
lane RX1	A-0[7:0] (2)	
lane RX2	A-1[15:8]	
lane RX3	A-1[7:0]	
lane RX4	B-0[15:8]	
lane RX5	B-0[7:0]	
lane RX6	B-1[15:8]	
lane RX7	B-1[7:0]	

(1) DAC A, sample 0, MSB byte
(2) DAC A, sample 0, LSB byte

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8.3.7 $\overline{\text{SYNC}}$ Interface

The DAC38RF82 (or DAC38RF89) JESD204B interface has two differential $\overline{\text{SYNC}}$ outputs called $\overline{\text{SYNC0}}$ and $\overline{\text{SYNC1}}$ to support one or two links. Alternatively, GPO0 and GPO1 can be used to output $\overline{\text{SYNC}}$ as a single-ended CMOS level. Each of the differential or CMOS outputs is enabled by a 2-bit register (fields GPO0_SEL, GPO1_SEL, SYNC0B_SEL, SYNC1B_SEL in register IO_CONFIG 8.5.2), with bit 0 enabling multi-DUC1 $\overline{\text{SYNC}}$ and bit 1 enabling multi-DUC2 $\overline{\text{SYNC}}$. If both are enabled, the SYNC\ signals are OR'ed.

The $\overline{\text{SYNC}}$ signal can be asserted low by the receiver either to make a synchronization request to initialize/reinitialize the link or to report an error to the transmitter. Synchronization requests must have a minimum duration of five frames plus nine octets rounded up to the nearest whole number of frames. To report an error, the $\overline{\text{SYNC}}$ signal is asserted for exactly two frames. The transmitter interprets any negative edge of its $\overline{\text{SYNC}}$ input as an error and any $\overline{\text{SYNC}}$ assertion lasting four frames or longer as a synchronization request. See the following sections in the standard for more details.

- 7.6.3 Errors requiring re-initialization
- 7.6.4 Error reporting via $\overline{\text{SYNC}}$ interface
- 8.4 $\overline{\text{SYNC}}$ signal decoding

8.3.8 Single or Dual Link Configuration

The DAC38RF82 (or DAC38RF89) JESD204B interface can be configures with one or two links. The advantage of using two links, one for each DAC, is that one link can be re-established without affecting the other link and DAC.

The configuration for each mode of operation are:

1. Dual DAC, dual link
   a. Program fields OCTETPATH0_SEL to OCTETPATH7_SEL in multi-DUC paged registers JESD_CROSSBAR1 (8.5.57) and JESD_CROSSBAR2 (8.5.58) so that each multi-DUC will pick data off of the appropriate SerDes lane.
   b. Appropriate bits in field LANE_ENA in multi-DUC paged register JESD_LN_EN (8.5.45) must be set for each multi-DUC enable the lanes used.
   c. Field ONE_DAC_ONLY in register RESET_CONFIG (8.5.1) should be '0' (default).
2. Dual DAC, single link
   a. Program OCTETPATH0_SEL to OCTETPATH7_SEL in multi-DUC paged registers JESD_CROSSBAR1 (8.5.57) and JESD_CROSSBAR2 (8.5.58) so that each multi-DUC will pick data off the appropriate SerDes lane.
   b. Appropriate bits in field LANE_ENA in multi-DUC paged register JESD_LN_EN (8.5.45) must be set for each multi-DUC enable the lanes used.
   c. Set field ONE_LINK_ONLY to '1' to configure TXENABLE output.
3. Single DAC, single link
   a. Set Field ONE_DAC_ONLY in register RESET_CONFIG (8.5.1) to '1' to gate clocks to unused multi-DUC2 for power savings.
   b. ONE_LINK_ONLY bit does not matter in this case.

8.3.9 Multi-Device Synchronization

In many applications, such as multi antenna systems where the various transmit channels information is correlated, it is required that the latency across the link is deterministic and multiple DAC devices are completely synchronized such that their outputs are phase aligned. The DAC38RF82 (or DAC38RF89) achieves the deterministic latency using SYSREF (JESD204B Subclass 1).

SYSREF is generated from the same clock domain as DACCLK. After having resynchronized its local multiframe clock (LMFC) to SYSREF, the DAC will request a link re-initialization via SYNC interface. Processing of the signal on the SYSREF input can be enabled and disabled via the SPI interface.

The SYSREF capture circuit and the timing requirements relative to device clock are described in *SYSREF Capture Circuit*.

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8.3.10 SYSREF Capture Circuit

The JESD204B standard for Device Subclass 1 introduces a SYSREF signal that can be used as a global timing reference to align the phase of the internal local multiframe clock (LMFC) and frame clock across multiple devices. This allows the system to achieve deterministic latency and align data samples across several data converters. The SYSREF signal accomplishes this goal by identifying a device clock edge for each chip that can be used as an alignment reference. In particular, the LMFC and frame clock align to the device clock edge upon which the SYSREF transition from “0” to “1” is sampled. SYSREF may be periodic, one-shot, or “gapped” periodic and its period must be a multiple of the LMFC period.

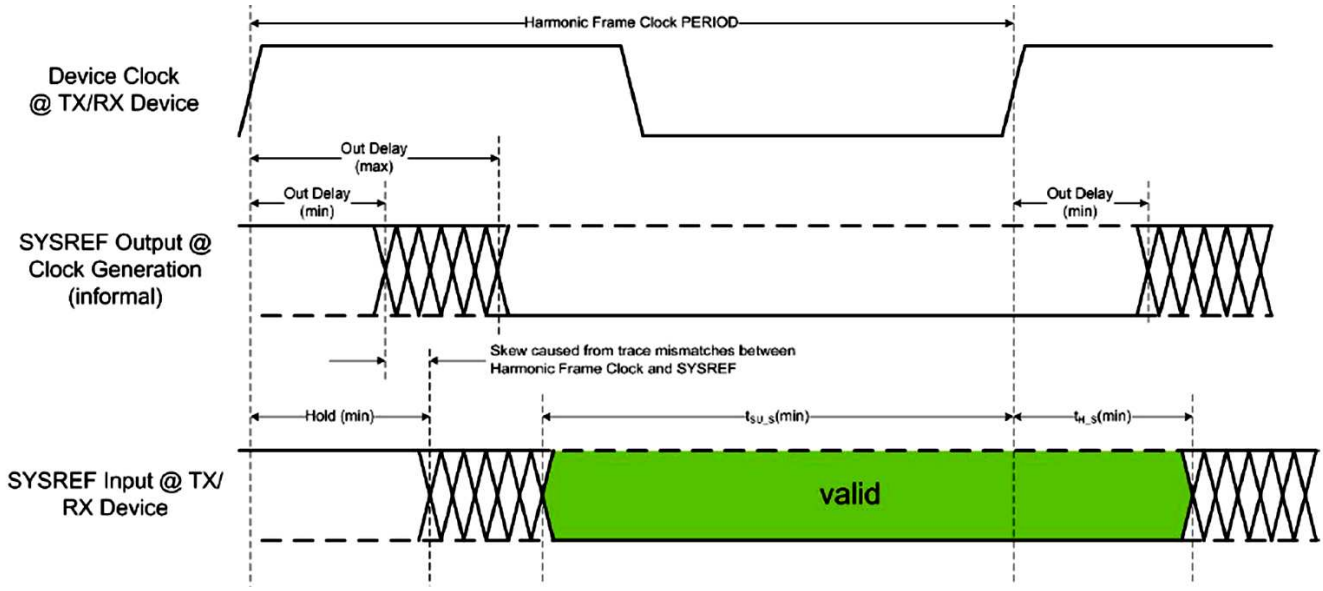

Figure 30. SYSREF Signal Timing

With high-speed device clocks, the phase of the SYSREF signals relative to the device clock must meet the setup/hold time requirements of each individual device clock. Historically, this has been done by controlling the board-level routing delay and/or employing commercial clock distribution capable of generating device clocks and SYSREF signals with programmable delays and with the option of splitting SYSREF into multiple SYSREFS, each with its own fine-tuned delay. Since the DAC38RF82 (or DAC38RF89) supports device clock frequencies up to 9 GHz, a SYSREF capture circuit is includes in the DAC38RF82 (or DAC38RF89) that allows a relaxation in meeting the device clock setup and hold.

The SYSREF capture circuit provides:

- tolerance to manufacturing and environmental variations in SYSREF phase
- immunity to sampling errors due to setup/hold/meta-stability
- information about phase of SYSREF relative to DAC clock inside the data converter
- software compensation for phase misalignment due to PCB design errors

The concepts behind the SYSREF capture scheme are illustrated in Figure 31.

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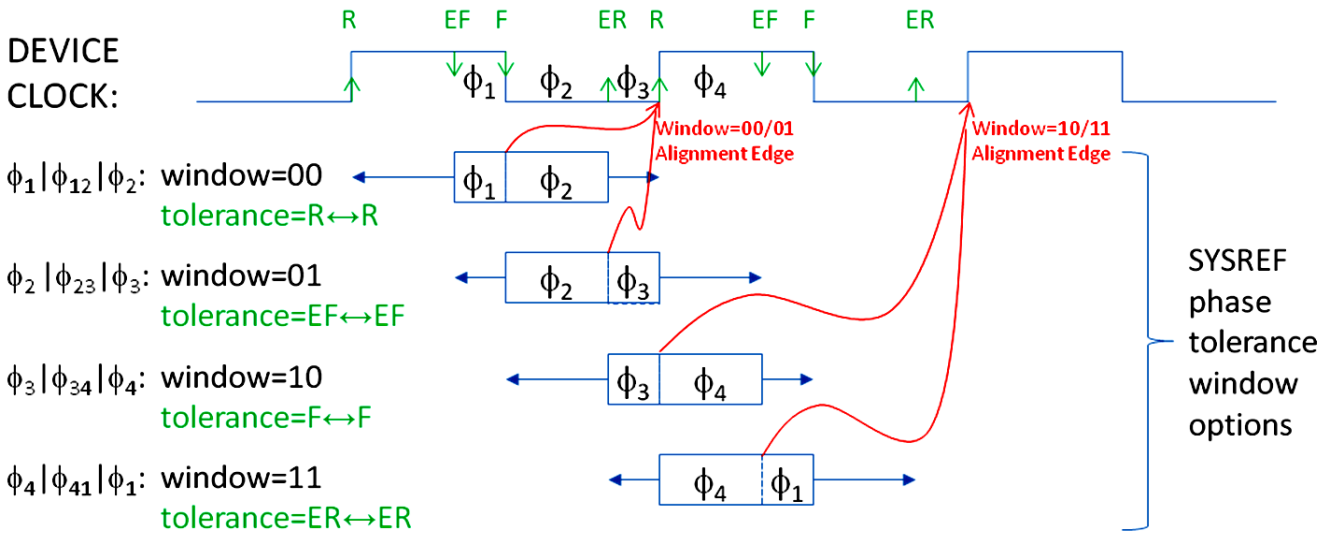

Figure 31. SYSREF Capture Strategy and Phase Tolerance Windows

To understand Figure 31, to begin with we'll ignore the SYSREF phase tolerance windows in the lower portion of the figure and focus on the blue clock waveform at the top of the figure. This waveform represents the device clock input to a particular DAC chip. The green arrows, labeled "R" and "F", correspond to the rising and falling edges of this clock (ignoring for the moment the additional arrows labeled "ER" and "EF"). While previous devices with lower device clocks captured SYSREF only on the rising edge of the device clock, the new scheme samples SYSREF on the falling edge as well, which provides more flexibility when optimizing the setup and hold time of the SYSREF capture path. Moreover, each time a rising SYSREF edge is captured, the chip remembers the clock phase during which the event occurred, and the system designer can later read back the phase information to observe the SYSREF timing relative to the device clock at the internal capture point. If SYSREF transitions close to the rising or falling clock edge sampling points the capture flop setup and hold time may not be met and the observed phase may be unreliable and subject to meta-stability phenomenon.

To reduce the sensitivity to setup/hold/meta-stability concerns an "early" version of the device clock is generated within the DAC and additional SYSREF samples are taken at the "early falling" and "early rising" edges of the clock (labeled "EF" and "ER", respectively, in Figure 31). The resulting set of four samples is used to narrow down the timing of the rising SYSREF edge to one of four possible clock phases. If the rising SYSREF transition takes place between the "EF" and "F" samples, then SYSREF is said to occur in phase θ1. Similarly, if it takes place between the "F" and "ER" samples, then it is said to occur in phase θ2. If SYSREF transitions between the "ER" and "R" samples, then it is said to occur in phase θ3. And, finally, if the SYSREF rising edge event happens between the "R" and "EF" samples, then it is said to occur in phase θ4. As mentioned before, the chip remembers all observed SYSREF phases and the user can later read them back. Since the delay between "early" and "on time" versions of the clock is intentionally chosen to be larger than the setup/hold/meta-stability window, at most one of the four samples can be affected even when the SYSREF transitions right at one of the four sampling points. Thus, the uncertainty in the observed SYSREF timing is limited to adjacent phases, and with twice as many sampling phases the resolution of the timing information is improved by a factor of two.

Referring to the lower portion of Figure 31, the user can now see how this information regarding the observed SYSREF phases is used to devise a reliable SYSREF capture methodology with a high degree of tolerance to manufacturing and environmental variations in SYSREF phase. Based on the SYSREF phases observed for a particular DAC chip during system characterization, the system designer can select one of four so-called "phase tolerance window" options (denoted "'00", "01", "10", and "11") to maximize immunity to manufacturing and environmental variations. For example, consider the default phase tolerance window labeled "window=00" in the figure. If, during characterization, the system designer observes (by reading back the recorded phase observations) that the rising SYSREF edge nominally occurs in either θ1 or θ2 or both (i.e. θ12) then he would

program that particular DAC chip to use phase tolerance window “00”. This mapping is indicated in the figure with the label “θ1|θ12|θ2: window=00”. Having programmed the device to use window “00”, all future SYSREF events that occur in θ1 or θ2 would trigger the LMFC and frame clock to be aligned using the following rising clock edge as the alignment reference (as indicated by the red arrow pointing to rising clock edge “R” and labeled “Window=00/01 alignment edge”).

The full extent of each phase tolerance window is indicated in the figure using “box and whisker” plots. For the “window=00” example, the “box” portion of the plot indicates that the phase tolerance window is centered on θ12 (to be precise on the boundary between θ1 and θ2) and the “whisker” portion indicates that even if the rising edge of SYSREF occurs as early as the preceding θ4 or as late as the following θ3 it still results in LMFC and frame clock alignment to the same rising clock edge indicated by the red arrow labeled “Window=00/01 alignment edge”. When programmed for phase tolerance window “00”, the DAC chip is tolerant to variations in the SYSREF timing ranging from a rising SYSREF edge that occurs just after one rising edge of clock to just before the next rising edge of the clock. The qualifying phrases “just after” and “just before” are used here to indicate that the SYSREF transition must occur far enough away from the rising edges of the clock to avoid setup/hold violations and prevent the device from concluding that the SYSREF transition has crossed out off the phase tolerance window when in fact it has not. The tolerance range for window “00” is from rising clock edge to rising clock edge and is indicated in the figure by the green text labeled “tolerance = R↔R”.

Following the above example, if characterization reveals SYSREF timing centered on θ23 then phase tolerance window “01” (with tolerance for SYSREF rising edge events from EF to EF) should be chosen. Notice that this option is tolerant even to rising SYSREF edges that occur after the rising device clock edge (i.e. in θ4) and will treat them just as if they had occurred in one of the earlier three phases, aligning to the same rising device clock edge indicated by the red arrow labeled “Window=00/01 Alignment Edge”. This allows the system designer to tolerate PCB design errors and/or environmental and manufacturing variations – achieving his intended alignment without having to make physical changes to the board to adjust the SYSREF timing.

Similarly, if characterization indicates that SYSREF timing is centered on θ34 or θ41 then phase tolerance window “10” or “11” can be selected, resulting in tolerance for “F↔F” or “ER↔ER” SYSREF timing, respectively. Note, however, that in these two cases the alignment reference edge is by default taken to be the subsequent rising edge of the device clock. Since this may not be the desired behavior, the DAC38RF82 (or DAC38RF89) allows the user to program in an optional alignment offset of θ1 if the default offset of 0 does not achieve the desired alignment. This feature is illustrated in Figure 32 where the user can see that by setting the alignment offset to -1, phase tolerance windows “10” and “11” can be made to trigger alignment to the earlier rising device clock edge used by windows “00” and “01”. Alternatively, the window “00” and “01” alignment edge can be pushed one cycle later by setting their alignment offset to +1.

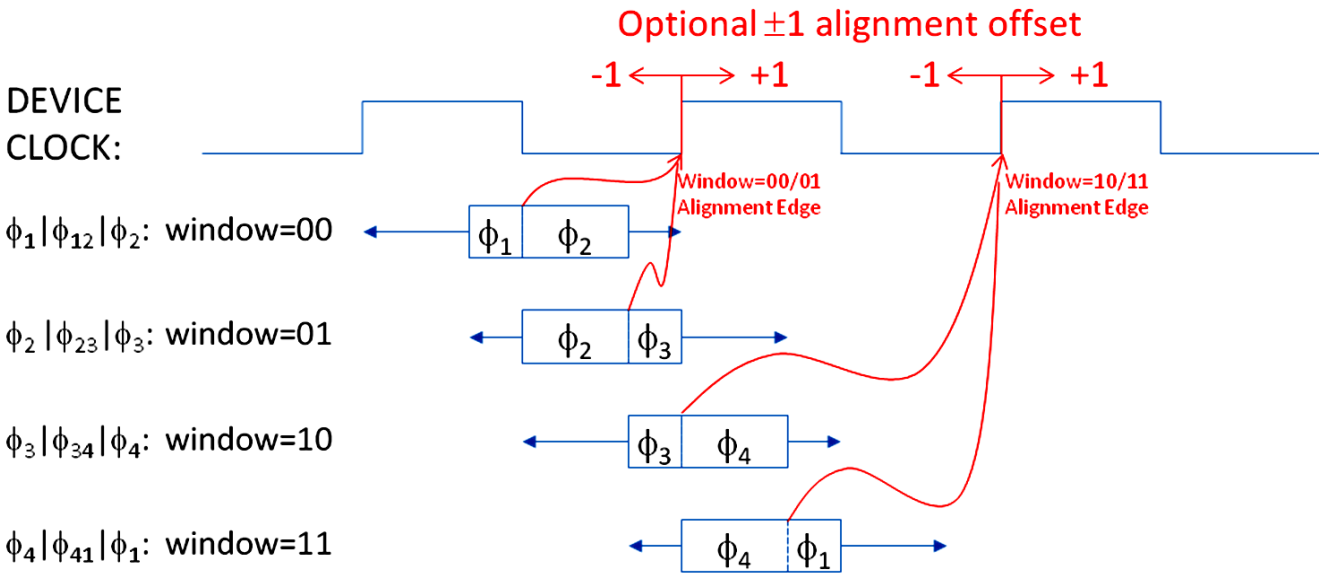

Figure 32. Optional SYSREF Alignment Offset

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Several important controls related to SYSREF alignment and capture timing are contained in register SYSR_CAPTURE (8.5.78). For example, as mentioned before, the device is capable of monitoring the observed phases of the rising SYSREF edge events; however, in order to avoid unwanted noise coupling from the SYSREF circuits into the DAC output, the SYSREF monitoring circuits are disabled by default. Field SYSR_STATUS_ENA enables SYSREF status monitoring. Field SYSR_PHASE_WDW contains the the phase tolerance window selected for normal operation, which is optimized during characterization. Field SYSR_ALIGN_DLY contains the control that allows the system designer to optionally offset the SYSREF alignment event by ±1 device clock cycles. Field SYSR_STATUS_ENA enables the SYSREF capture alignment accumulation and will generate alarms when enabled. Writing a “1” to field SYSR_ALIGN_SYNC clears the accumulated SYSREF alignment statistics. The SYSREF alignment block can be bypassed completely by field SYSREF_BYPASS_ALIGN, in which case SYSREF is latched by the rising edge of DACCLK.

When field SYSR_STATUS_ENA is high the device records the phase associated with each SYSREF event for use in characterizing the SYSREF capture timing and selecting an appropriate phase tolerance window. The phase data is available in two forms. First, each of the four phases has a corresponding “sticky” alarm flag indicating which phases have been observed since the last time the register was cleared. In addition, the device also accumulates statistics on the relative number of occurrences of each phase spanning multiple SYSREF events using saturating 8-bit counters. These accumulated real-time SYSREF statistics allow us to account for time-varying effects during characterization such as potential timing differences between the 1st and Nth edges in a “gapped” SYSREF pulse train. The counters are fields PHASE1_CNT and PHASE2_CNT in register SYSREF12_CNT (8.5.10), PHASE3_CNT and PHASE4_CNT in register SYSREF34_CNT (8.5.11), and ALIGN_TO_R1_CNT and ALIGN_TO_R3_CNT in register SYSREF_ALIGN_R (8.5.9).

The accumulated SYSREF statistics can be cleared by writing ‘1’ to SYSR_ALIGN_SYNC. This sync signal affects only the SYSREF statistics monitors and does not cause a sync of any other portions of the design. Before collecting phase statistics, the user must first enable the SYSREF status monitoring logic by setting the SYSR_STATUS_ENA bit. The user must then generate a repeating SYSREF input before using SYSR_ALIGN_SYNC to clear the statistic counters. This is necessary to flush invalid data out of the status pipeline.

The “sticky” alarm flags indicating which of the four phases have been observed since the last SYSR_ALIGN_SYNC write of ‘1’ are fields ALM_SYSRPHASE1 to ALM_SYSRPHASE4 and are contained in the ALM_SYSREF_DET register (8.5.6).

8.3.11 JESD204B Subclass 0 Support

Some functionality has been implemented to support Subclass 0 operation. Note that programming the SUBCLASSV configuration parameter has no functional impact on the logic. The value programmed for SUBCLASSV is only used in the initial lane alignment (ILA) sequence. The following configuration parameters are used to support Subclass 0 operation:

- Field SYSREF_MODE in register JESD_SYSR_MODE (8.5.56) = 0
- Field DISABLE_ERR_RPT in register JESD_ERR_OUT (8.5.53) = 1
- Field MIN_LATENCY_ENA in register JESD_MATCH (8.5.50) = 1

8.3.12 SerDes Test Modes through Serial Programming

The DAC38RF82 (or DAC38RF89) supports a number of basic pattern generation and verification of SerDes via the serial interface. Three pseudo random bit stream (PRBS) sequences are available, along with an alternating 0/1 pattern and a 20-bit user-defined sequence. The 2^7 - 1, 2^{31} - 1 or 2^{23} – 1 sequences implemented can often be found programmed into standard test equipment, such as a Bit Error Rate Tester (BERT). Pattern generation and verification selection is via field TESTPATT in register SRDS_CFG1 (8.5.86), as shown in Table 28.

Table 28. SerDes Test Pattern Selection

TESTPATT	EFFECT
000	Test mode disabled.
001	Alternating 0/1 Pattern. An alternating 0/1 pattern with a period of 2 UI.
010	Verify 2^7 - 1 PRBS. Uses a 7-bit LFSR with feedback polynomial $x^7 + x^6 + 1$.
011	Verify 2^{23} - 1 PRBS. Uses an ITU O.150 conformant 23-bit LFSR with feedback polynomial $x^{23} + x^{18} + 1$.
100	Verify 2^{31} - 1 PRBS. Uses an ITU O.150 conformant 31-bit LFSR with feedback polynomial $x^{31} + x^{28} + 1$.
101	User-defined 20-bit pattern. Uses the USR PATT IEEE1500 Tuning instruction field to specify the pattern. The default value is 0x66666.
11x	Reserved.

Pattern verification compares the output of the serial to parallel converter with an expected pattern. When there is a mismatch, the TESTFAIL bit is driven high, which can be programmed to come out the ALARM terminal by setting field DTEST in register DTEST (8.5.76) to “0011”.

8.3.13 SerDes Test Modes through IEEE 1500 Programming

DAC38RF82 (or DAC38RF89) also provide a number of advanced diagnostic capabilities controlled by the IEEE 1500 interface. These are:

- Accumulation of pattern verification errors;
- The ability to map out the width and height of the receive eye, known as Eye Scan;
- Rreal-time monitoring of internal voltages and currents;

The SerDes blocks support the following IEEE1500 instructions:

Table 29. IEEE1500 Instruction for SerDes Receivers

INSTRUCTION	OPCODE	DESCRIPTION
ws_bypass	0x00	Bypass. Selects a 1-bit bypass data register. Use when accessing other macros on the same IEEE1500 scan chain.
ws_cfg	0x35	Configuration. Write protection options for other instructions.
ws_core	0x30	Core. Fields also accessible via dedicated core-side ports.
ws_tuning	0x31	Tuning. Fields for fine tuning macro performance.
ws_debug	0x32	Debug. Fields for advanced control, manufacturing test, silicon characterization and debug.
ws_unshadowed	0x34	Unshadowed. Fields for silicon characterization.
ws_char	0x33	Char. Fields used for eye scan.

The data for each SerDes instruction is formed by chaining together sub-components called head, body (receiver or transmitter) and tail. DAC38RF82 (or DAC38RF89) uses two SerDes receiver blocks R0 and R1, each of which contains 4 receive lanes (channels), the data for each IEEE1500 instruction is formed by chaining {head, receive lane 0, receive lane 1, receive lane 2, receive lane 3, tail}. A description of bits in head, body and tail for each instruction is given as follows:

NOTE

All multi-bit signals in each chain are packed with bits reversed e.g. mpy[7:0] in ws_core head subchain is packed as {retime, enpll, mpy[0:7], vrange, lb[0:1]}. All DATA REGISTER READS from SerDes Block R0 should read 1 bit more than the desired number of bits and discard the first bit received on TDO e.g., to read 40-bit data from R0 block, 41 bits should be read off from TDO and the first bit received should be discarded. Similarly, any data written to SerDes Block R0 Data Registers should be prefixed with an extra 0.

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Table 30. ws_cfg Chain

FIELD	DESCRIPTION
HEAD (STARTING FROM THE MSB OF CHAIN)	
RETIME	No function.
CORE_WE	Core chain write enable.
RECEIVER (FOR EACH LANE 0, 1, 2, 3)	
CORE_WE	Core chain write enable.
TUNING_WE	Tuning chain write enable.
DEBUG_WE	Reserved.
CHAR_WE	Char chain write enable.
UNSHADOWED_WE	Reserved.
TAIL (ENDING WITH THE LSB OF CHAIN)	
CORE_WE	Core chain write enable.
TUNING_WE	Tuning chain write enable.
DEBUG_WE	Reserved.
RETIME	No function.
CHAIN LENGTH = 26 BITS	

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Table 31. ws_core Chain

FIELD	DESCRIPTION
HEAD (STARTING FROM THE MSB OF CHAIN)	
RETIME	No function.
ENPLL	PLL enable.
MPY[7:0]	PLL multiply.
VRANGE	VCO range.
ENDIVCLK	Enable DIVCLK output
LB[1:0]	Loop bandwidth
RECEIVER (FOR EACH LANE 0,1,2,3)	
ENRX	Receiver enable.
SLEEPRX	Receiver sleep mode.
BUSWIDTH[2:0]	Bus width.
RATE[1:0]	Operating rate.
INVPAIR	Invert polarity.
TERM[2:0]	Termination.
ALIGN[1:0]	Symbol alignment.
LOS[2:0]	Loss of signal enable.
CDR[2:0]	Clock/data recovery.
EQ[2:0]	Equalizer.
EQHLD	Equalizer hold.
ENOC	Offset compensation.
LOOPBACK[1:0]	Loopback.
BSINRXP	Boundary scan initialization.
BSINRXN	Boundary scan initialization.
RESERVED	Reserved.
Testpatt[2:0]	Test pattern selection.
TESTFAIL	Test failure (real time).
LOSTDTCT	Loss of signal detected (real time).
BSRXP	Boundary scan data.
BSRXN	Boundary scan data.
OCIP	Offset compensation in progress.
EQOVER	Receiver signal over equalized.
EQUNDER	Receiver signal under equalized.
LOSTDTCT	Loss of signal detected (sticky).
SYNC	Re-alignment done, or aligned comma output (sticky).
RETIME	No function.
TAIL (ENDING WITH THE LSB CHAIN)	
CLKBYP[1:0]	Clock bypass.
SLEEPPLL	PLL sleep mode.
RESERVED	Reserved.
LOCK	PLL lock (real time).
BSINITCLK	Boundary scan initialization clock.
ENBSTX	Enable TX boundary scan.
ENBSRX	Enable RX boundary scan.
ENBSPT	RX pulse boundary scan.
RESERVED	Reserved.
NEARLOCK	PLL near to lock.
UNLOCK	PLL lock (sticky).

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Table 31. ws_core Chain (continued)

FIELD	DESCRIPTION
CFG OVR	Configuration over-ride.
RETIME	No function.
CHAIN LENGTH = 196 BITS	

Table 32. ws_tuning Chain

FIELD	DESCRIPTION
HEAD (STARTING FROM THE MSB OF CHAIN)	
RETIME	No function.
RECEIVER (FOR EACH LANE 0,1,2,3)	
PATTERRTHR[2:0]	Resync error threshold.
PATT TIMER	PRBS timer.
RXDSEL[3:0]	Status select.
ENCOR	Enable clear-on-read for error counter.
EQZERO[4:0]	EQZ OVRi Equalizer zero.
EQZ OVR	Equalizer zero over-ride.
EQLEVEL[15:0]	EQ OVRi Equalizer gain observe or set.
EQ OVR	Equalizer over-ride.
EQBOOST[1:0]	Equalizer gain boost.
RXASEL[2:0]	Selects amux output.
TAIL (ENDING WITH THE LSB CHAIN)	
ASEL[3:0]	Selects amux output.
USR PATT[19:0]	User-defined test pattern.
RETIME	No function.
CHAIN LENGTH = 174 BITS	

Table 33. ws_char Chain

FIELD	DESCRIPTION
HEAD (STARTING FROM THE MSB OF CHAIN)	
RETIME	No function.
RECEIVER (FOR EACH LANE 0,1,2,3)	
TESTFAIL	Test failure (sticky).
ECOUNT[11:0]	Error counter.
ESWORD[7:0]	Eye scan word masking.
ES[3:0]	Eye scan.
ESPO[6:0]	Eye scan phase offset.
ES BIT SELECT[4:0]	Eye scan compare bit select.
ESVO[5:0]	Eye scan voltage offset.
ESVO OVR	Eye scan voltage offset override.
ESLEN[1:0]	Eye scan run length.
ESRUN	Eye scan run.
ESDONE	Eye scan done.
TAIL (ENDING WITH THE LSB CHAIN)	
RETIME	No function.
CHAIN LENGTH = 194 BITS	

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8.3.14 Error Counter

All receive channels include a 12-bit counter for accumulating pattern verification errors. This counter is accessible via the ECOUNT IEEE1500 Char field. It is an essential part of the eye scan capability (see the *Eye Scan* section).

The counter increments once for every cycle that the TESTFAIL bit is detected. The counter does not increment when at its maximum value (i.e., all 1s). When an IEEE1500 capture is performed, the count value is loaded into the ECOUNT scan elements (so that it can be scanned out), and the counter is then reset, provided NCOR is set high.

ECOUNT can be used to get a measure of the bit error rate. However, as the error rate increases, it becomes less accurate due to limitations of the pattern verification capabilities. Specifically, the pattern verifier checks multiple bits in parallel (as determined by the Rx bus width), and it is not possible to distinguish between 1 or more errors.

8.3.15 Eye Scan

All receive channels provide features which facilitate mapping the received data eye or extracting a symbol response. A number of fields accessible via the IEEE1500 Char scan chain allow the required low level data to be gathered. The process of transforming this data into a map of the eye or a symbol response must then be performed externally, typically in software.

The basic principle used is as follows:

- Enable dedicated eye scan input samplers, and generate an error when the value sampled differs from the normal data sample;
- Apply a voltage offset to the dedicated eye scan input samplers, to effectively reduce their sensitivity;
- Apply a phase offset to adjust the point in the eye that the dedicated eye scan data samples are taken;
- Reset the error counter to remove any false errors accumulated as a result of the voltage or phase offset adjustments;
- Run in this state for a period of time, periodically checking to see if any errors have occurred;
- Change voltage and/or phase offset, and repeat.

Alternatively, the algorithm can be configured to optimize the voltage offset at a specified phase offset, over a specified time interval.

Eye scan can be used in both synchronous and asynchronous systems, while receiving normal data traffic. The IEEE1500 Char fields used to directly control eye scan and symbol response extraction are ES, ESWORD, ES BIT SELECT, ESLEN, ESPO, ESVO, ESVO OVR, ESRUN and ESDONE. Eye scan errors are accumulated in ECOUNT.

The required eyescan mode is selected via the ES field, as shown in Table 34. When enabled, only data from the bit position within the 20-bit word specified via ES BIT SELECT is analyzed. In other words, only eye scan errors associated with data output at this bit position will accumulate in ECOUNT. The maximum legal ES BIT SELECT is 10011.

Table 34. Eye Scan Mode Selection

ES[3:0]	EFFECT
0000	Disabled. Eye scan is disabled.
0x01	Compare. Counts mismatches between the normal sample and the eye scan sample if ES[2] = 0, and matches otherwise.
0x10	Compare zeros. As ES = 0x01, but only analyses zeros, and ignores ones.
0x11	Compare ones. As ES = 0x01, but only analyses ones, and ignores zeroes.
0100	Count ones. Increments ECOUNT when the eye scan sample is a 1.
1x00	Average. Adjusts ESVO to the average eye opening over the time interval specified by ESLEN. Analyses zeroes when ES[2] = 0, and ones when ES[2]= 1.
1001 1110	Outer. Adjusts ESVO to the outer eye opening (i.e. lowest voltage zero, highest voltage 1) over the time interval specified by ESLEN. 1001 analyses zeroes, 1110 analyses ones.
1010 1101	Inner. Adjusts ESVO to the inner eye opening (i.e. highest voltage zero, lowest voltage 1) over the time interval specified by ESLEN. 1010 analyses zeroes, 1101 analyses ones.

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Table 34. Eye Scan Mode Selection (continued)

ES[3:0]	EFFECT
1x11	Timed Compare. As ES = 001x, but analyses over the time interval specified by ESLEN. Analyses zeroes when ES[2] = 0, and ones when ES[2] = 1.

When ES[3] = 0, the selected analysis runs continuously. However, when ES[3] = 1, only the number of qualified samples specified by ESLed, as shown in Table 35. In this case, analysis is started by writing a 1 to ESRUN (it is not necessary to set it back to 0). When analysis completes, ESDONE is set to 1.

Table 35. Eye Scan Run Length

ESLen	NUMBER OF SAMPLES ANALYZED
00	127
01	1023
10	8095
11	65535

When ESVO OVR = 1, the ESVO field determines the amount of offset voltage that is applied to the eye scan data samplers associated with rxpi and rxni. The amount of offset is variable between 0 and 300 mV in increments of ~10 mV, as shown Table 36. When ES[3] = 1, ESVO OVR must be 0 to allow the optimized voltage offset to be read back via ESVO.

Table 36. Eye Scan Voltage Offset

ESVO	OFFSET (mV)
100000	-310
…	…
111110	-20
111111	-10
000000	0
000001	10
000010	20
…	…
011111	300

The phase position of the samplers associated with rxpi and rxni, is controlled to a precision of 1/32UI. When ES is not 00, the phase position can be adjusted forwards or backwards by more than one UI using the ESPO field, as shown in Table 37. In normal use, the range should be limited to ±0.5 UI (+15 to –16 phase steps).

Table 37. Eye Scan Phase Offset

ESPO	OFFSET (1/32 UI)
011111	+63
…	…
000001	+1
000000	0
111111	-1
…	…
100000	-64

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8.3.16 JESD204B Pattern Test

The DAC38RF82 (or DAC38RF89) supports the following test patterns for JESD204B:

- Link layer test pattern by setting field JESD_TEST_SEQ in register JESD_LN_EN (8.5.45) and monitoring the lane alarms (1 = fail, 0 = pass)
  - Verify repeating /D.21.5/ high frequency pattern for random jitter (RJ)
  - Verify repeating /K.28.5/ mixed frequency pattern for deterministic jitter (DJ)
  - Verify repeating initial lane alignment (ILA) sequence
- RPAT, JSPAT or JTSPAT pattern can be verified using errors counter of 8b/10b errors produced over an amount of time to get an estimate of BER.
- Transport layer test pattern: implements a short transport layer pattern check based on F = 1, 2, 4 or 8. The short test pattern has a duration of one frame period and is repeated continuously for the duration of the test. Each sample has a unique value that can be identified with the position of the sample in the user data format. The sample values are such that correct sample values will never be decoded at the receiver if there is a mismatch between the mapping formats being used at the transmitter and receiver devices. This can generally be accomplished by ensuring there are no repeating sub patterns within the stream of samples being transmitted. Refer to the JESD204B standard section 5.1.6 for more details.

The DAC38RF82 (or DAC38RF89) expects the test samples, in a frame, transmitted by an logic device as per Table 38:

Table 38. Short Test Patterns

JESD Mode	i0	q0	i1	q1
82121	7CB8, F431	6DA9, E520	n/a	n/a
42111	7CB8	F431	n/a	n/a
22210	7CB8	F431	n/a	n/a
12410	7CB8	F431	n/a	n/a
44210	7CB8	F431	6DA9	E520
24410	7CB8	F431	6DA9	E520
41121	7CB8, F431	n/a	n/a	n/a
81180	7C00, B800, F400, 3100, 6D00, A900, E500, 2000	n/a	n/a	n/a
24310	7CB0	F430	6DA0	E520
41380	7CB0, F430, 6DA0, E520, F870, E960, DA50, CB40	n/a	n/a	n/a

The short test pattern has duration of one frame period and is repeated continuously for the duration of the test. Each sample has a unique value that can be identified with the position of the sample in the user data format. The sample values are such that correct sample values will never be decoded at the receiver if there is a mismatch between the mapping formats being used at the transmitter and receiver devices. This can generally be accomplished by ensuring there are no repeating sub patterns within the stream of samples being transmitted.

Following are the steps required to execute the short test functionality in DAC38RF82 (or DAC38RF89).

1. Configure other registers, make sure clocks are up and running.
2. Start driving short test patterns
3. Clear short test alarm by writing ‘0’ to field ALM_FROM_SHORTTEST in register ALM_SYSREF_PAP (8.5.67). This is a paged register, one for each Multi-DUC.
4. Enable short test by writing a ‘1’ to field SHORTTEST_ENA in register MULTIDUC_CFG2 (8.5.14).
5. Read the short test alarm from field ALM_FROM_SHORTTEST in register ALM_SYSREF_PAP (8.5.67). This is a paged register, one for each Multi-DUC

If the alarm read from the register is high, the short test has detected an error.

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8.3.17 Wideband DUC (wide-DUC)

Each DAC output in the DAC38RF82 ((or DAC38RF89)) can be supported by a wide band digital up-converter (DUC), which is called a wide-DUC. Figure 33 shows the implementation and signal processing features of the wide-DUC which is only available in the 2-TX modes (Table 9). For complex inputs, the in-phase (or I-channel) is path AB of DAC A and the phase of the NCO in this path (7.5.19) must be set to 0 degrees. Similarly, the quadrature phase (or Q-channel) is path AB of DAC B and the phase of the NCO in this path (7.5.19) must be set to 90 degrees. The NCO frequency in both I and Q paths (7.5.20) must be set to the same value. The SPI interface registers for the wide-DUC are addressed through paging, with page 1 supporting the I-channel and page 2 supporting Q-channel configuration of the wide-DUC. Register PAGE_SET (8.5.8) is used to set the pages. Both pages can be selected at the same time to program both channels of wide-DUC simultaneously.

The output of I and Q channels are added together using the output summation block (Figure 33). Bit 0 and Bit 2 of the register field OUTSUM_SEL must be set to for this to be accomplished.

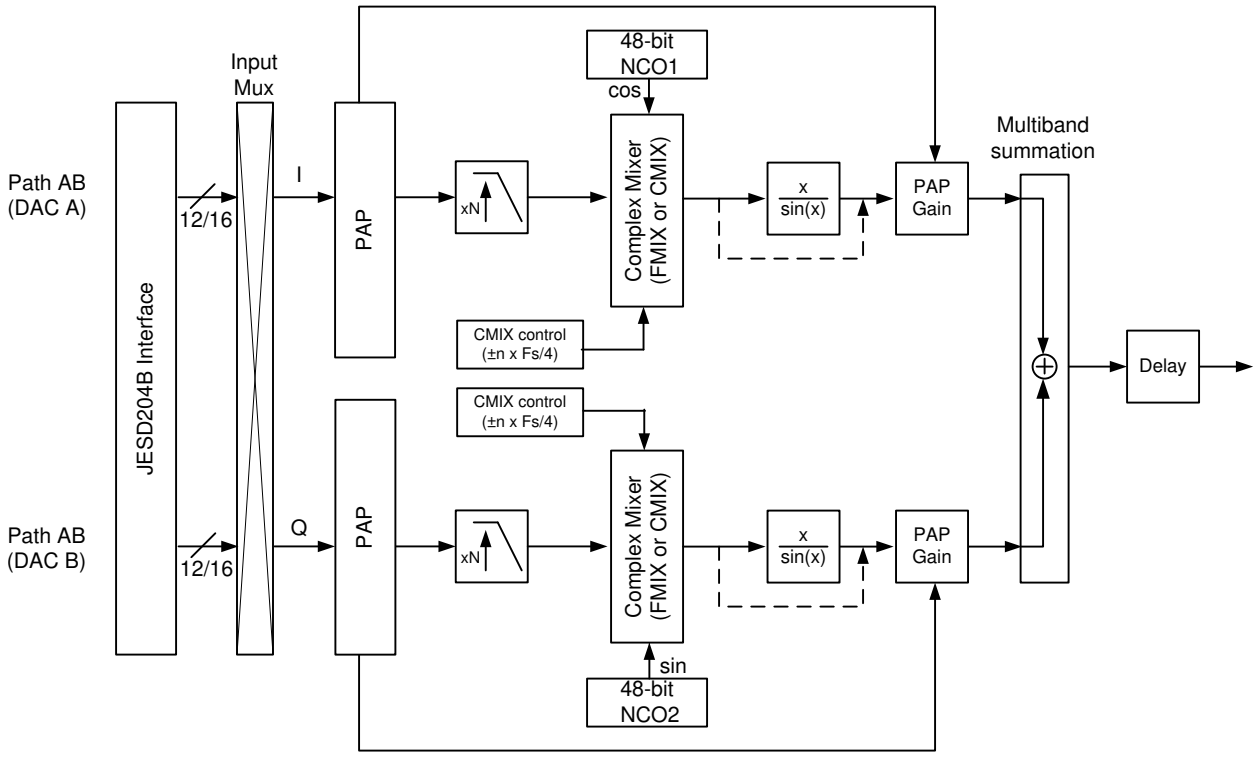

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Figure 33. DAC38RF82 Wide-DUC Signal Processing Block Diagram

8.3.18 Interpolation Block

The DAC38RF82 (or DAC38RF89) provides the optional interpolation of 2x in 12-bit input mode and 2x or 4x in 16-bit input mode. In addition, 1x interpolation can be used in 8, 12 or 16-bit input modes to pass the data directly to the DAC output. The SPI interface registers for the multi-DUCs are addressed through paging, with page 0 supporting the I channel and page 1 supporting the Q channel. Register PAGE_SET (8.4.8) is used to set the pages. Both pages can be selected at the same time to program both multi-DUCs simultaneously with the same settings.

8.3.18.1 Multi-DUC input

Each interpolation block accepts data from up to 8 SerDes lanes. A crossbar switch allows any SerDes lane to be mapped to any other SerDes lane. The crossbar switch is controlled by fields OCTETPATHx_SEL (x = [0..7]) in Registers JESD_CROSSBAR1 (8.5.57) and JESD_CROSSBAR2 (8.5.58).

8.3.18.2 Interpolation Filters

The digital upconverter first increases the sample rate of the IQ signal from the input sample rate to the final DAC sample rate through a series of interpolation filters. Different sets of filters are used to achieve different rates, as shown in Table 39. The interpolation rate is selected by field INTERP in register MULTIDUC_CFG1 (8.5.13).

Table 39. FIR filters Used for Different Interpolation Rates

FILTERS USED		
Interpolation Rate	**FIR0 (2x)**	**FIR1 (2x)**
2	x	
4	x	x

The FIR filter coefficients are shown in Table 40 The FIR filters are design with a passband BW of 0.4 x f_{INPUT}, a stopband attenuation of 90 dBc and ripple of < 0.001 dB. The composite frequency response for each interpolation factor are shown in *Figure 34*to *Figure 41*.

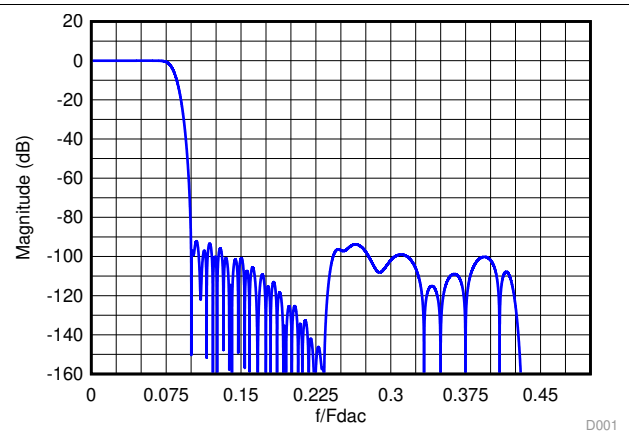

Figure 34. Composite Magnitude Response for 6x Interpolation

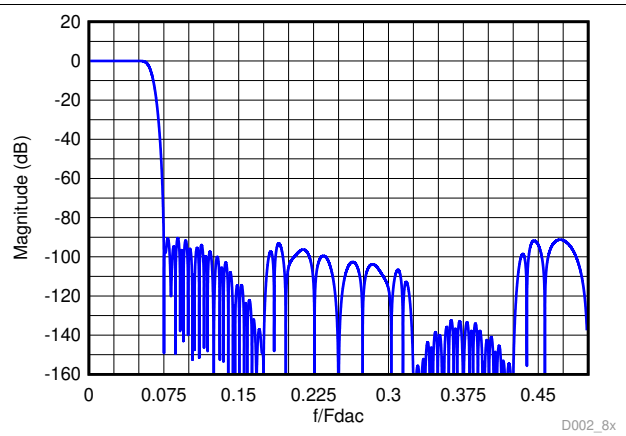

Figure 35. Composite Magnitude Response for 8x Interpolation

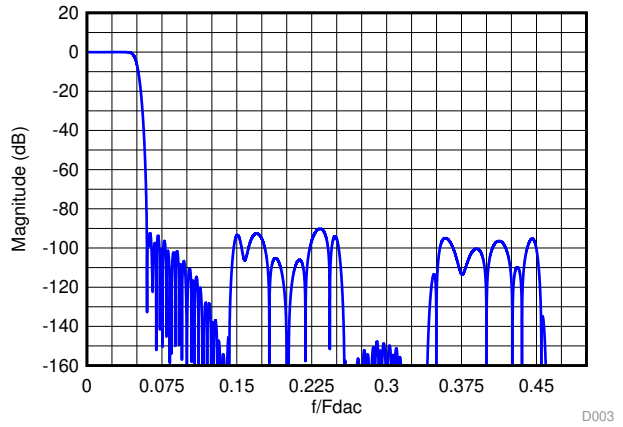

Figure 36. Composite Magnitude Response for 10x Interpolation

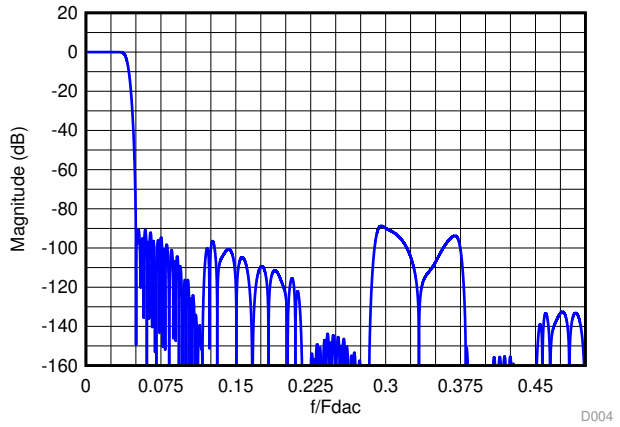

Figure 37. Composite Magnitude Response for 12x Interpolation

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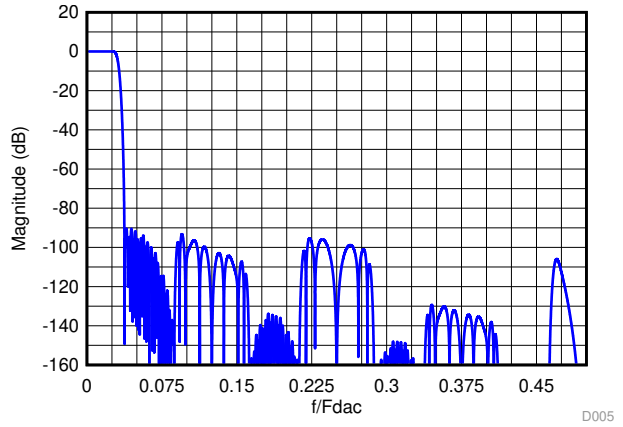

Figure 38. Composite Magnitude Response for 16x Interpolation

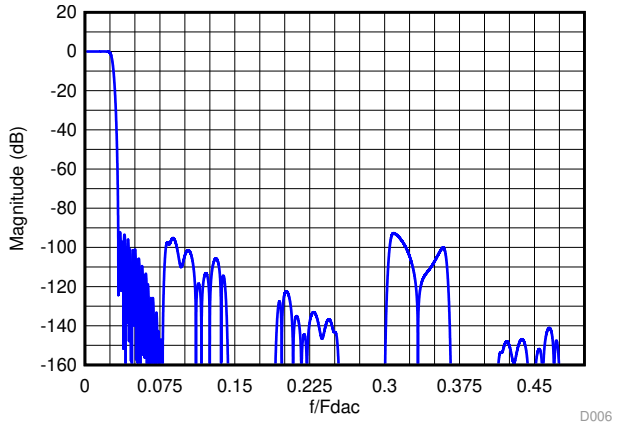

Figure 39. Composite Magnitude Response for 18x Interpolation

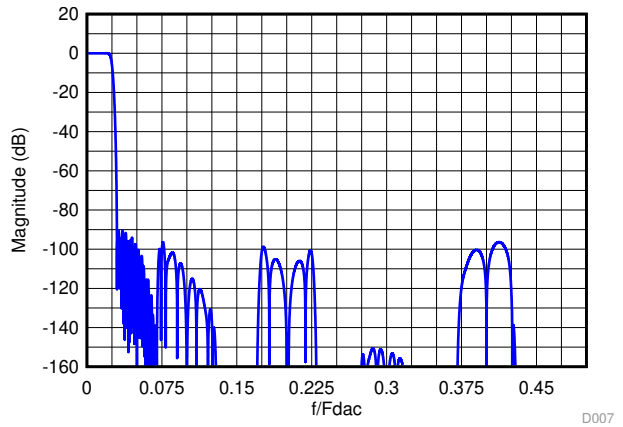

Figure 40. Composite Magnitude Response for 20x Interpolation

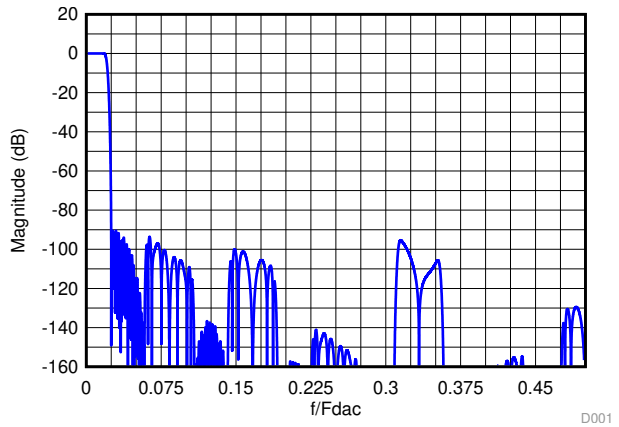

Figure 41. Composite Magnitude Response for 24x Interpolation

Table 40. FIR Filter Coefficients

tap	FIR0	FIR1	LPFIR0_5X	FIR2	LPFIR0_3X	FIR3	LPFIR1_3X	INVSINC
1	6	-12	-6	29	-14	3	25	1
2	0	0	-22	0	-61	0	88	-4
3	-19	84	-51	-214	-125	-25	22	13
4	0	0	-89	0	-95	0	-576	-50
5	47	-336	-117	1209	181	150	-1764	592
6	0	0	-106	2048	681	256	-2263	-50
7	-100	1006	-18	1209	972	150	491	13
8	0	0	171	0	347	0	8139	-4
9	192	-2691	449	-214	-1475	-25	18625	1
10	0	0	745	0	-3519	0	26365	
11	-342	10141	930	29	-3528	3	26365	
12	0	16384	841		707		18625	
13	572	10141	338		9337		8139	
14	0	0	-618		19445		491	
15	-914	-2691	-1892		26299		-2263	
16	0	0	-3147		26299		-1764	

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Table 40. FIR Filter Coefficients (continued)

tap	FIR0	FIR1	LPFIR0_5X	FIR2	LPFIR0_3X	FIR3	LPFIR1_3X	INVSINC
17	1409	1006	-3872		19445		-576	
18	0	0	-3500		9337		22	
19	-2119	-336	-1564		707		88	
20	0	0	2121		-3528		25	
21	3152	84	7336		-3519			
22	0	0	13430		-1475			
23	-4729	-12	19426		347			
24	0		24231		972			
25	7420		26904		681			
26	0		26904		181			
27	-13334		24231		-95			
28	0		19426		-125			
29	41527		13430		-61			
30	65536		7336		-14			
31	41527		2121					
32	0		-1564					
33	-13334		-3500					
34	0		-3872					
35	7420		-3147					
36	0		-1892					
37	-4729		-618					
38	0		338					
39	3152		841					
40	0		930					
41	-2119		745					
42	0		449					
43	1409		171					
44	0		-18					
45	-914		-106					
46	0		-117					
47	572		-89					
48	0		-51					
49	-342		-22					
50	0		-6					
51	192							
52	0							
53	-100							
54	0							
55	47							
56	0							
57	-19							
58	0							
59	6							

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8.3.18.3 JESD204B Modes, Interpolation and Clock phase Programming

Table 41 lists the register field values required for each JESD204B mode interpolation mode and clock phase. The register field addresses are listed in Table 42.

Table 41. Register Programming for JESD and Interpolation Mode

Mode			Register Field Programming								
L-M-F-S-Hd 1 TX/2TX	Interp	CLOCK PHASES (1-0)	INTERP (4-0)	CLKJESD_DIV (3-0)	CLKJESD_OUT_DIV (3-0)	L_M1 (4-0)	F_M1 (7-0)	M_M1 (7-0)	S_M1 (4-0)	HD	N_M1/N'_M1 (4-0)
82121/NA	6	11	00011	0110	0011	00111	0x00	0x01	00001	1	01111
	8	11	00100	0111	0100						
	12	11	00110	1010	0110						
	16	11	01000	1011	0111						
42111/84111	6	10	00011	0010	0011	00011	0x00	0x01	00000	1	01111
	8	11	00100	0011	0100						
	10	11	00101	0101	0101						
	12	11	00110	0110	0110						
	16	11	01000	0111	0111						
	18	11	01001	1001	1000						
	24	11	01100	1010	1010						
22210/44210	8	01	00100	0001	0100	00001	0x01	0x01	00000	0	01111
	12	10	00110	0010	0110						
	16	11	01000	0011	0111						
	18	11	01001	0100	1000						
	20	11	01010	0101	1001						
	24	11	01100	0110	1010						
12410/24410	16	01	01000	0001	0111	00000	0x03	0x01	00000	0	01111
	24	10	01100	0010	1010						
44210/88210	8	01	00100	0001	0100	00011	0x01	0x03	00000	0	01111
	12	10	00110	0010	0110						
	16	11	01000	0011	0111						
	24	11	01100	0110	1010						
24410/48410	16	01	01000	0001	0111	00001	0x03	0x03	00000	0	01111
	24	10	01100	0010	1010						
81180/NA	1	11	00000	0011	0001	00111	0x00	0x00	00111	0	00111
41380/82380	1	00	00000	1100	0000	00011	0x02	0x00	00111	0	01011
	2	00	00001	1101	0001						
41121/ 82121	1	01	00000	0000	0000	00011	0x00	0x00	00001	1	01111
	2	01	000001	0001	0001						
	4	11	00010	0011	0010						
24310/48310	24	11	01100	0011	1010	00001	0x02	0x03	00000	0	01011

Table 42. Register Field Addresses for JESD204B Mode, Interpolation and Clock Phase Programming

Register Field Name	Register	Register Address	Bit(s)	Hyperlink
INTERP	MULTIDUC_CFG1	0x0A	12-8	8.5.13
CLKJESD_DIV	SerDes_CLK	0x25	15-12	8.5.28
CLKJESD_OUT_DIV			11-8	
L_M1	JESD_K_L	0x4C	4-0	8.5.47
F_M1	JESD_RBD_F	0x4B	7-0	8.5.46
M_M1	JESD_M_S	0x4D	15-8	8.5.48
S_M1			4-0	

Table 42. Register Field Addresses for JESD204B Mode, Interpolation and Clock Phase Programming (continued)

Register Field Name	Register	Register Address	Bit(s)	Hyperlink
HD	JESD_N_HD_SCR	0x4E	6	8.5.49
N_M1			4-0	
N_M1' (NPRIME_M1)			12-8	
JESD_PHASE_MODE	JESD_LN_EN	0x4A	1-0	8.5.45
All registers are paged!				

8.3.18.4 Digital Quadrature Modulator

Each DUC in the DAC38RF8x has digital quadrature modulator (DQM) blocks with independent Numerically Controlled Oscillators (NCO) that converts the complex input signal to a real signal with flexible frequency placement between 0 and $f_{DAC}/2$. The NCOs are enabled by fields NCOAB_ENA and NCOCD_ENA in register MULTIDUC_CFG2 (8.5.14). The NCOs have 48-bit frequency registers (FREQ_NCOAB (8.5.25) and FREQ_NCOCD (8.5.26)) and 16-bit phase registers (PHASE_NCOAB (8.5.23) and PHASE_NCOCD (8.5.24)) that generate the sine and cosine terms for the complex mixing. The NCO block diagram is shown in Figure 42.

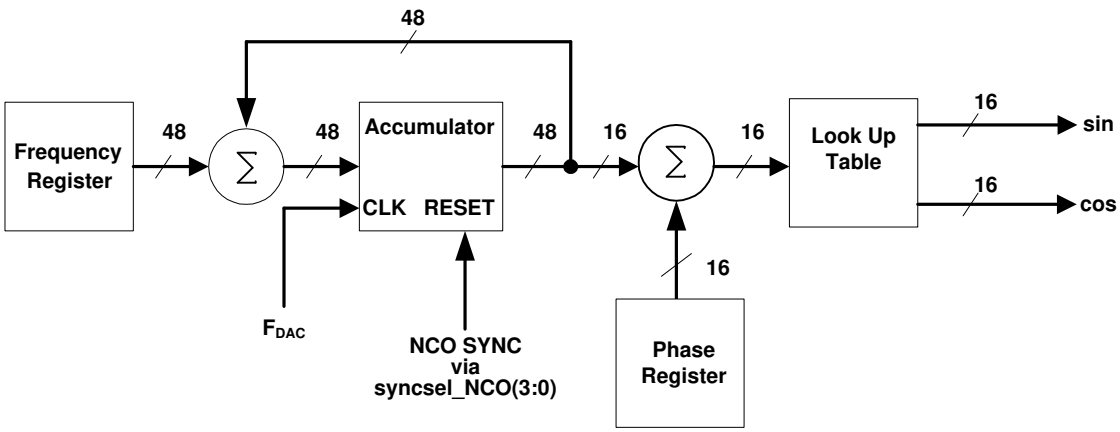

Figure 42. NCO Block Diagram

Synchronization of the NCOs occurs by resetting the NCO accumulators to zero. The synchronization source is selected by fields SYNCSEL_NCOAB and SYNCSEL_NCOCD in register SYNCSEL1 (8.5.29). The frequency word in the FREQ_NCOAB and FREQ_NCOCD registers are added to the accumulators every clock cycle, f_{DAC}.

The frequency and phase offset of the NCOs are:

$$f_{NCOAB(or\ CD)} = \frac{\mathbf{FREQ_NCOAB(or\ CD)} \times \mathbf{f_{DAC}}}{2^{48}} \tag{1}$$

$$\delta_{AB(or\ CD)} = 2\pi \times \frac{\mathbf{PHASE_NCOAB(or\ CD)}}{2^{16}} \tag{2}$$

Treating the complex channels as complex vectors of the form I + j Q, the output of the DQM is:

$$Output_{AB} = \left\{ I_{INPUTAB} \times cos\left(2\pi f_{NCOAB} t + \delta_{AB}\right) - Q_{INPUTAB} \times sin\left(2\pi f_{NCOAB} t + \delta_{AB}\right) \right\} \times 2^{\left(MIXERAB_GAIN - 1\right)} \tag{3}$$

$$Output_{CD} = \left\{ I_{INPUTCD} \times cos\left(2\pi f_{NCOCD} t + \delta_{CD}\right) - Q_{INPUTCD} \times sin\left(2\pi f_{NCOCD} t + \delta_{CD}\right) \right\} \times 2^{\left(MIXERCD_GAIN - 1\right)} \tag{4}$$

Where t is the time since the last resetting of the NCO accumulator and the fields MIXERAB_GAIN and MIXERCD_GAIN in register MULTIDUC_CFG2 (8.5.13) are either 0 or 1.

The maximum output amplitude of the DQM occurs if $I_{IN}(t)$ and $Q_{IN}(t)$ are simultaneously full scale amplitude and the sine and cosine arguments are equal to an integer multiple of $\pi/4$.

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With MIXERAB_GAIN or MIXERCD_GAIN = 0, the gain through the DQM is sqrt(2)/2 or -3 dB. This loss in signal power is in most cases undesirable, and it is recommended that the gain function be used to increase the signal by 3 dB to compensate. With MIXERAB_GAIN or MIXERCD_GAIN = 1, the gain through the DQM is sqrt(2) or +3 dB, which can cause clipping of the signal if $I_{IN}(t)$ and $Q_{IN}(t)$ are simultaneously near full scale amplitude and should therefore be used with caution.

8.3.18.5 Low Power Coarse Resolution Mixing Modes

In addition to the NCO the DAC38RFxx also has a coarse mixer block capable of shifting the input signal spectrum by the fixed mixing frequencies ±N x $f_{DAC}/8$. Using the coarse mixer instead of the full mixers will result in lower power consumption.

Treating the two complex channels as complex vectors of the form I(t) + j Q(t), the outputs of the coarse mixer is equivalent to:

$$Output_{AB} = I_{INPUTAB} \times cos\left(2\pi f_{CMIX_AB} t\right) - Q_{INPUTAB} \times sin\left(2\pi f_{CMIX_AB} t\right) \quad (5)$$

$$Output_{CD} = I_{INPUTCD} \times cos\left(2\pi f_{CMIX_CD} t\right) - Q_{INPUTCD} \times sin\left(2\pi f_{CMIX_CD} t\right) \quad (6)$$

Where f_{CMIX_AB} and f_{CMIX_CD} and the fixed mixing frequency selected by fields CMIX_AB or CMIX_CD in register CMIX (8.5.21). The coarse mixer blocks are disabled by setting CMIX_AB and CMIX_CD to 0x0.

The NCO and coarse mixers can be enabled simultaneously, although this is not useful in most cases as the full frequency range can be covered by the NCO.

8.3.18.6 Inverse Sinc Filter

The DAC38RF82 (or DAC38RF89) has a 9-tap inverse Sinc filter (INVSINC) that runs at the DAC update rate (f_{DAC}) that can be used to flatten the frequency response of the sample-and-hold output. The DAC sample-and-hold output sets the output current and holds it constant for one DAC clock cycle until the next sample, resulting in the well known sin(x)/x or Sinc(x) frequency response (Figure 43, red line). The inverse sinc filter response (Figure 43, blue line) has the opposite frequency response from 0 to 0.4 x f_{DAC}, resulting in the combined response (Figure 43, green line). Between 0 to 0.4 x f_{DAC}, the inverse sinc filter compensates the sample-and-hold roll-off with less than 0.03 dB error.

The inverse sinc filter has a gain > 1 at all frequencies. Therefore, the signal input to INVSINC must be reduced from full scale to prevent saturation in the filter. The amount of back-off required depends on the signal frequency, and is set such that at the signal frequencies the combination of the input signal and filter response is less than 1 (0 dB). For example, if the signal input to INVSINC is at 0.25 x f_{DAC}, the response of INVSINC is 0.9 dB, and the signal must be backed off from full scale by 0.9 dB to avoid saturation. The advantage of INVSINC having a positive gain at all frequencies is that the user is then able to optimize the back-off of the signal based on its frequency.

The inverse sinc filters are enabled by field ISFIR_ENA in register MULTIDUC_CFG1 (8.5.13).

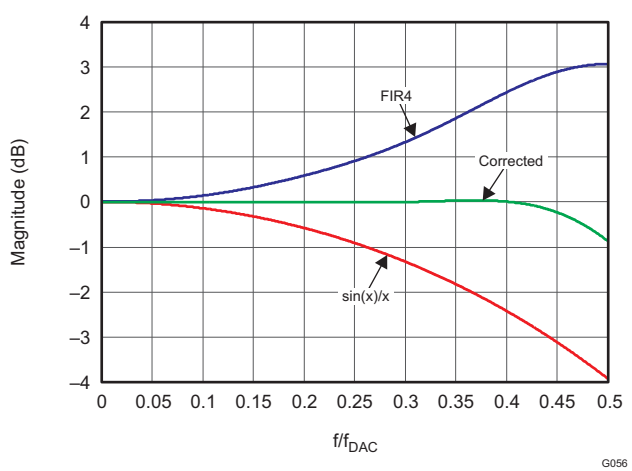

Figure 43. Composite Magnitude Spectrum for INVSINC

8.3.19 PA Protection Block

The DAC38RFxx incorporates an optional power amplifier protection (PAP) block to monitor when the input signal is two large, for example when an interface error occurs, and reduces the output signal power of the DAC. The PAP block achieves the functionality of reducing the input signal that crosses the threshold through three main sub-blocks. These are PAP trigger generation block, PAP gain state machine and GAIN block.

The PAP block keeps track of the input signal power by maintaining a sliding window accumulation of last N samples. N is selectable to be 32, 64 or 128 based on the setting (Table 43) of fields PAPAB_SEL_DLY in register PAP_CFG_AB (8.5.35) and PAPCD_SEL_DLY in register PAP_CFG_CD (8.5.36). The average amplitude of input signal is computed by dividing accumulated value by the number of samples in the delay-line (N). The result is then compared against the threshold in fields PAPAB_THRESH in register PAP_CFG_AB (8.5.35) and PAPCD_THRESH in register PAP_CFG_CD (8.5.36). If the threshold is violated, gain state machine is triggered which generated gain value to ramp down the DAC output signal amplitude. After the input signal returns to normal value, the state machine ramps up the DAC output signal amplitude.

Table 43. PAP Delay Line Selection

pap_sel_dly[1:0]	# of samples averaged
00	32
01	64
10	128
11	Reserved

The generation of the PAP trigger as explained as follows:

- The I and Q samples are treated separately – either can trigger attenuation
- In dual DUC modes, each IQ pair is treated separately and has a separate gain block
- 8 samples at the input are put through an absolute value circuit (all 2's complement)
- Next these values are vector summed to get a 12 bit result
- Then 12 bit result is placed into the delay line and summed into the accumulator
- The accumulator is also subtracting out the delayed 12 bit word corresponding to N = 32, N = 64 or N = 128
- Finally the accumulator output is divided down by N and rounded to 13 bits. These 13 bits are compared to the threshold in the SPI registers. A pap_trig occurs if the threshold is exceeded.

The PAP gain state machine generates the pap gain value to be applied on the output stream to reduce the output signal amplitude. The state machine below is used to control the attenuation of the DAC output and the gaining up of the signal again once the trigger is released.

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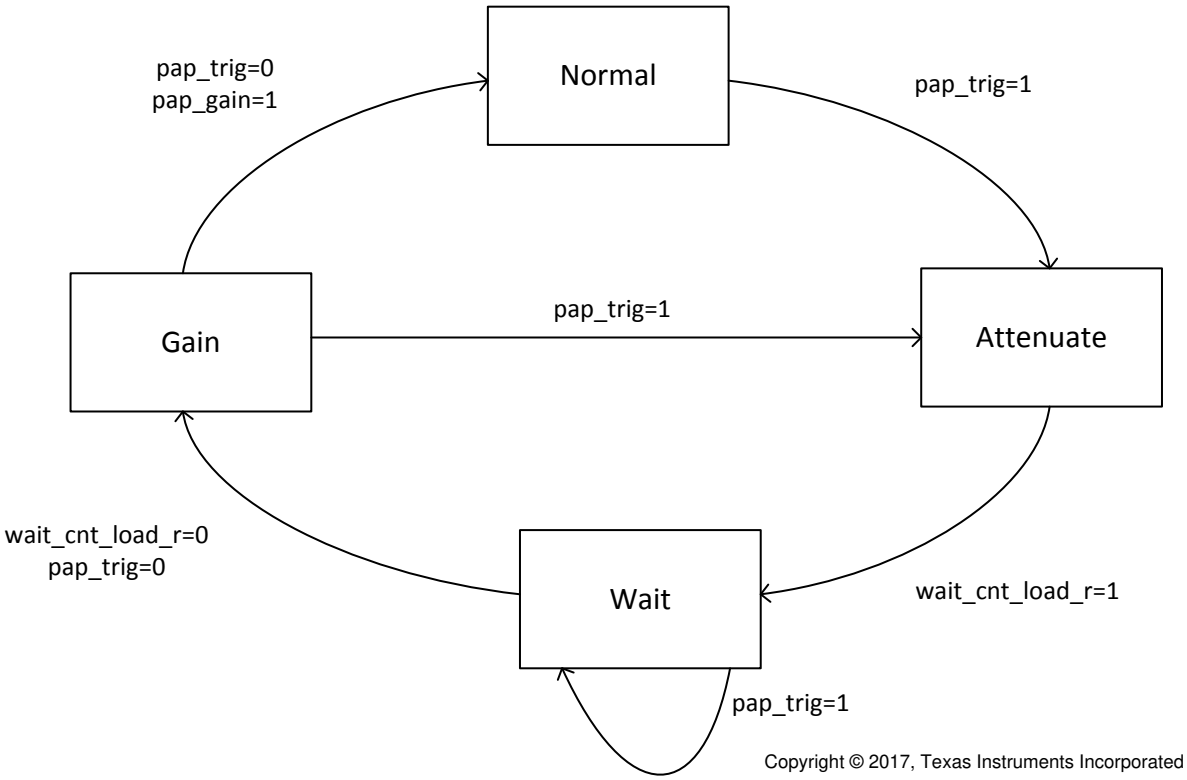

Figure 44. PAP Gain State Machine

The normal operating condition for the PAP block is the NORMAL state in Figure 44. However, when the PAP block detects an error condition it sets the pap_trig signal to '1' causing a state transition from NORMAL operation to the ATTENUATE state.

In the ATTENUTATE state the data path gain is scaled from 1.0 down to 0.0 by a programmable step amount set by fields PAPAB_GAIN_STEP in register PAP_GAIN_AB (8.5.31) and PAPCD_GAIN_STEP in register PAP_GAIN_CD (8.5.33). This value is always positive with the decimal place located between the MSB and MSB-1. Unity is equal to "1000000000". Each clock cycle (16 samples) the PAP_GAIN is stepped down by PAPAB_GAIN_STEP and PAPCD_GAIN_STEP until the gain is 0.

After PAP_GAIN is 0, the state machine moves on to the WAIT state. Here a programmable counter counts clock cycles to allow the condition for the pap_trig to be fixed. Fields PAPAB_WAIT in register PAP_WAIT_AB (8.5.32) and PAPCD_WAIT in register PAP_WAIT_CD (8.5.34) are used to select the number of clock cycles (samples = 16 x PAPAB_WAIT or 16 x PAPCD_WAIT) to wait before moving to the next state. Once the WAIT counter equals zero and pap_trig='0', the state machine moves on to the GAIN state. If the WAIT equals 0 but pap_trig still equals '1' then the state machine stays in the WAIT state until pap_trig ='0'.

8.3.20 Gain Block

The GAIN block also has additional output gain control through fields GAINAB in register GAINAB (8.5.39) and GAINCD in register GAINCD (8.5.40). Similar to PAP_GAIN value, the output gain is always positive with unity when GAINAB or GAINCD = "010000000000".

To reduce the power, the gain block clock has been gated whenever the pap is disabled and GAINAB or GAINCD is set to unity.

8.3.21 Output Summation

The OUTSUM block allows addition of samples from each DUC in the multi-DUC. It is also possible to add the output samples from the adjacent multi-DUC. Field OUTSUM_SEL in register OUTSUM (8.5.22) controls the summation for each multi-DUC. The functionality of the block can be represented by the following equation:

$$OUTSUM_{output} = SAME_{AB} + SAME_{CD} + ADJ_{AB} + ADJ_{CD} \quad (7)$$

In order to avoid overflow, rounding operation is performed after the addition to reduce the word size back to 16-bits. Exact number of bits rounded depends on the number of channels added. Table 44 shows the description of round after the summation.

Table 44. OUTSUM Scaling and Rounding

# OF CHANNELS ADDED	# OF BITS ROUNDED
0	0, Use bits[15:0] from the result
1	Use bits[16:1] from the result and bit[0] used for rounding
2	Use bits[17:2] from the result and bits[1:0] used for rounding
3	Use bits[18:3] from the result and bit[2:0 used for rounding
4	Use bits[19:4] from the result and bit[3:0] used for rounding

8.3.22 Output Delay

The signal following output summation can be programmably delayed by 0-15 DACCLK cycles through field OUTPUT_DELAY in register OUTSUM (8.5.20). The block takes 16 sample words (vec16) from both the A and B paths and shifts the them to 32 sample long delay line.

8.3.23 Polarity Inversion

The signal following the output delay can be inverted by a 2's complement conversion allowing the + and - DAC outputs to be swapped by asserting field DAC_COMPLEMENT in register MULTIDUC_CFG1 (8.5.13).

8.3.24 Temperature Sensor

The DAC38RF82 (or DAC38RF89) incorporates a temperature sensor block which monitors the die temperature by measuring the voltage across 2 transistors. The voltage is converted to an 8-bit digital word using a successive approximation (SAR) analog to digital conversion process. The result is scaled, limited and formatted as a twos complement value representing the temperature in degrees Celsius.

The sampling is controlled by the serial interface signals $\overline{\text{SDEN}}$ and SCLK. If the temperature sensor is enabled by writing a 0 to field TSENSE_SLEEP in register SLEEP_CONFIG (8.5.70), a conversion takes place each time the serial port is written or read. The data is only read and sent out by the digital block when the temperature sensor is read in field TEMPDATA in register TEMP_PLLVOLT (8.5.7). The conversion uses the first eight clocks of the serial clock as the capture and conversion clock, the data is valid on the falling eighth SCLK. The data is then clocked out of the chip on the rising edge of the ninth SCLK. No other clocks to the chip are necessary for the temperature sensor operation. As a result the temperature sensor is enabled even when the device is in sleep mode.

In order for the process described above to operate properly, the serial port read from register TEMP_PLLVOLT must be done with an SCLK period of at least 1 µs. If this is not satisfied the temperature sensor accuracy is greatly reduced.

8.3.25 Alarm Monitoring

The DAC38RF82 (or DAC38RF89) includes a flexible set of alarm monitoring that can be used to alert of a possible malfunction scenario. All the alarm events can be accessed either through the SIP registers and/or through the ALARM output. Once an alarm is set, the corresponding alarm bit must be reset through the serial interface to allow further testing. The set of alarms includes the following conditions:

- JESD alarms
  - Fields ALM_LANEx_ERR in registers JESD_ALM_Lx (x = 0-7, 8.5.59 to 8.5.66):
    - multiframe alignment_error. Occurs when multiframe alignment fails
    - frame alignment error. Occurs when multiframe alignment fails
    - link configuration error. Occurs when there is wrong link configuration
    - elastic buffer overflow. Occurs when bad RBD value is used
    - elastic buffer match error. Occurs when the first non-/K/ doesn't match the programmed data
    - code synchronization error

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  - 8b/10b not-in-table decode error
  - 8b/10b disparity error
  - Field ALM_FROM_SHORTTEST in register ALM_SYSREF_PAP (8.5.67): Occurs when the short pattern test fails.
- SerDes alarms
  - Field ALM_SD_LOTDET in register ALM_SD_DET 8.5.5): Occurs when there are loss of signal detect from SerDes lanes.
  - Fields ALM_FIFOx_FLAGS in registers JESD_ALM_Lx (x = 0-7, 8.5.59 to 8.5.66):
    - FIFO write error. Occurs if write request and FIFO is full.
    - FIFO write full: Occurs if FIFO is full.
    - FIFO read error. Occurs if read request and FIFO is empty.
    - FIFO read empty: Occurs if FIFO is empty.
  - Field ALM_SD0_PLL in register ALM_SYSREF_DET (8.5.6): Occurs if the PLL in the SerDes block 0 goes out of lock.
  - Field ALM_SD1_PLL in register ALM_SYSREF_DET (8.5.6): Occurs if the PLL in the SerDes block 1 goes out of lock.
- SYSREF alarm
  - Field ALM_SYSREF_ERR in register ALM_SYSREF_PAP (8.5.67): Occurs when the SYSREF is received at an unexpected time. If too many of these occur it will cause the JESD to go into synchronization mode again.
- DAC PLL alarm
  - Field PLL_LOCK in register ALM_SYSREF_DET (8.5.6). This register field is asserted when the PLL is unlocked. When used as an alarm output, a high signal indicates that the PLL is unlocked if the ALM_OUT_POL bit in register RESET_CONFIG is set to 1.
- PAP alarm
  - Field ALM_PAP in register ALM_SYSREF_PAP (8.5.67): Occurs when the average power is above the threshold. While any alarm_pap is asserted the attenuation for the appropriate data path is applied.

8.3.26 Differential Clock Inputs

Figure 45 shows the preferred configuration for driving the DACCLK+/- and SYSREF+/- with a differential ECL/PECL source.

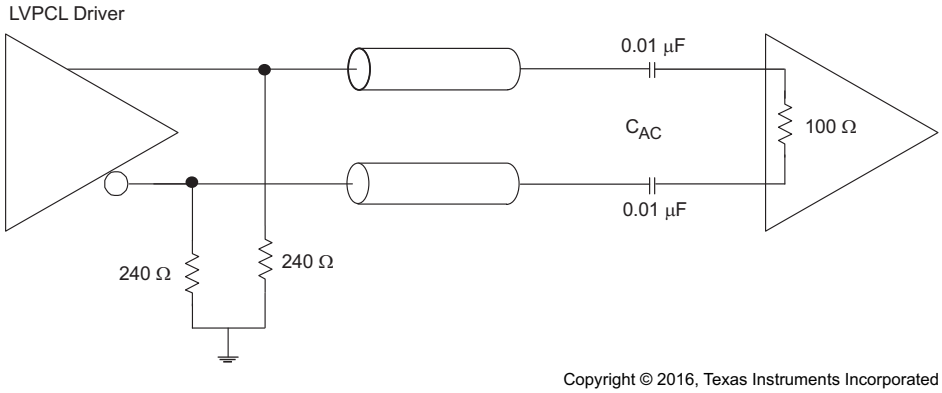

Figure 45. Preferred Clock Input Configuration With a Differential ECL/PECL Clock Source

8.3.27 CMOS Digital Inputs

Figure 46 shows a schematic of the equivalent CMOS digital inputs of the DAC38RF82 (or DAC38RF89). SDIO, SCLK, TCLK, SLEEP, TESTMODE and TXENABLE have internal pull-down resistors while SDEN, RESET, TMS, TDI and TRST have internal pull-up resistors. See the *Specifications* table for logic thresholds. The pull-up and pull-down circuitry is approximately equivalent to 10 kΩ.

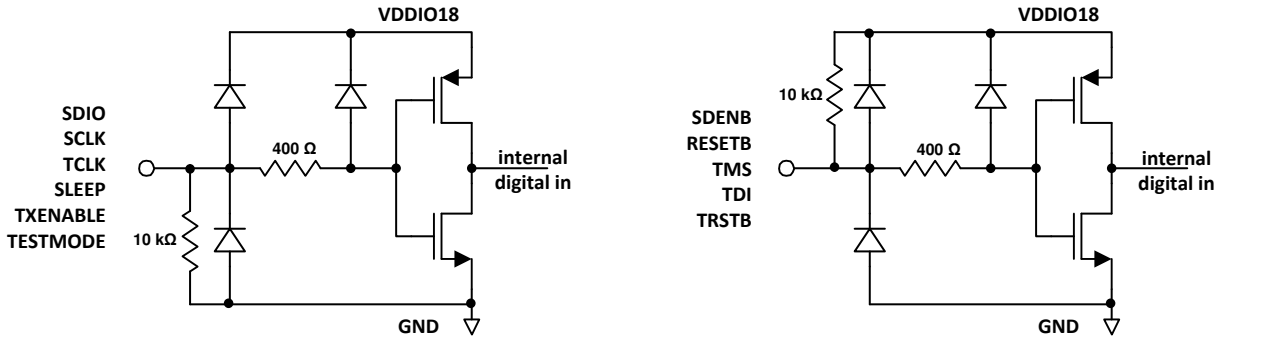

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Figure 46. CMOS Digital Equivalent Input

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8.3.28 DAC Fullscale Output Current

The DAC38RF82 (or DAC38RF89) uses a bandgap reference and control amplifier for biasing the full-scale output current. The DAC full scale output current is set by a combination of the fixed current through the external resistor RBIAS (connected to pin BIASJ) and current from course trim current sources:

$$IOUT_{FS} = I_{RBIAS} + I_{coarsetrim} \tag{8}$$

The bias current IBIAS through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage V_{BG} (nominally 0.9 V) and control amplifier. For normal operation, it is recommended that R_{BIAS} is set to 3.6 kΩ for a fixed current through R_{BIAS} of 250 µA. This current is scaled 128x internally, giving:

$$I_{RBIAS} = 128 \times \frac{V_{BG}}{R_{BIAS}} = 128 \times \frac{0.9V}{3.6\ k\Omega} = 32\ mA \tag{9}$$

The course trim current sources are configured through SPI register field DACFS in register DACFS (8.5.72), as follows:

$$I_{coarsetrim} = 2mA \times (DACFS - 11) \tag{10}$$

From the discussion above, the DAC full scale output current can be configured from 40 mA (DACFS[3:0] = 1111) down to 10 mA (DACFS[3:0] = 0000). In addition to the full scale signal current set by SPI register DACFS (8.5.72), an extra DC bias current is required to set the operating point of the output current sources(Table 45).

Table 45. DAC output current

DACFS (8.5.72)	Signal current (mA)	Total bias current (mA)(1)
0	10	1
1	12	1
2	14	2
3	16	2
4	18	3
5	20	3
6	22	4
7	24	5
8	26	5
9	28	6
10	30	6
11	32	7
12	34	7
13	36	8
14	38	8
15	40	9

(1) The bias current per each complementary output is half the total bias current

An external decoupling capacitor C_{EXT} of 0.1 µF should be connected externally to terminal EXTIO for compensation. The full-scale output current can be adjusted from 40 mA down to 10 mA by varying resistor R_{BIAS} From 3.6 kΩ to 14.4 kΩ.

8.3.29 Current Steering DAC Architecture

The DACs in the DAC38RF82 (or DAC38RF89) consist of a segmented array of NMOS current sources, capable of sinking a full-scale output current up to 40 mA (see Figure 47). Differential current switches direct the current to either one of the complimentary output nodes VOUT1/2+ or VOUT1/2-. Complimentary output currents enable differential operation, thus canceling out common mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, even order distortion components, and increasing signal output power by a factor of four.

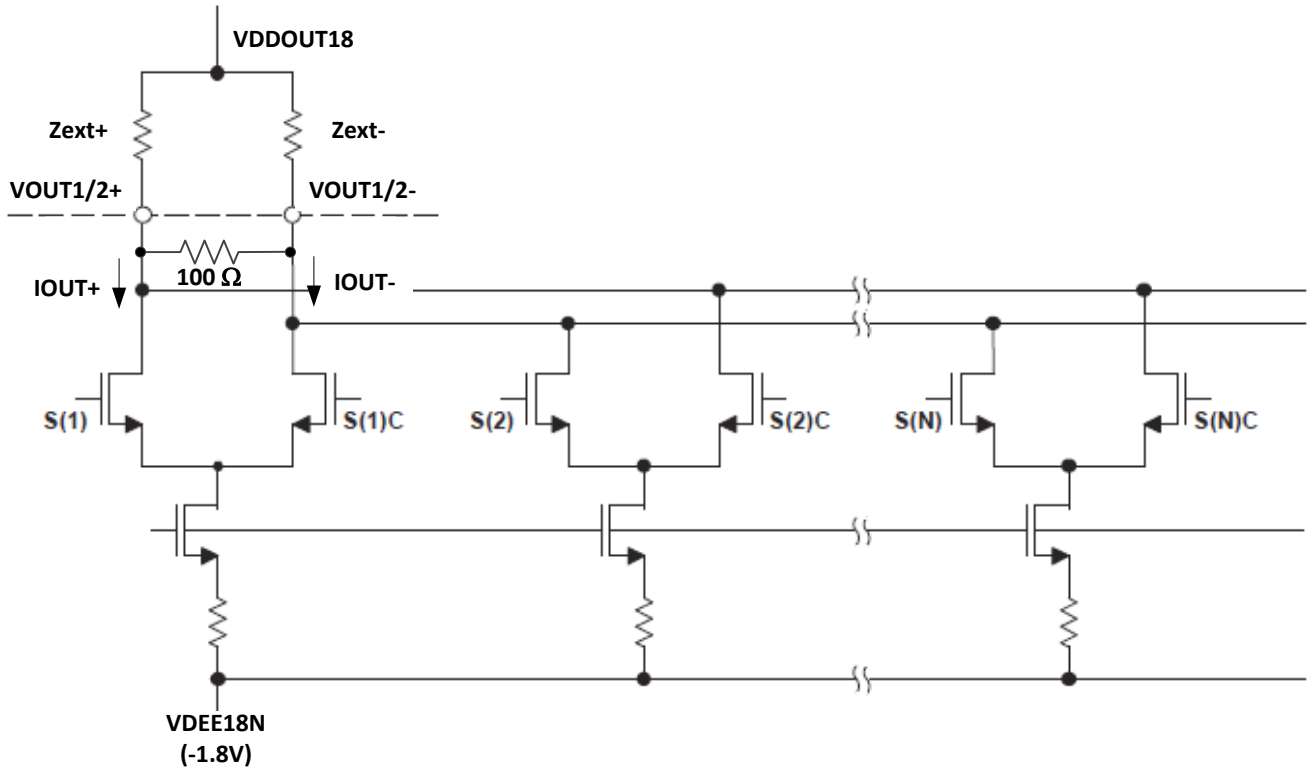

Figure 47. Current Steering DAC Architecture for DAC38RF82 (or DAC38RF89)

Referring to Figure 47, the total output current I_{OUTFS} is fixed, and is switched to either the + or – output by switches S(N):

$$IOUT_{FS} = IOUT+ + IOUT- \tag{11}$$

Since the output stage is a current sinking architecture, it will denote current into the DAC as + current, and the current flows IOUT+ and IOUT- into terminals VOUT1/2+ and VOUT1/2- respectively. IOUT+ and IOUT- can be expressed as:

$$IOUT+ = \frac{IOUT_{FS} \times CODE}{16384} \tag{12}$$

$$IOUT- = \frac{IOUT_{FS} \times (16383 - CODE)}{16384} \tag{13}$$

where CODE is the decimal representation of the 14-bit DAC core data input word. Note the signal path up to the DAC is 16-bits and the 2 LSBs are truncated for the DAC core data input word.

8.3.30 DAC Transfer Function

The DAC38RF82 (or DAC38RF89) has a differential output and is terminated internally with a differential 100-Ω load. The DAC38RF82 (or DAC38RF89) output compliance range is 1.3 to 2.3 V. Note that care should be taken not to exceed the compliance voltages at node VOUT1/2+ and VOUT1/2-, which would lead to increased signal distortion.

Referring again to Figure 47, denote the external impedance as seen by VOUT1/2+ as Zext+ and by VOUT1/2- as Zext-. Note that Zext+ and Zext- should terminate to VDDOUT18 to supply the output current for the DAC. Also, Zext+ and Zext- are ideally identical to maintain the differential balance of the output. The voltage at nodes VOUT1/2+ and VOUT1/2- generated by the current flow through the impedance is

$$VOUT1/2+ = \frac{IOUT+ \times (100\Omega + Zext+)}{(100\Omega + Zext+ + Zext-)} \times Zext+ + \frac{IOUT- \times Zext-}{(100\Omega + Zext+ + Zext-)} \times Zext+ \tag{14}$$

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$$VOUT1/2- = \frac{IOUT- \times (100\Omega + Zext-)}{(100\Omega + Zext+ + Zext-)} \times Zext+ + \frac{IOUT+ \times Zext+}{(100\Omega + Zext+ + Zext-)} \times Zext- \quad (15)$$

The DAC38RF82 (or DAC38RF89) can be easily configured to drive a doubly terminated 50-Ω cable using a properly selected 2:1 RF transformer (Figure 48). Note that the center tap of the primary input of the transformer has to be connected to the VDDOUT18 supply (nominally 1.8 V) to enable a DC current flow into the DAC. The AC load impedance as seen through 2:1 transformer is 100 Ω, which is split equally into Zext+ = Zext- = 50 Ω. The DC impedance for the transformer is a short to the center tap of the transformer, which drives the common mode of VOUT1/2+ and VOUT1/2- to 1.8V. To calculate the peak to peak output swing VOUT1/2PP at each node, the equations above simplify to:

$$VOUT1/2_{PP} = VOUT1/2+\Big|_{(IOUT+=IOUT_{FS}, IOUT-=0)} - VOUT1/2+\Big|_{(IOUT-=IOUT_{FS}, IOUT+=0)} \quad (16)$$

$$VOUT1/2_{PP} = \frac{IOUT_{FS} \times 50\Omega \times 150\Omega}{200\Omega} - \frac{IOUT_{FS} \times 50\Omega \times 50\Omega}{200\Omega} = IOUT_{FS} \times 25\Omega \quad (17)$$

With $IOUT_{OUTFS}$ = 40 mA, the swing becomes 1 V_{PP} at each node. With the common mode at 1.8 V due to the center tap, the voltage at VOUT1/2+ and VOUT1/2- varies between 1.3 and 2.3 V, which is the compliance range of the DAC.

The differential output swing is 2x $VOUT1/2_{PP}$, or 2 V_{PPDIFF}. On the load side of the transformer, this reduces to 1.414 V_{PP}, for a transferred load power of 7 dBm (assuming no loss).

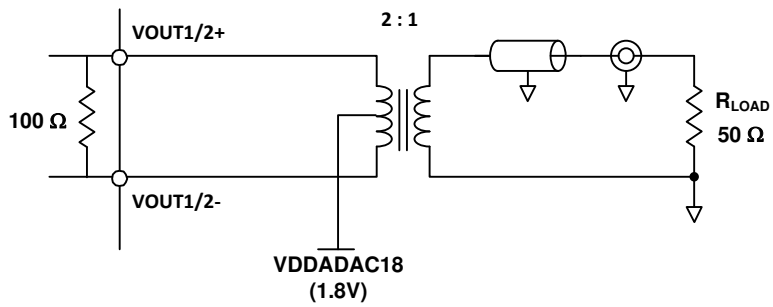

Figure 48. Driving a 50-Ω Load Using a 2:1 Impedance Ratio Transformer (DAC38RF82 (or DAC38RF89))

The DAC38RF82 (or DAC38RF89) can also be DC coupled. In this case, the termination voltage can be raised above 1.8 V (for example 2.3 V) so that the common mode for the output pin is nominally 1.8 V.

8.4 Device Functional Modes

8.4.1 Clocking Modes

The DAC38RF82 (or DAC38RF89) has both a single ended clock input DACCLKSE and a differential clock input DACCLK+/- to clock the device. The clock input is selected by field SEL_EXTCLK_DIFFSE in register CLK_PLL_CFG (8.5.79). The DAC38RF82 (or DAC38RF89) can be clock directly with a high frequency input clock at the DAC sample rate (PLL Bypass Mode), or an optional on-chip low-jitter phase-locked loop (PLL) can be used to generate the high frequency DAC sample clock internally from a lower frequency reference clock input (PLL Mode).

8.4.2 PLL Bypass Mode Programming

In PLL bypass mode a high quality clock is sourced to the DACCLK inputs. This clock is used to directly clock the DAC38RF82 (or DAC38RF89) DAC cores. This mode gives the device best performance and is recommended for extremely demanding applications.

The bypass mode is selected by setting the following:

1. Set field PLL_ENA in register CLK_PLL_CFG (8.5.79) to “0” to bypass the PLL circuitry.
2. Set field PLL_SLEEP in register SLEEP_CONFIG (8.5.70) to “1” to put the PLL and VCO into sleep mode.

Device Functional Modes (continued)

8.4.3 Internal PLL/VCO

The DAC38RF82 (or DAC38RF89) has an internal clock generation circuit consisting of a PLL and two selectable VCOs, as shown in Figure 49.

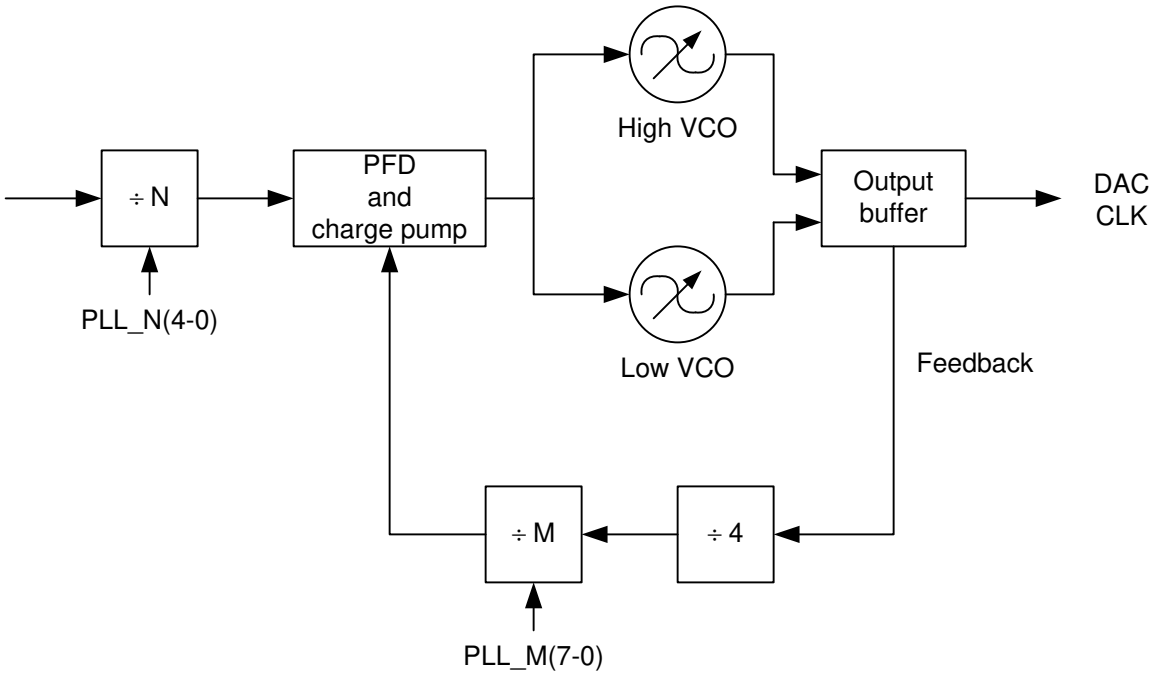

Figure 49. Internal PLL/VCO Block Diagram

DAC38RF82 (or DAC38RF89) each have a low VCO (VCO0) and high VCO (VCO1), but they are tuned to different center frequencies in each device. The VCO frequency ranges for each device are summarized in Electrical Characteristics - Digital Specifications. The VCO is selected through field PLL_VCOSEL in register PLL_CONFIG2 (8.5.81), with '0' selecting the low VCO and a '1' the high VCO. The 7 bit VCO tuning code in field PLL_VCO in register PLL_CONFIG2 (8.5.81) is used to tune the VCO frequency from the lowest frequency in the range to the highest frequency for the particular VCO used. For the low VCO the center VCO frequency is achieved with PLL_VCO = $63_{decimal}$ and for the high VCO the center frequency is achieved with PLL_VCO = $63_{decimal}$.

The supply current, and therefore; the analog signal amplitude in the VCO is controlled using the field PLL_VCO_RDAC in register PLL_CONFIG1 (8.5.80). This control signal should be set $15_{decimal}$ initially for 18 mA supply current in the VCO and ~1.4 V_{PP} single ended oscillation amplitude.

The PLL has no prescaler, so the DAC sample rate is the VCO frequency. In the PLL feedback path a fixed ÷ 4 frequency divider block receives the VCO output clock and divides its frequency by 4. The maximum operating frequency of the phase-frequency detector (PFD) and charge pump (CP) requires this. The M (feedback) clock divider takes the output clock signal from the fixed ÷4 block and divides it by a programmable ratio set by the 8-bit field in field PLL_M_M1 in register PLL_CONFIG1 (8.5.80). The programmable division ratio range is ÷1 to ÷256, and is the value of the 8 bit unsigned binary code + 1. Although it is possible to program the M divider to ÷1, ÷2 and ÷3, these values should not be used. As stated previously the PFD and CP have a finite maximum operating frequency, which is the VCO frequency divided by the fixed divider ratio multiplied by the minimum allowable M divider ratio.

$$PFD_CP_{Fmax} = Fvco / (Fixed_div \times Mdiv_{min}) \tag{18}$$

The N (reference) divider determines the ratio between the input reference clock frequency and the PFD operating frequency, and is set by the 5-bit field PLL_N_M1 in register CLK_PLL_CFG (8.5.79). The division ratio range is ÷1 to ÷32, and is the value of the 5-bit unsigned binary code + 1.

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Device Functional Modes (continued)

The charge pump output current amplitude is set using the 4-bit field PLL_CP_ADJ in in register PLL_CONFIG2 (8.5.81). The current amplitude is simply the digital code multiplied by the unit current amplitude of 100 µA. In a nominal condition, with the DAC38RF82 VCO0 running at 5.898 GHz, and with the M divider set to ÷4, the PFD will run at 368.625 MHz, and the change pump current should set to $6_{decimal}$, which gives 600 µA charge pump output current for a good phase margin of 69 degrees. If a higher M ratio (for lower PFD frequencies) are required the charge pump output current must be increased to maintain good loop stability and prevent excessive peaking in the phase noise response. The charge pump output current setting PLL_CP_ADJ should be adjusted in relation to the feedback (M) divider ratio PLL_M_M1 according to the following table to maintain a constant phase margin of 69 degrees.

Table 46. M vs Kp for Maintaining Good Stability

M	CP_ADJ
4	6
6	9
8	12
10	15

Similarly for the DAC38RF82 VCO2 running at 8.847 GHz, and with the M divider set to ÷4, the PFD will run at 552.9375 MHz as shown above. Here the change pump current should set to $6_{decimal}$, which gives 600 µA charge pump output current for a good phase margin of 69 degrees.

8.4.4 CLKOUT

The DAC38RF82 (or DAC38RF89) has a programmable output clock on CLKTX+/- balls that is a divided version of the internal DAC sample clock, either with or without PLL. Two frequency dividers, either DACCLK/3 or DACCLK/4, are available by programming field CLK_TX_DIV4 in register CLK_OUT (8.5.71). The output swing voltage is programmable from approximately 125 to 1460 $mV_{PP\text{-}DIFF}$ through field CLK_TX_SWING in register CLK_OUT (8.5.71).

Field CLK_TX_IDLE in register CLK_OUT (8.5.71) enables an idle state, in which the pins are driven to the proper common-mode levels in order to charge the external AC coupling caps but the clock output is disabled. The output clock circuit can be put to sleep by field CLK_TX_SLEEP in register SLEEP_CONFIG (8.5.70).

8.4.5 Serial Peripheral Interface (SPI)

The serial port of the DAC38RF82 (or DAC38RF89) is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of DAC38RF82 (or DAC38RF89). It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 terminal interface by SIF4_ENA in register IO_CONFIG (8.5.2). In both configurations, SCLK is the serial interface input clock and $\overline{SDEN}$ is serial interface enable. For 3 terminal configuration, SDIO is a bidirectional terminal for both data in and data out. For 4 terminal configuration, SDIO is bidirectional and SDO is data out only. Data is input into the device with the rising edge of SCLK. Data is output from the device on the falling edge of SCLK.

The SPI registers are reset by writing a 1 to SPI_RESET in register RESET_CONFIG (8.5.1).

Each read/write operation is framed by signal $\overline{SDEN}$ (Serial Data Enable Bar) asserted low. The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write as well as the 7-bit address to be accessed. Figure 50 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. The data transfer cycle consists of two bytes.

Figure 50. Instruction Byte of the Serial Interface

Bit	7 (MSB)	6	5	4	3	2	1	0
Description	R/W	A6	A5	A4	A3	A2	A1	A0

R/W - Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC38RF82 (or DAC38RF89) and a low indicates a write operation to DAC38RF82 (or DAC38RF89)

A6:A0 - Identifies the address of the register to be accessed during the read or write operation.

Figure 51 shows the serial interface timing diagram for a DAC38RF82 (or DAC38RF89) write operation. SCLK is the serial interface clock input to DAC38RF82 (or DAC38RF89). Serial data enable SDEN is an active low input to DAC38RF82 (or DAC38RF89). SDIO is serial data input. Input data to DAC38RF82 (or DAC38RF89) is clocked on the rising edges of SCLK.

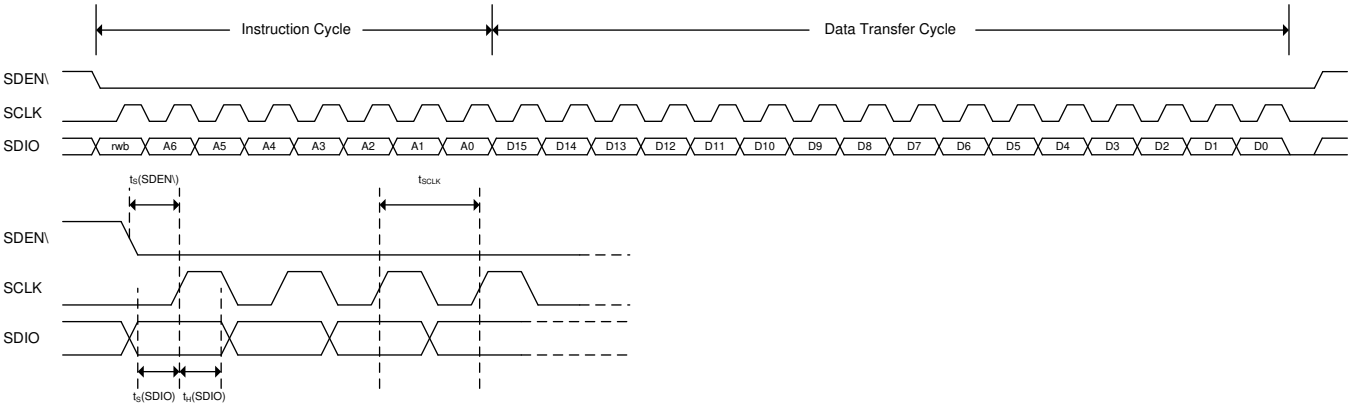

Figure 51. Serial Interface Write Timing Diagram

Figure 52 shows the serial interface timing diagram for a DAC38RF82 (or DAC38RF89) read operation. SCLK is the serial interface clock input to DAC38RF82 (or DAC38RF89). Serial data enable SDEN is an active low input to DAC38RF82 (or DAC38RF89). SDIO is serial data input during the instruction cycle. In 3 pin configuration, SDIO is data out from the DAC38RF82 (or DAC38RF89) during the data transfer cycle, while SDO is in a high-impedance state. In 4 pin configuration, both SDIO and SDO are data out from the DAC38RF82 (or DAC38RF89) during the data transfer cycle. At the end of the data transfer, SDIO and SDO will output low on the final falling edge of SCLK until the rising edge of SDEN when they will 3-state.

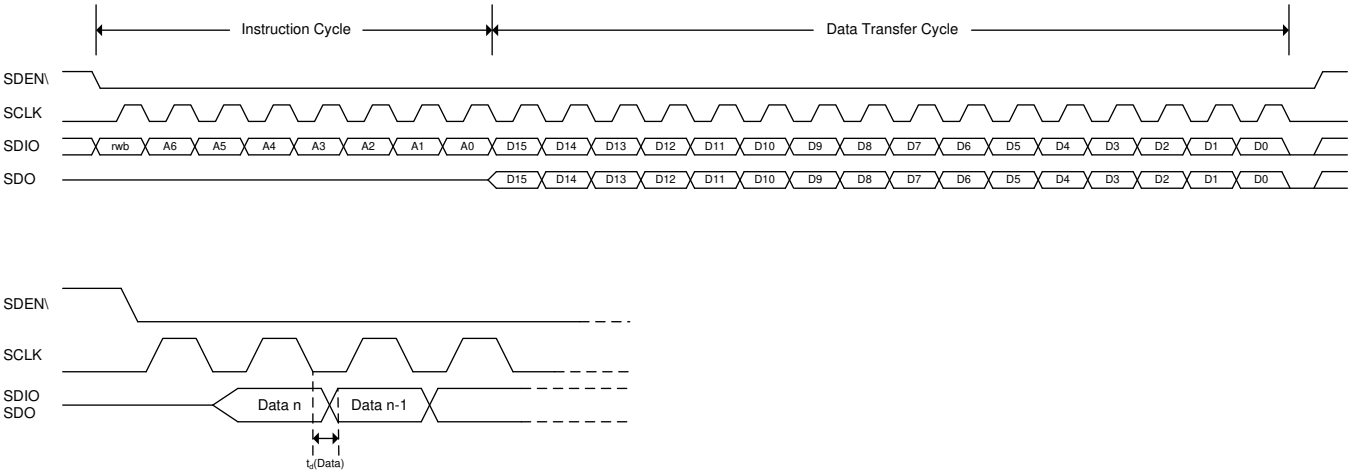

Figure 52. Serial Interface Read Timing Diagram

n the SIF interface there are four types of registers:

8.4.5.1 NORMAL (RW)

The NORMAL register type allows data to be written and read from. All 16-bits of the data are registered at the same time. There is no synchronizing with an internal clock thus all register writes are asynchronous with respect to internal clocks. There are three subtypes of NORMAL:

1. AUTOSYNC: A NORMAL register that causes a sync to be generated after the write is finished. These are used when it is desirable to synchronize the block after writing the register or if a single field that spans across multiple registers. For instance, the NCO requires three 16-bit register writes to set the frequency. Upon writing the last of these registers an autosync is generated to deliver the entire field to the NCO block

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at once, rather than in pieces after each individual register write. For a field that spans multiple registers, all non-AUTOSYNC registers for the field must be written first before the actual AUTOSYNC register.

2. No RESET Value: These are NORMAL registers, but the reset value cannot be specified. This could be because the register has some read only bits or some internal logic partially controls the bit values.
3. READ_ONLY (R): Registers that can only be read.

8.4.5.2 WRITE_TO_CLEAR (W0C)

These registers are just like NORMAL registers with one exception. They can be written and read, however, when the internal logic asynchronously sets a bit high in one of these registers, that bit stays high until it is written to '0'. This way interrupts will be captured and stay constant until cleared by the user.

8.5 Register Maps

Table 47. Register Summary

Address	Reset	Acronym	Register Name	Section
General Configuration Registers (PAGE_SET[2:0] = 000)				
0x00	0x5803	RESET_CONFIG	Chip Reset and Configuration	8.5.1
0x01	0x1800	IO_CONFIG	IO Configuration	8.5.2
0x02	0xFFFF	ALM_SD_MASK	Lane Signal Detect Alarm Mask	8.5.3
0x03	0xFFFF	ALM_CLK_MASK	Clock Alarms Mask	8.5.4
0x04	0x0000	ALM_SD_DET	SERDES Loss of Signal Detection Alarms	8.5.5
0x05	0x0000	ALM_SYSREF_DET	SYSREF Alignment Circuit Alarms	8.5.6
0x06	variable	TEMP_PLLVOLT	Temperature Sensor and PLL Loop Voltage	8.5.7
0x07-0x08	0x0000	Reserved	Reserved	
0x09	0x0000	PAGE_SET	Page Set	8.5.8
0x0A-0x77	0x0000	Reserved	Reserved	
0x78	0x0000	SYSREF_ALIGN_R	SYSERF Align to r1 and r3 Count	8.5.9
0x79	0x0000	SYSREF12_CNT	SYSREF Phase Count 1 and 2	8.5.10
0x7A	0x0000	SYSREF34_CNT	SYSREF Phase Count 3 and 4	8.5.11
0x7B-0x7E	0x0000	Reserved	Reserved	
0x7F	0x0008	VENDOR_VER	Vendor ID and Chip Version	8.5.12
Multi-DUC Configuration Registers (PAGE_SET[0] = 1 for multi-DUC1, PAGE_SET[1] = 1 for multi-DUC2)				
0x0A	0x02B0	MULTIDUC_CFG1	Multi-DUC Configuration (PAP, Interpolation)	8.5.13
0x0B	0x0000	Reserved	Reserved	
0x0C	0x2402	MULTIDUC_CFG2	Multi-DUC Configuration (Mixers)	8.5.14
0x0D	0x8300	JESD_FIFO	JESD FIFO Control	8.5.15
0x0E	0x00FF	ALM_MASK1	Alarm Mask 1	8.5.16
0x0F	0x1F83	ALM_MASK2	Alarm Mask 2	8.5.17
0x10	0xFFFF	ALM_MASK3	Alarm Mask 3	8.5.18
0x11	0xFFFF	ALM_MASK4	Alarm Mask 4	8.5.19
0x12	0x0000	JESD_LN_SKEW	JESD Lane Skew	8.5.20
0x13-0x16	0x0000	Reserved	Reserved	
0x17	0x0000	CMIX	CMIX Configuration	8.5.21
0x18	0x0000	Reserved	Reserved	
0x19	0x0000	OUTSUM	Output Summation and Delay	8.5.22
0x1A-0x1B	0x0000	Reserved	Reserved	
0x1C	0x0000	PHASE_NCOAB	Phase offset for AB path NCO	8.5.23
0x1D	0x0000	PHASE_NCOCD	Phase offset for CD path NCO	8.5.24
0x1E-0x20	0x0000	FREQ_NCOAB	Frequency for AB path NCO	8.5.25
0x21-0x23	0x0000	FREQ_NCOCD	Frequency for CD path NCO	8.5.26
0x24	0x0010	SYSREF_CLKDIV	SYSREF Use for Clock Divider	8.5.27
0x25	0x7700	SERDES_CLK	Serdes Clock Control	8.5.28
0x26	0x0000	Reserved	Reserved	

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Register Maps (continued)

Table 47. Register Summary (continued)

Address	Reset	Acronym	Register Name	Section
0x27	0x1144	SYNCSEL1	Sync Source Selection	8.5.29
0x28	0x0000	SYNCSEL2	Sync Source Selection	8.5.30
0x29	0x0000	PAP_GAIN_AB	PAP path AB Gain Attenuation Step	8.5.31
0x2A	0x0000	PAP_WAIT_AB	PAP path AB Wait Time at Gain = 0	8.5.32
0x2B	0x0000	PAP_GAIN_CD	PAP path CD Gain Attenuation Step	8.5.33
0x2C	0x0000	PAP_WAIT_CD	PAP path CD Wait Time at Gain = 0	8.5.34
0x2D	0x1FFF	PAP_CFG_AB	PAP path AB Configuration	8.5.35
0x2E	0x1FFF	PAP_CFG_CD	PAP path CD Configuration	8.5.36
0x2F	0x0000	SPIDAC_TEST1	Configuration for DAC SPI Constant	8.5.37
0x30	0x0000	SPIDAC_TEST2	DAC SPI Constant	8.5.38
0x31	0x0000	Reserved	Reserved	
0x32	0x0800	GAINAB	Gain for path AB	8.5.39
0x33	0x0800	GAINCD	Gain for path CD	8.5.40
0x34-0x40	0x0000	Reserved	Reserved	
0x41	0x0000	JESD_ERR_CNT	JESD Error Counter	8.5.41
0x42-0x45	0x0000	Reserved	Reserved	
0x46	0x0044	JESD_ID1	JESD ID 1	8.5.42
0x47	0x190A	JESD_ID2	JESD ID 2	8.5.43
0x48	0x31C3	JESD_ID3	JESD ID 3 and Subclass	8.5.44
0x49	0x0000	Reserved	Reserved	
0x4A	0x0003	JESD_LN_EN	JESD Lane Enable	8.5.45
0x4B	0x1300	JESD_RBD_F	JESD RBD Buffer and Frame Octets	8.5.46
0x4C	0x1303	JESD_K_L	JESD K and L Parameters	8.5.47
0x4D	0x0100	JESD_M_S	JESD M and S Parameters	8.5.48
0x4E	0x0F4F	JESD_N_HD_SCR	JESD N, HD and SCR Parameters	8.5.49
0x4F	0x1CC1	JESD_MATCH	JESD Character Match and Other	8.5.50
0x50	0x0000	JESD_LINK_CFG	JESD Link Configuration Data	8.5.51
0x51	0x00FF	JESD_SYNC_REQ	JESD Sync Request	8.5.52
0x52	0x00FF	JESD_ERR_OUT	JESD Error Output	8.5.53
0x53	0x0100	JESD_ILA_CFG1	JESD Configuration Value used for ILA Check	8.5.54
0x54	0x8E60	JESD_ILA_CFG2	JESD Configuration Value used for ILA Check	8.5.55
0x55-0x5B	0x0000	Reserved	Reserved	
0x5C	0x0001	JESD_SYSR_MODE	JESD SYSREF Mode	8.5.56
0x5D-0x5E	0x0000	Reserved	Reserved	
0x5F	0x0123	JESD_CROSSBAR1	JESD Crossbar Configuration 1	8.5.57
0x60	0x4567	JESD_CROSSBAR2	JESD Crossbar Configuration 2	8.5.58
0x61-0x63	0x0000	Reserved	Reserved	
0x64	0x0000	JESD_ALM_L0	JESD Alarms for Lane 0	8.5.59
0x65	0x0000	JESD_ ALM_L1	JESD Alarms for Lane 1	8.5.60
0x66	0x0000	JESD_ ALM_L2	JESD Alarms for Lane 2	8.5.61
0x67	0x0000	JESD_ALM_L3	JESD Alarms for Lane 3	8.5.62
0x68	0x0000	JESD_ALM_L4	JESD Alarms for Lane 4	8.5.63
0x69	0x0000	JESD_ALM_L5	JESD Alarms for Lane 5	8.5.64
0x6A	0x0000	JESD_ALM_L6	JESD Alarms for Lane 6	8.5.65
0x6B	0x0000	JESD_ALM_L7	JESD Alarms for Lane 7	8.5.66
0x6C	0x0000	ALM_SYSREF_PAP	SYSREF and PAP Alarms	8.5.67
0x6D	0x0000	ALM_CLKDIV1	Clock Divider Alarms 1	8.5.68
0x6E-0x77	0x0000	Reserved	Reserved	

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Register Maps (continued)

Table 47. Register Summary (continued)

Address	Reset	Acronym	Register Name	Section
Miscellaneous Configuration Registers (PAGE_SET[1:0] = 00, PAGE_SET[2] = 1)				
0x0A	0xFC03	CLK_CONFIG	Clock Configuration	8.5.69
0x0B	0x0022	SLEEP_CONFIG	Sleep Configuration	8.5.70
0x0C	0xA002	CLK_OUT	Divided Output Clock Configuration	8.5.71
0x0D	0xF000	DACFS	DAC Fullscale Current	8.5.72
0x0E-0x0F	0x0000	Reserved	Reserved	
0x10	0x0000	LCMGEN	Internal sysref generator	8.5.73
0x11	0x0000	LCMGEN_DIV	Counter for internal sysref generator	8.5.74
0x12	0x0000	LCMGEN_SPISYSREF	SPI SYSREF for internal sysref generator	8.5.75
0x13-0x1A	0x0000	Reserved	Reserved	
0x1B	0x0000	DTEST	Digital Test Signals	8.5.76
0x1C-0x22	0x0000	Reserved	Reserved	
0x23	0x03F3	SLEEP_CNTL	Sleep Pin Control	8.5.77
0x24	0x1000	SYSR_CAPTURE	SYSREF Capture Circuit Control	8.5.78
0x25-0x30	0x0000	Reserved	Reserved	
0x31	0x0200	CLK_PLL_CFG	Clock Input and PLL Configuration	8.5.79
0x32	0x0308	PLL_CONFIG1	PLL Configuration 1	8.5.80
0x33	0x4018	PLL_CONFIG2	PLL Configuration 2	8.5.81
0x34	0x0000	LVDS_CONFIG	LVDS Output Configuration	8.5.82
0x35	0x0018	PLL_FDIV	Fuse farm clock divider	8.5.83
0x36-0x3A	0x0000	Reserved	Reserved	
0x3B	0x0002	SRDS_CLK_CFG	Serdes Clock Configuration	8.5.84
0x3C	0x8228	SRDS_PLL_CFG	Serdes PLL Configuration	8.5.85
0x3D	0x0088	SRDS_CFG1	Serdes Configuration 1	8.5.86
0x3E	0x0909	SRDS_CFG2	Serdes Configuration 2	8.5.87
0x3F	0x0000	SRDS_POL	Serdes Polarity Control	8.5.88
0x40-0x75	0x0000	Reserved	Reserved	
0x76	0x0000	SYNCBOUT	JESD204B SYNCB Output	8.5.89

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8.5.1 Chip Reset and Configuration Register (address = 0x00) [reset = 0x5803]

Figure 53. Chip Reset and Configuration Register (RESET_CONFIG)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
RW	RW	RW	RW	RW	RW	RW	RW
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 48. RESET_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
15	SPI_RESET	RW	0	This will reset all the SPI registers once programmed.
14	ALM_OUT_POL	RW	1	Changes the polarity of the alarm output. 0= active low 1= active high
13	ALM_OUT_ENA	RW	0	Turn on the alarm pin
12	SYSCLK_ENA	RW	1	Turns on the dividers for the SYSCLK to the Fusefarm
11	AUTOLOAD_TRIG	RW	1	Causes a Fuse AUTOLOAD to be executed.
10:7	Reserved	RW	0000	Reserved
6	ONE_DAC_ONLY	RW	0	When set high only the SLICE0 is available.
5	ONE_LINK_ONLY	RW	0	This needs to be set high when a single link setup is being programmed to get the correct TXENABLE signal generation
4:2	Reserved	RW	000	Reserved
1	INIT_SLICE1	RW	1	Puts the multi-DAC2 JESD into initialization state
0	INIT_SLICE0	RW	1	Puts the multi-DAC1 JESD into initialization state

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8.5.2 IO Configuration Register (address = 0x01) [reset = 0x1800]

Figure 54. IO Configuration Register (IO_CONFIG)

15	14	13	12	11	10	9	8
0	0	0	1	1	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 49. IO_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
15:14	GPO0_SEL	RW	00	Selects the JESD SYNC_N signal coming out the GPO0 pin. Both bits can be asserted which does an oring of the SYNC_N signals from each multi-DUC. bit 0 = 1 then multi-DUC1 SYNC_N used bit 1 = 1 then multi-DUC2 SYNC_N is used
13:12	SYNC0B_SEL	RW	01	Selects the JESD SYNC_N signal coming out the SYNC0B pin. Both bits can be asserted which does an oring of the SYNC_N signals from each multi-DUC. bit 0 = 1 then multi-DUC1 SYNC_N used bit 1 = 1 then multi-DUC2 SYNC_N is used
11:10	SYNC1B_SEL	RW	10	Selects the JESD SYNC_N signal coming out the SYNC1B pin. Both bits can be asserted which does an oring of the SYNC_N signals from each multi-DUC. bit 0 = 1 then multi-DUC1 SYNC_N used bit 1 = 1 then multi-DUC2 SYNC_N is used
9:8	GPO1_SEL	RW	00	Selects the JESD SYNC_N signal coming out the GPO1 pin. Both bits can be asserted which does an oring of the SYNC_N signals from each multi-DUC. bit 0 = 1 then multi-DUC1 SYNC_N used bit 1 = 1 then multi-DUC2 SYNC_N is used
7	SPI4_ENA	RW	0	When set to a '1' the chip is in 4 pin SPI interface mode.
6	Reserved	RW	0	Reserved
5:0	ATEST	RW	000000	Select the analog test points: 000000: ATEST is off (ATEST Must be off during normal operation) 000001, 010001, 000110: *VSSCLK* 000010: *VDDPLL1* 000101: *VDDCLK* 000111, 001010, 010000: *VDDAPLL18* 001011: *VDDAVCO18* 001101: *VDDS18* 001110: *VDDE1* 001111, 111010, 111011, 111100: *DGND* 010011: *VDDTX1* 101001, 110001: *AGND* 101111, 111101, 111110, 11111: *VDDDIG1* 110000: *VDDA18*

8.5.3 Lane Single Detect Alarm Mask Register (address = 0x02) [reset = 0xFFFF]

Figure 55. Lane Single Detect Alarm Mask Register (ALM_SD_MASK)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 50. ALM_SD_MASK Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ALM_SD_MASK	R/W	0xFFFF	Used to mask alarms bit 15 - bit 8 : Reserved bit7 : lane 7 loss of signal detect bit6 : lane 6 loss of signal detect bit5 : lane 5 loss of signal detect bit4 : lane 4 loss of signal detect bit3 : lane 3 loss of signal detect bit2 : lane 2 loss of signal detect bit1 : lane1 loss of signal detect bit0 : lane 0 loss of signal detect

8.5.4 Clock Alarms Mask Register (address = 0x03) [reset = 0xFFFF

Figure 56. Clock Alarms Mask Register (ALM_CLK_MASK)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 51. ALM_CLK_MASK Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ALM_CLK_MASK	R/W	0xFFFF	Used to mask alarms bit 15 - bit 8 : Reserved bit 7 : alarm_sysrefphase4 bit 6 : alarm_sysrefphase3 bit 5 : alarm_sysrefphase2 bit 4 : alarm_sysrefphase1 bit 3 : alarm_align_to_r3 bit 2 : alarm_align_to_r1 bit 1 : alarm_sd0_pll bit 0 : alarm_sd1_pll

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8.5.5 SERDES Loss of Signal Detection Alarms Register (address = 0x04) [reset = 0x0000]

Figure 57. SERDES Loss of Signal Detection Alarms Register (ALM_SD_DET)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset

Table 52. ALM_SD_DET Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	W0C	0x00	Reserved
7:0	ALM_SD_LOSDET	W0C	0x00	Loss of signal detect outputs from the SERDES lanes: bit 7 = lane7 loss of signal bit 6 = lane6 loss of signal bit 5 = lane5 loss of signal bit 4 = lane4 loss of signal bit 3 = lane3 loss of signal bit 2 = lane2 loss of signal bit 1 = lane1 loss of signal bit 0 = lane0 loss of signal

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8.5.6 SYSREF Alignment Circuit Alarms Register (address = 0x05) [reset = 0x0000]

Figure 58. SYSREF Alignment Circuit Alarms Register (ALM_SYSREF_DET)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset

Table 53. ALM_SYSREF_DET Field Descriptions

Bit	Field	Type	Reset	Description
15:9	Reserved	W0C	0000000	Reserved
8	ALM_SYSRPHASE4	W0C	0	If high the sysrefphase4 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync.
7	ALM_SYSRPHASE3	W0C	0	If high the sysrefphase3 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync.
6	ALM_SYSRPHASE2	W0C	0	If high the sysrefphase2 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync.
5	ALM_SYSRPHASE1	W0C	0	If high the sysrefphase1 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync.
4	ALM_ALIGN_TO_R3	W0C	0	If high the align_to_r3 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync. TI Internal use only.
3	ALM_ALIGN_TO_R1	W0C	0	If high the align_to_r1 state has been observed in the sysrefalign logic at least once since the last sysrefalign sync. TI Internal use only.
2	ALM_SD0_PLL	W0C	0	Driven high if the PLL in the Serdes 0 block goes out of lock. A false alarm is generated at startup when the PLL is locking. User will have to reset this bit after start to monitor accurately.
1	ALM_SD1_PLL	W0C	0	Driven high if the PLL in the Serdes 1 block goes out of lock. A false alarm is generated at startup when the PLL is locking. User will have to reset this bit after start to monitor accurately.
0	PLL_LOCK	W0C	0	Asserted when PLL is unlocked.

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8.5.7 Temperature Sensor and PLL Loop Voltage Register (address = 0x06) [reset = variable]

Figure 59. Temperature Sensor and PLL Loop Voltage Register (TEMP_PLLVOLT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 54. TEMP_PLLVOLT Field Descriptions

Bit	Field	Type	Reset	Description
15:8	TEMPDATA	R	0x00	8 bits of data from the tempurature sensor
7:5	PLL_LFVOLT	R	0b000	PLL Loop filter voltage
4:0	Reserved	R	0b000	Reserved

8.5.8 Page Set Register (address = 0x09) [reset = 0x0000]

Figure 60. Page Set Register (PAGE_SET)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 55. PAGE_SET Field Descriptions

Bit	Field	Type	Reset	Description
15:0	PAGE_SET	R/W	0x0000	Each bit selects a page that is active. Multiple pages can be selected at the same time. No bits asserted means that MASTER is the only page selected. bit 0 = page0 : multi-DUC1 bit 1 = page1 : multi-DUC2 bit 2 = page2 : DIG_MISC bit 3-15: Reserved

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8.5.9 SYSREF Align to r1 and r3 Count Register (address = 0x78) [reset = 0x0000]

Figure 61. SYSREF Align to r1 and r3 Count Register (SYSREF_ALIGN_R)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	1	1	1	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 56. SYSREF_ALIGN_R Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALIGN_TO_R1_CNT	R	0x00	Part of the SYSREF Align block
7:0	ALIGN_TO_R3_CNT	R	0x00	Part of the SYSREF Align block

8.5.10 SYSREF Phase Count 1 and 2 Register (address = 0x79) [reset = 0x0000]

Figure 62. SYSREF Phase Count 1 and 2 Register (SYSREF12_CNT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	1	1	1	0	0	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 57. SYSREF12_CNT Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE2_CNT	R	0x00	Part of the SYSREF Align block
7:0	PHASE1_CNT	R	0x00	Part of the SYSREF Align block

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8.5.11 SYSREF Phase Count 3 and 4 Register (address = 0x7A) [reset = 0x0000]

Figure 63. SYSREF Phase Count 3 and 4 Register (SYSREF34_CNT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	1	1	1	0	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 58. SYSREF34_CNT Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE4_CNT	R	0x00	Part of the SYSREF Align block
7:0	PHASE3_CNT	R	0x00	Part of the SYSREF Align block

8.5.12 Vendor ID and Chip Version Register (address = 0x7F) [reset = 0x0008]]

Figure 64. Vendor ID and Chip Version Register (VENDOR_VER)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 59. VENDOR_VER Field Descriptions

Bit	Field	Type	Reset	Description
15	AUTOLOAD_DONE	R	0	Asserted when the Fusefarm Autoload sequence is done
14:10	EFC_ERR	R	00000	The error output from the fuse farm.
9:5	Reserved	R	00000	Reserved
4:3	VENDORID	R	01	TI identification
2:0	VERSION	R	001	Bits to determine what version of build for the chip.

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8.5.13 Multi-DUC Configuration (PAP, Interpolation) Register (address = 0x0A) [reset = 0x02B0]

Figure 65. Multi-DUC Configuration (PAP, Interolation) Register (MULTIDUC_CFG1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
1	0	0	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 60. MULTIDUC_CFG1 Field Descriptions

Bit	Field	Type	Reset	Description
15	DUAL_IQ	R/W	0	When asserted the SLICE uses both IQ paths
14	ISFIR_ENA	R/W	0	Turns on the inverse sync filter for the AB and CD paths when programmed to 1.
13	Not used	R/W	0	Not used
12:8	INTERP	R/W	00010	Determines the interpolation amount. 00000: 1x 00001: 2x 00010: 4x 00011: 6x 00100: 8x 00101: 10x 00110: 12x 01000: 16x 01001: 18x 01010: 20x 01100: 24x
7	ALM_ZEROS_TXEN	R/W	1	When asserted any alarm that isn't masked will mid-level the DAC output by setting the txenable_from_dig to '0'
6	DAC_COMPLEMENT	R/W	0	When asserted the DAC output will be 2's complemented. This helps with hookup at the board level.
5	ALM_ZEROS_JESD	R/W	1	When asserted any alarm that isn't masked will zero the data coming out of the JESD block.
4	ALM_OUT_ENA	R/W	1	When asserted the output from the selected SLICE will be passed on to the MASTER alarm control if it is also turned on then the alarm will be sent to the pad_alarm pin.
3	PAPA_ENA	R/W	0	Turns on the Power Amp Protection logic for path A.
2	PAPB_ENA	R/W	0	Turns on the Power Amp Protection logic for path B.
1	PAPC_ENA	R/W	0	Turns on the Power Amp Protection logic for path C.
0	PAPD_ENA	R/W	0	Turns on the Power Amp Protection logic for path D.

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8.5.14 Multi-DUC Configuration (Mixers) Register (address = 0x0C) [reset = 0x2402]

Figure 66. Multi-DUC Configuration (Mixers) Register (MULTIDUC_CFG2)

15	14	13	12	11	10	9	8
0	0	0	0	0	1	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 61. MULTIDUC_CFG2 Field Descriptions

Bit	Field	Type	Reset	Description
15:14	DAC_BITWIDTH	R/W	0b00	Determines the bit width of the data going to the DAC 00: 14 bits 01: 14 bits 10: 12 bits 11: 11 bits
13	ZERO_INVLD_DATA	R/W	1	When asserted; the data from the JESD block is zeroed in the mapper to prevent goofy output from the DAC. For test purposes this bit should be desasserted
12	SHORTTEST_ENA	R/W	0	Turns on the JESD SHORT pattern test (5.1.6.2)
11	Reserved	R/W	0	Reserved
10	Reserved	R/W	1	Reserved
9	MIXERAB_ENA	R/W	0	Turns on the mixer for the A and B streams
8	MIXERCD_ENA	R/W	0	Turns on the mixer for the C and D streams
7	MIXERAB_GAIN	R/W	0	Adds 6dB of gain when asserted
6	MIXERCD_GAIN	R/W	0	Adds 6dB of gain when asserted
5	NCOAB_ENA	R/W	0	When high the full NCO block is turned on.
4	NCOCD_ENA	R/W	0	When high the full NCO block is turned on.
3:2	Reserved	R/W	00	Reserved
1	TWOS	R/W	1	When asserted the chip is expecting 2's complement data is arriving through the JESD; otherwise offset binary is expected
0	Reserved	R/W	0	Reserved

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8.5.15 JESD FIFO Control Register (address = 0x0D) [reset = 0x1300]

Figure 67. JESD FIFO Control Register (JESD_FIFO)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 62. JESD_FIFO Field Descriptions

Bit	Field	Type	Reset	Description
15	FIFO_ZEROS_DATA	R/W	1	When asserted FIFO errors zero the data out of the JESD block. For test purposes this could be turned off to allow test patterns in the FIFO.
14:13	NOT USED	R/W	000	Not Used
12	SRDS_FIFO_ALM_CLR	R/W	0	Set to 1 to clear FIFO errors. Must be set to 0 for proper FIFO operation
11	Not used	R/W	0	Not used
10:8	FIFO_OFFSET	R/W	0000	Used to set the difference between read and write pointers in the JESD FIFO.
7:1	Reserved	R/W	0	Reserved
0	SPI_TXENABLE	R/W	0	When asserted the internal value of txenable = '1'

8.5.16 Alarm Mask 1 Register (address = 0x0E) [reset = 0x00FF]

Figure 68. Alarm Mask 1 Register (ALM_MASK1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 63. ALM_MASK1 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ALM_MASK1	R/W	0x00FF	Each bit is used to mask an alarm. Assertion masks the alarm: bit 15 = mask lane7 lane errors bit 14 = mask lane6 lane errors bit 13 = mask lane5 lane errors bit 12 = mask lane4 lane errors bit 11 = mask lane3 lane errors bit 10 = mask lane2 lane errors bit 9 = mask lane1 lane errors bit 8 = mask lane0 lane errors bit 7 = mask lane7 FIFO flags bit 6 = mask lane6 FIFO flags bit 5 = mask lane5 FIFO flags bit 4 = mask lane4 FIFO flags bit 3 = mask lane3 FIFO flags bit 2 = mask lane2 FIFO flags bit 1 = mask lane1 FIFO flags bit 0 = mask lane0 FIFO flags

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8.5.17 Alarm Mask 2 Register (address = 0x0F) [reset = 0xFFFF]

Figure 69. Alarm Mask 2 Register (ALM_MASK2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 64. ALM_MASK2 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ALMS_MASK2	R/W	0xFFFF	Each bit is used to mask an alarm. Assertion masks the alarm: bit 15 = not used bit 14 = not used bit 13 = not used bit 12 = mask SYSREF errors on link0 bit 11 = mask alarm from JESD shorttest bit 10 = mask alarm from PAPD bit 9 = mask alarm from PAPC bit 8 = mask alarm from PAPB bit 7 = mask alarm from PAPA bit 6 = not used bit 5 = not used bit 4 = not used bit 3 = not used bit 2 = not used bit 1 = mask alarm_clkdiv192_eq_zero bit 0 = mask alarm_clkdiv192_eq_mult1

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8.5.18 Alarm Mask 3 Register (address = 0x10) [reset = 0xFFFF]

Figure 70. Alarm Mask 3 Register (ALM_MASK3)

15	14	13	12	11	10	9	8
	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 65. ALM_MASK3 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ALMS_MASK3	R/W	0xFFFF	Each bit is used to mask an alarm. Assertion masks the alarm: bit 15 = mask alarm_clkdiv8_eq_zero bit 14 = mask alarm_clkdiv12_eq_zero bit 13 = mask alarm_clkdiv16_eq_zero bit 12 = mask alarm_clkdiv18_eq_zero bit 11 = mask alarm_clkdiv20_eq_zero bit 10 = mask alarm_clkdiv32_eq_zero bit 9 = mask alarm_clkdiv36_eq_zero bit 8 = mask alarm_clkdiv40_eq_zero bit 7 = mask alarm_clkdiv48_eq_zero bit 6 = mask alarm_clkdiv64_eq_zero bit 5 = mask alarm_clkdiv72_eq_zero bit 4 = mask alarm_clkdiv80_eq_zero bit 3 = mask alarm_clkdiv96_eq_zero bit 2 = maskalarm_ clkdiv128_eq_zero bit 1 = mask alarm_clkdiv144_eq_zero bit 0 = mask alarm_clkdiv160_eq_zero

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8.5.19 Alarm Mask 4 Register (address = 0x11) [reset = 0xFFFF]

Figure 71. Alarm Mask 4 Register (ALM_MASK4)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 66. ALM_MASK4 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ALMS_MASK4	R/W	0xFFFF	Each bit is used to mask an alarm. Assertion masks the alarm: bit 15 = mask alarm_clkdiv8_eq_mult1 bit 14 = mask alarm_clkdiv12_eq_mult1 bit 13 = mask alarm_clkdiv16_eq_mult1 bit 12 = mask alarm_clkdiv18_eq_mult1 bit 11 = mask alarm_clkdiv20_eq_mult1 bit 10 = mask alarm_clkdiv32_eq_mult1 bit 9 = mask alarm_clkdiv36_eq_mult1 bit 8 = mask alarm_clkdiv40_eq_mult1 bit 7 = mask alarm_clkdiv48_eq_mult1 bit 6 = mask alarm_clkdiv64_eq_mult1 bit 5 = mask alarm_clkdiv72_eq_mult1 bit 4 = mask alarm_clkdiv80_eq_mult1 bit 3 = mask alarm_clkdiv96_eq_mult1 bit 2 = maskalarm_ clkdiv128_eq_mult1 bit 1 = mask alarm_clkdiv144_eq_mult1 bit 0 = mask alarm_clkdiv160_eq_mult1

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8.5.20 JESD Lane Skew Register (address = 0x12) [reset = 0x0000]

Figure 72. JESD Lane Skew Register (JESD_LN_SKEW)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 67. JESD_LN_SKEW Field Descriptions

Bit	Field	Type	Reset	Description
15:5	NOT USED	R	0x0000	Not used
4:0	MEMIN_LANE_SKEW	R	0b00000	Measure of the lane skew for each link only. Bits are READ_ONLY

8.5.21 CMIX Configuration Register (address = 0x17) [reset = 0x0000]

Figure 73. CMIX Configuration Register (CMIX)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	0	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 68. CMIX Field Descriptions

Bit	Field	Type	Reset	Description
15:12	CMIX_AB	R/W	0x0	These bits turn on the different coarse mixing options. Combining the different options together can result in every possible n x Fs/8 [n=0->7]. Below is the valid programming table: cmix=(mem_fs8; mem_fs4; mem_fs2; mem_fsm4) 0000 : no mixing 0001 : -fs/4 0010 : fs/2 0100 : fs/4 1000 : fs/8 1100 : 3fs/8 1010 : 5fs/8 1110 : 7fs/8
11:4	Reserved	R/W	00000000 0	Reserved
3:0	CMIX_CD	R/W	0x0	These bits turn on the different coarse mixing options. Combining the different options together can result in every possible n x Fs/8 [n=0->7]. Below is the valid programming table: cmix=(mem_fs8; mem_fs4; mem_fs2; mem_fsm4) 0000 : no mixing 0001 : -fs/4 0010 : fs/2 0100 : fs/4 1000 : fs/8 1100 : 3fs/8 1010 : 5fs/8 1110 : 7fs/8

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8.5.22 Output Summation and Delay Register (address = 0x19) [reset = 0x0000]

Figure 74. Output Summation and Delay Register (OUTSUM)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 69. OUTSUM Field Descriptions

Bit	Field	Type	Reset	Description
15:12	OUTPUT_DELAY	R/W	0x0	Delays the output to the DAC 0 to 15 clock cycles
11:4	Reserved	R/W	0x00	Reserved
3:0	OUTSUM_SEL	R/W	0x0	Selects the output summing functions. Each bit selects another sample to sum. Multiple bits can be selected. bit 0 = add the path AB sample bit 1 = add the path CD sample bit 2 = add adjacent DAC path AB sample bit 3 = add adjacent DAC path CD sample

8.5.23 NCO Phase Path AB Register (address = 0x1C) [reset = 0x0000]

Figure 75. NCO Phase Path AB Register (PHASE_NCOAB)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 70. PHASE_NCOAB Field Descriptions

Bit	Field	Type	Reset	Description
15:0	PHASE_NCO1	Auto Sync	0x0000	The phase offset for the FULL NCO1 in the AB datapath.

8.5.24 NCO Phase Path CD Register (address = 0x1D) [reset = 0x0000]

Figure 76. NCO Phase Path CD Register (PHASE_NCOCD)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 71. PHASE_NCOCD Field Descriptions

Bit	Field	Type	Reset	Description
15:0	PHASE_NCO12	Auto Sync	0x0000	The phase offset for the FULL NCO2 in the CD datapath.

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8.5.25 NCO Frequency Path AB Register (address = 0x1E-0x20) [reset = 0x0000 0000 0000]

Figure 77. NCO Frequency Path AB Register (FREQ_NCOAB)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 72. FREQ_NCOAB Field Descriptions

Bit	Field	Type	Reset	Description
47:0	FREQ_NCOAB	R/W	0x0000 0000 0000	NCO frequency word for AB data path.

8.5.26 NCO Frequency Path CD Register (address = 0x21-0x23) [reset = 0x0000 0000 0000]

Figure 78. NCO Frequency Path CD Register (FREQ_NCOCD)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 73. FREQ_NCOCD Field Descriptions

Bit	Field	Type	Reset	Description
47:0	FREQ_NCOCD	R/W	0x0000 0000 0000	NCO frequency word for CD data path.

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8.5.27 SYSREF Use for Clock Divider Register (address = 0x24) [reset = 0x0010]

Figure 79. SYSREF Use for Clock Divder Register (SYSREF_CLKDIV)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 74. SYSREF_CLKDIV Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	Reserved
14:12	CDRVSER_SYSREF_DLY	R/W	000	Programmable delay the SYSREF by N dacclk cycles to the CDRV_SER clock dividers. By offsetting the clock to the different multi-DUC blocks, clock mixing could potentially be reduced.
11:7	Not used	R/W	00000	Not used
6:4	SYSREF_MODE	R/W	001	Determines how SYSREF is used to sync the clock dividers in the CDRV_SER block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses.
3:2	SYSREF_DLY	R/W	00	Delays the SYSREF into the CDRV_SER capture FF through 1 of 4 choices. This allows for extra delay in case the timing of the clock or SYSREF path isn't as good as we think.
1:0	Reserved	R/W	00	Reserved

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8.5.28 Serdes Clock Control Register (address = 0x25) [reset = 0x7700]

Figure 80. Serdes Clock Control Register (SERDES_CLK)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 75. SERDES_CLK Field Descriptions

Bit	Field	Type	Reset	Description
15:12	CLKJESD_DIV	R/W	0x7	This controls the selection of the clk_jesd output 0000 = div4 0001 = div8 0010 = div12 0011 = div16 0100 = div18 0101 = div20 0110 = div24 0111 = div32 1001 = div36 1010 = div48 1011 = div64 1100 = div5.333 1101 = div10.666 1110 = div21p333
11:8	CLKJESD_OUT_DIV	R/W	0x7	This controls the selection of the clk_jesd_out output 0000 = div8 0001 = div16 0010 = div32 0011 = div48 0100 = div64 0101 = div80 0110 = div96 0111 = div128 1000 = div144 1001 = div160 1010 = div192
7:0	Reserved	R/W	0x0	Reserved

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8.5.29 Sync Source Control 1 Register (address = 0x27) [reset = 0x1144]

Figure 81. Sync Source Control 1 Register (SYNCSEL1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	0	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 76. SYNCSEL1 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	SYNCSEL_MIXERAB	R/W	0x1	Controls the syncing of the double buffered SPI registers for the mixerAB block. These bits are enables so a ‘1’ in the bit place allows the sync to pass to the block. bit 0 = auto-sync from SPI register write bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync
11:8	SYNCSEL_MIXERCD	R/W	0x1	Controls the syncing of the double buffered SPI registers for the mixerCD block. These bits are enables so a ‘1’ in the bit place allows the sync to pass to the block. bit 0 = auto-sync from SPI register write bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync
7:4	SYNCSEL_NCOAB	R/W	0x4	Controls the syncing of NCOAB accumulators. These bits are enables so a ‘1’ in the bit place allows the sync to pass to the block. bit 0 = ‘0’ bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync
3:0	SYNCSEL_NCOCD	R/W	0x4	Controls the syncing of NCOCD accumulators. These bits are enables so a ‘1’ in the bit place allows the sync to pass to the block. bit 0 = ‘0’ bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync

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8.5.30 Sync Source Control 2 Register (address = 0x28) [reset = 0x0000]

Figure 82. Sync Source Control 2 Register (SYNCSEL2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 77. SYNCSEL2 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	Reserved	R/W	0x0	Reserved
11:8	SYNCSEL_PAPAB	R/W	0x0	Select the sync for the PAP A and B. bit 0 = ‘0’ bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync
7:4	SYNCSEL_PAPCD	R/W	0x0	Select the sync for the PAP C and D. bit 0 = ‘0’ bit 1 = sysref bit 2 = sync_out from JESD bit 3 = mem_spi_sync
3:2	Reserved	R/W	0b00	Reserved
1	SPI_SYNC	R/W	0	This is used to generate the SPI_SYNC signal
0	Reserved	R/W	0	Reserved

8.5.31 PAP path AB Gain Attenuation Step Register (address = 0x29) [reset = 0x0000]

Figure 83. PAP path AB Gain Attenuation Step Register (PAP_GAIN_AB)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 78. PAP_GAIN_AB Field Descriptions

Bit	Field	Type	Reset	Description
15:10	NOT USED	RW	000000	Not Used
9:0	PAPAB_GAIN_STEP		0x000	Gain attenuation step

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8.5.32 PAP path AB Wait Time Register (address = 0x2A) [reset = 0x0000]

Figure 84. PAP path AB Wait Time Register (PAP_WAIT_AB)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 79. PAP_WAIT_AB Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	000000	R/W	Reserved
9:0	PAPAB_WAIT	0x000	R/W	Number of clock cycles to wait after gain = 0

8.5.33 PAP path CD Gain Attenuation Step Register (address = 0x2B) [reset = 0x0000]

Figure 85. PAP path CD Gain Attenuation Step Register (PAP_GAIN_CD)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 80. PAP_GAIN_CD Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Not Used	R/W	000000	Not Used
9:0	PAPCD_GAIN_STEP	R/W	0x000	Gain attenuation step

8.5.34 PAP Path CD Wait Time Register (address = 0x2C) [reset = 0x0000]

Figure 86. PAP path CD Wait Time Register (PAP_WAIT_CD)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 81. PAP_WAIT_CD Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	R/W	000000	Reserved
9:0	PAPCD_WAIT	R/W	0x000	Number of clock cycles to wait after gain = 0

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8.5.35 PAP path AB Configuration Register (address = 0x2D) [reset = 0x0FFF]

Figure 87. PAP path AB Configuration Register (PAP_CFG_AB)

15	14	13	12	11	10	9	8
0	0	Reserved	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 82. PAP_CFG_AB Field Descriptions

Bit	Field	Type	Reset	Description
15:14	PAPAB_SEL_DLY	R/W	00	Controls the length of the delayline in the PAP AB logic. 00 : N =32 01 : N = 64 10 : N = 128 11 : Not Valid
13	Reserved	R/W	0	Reserved
12:0	PAPAB_THRESH	R/W	0xFFF	The threshold for the PAP AB trigger.

8.5.36 PAP path CD Configuration Register (address = 0x2E) [reset = 0x0FFF]

Figure 88. PAP path CD Configuration Register (PAP_CFG_CD)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 83. PAP_CFG_CD Field Descriptions

Bit	Field	Type	Reset	Description
15:14	PAPCD_SEL_DLY	R/W	00	Controls the length of the delay line in the PAP CD logic. 00 : N = 32 01 : N = 64 10 : N = 128 11 : Not Valid
13	Reserved	R/W	0	Reserved
12:0	PAPCD_THRESH	R/W	0xFFF	The threshold for the PAP CD trigger.

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8.5.37 DAC SPI Configuration Register (address = 0x2F) [reset = 0x0000]

Figure 89. DAC SPI Constant 1 Register (SPIDAC_TEST1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 84. SPIDAC_TEST1 Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	R/W	0x0000	Reserved
0	SPIDAC_ENA	R/W	0	When asserted the DAC output is set to the value in register SPIDAC. This can be used for trim setting and other static tests.

8.5.38 DAC SPI Constant Register (address = 0x30) [reset = 0x0000]

Figure 90. DAC SPI Constant Register (SPIDAC_TEST2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 85. SPIDAC_TEST2 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SPIDAC	R/W	0x0000	This value replaces the data at the output of the JESD so that the DAC value can be controlled

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8.5.39 Gain for path AB Register (address = 0x32) [reset = 0x0000]

Figure 91. Gain for path AB Register (GAINAB)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 86. GAINAB Field Descriptions

Bit	Field	Type	Reset	Description
15	GAINAB_ENA	R/W	0	Turns on the path AB gain block
14:12	Reserved	R/W	0x0	Reserved
11:0	GAINAB	R/W	0x400	Extra control of gain in the GAINAB block. This allows a fix gain to be added to the signal if needed.

8.5.40 Gain for path CD Register (address = 0x33) [reset = 0x0000]

Figure 92. Gain for path CD Register (GAINCD)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 87. GAINCD Field Descriptions

Bit	Field	Type	Reset	Description
15	GAINCD_ENA	R/W	0	Turns on the Path CD gain block
14:12	Reserved	R/W	0x0	Reserved
11:0	GAINCD	R/W	0x400	Extra control of gain in the GAINCD block. This allows a fix gain to be added to the signal if needed.

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8.5.41 JESD Error Counter Register (address = 0x41) [reset = 0x0000]

Figure 93. JESD Error Counter Register (JESD_ERR_CNT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 88. JESD_ERR_CNT Field Descriptions

Bit	Field	Type	Reset	Description
15:0	JESD_ERR_CNT	R	0x0000	This is the error count for the JESD link. This is a 16bit value that is not cleared until the JESD synchronization is required or errcnt_clr is programmed to '1'

8.5.42 JESD ID 1 Register (address = 0x46) [reset = 0x0044]

Figure 94. JESD ID 1 Register (JESD_ID1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 89. JESD_ID1 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	LID0	R/W	00000	JESD ID for lane 0
10:6	LID1	R/W	00001	JESD ID for lane 1
5:1	LID2	R/W	00010	JESD ID for lane 2
0	Reserved	R/W	0	Reserved

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8.5.43 JESD ID 2 Register (address = 0x47) [reset = 0x190A]

Figure 95. JESD ID 2 Register (JESD_ID2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 90. JESD ID 2 Register (JESD_ID2)

Bit	Field	Type	Reset	Description
15:11	LID3	R/W	00011	JESD ID for lane 3
10:6	LID4	R/W	00100	JESD ID for lane 4
5:1	LID5	R/W	00101	JESD ID for lane 5
0	Reserved	R/W	0	Reserved

8.5.44 JESD ID 3 and Subclass Register (address = 0x48) [reset = 0x31C3]

Figure 96. JESD ID 3 Register (JESD_ID3)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 91. JESD_ID3 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	LID6	R/W	00110	JESD ID for lane 6
10:6	LID7	R/W	00111	JESD ID for lane 7
5:4	Reserved	R/W	00	Reserved
3:1	SUBCLASSV	R/W	001	Selects the JESD subclass supported. Note: “001” is subclass 1 and “000” is subclass 0 they are the only modes supported; not used for operation but used for configuration. See field MIN_LATENCY_ENA in register JESD_MATCH (9.5.46) for use in subclass0
0	JESDV	R/W	1	Selects the version of JESD support(0=A; 1=B) NOTE: JESD 204B is only supported version.

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8.5.45 JESD Lane Enable Register (address = 0x4A) [reset = 0x0003]

Figure 97. JESD Lane Enable Register (JESD_LN_EN)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 92. JESD_LN_EN Field Descriptions

Bit	Field	Type	Reset	Description
15:8	LANE_ENA		0x00	Turn on each lane as needed. Signal is active high. bit 15 : lane7 enable bit 14 : lane6 enable bit 13 : lane5 enable bit 12 : lane4 enable bit 11 : lane3 enable bit 10 : lane2 enable bit 9 : lane1 enable bit 8 : lane0 enable
7:6	JESD_TEST_SEQ		00	Set to select and verify link layer test sequences. The error for these sequences comes out the lane alarms bit0. 1= a fail and 0 = pass. 00 : test sequence disabled 01 : verify repeating D.21.5 high frequency pattern for random jitter 10 : verify repeating K.28.5 mixed frequency pattern for deterministic jitter 11 : verify repeating ILA sequence
5:2	Reserved		0x0	Reserved
1:0	JESD_PHASE_MODE		11	Used to tell the JESD block how many clock phases are being used for lanes. 00 = 1 phase 01 = 2 phases 10 = 4 phases 11 = 8 phases

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8.5.46 JESD RBD Buffer and Frame Octets Register (address = 0x4B) [reset = 0x1300]

Figure 98. JESD RBD Buffer and Frame Octets Register (JESD_RBD_F)

15	14	13	12	11	10	9	8
			0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0		0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 93. JESD_RBD_F Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	00	Reserved
12:8	RBD	R/W	10011	This controls the amount of elastic buffers being used in the JESD. Larger numbers will mean more latency; but smaller numbers may not hold enough data to capture the input skew. This value must always be ≤ mem_k
7:0	F_M1	R/W	0x00	This is the number of octets in the frame - 1

8.5.47 JESD K and L Parameters Register (address = 0x4C) [reset = 0x1303]

Figure 99. JESD K and L Parameters Register (JESD_K_L)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 94. JESD_K_L Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	000	Reserved
12:8	K_M1	R/W	10011	The number of frames in a multi-frame - 1. 0 ≤ k - 1 < 32
7:5	Reserved	R/W	0	Reserved
4:0	L_M1	R/W	00011	The number of lanes used by the JESD - 1. 0 ≤ L -1 < 8

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8.5.48 JESD M and S Parameters Register (address = 0x4D) [reset = 0x0100]

Figure 100. JESD M and S Parameters Register (JESD_M_S)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 95. JESD_M_S Field Descriptions

Bit	Field	Type	Reset	Description
15:8	M_M1	R/W	0x01	The number of streams per frame - 1. 0 ≤ M - 1 < 256
7:5	Reserved	R/W	000	Reserved
4:0	S_M1	R/W	00000	The number of samples per stream per frame - 1.

8.5.49 JESD N, HD and SCR Parameters Register (address = 0x4E) [reset = 0x0F4F]

Figure 101. JESD N, HD and SCR Parameters Register (JESD_N_HD_SCR)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 96. JESD_N_HD_SCR Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	000	Reserved
12:8	NPRIME_M1	R/W	01111	The number of adjusted bits per sample - 1
7	Reserved	R/W	0	Reserved
6	HD	R/W	1	High density mode. Samples can cross the lane boundary
5	SCR	R/W	0	Turn on the scrambler
4:0	N_M1	R/W	01111	The number of bits per sample - 1

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8.5.50 JESD Character Match and Other Register (address = 0x4F) [reset = 0x1CC1]

Figure 102. JESD Character Match and Other Parameters Register (JESD_MATCH)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 97. JESD_MATCH Field Descriptions

Bit	Field	Type	Reset	Description
15:8	MATCH_DATA	R/W	0x1C	The character to match for buffer release. Normally it is a /R/=/K28.0/-0x1C but with these bits the user can program the value.
7	MATCH_SPECIFIC	R/W	1	Match a specific charater to start the JESD buffering when asserted; otherwise the first non-K will start the buffering.
6	MATCH_CTRL	R/W	1	When asserted the match character is a CONTROL character instead of a DATA character.
5	NO_LANE_SYNC	R/W	0	Assert if the TX side does not support lane initialization. This way the RX won't flag errors in the configuration portion of the ILA.
4:2	Not Used	R/W	000	Not Used
1	MIN_LATENCY_ENA	R/W	0	Enable minimum latency when set. This is needed for subclass 0 support.
0	JESD_COMMAALIGN_ENA	R/W	1	When asserted the JESD block SERDES comma align signal will be added with the SERDES ALIGN bit(0) to control when to shut off comma alignment. When this bit is deasserted; then the programmed bit(spi_config62(11)) is the only control.

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8.5.51 JESD Link Configuration Data Register (address = 0x50) [reset = 0x0000]

Figure 103. JESD Link Configuration Data Register (JESD_LINK_CFG)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 98. JESD_Link_CFG Field Descriptions

Bit	Field	Type	Reset	Description
15-12	ADJCNT	R/W	0x0	Lane configuration data for link. Reserved by DAC38RF8x except for lane configuration checking.
11	ADJDIR	R/W	0	Lane configuration data for link. Reserved by DAC38RF8x except for lane configuration checking.
10-7	BID	R/W	0x0	Lane configuration data for link. Reserved by DAC38RF8x except for lane configuration checking.
6-2	CF	R/W	00000	Lane configuration data for link. Reserved by DAC38RF8x except for lane configuration checking.
1-0	CS	R/W	00	Lane configuration data for link. Reserved by DAC38RF8x except for lane configuration checking.

8.5.52 JESD Sync Request Register (address = 0x51) [reset = 0x00FF]

Figure 104. JESD Sync Request Register (JESD_SYNC_REQ)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 99. JESD_SYNC_REQ Field Descriptions

Bit	Field	Type	Reset	Description
15:8	DID	R/W	0x00	Lane configuration
7:0	SYNC_REQUEST	R/W	0xFF	These bits select which errors cause a sync request. Sync requests take priority over the error notification; so if sync request isn't desired; set these bits to a '0'. bit 7 = multi-frame alignment error bit 6 = frame alignment error bit 5 = link configuration error bit 4 = elastic buffer overflow (bad RBD value) bit 3 = elastic buffer end char mismatch (match_ctrl match_data) bit 2 = code synchronization error bit 1 = 8b/10b not-in-table code error bit 0 = 8b/10b disparity error

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8.5.53 JESD Error Output Register (address = 0x52) [reset = 0x00FF]

Figure 105. JESD Error Output Register (JESD_ERR_OUT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 100. JESD_ERR_OUT Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	R/W	000000	Reserved
9	DISABLE_ERR_RPT	R/W	0	Assertion means that errors will not be reported on the sync_n output.
8	PHADJ	R/W	0	Lane configuration
7:0	ERR_ENA	R/W	0xFF	These bits select the errors generated are counted in the err_c for the link. The bits also control what signals are sent out the pad_syncb pin for error notification. bit 7 = multi-frame alignment error bit 6 = frame alignment error bit 5 = link configuration error bit 4 = elastic buffer overflow (bad RBD value) bit 3 = elastic buffer end char mismatch (match_ctrl match_data) bit 2 = code synchronization error bit 1 = 8b/10b not-in-table code error bit 0 = 8b/10b disparity error

8.5.54 JESD ILA Check 1 Register (address = 0x53) [reset = 0x0100]

Figure 106. JESD ILA Check 1 Register (JESD_ILA_CFG1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 101. JESD_ILA_CFG1 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ILA_M	R/W	0x01	JESD M-1 configuration value used only for ILA checking; may be set independently of the actual JESD mode
7:0	ILA_F	R/W	0x00	JESD F-1 configuration value used only for ILA checking; may be set independently of the actual JESD mode

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8.5.55 JESD ILA Check 2 Register (address = 0x54) [reset = 0x8E60]

Figure 107. JESD ILA Check 2 Register (JESD_ILA_CFG2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 102. JESD_ILA_CFG2 Field Descriptions

Bit	Field	Type	Reset	Description
15	ILA_HD	R/W	1	JESD HD configuration value used only for ILA checking; may be set independently of the actual JESD mode
14:10	ILA_L	R/W	00011	JESD L-1 configuration value used only for ILA checking; may be set independently of the actual JESD mode
9:5	ILA_K	R/W	10011	JESD K-1 configuration value used only for ILA checking; may be set independently of the actual JESD mode
4:0	ILA_S	R/W	00000	JESD S-1 configuration value used only for ILA checking; may be set independently of the actual JESD mode

8.5.56 JESD SYSREF Mode Register (address = 0x5C) [reset = 0x0001]

Figure 108. JESD SYSREF Mode Register (JESD_SYSR_MODE)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 103. JESD_SYSR_MODE Field Descriptions

Bit	Field	Type	Reset	Description
15:4	Reserved	R/W	0x000	Reserved
3	ERR_CNT_CLR	R/W	0	A transition from 0->1 causes the error_cnt to be cleared
2:0	SYSREF_MODE	R/W	001	Determines how SYSREF is used in the JESD synchronizing block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses. 101 = skip two SYSREFs and then use one 110 = skip two SYSREFs and then use all

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8.5.57 JESD Crossbar Configuration 1 Register (address = 0x5F) [reset = 0x0123]

Figure 109. JESD Crossbar Configuration 1 Register (JESD_CROSSBAR1)

15	14	13	12	11	10	9	8
Reserved	0	0	0	Reserved	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 104. JESD_CROSSBAR1 Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	Reserved
14:12	OCTETPATH0_SEL	R/W	000	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
11	Reserved	R/W	0	Reserved
10:8	OCTETPATH1_SEL	R/W	001	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
7	Reserved	R/W	0	Reserved
6:4	OCTETPATH2_SEL	R/W	010	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
3	Reserved	R/W	0	Reserved
2:0	OCTETPATH3_SEL	R/W	011	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7

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8.5.58 JESD Crossbar Configuration 2 Register (address = 0x60) [reset = 0x4567]

Figure 110. JESD_CROSSBAR2 Field DBits to Determine What Version of Build for the chip.escriptions

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 105. JESD_CROSSBAR2 Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	Reserved
14:12	OCTETPATH4_SEL	R/W	100	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
11	Reserved	R/W	0	Reserved
10:8	OCTETPATH5_SEL	R/W	101	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
7	Reserved	R/W	0	Reserved
6:4	OCTETPATH6_SEL	R/W	110	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7
3	Reserved	R/W	0	Reserved
2:0	OCTETPATH7_SEL	R/W	111	These bits are used by the cross-bar switch to map any lane to any other lane. The 3 bit term tells the mapper block what lane this particular lane is supposed to be treated as. 000 = treat as lane0 001 = treat as lane1 010 = treat as lane2 011 = treat as lane3 100 = treat as lane4 101 = treat as lane5 110 = treat as lane6 111 = treat as lane7

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8.5.59 JESD Alarms for Lane 0 Register (address = 0x64) [reset = 0x0000]

Figure 111. JESD Alarms for Lane 0 Register (JBits to determine what version of build for the chip.ESD_ALM_L0)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 106. JESD_ALM_L0 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALM_LANE0_ERR	W0C	0x00	Lane0 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO0_FLAGS	W0C	0x0	Lane0 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

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8.5.60 JESD Alarms for Lane 1 Register (address = 0x65 01100101) [reset = 0x0000]

Figure 112. JESD Alarms for Lane 1 Register (JESD_ALM_L1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 107. JESD_ALM_L1 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALM_LANE1_ERR	W0C	0x00	Lane1 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO1_FLAGS	W0C	0x0	Lane1 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

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8.5.61 JESD Alarms for Lane 2 Register (address = 0x66) [reset = 0x0000]

Figure 113. JESD Alarms for Lane 2 Register (JESD_ALM_L2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	0	1	1	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 108. JESD_ALM_L2 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALM_LANE2_ERR	W0C	0x00	Lane2 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO2_FLAGS	W0C	0x0	Lane2 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

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8.5.62 JESD Alarms for Lane 3 Register (address = 0x67) [reset = 0x0000]

Figure 114. JESD Alarms for Lane 3 Register (JESD_ALM_L3)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	0	1	1	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 109. JESD_ALM_L3 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALM_LANE3_ERR	W0C	0x00	Lane3 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO3_FLAGS	W0C	0x0	Lane3 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

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8.5.63 JESD Alarms for Lane 4 Register (address = 0x68) [reset = 0x0000]

Figure 115. JESD Alarms for Lane 4 Register (JESD_ALM_L4)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	0	0	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 110. JESD_ALM_L4 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALM_LANE4_ERR	W0C	0x00	Lane4 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO4_FLAGS	W0C	0x0	Lane4 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

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8.5.64 JESD Alarms for Lane 5 Register (address = 0x69) [reset = 0x0000]

Figure 116. 8.4.60 JESD Alarms for Lane 5 Register (address = 0x69) [reset = 0x0000]

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	0	0	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 111. JESD_ALM_L5 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALM_LANE5_ERR	W0C	0x00	Lane5 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO5_FLAGS	W0C	0x0	Lane5 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

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8.5.65 JESD Alarms for Lane 6 Register (address = 0x6A [reset = 0x0000]

Figure 117. JESD Alarms for Lane 6 Register (JESD_ALM_L6)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	0	1	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 112. JESD_ALM_L6 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALM_LANE6_ERR	W0C	0x00	Lane6 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO6_FLAGS	W0C	0x0	Lane6 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

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8.5.66 JESD Alarms for Lane 7 Register (address = 0x6B) [reset = 0x0000]

Figure 118. JESD Alarms for Lane 7 Register (JESD_ALM_L7)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	0	1	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 113. JESD Alarms for Lane 7 Register (JESD_ALM_L7)

Bit	Field	Type	Reset	Description
15:8	ALM_LANE7_ERR	W0C	0x00	Lane7 errors: bit 15 = multiframe alignment error bit 14 = frame alignment error bit 13 = link configuration error bit 12 = elastic buffer overflow (bad RBD value) bit 11 = elastic buffer match error. The first non-/K/ doesn't match "match_ctrl" and "match_data" programmed values. bit 10 = code synchronization error bit 9 = 8b/10b not-in-table code error bit 8 = 8b/10b disparity error
7:4	Reserved	W0C	0x0	Reserved
3:0	ALM_FIFO7_FLAGS	W0C	0x0	Lane7 FIFO errors: bit 3 = write_error : High if write request and FIFO is full (NOTE: only released when JESD block is initialize with mem_init_state) bit 2 = write_full : FIFO is FULL bit 1 = read_error : High if read request with empty FIFO (NOTE: only released when JESD block is initialize with mem_init_state) bit 0 = read_empty : FIFO is empty

8.5.67 SYSREF and PAP Alarms Register (address = 0x6C) [reset = 0x0000]

Figure 119. SYSREF and PAP Alarms Register (ALM_SYSREF_PAP)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	1	0	0
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 114. ALM_SYSREF_PAP Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	W0C	0	Reserved
12	ALM_SYSREF_ERR	W0C		Alarm caused when the sysref is placed at an incorrect location
11	ALM_FROM_SHORTTEST	W0C		This is the alarm from JESD during the SHORT TEST checking.
10:7	ALM_PAP	W0C	0x0	The alarms from the PAP blocks indicated which PAP was triggered. bit0 = PAPA bit1 = PAPB bit2 = PAPC bit3 = PAPD
6:2	Reserved	W0C	0x0	Reserved
1	ALM_DIV192_ZERO	W0C	0	This is asserted if the clkdiv192 in the CDRV_SER shift register is all zeros.
0	Not Used	W0C	0	Not Used

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8.5.68 Clock Divider Alarms 1 Register (address = 0x6D) [reset = 0x0000]

Figure 120. Clock Divider Alarms 1 Register (ALM_CLKDIV1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C
7	6	5	4	3	2	1	0
0	1	1	0	1	1	0	1
W0C	W0C	W0C	W0C	W0C	W0C	W0C	W0C

LEGEND: R/W = Read/Write; R = Read only; W0C = Write 0 to clear bit; -n = value after reset; -n = value after reset

Table 115. ALM_CLKDIV1 Field Descriptions

Bit	Field	Type	Reset	Description
15	ALM_DIV8_ZERO	W0C	0	Asserted if the clkdiv8 in the CDRV_SER shift register is all zeros.
14	ALM_DIV12_ZERO	W0C	0	Asserted if the clkdiv12 in the CDRV_SER shift register is all zeros.
13	ALM_DIV16_ZERO	W0C	0	Asserted if the clkdiv16 in the CDRV_SER shift register is all zeros.
12	ALM_DIV24_ZERO	W0C	0	Asserted if the clkdiv24 in the CDRV_SER shift register is all zeros. (Connected to the div18 port)
11	ALM_DIV20_ZERO	W0C	0	Asserted if the clkdiv20 in the CDRV_SER shift register is all zeros.
10	ALM_DIV32_ZERO	W0C	0	Asserted if the clkdiv32 in the CDRV_SER shift register is all zeros.
9	ALM_DIV36_ZERO	W0C	0	Asserted if the clkdiv36 in the CDRV_SER shift register is all zeros.
8	ALM_DIV40_ZERO	W0C	0	Asserted if the clkdiv40 in the CDRV_SER shift register is all zeros.
7	ALM_DIV48_ZERO	W0C	0	Asserted if the clkdiv48 in the CDRV_SER shift register is all zeros.
6	ALM_DIV64_ZERO	W0C	0	Asserted if the clkdiv64 in the CDRV_SER shift register is all zeros.
5	ALM_DIV72_ZERO	W0C	0	Asserted if the clkdiv72 in the CDRV_SER shift register is all zeros.
4	ALM_DIV80_ZERO	W0C	0	Asserted if the clkdiv80 in the CDRV_SER shift register is all zeros.
3	ALM_DIV96_ZERO	W0C	0	Asserted if the clkdiv96 in the CDRV_SER shift register is all zeros.
2	ALM_DIV128_ZERO	W0C	0	Asserted if the clkdiv128 in the CDRV_SER shift register is all zeros.
1	ALM_DIV144_ZERO	W0C	0	Asserted if the clkdiv144 in the CDRV_SER shift register is all zeros.
0	ALM_DIV160_ZERO	W0C	0	Asserted if the clkdiv160 in the CDRV_SER shift register is all zeros.

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8.5.69 Clock Configuration Register (address = 0x0A) [reset = 0xF000]

Figure 121. Clock Configuration Register (CLK_CONFIG)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 116. CLK_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
15	RCLK_SYNC_ENA	RW	1	When asserted the sysref is used to sync the clock divider in the centralclkdiv. This should be disabled after initial syncing.
14	FRCLK_DIV_ENA	RW	1	When asserted the full rate clock divider that provides the DIV4 phases to the DACs is enabled
13	DACA_FRCLK_ENA	RW	1	When asserted the full rate clock to the DACA block is enabled
12	DACB_FRCLK_ENA	RW	1	When asserted the full rate clock to the DACB block is enabled
11	DACA_DUMDATA	RW	0	Enables distortion enhancement for DACA when set high
10	DACB_DUMDATA	RW	0	Enables distortion enhancement for DACB when set high
9:2	Reserved	RW	0x000	Reserved
1	QRCLOCK_DACA_ENA	RW	1	Turns on the quarter rate clock for DACA when '1'
0	QRCLOCK_DACB_ENA	RW	1	Turns on the quarter rate clock for DACB when '1'

8.5.70 Sleep Configuration Register (address = 0x0B) [reset = 0x0022]

Figure 122. Clock Configuration Register (SLEEP_CONFIG)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 117. SLEEP_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
15:9	Reserved	RW	0000000	Reserved
8	VBGR_SLEEP	RW	0	Turns off the 'bandgap-over-R' bias
7	Reserved	RW	0	Reserved
6	TSENSE_SLEEP	RW	0	Turns off the temperature sensor
5	PLL_SLEEP	RW	1	Puts the PLL into sleep mode (FUSE Controlled)
4	CLKRECV_SLEEP	RW	0	When asserted the clock input receiver gets put into sleep mode. This also affects the FIFO_OSTR receiver as well.
3	DACA_SLEEP	RW	0	Puts the DACA into sleep mode
2	DACB_SLEEP	RW	0	Puts the DACB into sleep mode
1	CLK_TX_SLEEP	RW	1	When asserted the PLL TX clock output is in low power mode.
0	Reserved	RW	0	Reserved

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8.5.71 Divided Output Clock Configuration Register (address = 0x0C) [reset = 0x8000]

Figure 123. Divided Output Clock Configuration Register (CLK_OUT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 118. CLK_OUT Field Descriptions

Bit	Field	Type	Reset	Description
15	CLK_TX_IDLE	R/W	1	When high puts the CLK_TX circuitry in idle mode during which the CLKTX+ and CLKTX- output pins are driven to the proper common-mode levels in order to charge the external AC coupling caps. When low allows the divided clock to be driven onto the CLKTX+ and CLKTX- output pins.
14:13	CLK_TX_DIVSELECT	R/W	01	Selects either div2, div3 or div 4 output. 00 = divided by 3 01 = divided by 4 10 = divided by 2 11 = not valid
12	Reserved	R/W	0	Reserved
11:8	CLK_TX_SWING	R/W	0x0	Sets desired swing on CLKTX+ and CLKTX- outputs in mVpp-diff 0x0 125 0x1 232 0x2 337 0x3 440 0x4 540 0x5 639 0x6 736 0x7 831 0x8 924 0x9 1012 0xA 1097 0xB 1178 0xC 1255 0xD 1329 0xE 1398 0xF 1462
7:3	Reserved	R/W	00000	Reserved
2	CLK_TX_FLIP	R/W	0	Flips the polarity of CLKTX
1	TX_SYNC_ENA	R/W	1	Syncs the CLKTX with SYSREF when asserted
0	EXTREF_ENA	R/W	0	Allows the chip to use an external refernce(1) or the internal reference(0)

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8.5.72 DAC Fullscale Current Register (address = 0x0D) [reset = 0xF000]

Figure 124. DAC Fullscale Current Register (DACFS)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 119. DACFS Field Descriptions

Bit	Field	Type	Reset	Description
15:12	DACFS	R/W	0xF	Scales the output current is 16 equal steps from 10-40mA (10mA + 2mA*DACFS)
10:0	Reserved	R/W	0x000	Reserved

8.5.73 Internal SYSREF Generator Register (address = 0x10) [reset = 0x0000]

Figure 125. Internal SYSREF Register (LCMGEN)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 120. LCMGEN Field Descriptions

Bit	Field	Type	Reset	Description
15:4	Reserved	R/W	0x00	Reserved
3	LCMGEN_ENA	R/W	0	Enables the LCM custom logic
2	LCMGEN_RESET	R/W	0	Reset the LCM custom logic
1	LCMGEN_SPI_SYSREF_ENA	R/W	0	TBD
0	LCM_SYSREF_OUTSEL	R/W	0	Chooses between internal and external SYSREF

8.5.74 Counter for Internal SYSREF Generator Register (address = 0x11) [reset = 0x0000]

Figure 126. Counter for Internal SYSREF Generator Register (LCMGEN_DIV)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 121. LCMGEN_DIV Field Descriptions

Bit	Field	Type	Reset	Description
15:0	LCMGEN_DIV	R/W	0x00	Counter setting for the LCMGEN block

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8.5.75 SPI SYSREF for Internal SYSREF Generator Register (address = 0x12) [reset = 0x0000]

Figure 127. SPI SYSREF for Internal SYSREF Generator Register (LCMGEN_SPISYSREF)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 122. LCMGEN_SPISYSREF Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	R/W	0x00	Reserved
0	LCMGEN_SPI_SYSREF	R/W	0	SPI SYSREF for the LCMGEN block

8.5.76 Digital Test Signals Register (address = 0x1B) [reset = 0x0000]

Figure 128. Digital Test Signals Register (DTEST)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 123. DTEST Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	Reserved
14:12	DTEST_LANE	R/W	000	Selects the lane to check for the signals selected by field DTEST
11:8	DTEST	R/W	0x0	Allows digital test signals to come out the ALARM pin. 0000 : Test disabled; normal ALARM pin function 0001 : SERDES lanes 0 – 3 PLL clock/80 0010 : SERDES lanes 4 – 7 PLL clock/80 0011 : TESTFAIL (lane selected by field DTEST_LANE) 0100 : SYNC (lane selected by field DTEST_LANE) 0101 : OCIP (lane selected by field DTEST_LANE) 0110 : EQUNDER (lane selected by field DTEST_LANE) 0111 : EQOVER (lane selected by field DTEST_LANE) 1000 – 1111 : not used
7:0	Reserved	R/W	0x00	Reserved

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8.5.77 Sleep Pin Control Register (address = 0x23) [reset = 0xFFFF]

These fields control the routing of the SLEEP signal to different blocks. Assertion means that the SLEEP signal will be sent to the block. These bits do not override the SPI bits; just the SLEEP signal from the PAD.

Figure 129. Sleep Pin Control Register (SLEEP_CNTL)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	0	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 124. SLEEP_CNTL Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	R/W	11111	Reserved
9	CLKOUT_SLEEP	R/W	1	Allows the output clock to sleep
8	BG_SLEEP	R/W	1	Allows the band gap to sleep
7	TEMP_SLEEP	R/W	1	Allows the temp sensor to sleep
6	PLL_CP_SLEEP	R/W	1	Allows the PLL charge pump to sleep
5	PLL_SLEEP	R/W	1	Allows the PLL to sleep
4	CLK_RECV_SLEEP	R/W	1	Allows the clock receiver to sleep
3:2	Reserved	R/W	11	Reserved
1	DACB_SLEEP	R/W	1	Allows DACB to sleep
0	DACA_SLEEP	R/W	1	Allows DACA to sleep

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8.5.78 SYSREF Capture Circuit Control Register (address = 0x24) [reset = 0x1000]

Figure 130. SYSREF Capture Circuit Control Register (SYSR_CAPTURE)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 125. SYSR_CAPTURE Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SYSR_PHASE_WDW	R/W	00	sysref phase alignment tolerance window Centers sysref capture window as follows: 00 = Centered on phase φ12 (**DEFAULT**) 01 = Centered on phase φ23 10 = Centered on phase φ34 11 = Centered on phase φ41
13:12	SYSR_ALIGN_DLY	R/W	01	sysref alignment offset delay Optional alignment offset that allows system designer to work around hardware (e.g. PCB) alignment errors by letting him specify that the sysref pulse should be treated as occurring one device clock earlier or later than its observed position. Legal settings are as follows: 00 = Offset by -1 device clock cycles. Treat sysref as if it were captured 1 cycle earlier. 01 = No offset (**DEFAULT**) 10 = Offset by +1 device clock cycles. Treat sysref as if it were captured 1 cycle later. 11 = Reserved
11	SYSR_STATUS_ENA	R/W	0	Enable alignment status monitoring Enable logic that generates sysref alignment status information and accumulates statistics that can be read by the user. 0 = Disable sysref alignment status outputs (**DEFAULT**). Used during normal operation. 1 = Enable sysref alignment status outputs. Used when characterizing sysref capture timing.
10:2	Reserved	R/W	0x000	Reserved
1	SYSR_ALIGN_SYNC	R/W	0	Write a ‘1’ to this bit to clear accumulated sysref align statistics
0	SYSR_BYPS_ALIGN	R/W	0	Bypass sysref alignment logic. Bypass the 4x oversampled sysref alignment logic and instead capture the sysref signal using the legacy implementation of a flip-flop clocked directly by the rising edge of the device clock. 0 = Capture sysref using full-featured alignment circuit (**DEFAULT**) 1 = Bypass sysref alignment logic NOTE: When mem_sysref_bypass_align is enabled, the other sysref alignment controls have no effect.

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8.5.79 Clock Input and PLL Configuration Register (address = 0x31) [reset = 0x0200]

Figure 131. Clock Input and PLL Configuration Register (CLK_PLL_CFG)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 126. Clock Input and PLL Configuration Register (CLK_PLL_CFG)

Bit	Field	Type	Reset	Description
15:14	Reserved	R/W	00	Reserved
13	SEL_EXTCLK_DIFFSE	R/W	0	Selects the external differential or single ended clock for DACCLK. 0 = differential 1 = single ended
12	PLL_RESET	R/W	0	When set the M divider; N divider and PFD are held reset
11	PLL_NDIVSYNC_ENA	R/W	0	When asserted; the SYSREF input is used to sync the N dividers of the PLL.
10	PLL_ENA	R/W	0	Enables the PLL output as the DAC clock when set; the clock provided at the DACCLKP/N is used as the PLL reference clock. When cleared; the PLL is bypassed and the clock provided at the DACCLKP/N pins is used as the DAC clock
9	PLL_CP_SLEEP	R/W	1	Must be set to '0' for proper PLL operation. 1 = Charge pump is put to sleep and can be driven by external source through the ATEST pins.
8	Reserved	R/W	0	Reserved
7:3	PLL_N_M1	R/W	00000	Reference clock divider; divide by is N+1
2:0	LOCKDET_ADJ	R/W	000	Adjusts the lock detector sensitivity. Upper bit isn't used: x00 - highest sensitivity x11 - lowest sensitivity

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8.5.80 PLL Configuration 1 Register (address = 0x32) [reset = 0x0308]

Figure 132. PLL Configuration 1 Register (PLL_CONFIG1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 127. CONFIG1 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PLL_M_M1	R/W	0x03	VCO feedback divider; divide by is 4(M+1)
7:4	Reserved	R/W	0x0	Reserved
3:0	PLL_VCO_RDAC	R/W	0x8	Controls the VCO amplitude

8.5.81 PLL Configuration 2 Register (address = 0x33) [reset = 0x4018]

Figure 133. PLL Configuration 2 Register (PLL_CONFIG2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 128. PLL_CONFIG2 Field Descriptions

Bit	Field	Type	Reset	Description
15	PLL_VCOSEL	R/W	0	Selects between two VCOs 0 = 5.9 GHz VCO(2 turn inductor in upper VCO) 1 = 8.9 GHz VCO (1 turn in the lower VCO)
14:8	PLL_VCO	R/W	1000000	VCO frequency range
7:6	Reserved	R/W	000	Reserved
5:2	PLL_CP_ADJ	R/W	0110	Adjusts the charge pump current; 0 to 1.55 mA in 50 µA steps. Setting to 0000 will hold the LPF pin at 0 V
1	Reserved	R/W	0	Reserved
0	Reserved	R/W	0	Reserved. Always write 0

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8.5.82 LVDS Output Configuration Register (address = 0x34) [reset = 0x0000]

Figure 134. LVDS Output Configuration Register (LVDS_CONFIG)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 129. LVDS_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
15	LVDS_LOPWRB	R/W	0	LVDS Output current control LSB; allows output current to be scaled from ~2 mA to ~4 mA
14	LVDS_LOPWRA	R/W	0	LVDS Output current control MSB; allows output current to be scaled from ~2 mA to ~4 mA
13	LVDS_LPSEL	R/W	0	$\overline{\text{SYNC}}$ LVDS output on chip termination control; 100 Ω when cleared; 200 Ω Output current settings for the combination of bits 15:13 110 = 4.00 mA 010 = 3.50 mA 100 = 3.00 mA 000 = 2.50 mA – Default current 111 = 4.00 mA 011 = 3.33 mA 101 = 2.66 mA 001 = 2.00 mA
12	LVDS_EFUSE_SEL	R/W	0	Enable LVDS bias bandgap reference voltage to the ATEST multiplexer.
11:10	LVDS_TRIM	R/W	00	Adjusts the LVDS 1.2 V reference. LVDS_TRIM_ENA must be set and LVDS_EFUSE_SEL must be cleared for these bits to have any effect. 10 +70 mV 00 -70 mV 01 default 11 -20 mV.
9	LVDS_TRIM_ENA	R/W	0	When set and LVDS_EFUSE_SEL is cleared; the LVDS_TRIM adjustment is enabled. When cleared; the LVDS_TRIM has no effect.
8	LVDS_SYNC0_PD	R/W	0	The $\overline{\text{SYNC0}}$ LVDS output is in power down.
7	Reserved	R/W	0	Reserved
6	LVDS_SYNC0_CM	R/W	0	$\overline{\text{SYNC0}}$ LVDS output common mode is 1.2 V when cleared; 0.9 V when set.
5:0	Reserved	R/W	0x00	Reserved

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8.5.83 Fuse Farm clock divider Register (address = 0x35) [reset = 0x0018]

Figure 135. Fuse Farm clock divider Register (PLL_FDIV)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	0	1	1
R/W	R/W	R/1W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after rese1t

Table 130. PLL_FDIV Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	R/W	0	Reserved
7:0	PLL_FDIV	R/W	0x18	Clock divider for the Fuse farm

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8.5.84 Serdes Clock Configuration Register (address = 0x3B) [reset = 0x0002]

Figure 136. Serdes Clock Configuration Register (SRDS_CLK_CFG)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	0	1	1
R/W	R/W	R/1W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after rese1t

Table 131. SRDS_CLK_CFG Field Descriptions

Bit	Field	Type	Reset	Description
15	SERDES_CLK_SEL	R/W	0	Select either the PLL output of the DACCLK from the pad. 0 = DACCLK pad 1 = PLL output
14:11	SERDES_REFCLK_DIV	R/W	0x0	The divide amount for the serdes REFCLK minus 1
10:2	Reserved	R/W	0x000	Reserved
1:0	SERDES_REFCLK_PREDIV	R/W	10	These bits select the pre-divide on the DACCLK input clock before the DACCLK is used in the dividers used in the SERDES PLL REFCLK and the Fusefarm SYSCLK. 00 = if DACCLK input ≤ 2 GHz; prediv is set to div1 01 = if DACCLK input is ≤ 4 GHz and > 2 GHz, prediv is set to div2 10 = if DACCLK input is ≤ 9 GHz and > 4 GHz, prediv is set to div4 11 = Not valid

8.5.85 Serdes PLL Configuration Register (address = 0x3C) [reset = 0x8228]

Figure 137. Serdes PLL Configuration Register (SRDS_PLL_CFG)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 132. SRDS_PLL_CFG Field Descriptions

Bit	Field	Type	Reset	Description
15	ENDIVCLK	R/W	1	Enable divided by 5 output clock
14:3	CLKBYP	R/W	00	Serdes clock bypass
12:11	LB	R/W	00	Serdes PLL loop bandwidth
10	SLEEPPLL	R/W	0	Serdes PLL Sleep
9	VRANGE	R/W	1	Serdes PLL loop filter range
8:1	MPY	R/W	00010100	Serdes reference clock multiplication factor Table 4
0	CORRECT	R/W	0	AND'ed with LANE_ENA so it must be set to 1 for correct behavior

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8.5.86 Serdes Configuration 1 Register (address = 0x3D) [reset = 0x0x0088]

Figure 138. Serdes Configuration 1 Register (SRDS_CFG1)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 133. RDS_CFG1 Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0	Reserved
14:12	TESTPATT	R/W	000	Test pattern
11	BSINRXN	R/W	0	Enable boundary scan - pins
10	BSINRXP	R/W	0	Enable boundary scan + pins
9:8	Reserved	R/W	00	Reserved
7	ENOC	R/W	1	Enable Serdes offset compensation
6	EQHLD	R/W	0	Equalizer hold
5:3	EQ	R/W	001	Serdes equalizer
2:0	CDR	R/W	000	Clock data recovery algorithm settings

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8.5.87 Serdes Configuration 2 Register (address = 0x3E) [reset = 0x0x0909]

Figure 139. Serdes Configuration 2 Register (SRDS_CFG2)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 134. SRDS_CFG2 Field Descriptions

Bit	Field	Type	Reset	Description
15:13	LOS	R/W	000	Enables loss of signal detection. 000 - Disable detection 100 - Enable detection other - reserved
12:11	ALIGN	R/W	01	Enables external or internal symbol alignment 00 : Disabled 01 : Comma alignment 10: Align jog
10:8	TERM	R/W	001	Valid programming: 001 – AC coupling with common mode = 0.7 V 100 – 0 V common mode. 101 – 0.25 V common mode 111 – DC coupling with common mode of 0.6 V. (NOTE: This is not compatible with JESD)
7	Reserved	R/W	0	Reserved
6:5	RATE	R/W	00	Selects full (00), half (01), quarter (10) or eighth (11) rate operation.
4:2	BUSWIDTH	R/W	010	Selects the parallel interface width (16 or 20 bits). 0 : 20 bits 1: 16 bits
1	SLEEPRX	R/W	0	Powers the receiver down into the sleep (fast power up) state when high.
0	Reserved	R/W	1	Reserved

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8.5.88 Serdes Polarity Control Register (address = 0x3F) [reset = 0x0000]

Figure 140. Serdes Polarity Control Register (SRDS_POL)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 135. SRDS_POL Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	R/W	0x00	Reserved
7:0	INVPAIR	R/W	0x00	Allows the PN pairs of the different lanes to be inverted. bit 7 = lane7 bit 6 = lane6 bit 5 = lane5 bit 4 = lane4 bit 3 = lane3 bit 2 = lane2 bit 1 = lane1 bit 0 = lane0

8.5.89 JESD204B SYNCB OUTPUT Register (address = 0x76) [reset = 0x0000]

Figure 141. JESD204B SYNCB OUTPUT Register (SYNCBOUT)

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
0	0	1	1	1	0	1	1
R/W	R/W	R/1W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 136. SYNCBOUT Field Descriptions

Bit	Field	Type	Reset	Description
15:2	Reserved	R/W	0x00	Reserved
1	SYNCBOUT1	R/W	0	If the CMOS SYNC outputs are turned on, this bit will show the status of the JESD SYNCB1 signal
0	SYNCBOUT0	R/W	0	If the CMOS SYNC outputs are turned on, this bit will show the status of the JESD SYNCB0 signal

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Start-up Sequence

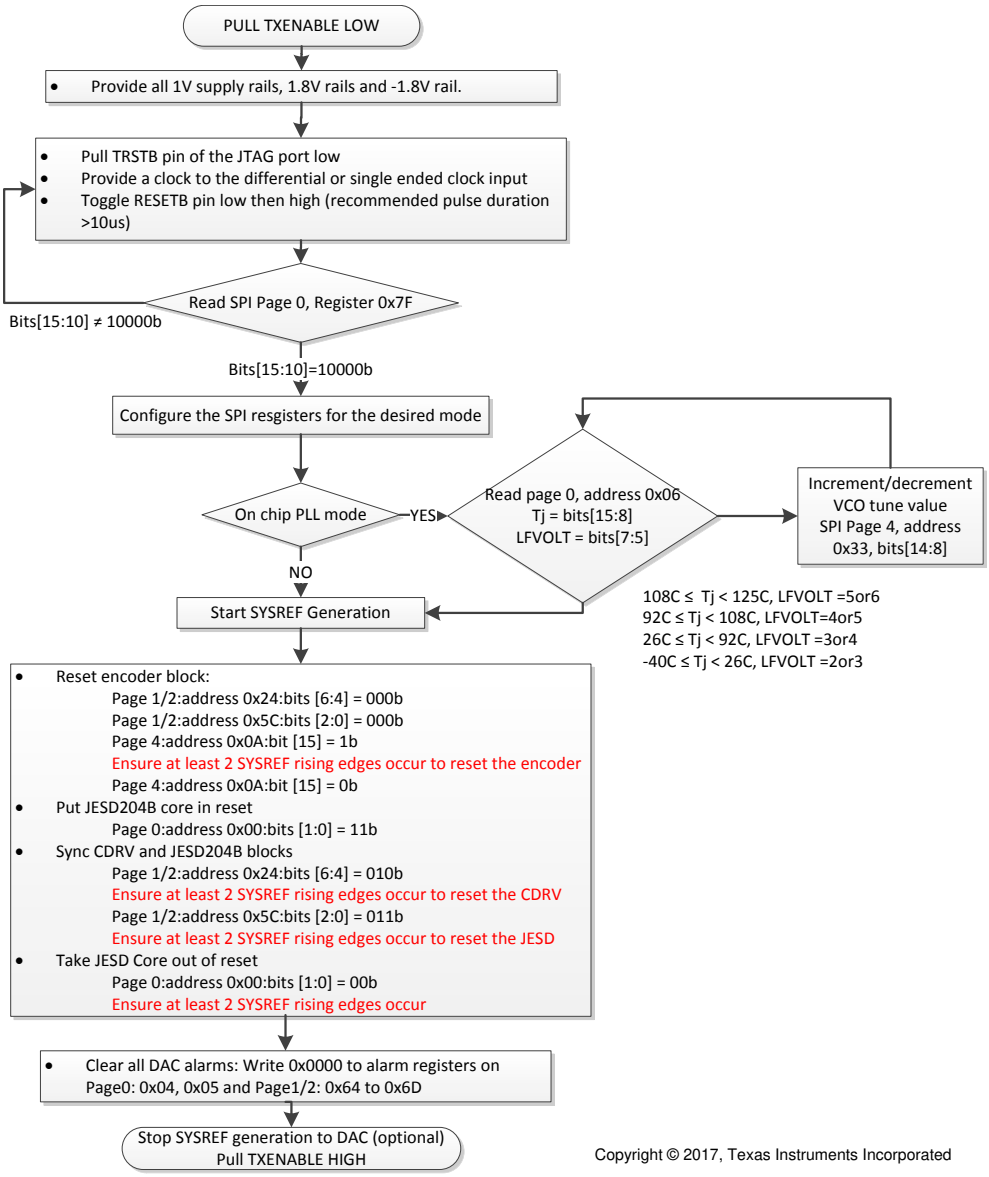

图 142. DAC38RF82/89 Recommended Startup Sequence

9.2 Typical Application

The block diagram of a typical DOCSIS downstream network is shown in 图 143. The physical layer (PHY) of the cable modem termination system (or CMTS) must support normal downstream operating range from 54 MHz to 1002 MHz as well as extended operating range up to 1794 MHz. The high input bandwidth (up to 3.33 GHz) of DAC38RF82 and DAC38RF89 makes these devices suitable for DOCSIS CMTS. Also the integrated high performance PLL simplifies system clocking by eliminating the need to generate and distribute high frequency sampling clock to the DAC. In the following sections, the performance of DAC38RF82 (and DAC38RF89) used to generate DOCSIS 3.0, Annex A, 6 MHz 256-QAM carriers will be described.

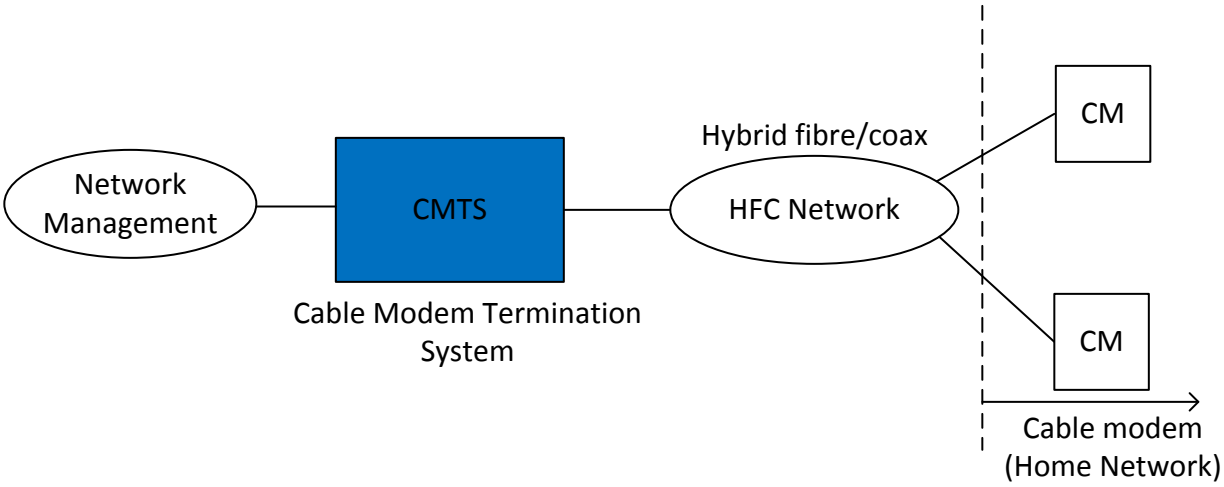

图 143. DOCSIS Downstream Network

9.2.1 Design Requirements

表 137. DOCSIS CMTS Design Features

Feature	Specification
Frequency range	54 MHz to 1002 MHz
No of carriers	1
Channel width	6 MHz
Modulation type	256 QAM
Modulation rate	5.3605 Msym/s
Data rate	2.4576 GSPS
MER (unequalized)	>48 dB
ACPR	>70 dBc

9.2.2 Detailed Design Procedure

A sample rate of 4.9152 GHz is selected for the DAC. This will make it possible to meet the out of band (up to 3GHz) spurious requirement of 65 dBc by pushing the DAC images to the 2nd Nyquist zone (2.4576 MHz to 4.9152 GHz). Because the input data rate is 2.4576 GSPS, the DAC interpolation is set to 2. To generate the 4.9152 GHz sampling clock for the DAC, a low frequency 409.6 MHz clock is provided to the DAC reference clock input. A detailed block diagram is shown in 图 144

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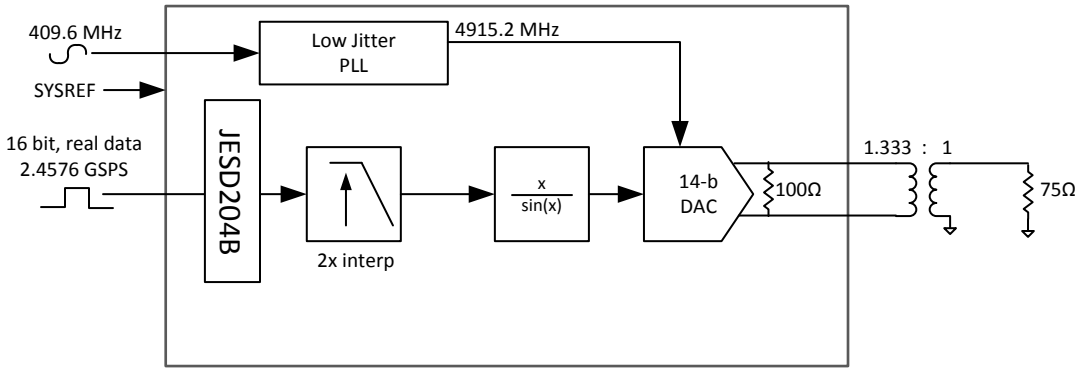

图 144. DOCSIS Downstream Network

9.2.3 Calculating the JESD204B SerDes rate

SerDes rate = 1.25 x (M/L) x Baseband data rate x Number of bits per sample (16)

M is a JESD204B interface parameter that refers to the number of data streams from FPGA to DAC

L is a JESD204B interface parameter that refers to the number of SerDes lanes used to transmit data

1.25 is a factor due to the 8B10B encoding of the baseband data

Example,

if the baseband data rate = 2457.6 MSPS and L-M-F-S-Hd = 4-1-1-2-1

$$\text{SerDes rate} = 1.25 \times (1/4) \times 2457.6 \times 16 = 12.288 \text{ Gbps} \quad (19)$$

9.2.4 Calculating valid JESD204B SYSREF Frequency

Valid SYSREF frequencies depend on the following parameters:

1. Sample clock frequency
2. JESD204B internal clock divider value (CLKJESD_DIV). This depends on the DAC JESD204B L-M-F-S mode and interpolation
3. Number of octets in a frame (F)
4. Number of frames in a multi-frame (K)

Maximum SYSREF frequency = (Sample clock frequency/N),

where N =LCM(CLKJESD_DIV,4 x K x F). N is the Least common multiple of 4 x K x F and CLKJESD_DIV.

All valid SYSREF frequencies are integer divisors of the maximum SYSREF frequency.

Example:

Given sampling clock frequency = 4.9152 GSPS, interpolation =2, DAC Mode=L-M-F-S=4-1-1-2 and K=20:

CLKJESD_DIV = 8 (CLKJESD_DIV)

Maximum SYSREF Frequency = 4915.2 MHz/80 = 61.44 MHz

Valid SYSREF Frequencies = 61.44 MHz/n, where n is any positive integer.

9.2.5 Application Curves

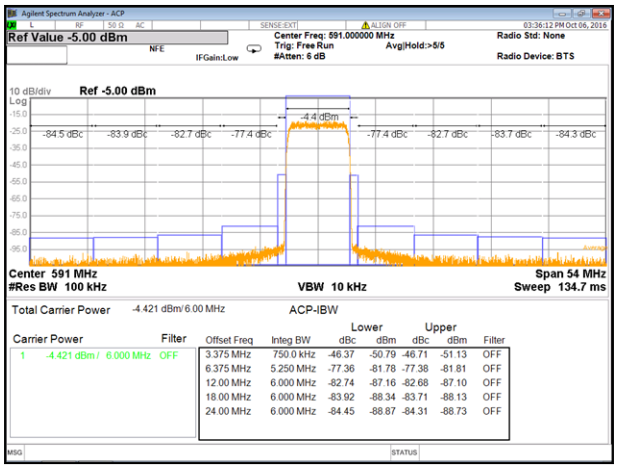

图 145. ACPR Performance of 6 MHz Single Carrier at 591 MHz

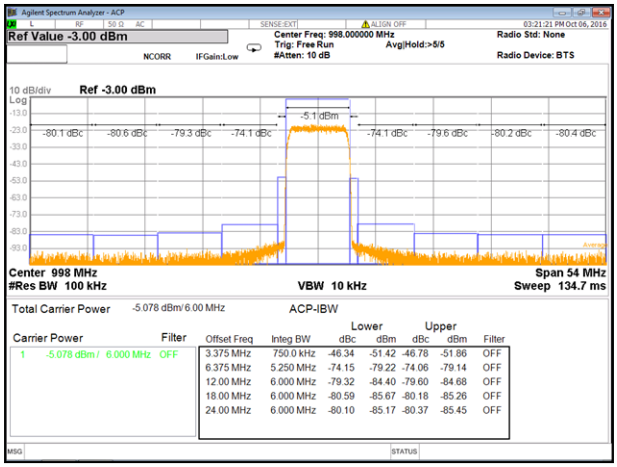

图 146. ACPR performance of 6 MHz Single Carrier at 998 MHz

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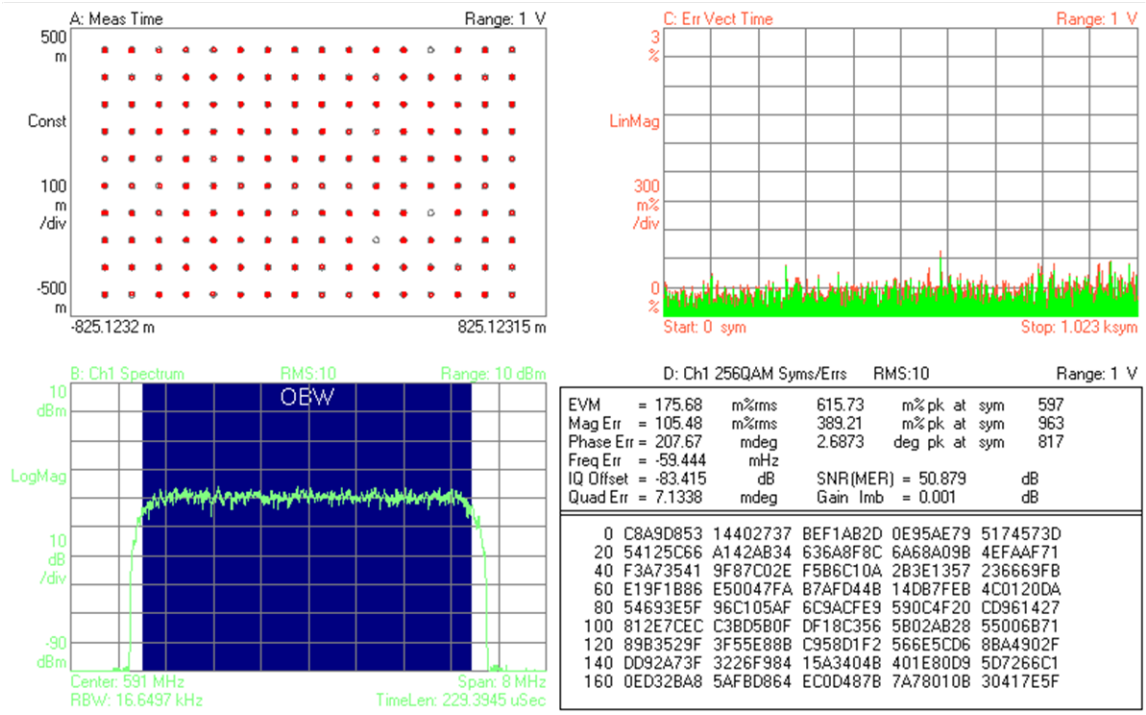

图 147. Unequalized MER of 6 MHz Single Carrier at 591 MHz

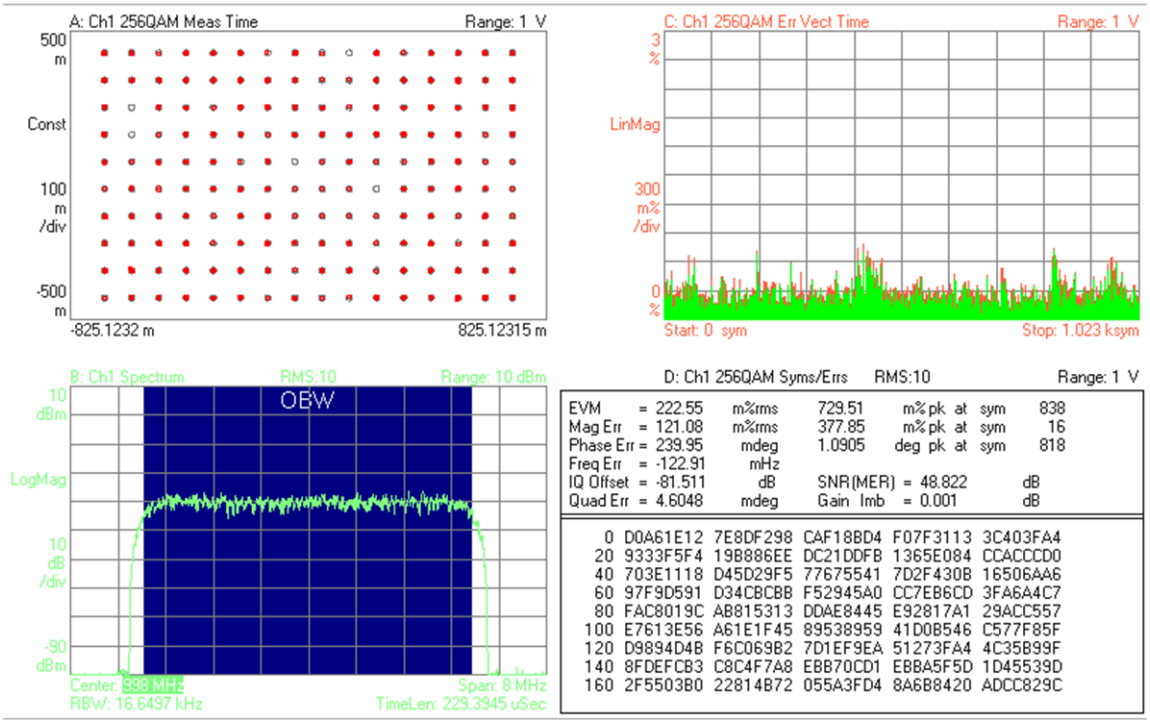

图 148. Unequalized MER of 6 MHz Single Carrier at 998 MHz

10 Power Supply Recommendations

Internally, DAC38RF82 (DAC38RF89) comprises a digital subsystem, an analog subsystem, and a clock subsystem. Ideally, the power supply scheme should be partitioned according to these three relatively independent blocks to minimize interactions between them. Most importantly, sensitive analog and clock circuit power supply must be separated from digital switching noise to reduce direct coupling and mixing of switching spurs. 表 138 shows the power supply rails for DAC38RF82 (DAC38RF89) grouped under their respective domains.

表 138. Power Supply Domains

Supply rail	Nominal voltage (V)	Domain
VDDIG1	+1.0	Digital
VDDIO18	+1.8	
VDDR18	+1.8	
VDDS18	+1.8	
VDDT1	+1.0	
VDDE1	+1.0	
VDDL1_1	+1.0	
VEE18N	-1.8	Analog
VDDA1	+1.0	
VDDA18	+1.8	
VDDOUT18	+1.8	
VDDPLL1	+1.0	Clock
VDDAPLL18	+1.8	
VDDAVCO18	+1.8	
VDDCLK1	+1.0	
VDDL2_1	+1.0	
VDDTX1	+1.0	
VDDTX18	+1.8	

An example power supply scheme suitable for most applications of DAC38RF82 (DAC38RF89) is shown in 图 149. It is recommended to use ferrite beads (FB) to isolate the individual rails from each other.

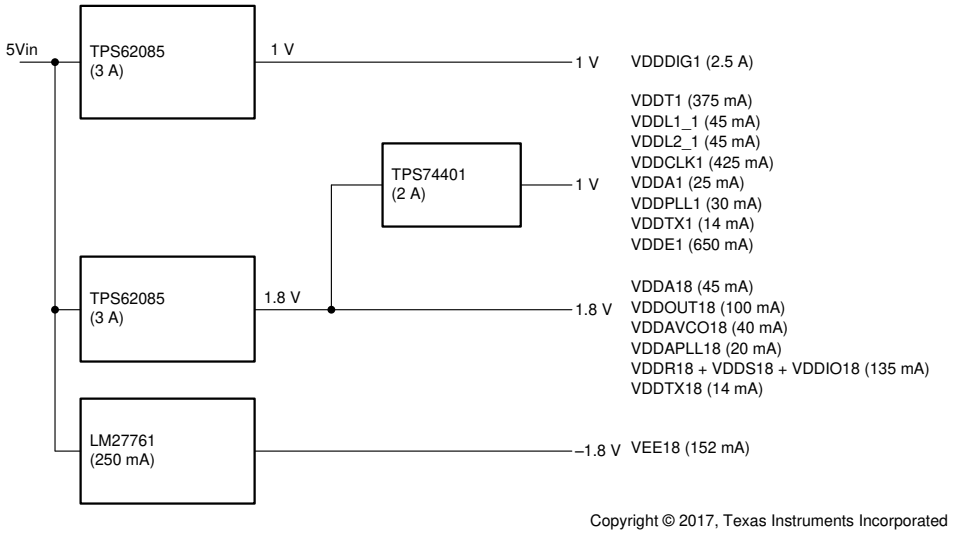

图 149. Power Supply Scheme for DAC38RF82 (DAC38RF89)

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10.1 Power Supply Sequencing

There are no power supply sequencing requirements for all the 1-V and 1.8-V power supplies. For the -1.8 V VEE18 rail, it is recommended that this supply is the last to be enabled. Enabling VEE18 (while other supply voltages are disabled) can cause a small negative voltage to be present at the other rails (that is, VDDA1 and VDDDIG1). This small negative voltage can interfere with the startup of some DC-DC converters or LDO connected to the 1 V and 1.8 V input power rails.

11 Layout

11.1 Layout Guidelines

- DAC RF output traces
  - Differential 100 Ω co-planar wave guide for output traces is recommended.
  - Use short RF traces. Place DAC close to edge of PCB to shorten the length of output and clock traces. This helps to minimize PCB loss and coupling
  - Stitch the ground plane with ground vias uniformly along the output trace.
  - Avoid width/spacing differences when entering a landing pad (eg. a balun) by tapering or by redefining width/space rules for the traces
- Power supply planes
  - Ensure sufficient lateral spacing between two power planes (about 3x the thickness of the plane is recommended)
  - Insert ground plane between adjacent power planes where possible

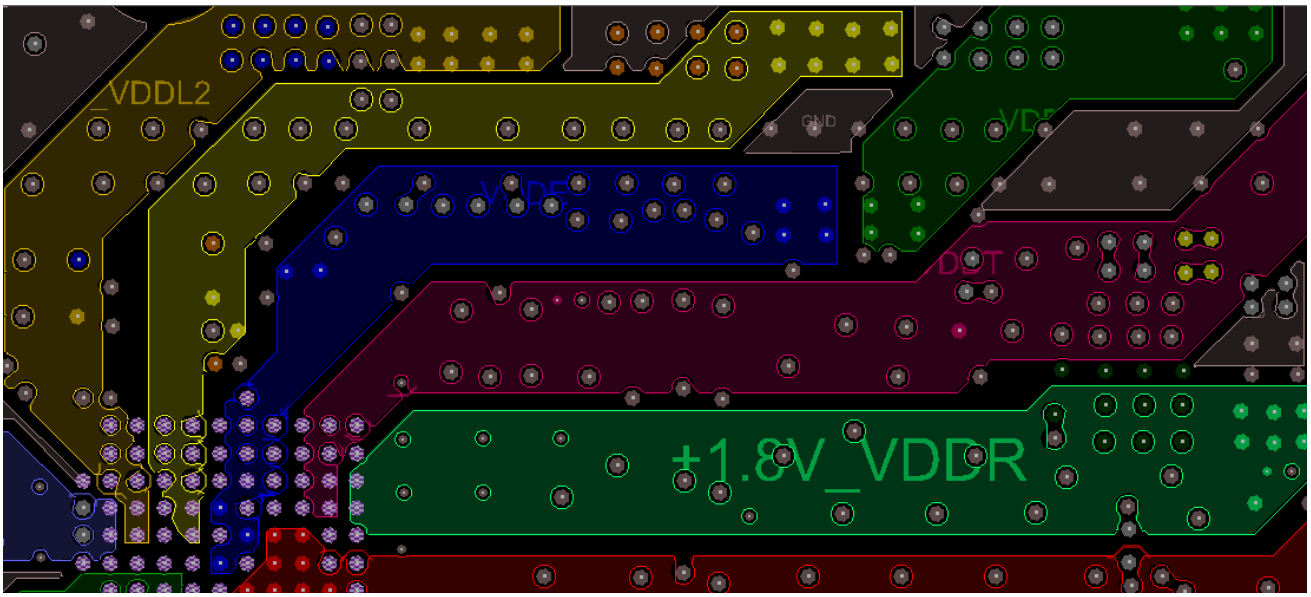

图 150. Example Power Plane Routing

- Bypass Capacitors
  - Use bypass capacitors with in-pad vias and place between the pin and the power plane. Avoid sharing ground vias or pads of bypass caps used for different power rails
  - Minimize stubs on bypass capacitors to avoid parasitic inductance

Layout Guidelines (接下页)

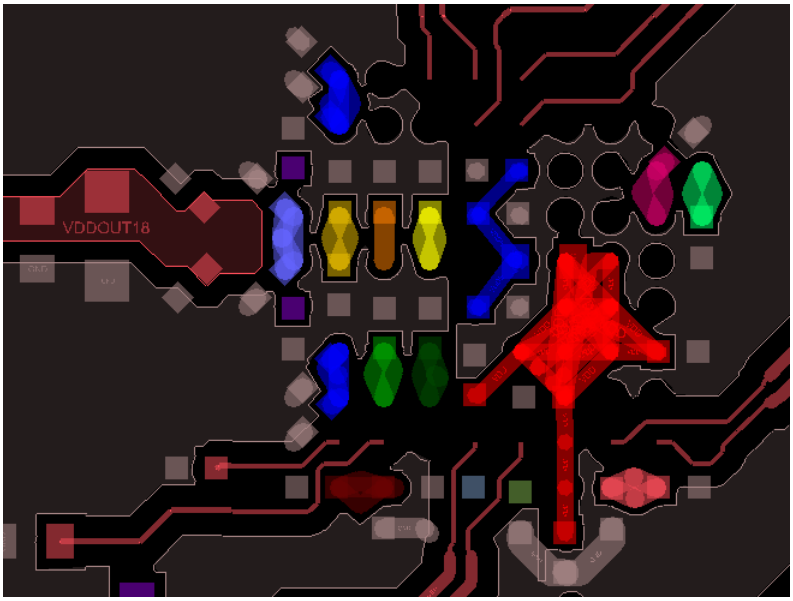

图 151. Bypass Capacitors Placed on the Power Supply Pin With In-pad Vias

- High speed SerDes traces
  - Route all SerDes traces straight and minimized sharp curves or serpentines. Route for best signal integrity
  - Some skew between SerDes traces can be tolerated. It is recommended to limit skew between traces to 320ps or less
  - Place ground planes between the SerDes traces for improved isolation

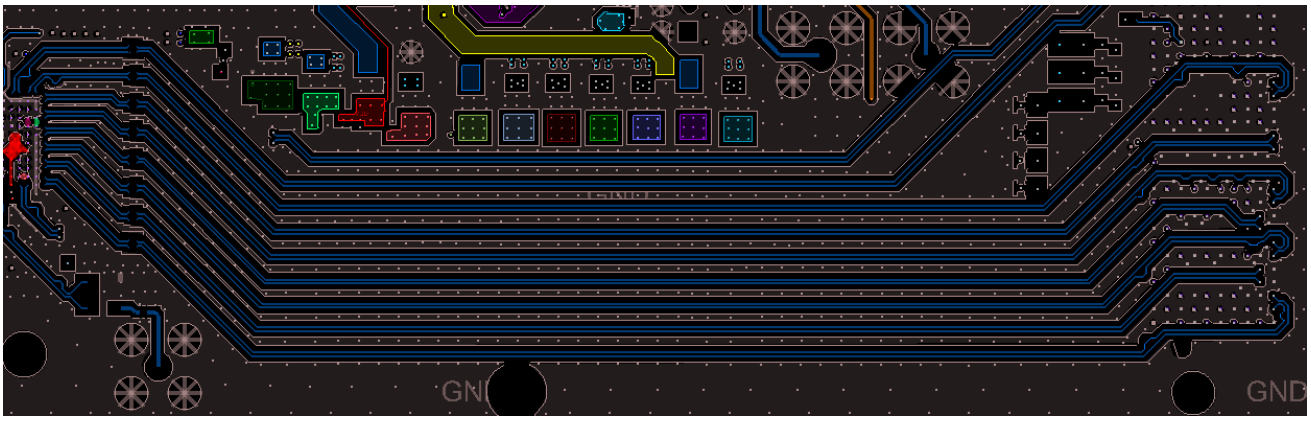

图 152. Layout Example of High Speed SerDes Traces

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11.2 Layout Example

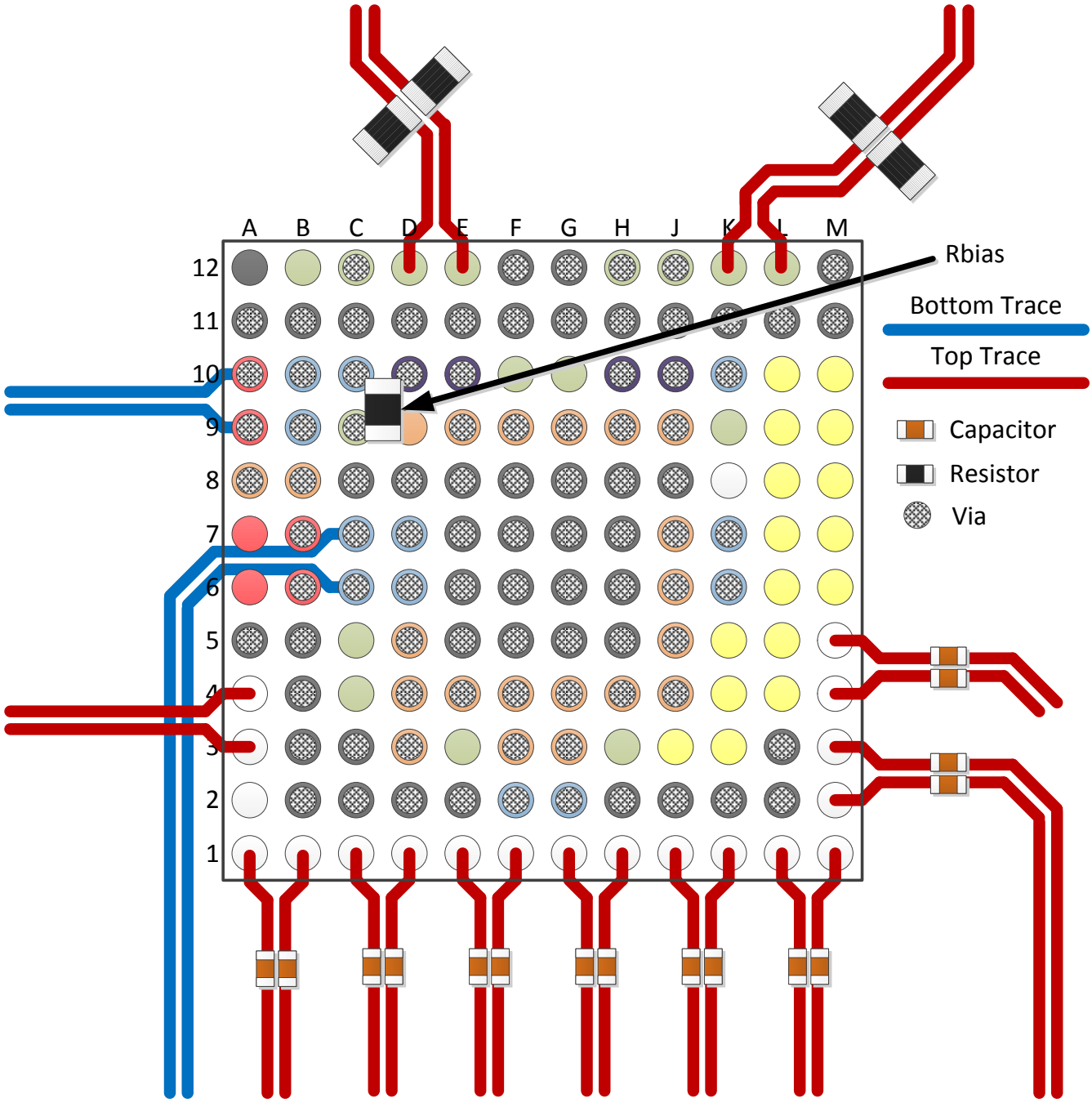

图 153. Layout Example

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **139.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
DAC38RF82	单击此处	单击此处	单击此处	单击此处	单击此处
DAC38RF89	单击此处	单击此处	单击此处	单击此处	单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 静电放电警告

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC38RF82IAAV	Active	Production	FCCSP (AAV) | 144	168 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF82I
DAC38RF82IAAVR	Active	Production	FCCSP (AAV) | 144	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF82I
DAC38RF89IAAV	Active	Production	FCCSP (AAV) | 144	168 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF89I
DAC38RF89IAAVR	Active	Production	FCCSP (AAV) | 144	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DAC38RF89I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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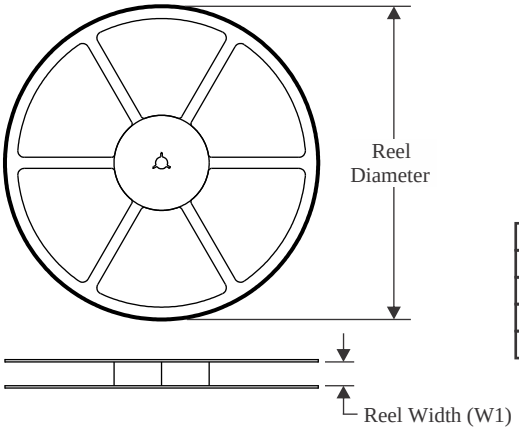
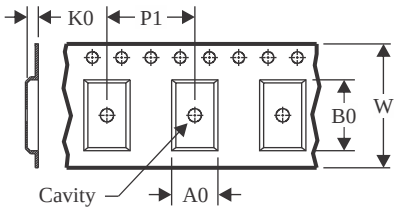
TAPE AND REEL INFORMATION

REEL DIMENSIONS

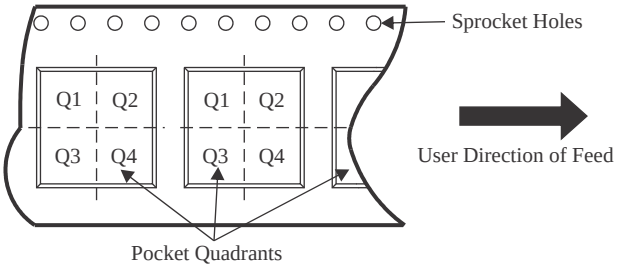


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

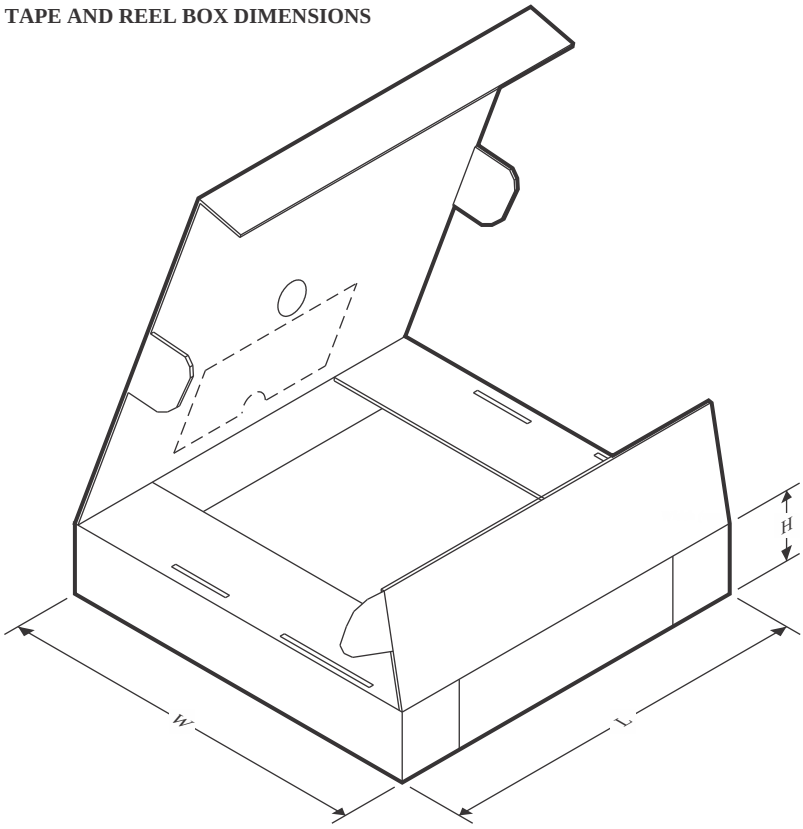
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC38RF82IAAVR	FCCSP	AAV	144	1000	330.0	24.4	10.3	10.3	2.5	16.0	24.0	Q1
DAC38RF89IAAVR	FCCSP	AAV	144	1000	330.0	24.4	10.3	10.3	2.5	16.0	24.0	Q1

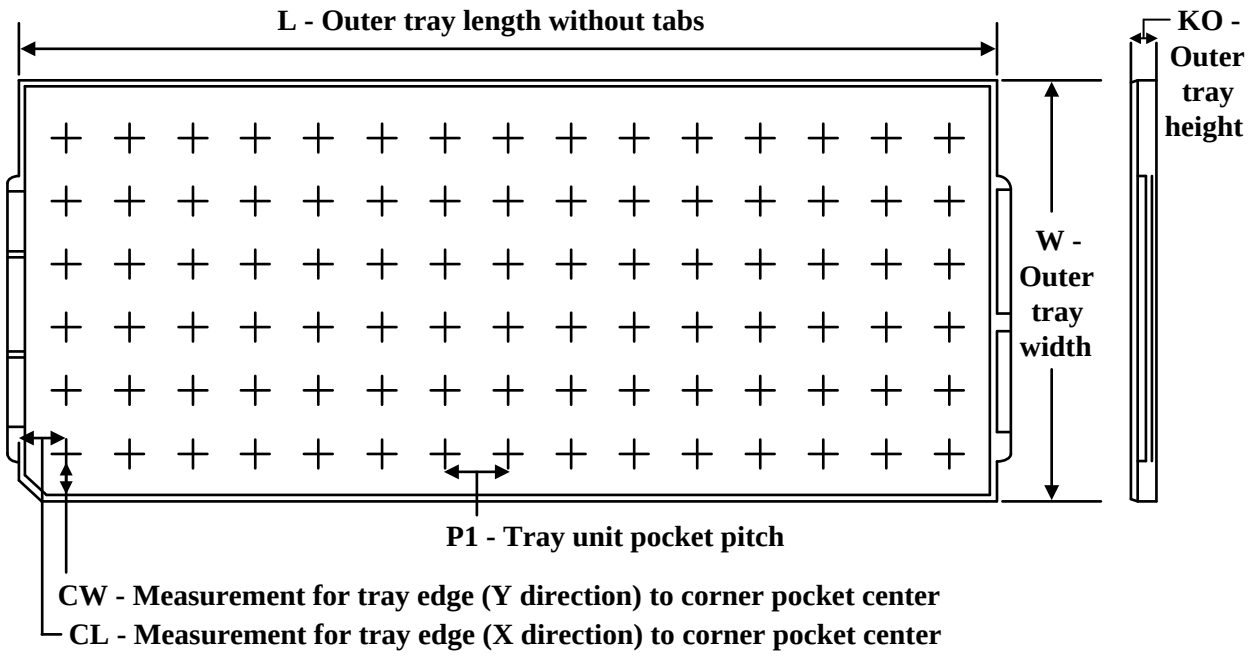
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC38RF82IAAVR	FCCSP	AAV	144	1000	350.0	350.0	43.0
DAC38RF89IAAVR	FCCSP	AAV	144	1000	350.0	350.0	43.0

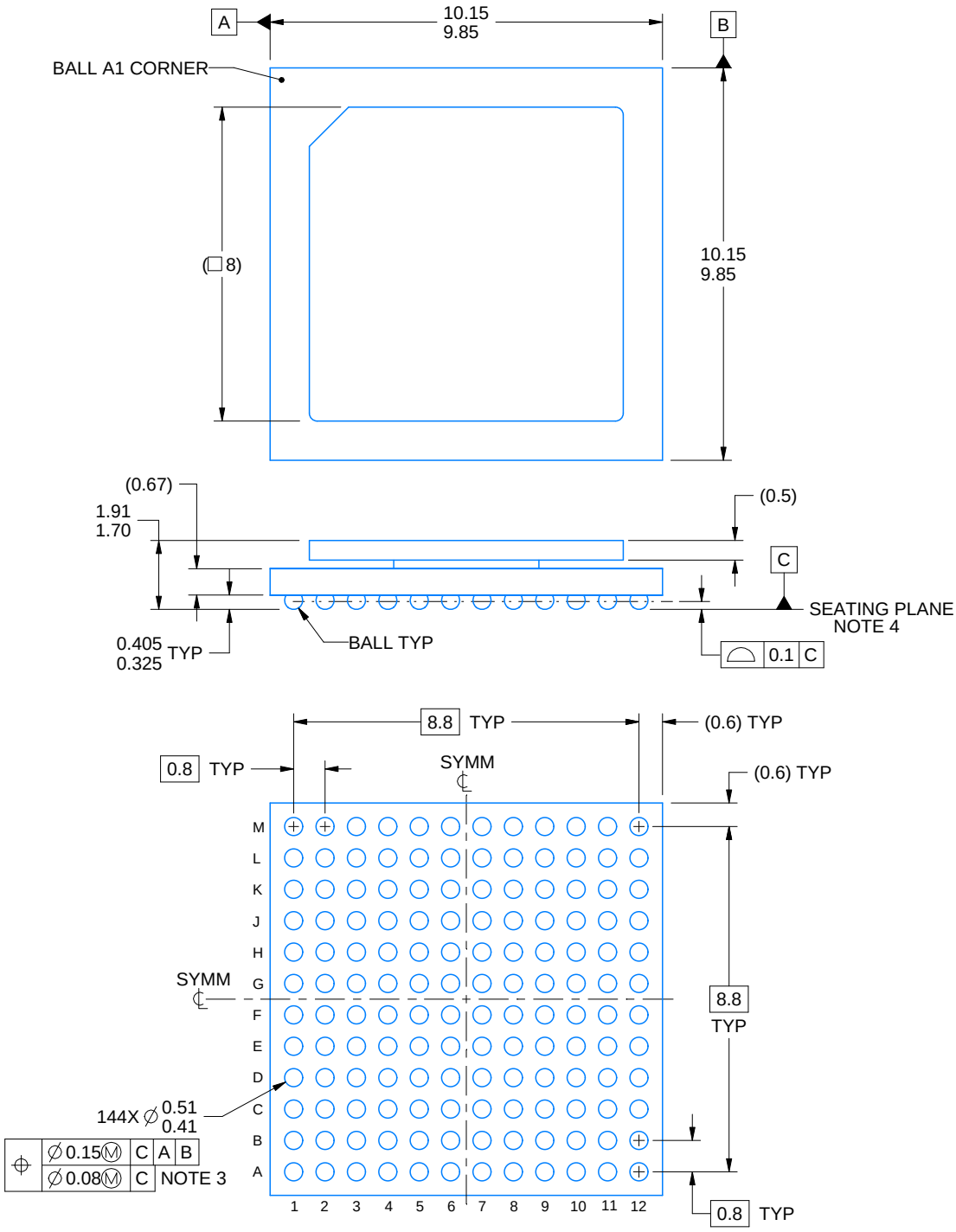
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

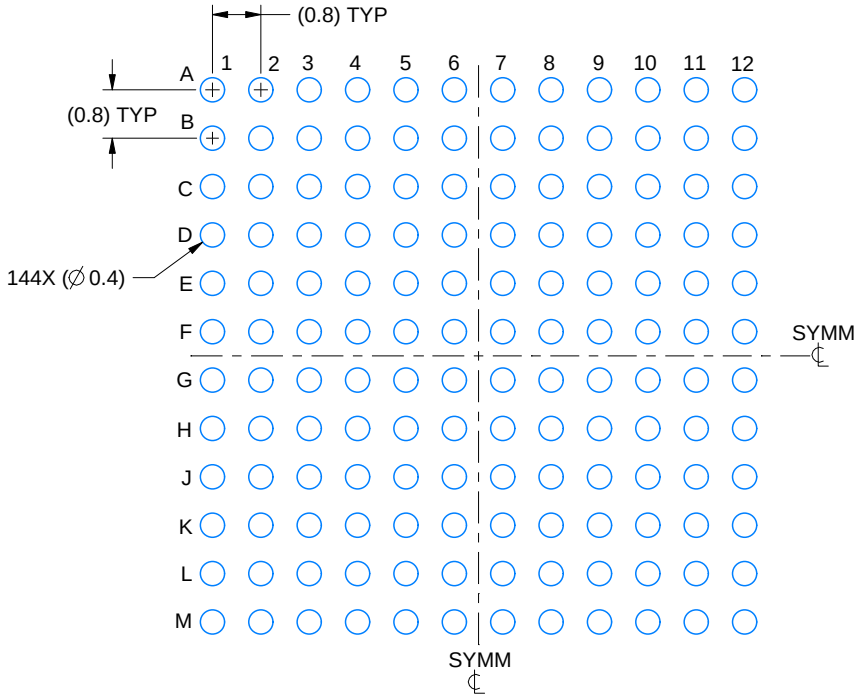
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC38RF82IAAV	AAV	FCCSP	144	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
DAC38RF89IAAV	AAV	FCCSP	144	168	8 X 21	150	315	135.9	7620	14.65	11	11.95

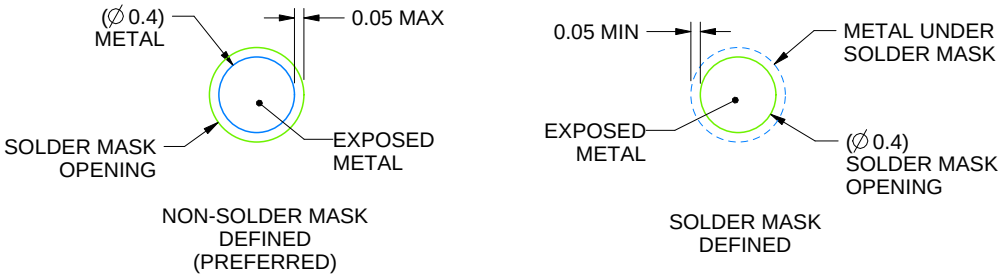


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

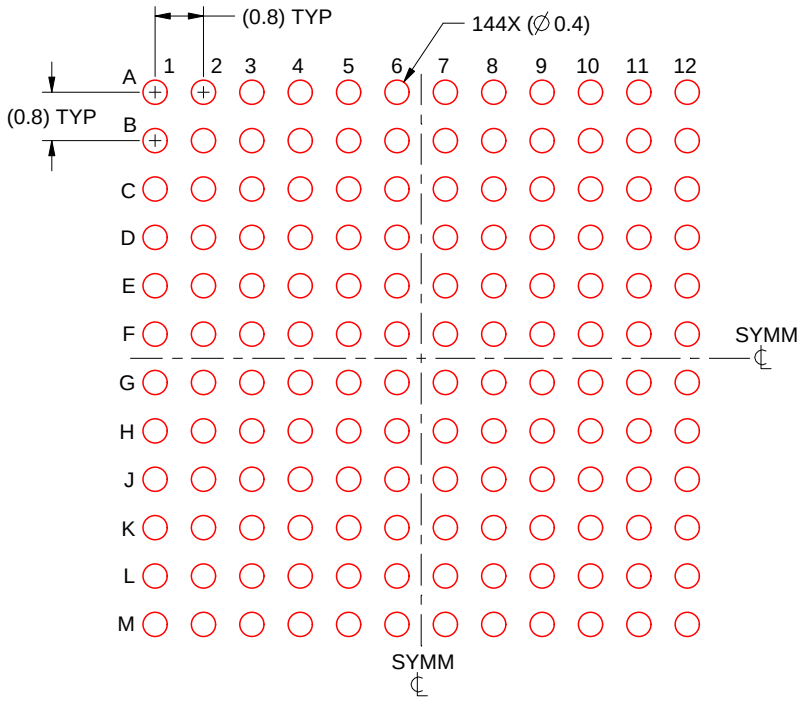


SOLDER MASK DETAILS
NOT TO SCALE

4219578/D 03/2023

NOTES: (continued)

6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4219578/D 03/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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