

# CSD75207W15 双路 P 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

## 1 特性

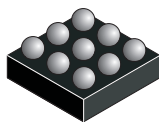
- 双路 P 通道 MOSFET
- 共源配置
- 小型封装尺寸 1.5mm x 1.5mm
- 栅极 - 源电压钳位
- 栅极静电放电 (ESD) 保护大于 4kV
  - 人体模型 (HBM) JEDEC 标准 JESD22-A114
- 无铅且无卤素
- 符合 RoHS 环保标准

## 2 应用范围

- 电池管理
- 电池保护
- 负载和输入开关

## 3 说明

CSD75207W15 器件设计用于在超薄且具有出色散热特性的超小外形尺寸封装内产生尽可能低的导通电阻和栅极电荷。低导通电阻与小型封装尺寸和低高度结合在一起，使得此器件非常适用于电池供电运行的空间受限应用。此器件也已经被授予美国专利 7952145, 7420247, 7235845 和 6600182。



### 产品概要

T <sub>A</sub> = 25°C		典型值		单位
V <sub>D1D2</sub>	漏极-漏极电压	-20		V
Q <sub>g</sub>	栅极电荷总量 (-4.5V)	2.9		nC
Q <sub>gd</sub>	栅漏栅极电荷	0.4		nC
R <sub>D1D2 (导通)</sub>	漏极到漏极导通电阻	V <sub>GS</sub> = -1.8V	119	mΩ
		V <sub>GS</sub> = -2.5V	64	mΩ
		V <sub>GS</sub> = -4.5V	45	mΩ
V <sub>GS(th)</sub>	阈值电压	-0.8		V

### 订购信息<sup>(1)</sup>

器件	封装	介质	数量	出货
CSD75207W15	1.5mm x 1.5mm 晶圆级封装	7 英寸卷带	3000	卷带封装

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

### 最大绝对额定值

T <sub>A</sub> = 25°C		值	单位
V <sub>D1D2</sub>	漏极-漏极电压	-20	V
V <sub>GS</sub>	栅源电压	-6.0	V
I <sub>D1D2</sub>	持续漏极到漏极电流 <sup>(1) (2)</sup>	-3.9	A
	脉冲漏极到漏极电流，T <sub>C</sub> = 25°C <sup>(3)</sup> 时测得	-24	A
I <sub>S</sub>	持续源引脚电流	-1.2	A
	<sup>(3)</sup> 脉冲源引脚电流	-15	A
I <sub>G</sub>	持续栅极钳位电流	-0.5	A
	脉冲栅极钳位电流 <sup>(3)</sup>	-7	A
P <sub>D</sub>	功率耗散 <sup>(1)</sup>	0.7	W
T <sub>J</sub> , T <sub>stg</sub>	运行结温和储存温度范围	-55 至 150	°C

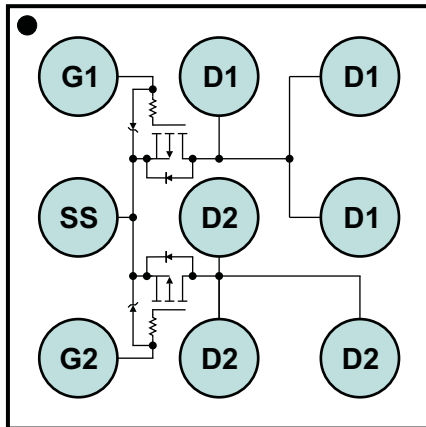
(1) 每个器件两侧均导电

(2) 器件在 105°C 温度下运行

(3) 脉冲持续时间 10μs, 占空比 ≤ 2%

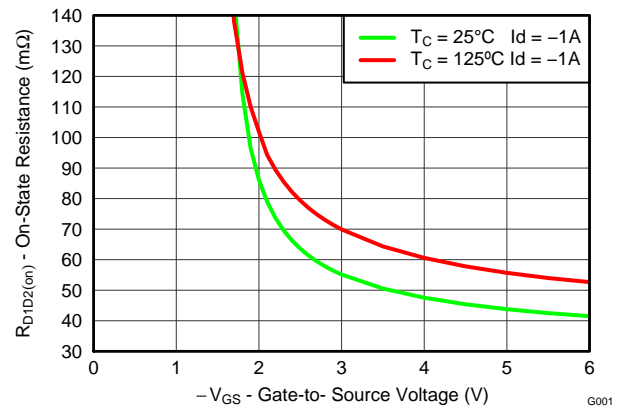


顶视图



P0109-01

$R_{D1D2}$  (导通) 与  $V_{GS}$  间的关系



## 目录

<b>1 特性</b> ..... 1 <b>2 应用范围</b> ..... 1 <b>3 说明</b> ..... 1 <b>4 修订历史记录</b> ..... 3 <b>5 Specifications</b> ..... 4 5.1 Electrical Characteristics..... 4 5.2 Thermal Information ..... 4 5.3 Typical MOSFET Characteristics..... 5	<b>6 器件和文档支持</b> ..... 8 6.1 商标 ..... 8 6.2 静电放电警告..... 8 6.3 术语表 ..... 8 <b>7 机械封装和可订购信息</b> ..... 9 7.1 CSD75207W15 封装尺寸..... 9 7.2 建议印刷电路板 (PCB) 焊盘图案..... 10 7.3 卷带封装信息..... 10
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## 4 修订历史记录

### Changes from Original (June 2013) to Revision A

**Page**

<ul style="list-style-type: none"> <li>• 持续漏极到漏极电流增加至 3.9A ..... 1</li> <li>• 更新了持续漏极到漏极电流条件，指定温度为 105°C..... 1</li> </ul>	<p>1</p> <p>1</p>
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## 5 Specifications

### 5.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated). Specifications and graphs are Per MOSFET unless otherwise stated. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

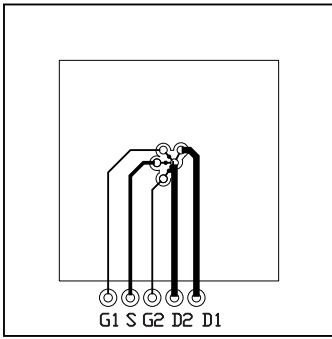
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{D1D2}$	Drain-to-Drain Voltage	$V_{GS} = 0\text{ V}, I_{D1D2} = -250\ \mu\text{A}$	-20			V
$BV_{GSS}$	Gate-to-Source Voltage	$V_{D1D2} = 0\text{ V}, I_G = -250\ \mu\text{A}$	-6			V
$I_{DDS}$	Drain-to-Drain Leakage Current	$V_{GS} = 0\text{ V}, V_{D1D2} = -16\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{D1D2} = 0\text{ V}, V_{GS} = -6\text{ V}$			-100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{D1D2} = V_{GS}, I_{DS} = -250\ \mu\text{A}$	-0.6	-0.8	-1.1	V
$R_{D1D2(on)}$	Drain-to-Drain On-Resistance	$V_{GS} = -1.8\text{ V}, I_{D1D2} = -1\text{ A}$		119	162	m $\Omega$
		$V_{GS} = -2.5\text{ V}, I_{D1D2} = -1\text{ A}$		64	77	m $\Omega$
		$V_{GS} = -4.5\text{ V}, I_{D1D2} = -1\text{ A}$		45	54	m $\Omega$
$g_{fs}$	Transconductance	$V_{D1D2} = -10\text{ V}, I_{D1D2} = -1\text{ A}$		6.2		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{D1D2} = -10\text{ V}, f = 1\text{ MHz}$		458	595	pF
$C_{OSS}$	Output Capacitance			225	293	pF
$C_{RSS}$	Reverse Transfer Capacitance			10.4	13.5	pF
$R_g$	Series Gate Resistance			27		$\Omega$
$Q_g$	Gate Charge Total (-4.5 V)	$V_{D1D2} = -10\text{ V}, I_{D1D2} = -1\text{ A}$		2.9	3.7	nC
$Q_{gd}$	Gate Charge – Gate to Drain			0.4		nC
$Q_{gs}$	Gate Charge – Gate to Source			0.7		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			0.4		nC
$Q_{OSS}$	Output Charge		$V_{D1D2} = -9.5\text{ V}, V_{GS} = 0\text{ V}$		3.1	
$t_{d(on)}$	Turn On Delay Time	$V_{D1D2} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_{D1D2} = -1\text{ A}, R_G = 30\ \Omega$		12.8		ns
$t_r$	Rise Time			8.6		ns
$t_{d(off)}$	Turn Off Delay Time			32.1		ns
$t_f$	Fall Time			16.0		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode Forward Voltage	$I_{D1D2} = -1\text{ A}, V_{GS} = 0\text{ V}$	-0.8	-1		V
$Q_{rr}$	Reverse Recovery Charge	$V_{dd} = -10\text{ V}, I_F = -1\text{ A}, di/dt = 200\text{ A}/\mu\text{s}$		10.5		nC
$t_{rr}$	Reverse Recovery Time	$V_{dd} = -10\text{ V}, I_F = -1\text{ A}, di/dt = 200\text{ A}/\mu\text{s}$		23		ns

### 5.2 Thermal Information

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

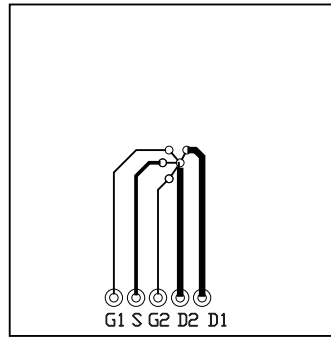
THERMAL METRIC		TYPICAL VALUE	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>(1) (2)</sup>	70	$^\circ\text{C}/\text{W}$
	Junction-to-Ambient Thermal Resistance <sup>(3) (2)</sup>	165	

- (1) Device mounted on FR4 material with Minimum Cu mounting area.
- (2) Measured with both devices biased in a parallel condition.
- (3) Device mounted on FR4 material with 1-inch<sup>2</sup> of Cu (2 oz).



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Typ  $R_{\theta JA} = 70^{\circ}\text{C/W}$   
when mounted on  
1-inch<sup>2</sup> of 2 oz. Cu.

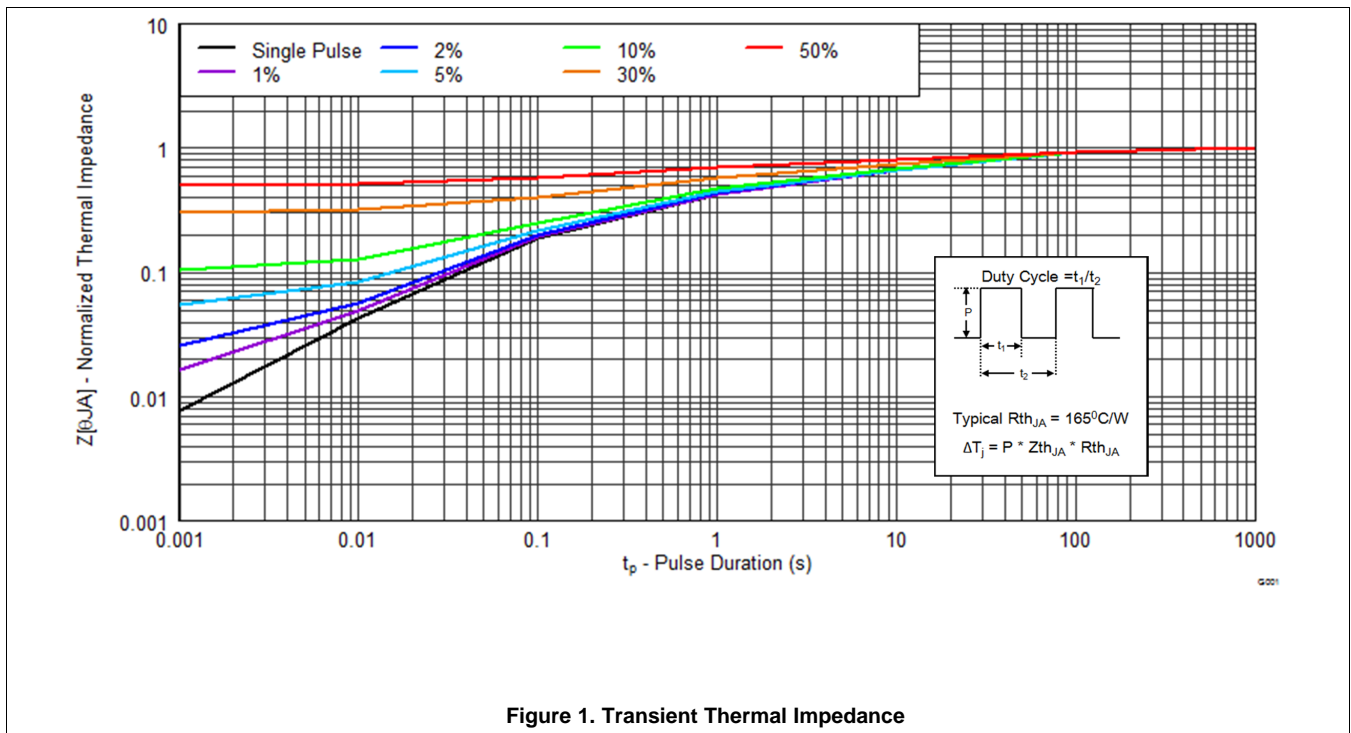


M0170-01

Typ  $R_{\theta JA} = 165^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of  
2-oz. Cu.

### 5.3 Typical MOSFET Characteristics

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

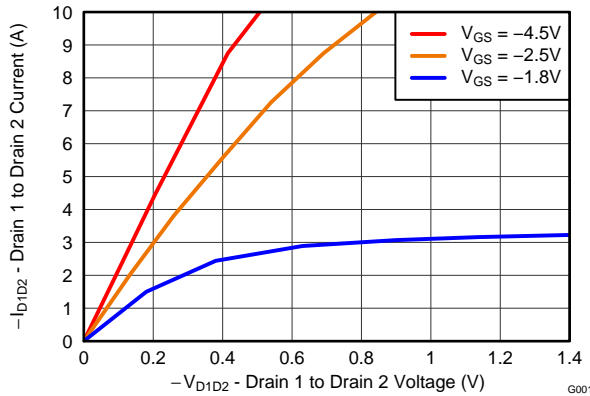


Figure 2. Saturation Characteristics

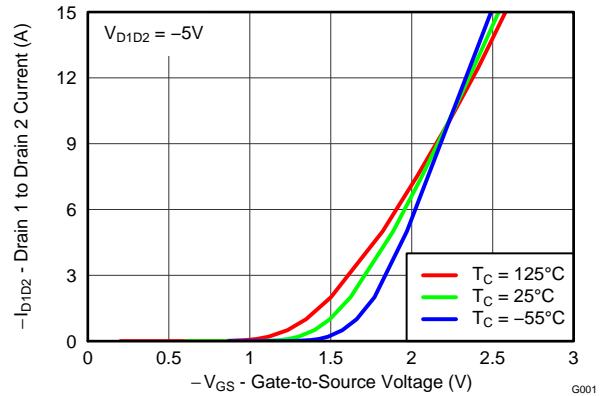


Figure 3. Transfer Characteristics

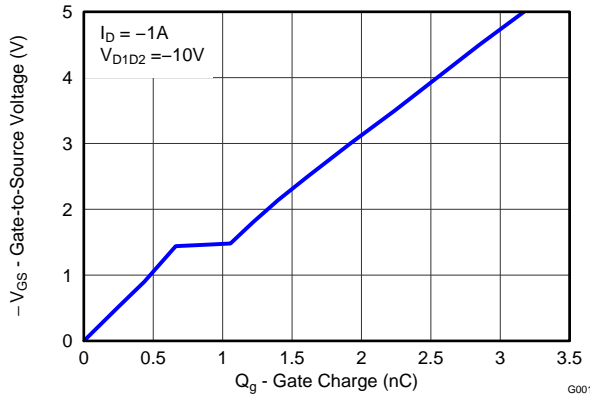


Figure 4. Gate Charge

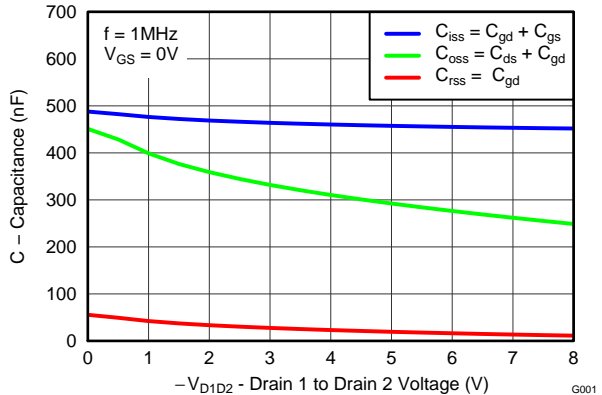


Figure 5. Capacitance

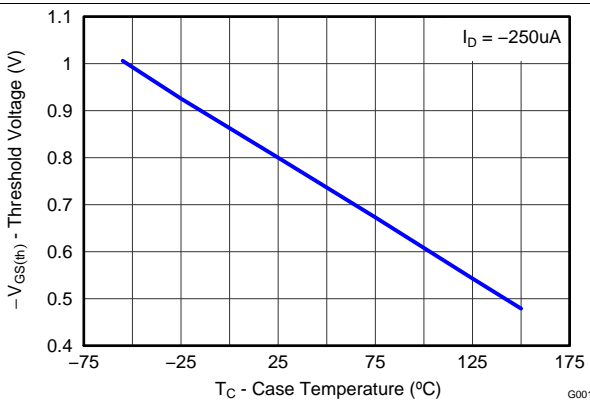


Figure 6. Threshold Voltage vs Temperature

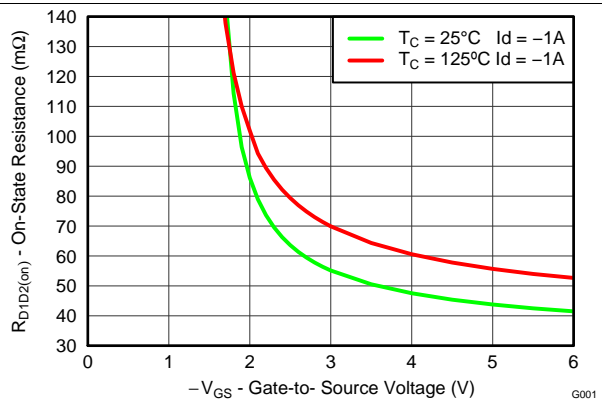


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

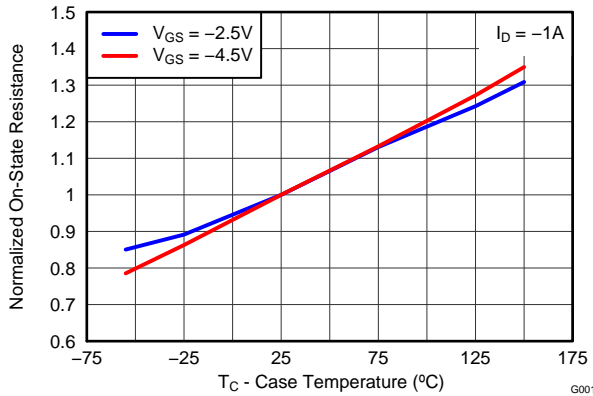


Figure 8. Normalized On-State Resistance vs Temperature

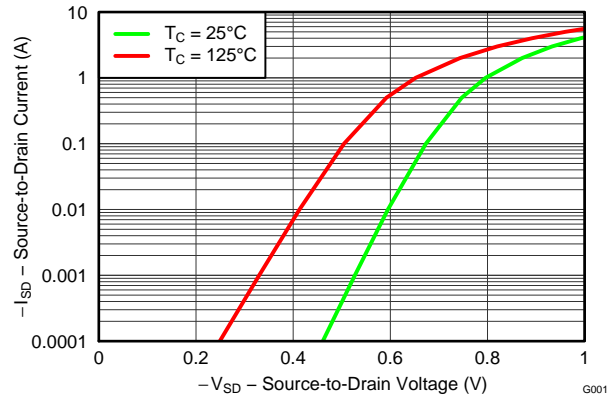


Figure 9. Typical Diode Forward Voltage

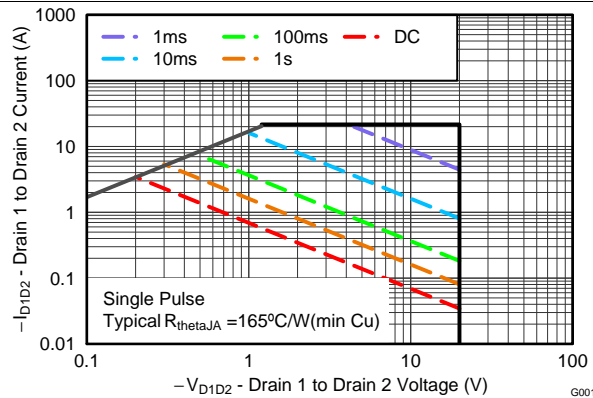


Figure 10. Maximum Safe Operating Area

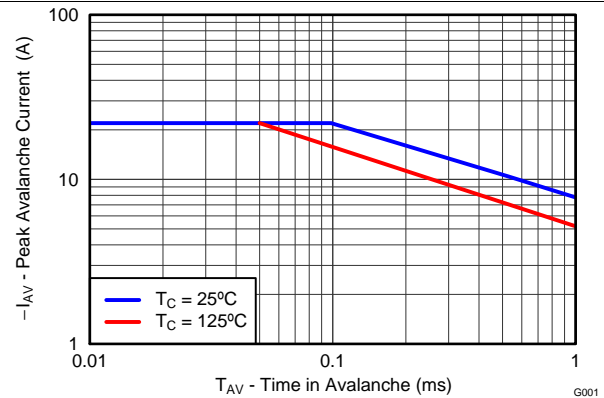


Figure 11. Single Pulse Unclamped Inductive Switching

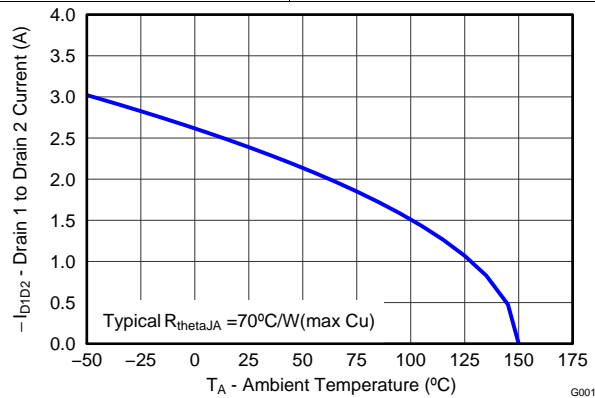


Figure 12. Maximum Drain Current vs Temperature

## 6 器件和文档支持

### 6.1 商标

NexFET is a trademark of Texas Instruments.

### 6.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 6.3 术语表

[SLYZ022](#) — *TI* 术语表。

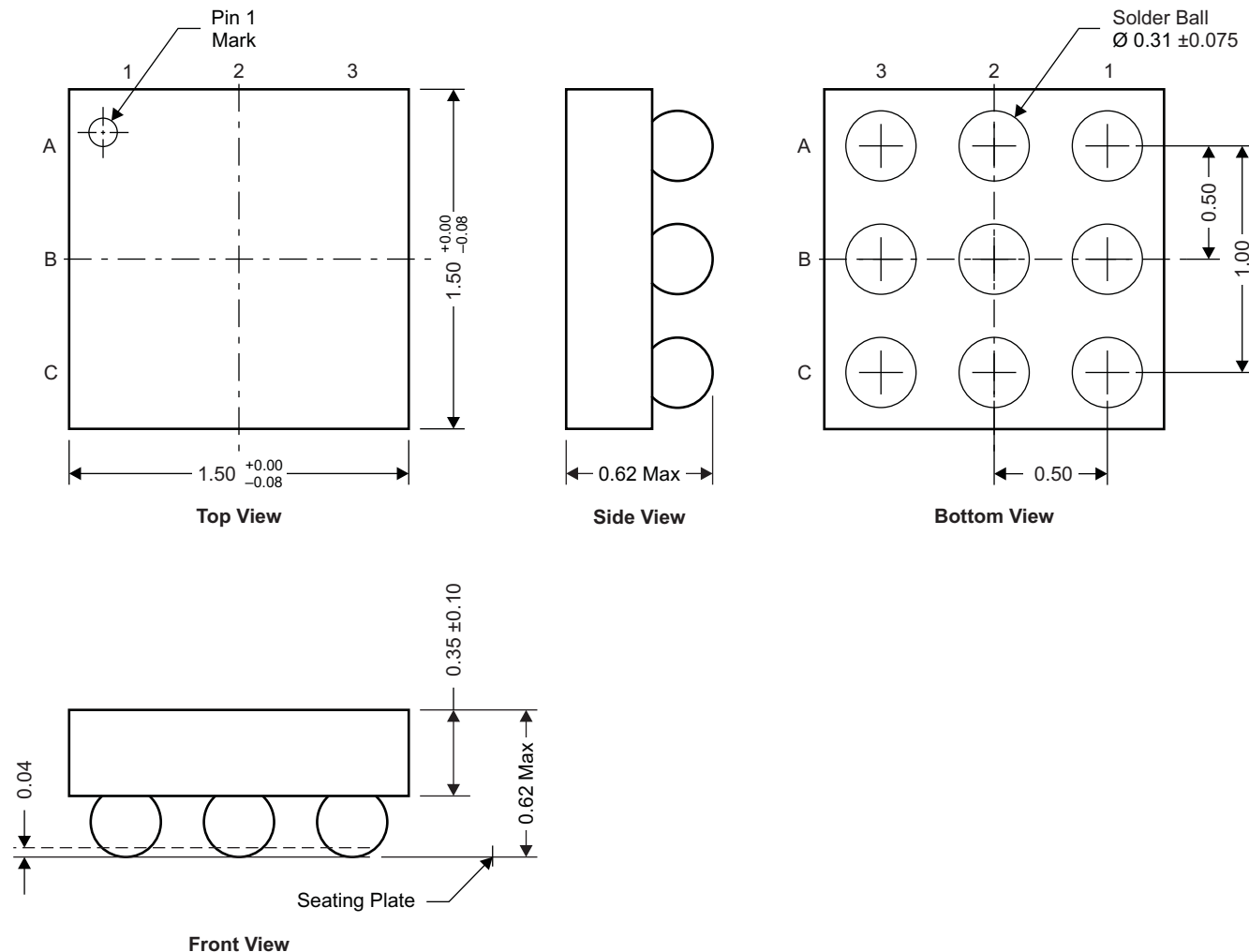
这份术语表列出并解释术语、首字母缩略词和定义。



## 7 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

### 7.1 CSD75207W15 封装尺寸



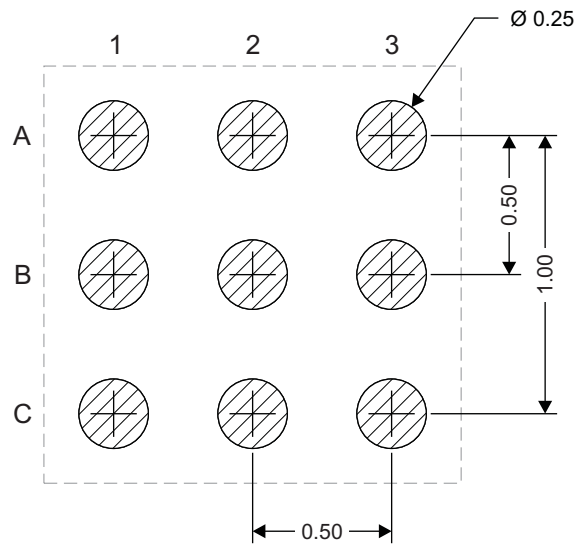
NOTE: 全部尺寸单位为 mm (除非另外注明)

M0171-01

#### 引脚分配

位置	名称
A1	栅极1
A2、A3 和 B3	Drain1
C1	Gate2
C2、C3 和 B2	Drain2
B1	源极检测

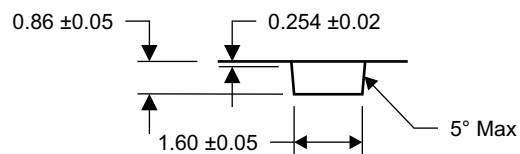
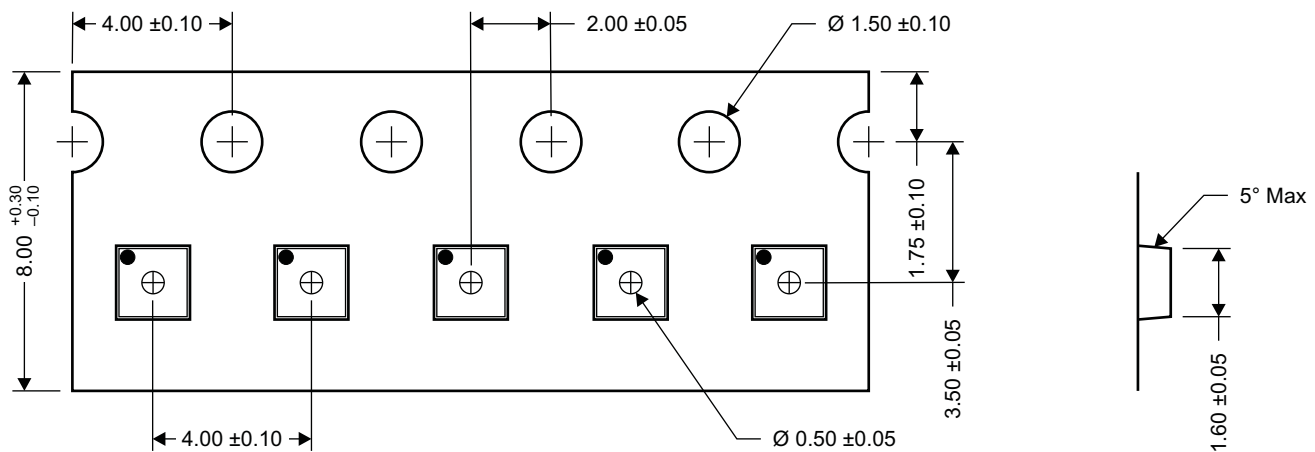
## 7.2 建议印刷电路板 (PCB) 焊盘图案



M0172-01

NOTE: 全部尺寸单位为 mm (除非另外注明)。

## 7.3 卷带封装信息



M0173-01

NOTE: 全部尺寸单位为 mm (除非另外注明)。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD75207W15</a>	Active	Production	DSBGA (YZF)   9	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75207
CSD75207W15.B	Active	Production	DSBGA (YZF)   9	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75207

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

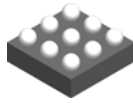
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD75207W15	DSBGA	YZF	9	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD75207W15	DSBGA	YZF	9	3000	182.0	182.0	20.0

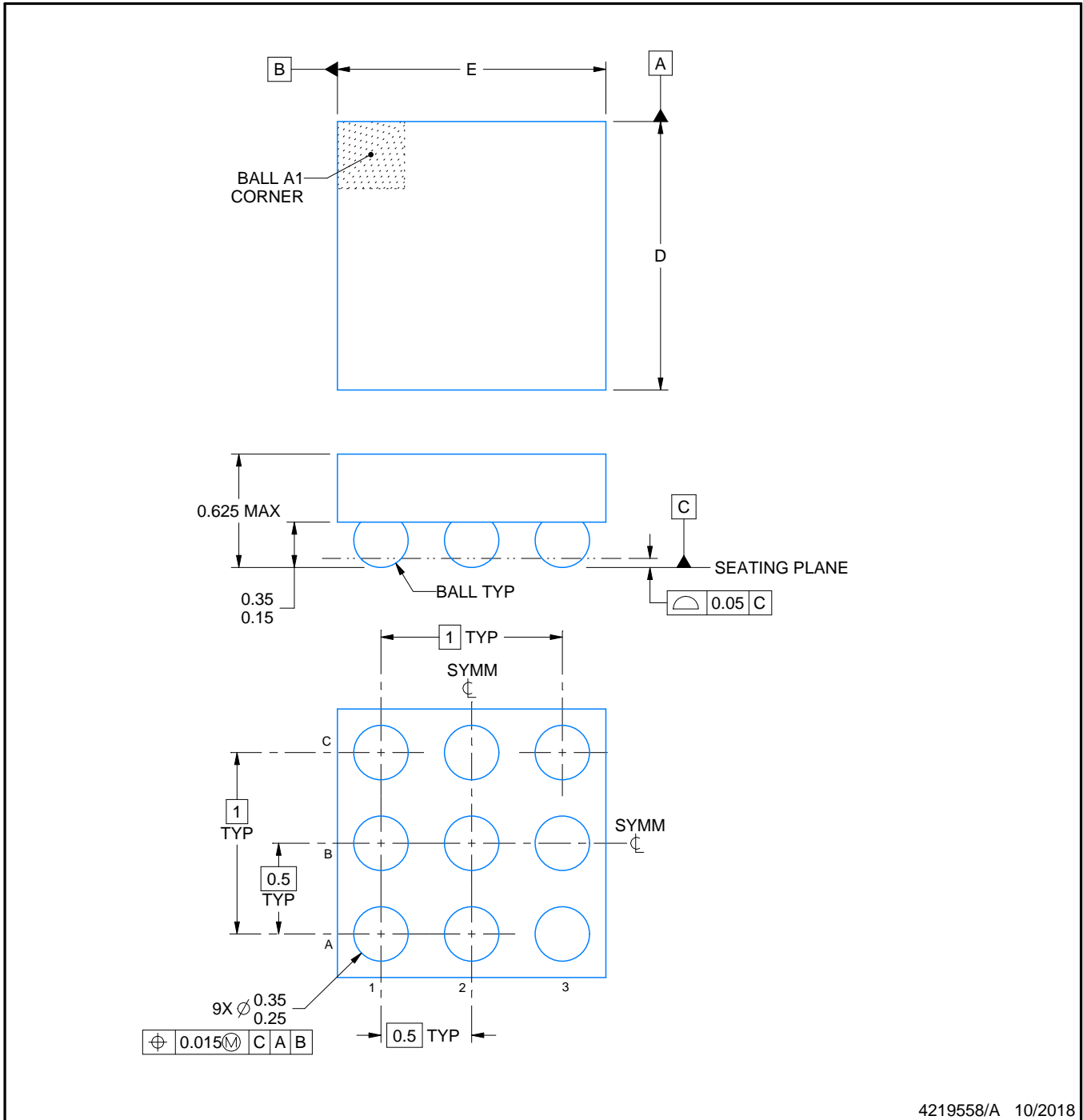
YZF0009



# PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

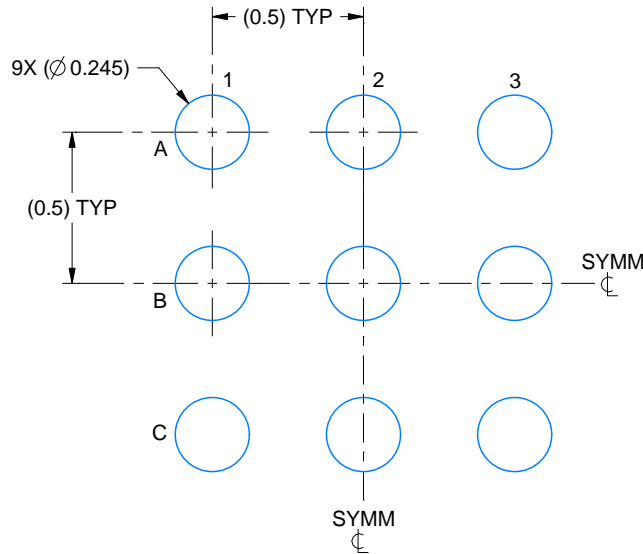
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

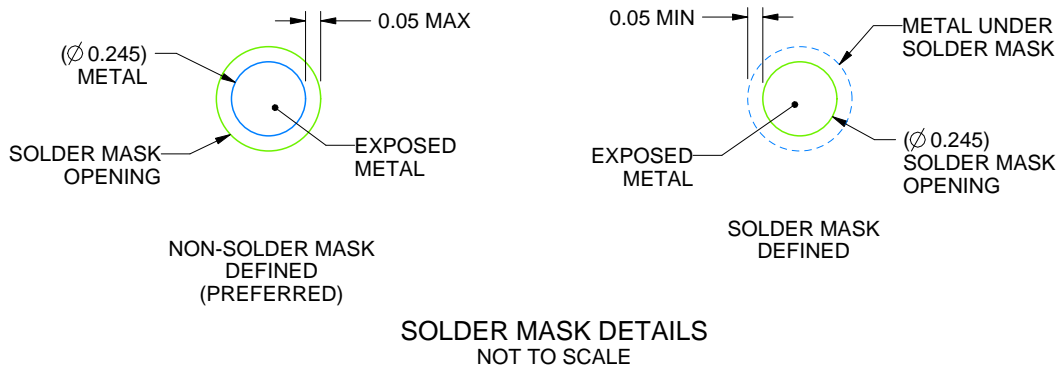
YZF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219558/A 10/2018

NOTES: (continued)

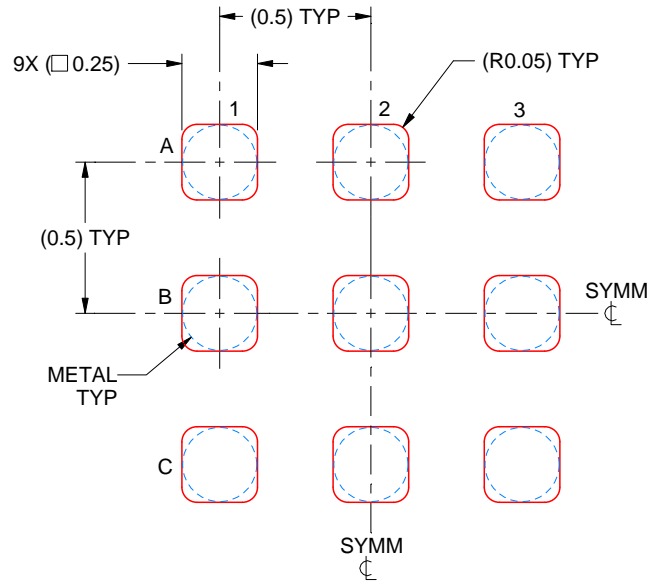
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 40X

4219558/A 10/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



## 重要通知和免责声明

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最后更新日期：2025 年 10 月