



CSD25404Q3 -20V P 沟道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 低 $R_{DS(on)}$
- 无卤素
- 符合 RoHS 标准
- 无铅引脚镀层
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 塑料封装

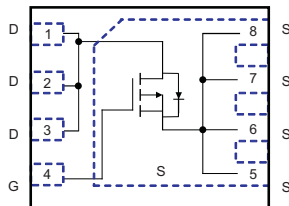
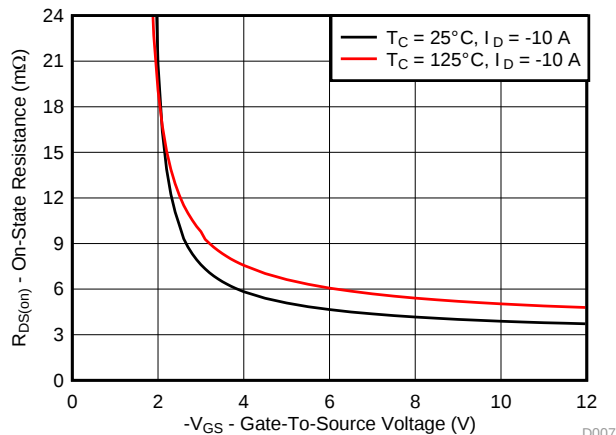
2 应用

- 直流-直流转换器
- 电池管理
- 负载开关
- 电池保护

3 说明

这款 -20V、5.5mΩ NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET) 旨在最大限度地降低功率转换和负载管理应用中的损耗。该器件采用 3.3mm × 3.3mm 小外形尺寸无引线 (SON) 封装，可提供出色的封装散热性能。

顶视图

 $R_{DS(on)}$ 与 V_{GS} 间的关系

D007

产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
V_{DS}	漏源电压	-20		V
Q_g	栅极电荷总量 (-4.5V)	10.9		nC
Q_{gd}	栅漏栅极电荷	2.2		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = -1.8\text{V}$	40	mΩ
		$V_{GS} = -2.5\text{V}$	10.1	mΩ
		$V_{GS} = -4.5\text{V}$	5.5	mΩ
V_{th}	阈值电压	-0.9		V

订购信息⁽¹⁾

器件	数量	包装介质	封装	运输
CSD25404Q3	2500	13 英寸卷带	SON 3.3mm × 3.3mm 塑料封装	卷带式
CSD25404Q3T	250	7 英寸卷带		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

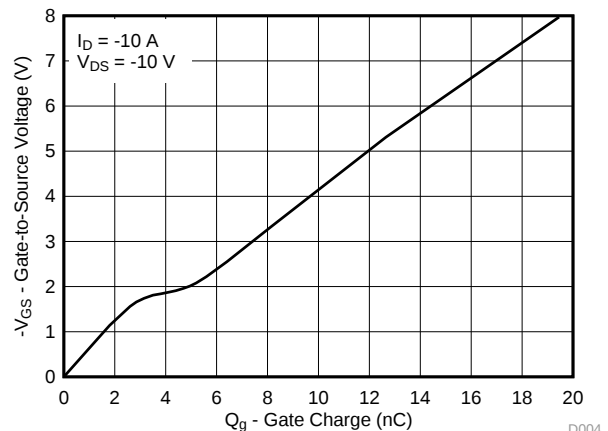
绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	±12	V
I_D	持续漏极电流, $T_C = 25^\circ\text{C}$	-104	A
	持续漏极电流 (受封装限制)	-60	
	持续漏极电流 ⁽¹⁾	-18	
I_{DM}	脉冲漏极电流 ⁽²⁾	-240	A
P_D	功耗 ⁽¹⁾	2.8	W
	功耗, $T_C = 25^\circ\text{C}$	96	
T_J, T_{stg}	工作结温, 储存温度	-55 至 150	°C

(1) $R_{\theta JA} = 45^\circ\text{C/W}$ ，这是在厚度为 0.060" 的环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸² 铜过渡垫片 (2 盎司) 上测得的典型值。

(2) 最大 $R_{\theta JC} = 1.3$ ，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%

栅极电荷



D004



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4 修订历史记录

日期	修订版本	注释
2015 年 11 月	*	最初发布。

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

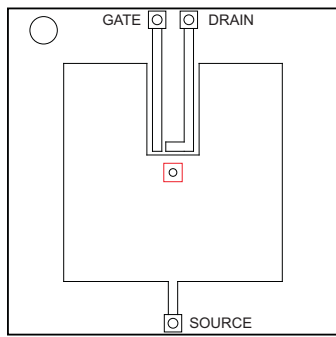
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = −250 μA	−20			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = −16 V			−1	μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = ±12 V			−100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = −250 μA	−0.65	−0.90	−1.15	V
R _{DS(on)}	Drain-to-source on resistance	V _{GS} = −1.8 V, I _D = −1 A		40	150	mΩ
		V _{GS} = −2.5 V, I _D = −10 A		10.1	12.1	mΩ
		V _{GS} = −4.5 V, I _D = −10 A		5.5	6.5	mΩ
g _{fs}	Transconductance	V _{DS} = −10 V, I _D = −10 A		47		S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input capacitance	V _{GS} = 0 V, V _{DS} = −10 V, f = 1 MHz		1630	2120	pF
C _{OSS}	Output capacitance			902	1170	pF
C _{RSS}	Reverse transfer capacitance			52	68	pF
R _G	Series gate resistance			0.8	2.4	Ω
Q _g	Gate charge total (−4.5 V)	V _{DS} = −10 V, I _D = −10 A		10.8	14.1	nC
Q _{gd}	Gate charge gate to drain			2.2		nC
Q _{gs}	Gate charge gate to source			2.8		nC
Q _{g(th)}	Gate charge at V _{th}			1.5		nC
Q _{OSS}	Output charge	V _{DS} = −10 V, V _{GS} = 0 V		9.0		nC
t _{d(on)}	Turn on delay time	V _{DS} = −10 V, V _{GS} = −4.5 V, I _D = −10 A, R _G = 5 Ω		13		ns
t _r	Rise time			8		ns
t _{d(off)}	Turn off delay time			35		ns
t _f	Fall time			13		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _S = −10 A, V _{GS} = 0 V	−0.8		−1	V
Q _{rr}	Reverse recovery charge	V _{DS} = −10 V, I _F = −10 A, di/dt = 200 A/μs		20.5		nC
t _{rr}	Reverse recovery time			26		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

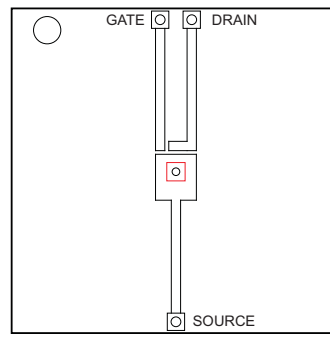
THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-case thermal resistance ⁽¹⁾			1.3	°C/W
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			55	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.



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Max $R_{\theta JA} = 55^{\circ}\text{C/W}$
when mounted on
1 inch² of 2 oz. Cu.

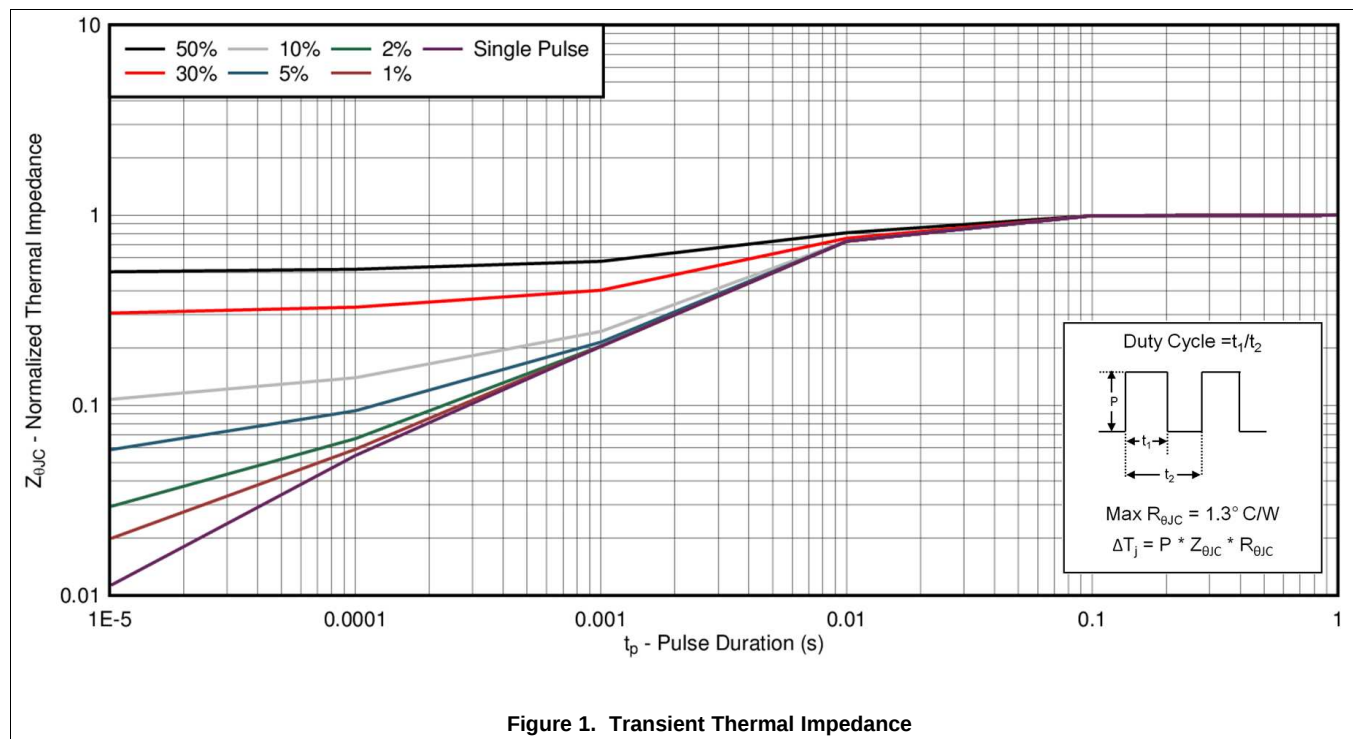


M0137-02

Max $R_{\theta JA} = 160^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2 oz. Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

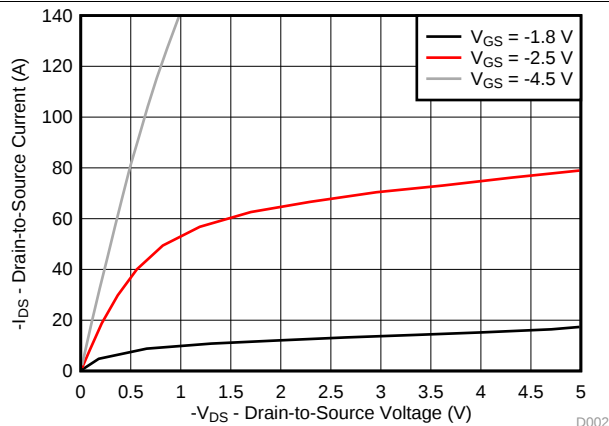


Figure 2. Saturation Characteristics

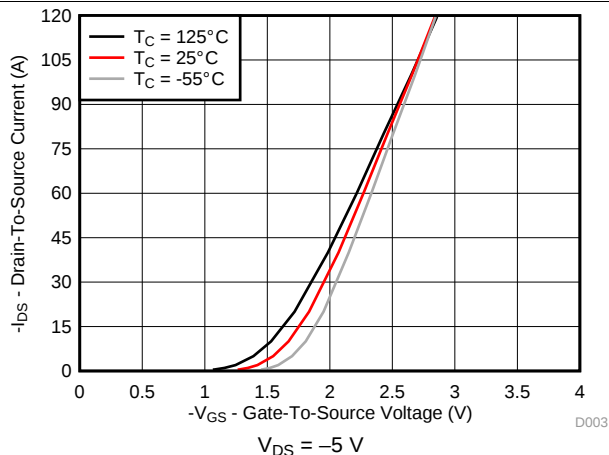


Figure 3. Transfer Characteristics

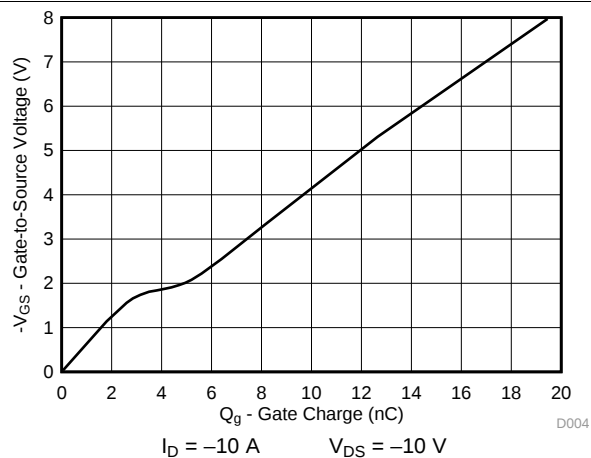


Figure 4. Gate Charge

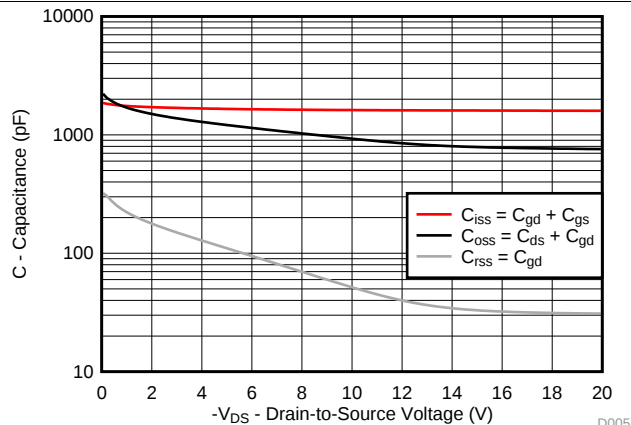


Figure 5. Capacitance

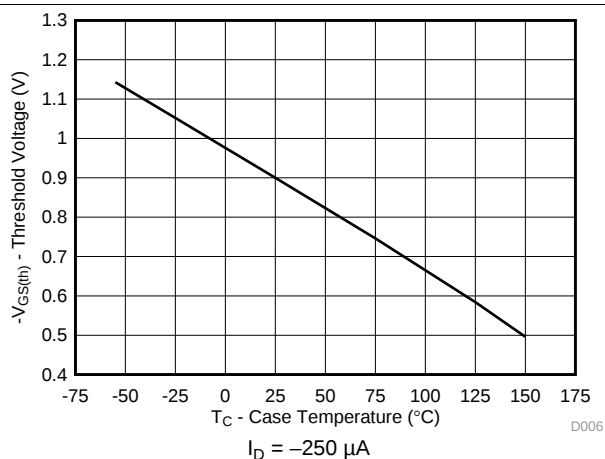


Figure 6. Threshold Voltage vs Temperature

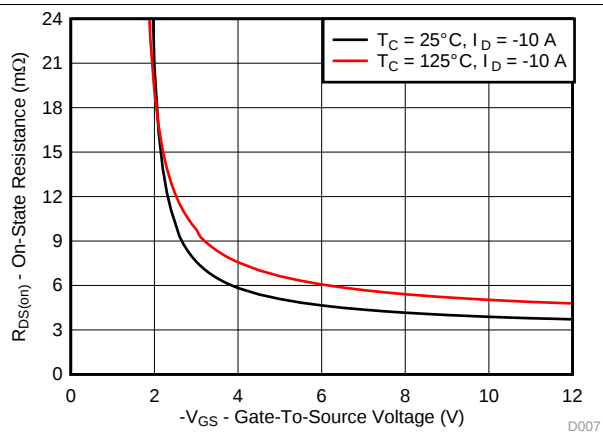


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

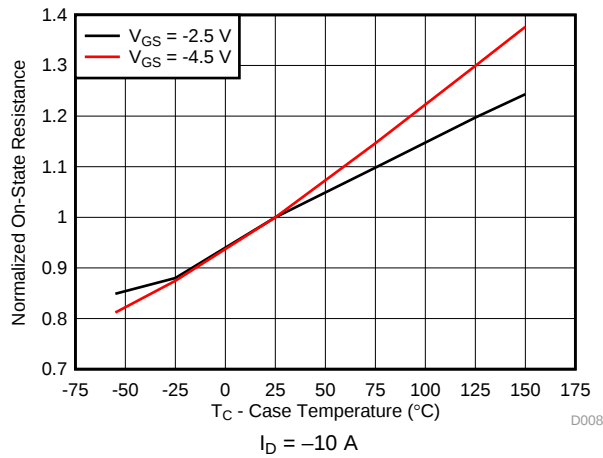


Figure 8. Normalized On-State Resistance vs Temperature

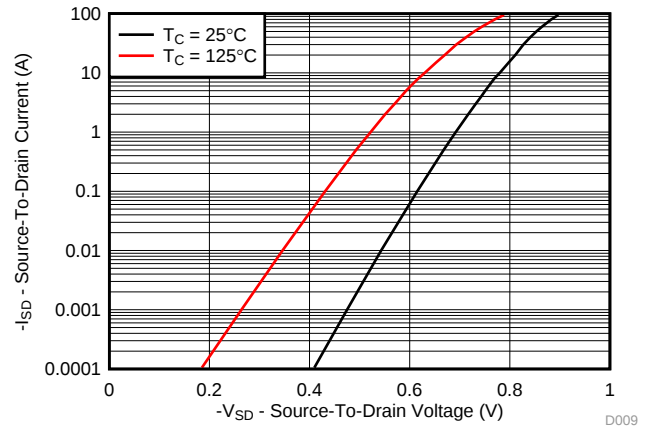


Figure 9. Typical Diode Forward Voltage

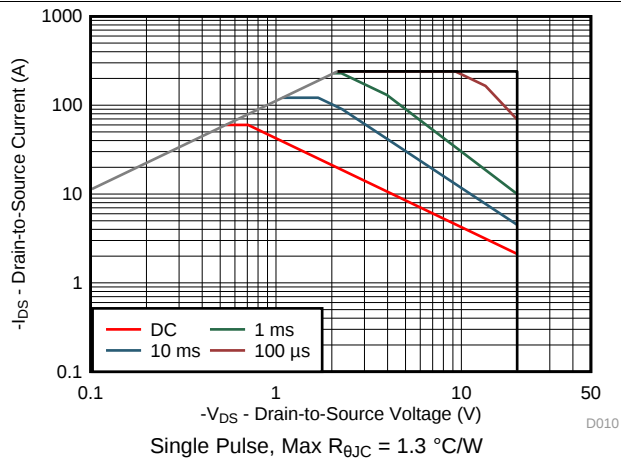


Figure 10. Maximum Safe Operating Area

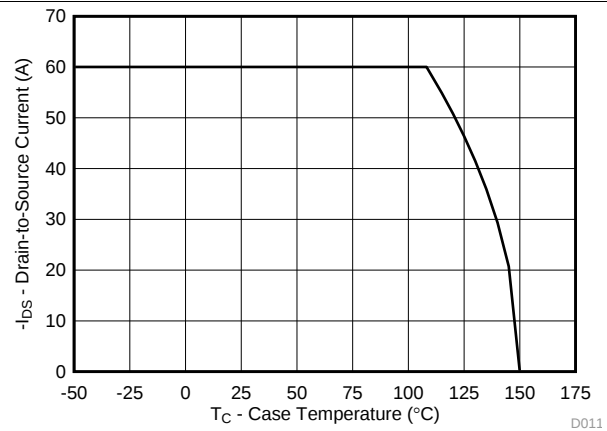


Figure 11. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 商标

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6.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.4 Glossary

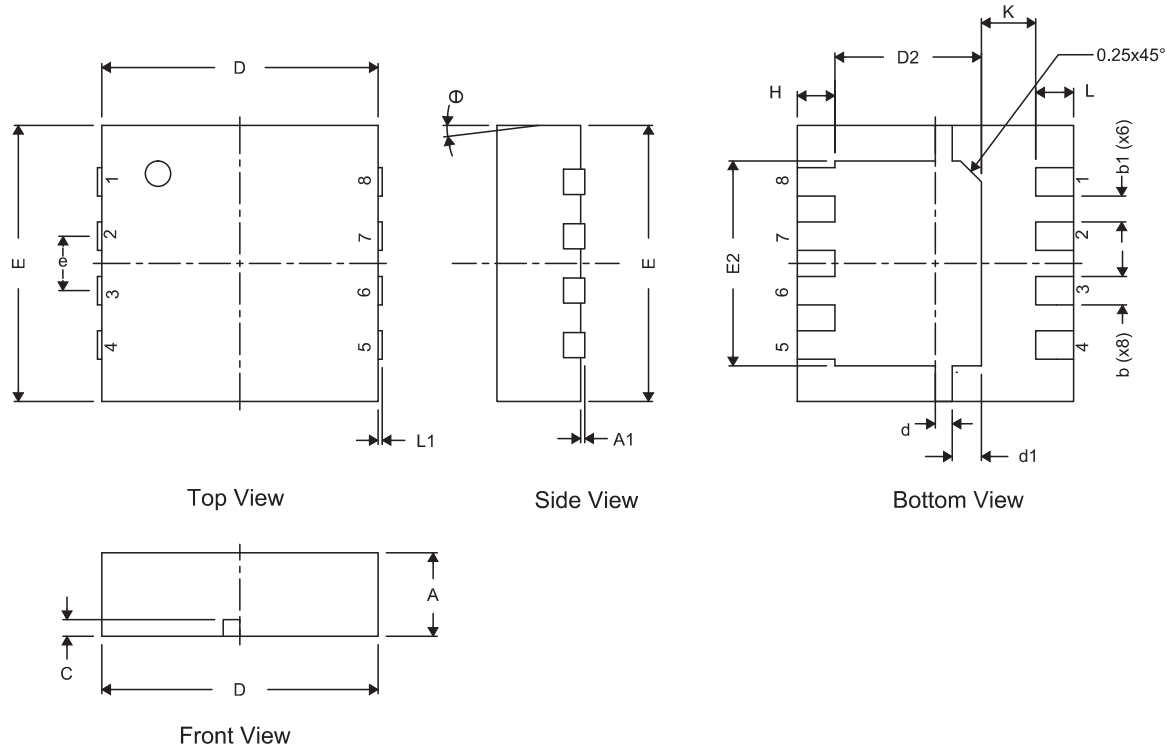
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

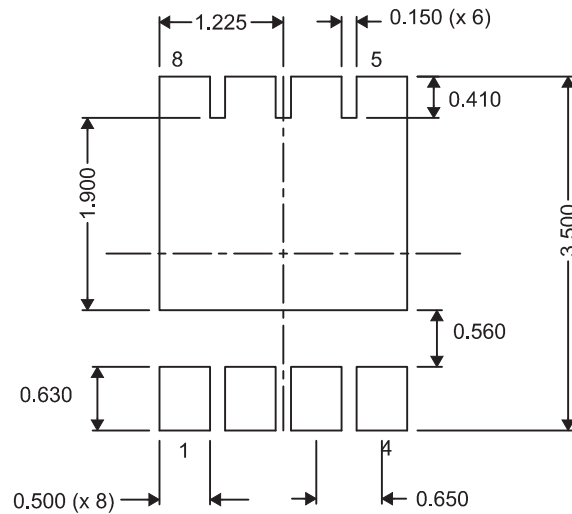
以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

7.1 CSD25404Q3 封闭尺寸



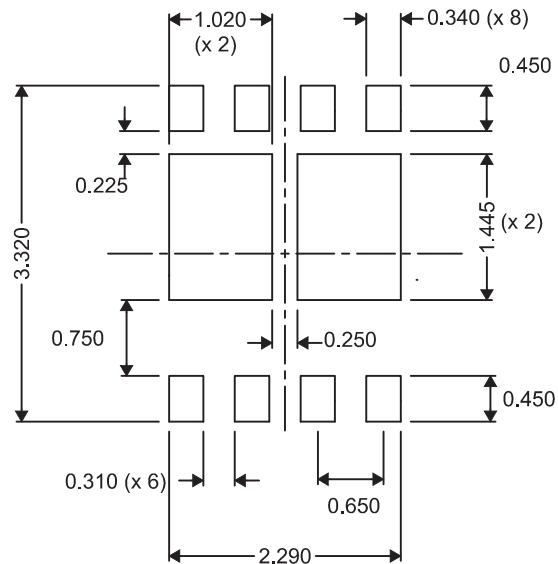
DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 (标称值)			0.012 (标称值)		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 典型值			0.026 典型值		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 典型值			0.026 典型值		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 建议 PCB 布局



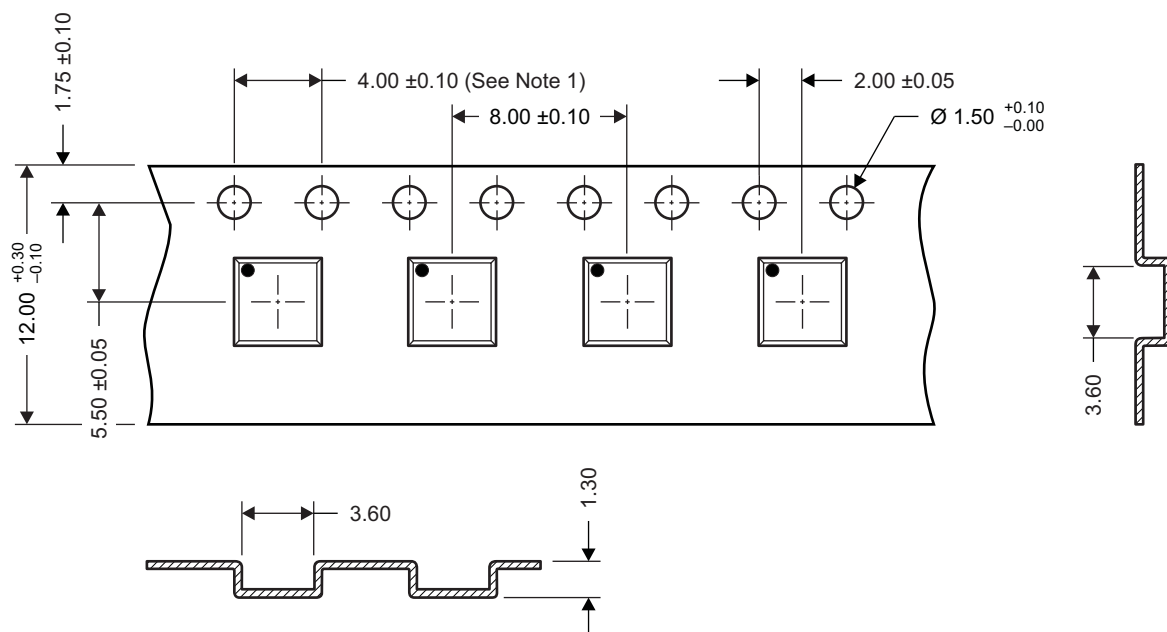
要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线, 请参见《应用说明》[SLPA005 - 通过 PCB 布局布线技巧来减少振铃](#)。

7.3 建议模板开口



全部尺寸单位为 mm, 除非另外注明。

7.4 Q3 卷带信息



M0144-01

注释:

1. 10 链轮孔距累积容差为 ± 0.2
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）。
5. 厚度： $0.30 \pm 0.05\text{mm}$
6. MSL1 260°C（红外 (IR) 和传导）无铅回流焊兼容

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD25404Q3	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD25404
CSD25404Q3.B	Active	Production	VSON-CLIP (DQG) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD25404
CSD25404Q3T	Active	Production	VSON-CLIP (DQG) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD25404
CSD25404Q3T.B	Active	Production	VSON-CLIP (DQG) 8	250 SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD25404

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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最后更新日期：2025 年 10 月