

CSD18511KCS 40V N 沟道 NexFET™ 功率 MOSFET

1 特性

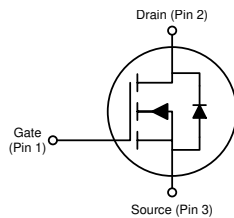
- 低 Q_g 和 Q_{gd}
- 低 $R_{DS(on)}$
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- TO-220 塑料封装

2 应用

- 次级侧同步整流器
- 电机控制

3 说明

这款 40V、2.1m Ω 、TO-220 NexFET™ 功率 MOSFET 旨在用于更大限度地降低功率转换应用中的损耗。



产品概要

$T_A = 25^\circ\text{C}$		典型值	单位
V_{DS}	漏源电压	40	V
Q_g	栅极电荷总量 (10V)	63.9	nC
Q_{gd}	栅极电荷 (栅极到漏极)	9.7	nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	3.2
		$V_{GS} = 10\text{V}$	2.1
$V_{GS(th)}$	阈值电压	1.8	V

器件信息(1)

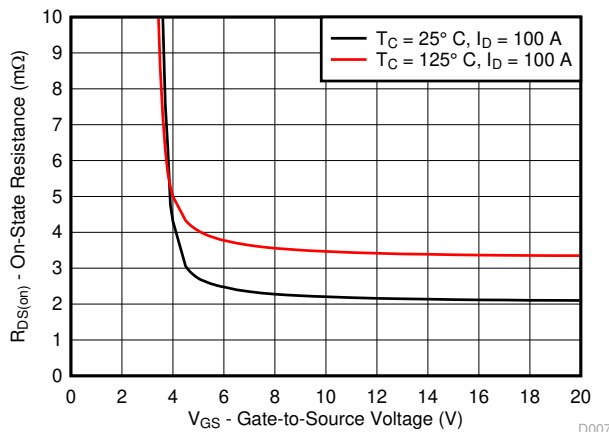
器件	介质	数量	封装	运输
CSD18511KCS	管装	50	TO-220 塑料封装	管装

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

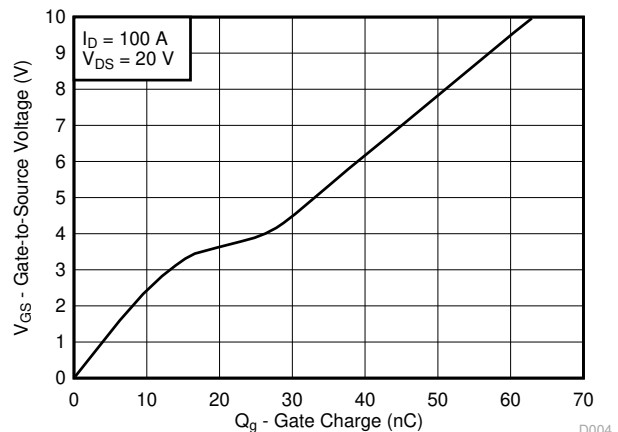
绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	40	V
V_{GS}	栅源电压	± 20	V
I_D	持续漏极电流 (受封装限制)	110	A
	持续漏极电流 (受器件限制), $T_C = 25^\circ\text{C}$ 时测得	194	
	持续漏极电流 (受器件限制), $T_C = 100^\circ\text{C}$ 时测得	137	
I_{DM}	脉冲漏极电流(1)	400	A
P_D	功率耗散	188	W
T_J 、 T_{stg}	工作结温, 贮存温度	-55 至 175	$^\circ\text{C}$
E_{AS}	雪崩能量, 单脉冲 $I_D = 56\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	156	mJ

(1) 最大 $R_{\theta JC} = 0.8^\circ\text{C/W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$ 。



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷



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4 Specifications

4.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 250 μ A	40			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 32V			1	μ A
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μ A	1.5	1.8	2.4	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 4.5V, I _D = 100A	3.2		4.2	mΩ
		V _{GS} = 10V, I _D = 100A	2.1		2.6	
g _{fs}	Transconductance	V _{DS} = 4V, I _D = 100A	249			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0V, V _{DS} = 20V, f = 1MHz		4570	5940	pF
C _{oss}	Output capacitance			454	591	pF
C _{rss}	Reverse transfer capacitance			235	306	pF
R _G	Series gate resistance			0.9	1.8	Ω
Q _g	Gate charge total (4.5V)	V _{DS} = 20V, I _D = 100A		31		nC
Q _g	Gate charge total (10V)			64		nC
Q _{gd}	Gate charge gate-to-drain			9.7		nC
Q _{gs}	Gate charge gate-to-source			17.9		nC
Q _{g(th)}	Gate charge at V _{th}			7.4		nC
Q _{oss}	Output charge	V _{DS} = 20V, V _{GS} = 0V		20.7		nC
t _{d(on)}	Turnon delay time	V _{DS} = 20V, V _{GS} = 10V, I _{DS} = 100A, R _G = 0Ω		8		ns
t _r	Rise time			6		ns
t _{d(off)}	Turnoff delay time			17		ns
t _f	Fall time			3		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 100A, V _{GS} = 0V		0.9	1.0	V
Q _{rr}	Reverse recovery charge	V _{DS} = 20V, I _F = 100A,		62		nC
t _{rr}	Reverse recovery time	di/dt = 300A/ μ s		31		ns

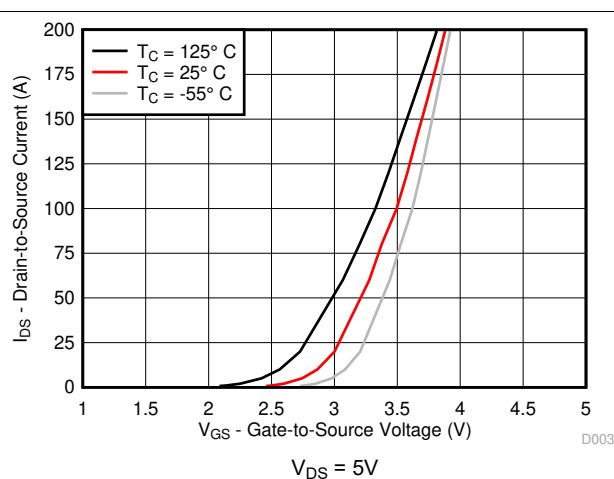
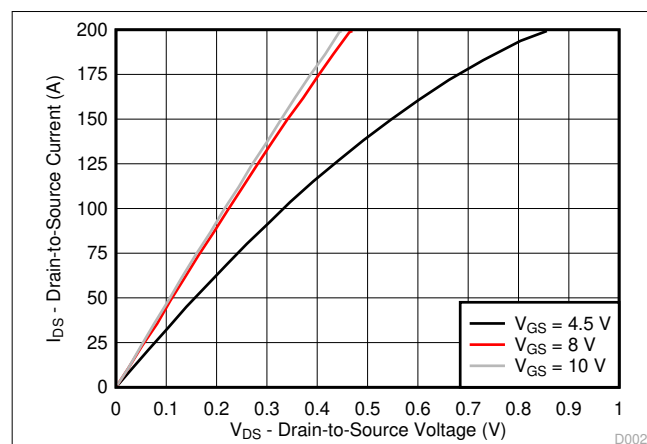
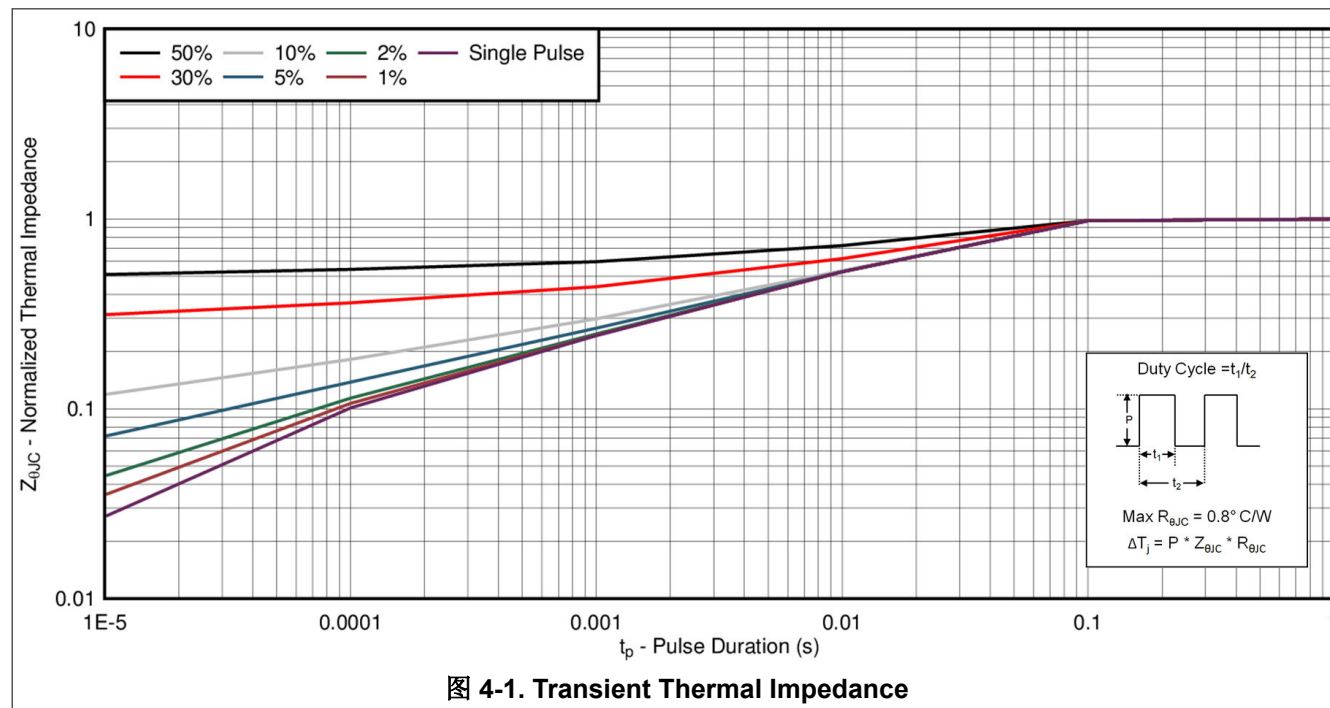
4.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C/W}$

4.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)



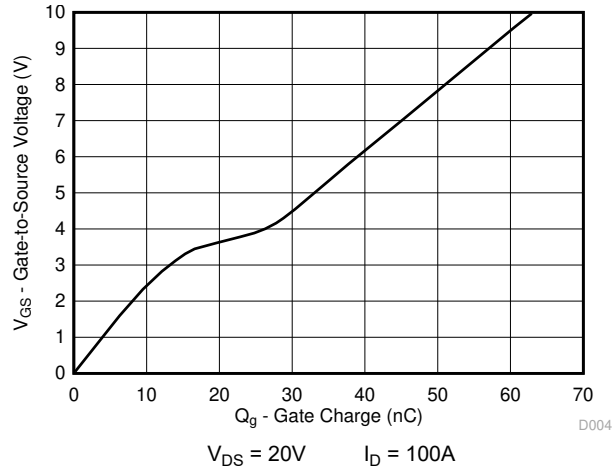


图 4-4. Gate Charge

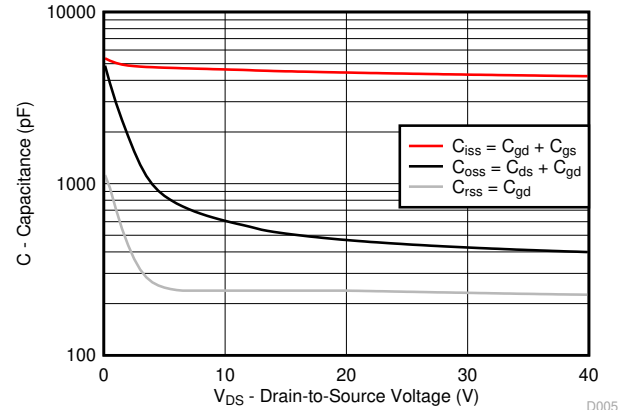


图 4-5. Capacitance

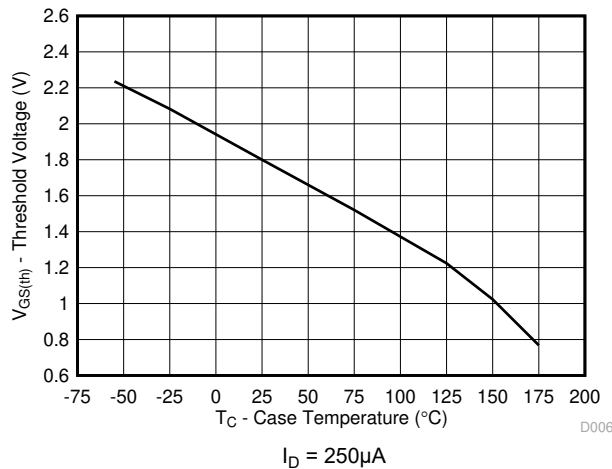


图 4-6. Threshold Voltage vs Temperature

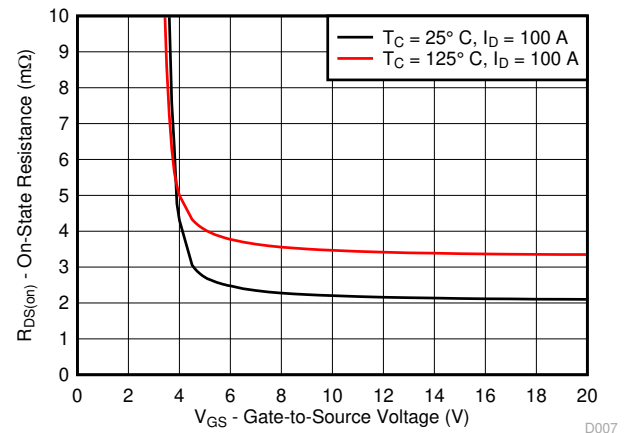


图 4-7. On-State Resistance vs Gate-to-Source Voltage

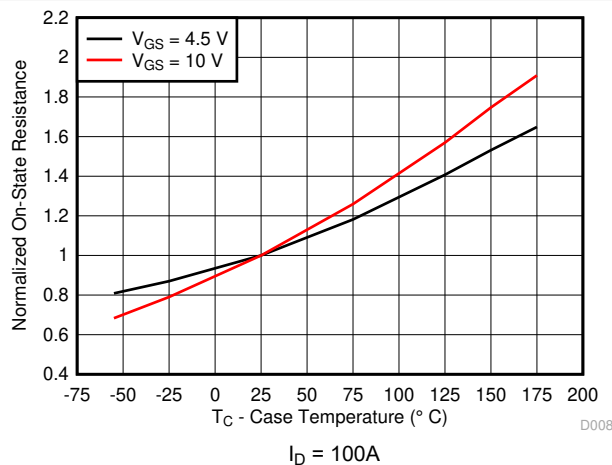


图 4-8. Normalized On-State Resistance vs Temperature

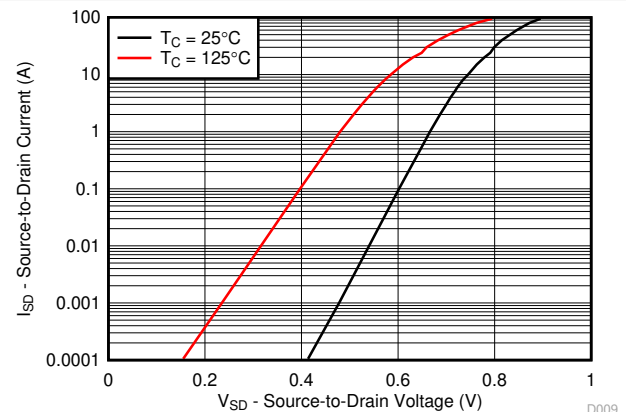


图 4-9. Typical Diode Forward Voltage

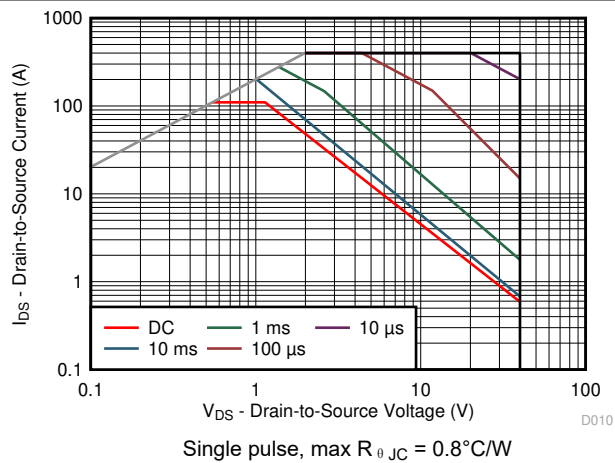


图 4-10. Maximum Safe Operating Area

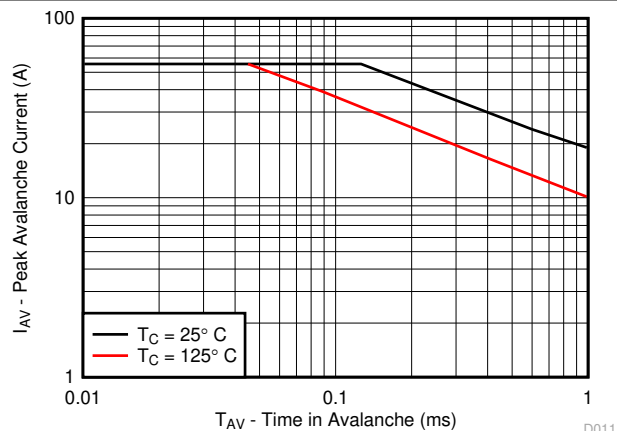


图 4-11. Single Pulse Unclamped Inductive Switching

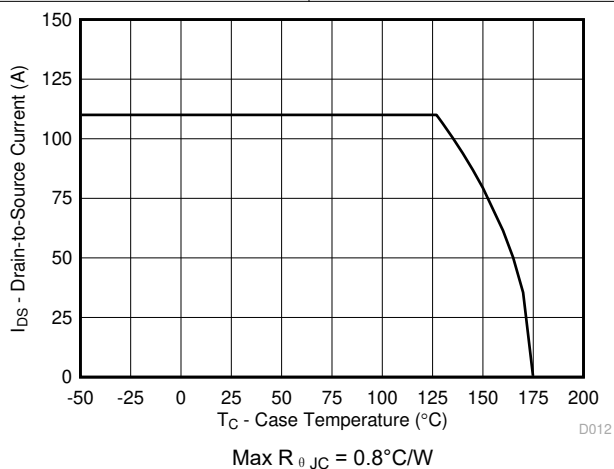


图 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.6 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

6 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (July 2017) to Revision A (March 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18511KCS	Active	Production	TO-220 (KCS) 3	50 TUBE	ROHS Exempt	SN	N/A for Pkg Type	-55 to 175	CSD18511KCS
CSD18511KCS.B	Active	Production	TO-220 (KCS) 3	50 TUBE	ROHS Exempt	SN	N/A for Pkg Type	-55 to 175	CSD18511KCS

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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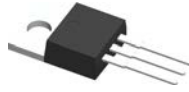
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CSD18511KCS	KCS	TO-220	3	50	532	34.1	700	9.6
CSD18511KCS.B	KCS	TO-220	3	50	532	34.1	700	9.6

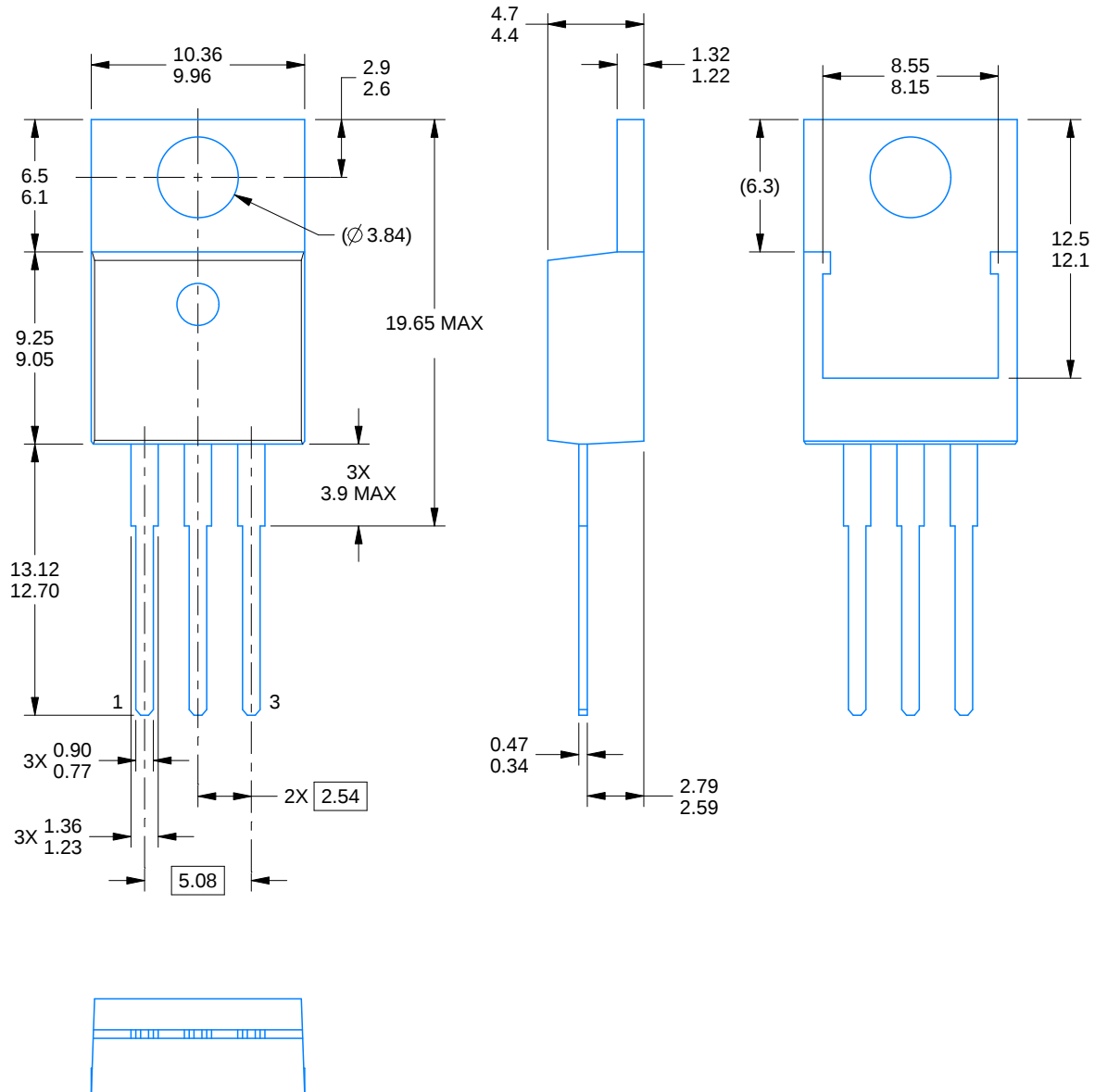


PACKAGE OUTLINE

KCS0003B

TO-220 - 19.65 mm max height

TO-220



4222214/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.

EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

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