



CSD17571Q2 30V N 沟道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 环保标准
- 无卤素
- 小外形尺寸无引线 (SON) 2mm × 2mm 塑料封装

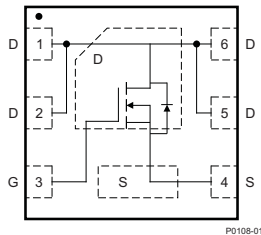
2 应用范围

- 针对负载开关应用进行了优化
- 存储、平板电脑和手持设备
- 针对控制场效应晶体管 (FET) 应用进行了优化

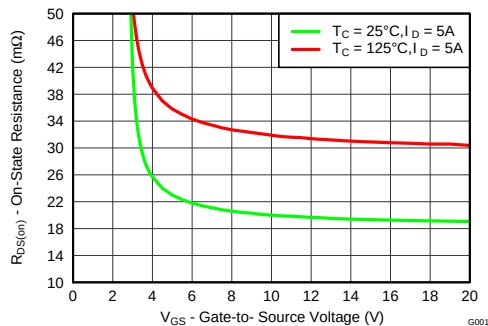
3 说明

这款 30V、20mΩ、SON 2mm × 2mm NexFET™ 功率 MOSFET 旨在以最大程度降低功率转换和负载管理应用中的损耗，同时提供出色的封装散热性能。

顶视图



P0108-01

 $R_{DS(on)}$ 与 V_{GS} 间的关系

产品概要

$T_A = 25^\circ\text{C}$		典型值	单位
V_{DS}	漏源电压	30	V
Q_g	栅极电荷总量 (4.5V)	2.4	nC
Q_{gd}	栅极电荷 (栅极到漏极)	0.6	nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	24
		$V_{GS} = 10\text{V}$	20
$V_{GS(th)}$	阈值电压	1.6	V

订购信息⁽¹⁾

器件	介质	数量	封装	出货
CSD17571Q2	7 英寸卷带	3000	SON 2mm x 2mm 塑料封装	卷带封装

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

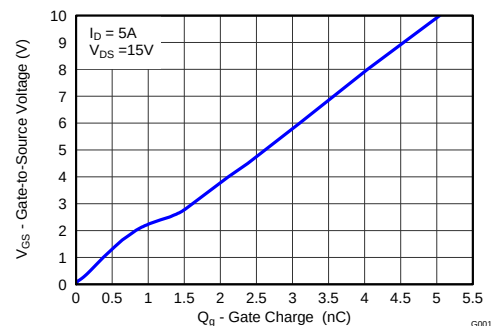
绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流 (受封装限制)	22	A
	持续漏极电流 ⁽¹⁾	7.6	A
I_{DM}	脉冲漏极电流, $T_A = 25^\circ\text{C}$ 时测得 ⁽²⁾	39	A
P_D	功率耗散 ⁽¹⁾	2.5	W
T_J , T_{stg}	运行结温和 储存温度范围	-55 至 150	$^\circ\text{C}$
E_{AS}	雪崩能量, 单一脉冲 $I_D = 12\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	7.2	mJ

(1) $R_{\theta JA} = 50$ ，这是在厚度为 0.060" 的环氧树脂 (FR4) 印刷电路板 (PCB) 上 1 in² (2 盎司) 铜焊盘上测得的典型值

(2) 脉冲持续时间 10μs，占空比 ≤ 2%

栅极电荷



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4 修订历史记录

Changes from Original (October 2013) to Revision A	Page
• Updated Figure #8	6

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 24 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	1.3	1.6	2	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 4.5 V, I _{DS} = 5 A		24	29	mΩ
		V _{GS} = 10 V, I _{DS} = 5 A		20	24	mΩ
g _{fs}	Transconductance	V _{DS} = 15 V, I _{DS} = 5 A	43			S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		360	468	pF
C _{OSS}	Output Capacitance			101	131	pF
C _{RSS}	Reverse Transfer Capacitance			9	12	pF
R _g	Series Gate Resistance		3.8	7.6		Ω
Q _g	Gate Charge Total (4.5 V)	V _{DS} = 15 V, I _{DS} = 5 A	2.4	3.1		nC
Q _{gd}	Gate Charge – Gate-to-Drain		0.6			nC
Q _{gs}	Gate Charge Gate-to-Source		0.9			nC
Q _{g(th)}	Gate Charge at V _{th}		0.6			nC
Q _{OSS}	Output Charge	V _{DS} = 15 V, V _{GS} = 0 V	3.4			nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 15 V, V _{GS} = 4.5 V, I _{DS} = 5 A R _G = 2 Ω	5.3			ns
t _r	Rise Time		19			ns
t _{d(off)}	Turn Off Delay Time		8			ns
t _f	Fall Time		2.6			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{DS} = 5 A, V _{GS} = 0 V	0.8	1		V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 15 V, I _F = 5 A, di/dt = 300 A/μs	2.3			nC
t _{rr}	Reverse Recovery Time		11			ns

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ unless otherwise specified

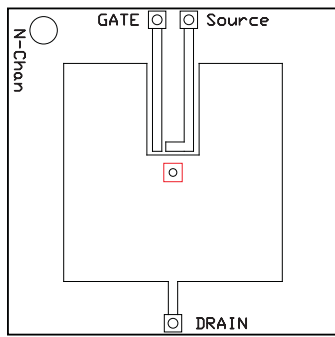
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance ⁽¹⁾			6.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			65	

- $R_{\theta JC}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

CSD17571Q2

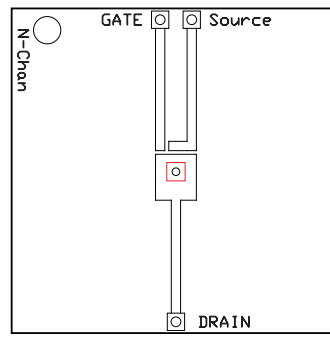
ZHCSBT4A – OCTOBER 2013 – REVISED JANUARY 2015

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Max $R_{\theta JA} = 65$ when
mounted on 1 inch²
(6.45 cm²) of 2 oz.
(0.071 mm thick) Cu.

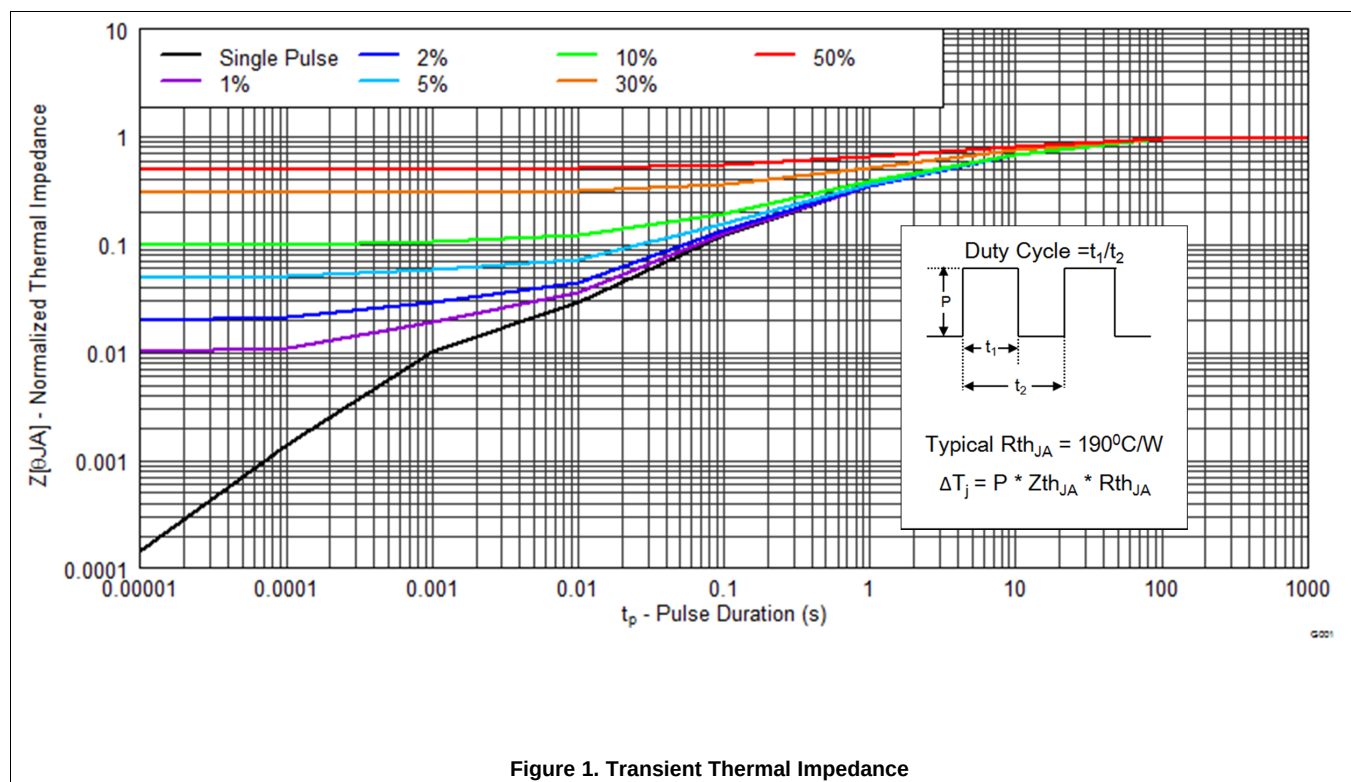


M0164-02

Max $R_{\theta JA} = 235$ when
mounted on minimum
pad area of 2 oz.
(0.071 mm thick) Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise specified



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ unless otherwise specified

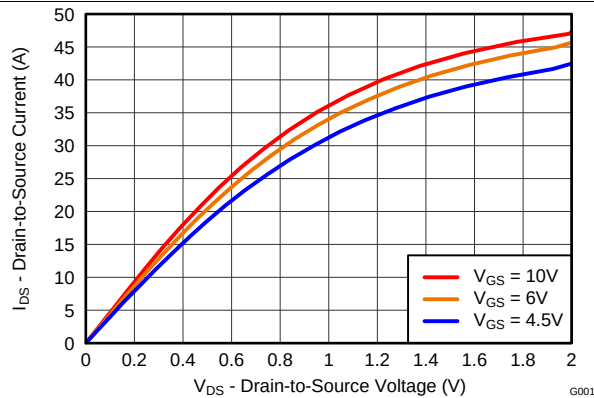


Figure 2. Saturation Characteristics

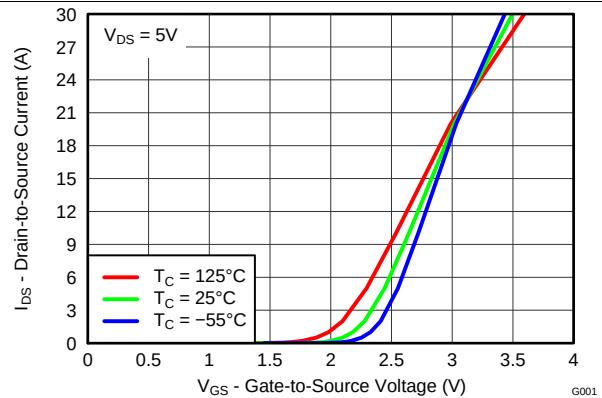


Figure 3. Transfer Characteristics

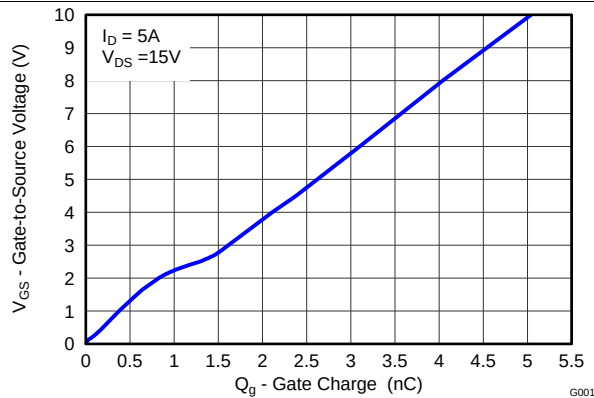


Figure 4. Gate Charge

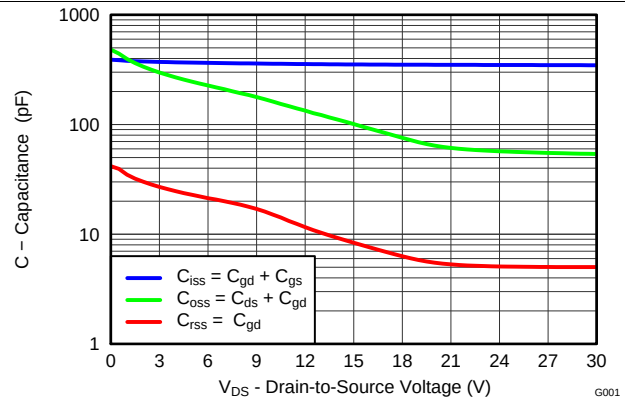


Figure 5. Capacitance

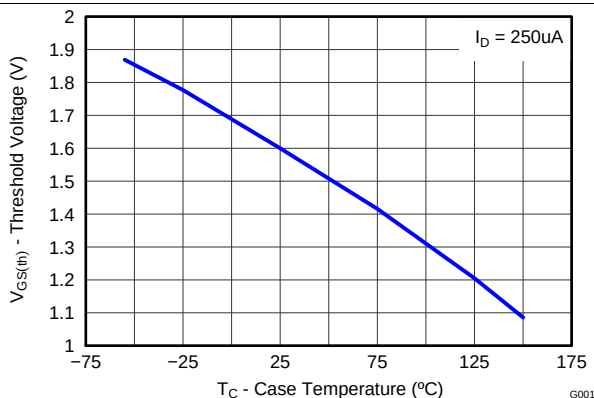


Figure 6. Threshold Voltage vs Temperature

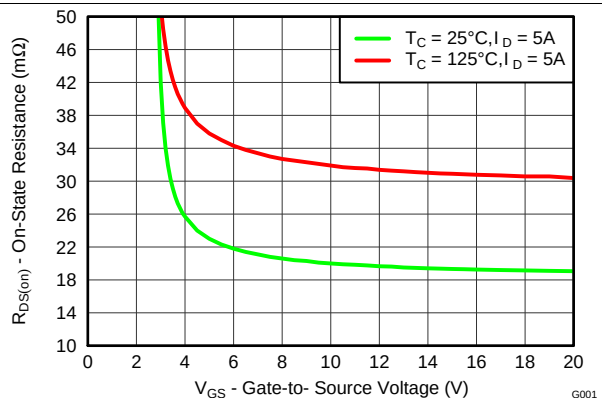


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ unless otherwise specified

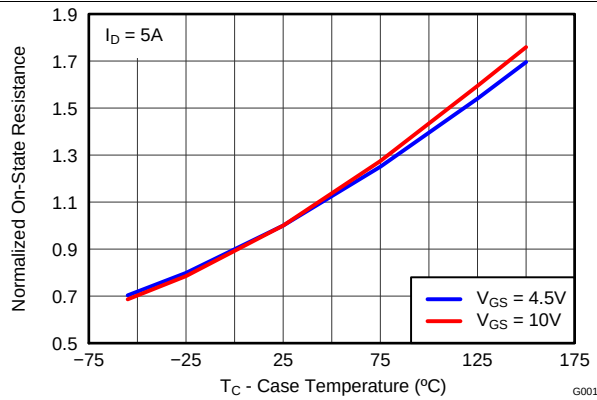


Figure 8. Normalized On-State Resistance vs Temperature

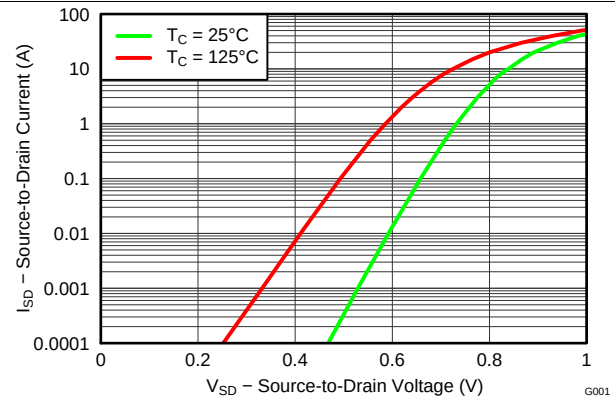


Figure 9. Typical Diode Forward Voltage

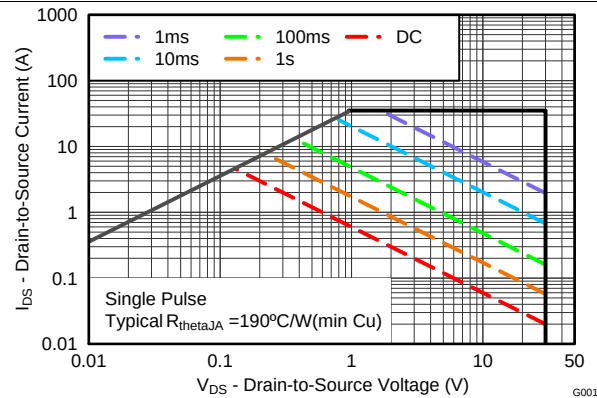


Figure 10. Maximum Safe Operating Area

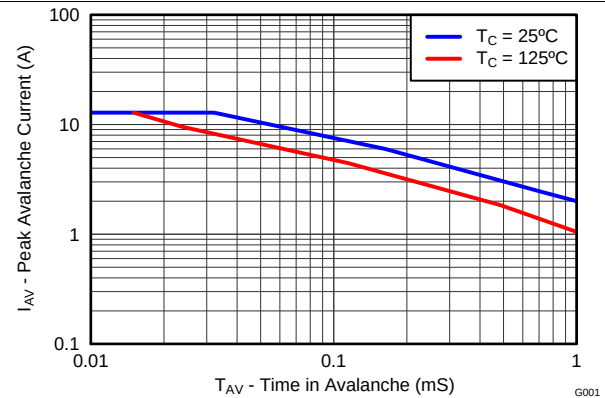


Figure 11. Single Pulse Unclamped Inductive Switching

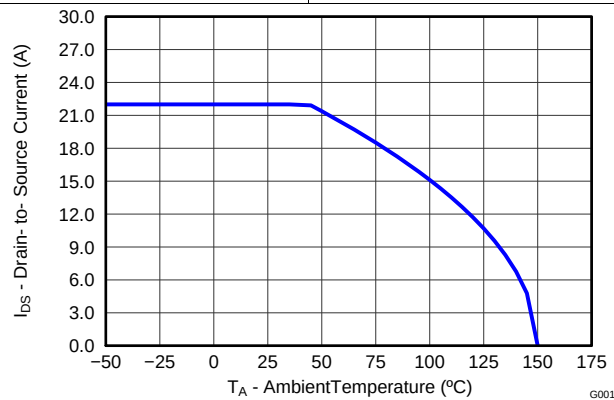


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

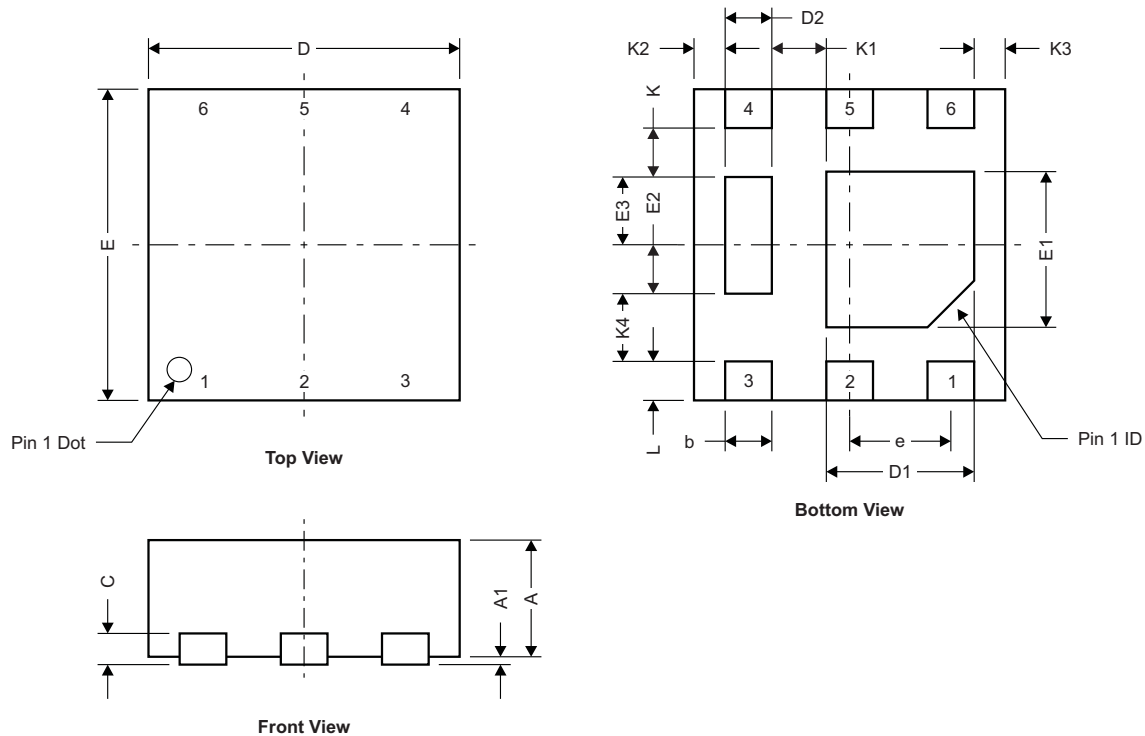
[SLYZ022](#) — *TI* 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

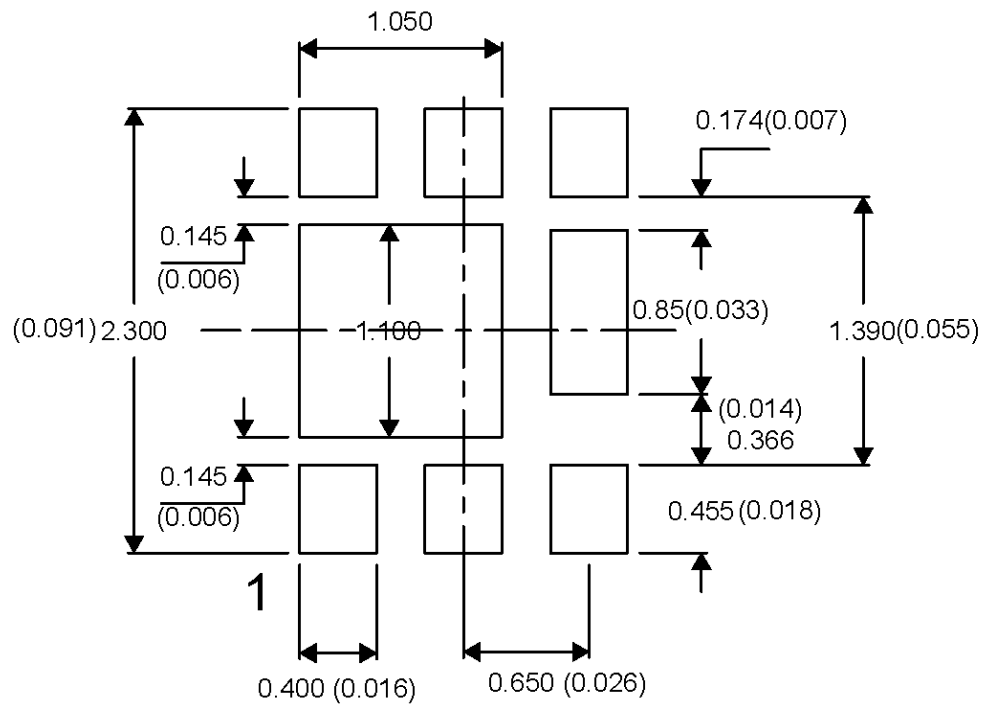
7.1 Q2 封装尺寸



M0165-01

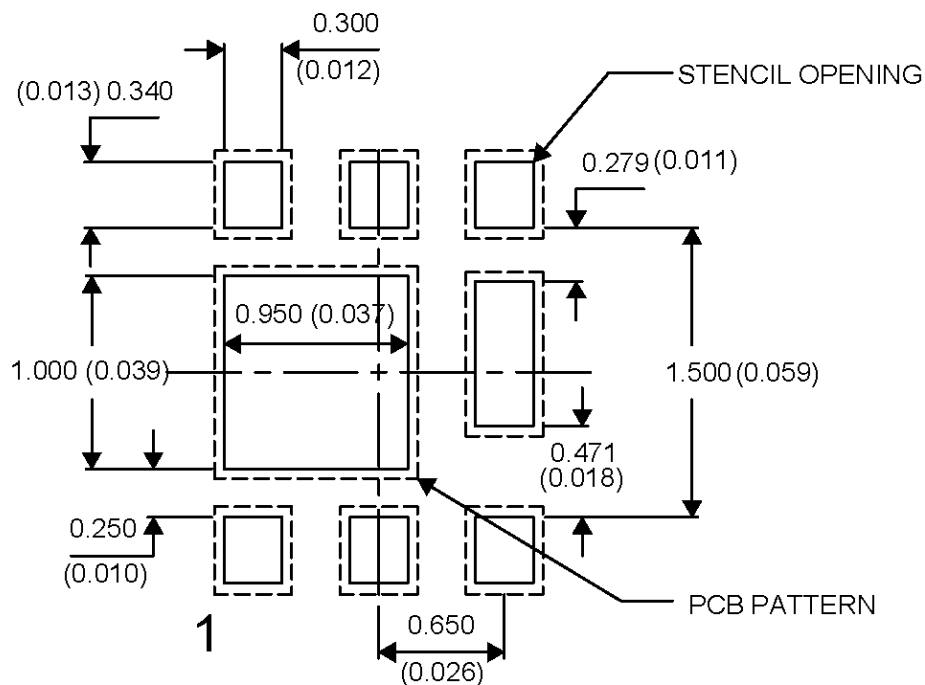
DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C		0.203 典型值			0.008 典型值	
D		2.000 典型值			0.080 典型值	
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2		0.300 典型值			0.012 典型值	
E		2.000 典型值			0.080 典型值	
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2		0.280 典型值			0.0112 典型值	
E3		0.470 典型值			0.0188 典型值	
e		0.650 BSC			0.026 典型值	
K		0.280 典型值			0.0112 典型值	
K1		0.350 典型值			0.014 典型值	
K2		0.200 典型值			0.008 典型值	
K3		0.200 典型值			0.008 典型值	
K4		0.470 典型值			0.0188 典型值	
L	0.200	0.25	0.300	0.008	0.010	0.012

7.1.1 建议 PCB 布局



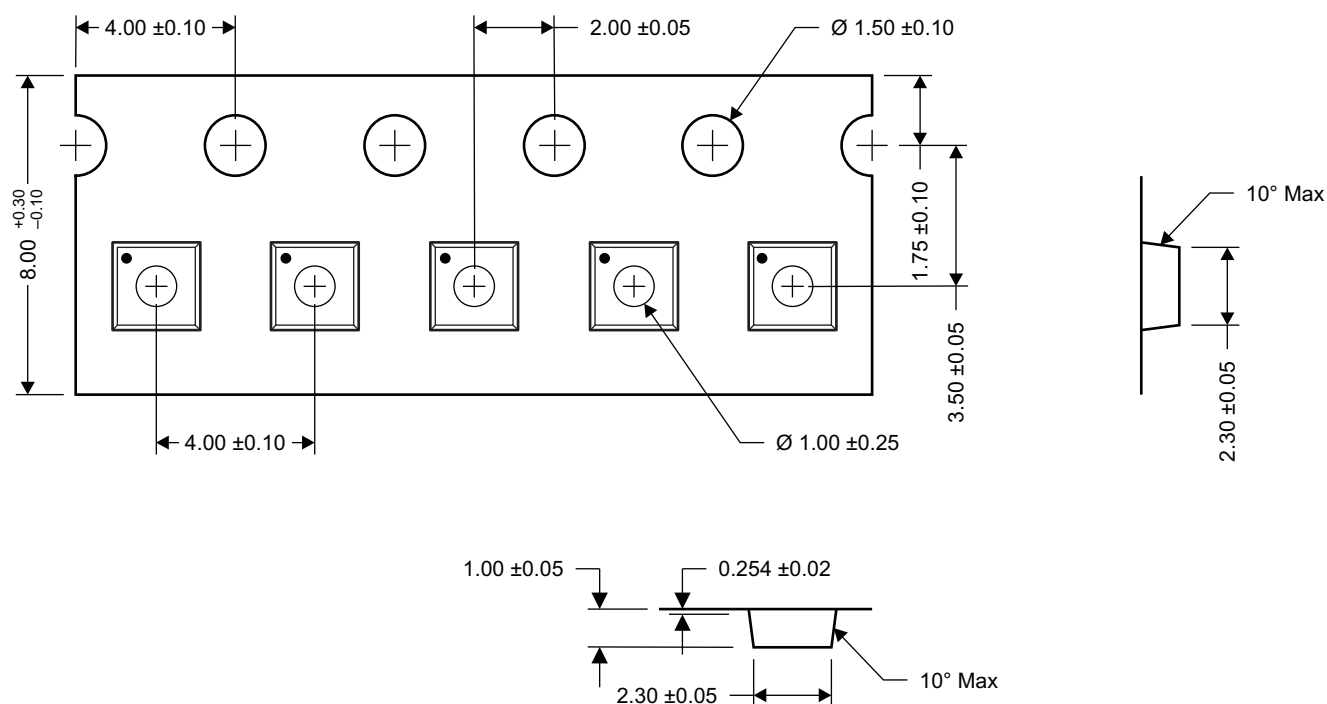
要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线, 请参见《应用说明》[SLPA005 - 通过 PCB 布局布线技巧来减少振铃](#)。

7.1.2 建议模板布局



Note: 全部尺寸单位为 mm, 除非另外注明。

7.2 Q2 卷带信息



- Notes:
1. 测自链齿孔中心线到孔眼中心线
 2. 10 个链齿孔的累积容差为 ± 0.20
 3. 其他材料可用
 4. 卷带的 SR 典型值最大为 10^9 OHM/SQ
 5. 全部尺寸单位为 mm，除非另外注明。

M0168-01

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17571Q2	Active	Production	WSON (DQK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1751
CSD17571Q2.B	Active	Production	WSON (DQK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1751
CSD17571Q2G4.B	Active	Production	WSON (DQK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1751

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

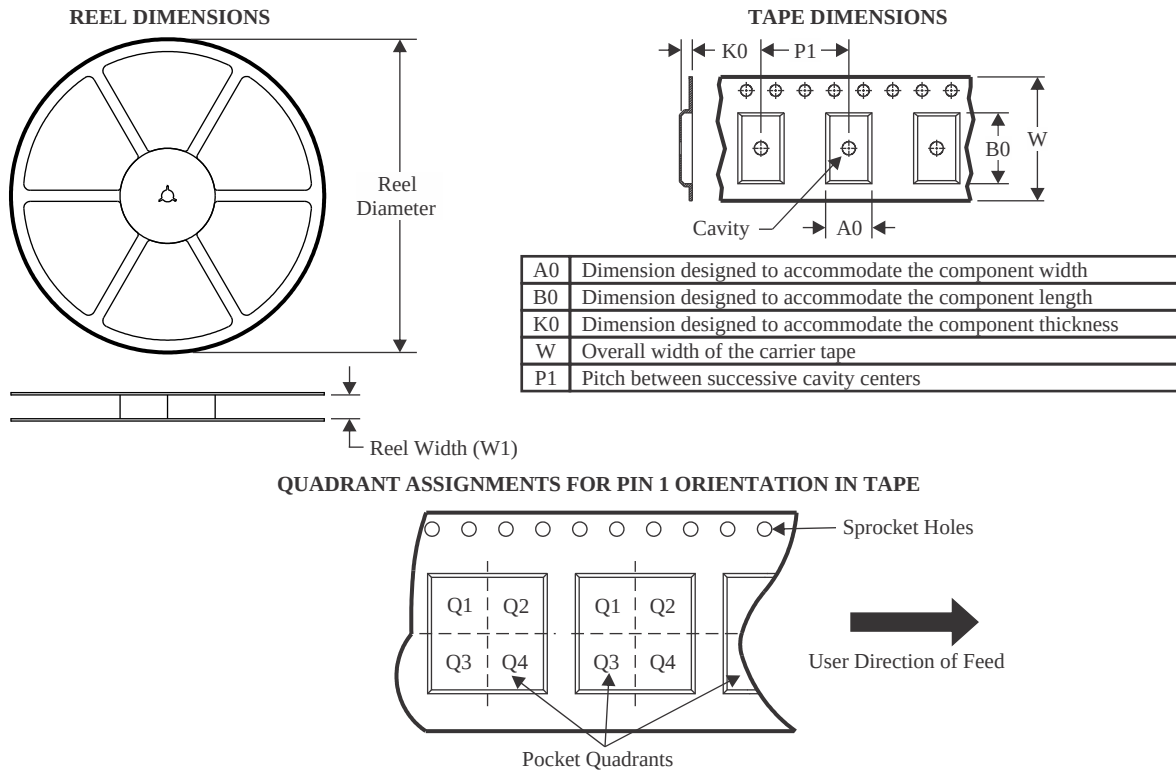
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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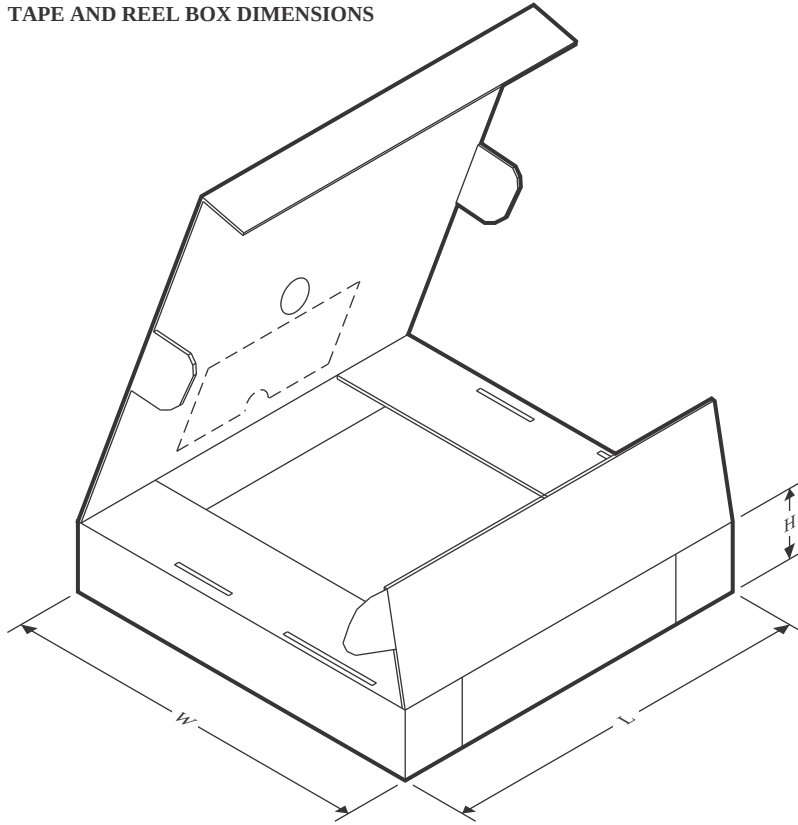
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17571Q2	WSO	DQK	6	3000	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17571Q2	WSON	DQK	6	3000	189.0	185.0	36.0

GENERIC PACKAGE VIEW

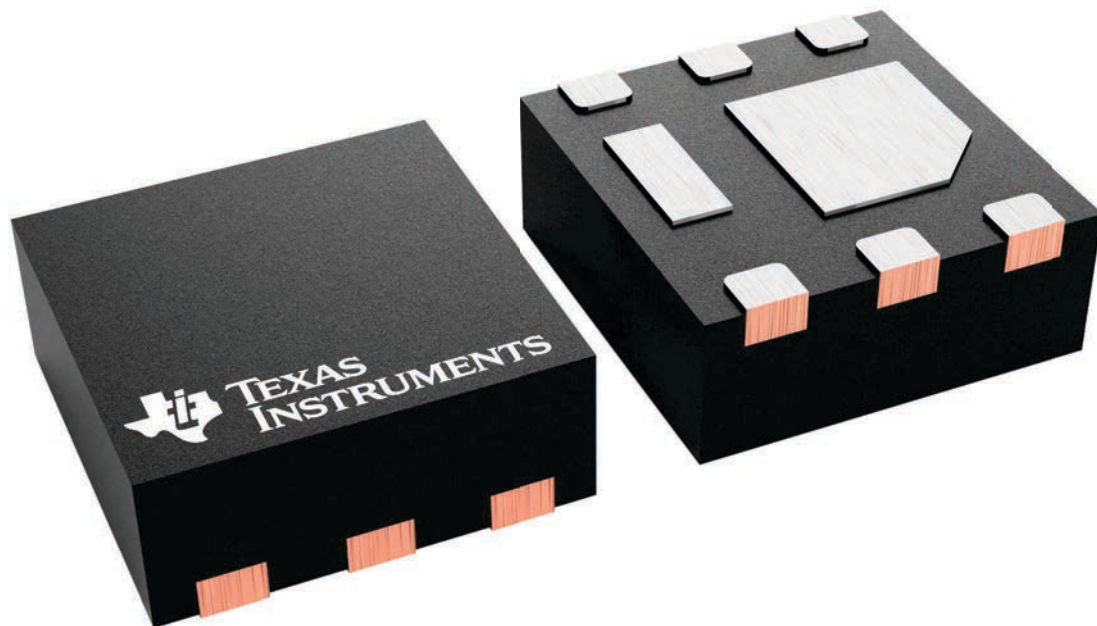
DQK 6

WSON - 0.8 mm max height

2 x 2, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

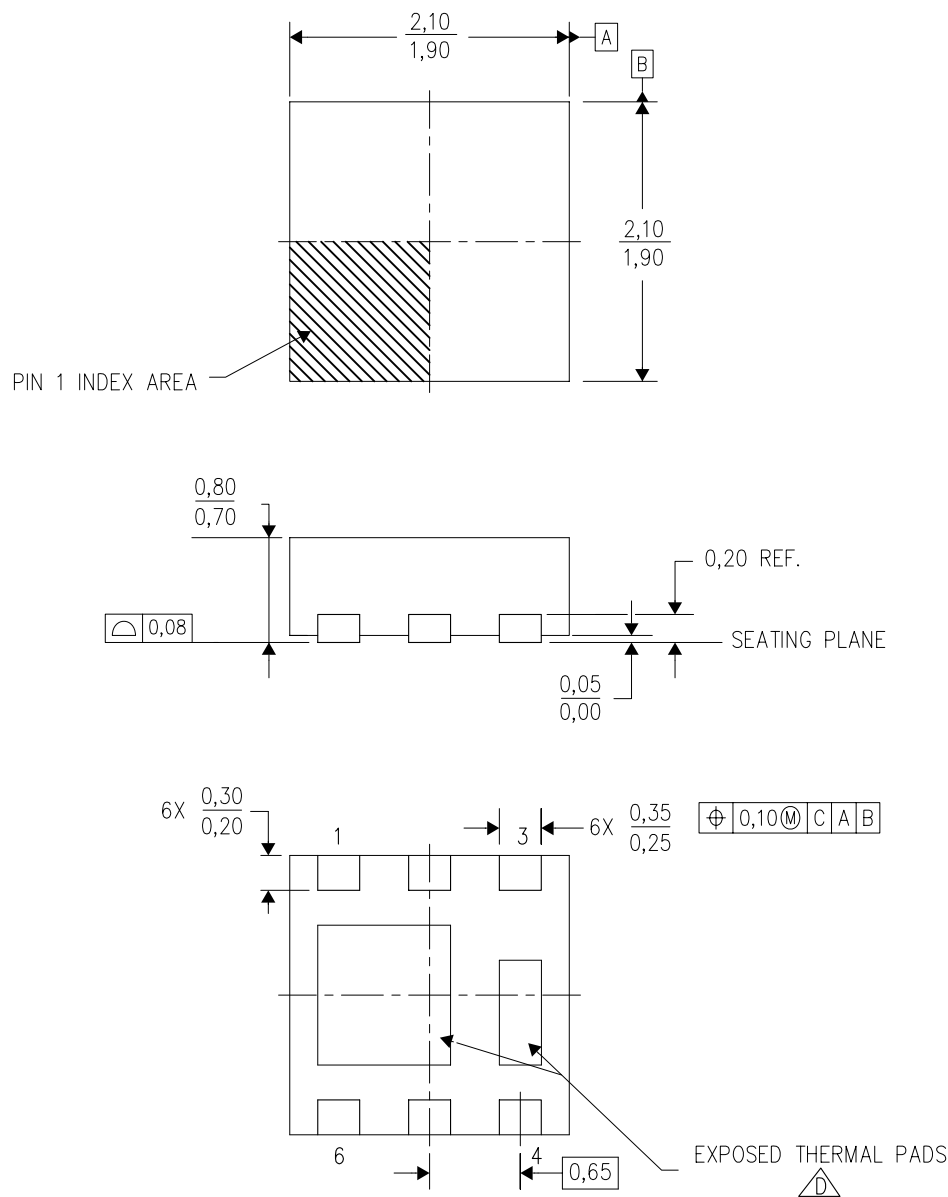
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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DQK (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4210192/B 01/10

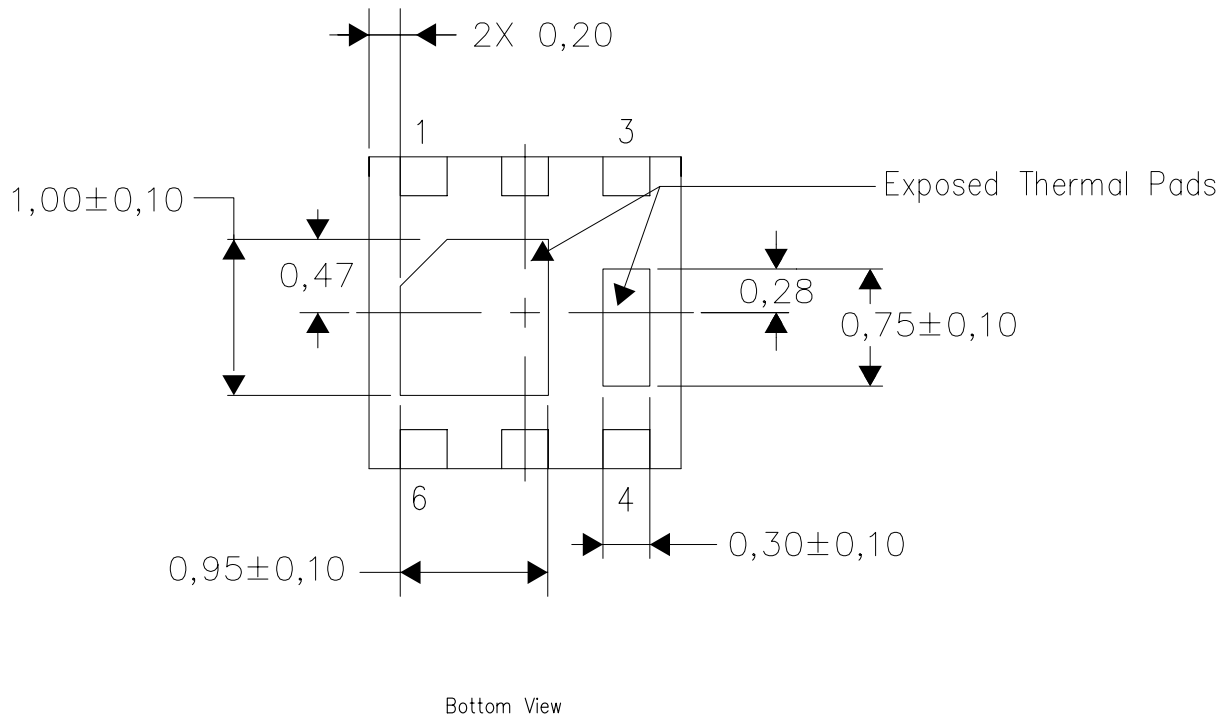
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - ⚠ D. The package thermal pads must be soldered to the board for thermal and mechanical performance.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

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