CSD17559Q5 30V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 极低电阻
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 5mm x 6mm 塑料封装

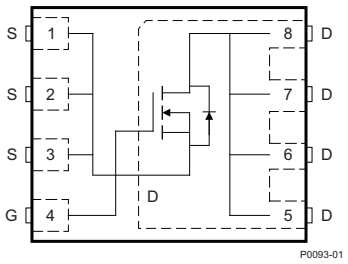
2 应用范围

- 网络互联、电信和计算系统中的负载点同步降压
- 同步整流
- 有源或操作 (ORing) 和热插拔应用

3 说明

这款 30V，0.95mΩ，5mm × 6mm SON 封装 NexFET™ 功率 MOSFET 设计用于大大降低同步整流和其它功率转换应用中的损耗。

顶视图



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	栅极电荷总量 (4.5V)	39		nC
Q_{gd}	栅漏栅极电荷	9.3		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5 V	1.15	mΩ
		V_{GS} = 10V	0.95	mΩ
$V_{GS(th)}$	阈值电压	1.4		V

订购信息(1)

器件	数量	介质	封装	出货
CSD17559Q5	2500	13 英寸卷带	SON 5mm x 6mm 塑料封装	卷带封装
CSD17559Q5T	250	13 英寸卷带		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

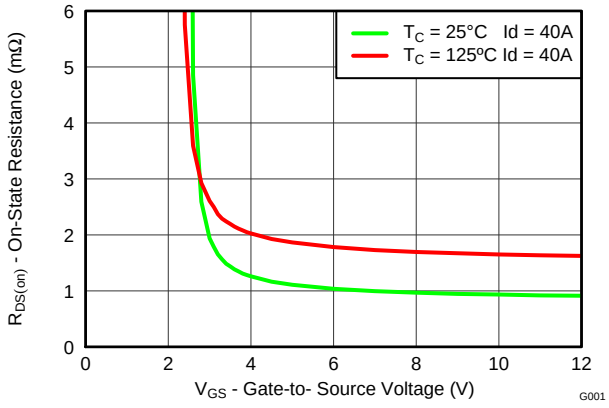
最大绝对额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	100	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	257	
	持续漏极电流(1)	40	A
I_{DM}	脉冲漏极电流(2)	400	A
P_D	功率耗散(1)	3.2	W
	功率耗散，T_C = 25°C	96	
T_J，T_{stg}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 104A，L = 0.1mH，R_G = 25Ω	541	mJ

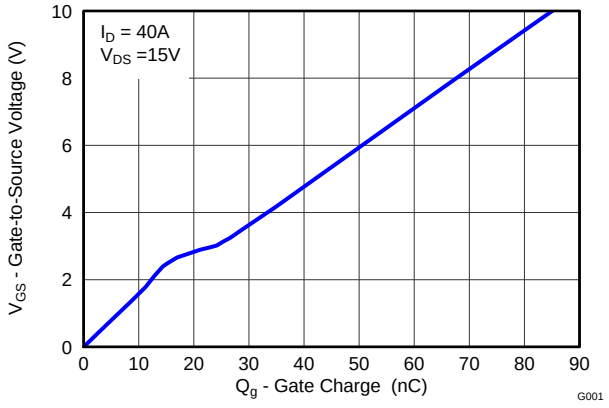
(1) $R_{\theta JA}$ = 40°C/W，这是在厚度为 0.06 英寸 (1.52 mm) 的环氧板 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2 (6.45 cm^2)，2 盎司（厚度为 0.071 mm）的铜过渡垫片上测得的典型值。

(2) 最大 $R_{\theta JC}$ = 1.2°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



目录

4 修订历史记录

Changes from Original (Novermber 2012) to Revision A **Page**

- 1
- 已添加 已添加小卷带信息 1
- 已将最大脉冲漏极电流增至 400A 1
- 添加了外壳温度保持在 25°C 时的最大功耗一行 1
- 更新了最大脉冲电流条件 1
- Updated Figure 1 to a normalized $R_{\theta JC}$ curve 4
- Updated the SOA in Figure 10 6

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_{DS} = 250 µA	30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.2	1.4	1.7	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_{DS} = 40 A		1.15	1.5	mΩ
		V_{GS} = 10 V, I_{DS} = 40 A		0.95	1.15	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 40 A		235		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		7070	9200	pF
C_{oss}	Output Capacitance			1780	2314	pF
C_{rss}	Reverse Transfer Capacitance			87	113	pF
R_G	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 15 V, I_{DS} = 40 A		39	51	nC
Q_{gd}	Gate Charge Gate-to-Drain			9.3		nC
Q_{gs}	Gate Charge Gate-to-Source			14.4		nC
$Q_{g(th)}$	Gate Charge at V_{th}			8.3		nC
Q_{oss}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		50		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 40 A, R_G = 2 Ω		20		ns
t_r	Rise Time			41		ns
$t_{d(off)}$	Turn Off Delay Time			32		ns
t_f	Fall Time			14		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 40 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD}= 15 V, I_F = 40 A, di/dt = 300 A/µs		80		nC
t_{rr}	Reverse Recovery Time			37		ns

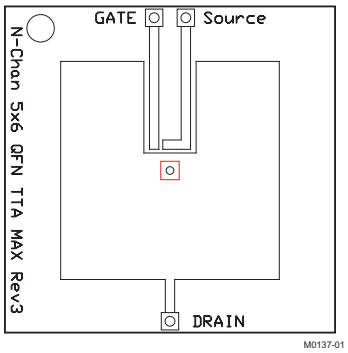
5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

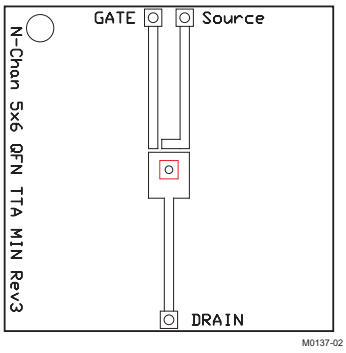
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			1.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

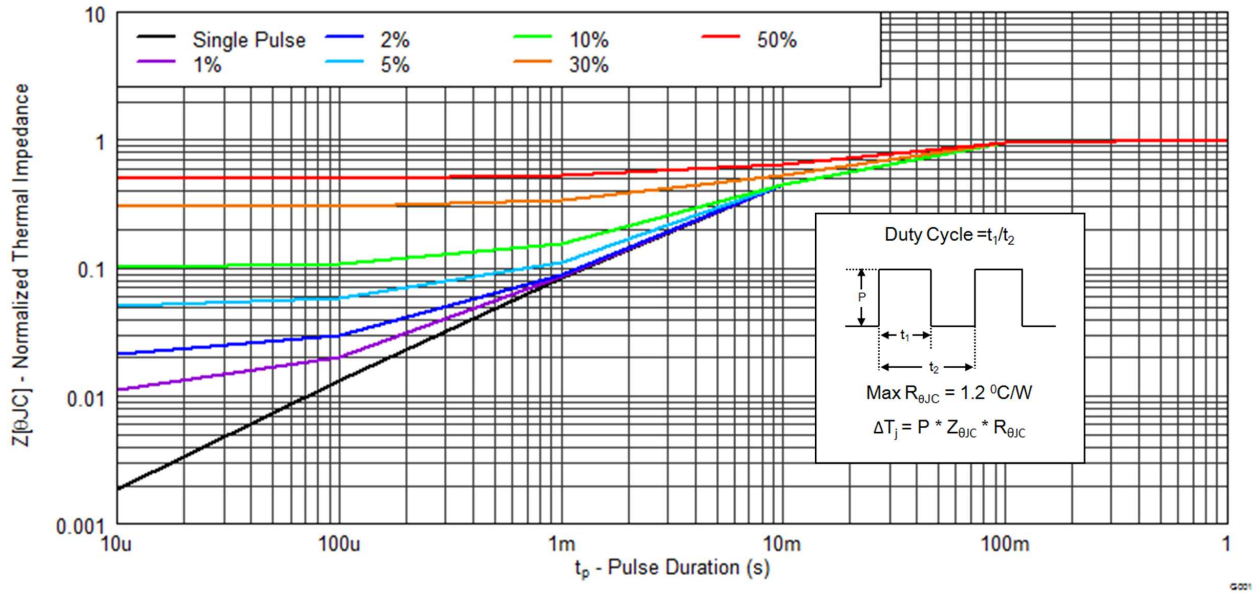


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

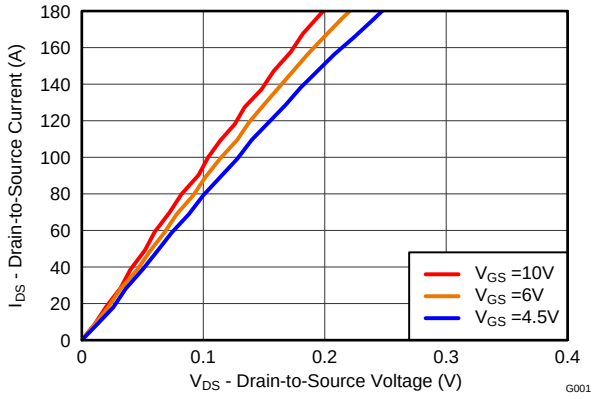


Figure 2. Saturation Characteristics

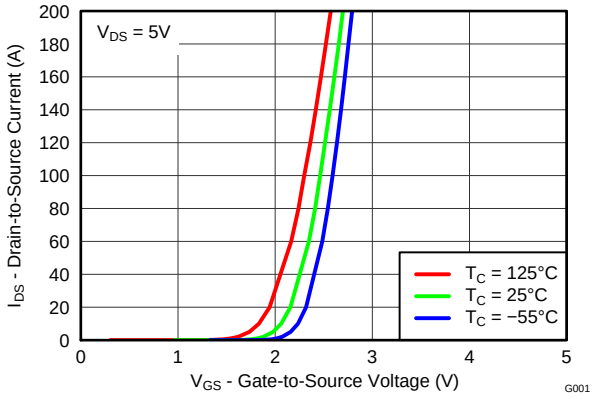


Figure 3. Transfer Characteristics

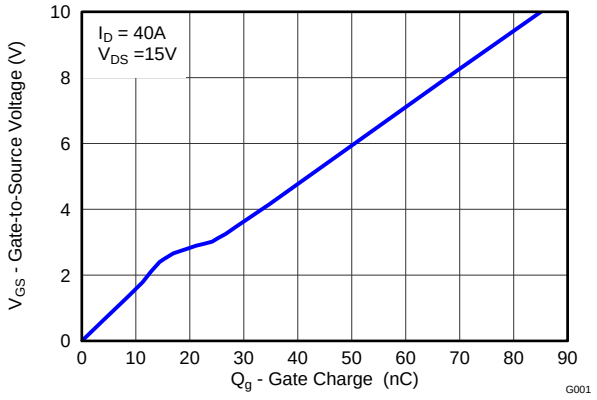


Figure 4. Gate Charge

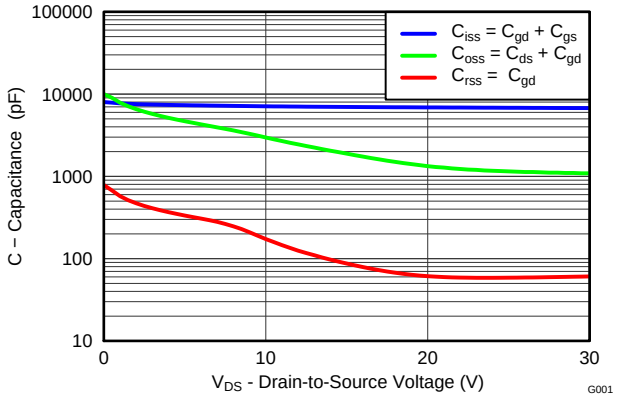


Figure 5. Capacitance

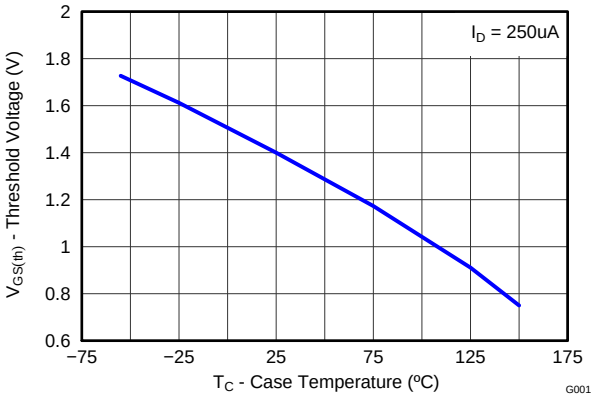


Figure 6. Threshold Voltage vs Temperature

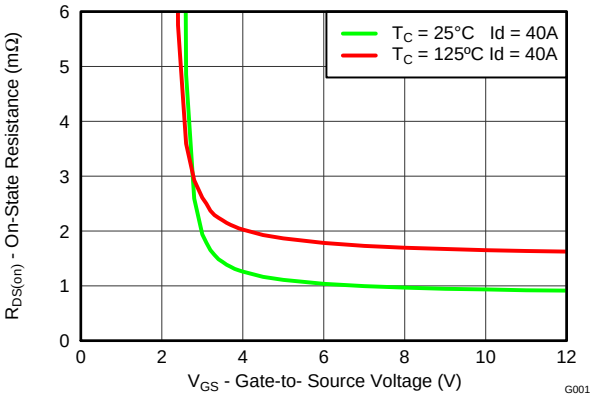


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

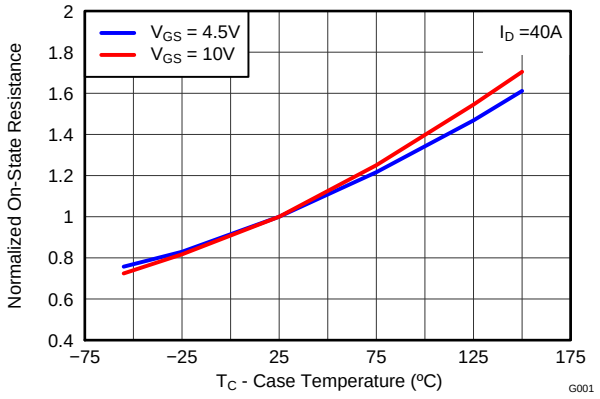


Figure 8. Normalized On-State Resistance vs Temperature

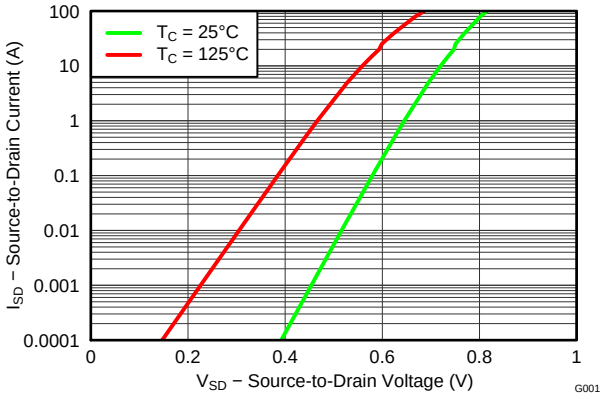


Figure 9. Typical Diode Forward Voltage

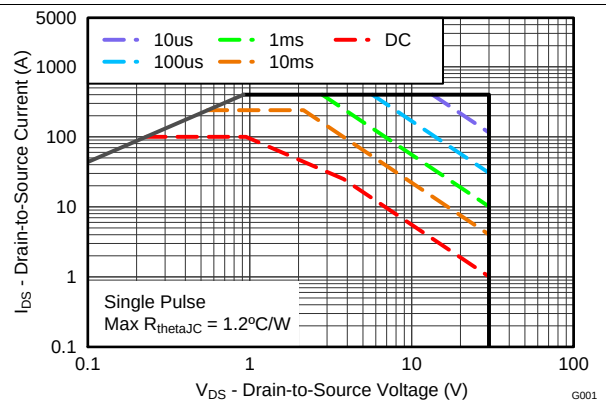


Figure 10. Safety Operating Area

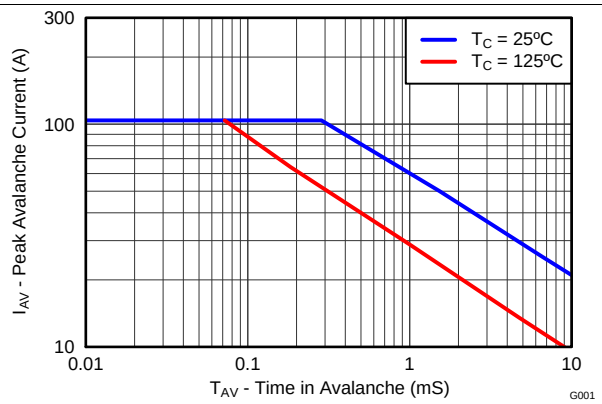


Figure 11. Single Pulse Unclamped Inductive Switching

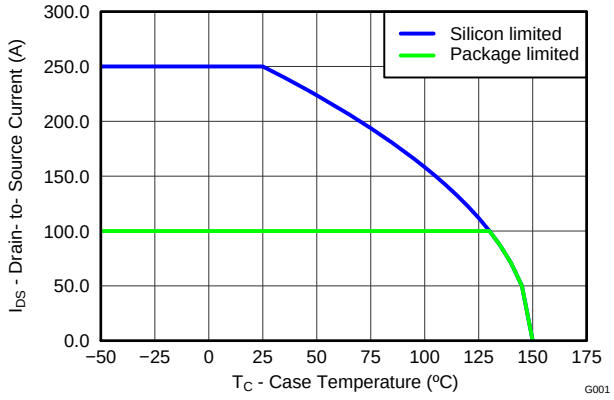


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.

6.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

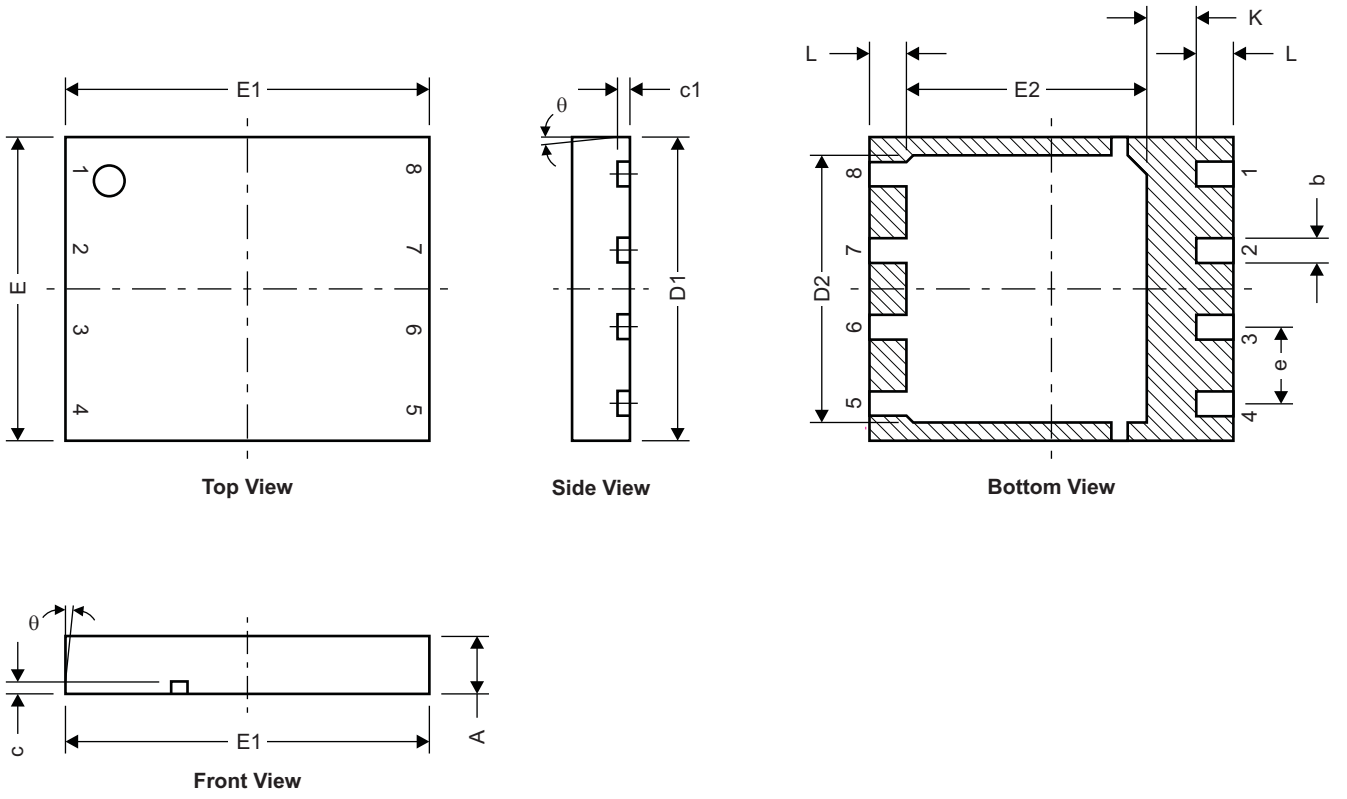
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械封装和可订购信息

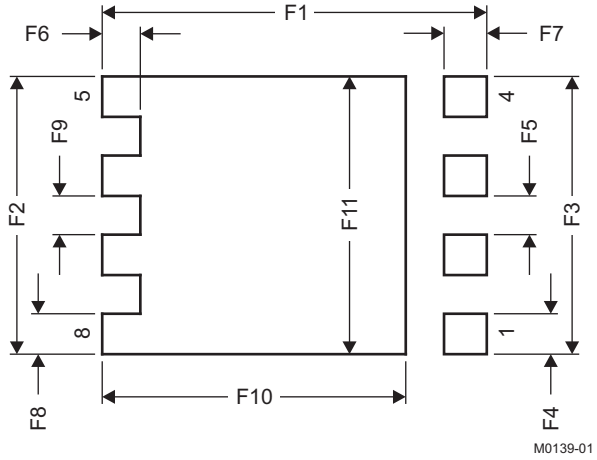
以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q5 封装尺寸



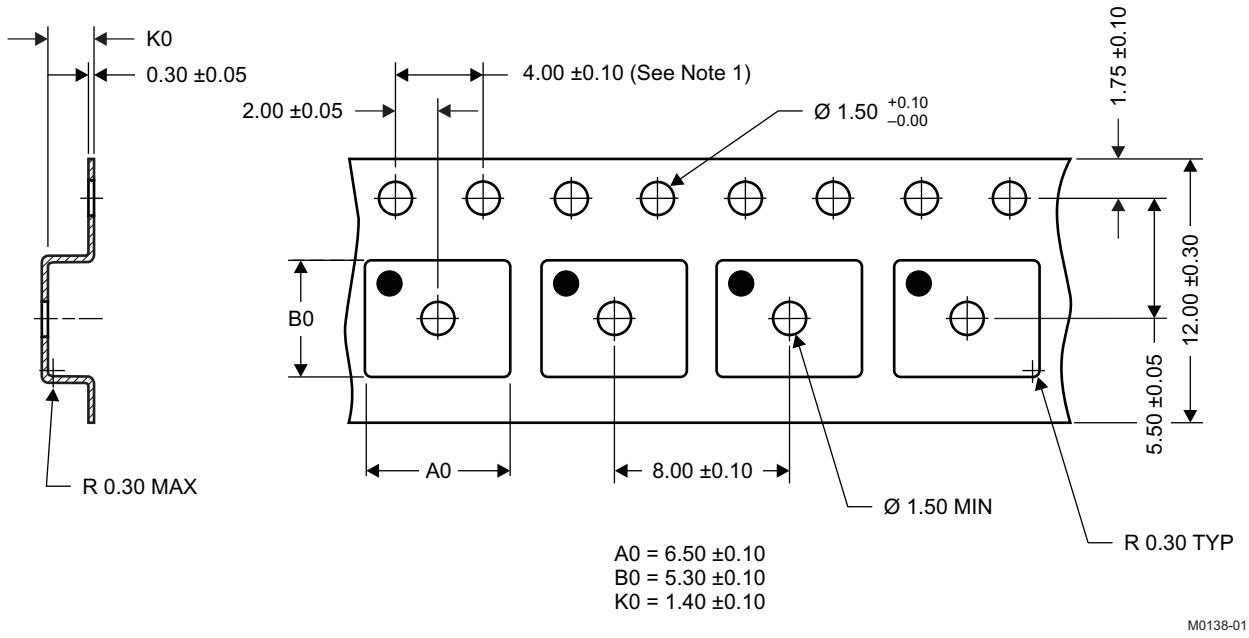
DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 典型值		0.050	
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
θ	0.00	—	—	—

建议印刷电路板 **(PCB)** 布局



DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

7.2 Q5 卷带信息



注释：

1. 10 个链齿孔的累积容差为 ±0.2
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）。
5. 厚度：0.30 ± 0.05mm
6. MSL1 260°C（红外 (IR) 和传导）PbF 回流焊兼容。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17559Q5	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17559
CSD17559Q5.B	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17559
CSD17559Q5T	Active	Production	VSON-CLIP (DQH) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17559
CSD17559Q5T.B	Active	Production	VSON-CLIP (DQH) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17559

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

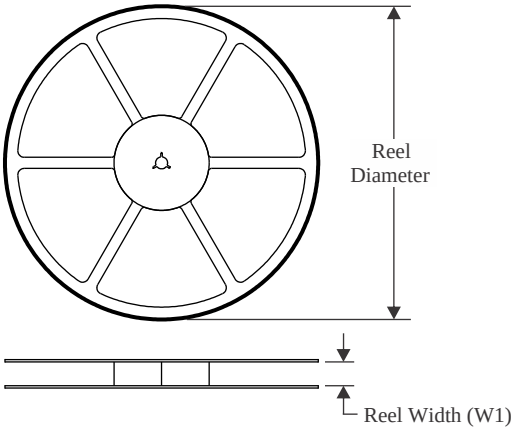
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

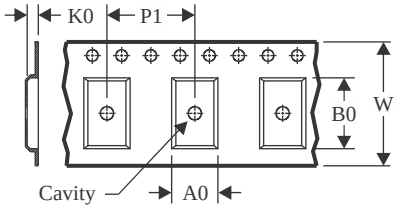
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

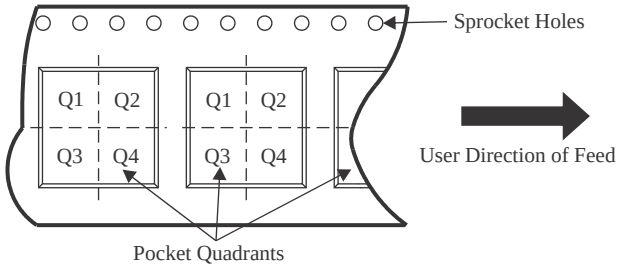


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

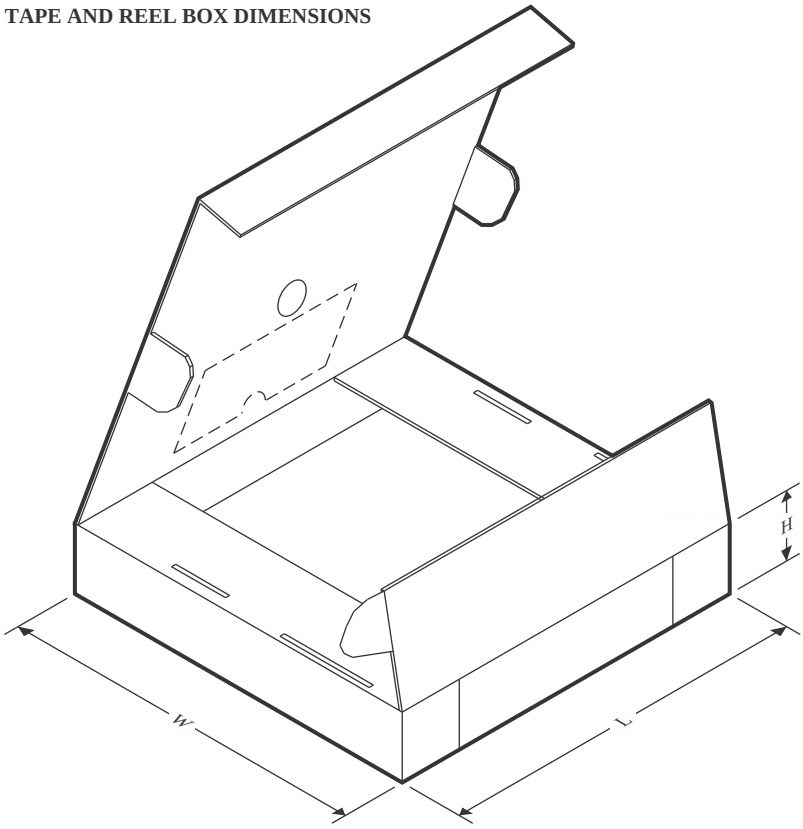
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17559Q5T	VSON-CLIP	DQH	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17559Q5T	VSON-CLIP	DQH	8	250	180.0	180.0	79.0

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