CSD17382F4 30V N 沟道 FemtoFET™ MOSFET

1 特性

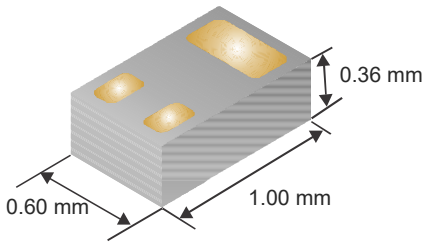
- 低导通电阻
- 低 Q_g 和 Q_{gd}
- 低阈值电压
- 超小封装尺寸（0402 外壳尺寸）
  - 1.0mm × 0.6mm
- 超薄型封装
  - 厚度为 0.36mm
- 集成型 ESD 保护二极管
  - 额定值 > 3kV 人体放电模型 (HBM)
  - 额定值 > 2kV 充电器件模型 (CDM)
- 无铅且无卤素
- 符合 RoHS

2 应用

- 针对负载开关应用进行了优化
- 针对通用开关应用进行了优化
- 单节电池应用
- 手持式和移动类应用

3 说明

该 30V、54mΩ N 沟道 FemtoFET™ MOSFET 技术经过设计和优化，能最大限度地减小在许多手持式和移动应用中的空间占用。这项技术能够在替代标准小信号 MOSFET 的同时将封装尺寸减小至少 60%。



典型器件尺寸

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	总栅极电荷 (4.5V)	2.1		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.63		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 1.8V	110	mΩ
		V_{GS} = 2.5V	67	mΩ
		V_{GS} = 4.5V	56	mΩ
		V_{GS} = 8.0V	54	mΩ
$V_{GS(th)}$	阈值电压	0.9		V

器件信息

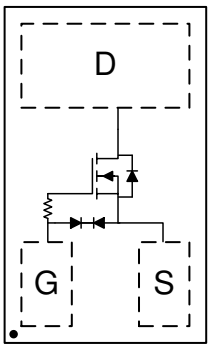
器件(1)	数量	介质	封装	配送
CSD17382F4	3000	7 英寸卷带	Femto (0402) 1.0mm × 0.6mm 无引线 SMD	卷带包装
CSD17382F4T	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	10	V
I_D	持续漏极电流(1)	2.3	A
I_{DM}	脉冲漏极电流(2)	14.8	A
P_D	功率耗散(1)	500	mW
ESD 等级	人体放电模型 (HBM)	3000	V
	组件充电模式 (CDM)	2000	V
T_J、T_{stg}	工作结温、贮存温度	–55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 6.5A，L = 0.1mH，R_G = 25Ω	2.1	mJ

(1) 典型 $R_{\theta JA}$ = 245°C/W（在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上安装 1 平方英寸 (6.45cm²)、2oz、0.071mm 厚的铜焊盘时）。
(2) 脉冲持续时间 ≤ 100μs，占空比 ≤ 1%.



顶视图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (October 2021) to Revision C (February 2022) **Page**

- 将超薄型封装要点中的厚度从 0.35mm 更改为 0.36mm.....1
- 将超薄型封装图片中的厚度从 0.35mm 更新为 0.36mm.....1
- Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....8
- Added FemtoFET Surface Mount Guide note.....9

Changes from Revision A (December 2016) to Revision B (October 2021) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1

Changes from Revision * (April 2016) to Revision A (December 2016) **Page**

- Changed the TEST CONDITIONS for g_{fs} Transconductance From: V_{DS} = 15 V To: V_{DS} = 3 V in the 节 5.1 section. 3
- Added 节 6.2 in the 节 6 section. 7
- Updated all mechanical drawings. 8

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 μA	30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 10 V			5	μA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	0.7	0.9	1.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 1.8 V, I_{DS} =0.5 A		110	180	mΩ
		V_{GS} = 2.5 V, I_{DS} =0.5 A		67	82	mΩ
		V_{GS} = 4.5 V, I_{DS} = 0.5 A		56	67	mΩ
		V_{GS} = 8.0 V, I_{DS} = 0.5 A		54	64	mΩ
g_{fs}	Transconductance	V_{DS} = 3 V, I_{DS} = 0.5 A		5.9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		267	347	pF
C_{oss}	Output capacitance			31.0	40.3	pF
C_{rss}	Reverse transfer capacitance			15.0	19.5	pF
R_G	Series gate resistance			220		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_{DS} = 0.5 A		2.1	2.7	nC
Q_{gd}	Gate charge gate-to-drain			0.63		nC
Q_{gs}	Gate charge gate-to-source			0.41		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.12		nC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		1.53		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 0.5 A, R_G = 0 Ω		59		ns
t_r	Rise time			111		ns
$t_{d(off)}$	Turn off delay time			279		ns
t_f	Fall time			270		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 0.5 A, V_{GS} = 0 V		0.7	1.0	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	85	°C/W
	Junction-to-ambient thermal resistance(2)	245	°C/W

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz. (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

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5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

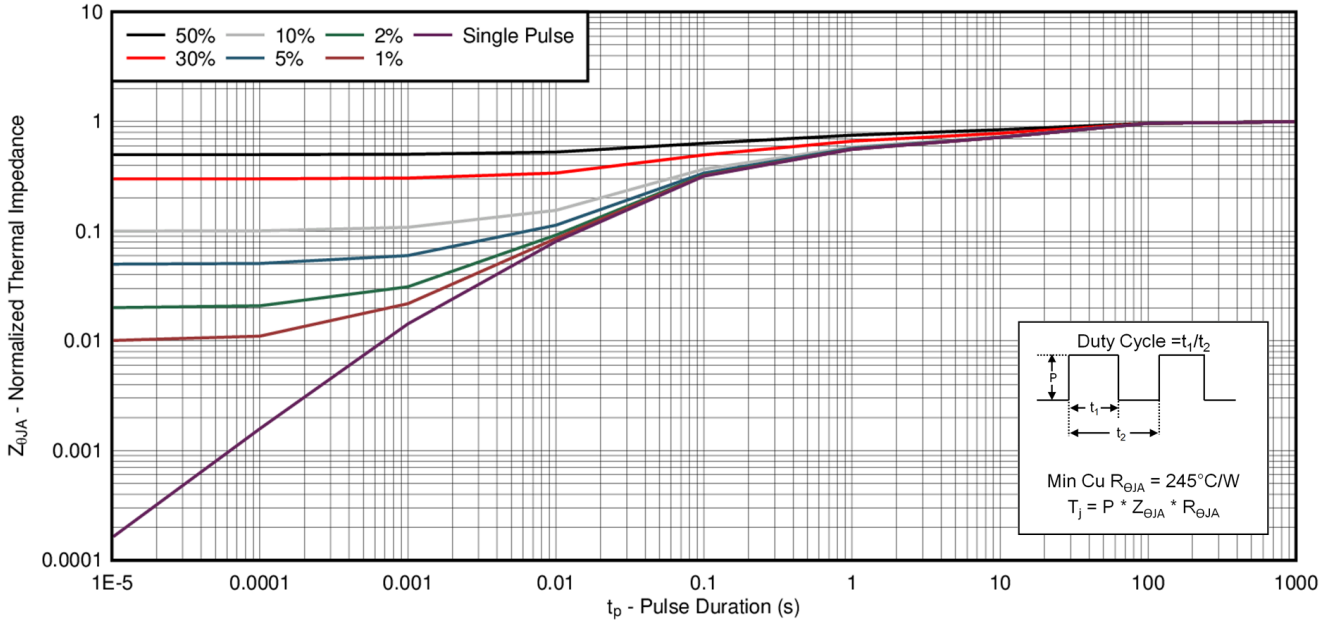


图 5-1. Transient Thermal Impedance

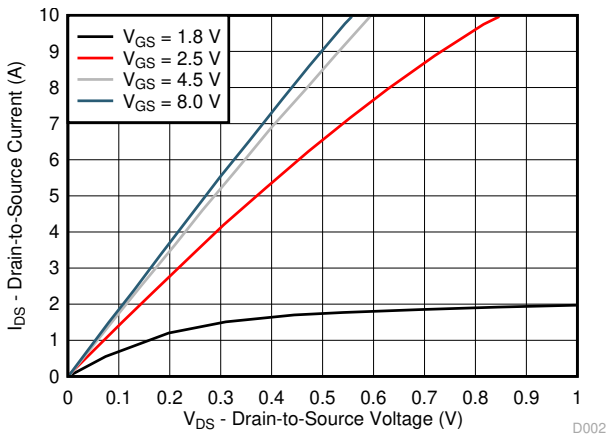
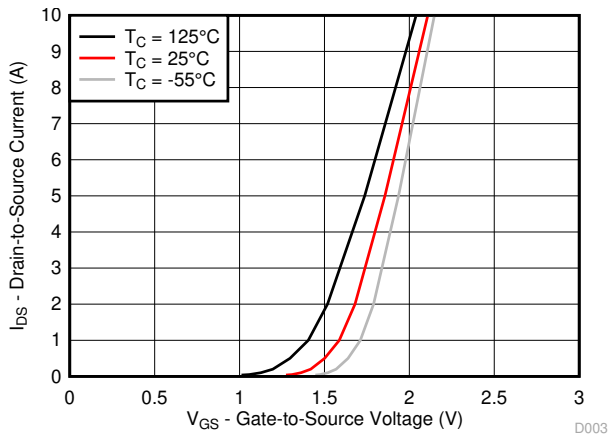


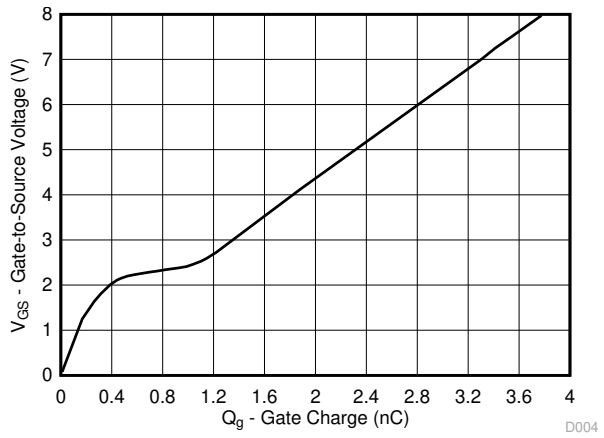
图 5-2. Saturation Characteristics



V_{DS} = 5 V

图 5-3. Transfer Characteristics

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I_D = 0.5 A V_{DS} = 15 V

图 5-4. Gate Charge

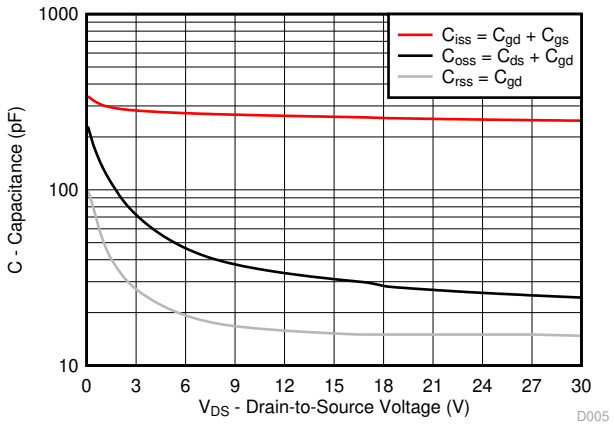
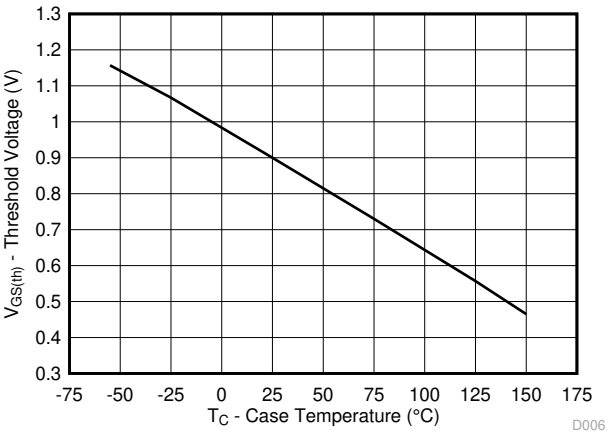


图 5-5. Capacitance



I_D = 250 µA

图 5-6. Threshold Voltage vs Temperature

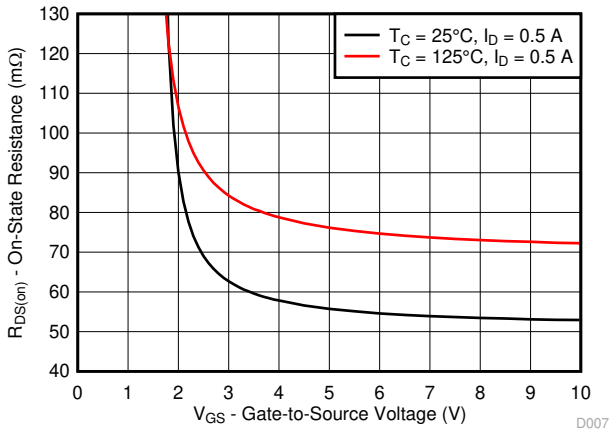
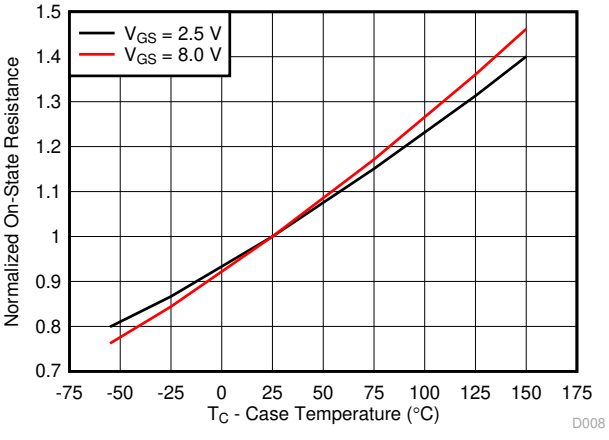


图 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 0.5 A

图 5-8. Normalized On-State Resistance vs Temperature

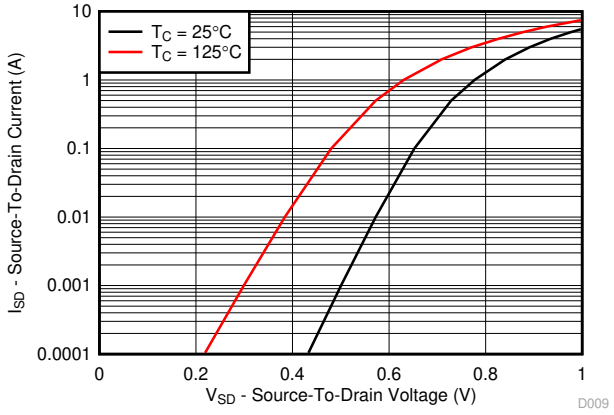
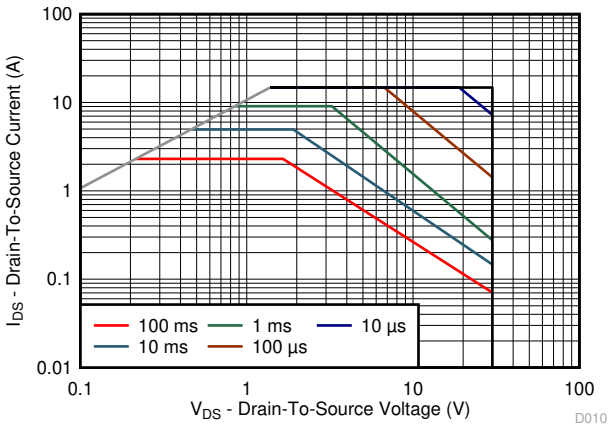


图 5-9. Typical Diode Forward Voltage



Single Pulse, Typ $R_{\theta JA}$ = 245°C/W (min Cu)

图 5-10. Maximum Safe Operating Area (SOA)

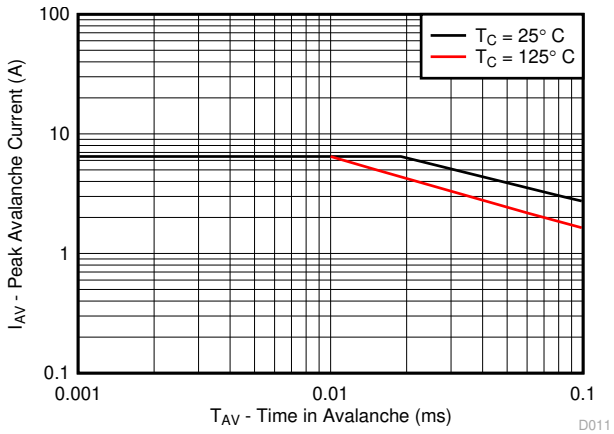
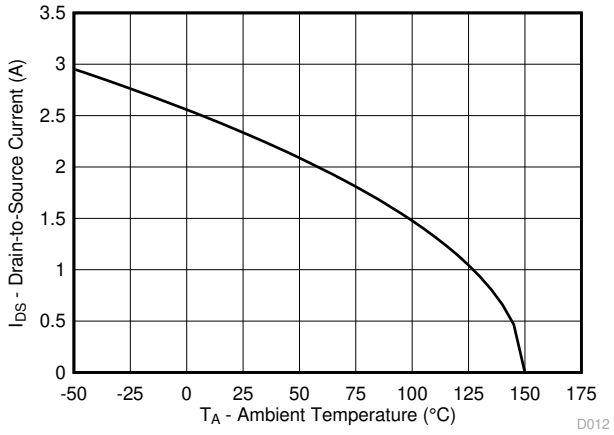


图 5-11. Single Pulse Unclamped Inductive Switching



Typical $R_{\theta JA}$ = 245°C/W (min Cu)

图 5-12. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 术语表

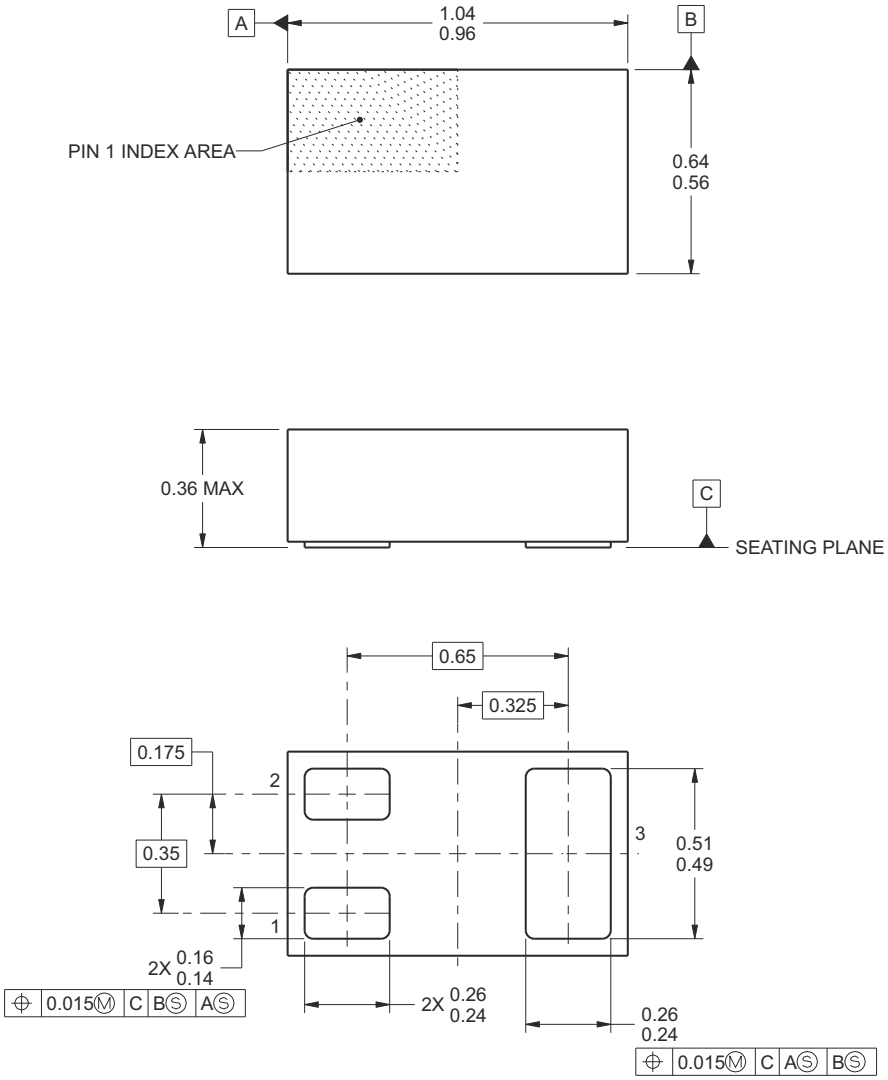
TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



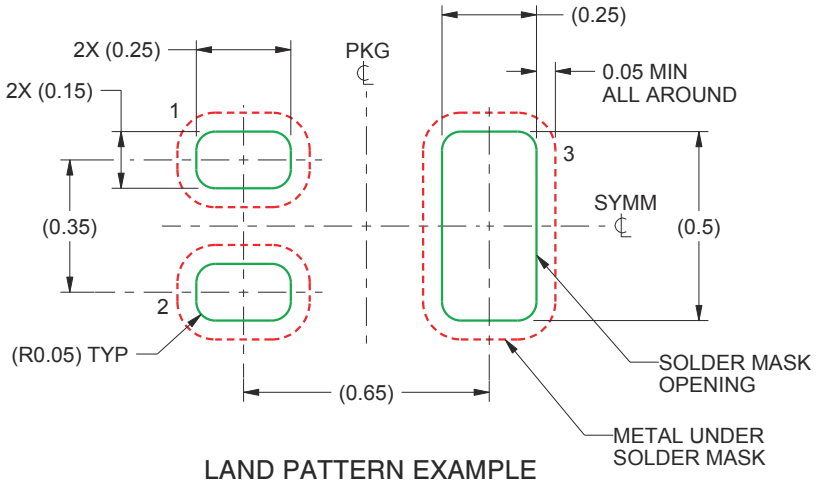
A. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

B. This drawing is subject to change without notice.

C. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

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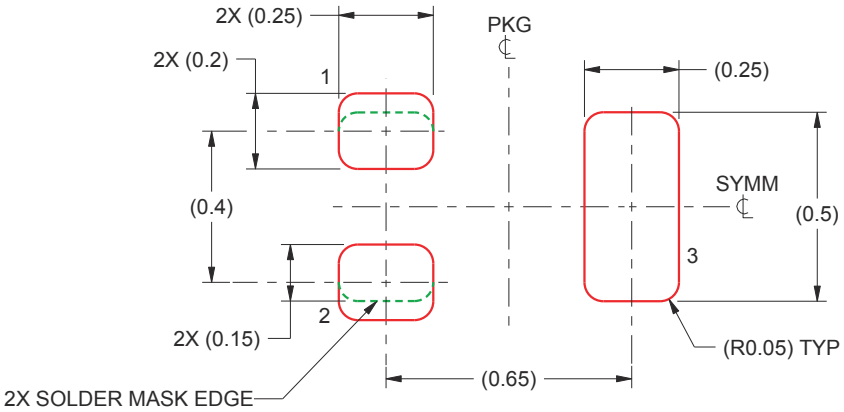
7.2 Recommended Minimum PCB Layout



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED

A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern

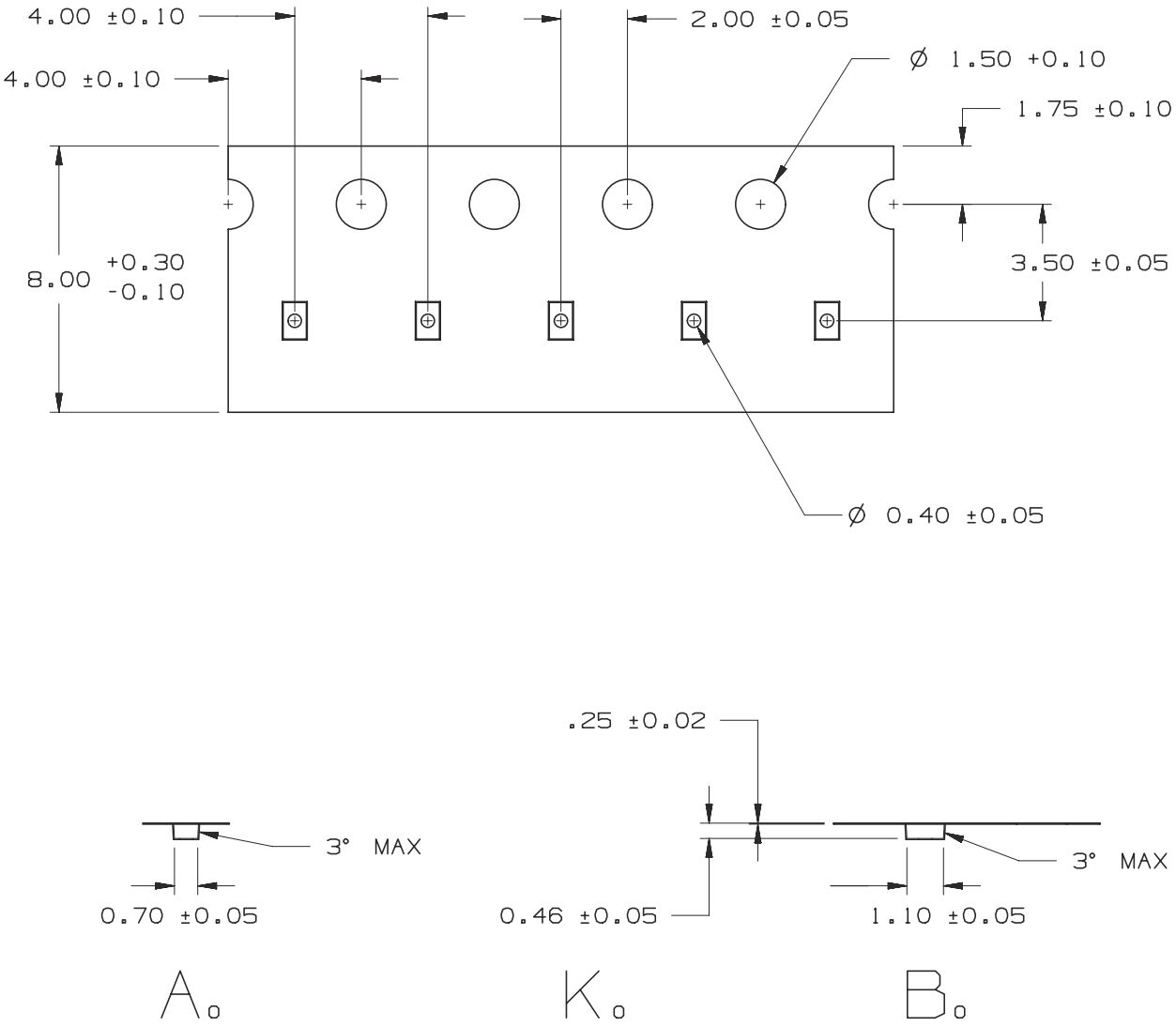


SOLDER PASTE EXAMPLE

A. All dimensions are in millimeters.
B. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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7.4 CSD17382F4 Embossed Carrier Tape Dimensions



A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17382F4	Active	Production	PICOSTAR (YJC) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	HM
CSD17382F4.B	Active	Production	PICOSTAR (YJC) | 3	3000 | LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	HM
CSD17382F4T	Active	Production	PICOSTAR (YJC) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	HM
CSD17382F4T.B	Active	Production	PICOSTAR (YJC) | 3	250 | SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	HM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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