

CSD17313Q2Q1 30V N 沟道 NexFET™ 功率 MOSFET

1 特性

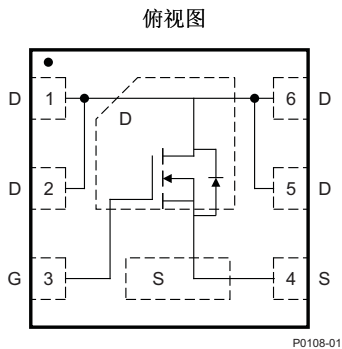
- 符合汽车应用 应用
- 针对 5V 栅极驱动器进行了优化
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 无铅
- 符合 RoHS 环保标准
- 无卤素
- 小外形尺寸无引线 (SON) 2mm x 2mm 塑料封装

2 应用

- 直流/直流转换器
- 电池和负载管理

3 说明

该 30V、24mΩ、2mm x 2mm SON NexFET™ 功率 MOSFET 旨在用于最大程度降低功率转换应用中的 并针对 5V 栅极驱动器应用进行了优化 应用中，2mm x 2mm SON 针对封装尺寸提供了出色的散热性能。



产品概要

$T_A = 25^\circ\text{C}$		典型值	单位
V_{DS}	漏源电压	30	V
Q_g	总栅极电荷 (4.5V)	2.1	nC
Q_{gd}	栅极电荷 (栅极到漏极)	0.4	nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 3\text{V}$	31 mΩ
		$V_{GS} = 4.5\text{V}$	26 mΩ
		$V_{GS} = 8\text{V}$	24 mΩ
$V_{GS(th)}$	阈值电压	1.3	V

订购信息⁽¹⁾

器件编号	数量	包装介质	封装	发货
CSD17313Q2Q1	3000	13 英寸卷带	SON 2mm x 2mm 塑料封装	卷带封装
CSD17313Q2Q1T	250	7 英寸卷带		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

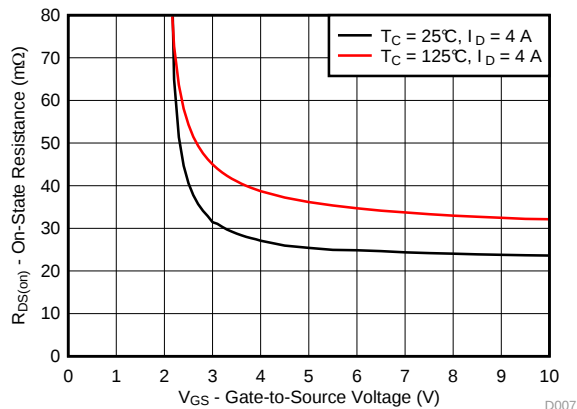
绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	+10 / -8	V
I_D	持续漏极电流 (受封装限制)	5	A
	持续漏极电流 (受器件限制), $T_C = 25^\circ\text{C}$	19	
	持续漏极电流 ⁽¹⁾	7.3	
I_{DM}	脉冲漏极电流, $T_A = 25^\circ\text{C}$ ⁽²⁾	57	A
P_D	功率耗散 ⁽¹⁾	2.4	W
	功率耗散, $T_C = 25^\circ\text{C}$	17	
T_J, T_S	运行结温和储存温度范围	-55 至 150	$^\circ\text{C}$
E_{AS}	雪崩能量, 单一脉冲, $I_D = 19\text{A}$, $L = 0.1\text{mH}$, $R_{GS} = 25\Omega$	18	mJ

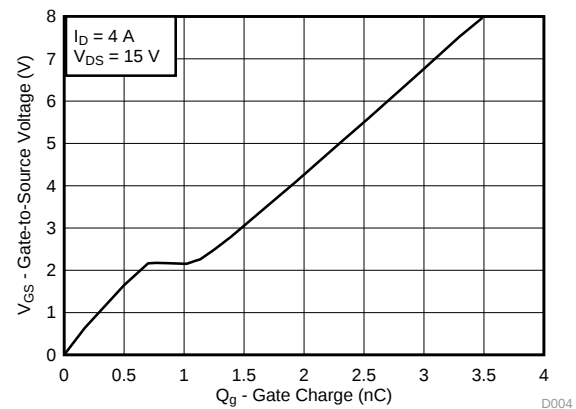
(1) $R_{\theta JA} = 53^\circ\text{C/W}$, 这是在 0.06 英寸厚 FR4 PCB 上的 1 平方英寸 2 盎司的铜焊盘上测得的典型值。

(2) 最大 $R_{\theta JC} = 7.4^\circ\text{C/W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$ 。

导通电阻与源极电压



栅极电荷



目录

1	特性	1	6.1	社区资源	7
2	应用	1	6.2	商标	7
3	说明	1	6.3	静电放电警告	7
4	修订历史记录	2	6.4	Glossary	7
5	Specifications	3	7	机械、封装和可订购信息	8
5.1	Electrical Characteristics	3	7.1	Q2 封装尺寸	8
5.2	Thermal Information	3	7.2	建议 PCB 布局	9
5.3	Typical MOSFET Characteristics	4	7.3	建议的模版布局	9
6	器件和文档支持	7	7.4	Q2 卷带信息	10

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (March 2013) to Revision D	Page
• 改进了 说明	1
• 向订购信息 表中添加了 7 英寸卷带	1
• 更新了持续漏极电流	1
• 更新了脉冲电流条件	1
• Updated Figure 1 to show $R_{\theta JC}$ curves	4
• Added $V_{GS} = 4.5\text{ V}$ line in Figure 8	5
• Updated the SOA in Figure 10	6
• 添加了 器件和文档 部分。	9

Changes from Revision B (January 2013) to Revision C	Page
• Changed Figure 10 , Maximum Safe Operating Area	5

Changes from Revision A (November 2012) to Revision B	Page
• 更改了建议的 PCB 布局	9
• 添加了建议的模版布局	9

Changes from Original (October 2012) to Revision A	Page
• 将器件编号从 CSD17313Q2-Q1 更改成了 CSD17313Q2Q1	1

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)

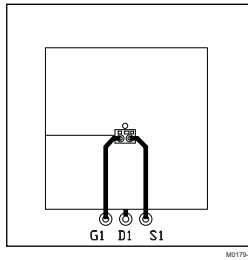
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
I _{DSS}	Drain-to-source leakage	V _{GS} = 0 V, V _{DS} = 24 V			1	μA
I _{GSS}	Gate-to-source leakage	V _{DS} = 0 V, V _{GS} = +10 / -8 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.9	1.3	1.8	V
R _{DS(on)}	Drain-to-source on resistance	V _{GS} = 3 V, I _D = 4 A		31	42	mΩ
		V _{GS} = 4.5 V, I _D = 4 A		26	32	mΩ
		V _{GS} = 8 V, I _D = 4 A		24	30	mΩ
g _{fs}	Transconductance	V _{DS} = 15 V, I _D = 4 A		16		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		260	340	pF
C _{oss}	Output capacitance			140	180	pF
C _{rss}	Reverse transfer capacitance			13	17	pF
R _G	Series gate resistance			1.3	2.6	Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 15 V, I _D = 4 A		2.1	2.7	nC
Q _{gd}	Gate charge – gate-to-drain			0.4		nC
Q _{gs}	Gate charge – gate-to-source			0.7		nC
Q _{g(th)}	Gate charge at V _{th}			0.3		nC
Q _{oss}	Output charge	V _{DS} = 13.5 V, V _{GS} = 0 V		3.8		nC
t _{d(on)}	Turn on delay time	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 4 A, R _G = 2 Ω		2.8		ns
t _r	Rise time			3.9		ns
t _{d(off)}	Turn off delay time			4.2		ns
t _f	Fall time			1.3		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 4 A, V _{GS} = 0V		0.85	1	V
Q _{rr}	Reverse recovery charge	V _{DD} = 13.5 V, I _F = 4 A, di/dt = 300 A/μs		6.4		nC
t _{rr}	Reverse recovery time			12.9		ns

5.2 Thermal Information

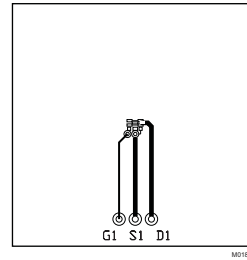
 $T_A = 25^\circ\text{C}$ (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance junction-to-case ⁽¹⁾			7.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal resistance junction-to-ambient ⁽¹⁾⁽²⁾			67	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch $\times$ 1.5-inch (3.81-cm $\times$ 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



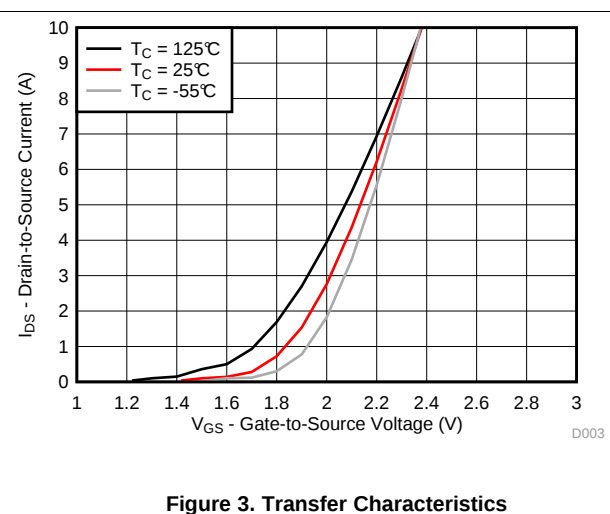
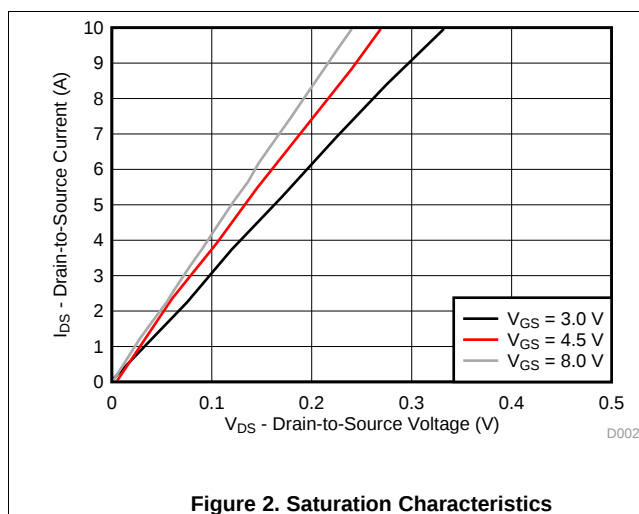
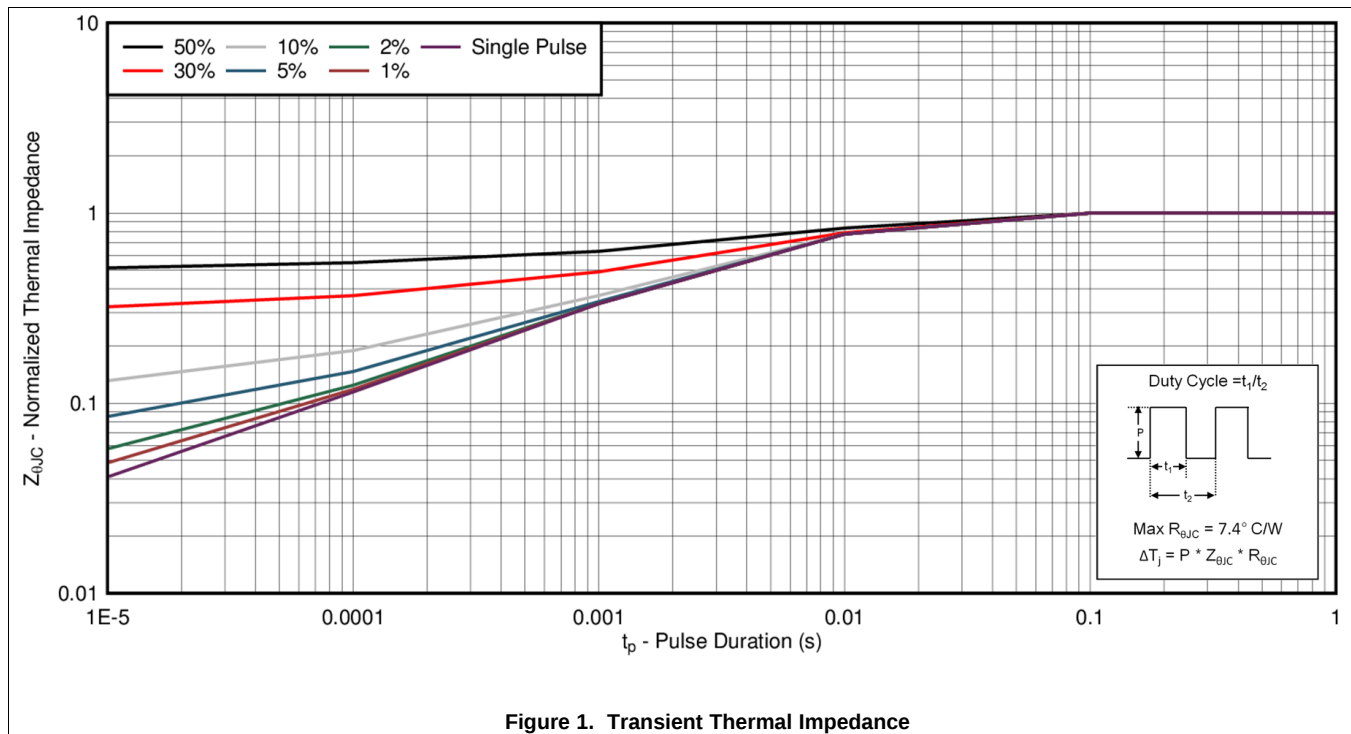
Max $R_{\theta JA} = 67^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2
oz. (0.071 mm thick)
Cu.



Max $R_{\theta JA} = 228^{\circ}\text{C/W}$
when mounted on a
minimum pad area of 2
oz. (0.071 mm thick)
Cu.

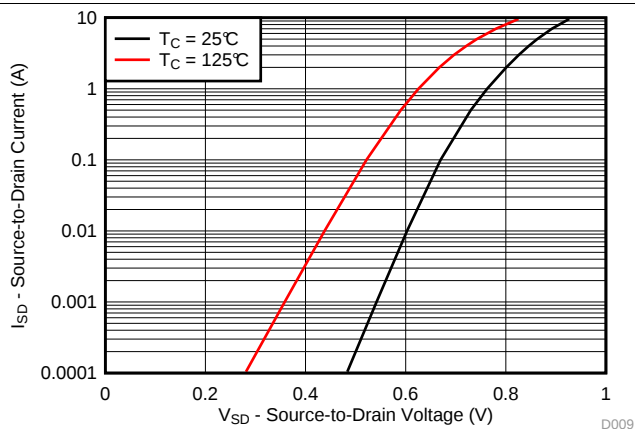
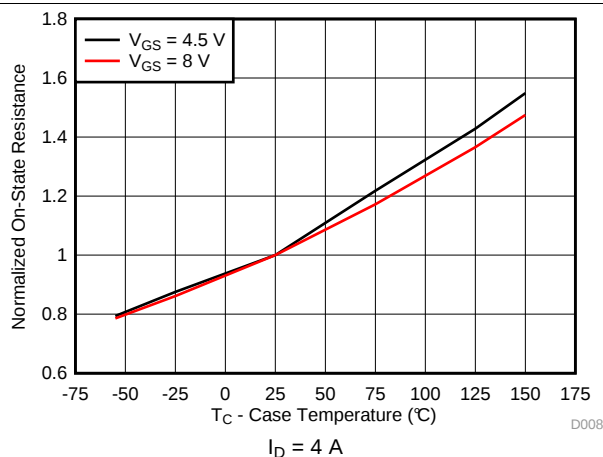
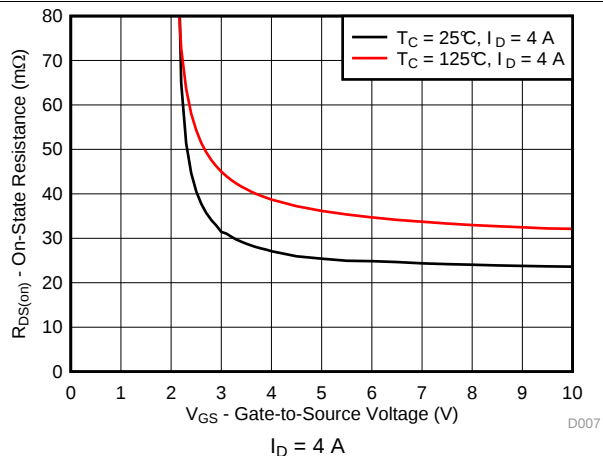
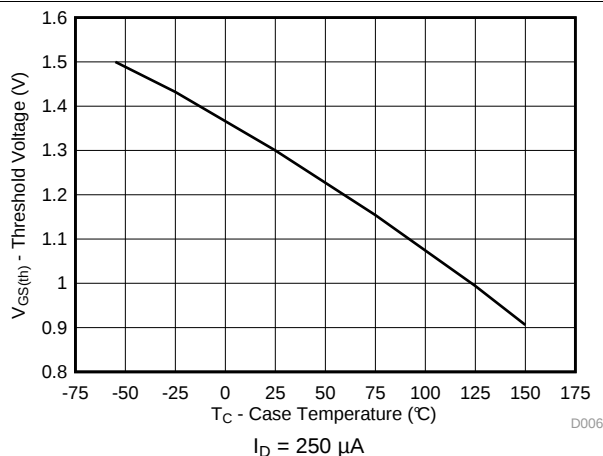
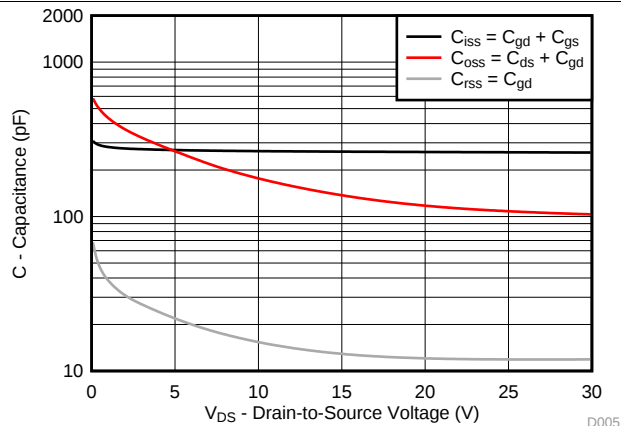
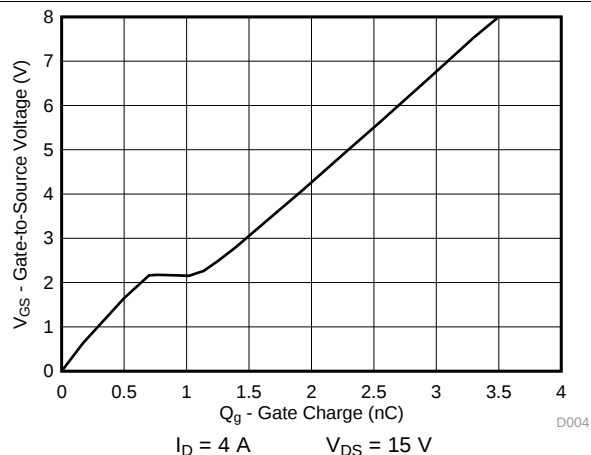
5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise noted)



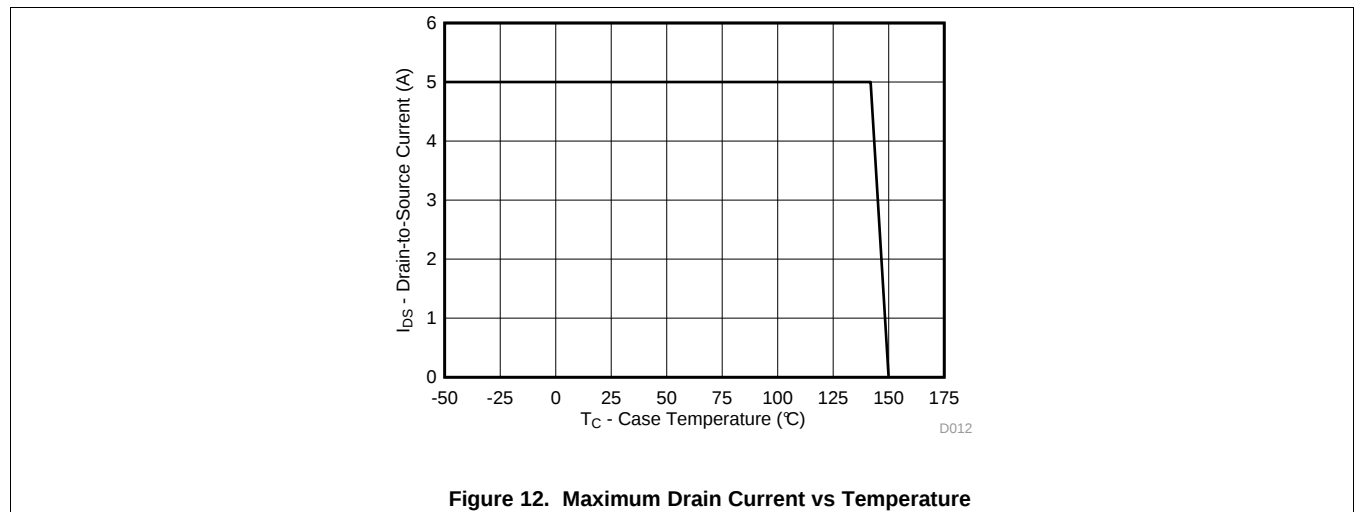
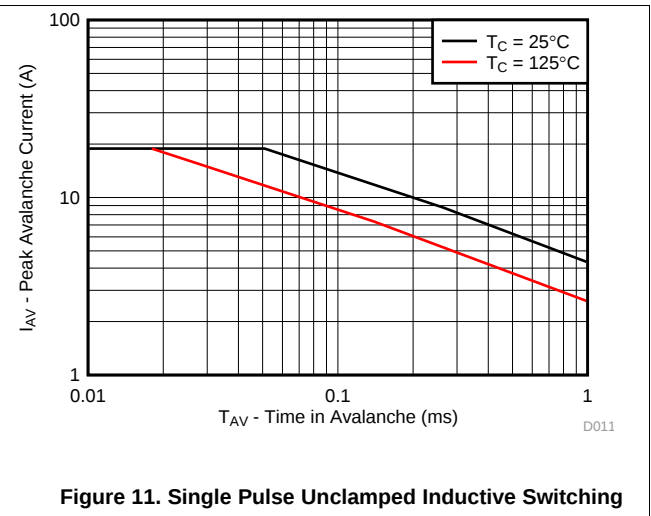
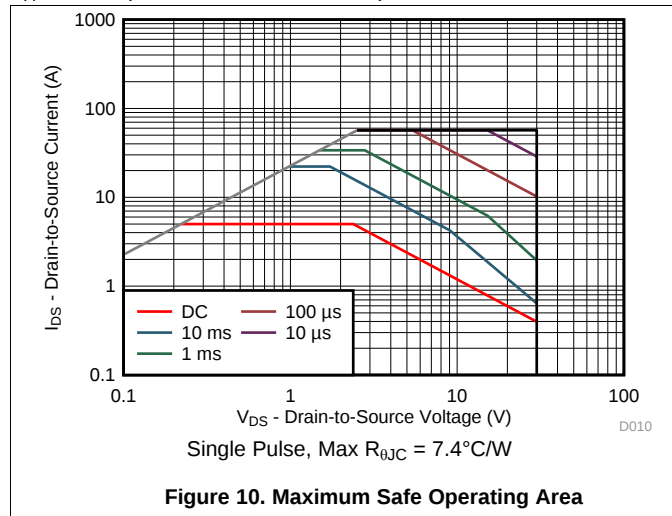
Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)



6 器件和文档支持

6.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.2 商标

NexFET, E2E are trademarks of Texas Instruments.
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6.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

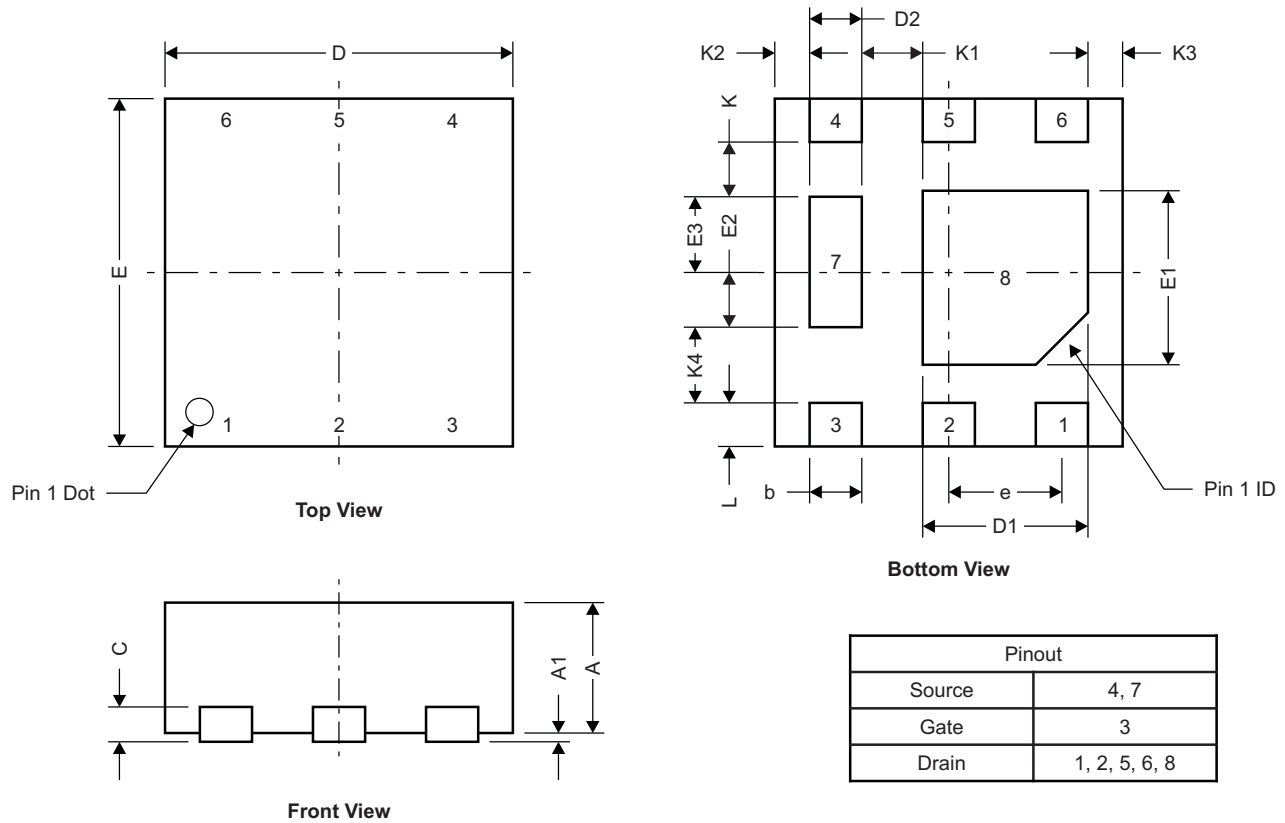
6.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

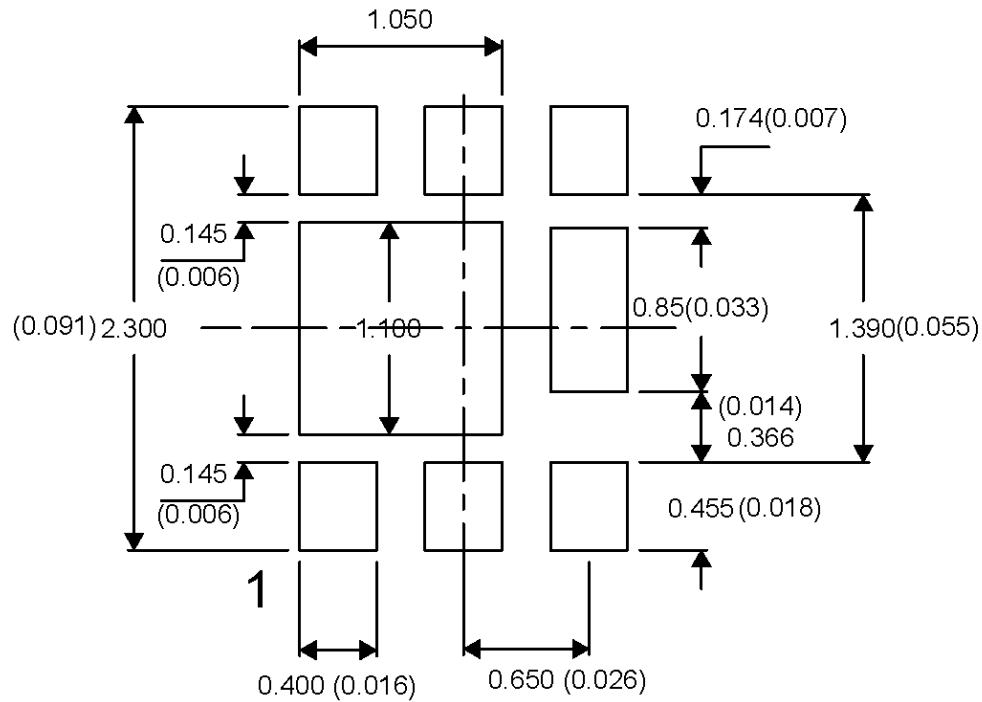
7.1 Q2 封装尺寸



M0175-02

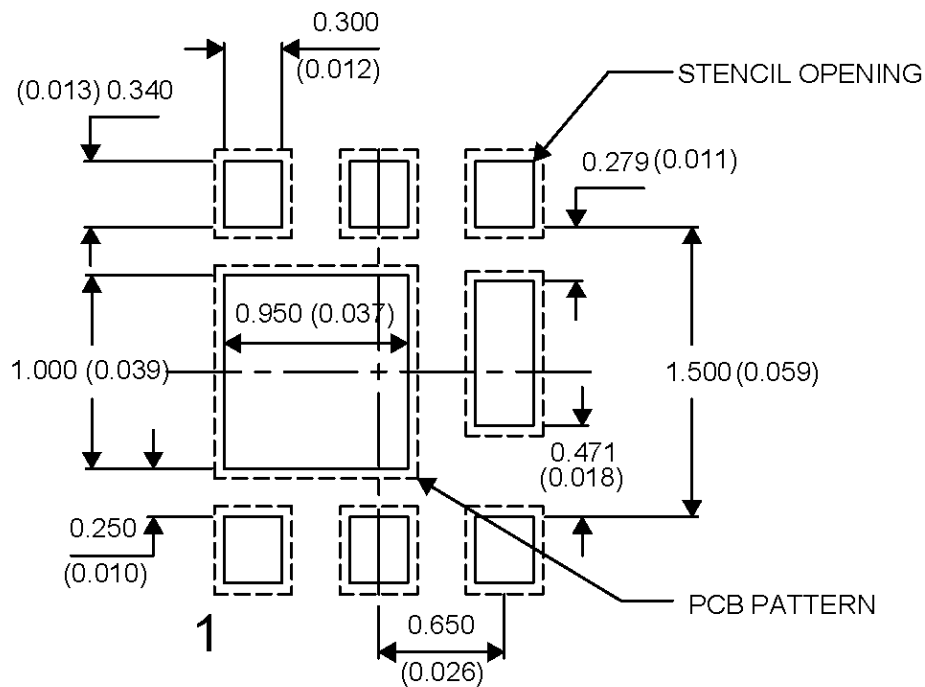
DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C	0.203 典型值			0.008 典型值		
D	2.000 典型值			0.080 典型值		
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2	0.300 典型值			0.012 典型值		
E	2.000 典型值			0.080 典型值		
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2	0.280 典型值			0.0112 典型值		
E3	0.470 典型值			0.0188 典型值		
e	0.650 BSC			0.026 典型值		
K	0.280 典型值			0.0112 典型值		
K1	0.350 典型值			0.014 典型值		
K2	0.200 典型值			0.008 典型值		
K3	0.200 典型值			0.008 典型值		
K4	0.470 典型值			0.0188 典型值		
L	0.200	0.25	0.300	0.008	0.010	0.012

7.2 建议 PCB 布局



如需了解针对 PCB 设计的建议电路布局，请参阅应用手册《通过 PCB 布局技巧来减少振铃》，（[SLPA005](#)）。

7.3 建议的模版布局



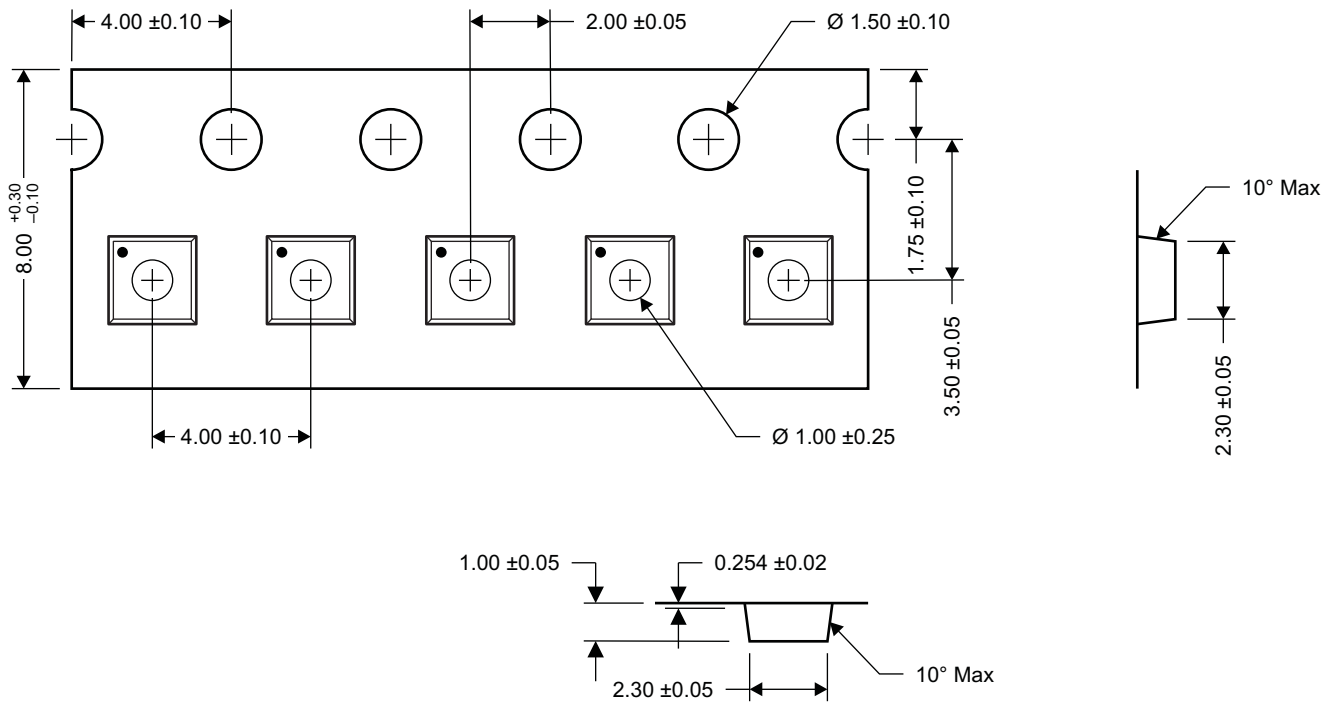
Note: 全部尺寸单位为 mm，除非另外注明。

CSD17313Q2Q1

ZHCSAF2D – OCTOBER 2012 – REVISED SEPTEMBER 2015

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7.4 Q2 卷带信息



- Notes:
1. 测自链齿孔中心线到孔眼中心线
 2. 10 个链齿孔的累积容差为 ± 0.20
 3. 其他材料可用
 4. 卷带的 SR 典型值最大为 10^8 OHM/SQ
 5. 除非另有说明，否则所有尺寸单位均为 mm。

M0168-01

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17313Q2Q1T	Obsolete	Production	WSO (DQK) 6	-	-	Call TI	Call TI	0 to 0	733Q

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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最后更新日期：2025 年 10 月