CD74HC4051-Q1 汽车级模拟多路复用器或多路信号分离器

1 特性

- 符合汽车应用要求
- 宽模拟输入电压范围：±5V（最大值）
- 低导通电阻：
  - 70Ω 典型值 (V_{CC} – V_{EE} = 4.5V)
  - 40Ω 典型值 (V_{CC} – V_{EE} = 9V)
- 低开关间串扰
- 快速开关和传播速度
- 先断后合开关
- 工作控制电压 = 2V 至 6V
- 开关电压 = 0V 至 10V
- 高抗噪性，N_{IL} 和 N_{IH} = V_{CC} 的 30%，V_{CC} = 5V

2 应用

- 数字射频
- 信号门控
- 工厂自动化
- 电视
- 电器
- 可编程逻辑电路
- 传感器

3 说明

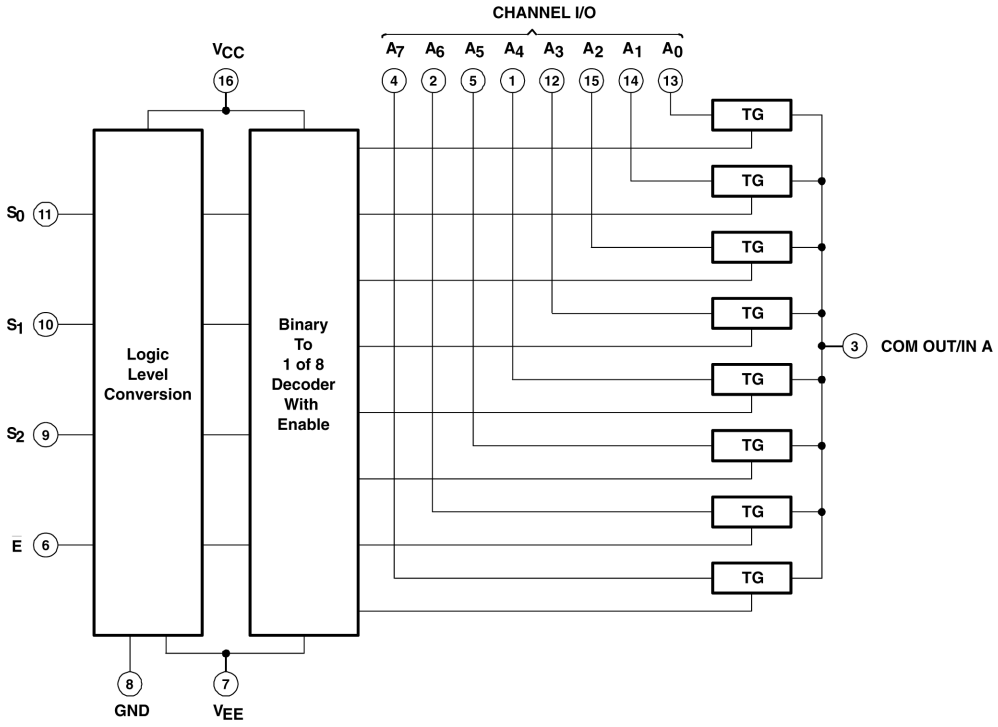
此器件是数字控制的模拟开关，其使用硅栅 CMOS 技术并借助标准 CMOS 集成电路的低功耗特性来实现与 LSTTL 接近的运行速度。

此模拟多路复用器/多路信号分离器可控制模拟电压，该电压可能会在整个电源电压范围内变化（例如，V_{CC} 变为 V_{EE}）。这些双向开关可将任何模拟输入用作输出，反之亦然。这些开关具有低导通电阻和低关断泄漏。此外，此器件具有使能控制 ($\overline{E}$)，当处于高电平时将禁用所有开关，将所有开关置于关断状态。

封装信息

器件型号	封装(1)	封装尺寸(2)
CD74HC4051-Q1	PW（TSSOP，16）	5mm × 6.4mm
	D（SOIC，16）	9.9mm × 3.9mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

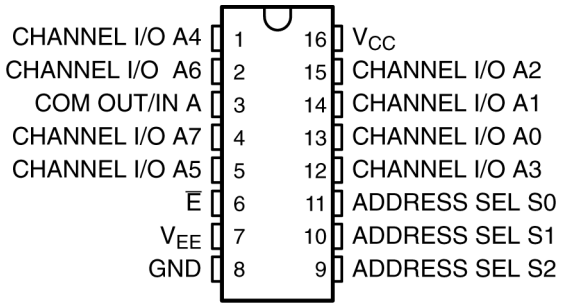


图 4-1. PW, D Package, 16-Pin TSSOP, SOIC (Top View)

表 4-1. Function Table

INPUTS				ON CHANNEL(S)
E	S_2	S_1	S_0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC} – V_{EE} (see (2))	Supply voltage range		−0.5	10.5	V
V_{CC}	Supply voltage range		−0.5	7	V
V_{EE}	Supply voltage range		+0.5	−7	V
I_{IK} (V_I < −0.5V or V_I > V_{CC} + 0.5V)	Input clamp current			±20	mA
I_{OK} (V_O < V_{EE} − 0.5V or V_O > V_{CC} + 0.5V)	Output clamp current			±20	mA
(V_I > V_{EE} − 0.5V or V_I < V_{CC} + 0.5V)	Switch current			±25	mA
	Continuous current through V_{CC} or GND			±50	mA
I_{EE}	V_{EE} current			−20	mA
$R_{\theta JA}$	Package thermal impedance	D package		91.6	°C/W
		PW package		116.5	°C/W
T_J	Maximum junction temperature			150	°C
Lead temperature (during soldering):		At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max		300	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to GND unless otherwise specified.

5.2 Recommended Operating Conditions

(see (1))

			MIN	MAX	UNIT
V_{CC}	Supply voltage (see (2))		2	6	V
	Supply voltage, V_{CC} – V_{EE} (see 图 5-1)		2	10	V
V_{EE}	Supply voltage, (see (2) and 图 5-2)		0	−6	V
V_{IH}	High-level input voltage	V_{CC} = 2V	1.5		V
		V_{CC} = 4.5V	3.15		
		V_{CC} = 6V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2V		0.5	V
		V_{CC} = 4.5V		1.35	
		V_{CC} = 6V		1.8	
V_I	Input control voltage		0	V_{CC}	V
V_{IS}	Analog switch I/O voltage		V_{EE}	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2V	0	1000	ns
		V_{CC} = 4.5V	0	500	
		V_{CC} = 6V	0	400	
T_A	Operating free-air temperature		−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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(2) In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from r_{on} values shown in electrical characteristics table). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

5.3 Recommended Operating Area as a Function of Supply Voltages

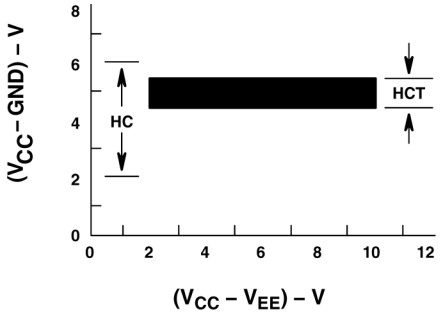


图 5-1. $(V_{CC} – V_{EE}) – V$

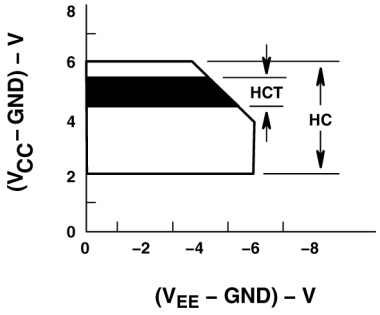


图 5-2. $(V_{EE} – GND) – V$

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{EE}	V_{CC}	T_A = 25 °C			T_A = –40 °C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
r_{on}	I_O = 1 mA, V_I = V_{IH} or V_{IL}, See 图 5-3	V_{IS} = V_{CC} or V_{EE}	0V	4.5V		70	160		240	Ω
			0V	6V		60	140		210	
			−4.5 V	4.5V		40	120		180	
		V_{IS} = V_{CC} to V_{EE}	0V	4.5V		90	180		270	
			0V	6V		80	160		240	
			−4.5 V	4.5V		45	130		195	
Δr_{on}	Between any two channels		0V	4.5V		10				Ω
			0V	6V		8.5				
			−4.5 V	4.5V		5				
I_{IZ}	For switch OFF: When V_{IS} = V_{CC}, V_{OS} = V_{EE}; When V_{IS} = V_{EE}, V_{OS} = V_{CC} For switch ON: All applicable combinations of V_{IS} and V_{OS} voltage levels, V_I = V_{IH} or V_{IL}		0V	6V			±0.2		±2	µA
			−5V	5V			±0.4		±4	
I_{IL}	V_I = V_{CC} or GND		0V	6V			±0.1		±1	µA
I_{CC}	I_O = 0, V_I = V_{CC} or GND	When V_{IS} = V_{EE}, V_{OS} = V_{CC}	0V	6V			12		160	µA
		When V_{IS} = V_{CC}, V_{OS} = V_{EE}	−5V	5V			32		320	

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5.5 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 图 6-5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{EE}	V_{CC}	T_A = 25°C			T_A = −40 °C TO 125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t_{pd}	IN	OUT	C_L = 15pF		5V		4				ns
			C_L = 50pF	0V	2V			60		90	ns
					4.5V			12		18	
					6V			10		15	
				−4.5 V	4.5V			8		12	
t_{en}	ADDRESS SEL or $\overline{E}$	OUT	C_L = 15pF		5V		19				ns
			C_L = 50pF	0V	2V			325		490	
					4.5V			45		68	
					6V			38		57	
				−4.5 V	4.5V			32		48	
t_{dis}	ADDRESS SEL or $\overline{E}$	OUT	C_L = 15pF		5V		27				ns
			C_L = 50pF	0V	2V			250		400	
					4.5V			50		68	
					6V			44		57	
				−4.5 V	4.5V			44		55	
C_I	Control		C_L = 50pF					10		10	pF

5.6 Operating Characteristics

V_{CC} = 5V, T_A = 25°C, Input t_r, t_f = 6 ns

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance (see (1))	50	pF

(1) C_{pd} is used to determine the dynamic power consumption, per package.

- $P_D = C_{pd} V_{CC}^2 f_I + \Sigma (C_L + C_S) V_{CC}^2 f_O$
- f_O = output frequency
- f_I = input frequency
- C_L = output load capacitance
- C_S = switch capacitance
- V_{CC} = supply voltage

5.7 Analog Channel Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{EE}	V_{CC}	MIN	TYP	MAX	UNIT
C_I	Switch input capacitance					5		pF
C_{COM}	Common output capacitance					25		pF
f_{max}	Minimum switch frequency response at −3 dB	See 图 6-1 and 图 5-4, and (1) and (2)	−2.25V	2.25V		145		MHz
			−4.5V	4.5V		180		

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5.7 Analog Channel Characteristics（续）

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{EE}	V_{CC}	MIN	TYP	MAX	UNIT
THD	Sine-wave distortion	See 图 6-2	−2.25V	2.25V		0.035		%
			−4.5V	4.5V		0.018		
O_{ISO}	Switch OFF signal feed through	See 图 6-4 and 图 5-5, and (2) and (3)	−2.25V	2.25V		−73		dB
			−4.5V	4.5V		−75		

(1) Adjust input voltage to obtain 0 dBm at V_{OS} for f_{IN} = 1MHz.
(2) V_{IS} is centered at (V_{CC} − V_{EE})/2.
(3) Adjust input for 0 dBm.

5.8 Typical Characteristics

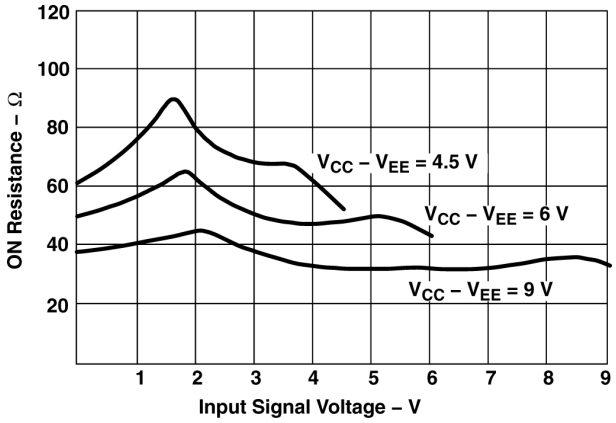


图 5-3. Typical on Resistance vs Input Signal Voltage

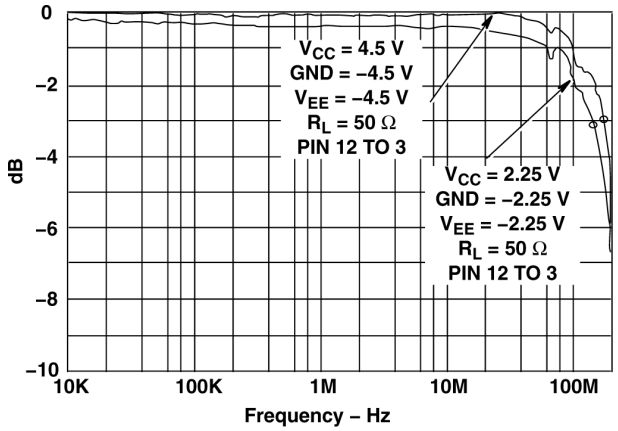


图 5-4. Channel on Bandwidth

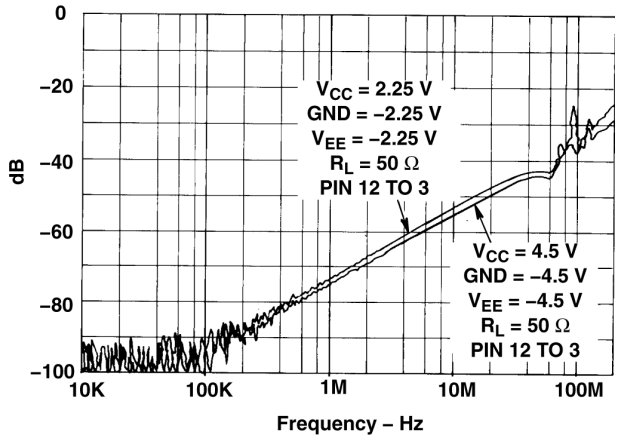


图 5-5. Channel off Feed-through

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6 Parameter Measurement Information

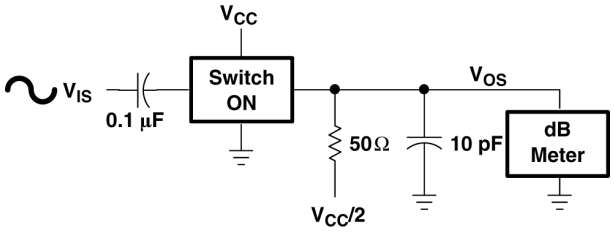


图 6-1. Frequency-Response Test Circuit

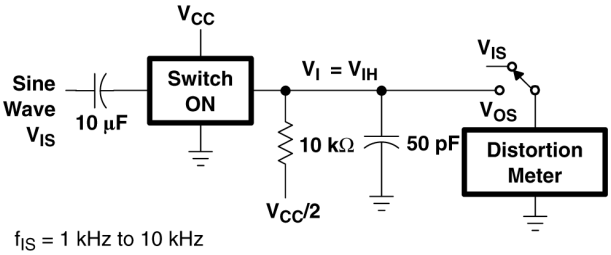


图 6-2. Sine-Wave Distortion Test Circuit

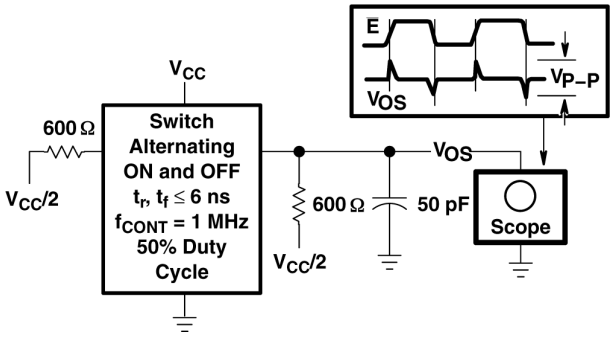


图 6-3. Control to Switch Feed-through Noise Test Circuit

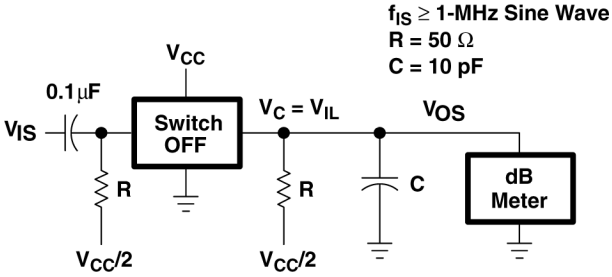
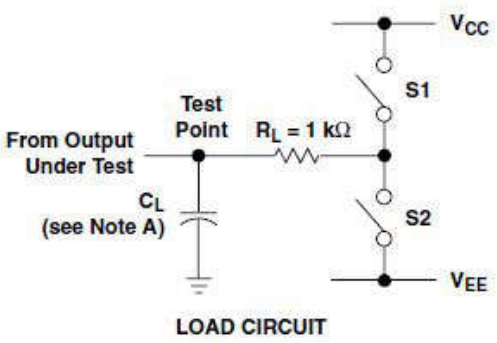
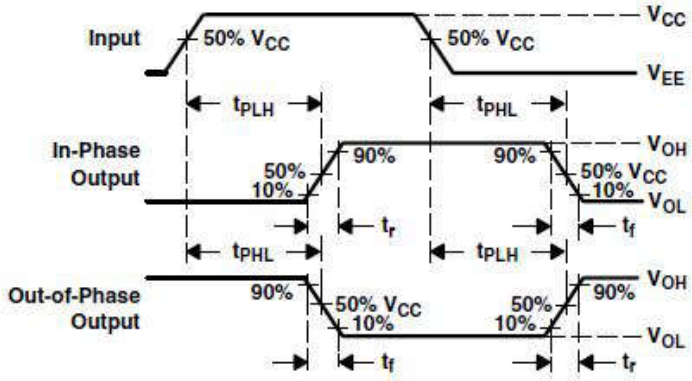


图 6-4. Switch off Signal Feed-through Test Circuit

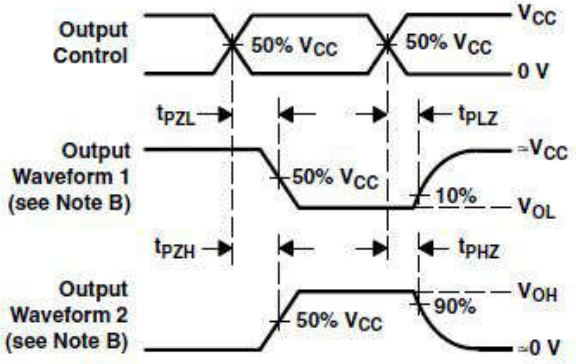


LOAD CIRCUIT

PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

图 6-5. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Functional Block Diagram

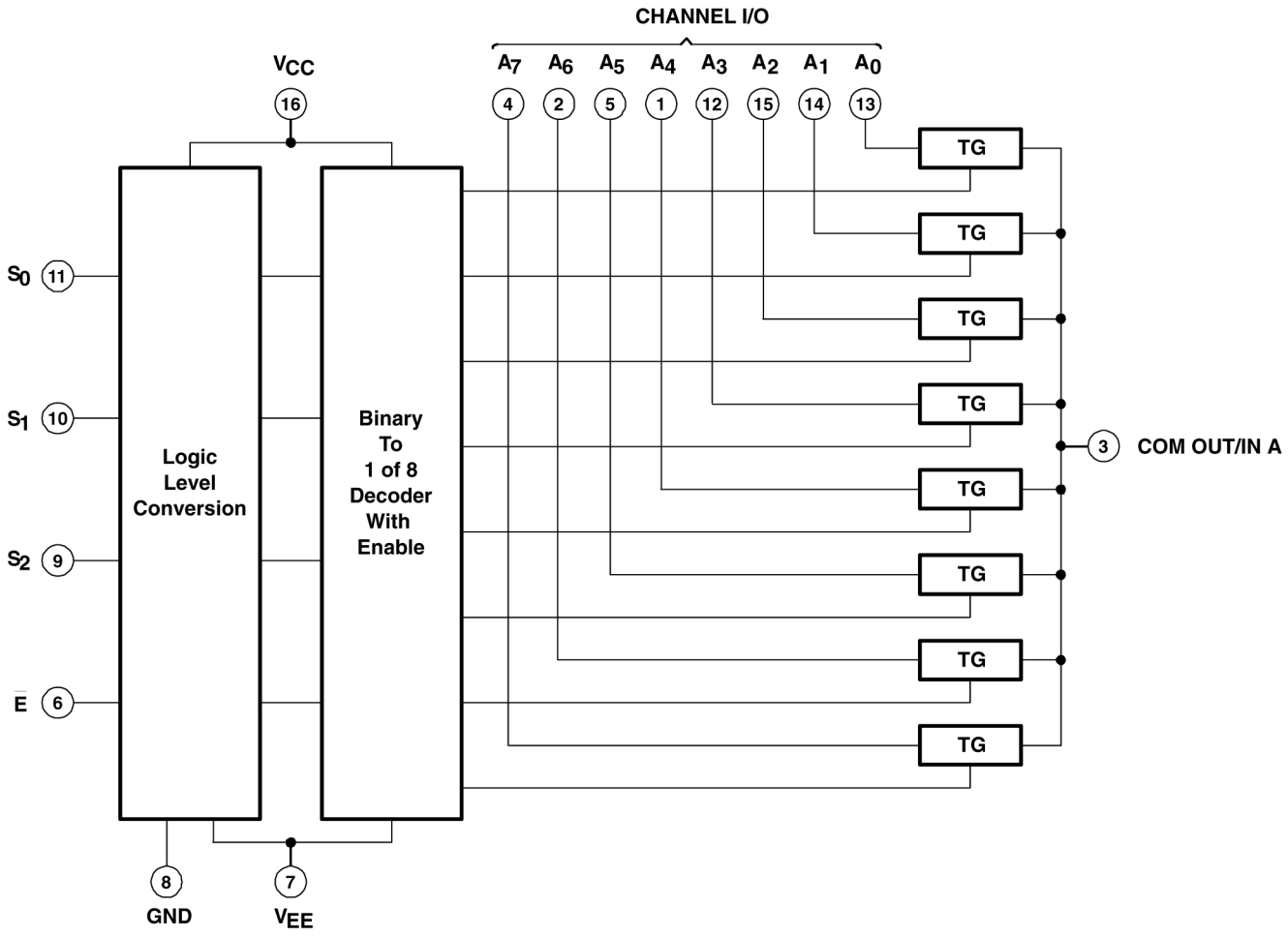


图 7-1. Logic Diagram (Positive Logic)

7.2 Device Functional Modes

表 7-1. Function Table

INPUTS				ON CHANNEL(S)
$\overline{E}$	S_2	S_1	S_0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (April 2008) to Revision B (April 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 将 M（SOIC，16）更改为 D（SOIC，16），以准确反映封装图	1
• Changed the package thermal impedance for the D package from: *73°C/W* to: *91.6°C/W*	3
• Changed the package thermal impedance for the PW package from: *108°C/W* to: *116.5°C/W*	3
• Changed I_{CC} MAX from: *8 μA* to: *12 μA* when V_{IS} = V_{EE}, V_{OS} = V_{CC} at a TA = 25°C	4
• Changed I_{CC} MAX from: *16 μA* to: *32 μA* when V_{IS} = V_{CC}, V_{OS} = V_{EE} at a TA = 25°C	4
• Changed t_{en} MAX from: *225ns* to: *325ns* when C_L = 50pF at a TA = 25°C and from: *340ns* to: *490ns* when C_L = 50pF at a TA = -40°C to 125°C	5
• Changed t_{dis} TYP from: *19ns* to: *27ns* when C_L = 15pF at a TA = 25°C	5
• Changed t_{dis} MAX from: *225ns* to: *250ns* when C_L = 50pF, V_{EE} = 0V, and V_{CC} = 2V at a TA = 25°C, and from: *340ns* to: *400ns* at a TA = -40°C to 125°C	5
• Changed t_{dis} MAX from: *45ns* to: *50ns* when C_L = 50pF, V_{EE} = 0V, and V_{CC} = 4.5V at a TA = 25°C	5
• Changed t_{dis} MAX from: *38ns* to: *44ns* when C_L = 50pF, V_{EE} = 0V, and V_{CC} = 6V at a TA = 25°C	5
• Changed t_{dis} MAX from: *32ns* to: *44ns* when C_L = 50pF, V_{EE} = -4.5V, and V_{CC} = 4.5V at a TA = 25°C, and from: *48ns* to: *55ns* at a TA = -40°C to 125°C	5
• Removed the TBD $\overline{E}$ or ADDRESS SEL to switch feed-through noise parameter	5

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC4051QM96G4Q1	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 125	HC4051Q
CD74HC4051QM96Q1	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4051Q
CD74HC4051QM96Q1.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4051Q
CD74HC4051QPWRG4Q1	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 125	HJ4051Q
CD74HC4051QPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HJ4051Q
CD74HC4051QPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ4051Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD74HC4051-Q1 :

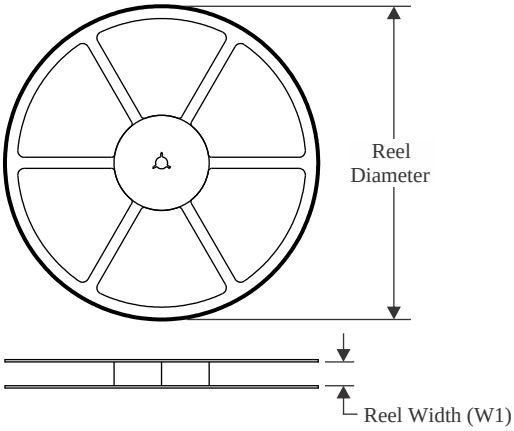
- Catalog : CD74HC4051
- Enhanced Product : CD74HC4051-EP
- Military : CD54HC4051

NOTE: Qualified Version Definitions:

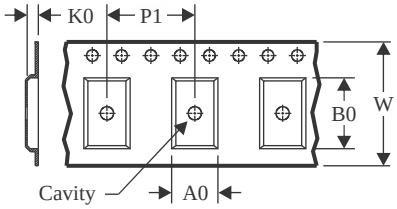
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

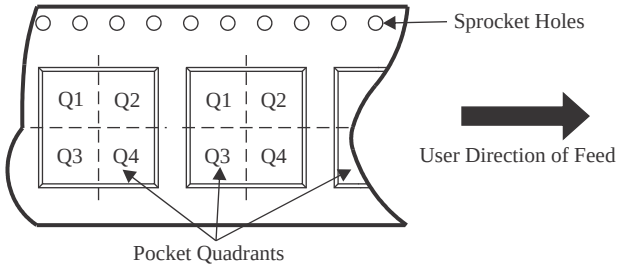


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

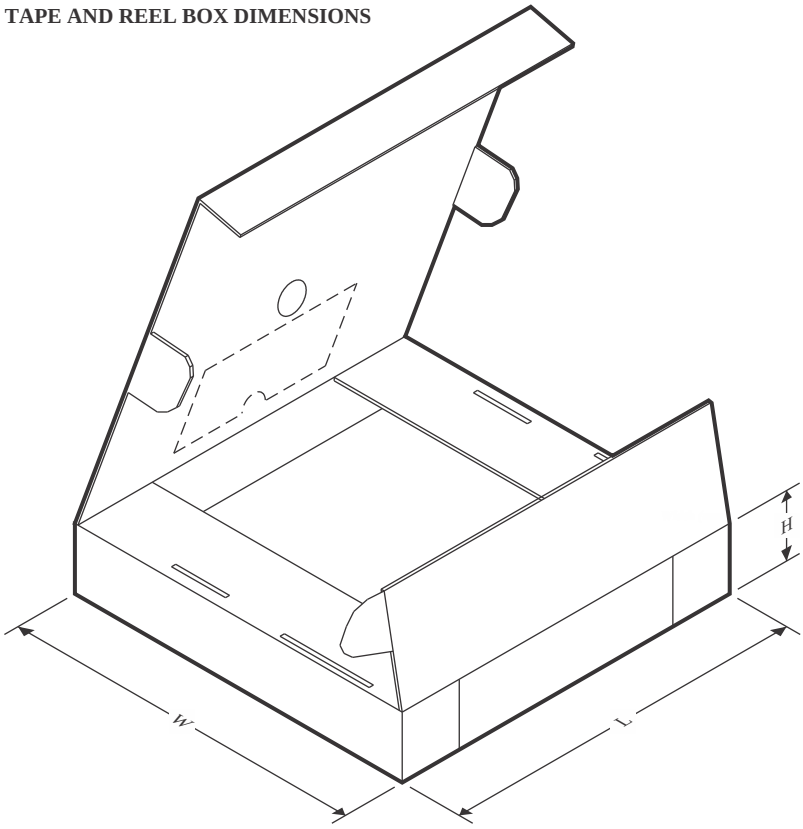
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

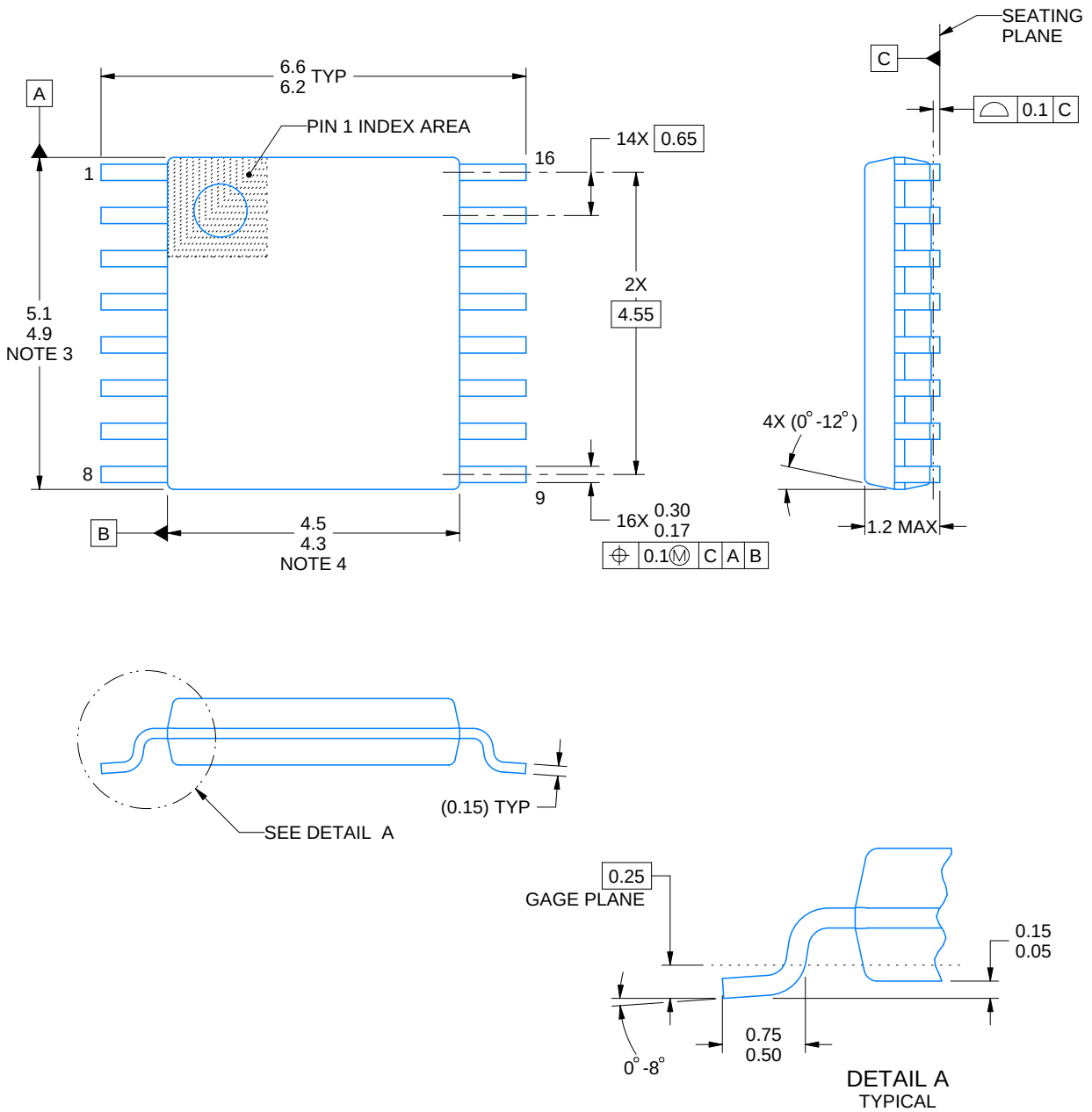
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

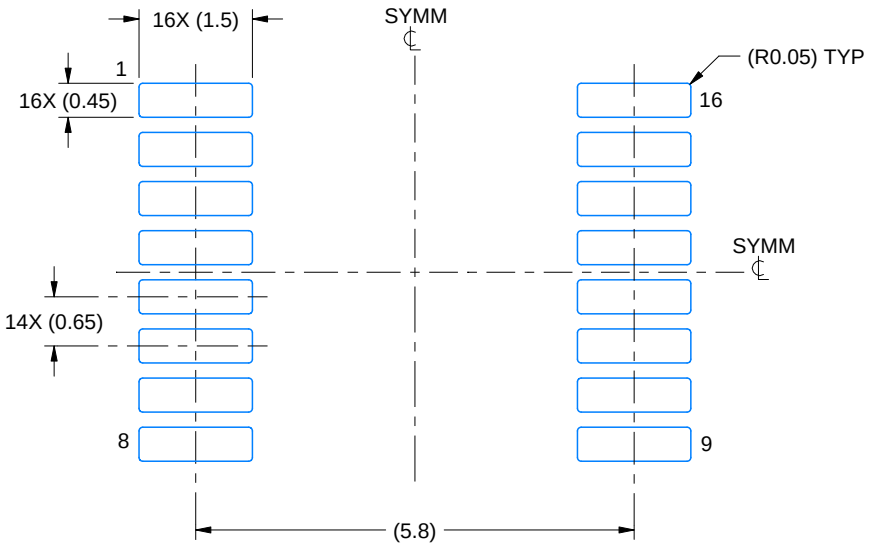
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

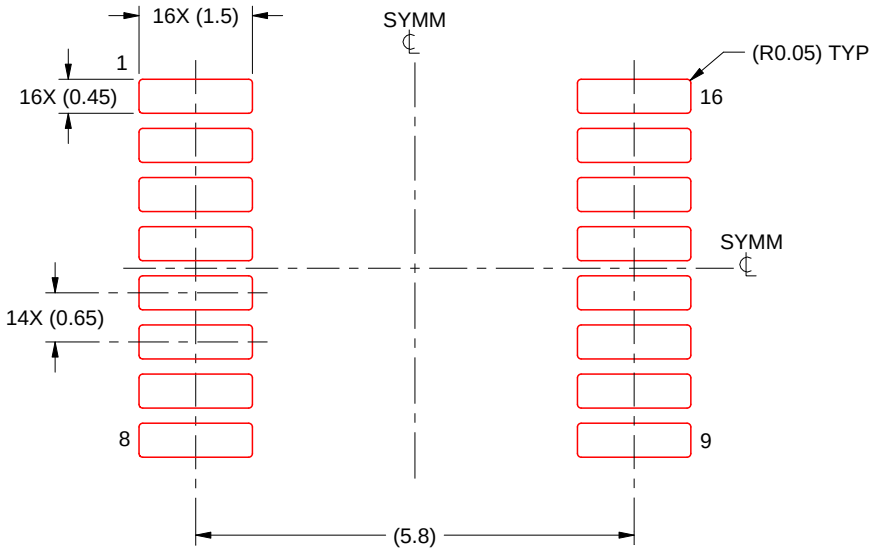


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



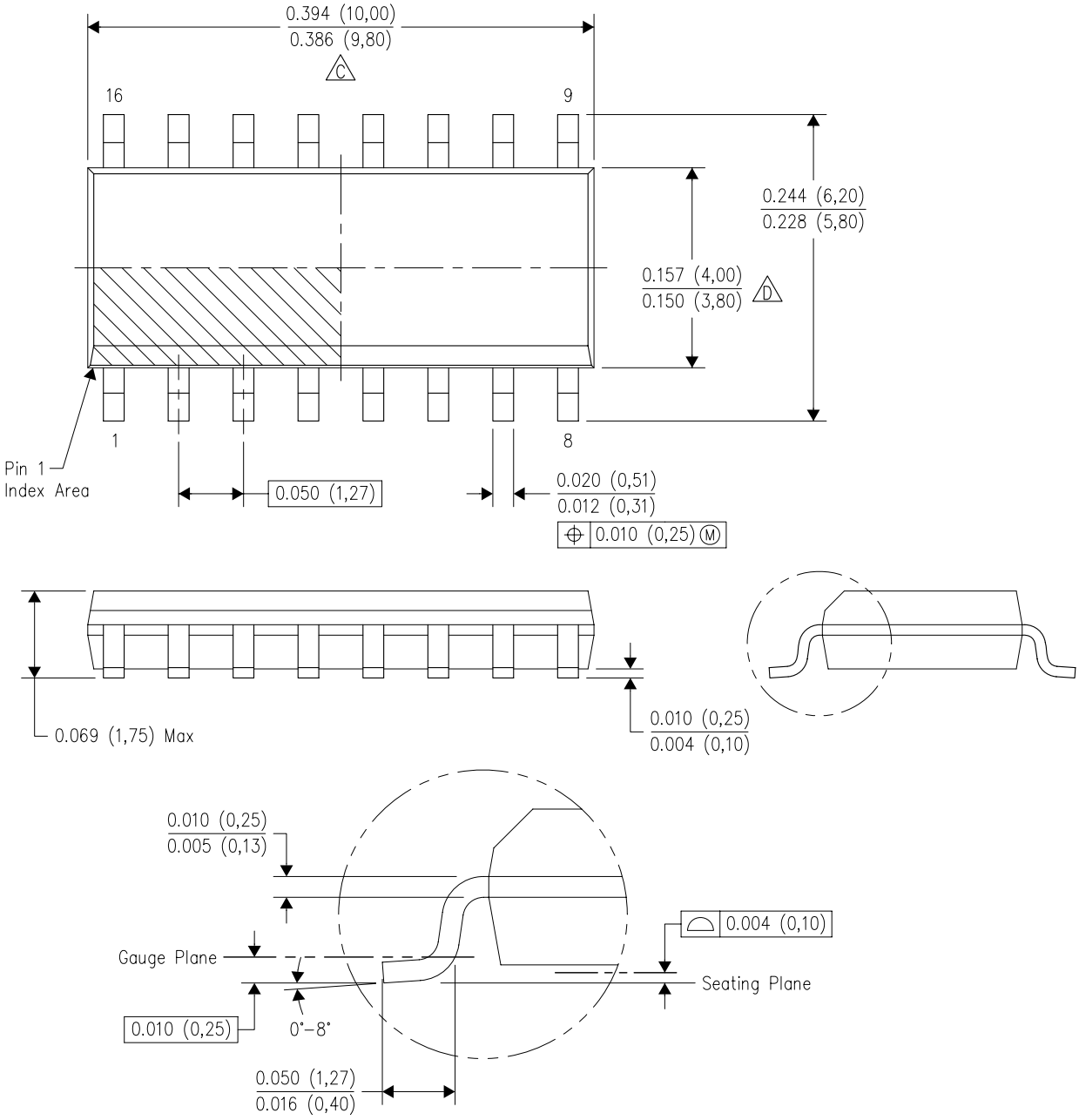
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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