

CDx4HC(T)166 高速 CMOS 逻辑 8 位并行输入/串行输出移位寄存器

1 特性

- 缓冲输入
- 扇出 (在温度范围内)
 - 标准输出: 10 个 LSTTL 负载
 - 总线驱动器输出: 15 个 LSTTL 负载
- 宽工作温度范围: -55°C 至 125°C
- 平衡的传播延迟时间及转换时间
- 与 LSTTL 逻辑 IC 相比, 功耗显著降低
- HC 类型
 - 2 V 至 6 V 工作电压
 - 高抗噪性: 当 $V_{CC} = 5\text{ V}$ 时, $N_{IL} = 30\%$, $N_{IH} = V_{CC}$ 的 30%
- HCT 类型
 - 4.5 V 至 5.5 V 工作电压
 - 直接 LSTTL 输入逻辑兼容性, $V_{IL} = 0.8\text{ V}$ (最大值), $V_{IH} = 2\text{ V}$ (最小值)

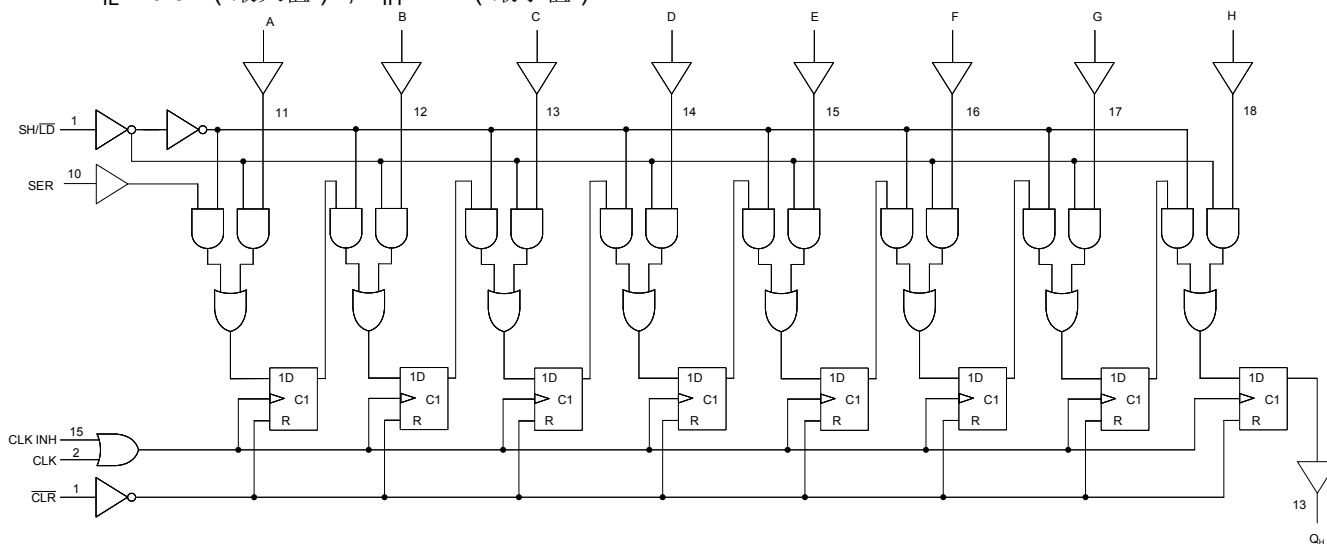
2 说明

HC166 和 HCT166 8 位移位寄存器采用硅栅 CMOS 技术制造。该器件具有标准 CMOS 集成电路的低功耗特性, 并可在与等效低功耗肖特基器件相当的速度下运行。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
CD54HC166F3A	CDIP (16)	24.38mm × 6.92mm
CD54HCT166F3A	CDIP (16)	24.38mm × 6.92mm
CD74HC166M	SOIC (16)	9.90mm × 3.90mm
CD74HCT166M	SOIC (16)	9.90mm × 3.90mm
CD74HC166E	PDIP (16)	19.31mm × 6.35mm
CD74HCT166E	PDIP (16)	19.31mm × 6.35mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



功能图



Table of Contents

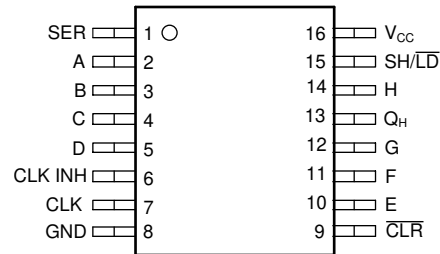
1 特性	1	7.2 Functional Block Diagram.....	11
2 说明	1	7.3 Device Functional Modes.....	12
3 Revision History	2	8 Power Supply Recommendations	13
4 Pin Configuration and Functions	3	9 Layout	13
5 Specifications	4	9.1 Layout Guidelines.....	13
5.1 Absolute Maximum Ratings ⁽¹⁾	4	10 Device and Documentation Support	14
5.2 Recommended Operating Conditions.....	4	10.1 接收文档更新通知.....	14
5.3 Thermal Information.....	4	10.2 支持资源.....	14
5.4 Electrical Characteristics.....	5	10.3 Trademarks.....	14
5.5 Prerequisite for Switching Characteristics.....	6	10.4 Electrostatic Discharge Caution.....	14
5.6 Switching Characteristics.....	8	10.5 术语表.....	14
6 Parameter Measurement Information	9	11 Mechanical, Packaging, and Orderable Information	14
7 Detailed Description	11		
7.1 Overview.....	11		

3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (October 2003) to Revision D (February 2022)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准.....	1

4 Pin Configuration and Functions



J, N, or D package
16-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		- 0.5	7	V
I _{IK}	Input diode current	For V _I < -0.5 V or V _I > V _{CC} + 0.5 V		±20	mA
I _{OK}	Output diode current	For V _O < -0.5 V or V _O > V _{CC} + 0.5 V		±20	mA
I _O	Drain current, per output	For -0.5 V < V _O < V _{CC} + 0.5 V		±25	mA
I _O	Output source or sink current per output pin	For V _O > -0.5 V or V _O < V _{CC} + 0.5 V		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C
	Lead temperature (Soldering 10s)(SOIC - lead tips only)			300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	V
V _I , V _O	Input or output voltage		0	V _{CC}	V
t _t	Input rise and fall time	2V		1000	ns
		4.5V		500	
		6V		400	
T _A	Temperature range		- 55	125	°C

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	UNIT
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	73	67	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽²⁾	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V _{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V _{IL}	Low level input voltage		2		0.5		0.5		0.5		V
			4.5		1.35		1.35		1.35		V
			6		1.8		1.8		1.8		V
V _{OH}	High level output voltage	I _{OH} = - 20 µA	2	1.9			1.9		1.9		V
		I _{OH} = - 20 µA	4.5	4.4			4.4		4.4		V
		I _{OH} = - 20 µA	6	5.9			5.9		5.9		V
	High level output voltage	I _{OH} = - 4 mA	4.5	3.98			3.84		3.7		V
		I _{OH} = - 5.2 mA	6	5.48			5.34		5.2		V
V _{OL}	Low level output voltage	I _{OL} = 20 µA	2		0.1		0.1		0.1		V
		I _{OL} = 20 µA	4.5		0.1		0.1		0.1		V
		I _{OL} = 20 µA	6		0.1		0.1		0.1		V
	Low level output voltage	I _{OL} = 4 mA	4.5		0.26		0.33		0.4		V
		I _{OL} = 5.2 mA	6		0.26		0.33		0.4		V
I _I	Input leakage current	V _I = V _{CC} or GND	6		±0.1		±1		±1		µA
I _{CC}	Supply current	V _I = V _{CC} or GND	6		8		80		160		µA
HCT TYPES											
V _{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V _{IL}	Low level input voltage		4.5 to 5.5		0.8		0.8		0.8		V
V _{OH}	High level output voltage	I _{OH} = - 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage	I _{OH} = - 4 mA	4.5	3.98			3.84		3.7		V
V _{OL}	Low level output voltage	I _{OL} = 20 µA	4.5		0.1		0.1		0.1		V
	Low level output voltage	I _{OL} = 4 mA	4.5		0.26		0.33		0.4		V
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1		±1		µA
I _{CC}	Supply current	V _I = V _{CC} or GND	5.5		8		80		160		µA

5.4 Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS ⁽²⁾	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC} ⁽¹⁾	Additional supply current per input pin	DS, D0-D7 inputs held at V _{CC} - 2.1 V	4.5 to 5.5		100	72		90		98	μA
		PE input held at V _{CC} - 2.1 V	4.5 to 5.5		100	126		157.5		171.5	
		CP, CE inputs held at V _{CC} - 2.1 V	4.5 to 5.5		100	180		225		245	
		MR inputs held at V _{CC} - 2.1 V	4.5 to 5.5		100	72		90		98	

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

(2) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Prerequisite for Switching Characteristics

See (Parameter Measurement Information)

PARAMETER		V _{CC} (V)	25°C		-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
f _{MAX}	Clock frequency	2	6		5		4		MHz
		4.5	30		25		20		MHz
		6	35		29		23		MHz
t _w	MR pulse width	2	100		125		150		ns
		4.5	20		25		30		ns
		6	17		21		26		ns
t _w	Clock pulse width	2	80		100		120		ns
		4.5	16		20		24		ns
		6	14		17		20		ns
t _{SU}	Set-up time Data and CE to clock	2	80		100		120		ns
		4.5	16		20		24		ns
		6	14		17		20		ns
t _H	Hold time data to clock	2	1		1		1		ns
		4.5	1		1		1		ns
		6	1		1		1		ns
t _{REM}	Removal time MR to clock	2	0		0		0		ns
		4.5	0		0		0		ns
		6	0		0		0		ns
t _{SU}	Set-up time PE to CP	2	145		180		220		ns
		4.5	29		36		44		ns
		6	25		31		38		ns
t _H	Hold time PE to CP or CE	2	0		0		0		ns
		4.5	0		0		0		ns
		6	0		0		0		ns
HCT TYPES									
f _{MAX}	Clock frequency	4.5	25		20		16		MHz
t _w	MR pulse width	4.5	35		44		53		ns
t _w	Clock pulse width	4.5	20		25		30		ns

See ([Parameter Measurement Information](#))

PARAMETER		V _{CC} (V)	25°C		-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{SU}	Set-up time data and $\overline{CE}$ to clock	4.5	16		20		24		ns
t _H	Hold time data to clock	4.5	0		0		0		ns
t _{REM}	Removal time $\overline{MR}$ to clock	4.5	0		0		0		ns
t _{SU}	Set-up time $\overline{PE}$ to CP	4.5	30		38		45		ns
t _H	Hold time $\overline{PE}$ to CP or $\overline{CE}$	4.5	0		0		0		ns

5.6 Switching Characteristics

Input t_r , t_f = 6 ns. Unless otherwise specified, C_L = 50pF. See (Parameter Measurement Information)

(1) C_{PD} is used to determine the dynamic power consumption, per gate.

(2) $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

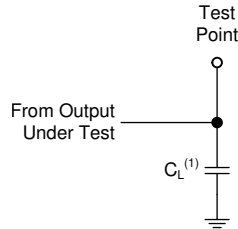
(3) C_L = 15 and V_{CC} = 5 V.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_f < 6 \text{ ns}$.

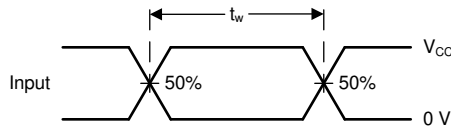
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

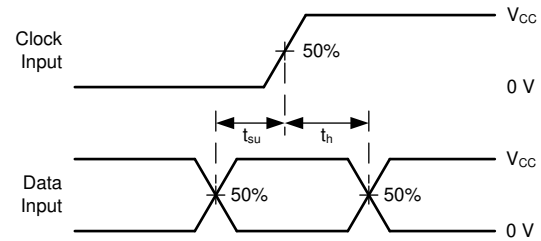


(1) C_L includes probe and test-fixture capacitance.

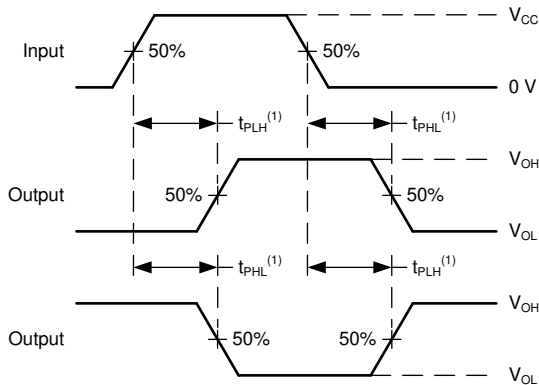
图 6-1. Load Circuit for Push-Pull Outputs



**图 6-2. Voltage Waveforms, Standard CMOS Inputs
Pulse Duration**

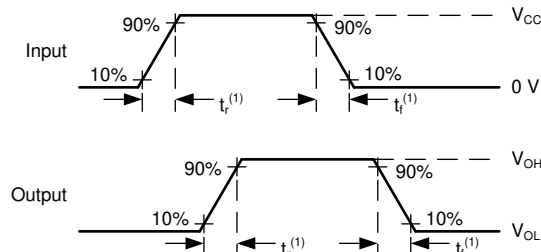


**图 6-3. Voltage Waveforms, Standard CMOS Inputs
Setup and Hold Times**



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

**图 6-4. Voltage Waveforms, Standard CMOS Inputs
Setup Propagation Delays**



(1) The greater between t_r and t_f is the same as t_t .

**图 6-5. Voltage Waveforms, Input and Output
Transition Times for Standard CMOS Input Devices**

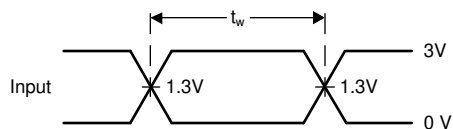


图 6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

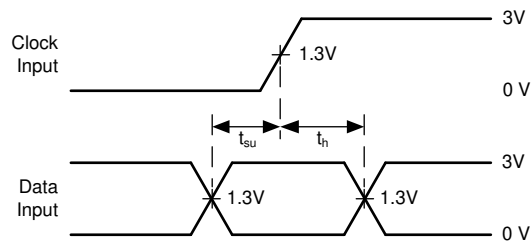
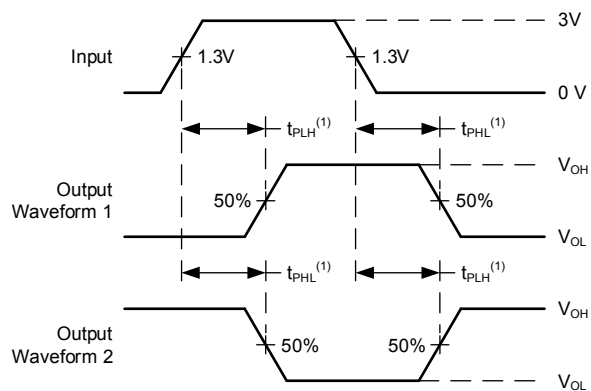


图 6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

图 6-8. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays

7 Detailed Description

7.1 Overview

The 'HC166 and 'HCT166 8-bit shift register is fabricated with silicon gate CMOS technology. It possesses the low power consumption of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device.

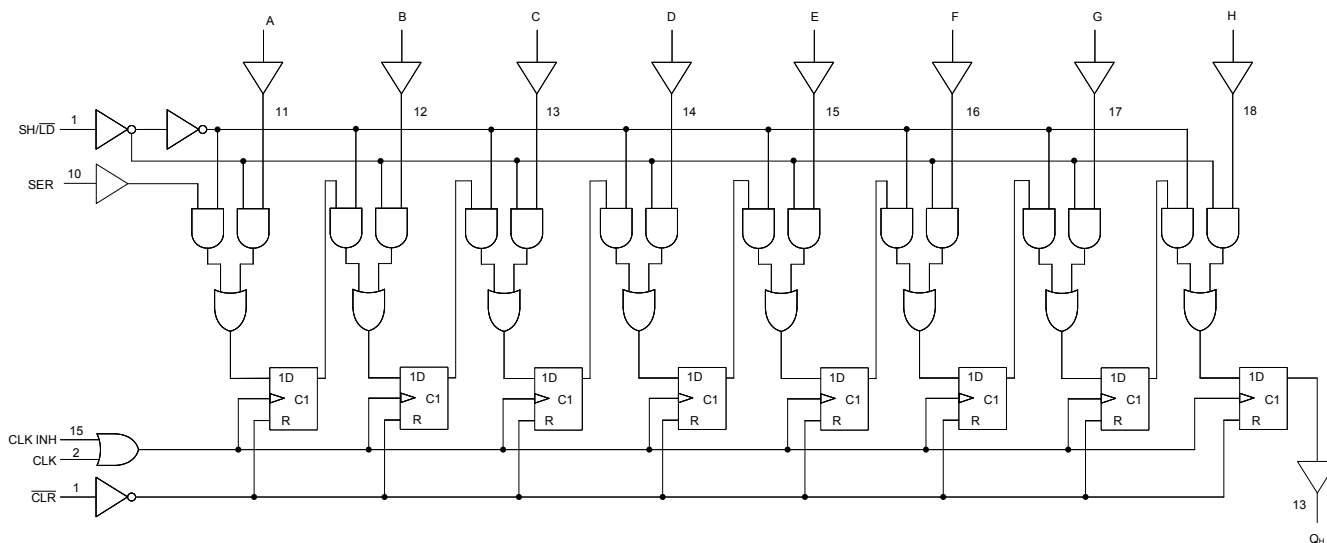
The 'HCT166 is functionally and pin compatible with the standard 'LS166.

The 166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into the internal bit position Q0 from Serial Data Input (DS), and the remaining bits are shifted one place to the right (Q0 → Q1 → Q2, etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q7 output is connected to the DS input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation.

A LOW on the Controller Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Truth Table⁽¹⁾

INPUTS						INTERNAL Q STATES		OUTPUT Q7
MASTER RESET	PARALLEL ENABLE	CLOCK ENABLE	CLOCK	SERIAL	PARALLEL D0 D7	Q0	Q1	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q00	Q10	Q0
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q0n	Q6n
H	H	L	↑	L	X	L	Q0n	Q6n
H	X	H	↑	X	X	Q00	Q10	Q70

- (1) H = High Voltage Level,
 L = Low Voltage Level,
 X = Don't Care,
 ↑ = Transition from Low to High Level,
 a...h = The level of steady-state input at inputs D0 thru D7, respectively,
 Q00, Q10, Q70 = The level of Q0, Q1, or Q7, respectively, before the indicated steady-state input conditions were established
 Q0n, Q6n = The level of Q0 or Q6, respectively, before the most recent ↑ transition of the clock.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

TI 提供技术和可靠性数据 (包括数据表)、设计资源 (包括参考设计)、应用或其他设计建议、网络工具、安全信息和其他资源, 不保证没有瑕疵且不做任何明示或暗示的担保, 包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任: (1) 针对您的应用选择合适的 TI 产品, (2) 设计、验证并测试您的应用, (3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更, 恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务, TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com/legal/termsofsale.html>) 或 [ti.com](https://www.ti.com) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2021, 德州仪器 (TI) 公司

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54HC166F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC166F3A
CD54HC166F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC166F3A
CD54HCT166F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT166F3A
CD54HCT166F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT166F3A
CD74HC166E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC166E
CD74HC166E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC166E
CD74HC166M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC166M
CD74HC166M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC166M
CD74HC166M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC166M
CD74HCT166E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT166E
CD74HCT166E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT166E
CD74HCT166EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT166E
CD74HCT166M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT166M
CD74HCT166M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HCT166M
CD74HCT166M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT166M
CD74HCT166M96G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT166M
CD74HCT166M96G4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT166M
CD74HCT166MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT166M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC166, CD54HCT166, CD74HC166, CD74HCT166 :

- Catalog : [CD74HC166](#), [CD74HCT166](#)
- Military : [CD54HC166](#), [CD54HCT166](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC166M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT166M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT166M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC166M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT166M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT166M96G4	SOIC	D	16	2500	353.0	353.0	32.0

TUBE

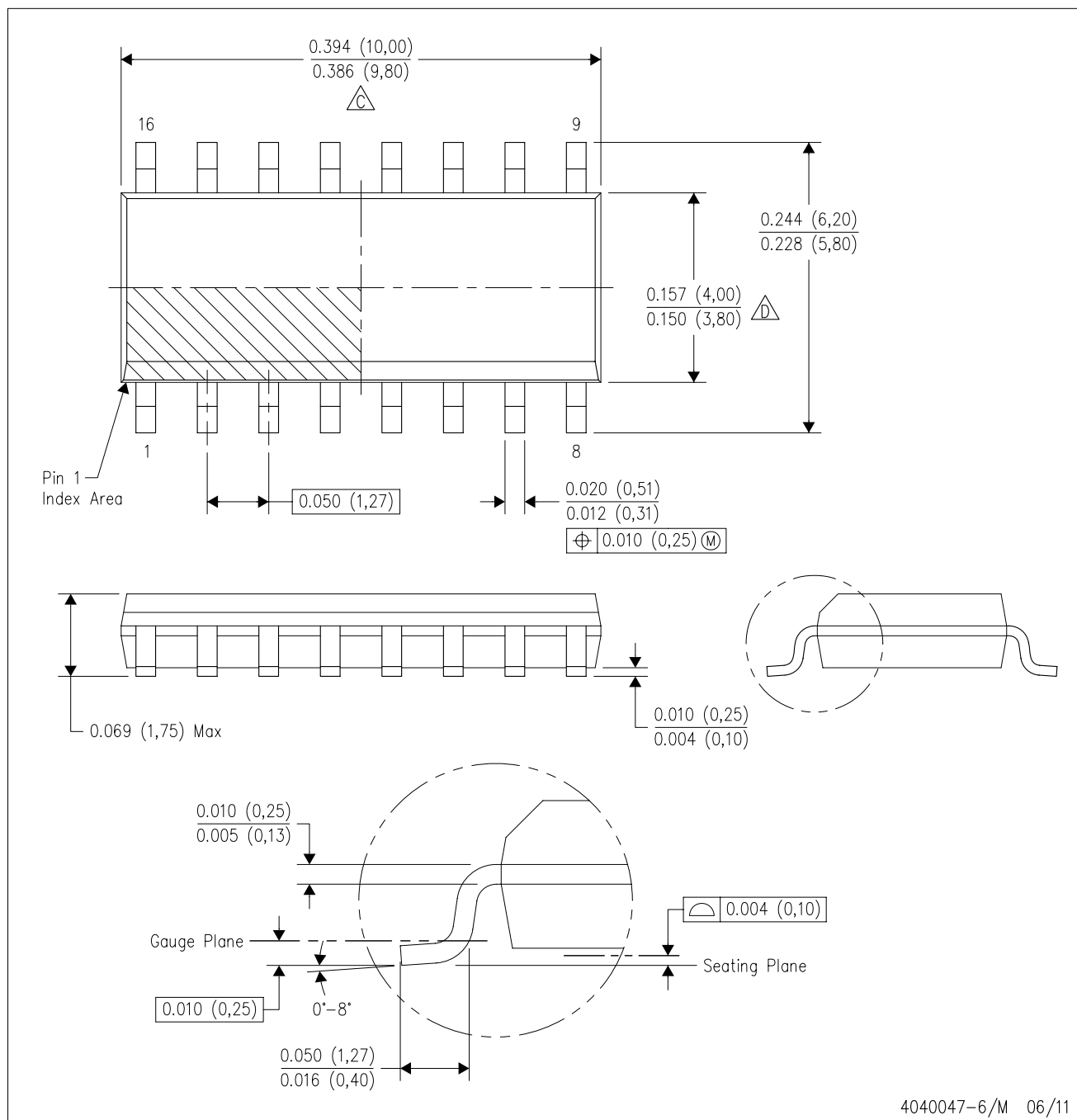


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC166E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC166E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC166E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC166E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT166E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT166E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT166E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT166E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT166EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT166EE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



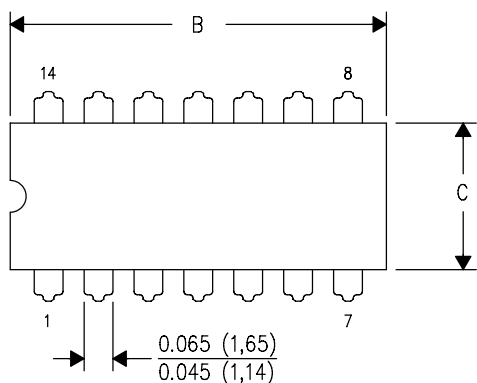
4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

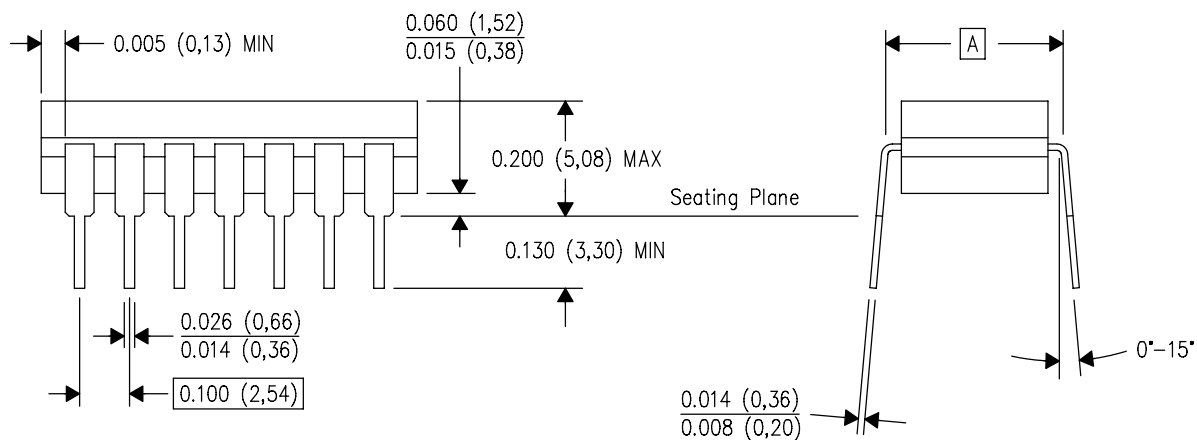
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月