

High-Speed CMOS Logic 4- to 16-Line Decoder/Demultiplexer

Features

- Two Enable Inputs to Facilitate Demultiplexing and Cascading Functions
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC154 and 'HCT154 are 4- to 16-line decoders/demultiplexers with two enable inputs, E1 and E2.

A High on either enable input forces the output into the High state. The demultiplexing function is performed by using the four input lines, A0 to A3, to select the output lines \bar{Y}_0 to \bar{Y}_{15} , and using one enable as the data input while holding the other enable low.

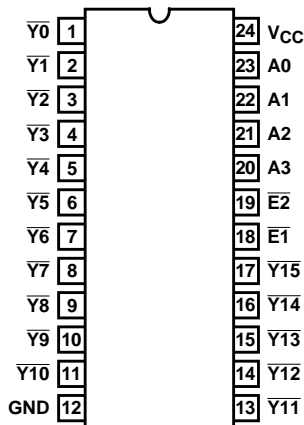
Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|---------------|------------------|--------------|
| CD54HC154F3A | -55 to 125 | 24 Ld CERDIP |
| CD54HCT154F3A | -55 to 125 | 24 Ld CERDIP |
| CD74HC154E | -55 to 125 | 24 Ld PDIP |
| CD74HC154EN | -55 to 125 | 24 Ld PDIP |
| CD74HC154M | -55 to 125 | 24 Ld SOIC |
| CD74HC154M96 | -55 to 125 | 24 Ld SOIC |
| CD74HCT154E | -55 to 125 | 24 Ld PDIP |
| CD74HCT154EN | -55 to 125 | 24 Ld PDIP |
| CD74HCT154M | -55 to 125 | 24 Ld SOIC |
| CD74HCT154M96 | -55 to 125 | 24 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

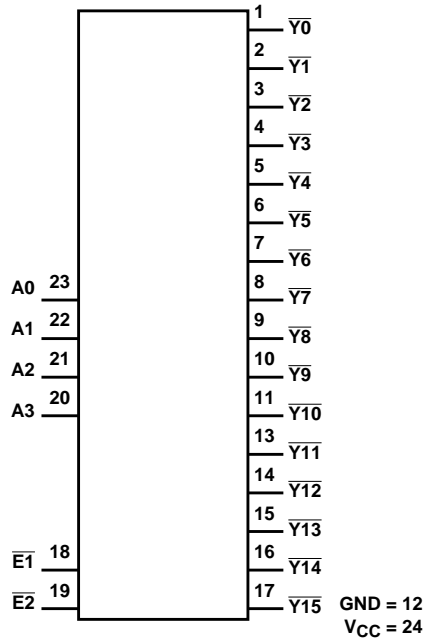
Pinout

CD54HC154, CD54HCT154
(CERDIP)
CD74HC154, CD74HCT154
(PDIP, SOIC)
TOP VIEW



CD54HC154, CD74HC154, CD54HCT154, CD74HCT154

Functional Diagram



TRUTH TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | | | | | | | | | | |
|-----------------|-----------------|----|----|----|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|---|
| $\overline{E1}$ | $\overline{E2}$ | A3 | A2 | A1 | A0 | $\overline{Y0}$ | $\overline{Y1}$ | $\overline{Y2}$ | $\overline{Y3}$ | $\overline{Y4}$ | $\overline{Y5}$ | $\overline{Y6}$ | $\overline{Y7}$ | $\overline{Y8}$ | $\overline{Y9}$ | $\overline{Y10}$ | $\overline{Y11}$ | $\overline{Y12}$ | $\overline{Y13}$ | $\overline{Y14}$ | $\overline{Y15}$ | |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

CD54HC154, CD74HC154, CD54HCT154, CD74HCT154

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} | $\pm 50mA$ |

Thermal Information

| | |
|--|------------------------------------|
| Thermal Resistance (Typical) | θ_{JA} ($^{\circ}C/W$) |
| E (PDIP) Package (.600) (Note 1) | 67 |
| EN (PDIP) Package (.300) (Note 1) | 67 |
| M (SOIC) Package (Note 2) | 46 |
| Maximum Junction Temperature | 150 $^{\circ}C$ |
| Maximum Storage Temperature Range | -65 $^{\circ}C$ to 150 $^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | 300 $^{\circ}C$ |
| (SOIC - Lead Tips Only) | |

Operating Conditions

| | |
|---|------------------------------------|
| Temperature Range (T_A) | -55 $^{\circ}C$ to 125 $^{\circ}C$ |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I , V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25 $^{\circ}C$ | | | -40 $^{\circ}C$ TO 85 $^{\circ}C$ | | -55 $^{\circ}C$ TO 125 $^{\circ}C$ | | UNITS |
|---|----------|----------------------|------------|--------------|----------------|-----|-----------|-----------------------------------|---------|------------------------------------|---------|---------|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA |
| Quiescent Device Current | I_{CC} | V_{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA |

CD54HC154, CD74HC154, CD54HCT154, CD74HCT154

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} and GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI _{CC} (Note 3) | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|---------------------------------|------------|
| A0 - A3 | 1.4 |
| E ₁ , E ₂ | 1.3 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Switching Specifications Input t_p, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|-------------------------------------|-----------------------|-----------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| Propagation Delay (Figure 1) Address to Output | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 175 | - | 220 | - | 265 | ns |
| | | | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | C _L = 15pF | 5 | - | 14 | - | - | - | - | - | ns |
| | | | C _L = 50pF | 6 | - | - | 30 | - | 37 | - | 45 |

CD54HC154, CD74HC154, CD54HCT154, CD74HCT154

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|--------------------|---------------------|--------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $\overline{E1}$ to Output | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | - | 175 | - | 220 | - | 265 | ns |
| | | | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 14 | - | - | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | - | 30 | - | 37 | - | 45 | ns |
| $\overline{E2}$ to Output | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | - | 175 | - | 220 | - | 265 | ns |
| | | | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 14 | - | - | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | - | 30 | - | 37 | - | 45 | ns |
| Output Transition Time (Figure 1) | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | C_{IN} | - | - | - | 10 | - | 10 | - | 10 | pF | |
| Power Dissipation Capacitance (Notes 4, 5) | C_{PD} | - | 5 | - | 88 | - | - | - | - | pF | |

HCT TYPES

| | | | | | | | | | | | |
|---|--------------------|---------------------|-----|---|----|----|----|----|----|----|----|
| Propagation Delay (Figure 2) Address to Output | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 14 | - | - | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 4.5 | - | - | 34 | - | 43 | - | 51 | ns |
| $\overline{E1}$ to Output | t_{PLH}, t_{PHL} | $C_L = 15\text{pF}$ | 5 | - | 14 | - | - | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 4.5 | - | - | 34 | - | 43 | - | 51 | ns |
| $\overline{E2}$ to Output | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 34 | - | 43 | - | 51 | ns |
| | | $C_L = 15\text{pF}$ | 5 | - | 14 | - | - | - | - | - | ns |
| Output Transition Time | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Input Capacitance | C_{IN} | - | - | - | 10 | - | 10 | - | 10 | pF | |
| Power Dissipation Capacitance (Notes 4, 5) | C_{PD} | - | 5 | - | 84 | - | - | - | - | pF | |

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms

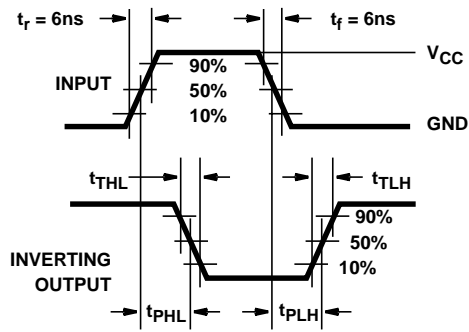


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

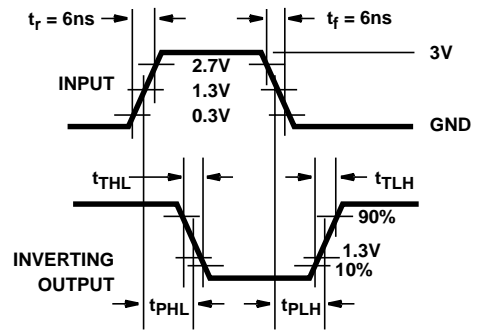


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------------|
| 5962-8670101JA | Active | Production | CDIP (J) 24 | 15 TUBE | No | Call TI | N/A for Pkg Type | -55 to 125 | 5962-8670101JA CD54HCT154F3A |
| 5962-8682201JA | Active | Production | CDIP (J) 24 | 15 TUBE | No | Call TI | N/A for Pkg Type | -55 to 125 | 5962-8682201JA CD54HC154F3A |
| CD54HC154F3A | Active | Production | CDIP (J) 24 | 15 TUBE | No | Call TI | N/A for Pkg Type | -55 to 125 | 5962-8682201JA CD54HC154F3A |
| CD54HC154F3A.A | Active | Production | CDIP (J) 24 | 15 TUBE | No | Call TI | N/A for Pkg Type | -55 to 125 | 5962-8682201JA CD54HC154F3A |
| CD54HCT154F3A | Active | Production | CDIP (J) 24 | 15 TUBE | No | Call TI | N/A for Pkg Type | -55 to 125 | 5962-8670101JA CD54HCT154F3A |
| CD54HCT154F3A.A | Active | Production | CDIP (J) 24 | 15 TUBE | No | Call TI | N/A for Pkg Type | -55 to 125 | 5962-8670101JA CD54HCT154F3A |
| CD74HC154M | Obsolete | Production | SOIC (DW) 24 | - | - | Call TI | Call TI | -55 to 125 | HC154M |
| CD74HC154M96 | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -55 to 125 | HC154M |
| CD74HC154M96.A | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC154M |
| CD74HC154M96E4 | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC154M |
| CD74HC154M96G4 | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC154M |
| CD74HC154M96G4.A | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC154M |
| CD74HCT154M | Obsolete | Production | SOIC (DW) 24 | - | - | Call TI | Call TI | -55 to 125 | HCT154M |
| CD74HCT154M96 | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT154M |
| CD74HCT154M96.A | Active | Production | SOIC (DW) 24 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT154M |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54HC154, CD54HCT154, CD74HC154, CD74HCT154 :

- Catalog : [CD74HC154](#), [CD74HCT154](#)
- Military : [CD54HC154](#), [CD54HCT154](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC154M96 | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74HC154M96G4 | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74HCT154M96 | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

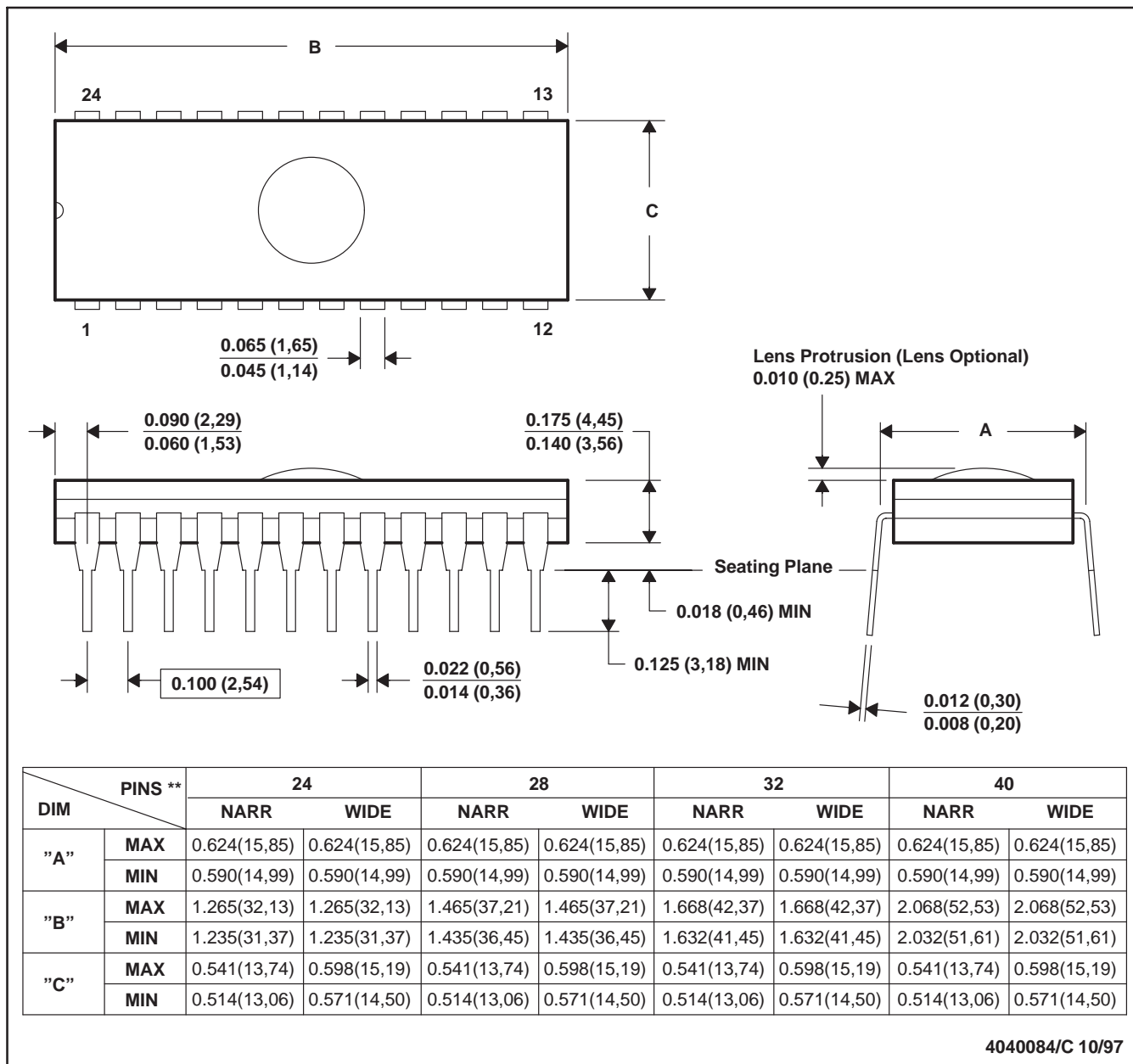

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC154M96 | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| CD74HC154M96G4 | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| CD74HCT154M96 | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
 D. This package can be hermetically sealed with a ceramic lid using glass frit.
 E. Index point is provided on cap for terminal identification.

DW (R-PDSO-G24)

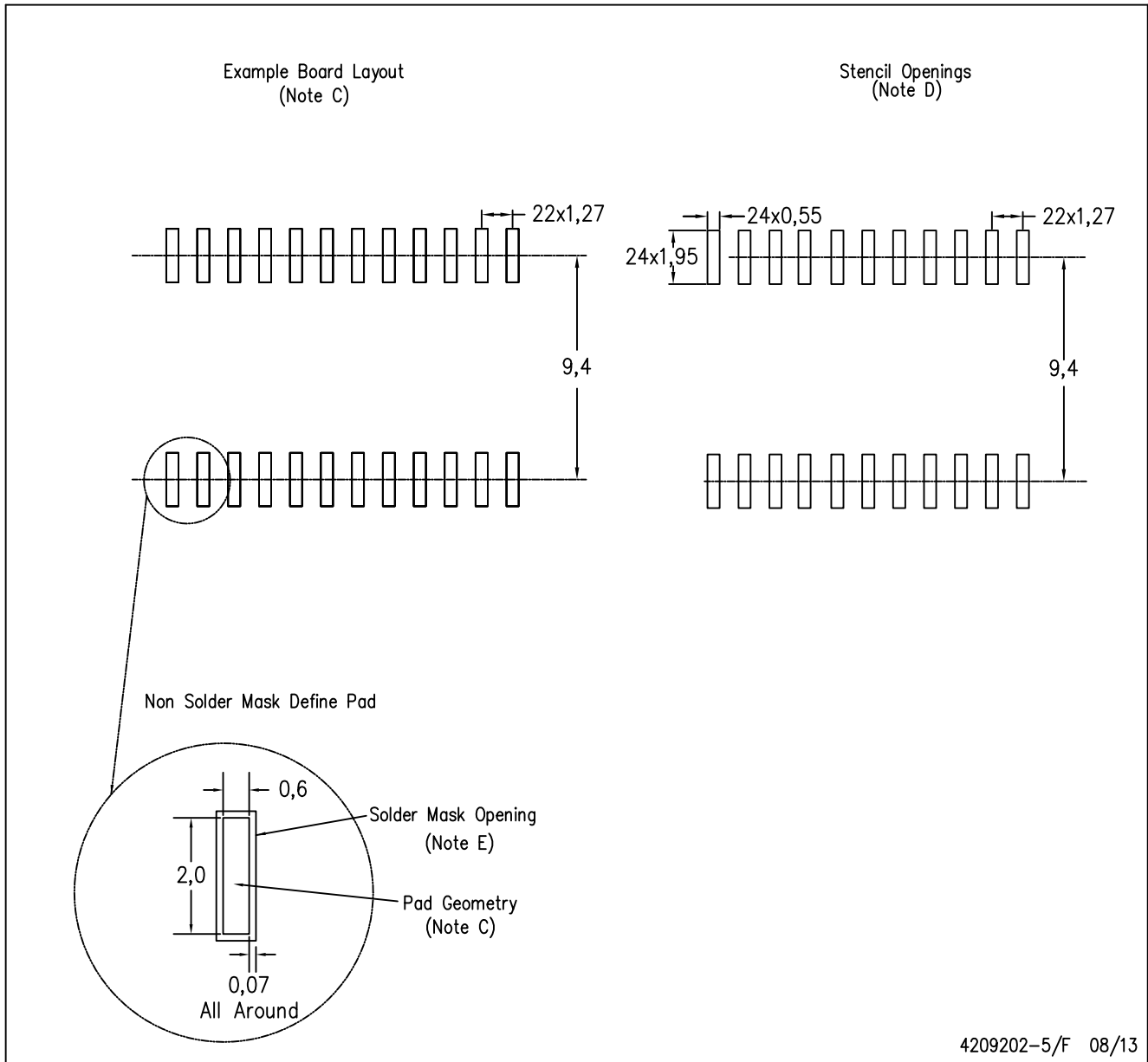
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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