

CDx4HC151、CDx4HCT151 高速 CMOS 逻辑 8 输入多路复用器

1 特性

- 互补数据输出
- 缓冲输入和输出
- 扇出 (在温度范围内)
 - 标准输出: 10 个 LSTTL 负载
 - 总线驱动器输出: 15 个 LSTTL 负载
- 宽工作温度范围: -55°C 至 125°C
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比, 可显著降低功耗
- 备选制造商为 Philips/Sigmetics
- HC 类型
 - 工作电压为 2 V 至 6 V
 - 高抗噪性: 当 $V_{CC} = 5 V$ 时, $N_{IL} = 30\%$, $N_{IH} = V_{CC}$ 的 30%
- HCT 类型
 - 4.5 V 至 5.5 V 工作电压
 - 直接 LSTTL 输入逻辑兼容性, $V_{IL} = 0.8 V$ (最大值), $V_{IH} = 2 V$ (最小值)
 - CMOS 输入兼容性, 当电压为 V_{OL} 、 V_{OH} 时, $I_i \leq 1 \mu A$

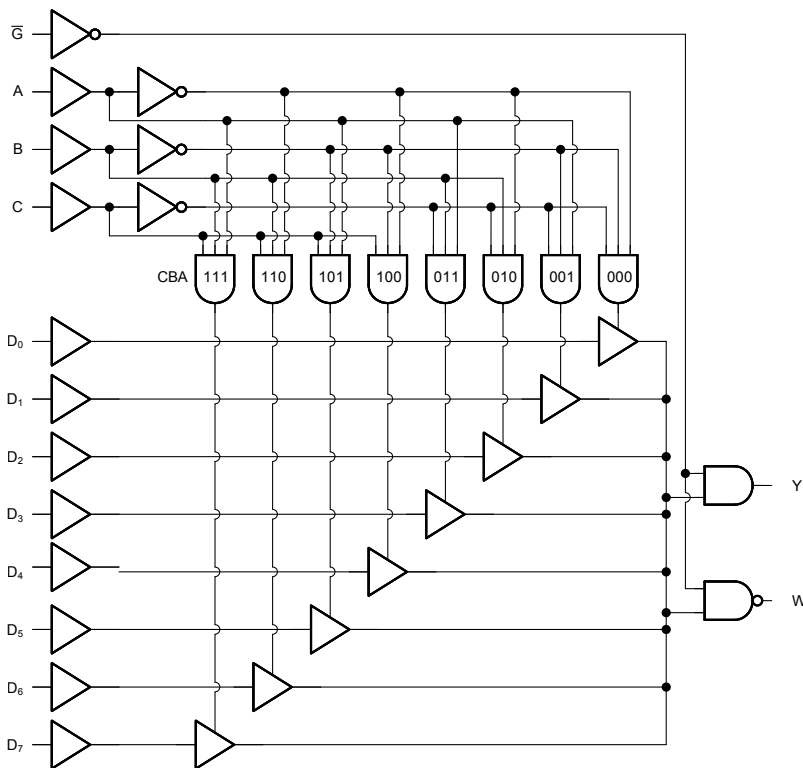
2 说明

'HC151 和 'HCT151 是单路 8 通道数字多路复用器, 具有 A、B、C 三个二进制控制输入和一个低电平有效使能 ($\bar{G}$) 输入。三个二进制信号从 8 个通道中选择 1 个。输出既有反相 (W) 也有同相 (Y)。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
CD74HC151M	SOIC (16)	9.90mm × 3.90mm
CD74HC151E	PDIP (16)	19.31mm × 6.35mm
CD54HC151F3A	陶瓷双列直插封装 (CDIP) (16)	24.38mm × 6.92mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



功能图



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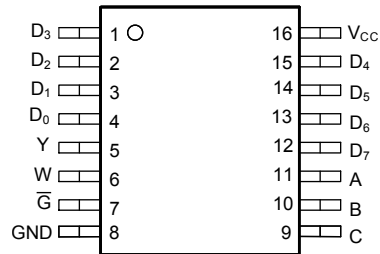
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3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (October 2003) to Revision D (November 2021)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准.....	1
• 更新了引脚名称，以符合现行的 TI 命名约定 I ₃ 现在是 D ₃ ，I ₂ 现在是 D ₂ ，I ₁ 现在是 D ₁ ，I ₀ 现在是 D ₀ ， $\bar{Y}$ 现在是 W， $\bar{E}$ 现在是 $\bar{G}$ ，S ₂ 现在是 C，S ₁ 现在是 B，S ₀ 现在是 A，I ₇ 现在是 D ₇ ，I ₆ 现在是 D ₆ ，I ₅ 现在是 D ₅ ，I ₄ 现在是 D ₄	1

4 Pin Configuration and Functions



J, N, or D package
16-Pin CDIP, PDIP, SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
I _{IK}	Input diode current	(V _I < -0.5 V or V _I > V _{CC} + 0.5 V)		±20	mA
I _{OK}	Output diode current	(V _O < -0.5 V or V _O > V _{CC} + 0.5 V)		±20	mA
I _O	Continuous output current	(V _O > -0.5 V or V _O < V _{CC} + 0.5 V)		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C
	Lead Temperature (Soldering 10s)			300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
T _A	Temperature Range		- 55	125	°C
V _{CC}	Supply Voltage Range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V _I , V _O	DC Input or Output Voltage		0	V _{CC}	V
t _t	Input Rise and Fall Time	2 V		1000	ns
		4.5 V		500	
		6 V		400	

5.3 Thermal Information

THERMAL METRIC		CD74HC151, CD74HCT151		UNIT
		D (SOIC)	N (PDIP)	
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	73	67	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V _{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V _{IL}	Low level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		
			6	1.8			1.8		1.8		
V _{OH}	High level output voltage	I _{OH} = - 20 μA	2	1.9			1.9		1.9		V
		I _{OH} = - 20 μA	4.5	4.4			4.4		4.4		
		I _{OH} = - 20 μA	6	5.9			5.9		5.9		
	High level output voltage	I _{OH} = - 4 mA	4.5	3.98			3.84		3.7		
		I _{OH} = - 5.2 mA	6	5.48			5.34		5.2		
V _{OL}	Low level output voltage	I _{OL} = 20 μA	2	0.1			0.1		0.1		V
		I _{OL} = 20 μA	4.5	0.1			0.1		0.1		
		I _{OL} = 20 μA	6	0.1			0.1		0.1		
	Low level output voltage	I _{OL} = 4 mA	4.5	0.26			0.33		0.4		
		I _{OL} = 5.2 mA	6	0.26			0.33		0.4		
I _I	Input leakage current	V _I = V _{CC} or GND	6	±0.1			±1		±1		μA
I _{CC}	Supply current	V _I = V _{CC} or GND	6	8			80		160		μA
HCT TYPES											
V _{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V _{IL}	Low level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V _{OH}	High level output voltage	I _{OH} = - 20 μA	4.5	4.4			4.4		4.4		V
	High level output voltage	I _{OH} = - 4 mA	4.5	3.98			3.84		3.7		
V _{OL}	Low level output voltage	I _{OL} = 20 mA	4.5	0.1			0.1		0.1		V
	Low level output voltage	I _{OL} = 4 mA	4.5	0.26			0.33		0.4		
I _I	Input leakage current	V _I = V _{CC} or GND	5.5	± 0.1			±1		± 1		μA
I _{CC}	Supply current	V _I = V _{CC} or GND	5.5	8			80		160		μA
Δ I _{CC} (2)	Additional supply current per input pin	Select inputs held at V _{CC} - 2.1	4.5 to 5.5	100 540			675		735		μA
		Data inputs held at V _{CC} - 2.1	4.5 to 5.5	100 162			202.5		220.5		
		Enable inputs held at V _{CC} - 2.1	4.5 to 5.5	100 108			135		147		

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

5.5 Switching Characteristics

Input $t_i = 6\text{ns}$. Unless otherwise specified, $C_L = 50\text{pF}$. (See [Parameter Measurement Information](#))

PARAMETER		V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t _{pd}	Any Data Input to Y	2			170		215		255	ns
		4.5		14 ⁽³⁾	34		43		51	
		6			29		37		43	
	Any Data Input to W	2			185		230		280	ns
		4.5		15 ⁽³⁾	37		46		56	
		6			31		39		48	
	Any Select to Y	2			185		230		280	ns
		4.5		15 ⁽³⁾	37		46		56	
		6			31		39		48	
	Any Select to W	2			205		255		310	ns
		4.5		17 ⁽³⁾	41		51		62	
		6			35		43		53	
	Enable to Y	2			140		175		210	ns
		4.5		11 ⁽³⁾	28		35		42	
		6			24		30		36	
	Enable to W	2			145		180		220	ns
		4.5		12 ⁽³⁾	29		36		44	
		6			25		31		38	
t _t	Output Transition Time	2			75		95		110	ns
		4.5			15		19		22	
		6			13		16		19	
C _{IN}	Input Capacitance				10		10		10	pF
C _{PD}	Power Dissipation Capacitance ^{(1) (2)}	5		59						pF
HCT TYPES										
t _{pd}	Any Data Input to Y	4.5		16 ⁽³⁾	38		48		57	ns
	Any Data Input to W	4.5		15 ⁽³⁾	36		45		54	ns
	Any Select to Y	4.5		17 ⁽³⁾	41		51		62	ns
	Any Select to W	4.5		18 ⁽³⁾	43		54		65	ns
	Enable to Y	4.5		12 ⁽³⁾	29		36		44	ns
C _L = 50 pF	Enable to W	4.5		15 ⁽³⁾	36		46		54	ns
t _t	Output Transition Time	4.5			15		19		22	ns
C _{IN}	Input Capacitance				10		10		10	pF
C _{PD}	Power Dissipation Capacitance ^{(1) (2)}	5		58						pF

(1) C_{PD} is used to determine the dynamic power consumption, per gate.

(2) $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

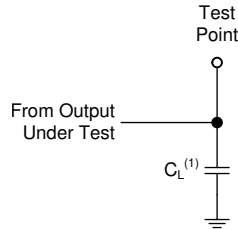
(3) $C_L = 15\text{ pF}$ and $V_{CC} = 5\text{ V}$

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_f < 6 \text{ ns}$.

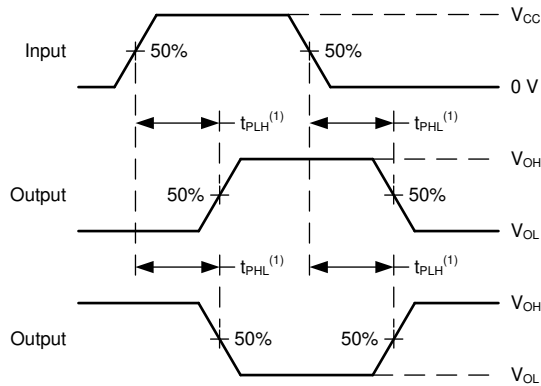
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



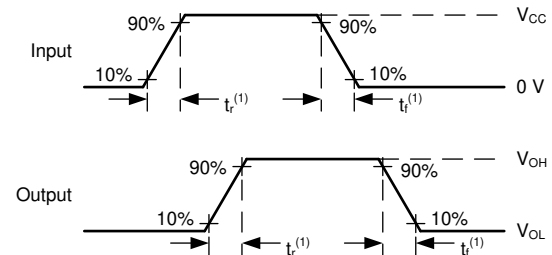
(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for Push-Pull Outputs



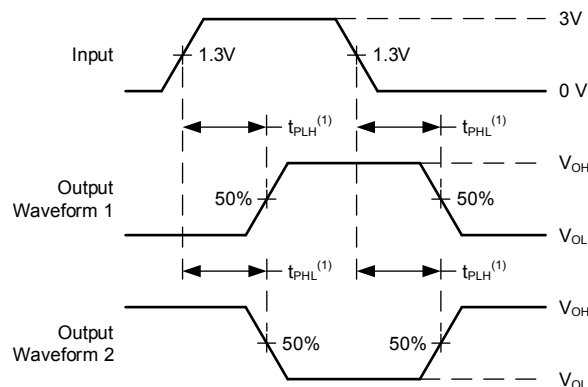
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

图 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t .

图 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

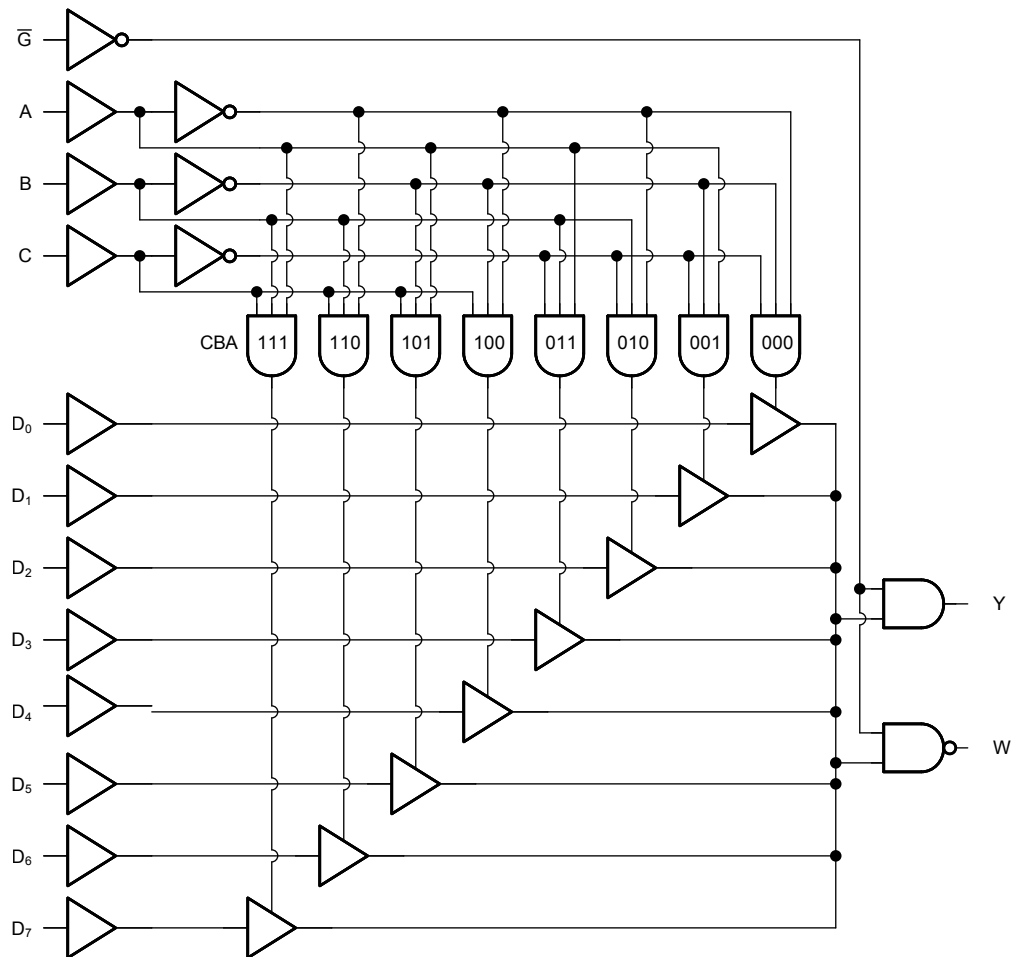
图 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

7.1 Overview

The ' HC151 and ' HCT151 are single 8-channel digital multiplexers having three binary control inputs, A, B and C and an active low enable ($\overline{G}$) input. The three binary signals select 1 of 8 channels. Outputs are both inverting (W) and non-inverting (Y).

7.2 Functional Block Diagram



7.3 Device Functional Modes

SELECT INPUTS ⁽¹⁾			DATA INPUTS								ENABLE	OUTPUT	
C	B	A	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	$\bar{G}$	W	Y
X	X	X	X	X	X	X	X	X	X	X	H	H	L
L	L	L	L	X	X	X	X	X	X	X	L	H	L
L	L	L	H	X	X	X	X	X	X	X	L	L	H
L	L	H	X	L	X	X	X	X	X	X	L	H	L
L	L	H	X	H	X	X	X	X	X	X	L	L	H
L	H	L	X	X	L	X	X	X	X	X	L	H	L
L	H	L	X	X	H	X	X	X	X	X	L	L	H
L	H	H	X	X	X	L	X	X	X	X	L	H	L
L	H	H	X	X	X	H	X	X	X	X	L	L	H
H	L	L	X	X	X	X	L	X	X	X	L	H	L
H	L	L	X	X	X	X	H	X	X	X	L	L	H
H	L	H	X	X	X	X	X	L	X	X	L	H	L
H	L	H	X	X	X	X	X	H	X	X	L	L	H
H	H	L	X	X	X	X	X	X	L	X	L	H	L
H	H	L	X	X	X	X	X	X	H	X	L	L	H
H	H	H	X	X	X	X	X	X	X	L	L	H	L
H	H	H	X	X	X	X	X	X	X	H	L	L	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9065201MEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9065201ME A CD54HCT151F3A
CD54HC151F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8412801EA CD54HC151F3A
CD54HC151F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8412801EA CD54HC151F3A
CD54HCT151F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9065201ME A CD54HCT151F3A
CD54HCT151F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9065201ME A CD54HCT151F3A
CD74HC151E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC151E
CD74HC151E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC151E
CD74HC151EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC151E
CD74HC151M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC151M
CD74HC151M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC151M
CD74HC151M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC151M
CD74HC151M96G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC151M
CD74HC151M96G4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC151M
CD74HC151MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC151M
CD74HCT151E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT151E
CD74HCT151E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT151E
CD74HCT151M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT151M
CD74HCT151M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT151M
CD74HCT151M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT151M
CD74HCT151M96G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT151M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54HC151, CD54HCT151, CD74HC151, CD74HCT151 :

- Catalog : [CD74HC151](#), [CD74HCT151](#)
- Military : [CD54HC151](#), [CD54HCT151](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

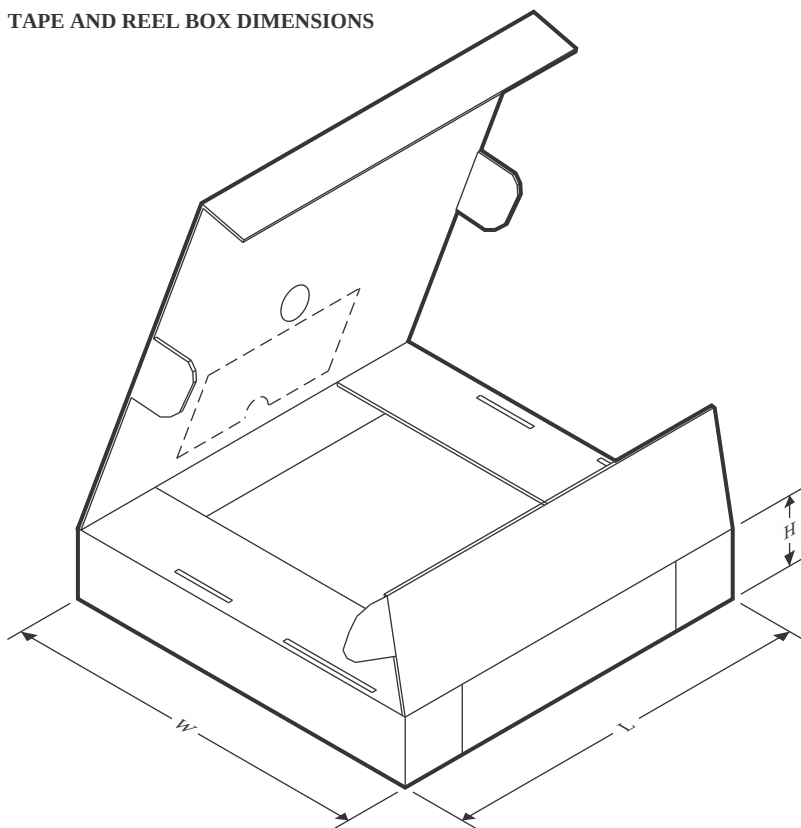
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC151M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC151M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT151M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC151M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC151M96G4	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT151M96	SOIC	D	16	2500	353.0	353.0	32.0

TUBE

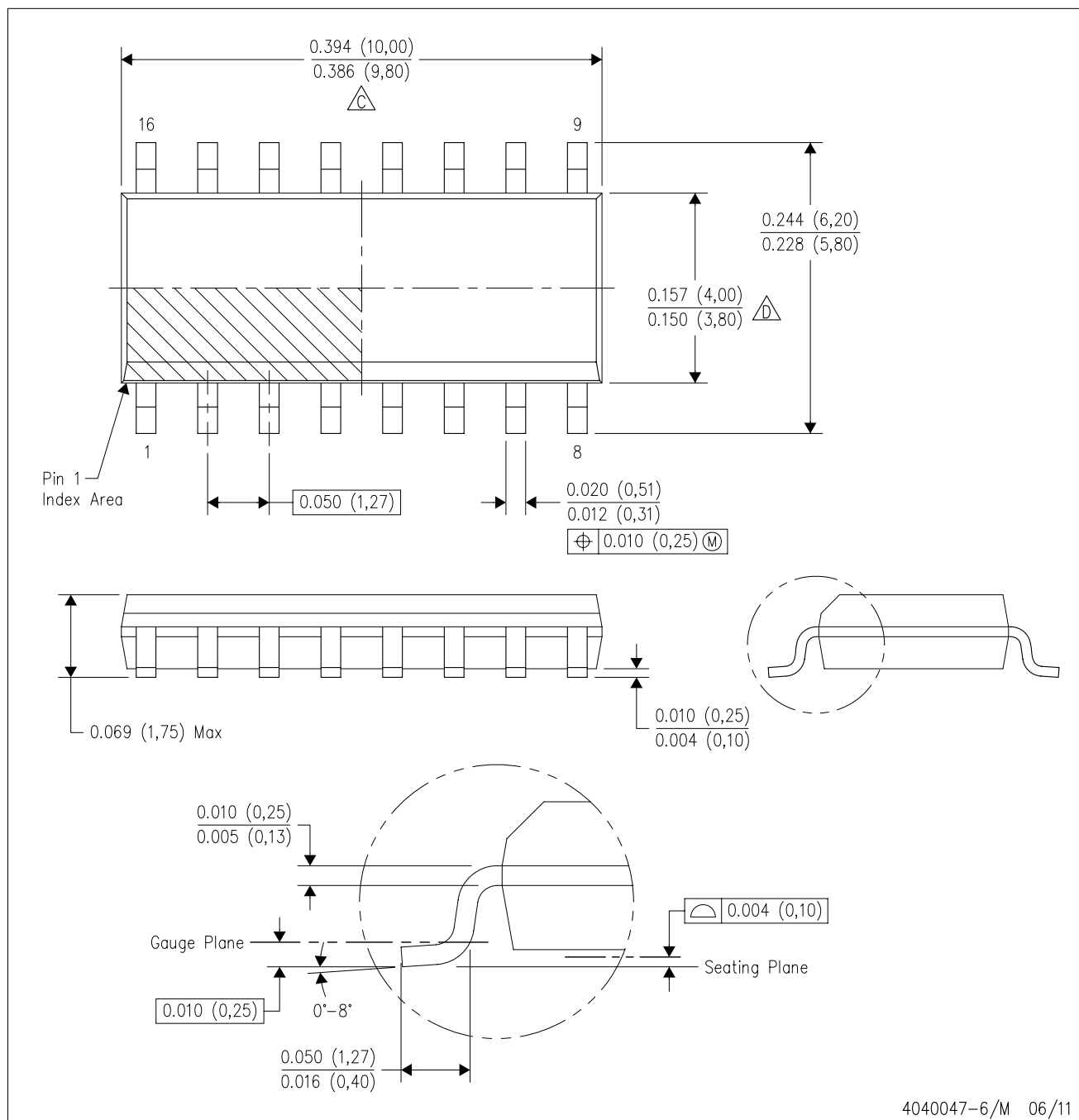


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC151E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC151E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC151E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC151E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC151EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC151EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT151E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT151E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT151E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT151E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



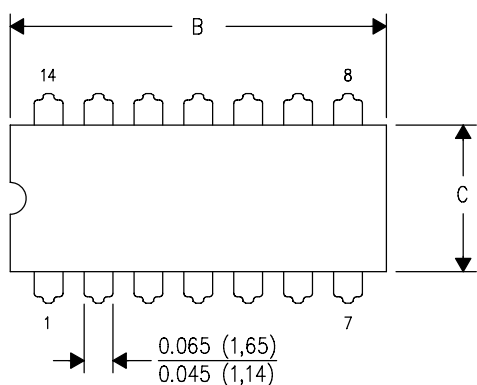
4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

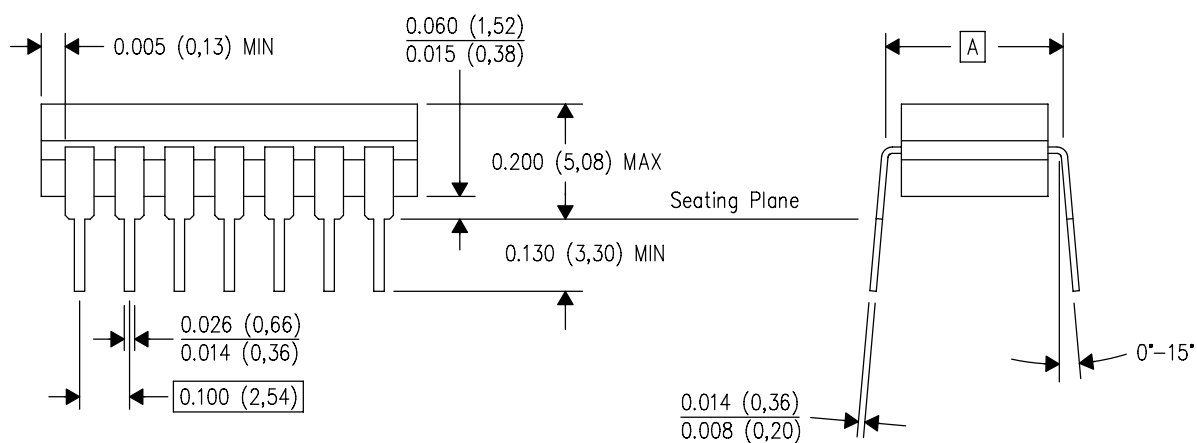
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



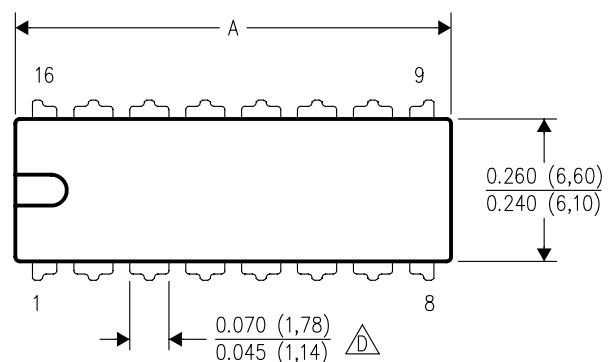
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

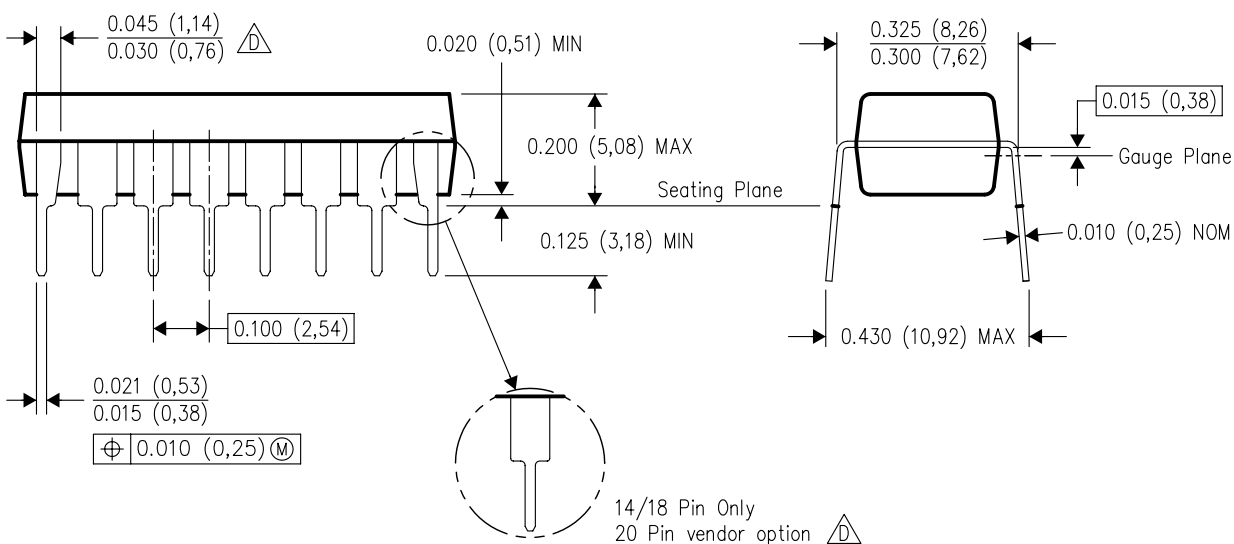
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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