针对 2.4GHz 射频 (RF) 应用的片上系统

特性

- 射频 **(RF)** 部分
  - 单片 **2.4GHz RF** 收发器和微控制器 **(MCU)**
  - 支持 **250kbps**，**500kbps**，**1Mbps** 和 **2Mbps** 数据速率
  - 出色的链路预算，无需外部前端即可实现长距离通信
  - 高达 **5dBm** 的可编程输出功率
  - 出色的接收器灵敏度（**2Mbps** 时为 **-90Bm**，**256kbps** 时为 **-9dBm**）
  - 适用于符合世界范围内的射频标准的系统：**ETSI EN 300 328** 和 **EN 300 440 2** 类（欧洲），**FCC CFR47** 第 **15** 部分（美国），和 **ARIB STD-T66**（日本）
  - 精确的接收信号强度指示器 **(RSSI)** 功能
- 布局
  - 极少的外部组件
  - 适用于单层印刷电路板 **(PCB)** 应用的引脚引线
  - 提供参考设计
  - **32** 引脚 **5mm x 5mm** 四方扁平无引线 **(QFN)**（**16** 通用 **I/O** 引脚）封装
- 低功率
  - 激活模式 **RX** 最佳性能：**21.2mA**
  - 激活模式 **TX (0dBm)**：**26mA**
  - 功率模式 **1**（**5μs** 唤醒）：**235μA**
  - 功率模式 **2**（睡眠定时器打开）：**0.9μA**
  - 功率模式 **3**（外部中断）：**0.4μA**
  - 宽电源电压范围（**2V** 至 **3.6V**）
  - 在所有功率模式下的完全 **RAM** 和寄存器保持
- 微控制器
  - 具有代码预取功能的高性能和低功率 **8051** 微控制器内核
  - **32KB** 闪存程序内存
  - **1KB SRAM**
  - 支持硬件调试
  - 扩展基带自动化，包括自动确认和地址解码
- 外设
  - 可访问所有内存区域和外设的两个通道 **DMA**
  - 通用定时器（**1** 个 **16** 位，**2** 个 **8** 位）
  - 无线电定时器，**40** 位
  - 红外 **(IR)** 生成电路
  - 多个振荡器：
    - **32MHz** 晶体振荡器 **(XOSC)**
    - **16MHz RC** 振荡器 **(RCOSC)**
    - **32MHz RCOSC**
  - 具有捕捉功能的 **32kHz** 睡眠定时器
  - 高级加密标准 **(AES)** 安全协处理器
  - 通用异步收发器 **(UART)** / 串行外设接口 **(SPI)** / **I^2C** 串行接口
  - **16** 个通用 **I/O** 引脚（**3 x 20mA** 驱动强度，其余引脚有 **4mA** 的驱动强度）
  - 安全装置定时器
  - 真随机数发生器
  - 模数转换器 **(ADC)** 和模拟比较器

应用范围

- 专有 **2.4 GHz** 系统
- 人机接口器件（键盘、鼠标）
- 消费类电子产品

这些装置包含有限的内置 ESD 保护。

存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

说明

CC2543 是一款经优化的针对数据速率高达 2Mbps 且使用低物料清单成本制造的片上系统 (SoC) 解决方案。 CC2543 将处于领先地位的 RF 收发器的出色性能与一个单周期 8051 兼容 CPU，32KB 系统内可编程闪存存储器，高达 1KB RAM，以及许多其它功能强大的特性组合在一起。 CC2543 有高效的功率模式（RAM 和寄存器保持电流低于 1μA），这使得它非常适合应用于要求超低功耗的低占空比系统。 运行模式间较短的转换时间进一步确保了低能耗。

CC2543 与 CC2541/CC2544/CC2545 兼容。 它采用带有 SPI/UART/USB 接口的 5mm x 5mm QFN32 封装。 供货时，CC2543 带有由德州仪器 (TI) 提供的完整参考设计。

此器件针对无线消费类产品和人机接口器件 (HID) 应用。 CC2543 专为诸如无线鼠标的外设器件而设计。

方框图请见Figure 7。

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage VDD	All supply pins must have the same voltage	–0.3	3.9	V
Voltage on any digital pin		–0.3	VDD + 0.3 ≤ 3.9	V
Input RF level			10	dBm
Storage temperature range		–40	125	°C
ESD(2)	All pins, excluding 20 and 21, according to human-body model, JEDEC STD 22, method A114 (HBM)		2.5	kV
	All pins, according to human-body model, JEDEC STD 22, method A114 (HBM)		1.5	kV
	According to charged-device model, JEDEC STD 22, method C101 (CDM)		750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) **CAUTION**: ESD sensitive device. Precaution should be used when handing the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Operating ambient temperature range, T_A		–40	85	°C
Operating supply voltage VDD	All supply pins must have same voltage	2	3.6	V

ELECTRICAL CHARACTERISTICS

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C and VDD = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	2 Mbps, GFSK, 320-kHz deviation				
I_{core} – Core current consumption	RX mode, no peripherals active, low MCU activity		21.2		mA
	TX mode, 0-dBm output power, no peripherals active, low MCU activity		26		mA
	TX mode, 5-dBm output power, no peripherals active, low MCU activity		29.4		mA
	Active mode, 16-MHz RCOSC, Low MCU activity		3		mA
	Active mode, 32-MHz clock frequency, low MCU activity		6		mA
	Power mode 0, CPU clock halted, all peripherals on, no clock division, 32-MHz crystal selected		4.5		mA
	Power mode 0, CPU clock halted, all peripherals on, clock division at max (Limits max speed in peripherals except radio), 32-MHz crystal selected		3.1		mA
	Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crys tal oscillator off; 32.753-kHz RCOSC, POR, BOD, and sleep timer active; RAM and register retention		235		µA
	Power mode 2. Digital regulator off, 16 MHz RCOSC and 32 MHz crystal oscillator off; 32.753 kHz RCOSC, POR and sleep timer active; RAM and register retention		0.9		µA
	Power mode 3. Digital regulator off, no clocks, POR active; RAM and register retention		0.4		µA
I_{peri} – Peripheral current consumption (Adds to core current I_{core} for each peripheral unit activated)	Timer 1 (16-bit). Timer running, 32-MHz XOSC used		90		µA
	Radio timer(40 bit). Timer running, 32-MHz XOSC used		90		µA
	Timer 3 (8-bit). Timer running, 32-MHz XOSC used		60		µA
	Timer 4 (8-bit). Timer running, 32-MHz XOSC used		70		µA
	Sleep timer. Including 32.753-kHz RCOSC		0.6		µA

GENERAL CHARACTERISTICS

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C and VDD = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP AND TIMING					
Power mode 1 → Active	Digital regulator ON, 16-MHz RCOSC and 32-MHz crystal oscillator OFF. Start-up of 16-MHz RCOSC		5		µs
Power mode 2 or 3 → Active	Digital regulator OFF, 16 MHz RCOSC and 32 MHz crystal oscillator OFF. Start-up of regulator and 16 MHz RCOSC		130		µs
Active → TX or RX	Crystal ESR = 16 Ω. Initially running on 16-MHz RCOSC, with 32-MHz XOSC OFF		500		µs
	With 32-MHz XOSC initially ON		180		µs
RX/TX turnaround	RCOSC, with 32MHz XOSC OFF		130		µs
RADIO PART					
RF frequency range	Programmable in 1-MHz steps	2379		2496	MHz
Data rates and modulation formats	2 Mbps, GFSK 320-kHz deviation 2-Mbps, GFSK 500 kHz deviation 1-Mbps, GFSK 250 kHz deviation 1-Mbps, GFSK 160 kHz deviation 500 kbps, MSK 250 kbps, GFSK 160 kHz deviation 250 kbps, MSK				

RF RECEIVE SECTION

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C, VDD = 3 V, and f_C = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps, GFSK, 320-kHz DEVIATION, 0.1% BER					
Receiver sensitivity			–86		dBm
Saturation			–8		dBm
Co-channel rejection	Wanted signal at –67 dBm		–13		dB
In-band blocking rejection	±2-MHz offset, wanted signal at –67 dBm		–1		dB
	±4-MHz offset, wanted signal at –67 dBm		34		
	>±6-MHz offset, wanted signal at –67 dBm		38		
Out-of-band blocking rejection	1-MHz resolution. Wanted signal at –67 dBm, f < 2 GHz Two exception frequencies with poorer performance		–32		dBm
	1-MHz resolution. Wanted signal at –67 dBm, 2 GHz > f < 3 GHz Two exception frequencies with poorer performance		–38		
	1-MHz resolution. Wanted signal at –67 dBm, f > 3GHz Two exception frequencies with poorer performance		–12		
Intermodulation	Wanted signal at –64 dBm, 1st interferer is CW, 2nd interferer is GFSK-modulated signal. Offsets of interferers are: 6 and 12 MHz 8 and 16 MHz 10 and 20 MHz		–43		dBm
Frequency error tolerance(1)	Including both initial tolerance and drift. Sensitivity better than –70 dBm. 250 byte payload.	–300		300	kHz
Symbol rate error tolerance(2)	Sensitivity better than -70 dBm. 250 byte payload.	–120		120	ppm
2 Mbps, GFSK, 500 kHz DEVIATION, 0.1% BER					
Receiver sensitivity			–90		dBm
Saturation			–3		dBm
Co-channel rejection	Wanted signal at –67 dBm		–10		dB
In-band blocking rejection	±2 MHz offset, wanted signal at –67 dBm		–3		dB
	±4 MHz offset, wanted signal at –67 dBm		36		dB
	>±6 MHz offset, wanted signal at –67 dBm		44		dB
Frequency error tolerance(1)	Including both initial tolerance and drift. Sensitivity better than –70 dBm. 250 byte payload.	–300		300	kHz
Symbol rate error tolerance(2)	Sensitivity better than -70 dBm. 250 byte payload.	–120		120	ppm
1 Mbps, GFSK, 250 kHz DEVIATION, 0.1% BER					
Receiver sensitivity			–94		dBm
Saturation			6		dBm
Co-channel rejection	Wanted signal at –67 dBm		–7		dB
In-band blocking rejection	±1 MHz offset, wanted signal –67 dBm		0		dB
	±2 MHz offset, wanted signal –67 dBm		30		
	±3 MHz offset, wanted signal –67 dBm		34		
	>±5 MHz offset, wanted signal –67 dBm		38		
Frequency error tolerance	Including both initial tolerance and drift. Sensitivity better than –70 dBm. 250 byte payload.	–250		250	kHz
Symbol rate error tolerance	Sensitivity better than –70 dBm. 250 byte payload.	-80		80	ppm

(1) Difference between center frequency of the received RF signal and local oscillator frequency
(2) Difference between incoming symbol rate and the internally generated symbol rate

RF RECEIVE SECTION (continued)

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C, VDD = 3 V, and f_C = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
1 Mbps, GFSK, 160 kHz DEVIATION, 0.1% BER					
Receiver sensitivity			–91		dBm
Saturation			6		dBm
Co-channel rejection	Wanted signal at –67 dBm		–8		dB
In band blocking rejection	±1 MHz offset, wanted signal at –67 dBm		2		dB
	±2 MHz offset, wanted signal at –67 dBm		28		
	±3 MHz offset, wanted signal at –67 dBm		33		
	>±5 MHz offset, wanted signal at –67 dBm		36		
Frequency error tolerance	Including both initial tolerance and drift, Sensitivity better than –67 dBm	–250		250	kHz
Symbol rate error tolerance	Maximum packet length	–80		80	ppm
500 kbps, MSK, 0.1% BER					
Receiver sensitivity			–98		dBm
Saturation			6		dBm
Co-channel rejection	Wanted signal at –67 dBm		–5		dB
In band blocking rejection	±1 MHz offset, wanted signal at –67 dBm		21		dB
	±2 MHz offset, wanted signal at –67 dBm		32		
	>±2 MHz offset, wanted signal at –67 dBm		33		
Frequency error tolerance	Including both initial tolerance and drift, Sensitivity better than –67dBm	–150		150	kHz
Symbol rate error tolerance	Maximum packet length	–60		60	ppm
250 kbps, GFSK, 160 kHz DEVIATION , 0.1% BER					
Receiver sensitivity			–98		dBm
Saturation			6		dBm
Co-channel rejection	Wanted signal at –67 dBm		–2		dB
In-band blocking rejection	±1 MHz offset, wanted signal at –67 dBm		22		dB
	±2 MHz offset, wanted signal at –67 dBm		32		
	>±2 MHz offset, wanted signal at –67 dBm		32		
Frequency error tolerance	Including both initial tolerance and drift, Sensitivity better than –67 dBm	–150		150	kHz
Symbol rate error tolerance	Maximum packet length	–60		60	ppm
250 kbps, MSK, 0.1% BER					
Receiver sensitivity			–98		dBm
Saturation			6		dBm
Co-channel rejection	Wanted signal at –67 dBm		–5		dB
In-band blocking rejection	±1 MHz offset, wanted signal at –67 dBm		21		dB
	±2 MHz offset, wanted signal at –67 dBm		32		
	>2 MHz offset, wanted signal at –67 dBm		33		
Frequency error tolerance	Including both initial tolerance and drift, Sensitivity better than –67 dBm	–150		150	kHz
Symbol rate error tolerance	Maximum packet length	–60		60	ppm
ALL RATES/FORMATS					
Spurious emission in RX. Conducted measurement	f < 1 GHz		–67		dBm
Spurious emission in RX. Conducted measurement	f > 1 GHz		–60		dBm

RF TRANSMIT SECTION

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C, VDD = 3 V, and f_C = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, maximum setting	Delivered to a single-ended 50-Ω load through a balun using maximum recommended output power setting.		5		dBm
Output power, minimum setting	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting.		–20		dBm
Programmable output power range	Delivered to a single-ended 50-Ω load through a balun.		25		dB
Spurious emission in TX. Conducted measurement	f < 1 GHz		–46		dBm
	f > 1 GHz		–46		dBm
	Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations: ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)				

Use a simple LC filter (1.6nH and 1.8pF in parallel to ground) to pass ETSI conducted requirements below 1GHz in restricted bands. For radiated measurements low antenna gain for these frequencies (depending on antenna design) can achieve the same attenuation of these low frequency components (see EM reference design).

32-MHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C, VDD = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency			32		MHz
Crystal frequency accuracy requirement	250 kbps and 500 kbps data rates 1 Mbps data rate 2 Mbps data rate	–30 –40 –60		30 40 60	ppm
Equivalent series resistance		6		60	Ω
Crystal shunt capacitance		1		7	pF
Crystal load capacitance		10		16	pF
Start-up time			0.25		ms
Power-down guard time	The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load.	3			ms

32-kHz RC OSCILLATOR

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C, VDD = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency			32.753		kHz
Frequency accuracy after calibration			±0.2%		
Temperature coefficient			0.4		%/ºC
Supply-voltage coefficient			3		%/V
Calibration time			2		ms

16-MHz RC OSCILLATOR

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C, VDD = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency			16		MHz
Uncalibrated frequency accuracy			±18%		
Frequency accuracy after calibration			±0.6%		
Start-up time			10		µs
Initial calibration time			50		µs

RSSI CHARACTERISTICS

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C, VDD = 3 V, unless otherwise noted.

2Mbps, GFSK, 320-kHz Deviation, 0.1% BER and 2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER			
RSSI range(1)	Reduced gain by AC algorithm	64	dB
	High gain by AGC algorithm	64	
RSSI offset(1)	Reduced gain by AGC algorithm	79	dBm
	High gain by AGC algorithm	99	
Absolute uncalibrated accuracy(1)		±3	dB
Step size (LSB value)		1	dB
All Other Rates/Formats			
RSSI range(1)		64	dB
RSSI offset(1)		99	dBm
Absolute uncalibrated accuracy		±3	dB
Step size (LSB value)		1	dB

(1) Assuming CC2543 EM reference design. Other RF designs give an offset from the reported value.

FREQUENCY SYNTHESIZER CHARACTERISTICS

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C, VDD = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier	At ±1 MHz from carrier		–112		dBc/Hz
	At ±3 MHz from carrier		–119		
	At ±5 MHz from carrier		–122		

ANALOG TEMPERATURE SENSOR

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C, VDD = 3 V unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output	Measured using integrated ADC, internal band-gap voltage reference, and maximum resolution		1480		12-bit
Temperature coefficient			4.5		/ 1ºC
Voltage coeficcient			1		/ 0.1V
Initial accuracy without calibration			±10		ºC
Accuracy using 1-point calibration			±5		ºC
Current consumption when enabled			0.5		mA

COMPARATOR CHARACTERISTICS

T_A = 25°C, VDD = 3 V. All measurement results are obtained using the CC2543 reference designs, post-calibration.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common-mode maximum voltage			VDD		V
Common-mode minimum voltage			–0.3		
Input offset voltage			1		mV
Offset vs temperature			16		µV/°C
Offset vs operating voltage			4		mV/V
Supply current			230		nA
Hysteresis			0.15		mV

ADC CHARACTERISTICS

T_A = 25°C and VDD = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage	VDD is voltage from supply	0		VDD	V
	External reference voltage	VDD is voltage from supply	0		VDD	V
	External reference voltage differential	VDD is voltage from supply	0		VDD	V
	Input resistance, signal	Simulated using 4-MHz clock speed		197		kΩ
	Full-scale signal(1)	Peak-to-peak, defines 0 dBFS		2.97		V
ENOB(1)	Effective number of bits	Single-ended input, 7-bit setting		5.7		bits
		Single-ended input, 9-bit setting		7.5		
		Single-ended input, 10-bit setting		9.3		
		Single-ended input, 12-bit setting		10.3		
		Differential input, 7-bit setting		6.5		
		Differential input, 9-bit setting		8.3		
		Differential input, 10-bit setting		10		
		Differential input, 12-bit setting		11.5		
		10-bit setting, clocked by RCOSC		9.7		
		12-bit setting, clocked by RCOSC		10.9		
	Useful power bandwidth	7-bit setting, both single and differential		0–20		kHz
THD	Total harmonic distortion	Single ended input, 12-bit setting, –6 dBFS(1)		–75.2		dB
		Differential input, 12-bit setting, –6 dBFS(1)		–86.6		
	Signal to nonharmonic ratio	Single-ended input, 12-bit setting(1)		70.2		dB
		Differential input, 12-bit setting(1)		79.3		
		Single-ended input, 12-bit setting, –6 dBFS(1)		78.8		
		Differential input, 12-bit setting, –6 dBFS(1)		88.9		
CMRR	Common-mode rejection ratio	Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		>84		dB
	Crosstalk	Single ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		>84		dB
	Offset	Midscale		–3		mV
	Gain error			0.68%		
DNL	Differential nonlinearity	12-bit setting, mean(1)		0.05		LSB
		12-bit setting, maximum(1)		0.9		
INL	Integral nonlinearity	12-bit setting, mean(1)		4.6		LSB
		12-bit setting, maximum(1)		13.3		
		12-bit setting, mean, clocked by RCOSC		10		
		12-bit setting, max, clocked by RCOSC		29		
SINAD (–THD+N)	Signal-to-noise-and-distortion	Single ended input, 7-bit setting(1)		35.4		dB
		Single ended input, 9-bit setting(1)		46.8		
		Single ended input, 10-bit setting(1)		57.5		
		Single ended input, 12-bit setting(1)		66.6		
		Differential input, 7-bit setting(1)		40.7		
		Differential input, 9-bit setting(1)		51.6		
		Differential input, 10-bit setting(1)		61.8		
		Differential input, 12-bit setting(1)		70.8		
	Conversion time	7-bit setting		20		µs
		9-bit setting		36		
		10-bit setting		68		
		12-bit setting		132		

(1) Measured with 300-Hz sine-wave input and VDD as reference.

ADC CHARACTERISTICS (continued)

T_A = 25°C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power consumption			1.2		mA
Internal reference VDD coefficient			4		mV/V
Internal reference temperature coefficient			0.4		mV/10°C
Internal reference voltage			1.15		V

DC CHARACTERISTICS

Measured on Texas Instruments CC2543EM reference design with T_A = 25°C, VDD = 3 V, unless otherwise noted.(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.5			V
Logic-0 input current		–50		50	nA
Logic-1 input current		–50		50	nA
I/O pin pullup and pulldown resistors			20		kΩ
Logic-0 output voltage 4-mA pins	Output load 4 mA			0.5	V
Logic-1 output voltage 4-mA pins	Output load 4 mA	2.4			V
Logic-0 output voltage 20-mA pins	Output load 20 mA			0.5	V
Logic-1 output voltage 20-mA pins	Output load 20 mA	2.4			V

(1) Note that only two of the three 20mA pins can drive in the same direction at the same time, and toggle at the same time.

CONTROL INPUT AC CHARACTERISTICS

T_A = –40°C to 85°C, VDD = 2 V to 3.6 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System clock, f_{SYSCLK} t_{SYSCLK} = 1/ f_{SYSCLK}	The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used.	16		32	MHz
RESET_N low duration	See item 1, Figure 1. This is the shortest pulse that is recognized as a complete reset pin request. Note that shorter pulses may be recognized but do not lead to complete reset of all modules within the chip.	1			µs
Interrupt pulse duration	See item 2, Figure 1.This is the shortest pulse that is recognized as an interrupt request.	20			ns

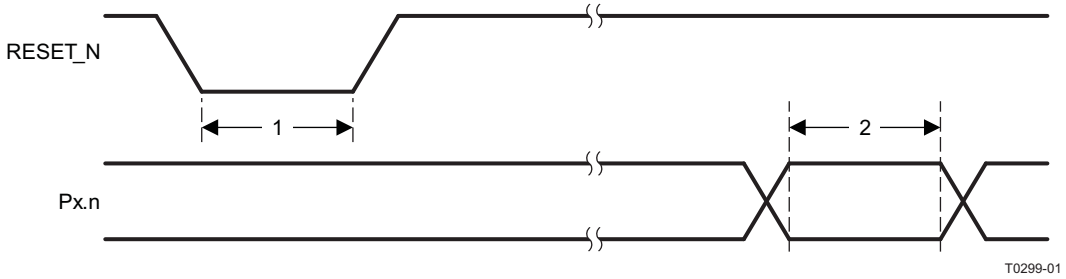


Figure 1. Control Input AC Characteristics

SPI AC CHARACTERISTICS

T_A = –40°C to 85°C, VDD = 2 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	SCK period	Master, RX and TX	250			ns
		Slave, RX and TX	250			
	SCK duty cycle	Master		50%		
t_2	SSN low to SCK, Figure 2 and Figure 3	Master	63			ns
		Slave	63			
t_3	SCK to SSN high	Master	63			ns
		Slave	63			
t_4	MOSI early out	Master, load = 10 pF			7	ns
t_5	MOSI late out	Master, load = 10 pF			10	ns
t_6	MISO setup	Master	90			ns
t_7	MISO hold	Master	10			ns
	SCK duty cycle	Slave		50%		ns
t_{10}	MOSI setup	Slave	35			ns
t_{11}	MOSI hold	Slave	10			ns
t_8	MISO early out	Slave, load = 10 pF			0	ns
t_9	MISO late out	Slave, load = 10 pF			95	ns
	Operating frequency	Master, TX only			8	MHz
		Master, RX and TX			4	
		Slave, RX only			8	
		Slave, RX and TX			4	

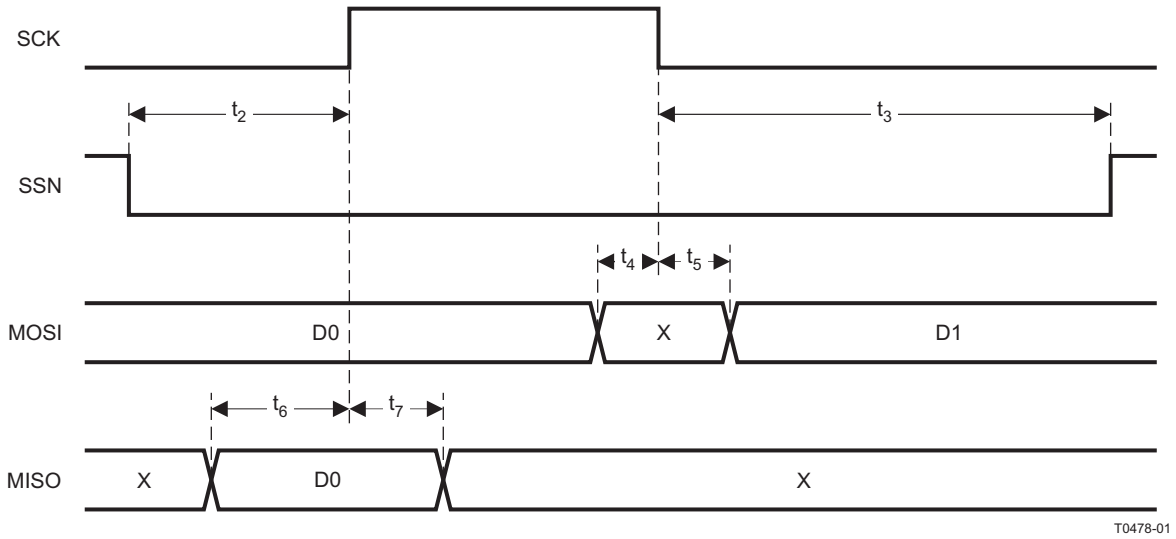


Figure 2. SPI Master AC Characteristics

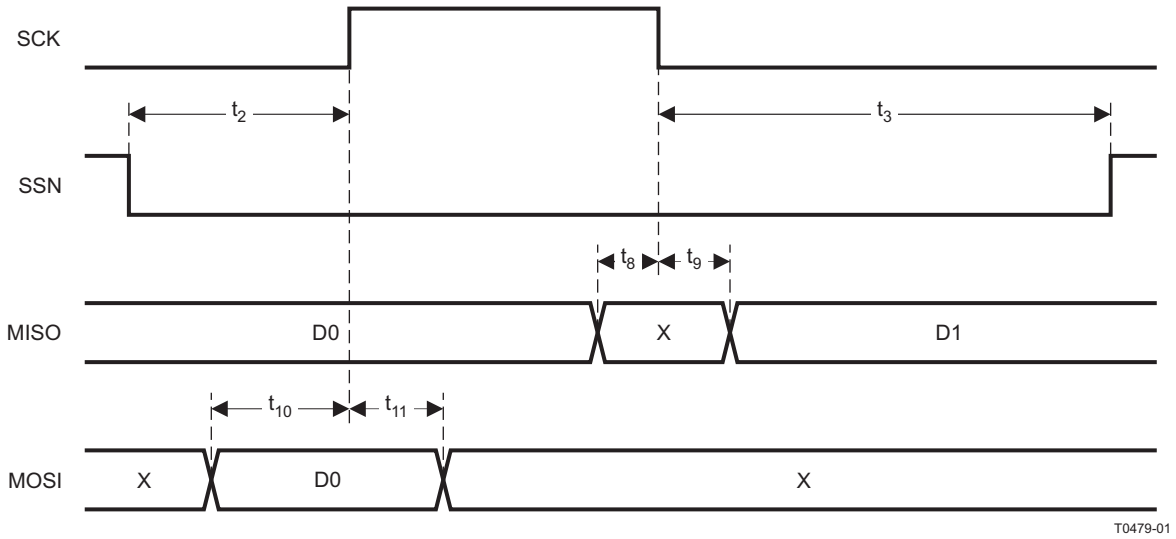


Figure 3. SPI Slave AC Characteristics

DEBUG INTERFACE AC CHARACTERISTICS

T_A = –40°C to 85°C, VDD = 2 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk_dbg}	Debug clock frequency (see Figure 4)				12	MHz
t_1	Allowed high pulse on clock (see Figure 4)		35			ns
t_2	Allowed low pulse on clock (see Figure 4)		35			ns
t_3	EXT_RESET_N low to first falling edge on debug clock (see Figure 5)		167			ns
t_4	Falling edge on clock to EXT_RESET_N high (see Figure 5)		83			ns
t_5	EXT_RESET_N high to first debug command (see Figure 5)		83			ns
t_6	Debug data setup (see Figure 6)		2			ns
t_7	Debug data hold (see Figure 6)		4			ns
t_8	Clock-to-data delay (see Figure 6)	Load = 10 pF			30	ns

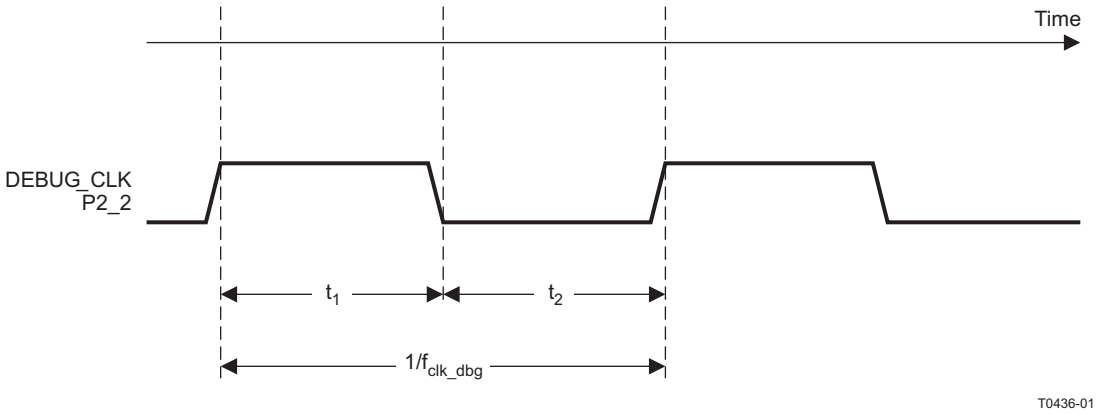


Figure 4. Debug Clock – Basic Timing

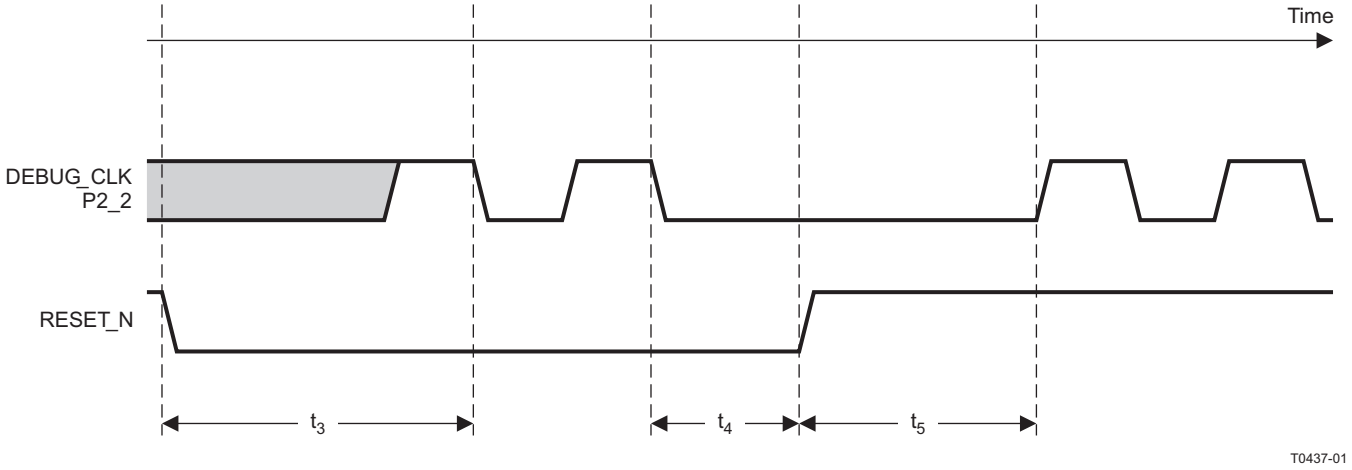


Figure 5. Debug Enable Timing

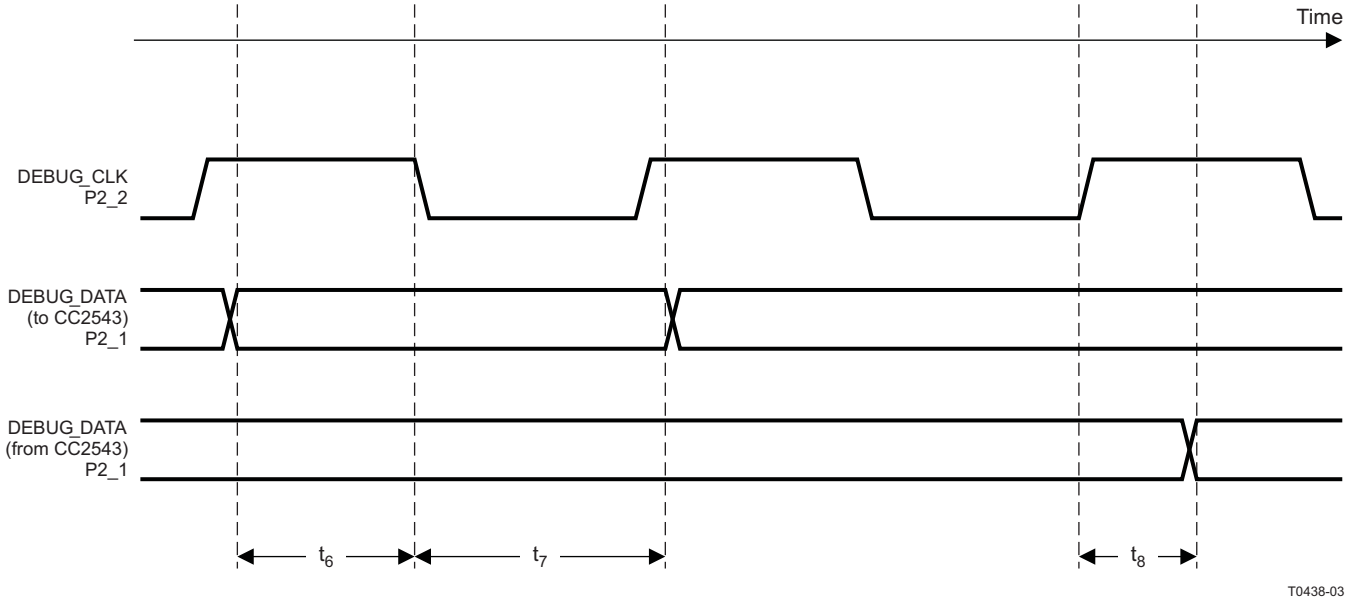


Figure 6. Data Setup and Hold Timing

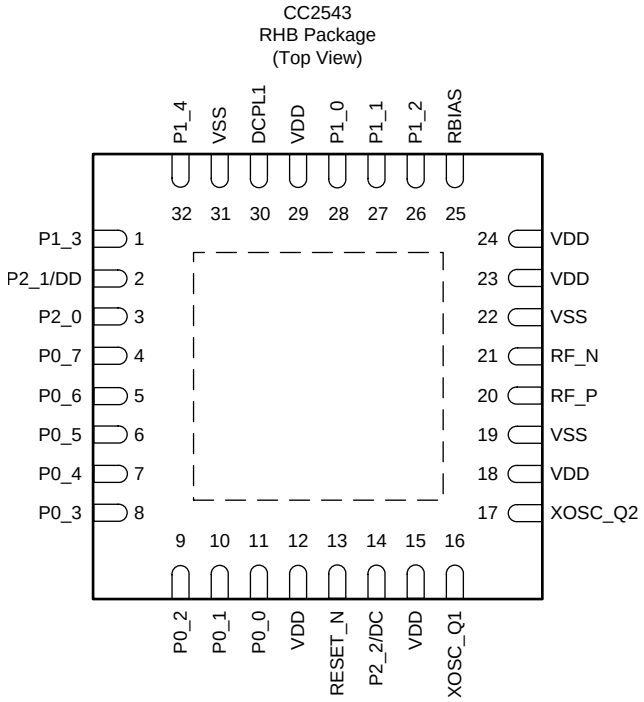
TIMER INPUTS AC CHARACTERISTICS

T_A = –40°C to 85°C, VDD = 2 V to 3.6 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capture pulse duration	Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate at the current system clock rate (16 MHz or 32 MHz).	1.5			t_{SYSCLK}

DEVICE INFORMATION

PIN DESCRIPTIONS



NOTE: The exposed ground pad must be connected to a solid ground plane; this is the main ground connection for the chip.

Table 1. Pin Description Table

NAME	PIN	PIN TYPE	DESCRIPTION
P1_3	1	Digital I/O	Port 1.3
P2_1/DD	2	Digital I/O / Debug	Port 2.1 / Debug Data
P2_0	3	Digital I/O	Port 2.0
P0_7	4	Digital I/O	Port 0.7
P0_6	5	Digital I/O	Port 0.6
P0_5	6	Digital I/O	Port 0.5
P0_4	7	Digital I/O	Port 0.4
P0_3	8	Digital I/O	Port 0.3
P0_2	9	Digital I/O	Port 0.2
P0_1	10	Digital I/O	Port 0.1
P0_0	11	Digital I/O	Port 0.0
VDD	12	Power (analog)	2-V-3.6V analog power-supply connection
RESET_N	13	Digital input	Reset, active-low
P2_2/DC	14	Digital I/O / Debug	Port 2.2 / Debug Clock
VDD	15	Power (analog)	2-V-3.6V analog power-supply connection
XOSC_Q1	16	Analog O	32-MHz crystal oscillator pin 1
XOSC_Q2	17	Analog O	32-MHz crystal oscillator pin 2
VDD	18	Power (analog)	2-V-3.6V analog power-supply connection
VSS	19	Unused pin	Connect to ground
RF_P	20	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX

Table 1. Pin Description Table (continued)

NAME	PIN	PIN TYPE	DESCRIPTION
RF_N	21	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
VSS	22	Unused pin	Connect to ground
VDD	23	Power (analog)	2-V–3.6-V analog power-supply connection
VDD	24	Power (analog)	2-V–3.6-V analog power-supply connection
RBIAS	25	Analog I/O	External precision bias resistor for reference current
P1_2	26	Digital I/O	Port 1.2, 20 mA
P1_1	27	Digital I/O	Port 1.1, 20 mA
P1_0	28	Digital I/O	Port 1.0, 20 mA
VDD	29	Power (analog)	2-V–3.6-V analog power-supply connection
DCPL1	30	Power (digital)	1.8-V digital power-supply decoupling. Do not use for supplying external circuits.
VSS	31	Unused pin	Connect to ground
P1_4	32	Digital I/O	Port 1.4
VSS	Ground pad	Ground	Must be connected to solid ground as this is the main ground connection for the chip. See Pinout Diagram.

BLOCK DIAGRAM

A block diagram of the CC2543 is shown in Figure 7. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given. See CC2543/44/45 User's Guide (SWRU283) for more details.

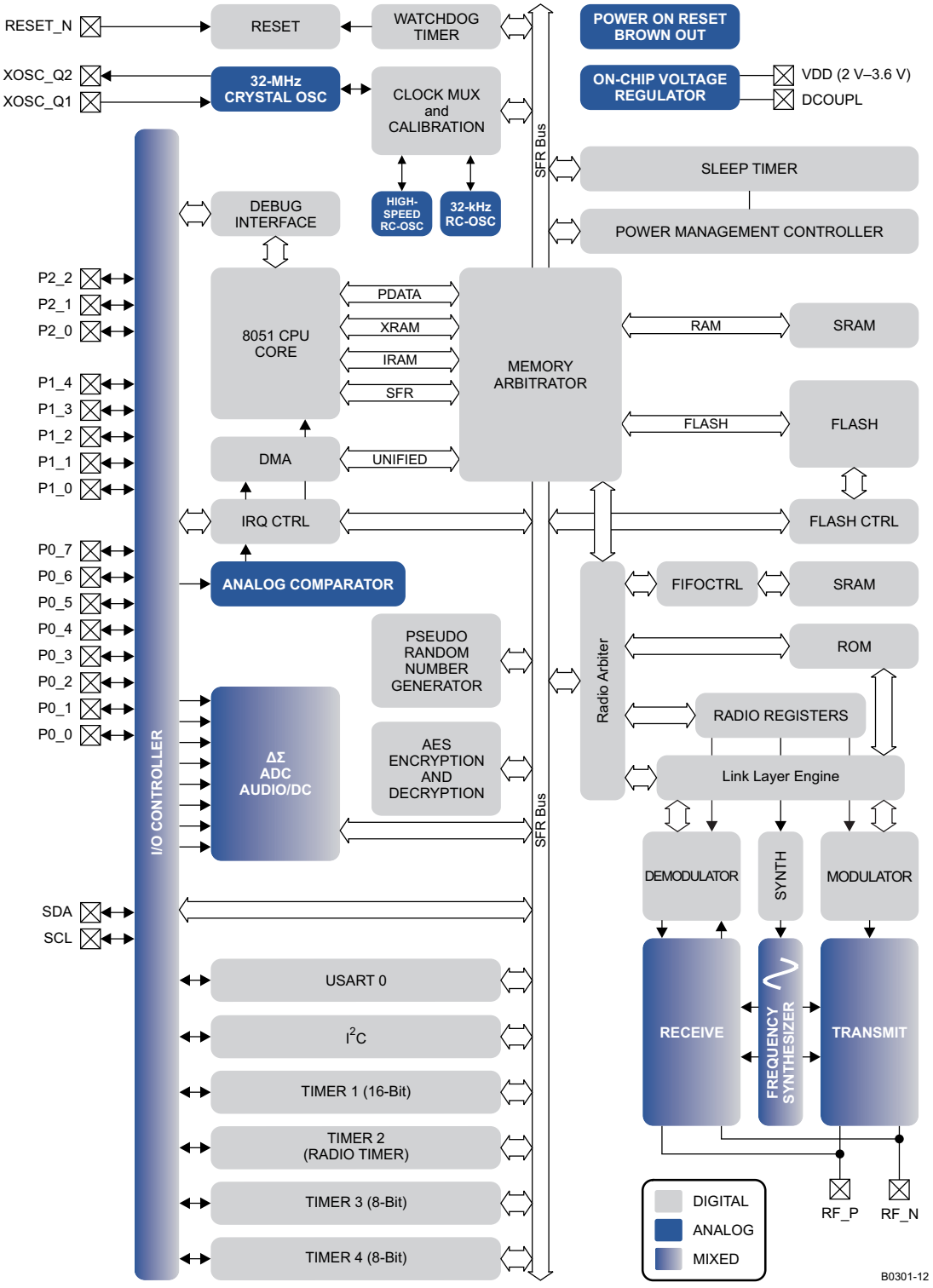


Figure 7. CC2543 Block Diagram

BLOCK DESCRIPTIONS

CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE/XDATA), a debug interface, and an 15-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in Figure 7 as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The **1-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces.

The **18-KB/32-KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bytewise programming. See User Guide for details on the flash controller.

A versatile two-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USART, timers, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

The **interrupt controller** services a total of 17 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. Any interrupt service request is serviced also when the device is in idle mode by going back to active mode. Some interrupts can also wake up the device from sleep mode (when in sleep mode, the device is in low-power mode PM1, PM2 or PM3).

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to perform an erasure of the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute supplied instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between several different I/O pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that uses an internal 32.753-kHz RC oscillator. The sleep timer runs continuously in all operating modes. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power modes 1 or 2.

A built-in **watchdog timer** allows the CC2543 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer used by the Radio. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which a packet ends. There are two 16-bit timer-compare registers and two 24-bit overflow-compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 is configurable as either an SPI master/slave or a UART. It provides double buffering on both RX and TX and hardware flow control and is thus well suited to high-throughput full-duplex applications. The USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USART samples the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The **I^2C** module provides a digital peripheral connection with two pins and supports both master and slave operation.

The **ADC** supports 7 bits (30 kHz bandwidth) to 12 bits (4 kHz bandwidth) of resolution. DC and audio conversions with up to eight input channels (Port 0) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

The ultralow-power **analog comparator** enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is mapped into the digital I/O port and can be treated by the MCU as a regular digital input.

TYPICAL CHARACTERISTICS

RX CURRENT vs TEMPERATURE

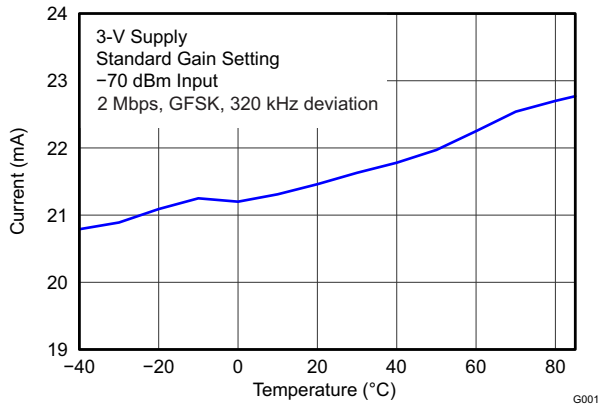


Figure 8.

TX CURRENT vs TEMPERATURE

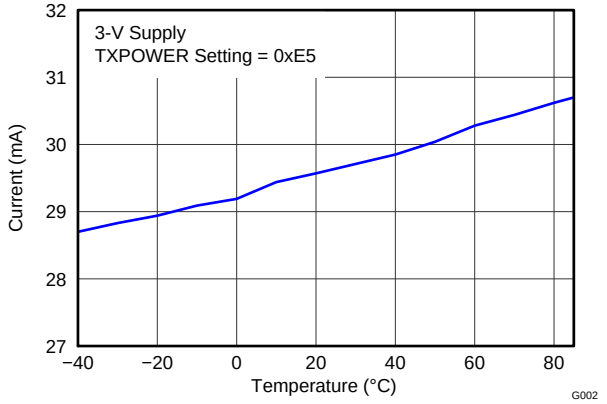


Figure 9.

RX SENSITIVITY vs TEMPERATURE

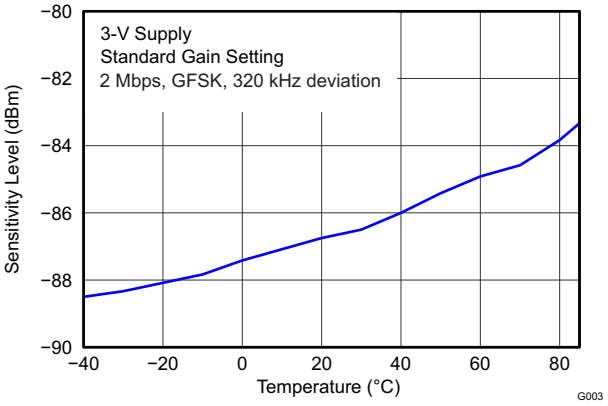


Figure 10.

TX POWER vs TEMPERATURE

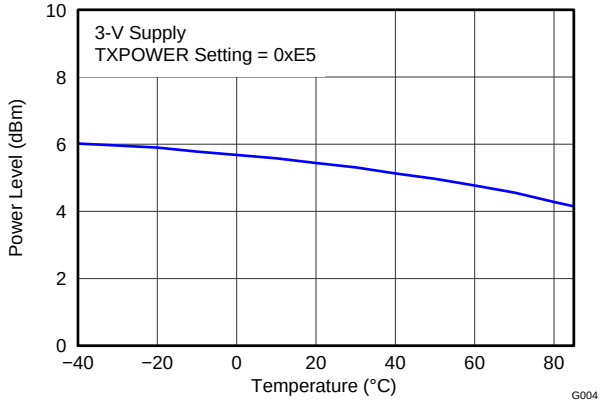


Figure 11.

RX CURRENT vs SUPPLY VOLTAGE

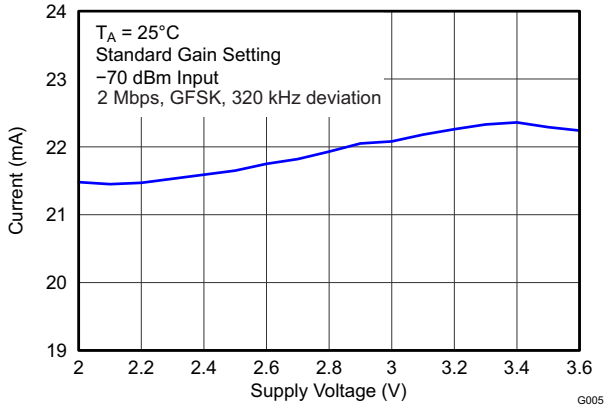


Figure 12.

TX CURRENT vs SUPPLY VOLTAGE

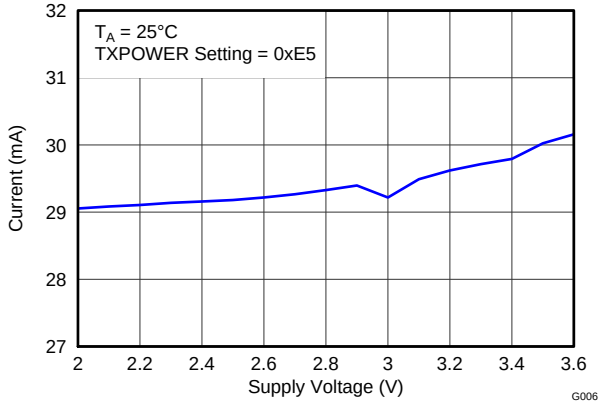


Figure 13.

TYPICAL CHARACTERISTICS (continued)

RX SENSITIVITY vs SUPPLY VOLTAGE

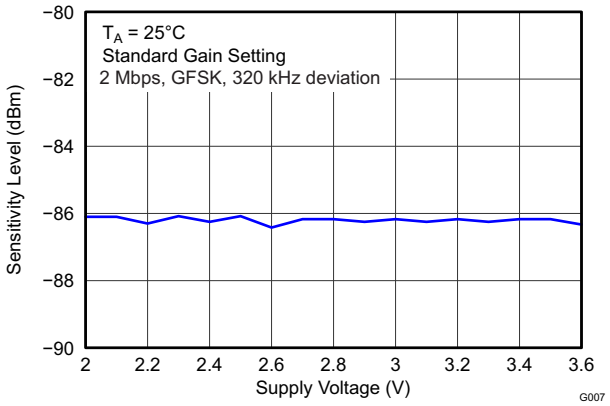


Figure 14.

TX POWER vs SUPPLY VOLTAGE

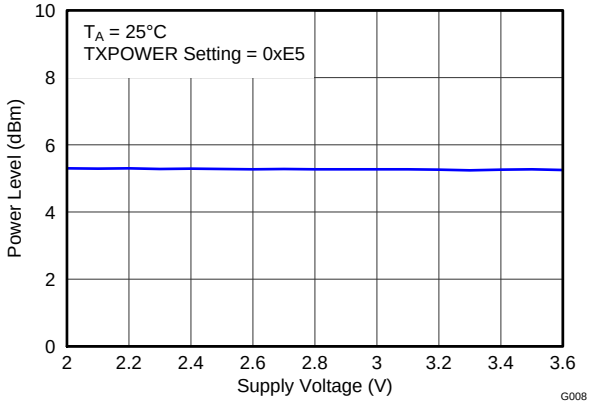


Figure 15.

RX SENSITIVITY vs FREQUENCY

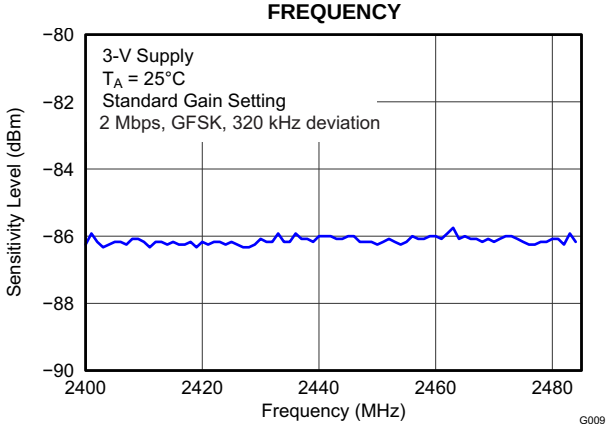


Figure 16.

TX POWER vs FREQUENCY

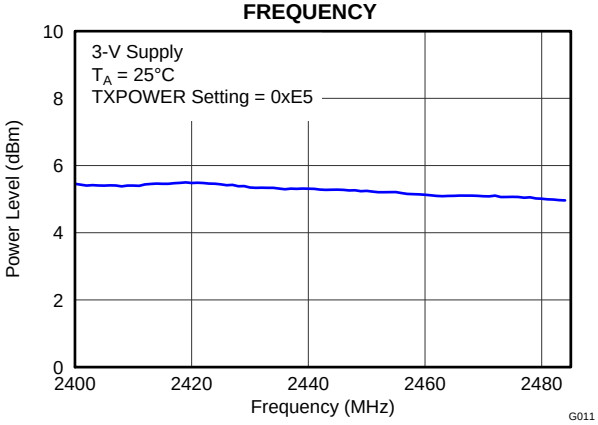


Figure 17.

RX INTERFERER REJECTION (SELECTIVITY) vs INTERFERER FREQUENCY

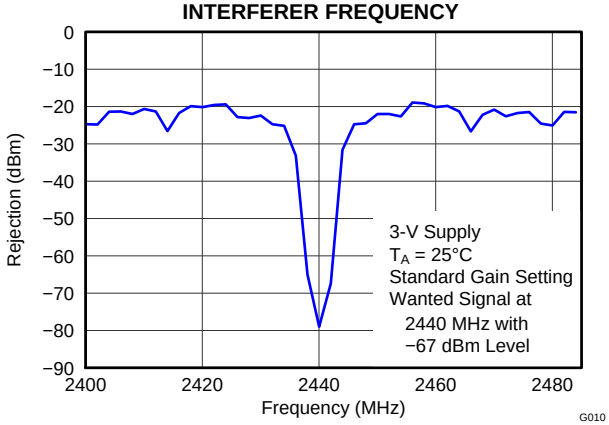


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Table 2. Recommended Output Power Settings(1)

TXPOWER Register Setting	Typical Output Power (dBm)
0xE5	5
0xD5	4
0xC5	3
0xB5	2
0xA5	0
0x95	–2
0x85	–3
0x75	–4
0x65	–6
0x55	–8
0x45	–11
0x35	–13
0x25	–15
0x15	–17
0x05	–20

(1) Measured on Texas Instruments CC2543 EM reference design with TA = 25°C, VDD = 3 V and fc = 2440 MHz. See SWRU283 for recommended register settings.

APPLICATION INFORMATION

Few external components are required for the operation of the CC2543. A typical application circuit is shown in Figure 19. For suggestions of component values other than those listed in Table 3, see reference design CC2543EM. The performance stated in this data sheet is only valid for the CC2543EM reference design. To obtain similar performance, the reference design should be copied as closely as possible.

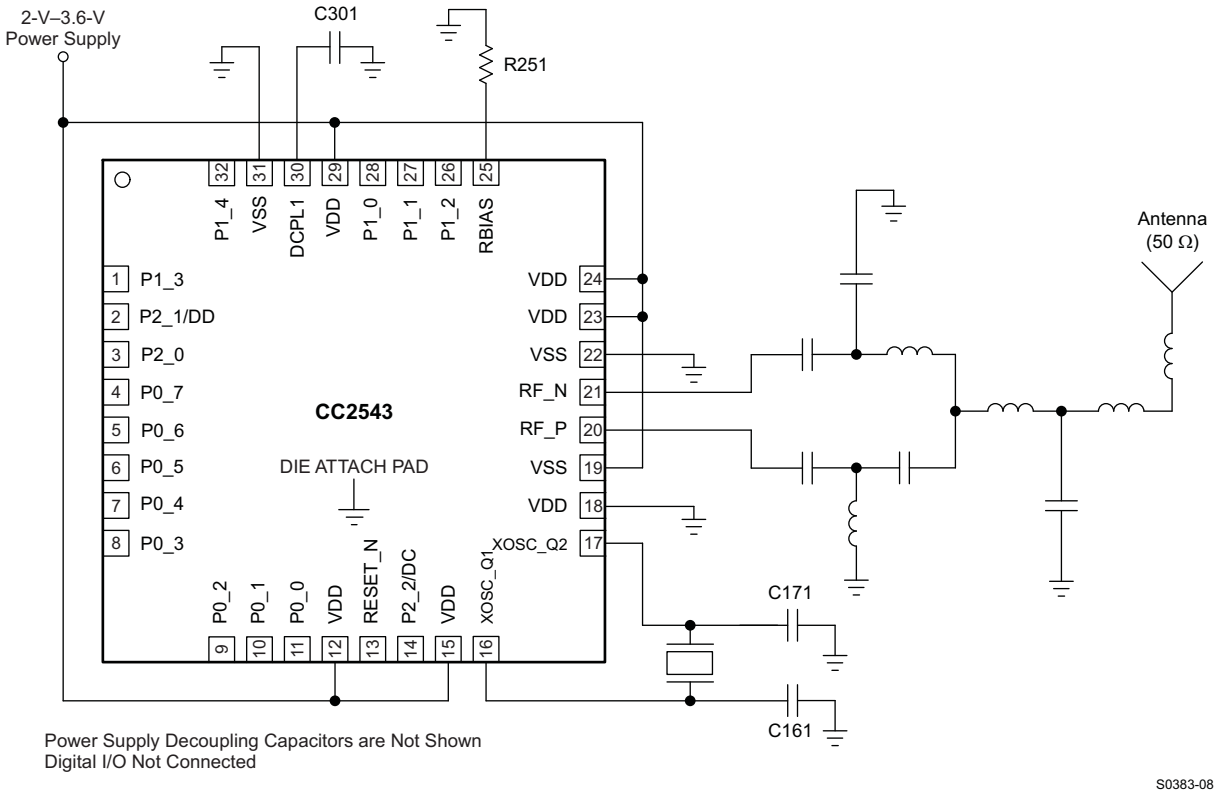


Figure 19. CC2543 Application Circuit

Table 3. Overview of External Components (Excluding Balun, Crystal and Supply Decoupling Capacitors)

COMPONENT	DESCRIPTION	VALUE
C301	Decoupling capacitor for the internal 1.8V digital voltage regulator	1 µF
R251	Precision resistor ±1%, used for internal biasing	56 kΩ

Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. See reference design, CC2543EM, for recommended balun.

Crystal

An external 32-MHz crystal with two loading capacitors is used for the 32-MHz crystal oscillator. The load capacitance seen by the 32-MHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{161}} + \frac{1}{C_{171}}} + C_{parasitic} \quad (1)$$

A series resistor may be used to comply with ESR requirement.

On-Chip 1.8-V Voltage Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires a decoupling capacitor (C301) for stable operation.

Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

REVISION HISTORY

Changes from Original (April 2012) to Revision A — **Page**

- Changed 将数据表的状态从产品预览改为生产数据 1

Changes from Revision A (April 2012) to Revision B — **Page**

- Added Comparator Characteristics specifications 7
- Added ADC Characteristics specifications 8

Changes from Revision B (May 2012) to Revision C — **Page**

- Changed the Temperature coefficient Unit value From: mV/°C To: / 0.1°C 7

Changes from Revision C (August 2012) to Revision D — **Page**

- Changed the Pin Package From: RHM to: RHB 13

Changes from Revision D (November 2012) to Revision E — **Page**

- Changed the ADC CHARACTERISTICS Test Conditions From: VDD is voltage on AVDD5 pin To: VDD is voltage from supply 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2543RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2543	Samples
CC2543RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2543	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

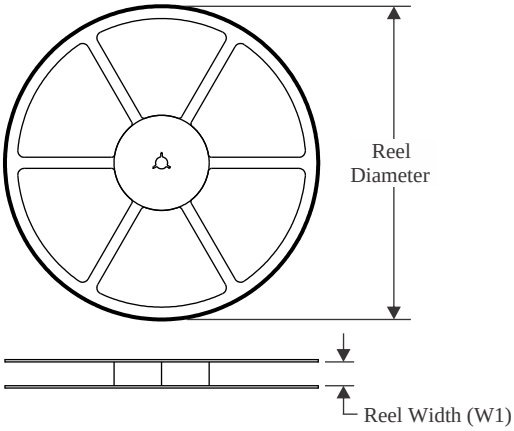
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

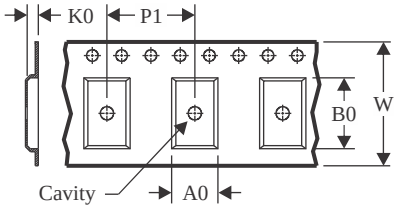
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

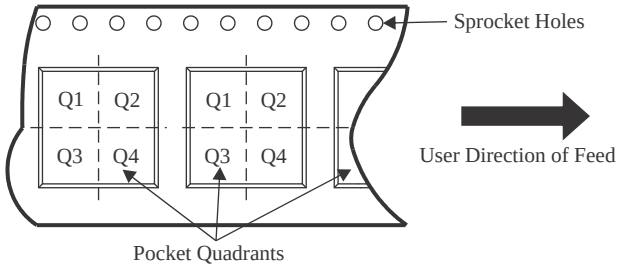


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

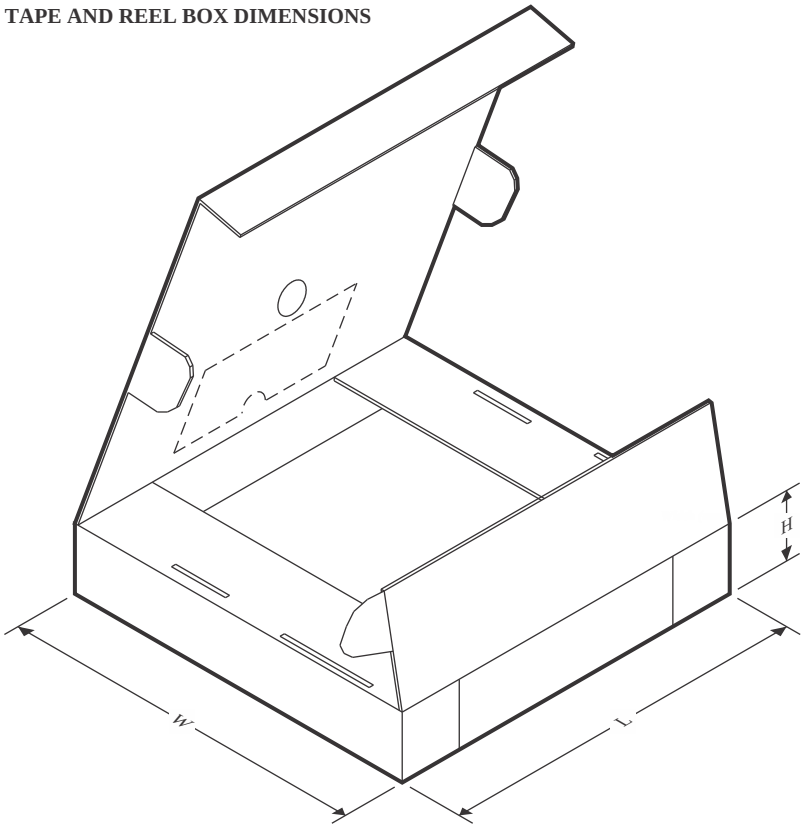
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2543RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2543RHBR	VQFN	RHB	32	3000	350.0	350.0	43.0

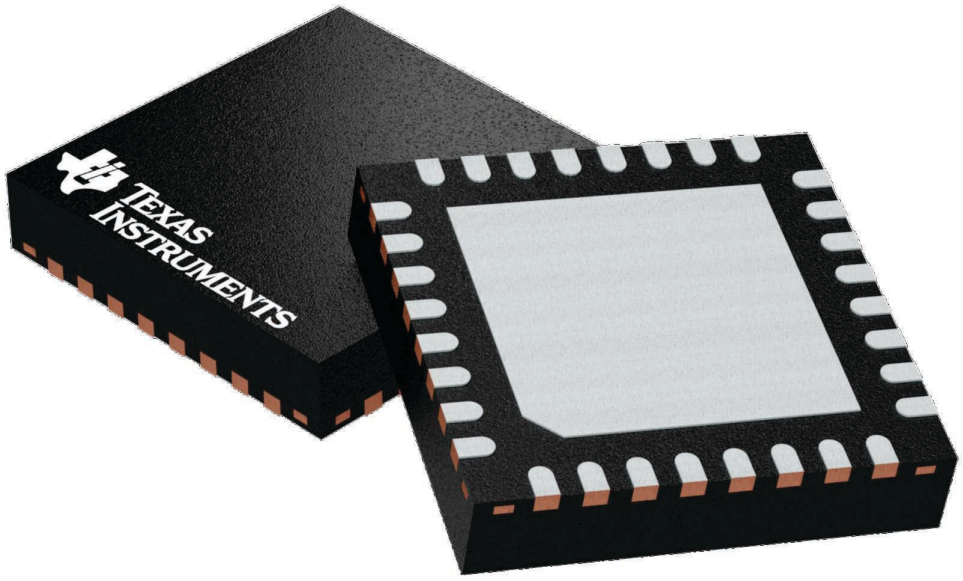
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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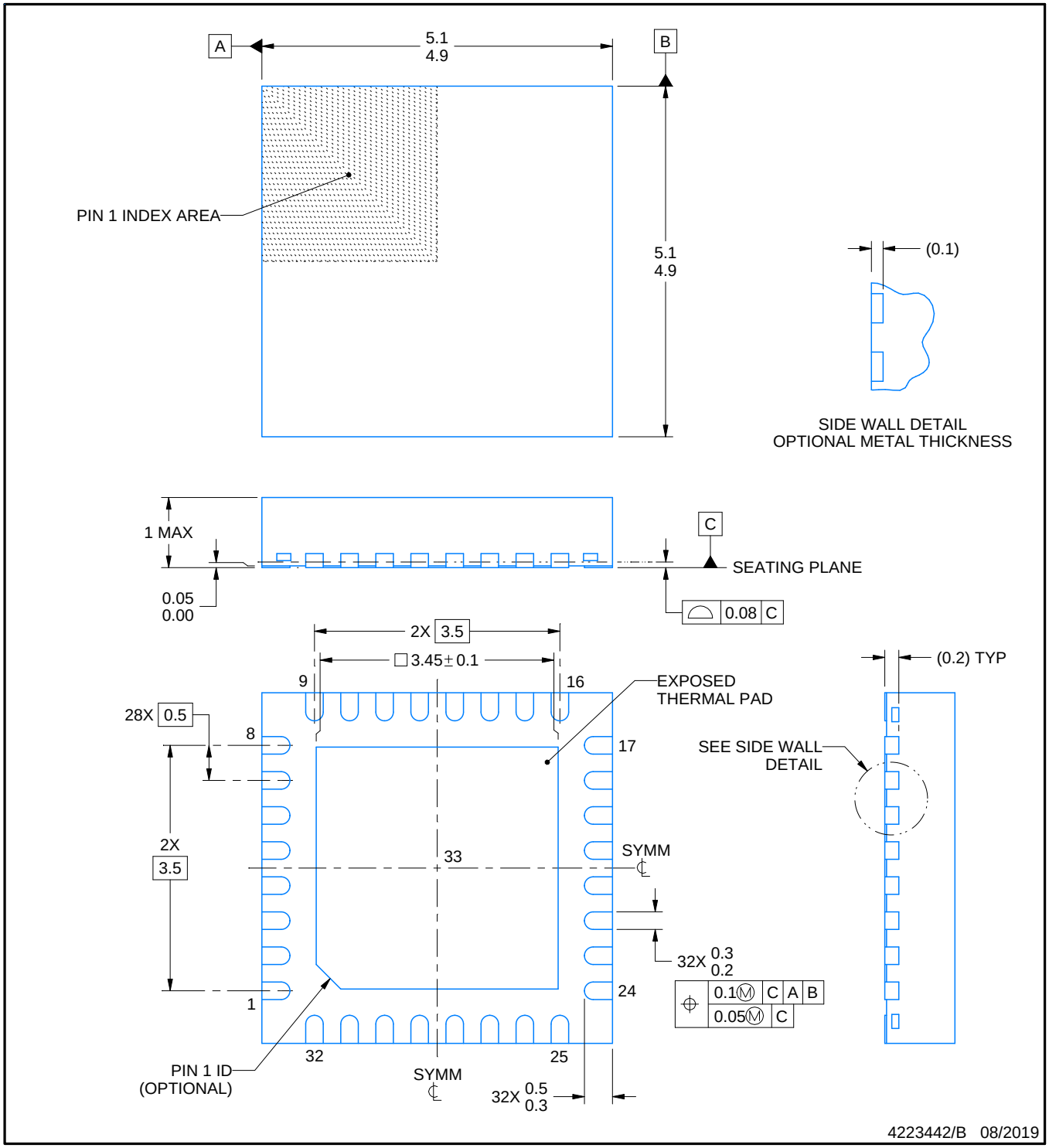
RHB0032E

PACKAGE OUTLINE

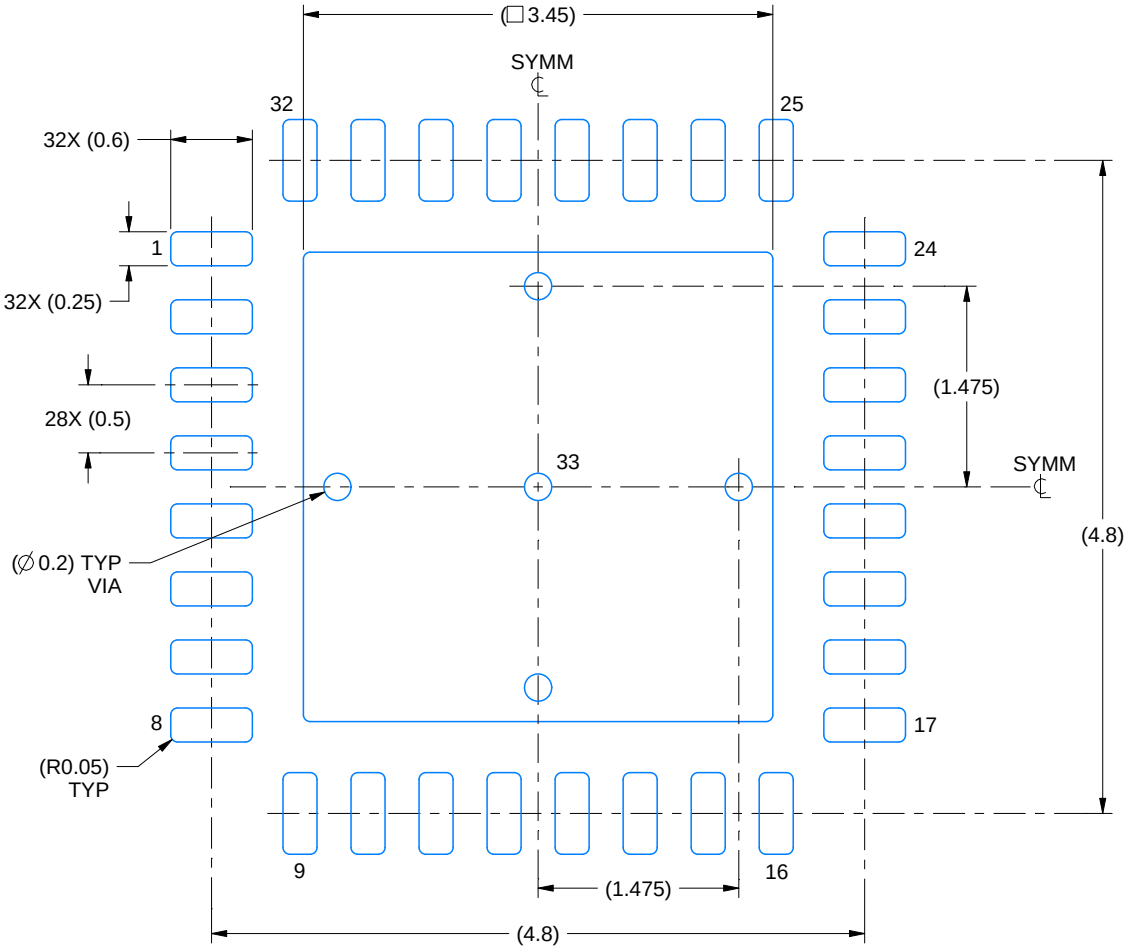
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

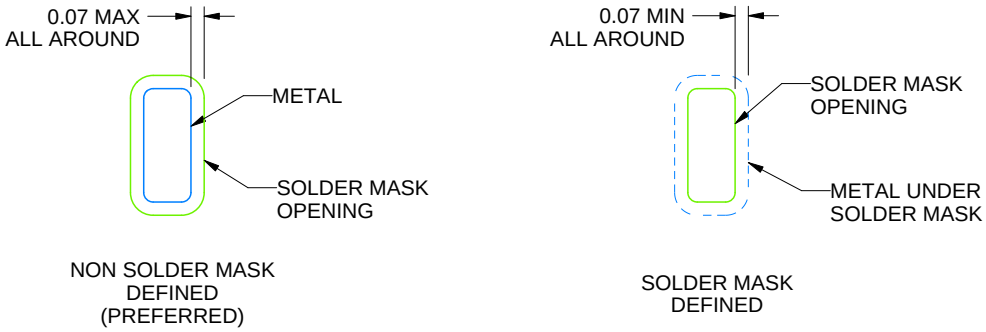


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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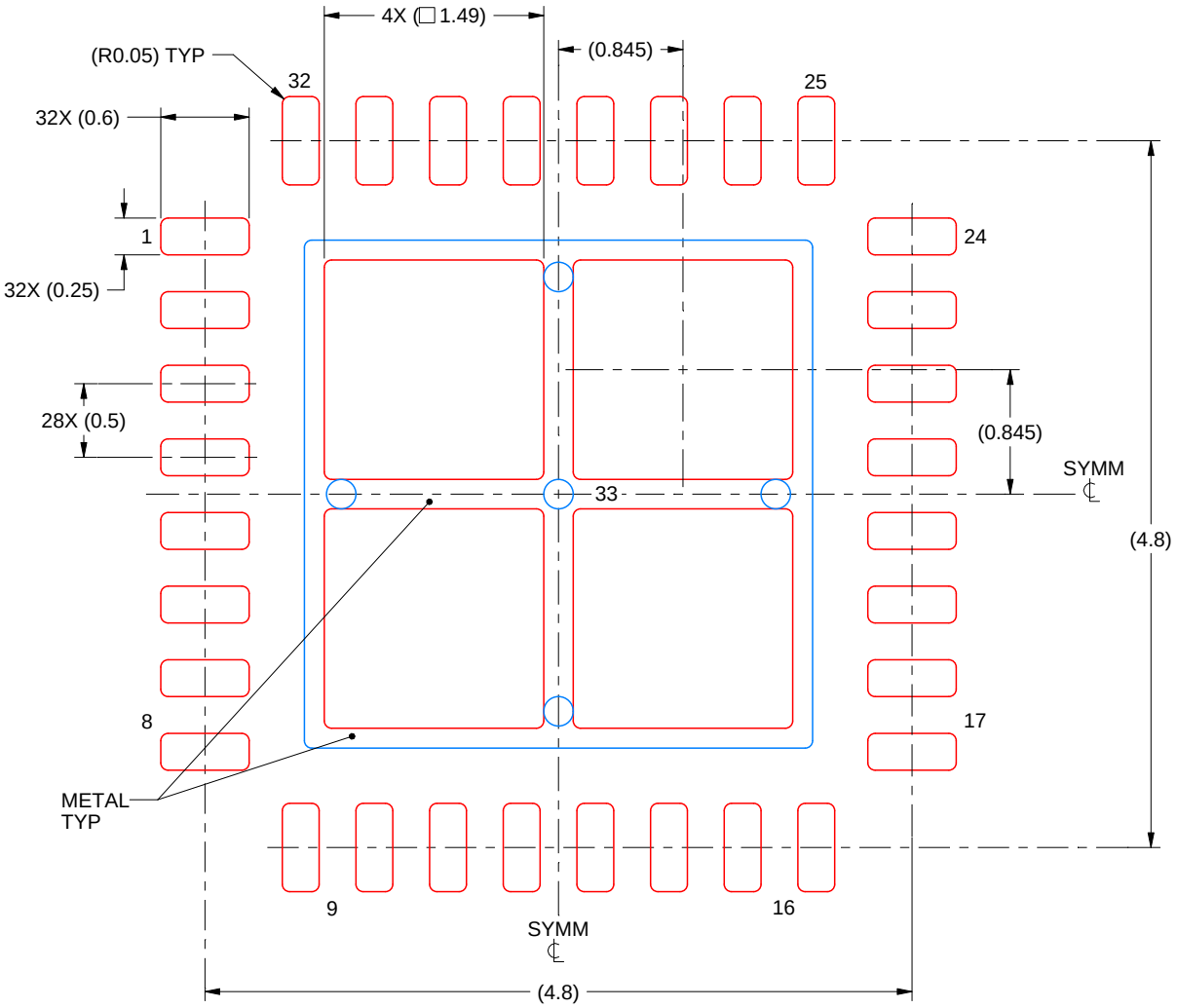
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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