CC2540T 扩展工业温度 *Bluetooth*® 智能无线 MCU

1 器件概述

1.1 特性

- 真正的单芯片蓝牙低能耗 (BLE) 解决方案：CC2540T 既能够运行应用程序，也能够运行 BLE 协议栈，包括可连接各类传感器等元件的外设
- 工作温度最高达 125°C
- 6mm × 6mm 封装
- 射频 (RF)
  - *Bluetooth*®低能耗技术
  - 优异的链路预算（最高可达 97dB）， 支持 不带外部前端的远距离应用
  - 精确的数字接收信号强度指示器 (RSSI)
  - 适用于符合全球射频规范的系统：
    - ETSI EN 300 328 和 EN 300 440 2 类（欧洲）
    - FCC CFR47 第 15 部分（美国）
    - ARIB STD-T66（日本）
- 布局
  - 极少的外部组件
  - 提供参考设计
  - 6mm x 6mm VQFN40 封装
- 低功耗
  - 有源模式 RX 低至 19.6mA
  - 有源模式 TX (–6dBm)：24mA
  - 功率模式 1（3µs 唤醒时间）：235µA
  - 功率模式 2（睡眠定时器打开）：0.9µA
  - 功率模式 3（外部中断）：0.4µA
  - 宽电源电压范围 (2V-3.6V)
  - 在所有功率模式下具有完全 RAM 和寄存器保持
- 兼容 TPS62730，工作模式下功耗较低
  - RX 低至 15.8mA（3V 电源）
  - TX (–6dBm)：18.6mA (3V 电源)
- 微控制器
  - 高性能、低功耗的 8051 微控制器内核
  - 256KB 系统内可编程闪存
  - 8KB SRAM
- 外设
  - 具有 8 通道和可配置分辨率的 12 位模数转换器 (ADC)
  - 集成超低功耗比较器
  - 通用定时器（1 个 16 位，2 个 8 位）
  - 21 个通用 I/O (GPIO) 引脚（19 x 4mA，2 x 20mA）
  - 具有捕捉功能的 32kHz 睡眠定时器
  - 2 个功能强大、支持几种串行协议的通用异步接收发器 (UART)
  - 全速 USB 接口
  - 红外 (IR) 生成电路
  - 功能强大的 5 通道直接内存访问 (DMA)
  - 高级加密标准 (AES) 安全协处理器
  - 电池监视器和温度传感器
  - 每个 CC2540T 均包含唯一的 48 位 IEEE 地址
- 符合针对单模式蓝牙低能耗 (BLE) 解决方案的符合*蓝牙*4.0 协议的堆栈
  - 完全功率优化堆栈，包括控制器和主机
    - GAP：中央设备、外设、观察者或广播者（包括组合角色）
    - 属性协议 (ATT) 和通用属性配置文件 (GATT)：客户端和服务器
    - 对称式对多重处理 (SMP)：AES-128 加密和解密
    - L2CAP
  - 示例 应用 和配置文件
    - 针对 GAP 中心 和外围作用 的一般应用
    - 距离临近、加速计、简单关键字和电池 GATT 服务
  - 多重配置选项
    - 单芯片配置，允许应用在 CC2540T 上运行
    - 针对外部微处理器所运行 应用程序 的网络处理器接口
  - BTool：评估、开发和测试的 Windows PC 应用
- 开发工具
  - CC2540T 迷你开发套件
  - SmartRF™软件
  - 由用于 8051 的 IAR Embedded Workbench™软件提供支持

1.2 应用

- 2.4GHz *蓝牙*低能耗系统
- 照明
- 电机监控
- 接近传感
- 电缆更换
- 电动工具
- 维护
- 无线 HMI 和远程显示
- USB 软件狗
- 智能手机连接

1.3 说明

CC2540T 器件是一款真正具备成本效益的低功耗无线 MCU，适用于*蓝牙*低能耗 应用。CC2540T 可在总物料成本低廉的前提下构建耐用的 BLE 主控或受控节点，工作温度最高可达 125°C。CC2540T 将一款性能出色的 RF 收发器、一个符合行业标准的增强型 8051 MCU、系统内置可编程闪存存储器、8KB RAM 及其他功能强大的支持 特性 及外设组合在一起。CC2540T 适用于要求超低功耗的系统。提供有超低功耗睡眠模式。运行模式间的切换时间短，有助于实现更低功耗。

CC2540TF256 与德州仪器的 (TI) *蓝牙*低能耗协议栈相结合，提供市面上最灵活、最经济高效的单模式*蓝牙*低能耗解决方案。

表 1-1. 器件信息(1)

产品型号	封装	封装尺寸（标称值）
CC2540TF256RHAR	VQFN (40)	6.00mm x 6.00mm
CC2540TF256RHAT	VQFN (40)	6.00mm x 6.00mm

(1) 更多信息请参见节 8，*机械封装和可订购信息*。

1.4 功能方框图

图 1-1 所示为 CC2540T 器件的功能框图。

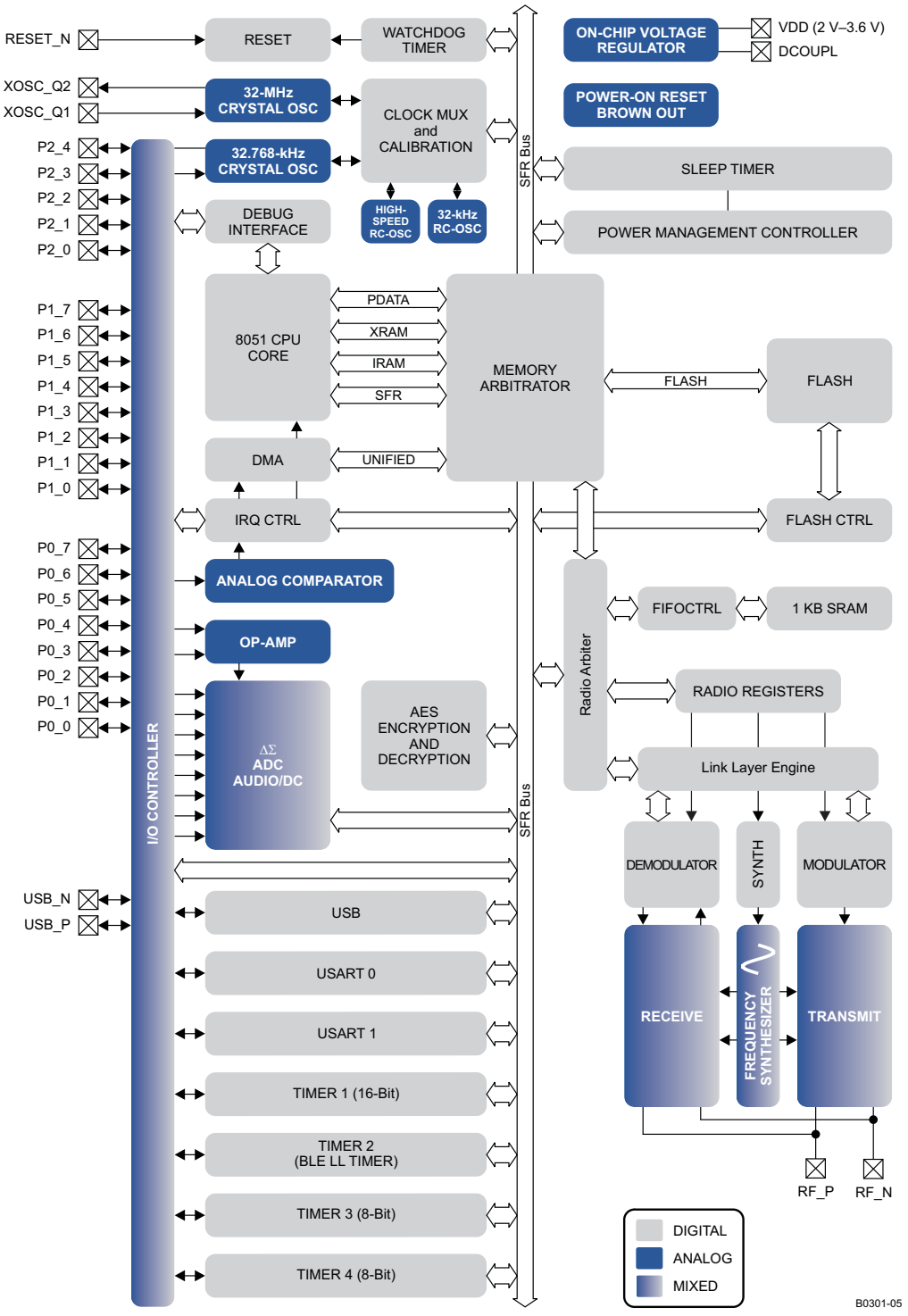


图 **1-1.** 功能方框图

内容

2 修订历史记录

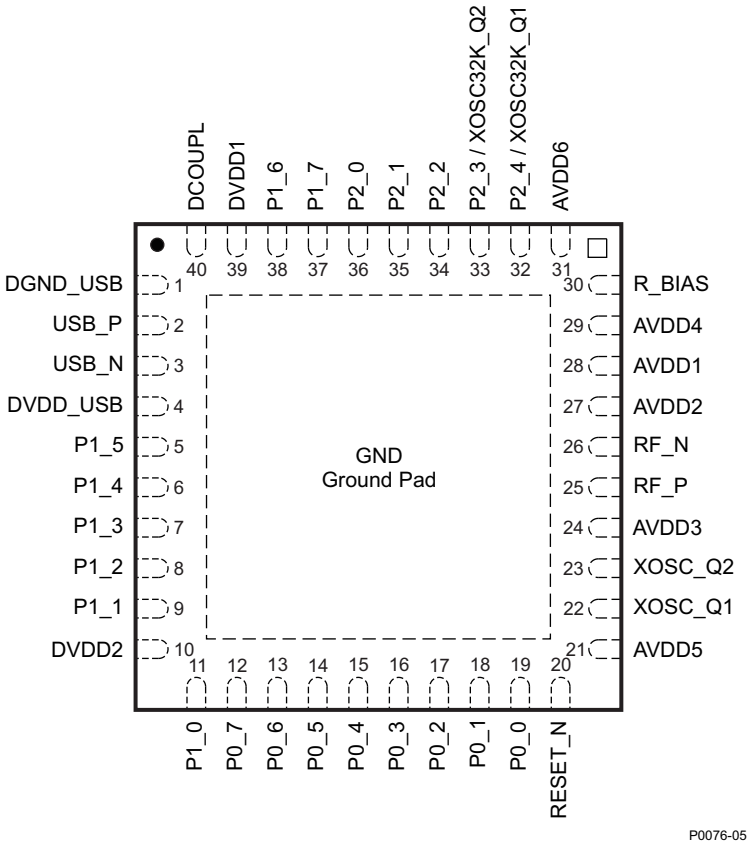
注：之前版本的页码可能与当前版本有所不同。

Changes from July 2, 2015 to November 30, 2015 **Page**

- 已更改 *中的部分项特性* 1
- Changed from *Handling Ratings* table to *ESD Ratings* table 7
- Added MIN value for output power in the *RF Transmit Section* table 10
- Added *Bluetooth Low Energy Light Reference Design* to the document. 27

3 Terminal Configuration and Functions

The CC2540T pinout is shown in Figure 3-1, and a short description of the pins follows in *Section 3.1*.



NOTE: The exposed ground pad must be connected to a solid ground plane, as this is the ground connection for the chip.

Figure 3-1. CC2540T
RHA Package (VQFN)
Top View

3.1 Pin Attributes

Table 3-1. Pin Attributes

NAME	NO.	TYPE	DESCRIPTION
AVDD1	28	Power (analog)	2-V to 3.6-V analog power-supply connection
AVDD2	27	Power (analog)	2-V to 3.6-V analog power-supply connection
AVDD3	24	Power (analog)	2-V to 3.6-V analog power-supply connection
AVDD4	29	Power (analog)	2-V to 3.6-V analog power-supply connection
AVDD5	21	Power (analog)	2-V to 3.6-V analog power-supply connection
AVDD6	31	Power (analog)	2-V to 3.6-V analog power-supply connection
DCOUPL	40	Power (digital)	1.8-V digital power-supply decoupling. Do not use for supplying external circuits.
DGND_USB	1	Ground pin	Connect to GND
DVDD_USB	4	Power (digital)	2-V to 3.6-V digital power-supply connection
DVDD1	39	Power (digital)	2-V to 3.6-V digital power-supply connection
DVDD2	10	Power (digital)	2-V to 3.6-V digital power-supply connection
GND	—	Ground	The ground pad must be connected to a solid ground plane.
P0_0	19	Digital I/O	Port 0.0
P0_1	18	Digital I/O	Port 0.1
P0_2	17	Digital I/O	Port 0.2
P0_3	16	Digital I/O	Port 0.3
P0_4	15	Digital I/O	Port 0.4
P0_5	14	Digital I/O	Port 0.5
P0_6	13	Digital I/O	Port 0.6
P0_7	12	Digital I/O	Port 0.7
P1_0	11	Digital I/O	Port 1.0: 20-mA drive capability
P1_1	9	Digital I/O	Port 1.1: 20-mA drive capability
P1_2	8	Digital I/O	Port 1.2
P1_3	7	Digital I/O	Port 1.3
P1_4	6	Digital I/O	Port 1.4
P1_5	5	Digital I/O	Port 1.5
P1_6	38	Digital I/O	Port 1.6
P1_7	37	Digital I/O	Port 1.7
P2_0	36	Digital I/O	Port 2.0
P2_1	35	Digital I/O	Port 2.1
P2_2	34	Digital I/O	Port 2.2
P2_3/ XOSC32K_Q2	33	Digital I/O, Analog I/O	Port 2.3/32.768 kHz XOSC
P2_4/ XOSC32K_Q1	32	Digital I/O, Analog I/O	Port 2.4/32.768 kHz XOSC
RBIAS	30	Analog I/O	External precision bias resistor for reference current
RESET_N	20	Digital input	Reset, active-low
RF_N	26	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	25	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
USB_N	3	Digital I/O	USB N
USB_P	2	Digital I/O	USB P
XOSC_Q1	22	Analog I/O	32-MHz crystal oscillator pin 1 or external-clock input
XOSC_Q2	23	Analog I/O	32-MHz crystal oscillator pin 2

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage	All supply pins must have the same voltage	–0.3	3.9	V
Voltage on any digital pin		–0.3	VDD + 0.3, ≤ 3.9	V
Input RF level			10	dBm
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

4.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge (ESD) performance	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001(1)		±2000	V
		Charged Device Model (CDM), per JESD22-C101(2)	All pins	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature range, T_A	–40	125	°C
Operating supply voltage	2	3.6	V

4.4 Electrical Characteristics

Measured on the TI CC2540 EM reference design with T_A = 25°C and V_{DD} = 3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{core}	Core current consumption	Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, BOD and sleep timer active; RAM and register retention		235		µA
		Power mode 2. Digital regulator off; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, and sleep timer active; RAM and register retention		0.9		
		Power mode 3. Digital regulator off; no clocks; POR active; RAM and register retention		0.4		
		Low MCU activity: 32-MHz XOSC running. No radio or peripherals. No flash access, no RAM access.		6.7		mA
I_{peri}	Peripheral current consumption(1)	Timer 1. Timer running, 32-MHz XOSC used		90		µA
		Timer 2. Timer running, 32-MHz XOSC used		90		
		Timer 3. Timer running, 32-MHz XOSC used		60		
		Timer 4. Timer running, 32-MHz XOSC used		70		
		Sleep timer, including 32.753-kHz RCOSC		0.6		
		ADC, when converting		1.2		mA

(1) Adds to core current I_{core} for each peripheral unit activated.

4.5 Thermal Resistance Characteristics for RHA Package

NAME	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s)(3)
$R\Theta_{JC}$	Junction-to-case	16.1	0.00
$R\Theta_{JB}$	Junction-to-board	5.5	0.00
$R\Theta_{JA}$	Junction-to-free air	30.6	0.00
$R\Theta_{JMA}$	Junction-to-moving air	0.2	0.00
Psi_{JT}	Junction-to-package top	5.4	0.00
Psi_{JB}	Junction-to-board	1.0	0.00

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70ºC is assumed.
(3) m/s = meters per second.

4.6 General Characteristics

Measured on the TI CC2540 EM reference design with T_A = 25°C and V_{DD} = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP AND TIMING					
Power mode 1 → Active	Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC		4		µs
Power mode 2 or 3 → Active	Digital regulator off, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of regulator and 16-MHz RCOSC		120		µs
Active → TX or RX	Crystal ESR = 16 Ω. Initially running on 16-MHz RCOSC, with 32-MHz XOSC OFF		410		µs
	With 32-MHz XOSC initially on		160		µs
RX/TX turnaround			150		µs
RADIO PART					
RF frequency range	Programmable in 2-MHz steps	2402		2480	MHz
Data rate and modulation format	1 Mbps, GFSK, 250-kHz deviation				

4.7 RF Receive Section

Measured on the TI CC2540 EM reference design with T_A = 25°C, V_{DD} = 3 V, f_c = 2440 MHz
1 Mbps, GFSK, 250-kHz deviation, *Bluetooth* low energy mode, and 0.1% BER(1).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity(2)	High-gain mode		–93		dBm
Receiver sensitivity(2)	Standard mode		–87		dBm
Saturation(3)			6		dBm
Co-channel rejection(3)			–5		dB
Adjacent-channel rejection(3)	±1 MHz		–5		dB
Alternate-channel rejection(3)	±2 MHz		30		dB
Blocking(3)			–30		dBm
Frequency error tolerance(4)	Including both initial tolerance and drift	–250		250	kHz
Symbol rate error tolerance(5)		–80		80	ppm
Spurious emission. Only largest spurious emission stated within each band.	Conducted measurement with a 50-Ω single-ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–75		dBm
Current consumption	RX mode, standard mode, no peripherals active, low MCU activity, MCU at 250 kHz		19.6		mA
	RX mode, high-gain mode, no peripherals active, low MCU activity, MCU at 250 kHz		22.1		
	RX mode, high-gain mode, no peripherals active, low MCU activity, MCU at 250 kHz; T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V, and f_c = 2402 MHz to 2480 MHz			30.5	

(1) 0.1% BER maps to 30.8% PER
(2) The receiver sensitivity setting is programmable using a TI BLE stack vendor-specific API command. The default value is standard mode.
(3) Results based on standard gain mode
(4) Difference between center frequency of the received RF signal and local oscillator frequency
(5) Difference between incoming symbol rate and the internally generated symbol rate

4.8 RF Transmit Section

Measured on the TI CC2540 EM reference design with T_A = 25°C, V_{DD} = 3 V and f_c = 2440 MHz.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power	Delivered to a single-ended 50-Ω load through a balun using maximum recommended output power setting	1	4		dBm
	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting		–23		
Programmable output power range	Delivered to a single-ended 50 Ω load through a balun		27		dB
Spurious emissions	Conducted measurement with a 50-Ω single-ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66 (1)		–41		dBm
Current consumption	TX mode, –23-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		21.1		mA
	TX mode, –6-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		23.8		
	TX mode, 0-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		27		
	TX mode, 4-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		31.6		
	TX mode, 4-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz; T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V, and f_c = 2402 MHz to 2480 MHz			39.6	
Optimum load impedance	Differential impedance as seen from the RF port (RF_P and RF_N) toward the antenna		70 + j30		Ω

(1) Designs with antenna connectors that require conducted ETSI compliance at 64 MHz should insert an LC resonator in front of the antenna connector. Use a 1.6-nH inductor in parallel with a 1.8-pF capacitor. Connect both from the signal trace to a good RF ground.

4.9 Current Consumption With TPS62730

Measured on the TI CC2540TPS62730 EM reference design with T_A = 25°C, V_{DD} = 3 V, and f_c = 2440 MHZ.
1 Mbps, GFSK, 250-kHz deviation, *Bluetooth* low energy mode, 1% BER (1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current consumption	RX mode, standard mode, no peripherals active, low MCU activity, MCU at 1 MHZ		15.8		mA
	RX mode, high-gain mode, no peripherals active, low MCU activity, MCU at 1 MHZ		17.8		
	TX mode, –23-dBm output power, no peripherals active, low MCU activity, MCU at 1 MHZ		16.5		
	TX mode, –6-dBm output power, no peripherals active, low MCU activity, MCU at 1 MHZ		18.6		
	TX mode, 0-dBm output power, no peripherals active, low MCU activity, MCU at 1 MHZ		21		
	TX mode, 4-dBm output power, no peripherals active, low MCU activity, MCU at 1 MHZ		24.6		

(1) 0.1% BER maps to 30.8% PER

4.10 32-MHz Crystal Oscillator

Measured on the TI CC2540 EM reference design with T_A = 25°C and V_{DD} = 3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32		MHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance		6		60	Ω
C_0	Crystal shunt capacitance		1		7	pF
C_L	Crystal load capacitance		10		16	pF
	Start-up time			0.25		ms
	Power-down guard time	The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load.	3			ms

(1) Including aging and temperature dependency, as specified by [1]

4.11 32.768-kHz Crystal Oscillator

Measured on the TI CC2540 EM reference design with T_A = 25°C and V_{DD} = 3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32.768		kHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance			40	130	kΩ
C_0	Crystal shunt capacitance			0.9	2	pF
C_L	Crystal load capacitance			12	16	pF
	Start-up time			0.4		s

(1) Including aging and temperature dependency, as specified by [1]

4.12 32-kHz RC Oscillator

Measured on the TI CC2540 EM reference design with T_A = 25°C and V_{DD} = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency(1)			32.753		kHz
Frequency accuracy after calibration			±0.2%		
Temperature coefficient(2)			0.4		%/°C
Supply-voltage coefficient(3)			3		%/V
Calibration time(4)			2		ms

(1) The calibrated 32-kHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 977.
(2) Frequency drift when temperature changes after calibration
(3) Frequency drift when supply voltage changes after calibration
(4) When the 32-kHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEPCMD.OSC32K_CALDIS is set to 0.

4.13 16-MHz RC Oscillator

Measured on the TI CC2540 EM reference design with T_A = 25°C and V_{DD} = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency(1)			16		MHz
Uncalibrated frequency accuracy			±18%		
Calibrated frequency accuracy			±0.6%		
Start-up time			10		µs
Initial calibration time(2)			50		µs

(1) The calibrated 16-MHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 2.
(2) When the 16-MHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEPCMD.OSC_PD is set to 0.

4.14 RSSI Characteristics

Measured on the TI CC2540 EM reference design with T_A = 25°C and V_{DD} = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Useful RSSI range(1)	High-gain mode		–99 to –44		dBm
	Standard mode		–90 to –35		
Absolute uncalibrated RSSI accuracy(1)	High-gain mode		±4		dB
Step size (LSB value)			1		dB

(1) Assuming CC2540 EM reference design. Other RF designs give an offset from the reported value.

4.15 Frequency Synthesizer Characteristics

Measured on the TI CC2540 EM reference design with T_A = 25°C, V_{DD} = 3 V and f_c = 2440 MHz.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier	At ±1-MHz offset from carrier		–109		dBc/Hz
	At ±3-MHz offset from carrier		–112		
	At ±5-MHz offset from carrier		–119		

4.16 Analog Temperature Sensor

Measured on the TI CC2540 EM reference design with T_A = 25°C and V_{DD} = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output	Measured using integrated ADC, internal band-gap voltage reference, and maximum resolution		1480		12-bit
Temperature coefficient			4.5		/ 1°C
Voltage coefficient			1		/ 0.1 V
Initial accuracy without calibration			±10		°C
Accuracy using 1-point calibration			±5		°C
Current consumption when enabled			0.5		mA

4.17 Comparator Characteristics

T_A = 25°C, V_{DD} = 3 V. All measurement results are obtained using the CC2540T reference designs, post-calibration.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common-mode maximum voltage			VDD		V
Common-mode minimum voltage			–0.3		
Input offset voltage			1		mV
Offset versus temperature			16		µV/°C
Offset versus operating voltage			4		mV/V
Supply current			230		nA
Hysteresis			0.15		mV

4.18 ADC Characteristics

T_A = 25°C and V_{DD} = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage	VDD is voltage on AVDD5 pin	0		VDD	V
	External reference voltage	VDD is voltage on AVDD5 pin	0		VDD	V
	External reference voltage differential	VDD is voltage on AVDD5 pin	0		VDD	V
	Input resistance, signal	Simulated using 4-MHz clock speed		197		kΩ
	Full-scale signal(1)	Peak-to-peak, defines 0 dBFS		2.97		V
ENOB(1)	Effective number of bits	Single-ended input, 7-bit setting		5.7		bits
		Single-ended input, 9-bit setting		7.5		
		Single-ended input, 10-bit setting		9.3		
		Single-ended input, 12-bit setting		10.3		
		Differential input, 7-bit setting		6.5		
		Differential input, 9-bit setting		8.3		
		Differential input, 10-bit setting		10		
		Differential input, 12-bit setting		11.5		
		10-bit setting, clocked by RCOSC		9.7		
		12-bit setting, clocked by RCOSC		10.9		
	Useful power bandwidth	7-bit setting, both single and differential		0–20		kHz
THD	Total harmonic distortion	Single ended input, 12-bit setting, –6 dBFS(1)		–75.2		dB
		Differential input, 12-bit setting, –6 dBFS(1)		–86.6		
	Signal to nonharmonic ratio	Single-ended input, 12-bit setting(1)		70.2		dB
		Differential input, 12-bit setting(1)		79.3		
		Single-ended input, 12-bit setting, –6 dBFS(1)		78.8		
		Differential input, 12-bit setting, –6 dBFS(1)		88.9		
CMRR	Common-mode rejection ratio	Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		>84		dB
	Crosstalk	Single ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		>84		dB
	Offset	Midscale		–3		mV
	Gain error			0.68%		
DNL	Differential nonlinearity	12-bit setting, mean(1)		0.05		LSB
		12-bit setting, maximum(1)		0.9		
INL	Integral nonlinearity	12-bit setting, mean(1)		4.6		LSB
		12-bit setting, maximum(1)		13.3		
		12-bit setting, mean, clocked by RCOSC		10		
		12-bit setting, max, clocked by RCOSC		29		
SINAD (–THD+N)	Signal-to-noise-and-distortion	Single ended input, 7-bit setting(1)		35.4		dB
		Single ended input, 9-bit setting(1)		46.8		
		Single ended input, 10-bit setting(1)		57.5		
		Single ended input, 12-bit setting(1)		66.6		
		Differential input, 7-bit setting(1)		40.7		
		Differential input, 9-bit setting(1)		51.6		
		Differential input, 10-bit setting(1)		61.8		
		Differential input, 12-bit setting(1)		70.8		

(1) Measured with 300-Hz sine-wave input and VDD as reference.

ADC Characteristics *(continued)*

T_A = 25°C and V_{DD} = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion time	7-bit setting		20		µs
	9-bit setting		36		
	10-bit setting		68		
	12-bit setting		132		
Power consumption			1.2		mA
Internal reference VDD coefficient			4		mV/V
Internal reference temperature coefficient			0.4		mV/10°C
Internal reference voltage			1.24		V

4.19 Control Input AC Characteristics

T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System clock, f_{SYSCLK} $t_{SYSCLK} = 1 / f_{SYSCLK}$	The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used.	16		32	MHz
RESET_N low duration	See item 1 in Figure 4-1. This is the shortest pulse that is recognized as a complete reset pin request. Note that shorter pulses may be recognized but do not lead to complete reset of all modules within the chip.	1			µs
Interrupt pulse duration	See item 2 in Figure 4-1. This is the shortest pulse that is recognized as an interrupt request.	20			ns

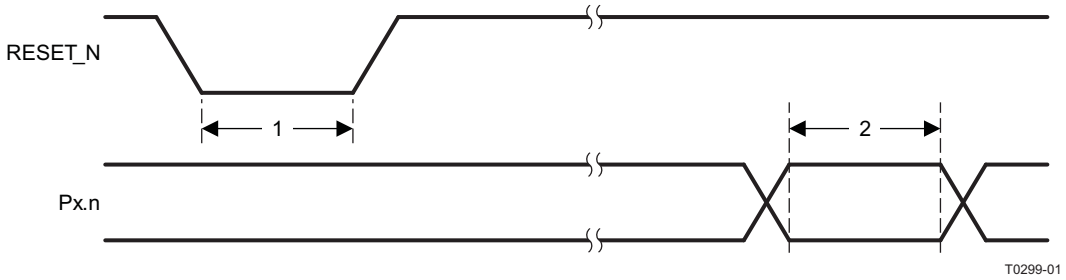


Figure 4-1. Control Input AC Characteristics

4.20 SPI AC Characteristics

T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	SCK period	Master, RX and TX	250			ns
		Slave, RX and TX	250			
	SCK duty cycle	Master		50%		
t_2	SSN low to SCK	Master	63			ns
		Slave	63			
t_3	SCK to SSN high	Master	63			ns
		Slave	63			
t_4	MOSI early out	Master, load = 10 pF			7	ns
t_5	MOSI late out	Master, load = 10 pF			10	ns
t_6	MISO setup	Master	90			ns
t_7	MISO hold	Master	10			ns
	SCK duty cycle	Slave		50%		ns
t_{10}	MOSI setup	Slave	35			ns
t_{11}	MOSI hold	Slave	10			ns
t_9	MISO late out	Slave, load = 10 pF			95	ns
	Operating frequency	Master, TX only			8	MHz
		Master, RX and TX			4	
		Slave, RX only			8	
		Slave, RX and TX			4	

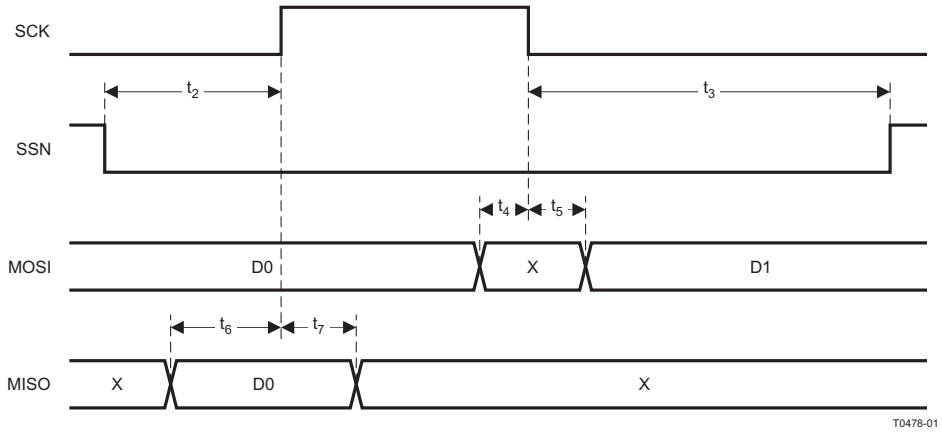


Figure 4-2. SPI Master AC Characteristics

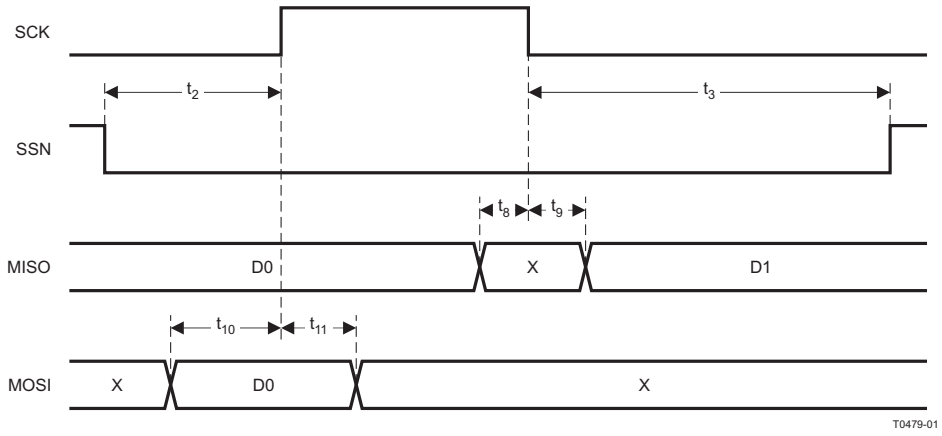


Figure 4-3. SPI Slave AC Characteristics

4.21 Debug Interface AC Characteristics

T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk_dbg}	Debug clock frequency (see Figure 4-4)				12	MHz
t_1	Allowed high pulse on clock (see Figure 4-4)		35			ns
t_2	Allowed low pulse on clock (see Figure 4-4)		35			ns
t_3	EXT_RESET_N low to first falling edge on debug clock (see Figure 4-6)		167			ns
t_4	Falling edge on clock to EXT_RESET_N high (see Figure 4-6)		83			ns
t_5	EXT_RESET_N high to first debug command (see Figure 4-6)		83			ns
t_6	Debug data setup (see Figure 4-5)		2			ns
t_7	Debug data hold (see Figure 4-5)		4			ns
t_8	Clock-to-data delay (see Figure 4-5)	Load = 10 pF			30	ns

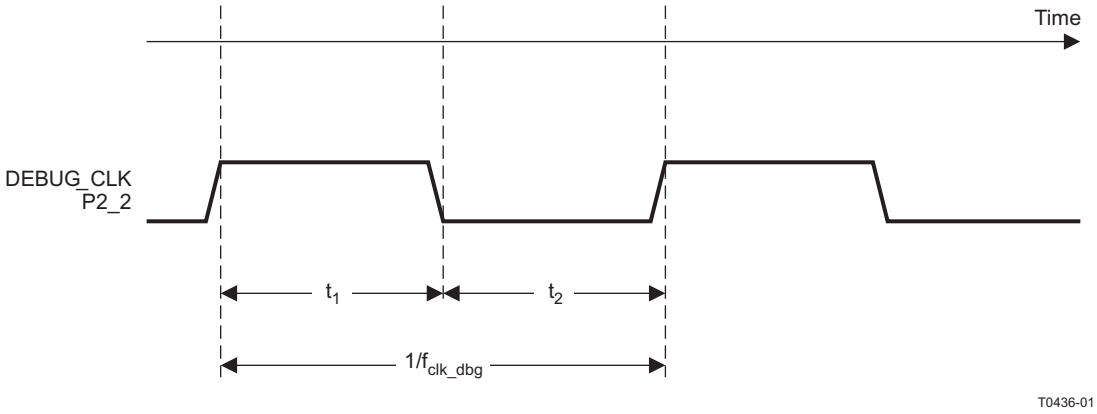


Figure 4-4. Debug Clock–Basic Timing

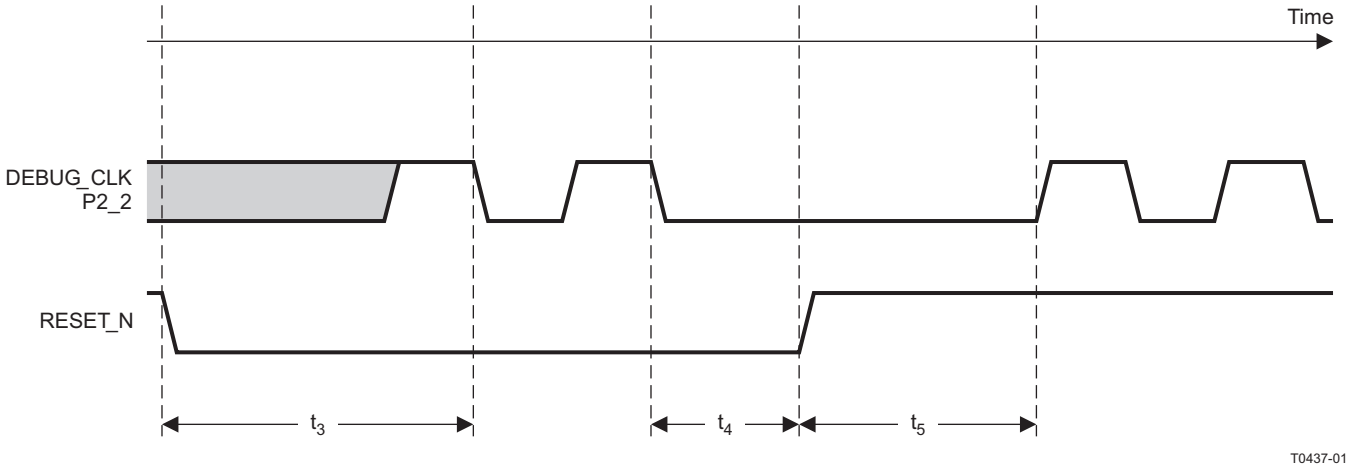


Figure 4-5. Debug Enable Timing

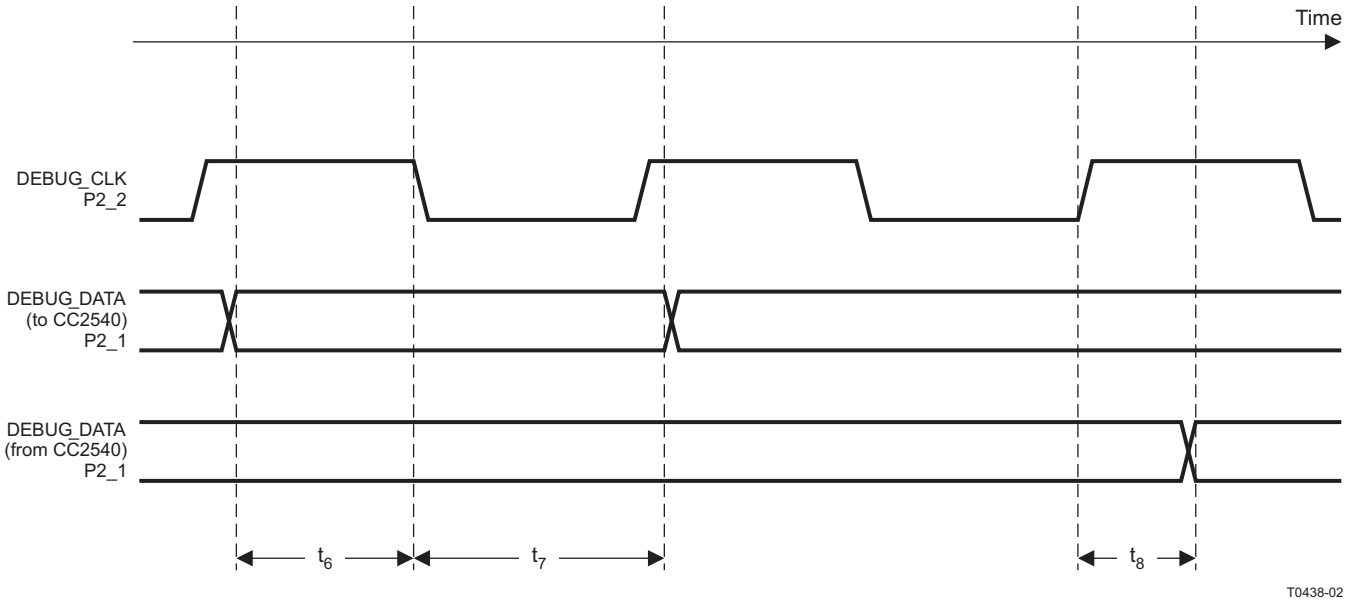


Figure 4-6. Data Setup and Hold Timing

4.22 Timer Inputs AC Characteristics

T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V

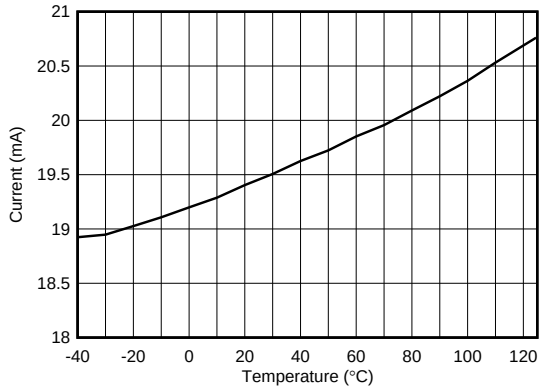
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capture pulse duration	Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate at the current system clock rate (16 MHz or 32 MHz).	1.5			t_{SYSCLK}

4.23 DC Characteristics

T_A = 25°C, V_{DD} = 3 V

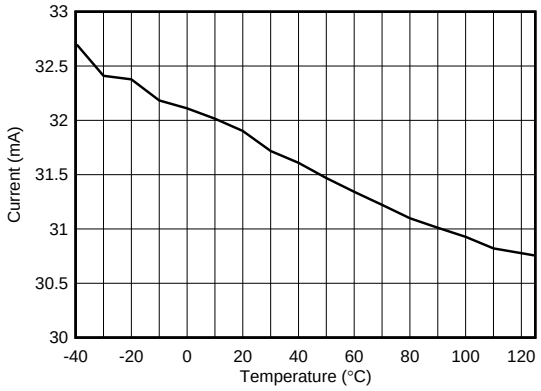
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.5			V
Logic-0 input current	Input equals 0 V	–50		50	nA
Logic-1 input current	Input equals VDD	–50		50	nA
I/O-pin pullup and pulldown resistors			20		kΩ
Logic-0 output voltage, 4-mA pins	Output load 4 mA			0.5	V
Logic-1 output voltage, 4-mA pins	Output load 4 mA	2.4			V

4.24 Typical Characteristics



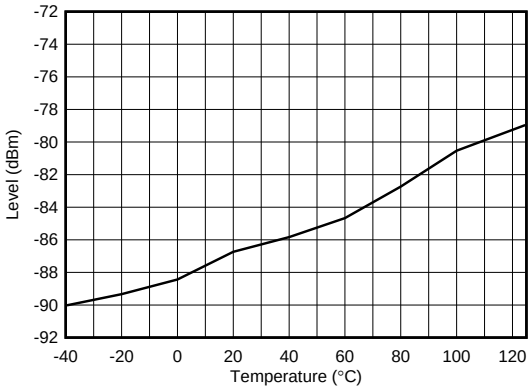
Gain = Standard Setting
Input = –70 dBm
V_{CC} = 3 V

Figure 4-7. RX Current in Wait for Sync vs Temperature



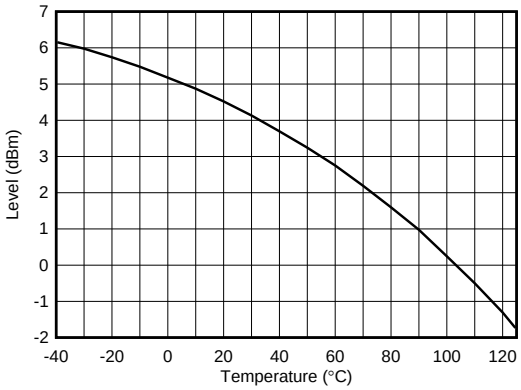
TX Power Setting = 4 dBm
V_{CC} = 3 V

Figure 4-8. TX Current vs Temperature



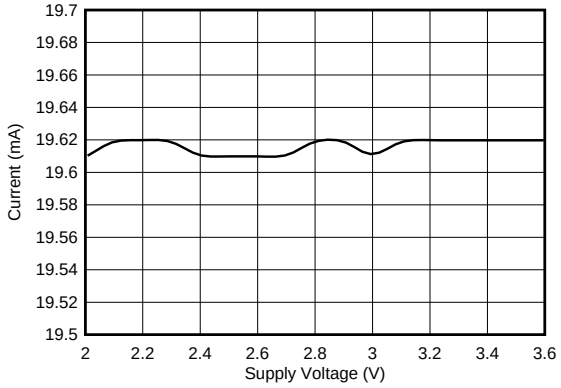
Gain = Standard Setting
V_{CC} = 3 V

Figure 4-9. RX Sensitivity vs Temperature



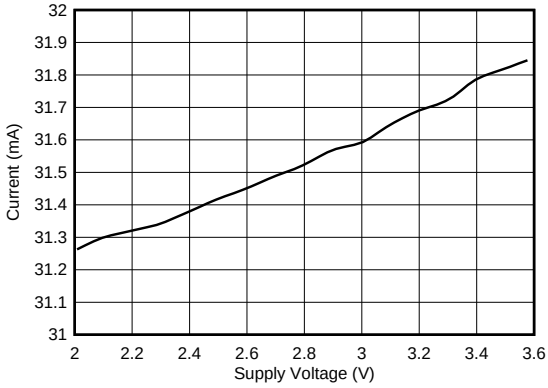
TX Power Setting = 4 dBm
V_{CC} = 3 V

Figure 4-10. TX Power vs Temperature



Gain = Standard Setting
Input = –70 dBm
T_A = 25°C

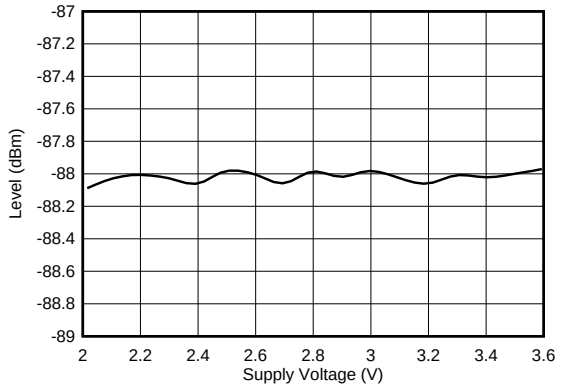
Figure 4-11. RX Current in Wait for Sync vs Supply Voltage



T_A = 25°C
TX Power Setting = 4 dBm

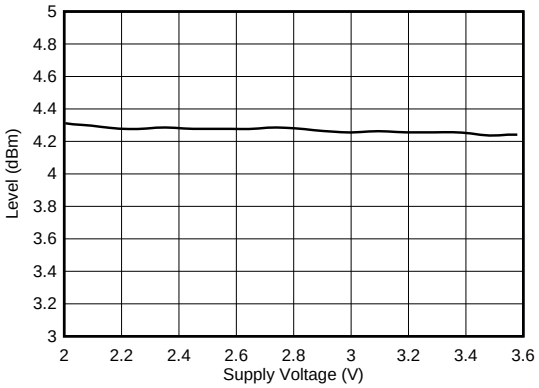
Figure 4-12. TX Current vs Supply Voltage

Typical Characteristics *(continued)*



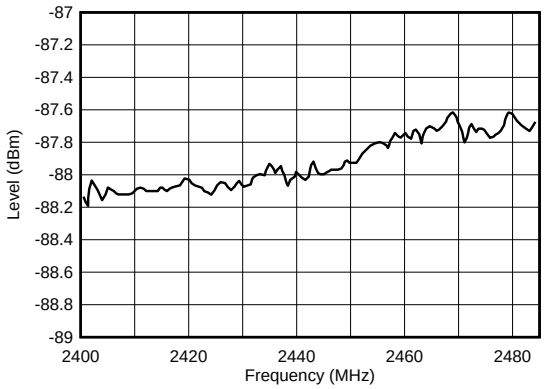
Gain = Standard Setting
T_A = 25°C

Figure 4-13. RX Sensitivity vs Supply Voltage



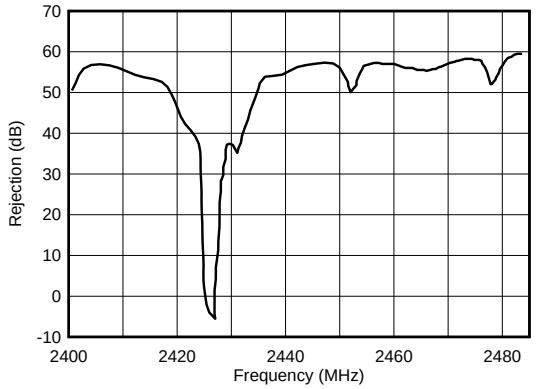
T_A = 25°C
TX Power Setting = 4 dBm

Figure 4-14. TX Power vs Supply Voltage



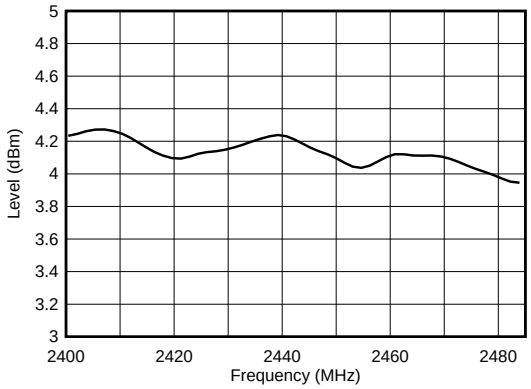
Gain = Standard Setting
T_A = 25°C
V_{CC} = 3 V

Figure 4-15. RX Sensitivity vs Frequency



T_A = 25°C
Wanted Signal at 2426 MHz with –67 dBm Level
V_{CC} = 3 V
Gain = Standard Setting

Figure 4-16. RX Interferer Rejection (Selectivity) vs Interferer Frequency



T_A = 25°C
TX Power Setting = 4 dBm
V_{CC} = 3 V

Figure 4-17. TX Power vs Frequency

Table 4-1. Output Power and Current Consumption(1)(2)

TYPICAL OUTPUT POWER (dBm)	TYPICAL CURRENT CONSUMPTION (mA)	TYPICAL CURRENT CONSUMPTION WITH TPS62730 (mA)
4	32	24.6
0	27	21
–6	24	18.5
–23	21	16.5

(1) Measured on Texas Instruments CC2540 EM reference design with T_A = 25°C, V_{DD} = 3 V and f_c = 2440 MHz. See SWRU191 for recommended register settings.
(2) Measured on Texas Instruments CC2540TPS62730 EM reference design with T_A = 25°C, V_{DD} = 3 V and f_c = 2440 MHz. See SWRU191 for recommended register settings.

4.25 Typical Current Savings

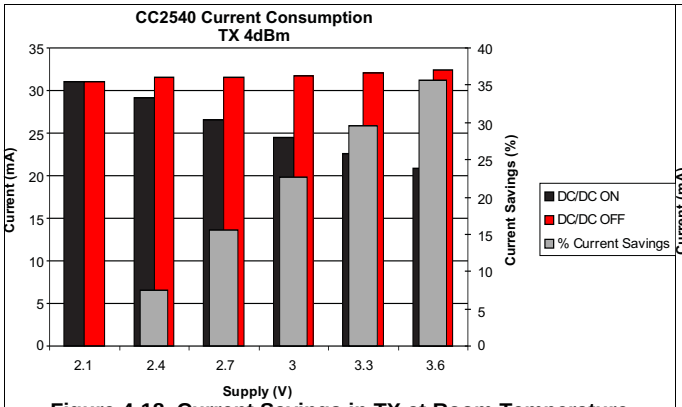


Figure 4-18. Current Savings in TX at Room Temperature

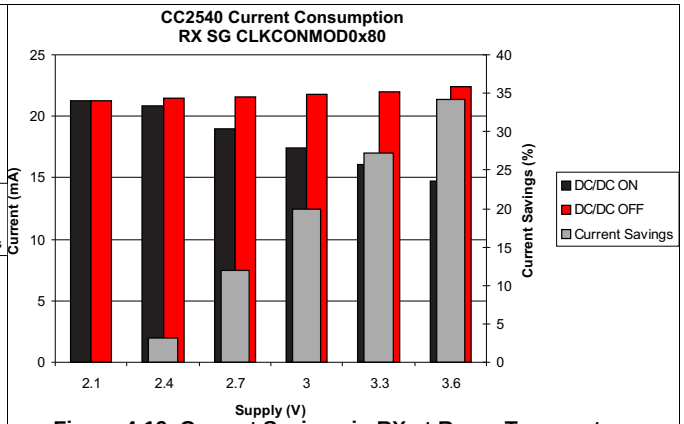


Figure 4-19. Current Savings in RX at Room Temperature

See the application note (SWRA365) for information regarding the CC2540T and TPS62730 como board and the current savings that can be achieved using the como board.

5 Detailed Description

5.1 Overview

The modules of the CC2540T device can be roughly divided into one of three categories:

- CPU-related modules
- Modules related to power, test, and clock distribution
- Radio-related modules

A short description of each module is given in the following subsections.

5.2 Functional Block Diagram

A block diagram of the CC2540T is shown in Figure 5-1.

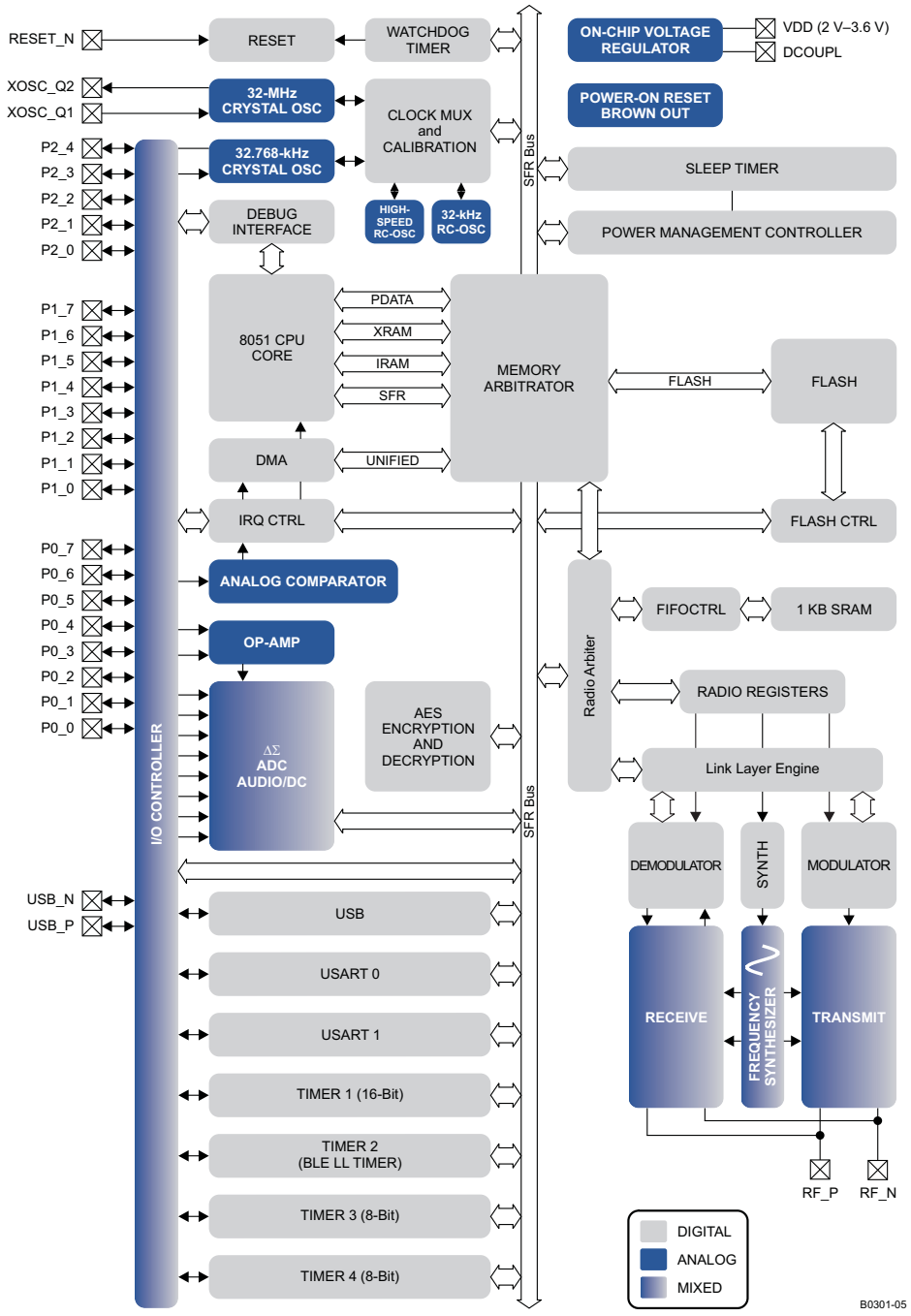


Figure 5-1. CC2540T Block Diagram

5.3 Block Descriptions

5.3.1 CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE/XDATA), a debug interface, and an 18-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, with XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in Figure 5-1 as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The **8-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces. The SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power modes 2 and 3).

The **256-KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

5.3.2 Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bytewise programming. See the User's Guide (SWRU191) for details on the flash controller.

A versatile five-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, and so forth) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

Each CC2540T contains a unique 48-bit IEEE address that can be used as the public device address for a *Bluetooth* device. Designers are free to use this address, or provide their own, as described in the *Bluetooth* specification.

The **interrupt controller** services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I/O and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the CC2540T back to the active mode.

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that can either use an external 32.768-kHz crystal oscillator or an internal 32.753-kHz RC oscillator. The sleep timer runs continuously in all operating modes except power mode 3. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power modes 1 or 2.

A built-in **watchdog timer** allows the CC2540T to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter and capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer used by the *Bluetooth* low energy stack. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received or transmitted, or it is used to record the exact time at which transmission ends. There are two 16-bit timer-compare registers and two 24-bit overflow-compare registers that can be used to give exact timing for the start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 and USART 1 are each configurable as either an SPI master or slave, or as a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, which leaves the ordinary timers free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

The **ADC** supports 7 to 12 bits of resolution with a corresponding range of bandwidths from 30-kHz to 4-kHz, respectively. DC and audio conversions with up to eight input channels (I/O controller pins) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The ultralow-power **analog comparator** enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is connected to the I/O controller interrupt detector and can be treated by the MCU as a regular I/O pin interrupt.

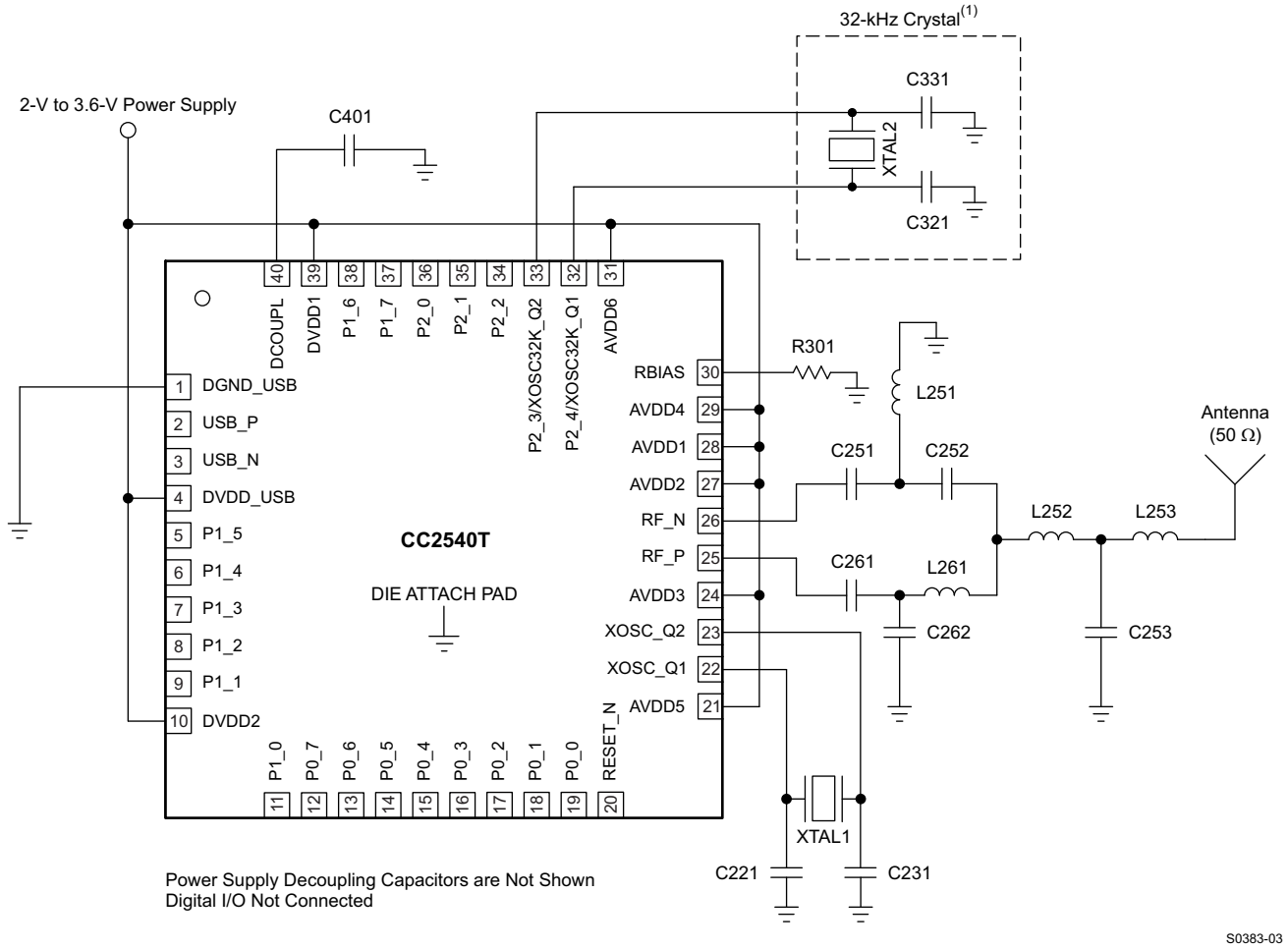
6 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

Few external components are required for the operation of the CC2540T. A typical application circuit is shown in Figure 6-1.



(1) 32-kHz crystal is mandatory when running the chip in low-power modes, except if the link layer is in the standby state (Vol. 6 Part B Section 1.1, see [1]).

NOTE: Different antenna alternatives will be provided as reference designs.

Figure 6-1. CC2540T Application Circuit

Table 6-1. Overview of External Components (Excluding Supply Decoupling Capacitors)

COMPONENT	DESCRIPTION	VALUE
C221	32-MHz XTAL loading capacitor	12 pF
C231	32-MHz XTAL loading capacitor	12 pF
C251	Part of the RF matching network	18 pF
C252	Part of the RF matching network	1 pF
C253	Part of the RF matching network	1 pF
C261	Part of the RF matching network	18 pF
C262	Part of the RF matching network	1 pF
C321	32-kHz XTAL loading capacitor	15 pF
C331	32-kHz XTAL loading capacitor	15 pF
C401	Decoupling capacitor for the internal digital regulator	1 µF
L251	Part of the RF matching network	2 nH
L252	Part of the RF matching network	1 nH
L253	Part of the RF matching network	3 nH
L261	Part of the RF matching network	2 nH
R301	Resistor used for internal biasing	56 kΩ

6.2 Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. The recommended balun shown consists of C262, L261, C252, and L252.

6.3 Crystal

An external 32-MHz crystal, XTAL1, with two loading capacitors (C221 and C231) is used for the 32-MHz crystal oscillator. See Section 4.10 for details. The load capacitance seen by the 32-MHz crystal is given by Equation 1:

$$C_L = \frac{1}{\frac{1}{C_{221}} + \frac{1}{C_{231}}} + C_{parasitic} \quad (1)$$

XTAL2 is an optional 32.768-kHz crystal, with two loading capacitors (C321 and C331) used for the 32.768-kHz crystal oscillator. The 32.768-kHz crystal oscillator is used in applications where both very low sleep-current consumption and accurate wake-up times are needed. The load capacitance seen by the 32.768-kHz crystal is given by Equation 2:

$$C_L = \frac{1}{\frac{1}{C_{321}} + \frac{1}{C_{331}}} + C_{parasitic} \quad (2)$$

A series resistor may be used to comply with the ESR requirement.

6.4 On-Chip 1.8-V Voltage Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires a decoupling capacitor (C401) for stable operation.

6.5 Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely (see Section 6.6).

6.6 Reference Design

Bluetooth Low Energy Light Reference Design

This reference design is an example of using the SimpleLink™ *Bluetooth* low energy CC2540T high temperature range, wireless microcontroller in lighting applications. The board includes RGBW LEDs controlled by the CC2540T and is USB powered. The board can be controlled out-of-the-box by the TI BLE Multitool smart phone app.

7 器件和文档支持

7.1 文档支持

7.1.1 相关文档

以下文档介绍了 CC2540T 处理器。在 www.ti.com 内提供这些文档的副本。

[1] 《*Bluetooth*® Core 技术规范，核心版本 4.0》

SWRU191 《CC253x 适用于 2.4GHz IEEE 802.15.4 和 ZigBee® 应用程序的片上系统解决方案，CC2540/41 适用于 2.4Ghz *蓝牙*低能耗应用的片上系统 应用程序》

SWRA365 使用 TPS62730 节省 CC254x 电流

7.1.2 社区资源

下列链接提供到 TI 社区资源的连接。 链接的内容由各个分销商“按照原样”提供。 这些内容并不构成 TI 技术规范和标准且不一定反映 TI 的观点；请见 TI 的使用条款。

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德州仪器 **(TI)** 嵌入式处理器维基网站 ***德州仪器 (TI) 嵌入式处理器维基网站。*** 此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

7.2 德州仪器 (TI) 低功耗射频网站

- 论坛、视频和博客
- 射频设计帮助
- E2E 交流互动

访问 www.ti.com/lprf-forum 立即体验。

7.3 德州仪器 (TI) 低功耗射频开发者网络

德州仪器 (TI) 建立了一个大型低功耗射频开发合作伙伴网络，帮助客户加快应用开发。此网络中包括推荐的公司、射频顾问和独立设计工作室，他们可提供一系列硬件模块产品和设计服务，其中包括：

- 射频电路、低功耗射频和 ZigBee®设计服务
- 低功耗射频和 ZigBee 模块解决方案以及开发工具
- 射频认证服务和射频电路制造

是否需要有关模块、工程服务或开发工具的帮助？

请搜索低功耗射频开发者网络工具查找适合的合作伙伴。
www.ti.com/lprfnetwork

7.4 低功耗射频电子新闻简报

通过低功耗射频电子新闻简报，用户能够了解到最新的产品、新闻稿、开发者相关新闻以及关于德州仪器 (TI) 低功耗射频产品其它新闻和活动。低功耗射频电子新闻简报文章包含可获取更多在线信息的链接。

访问
www.ti.com/lprfnewsletter 立即注册

7.5 商标

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IAR Embedded Workbench is a trademark of IAR Systems AB.
ZigBee is a registered trademark of ZigBee Alliance, Inc.
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7.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.7 出口管制提示

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7.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 机械、封装和可订购信息

8.1 封装信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC2540TF256RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	CC2540T F256
CC2540TF256RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2540T F256
CC2540TF256RHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2540T F256
CC2540TF256RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	CC2540T F256
CC2540TF256RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2540T F256
CC2540TF256RHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2540T F256

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

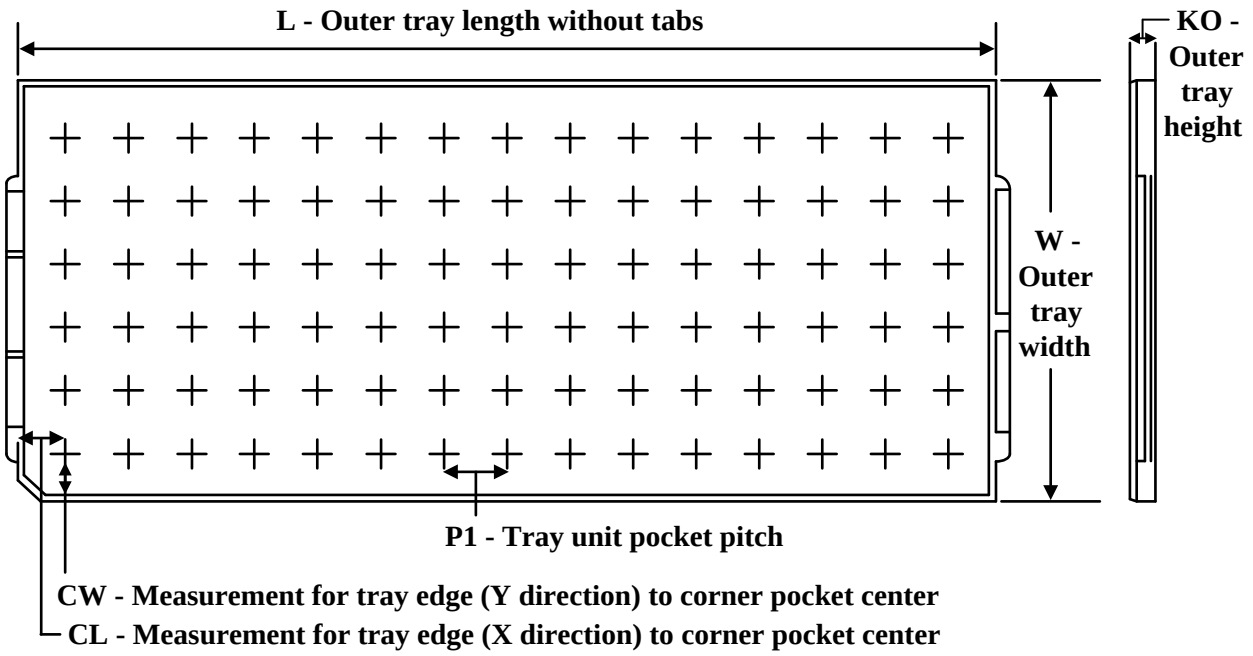
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
CC2540TF256RHAR	RHA	VQFN	40	2500	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CC2540TF256RHAR.A	RHA	VQFN	40	2500	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CC2540TF256RHAR.B	RHA	VQFN	40	2500	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CC2540TF256RHAT	RHA	VQFN	40	250	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CC2540TF256RHAT	RHA	VQFN	40	250	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CC2540TF256RHAT.A	RHA	VQFN	40	250	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CC2540TF256RHAT.A	RHA	VQFN	40	250	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CC2540TF256RHAT.B	RHA	VQFN	40	250	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
CC2540TF256RHAT.B	RHA	VQFN	40	250	35 X 14	150	315	135.9	7620	8.8	7.9	8.15

GENERIC PACKAGE VIEW

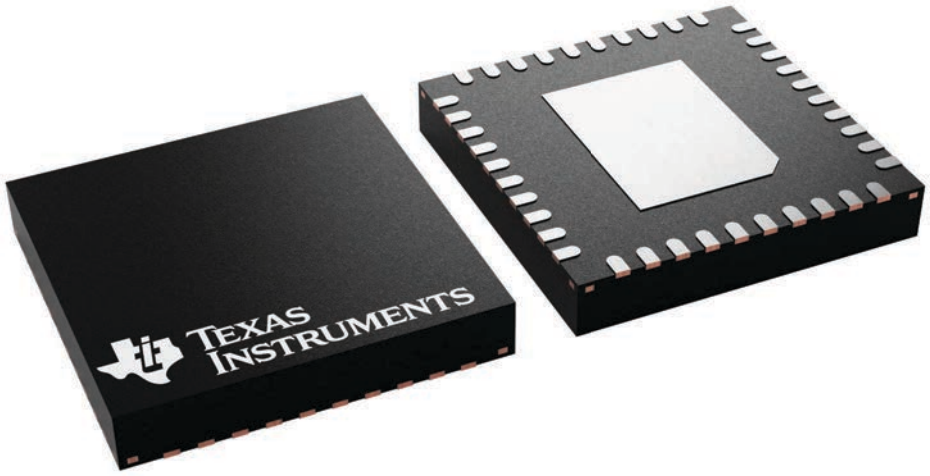
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



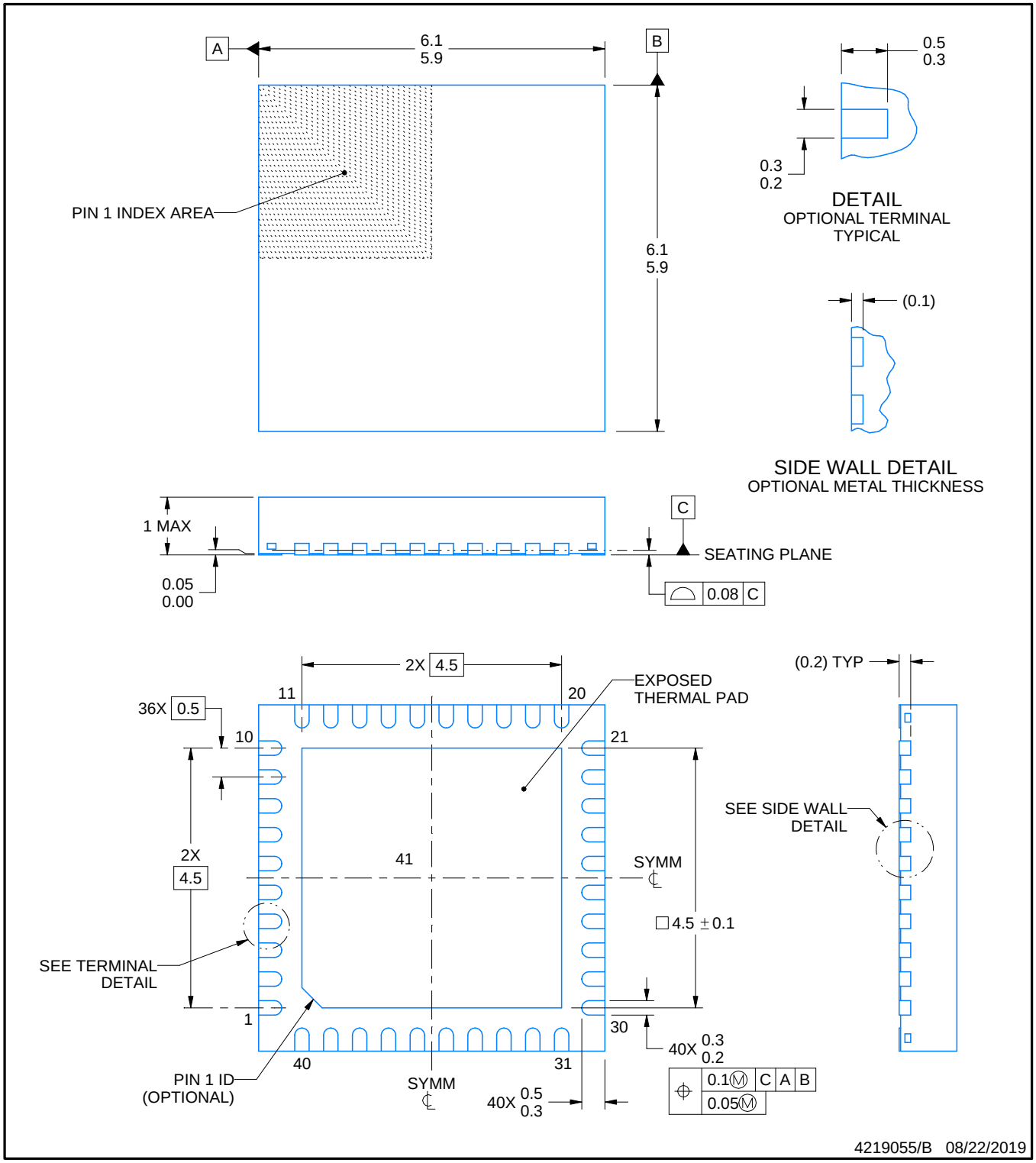
4225870/A

PACKAGE OUTLINE

RHA0040H

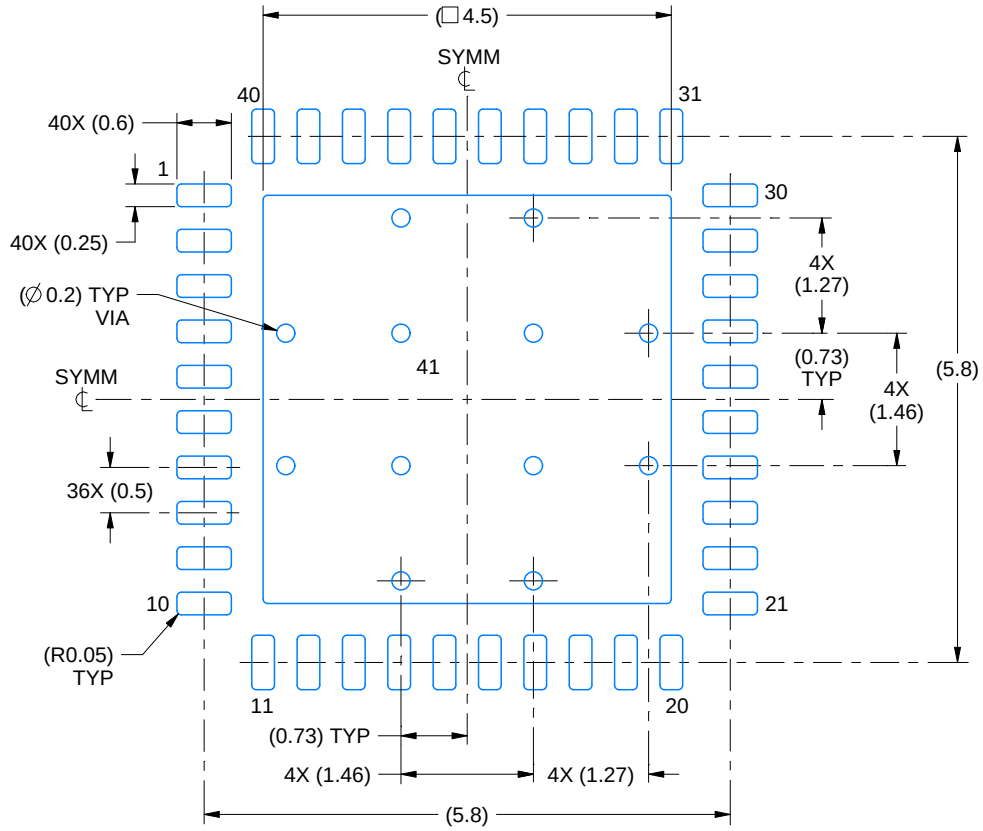
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

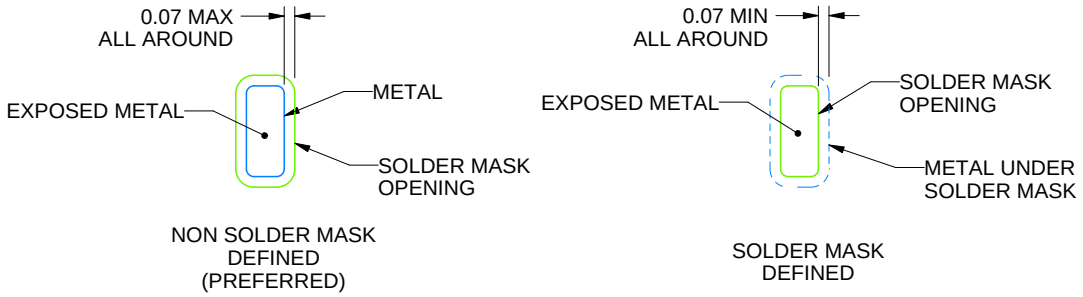


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

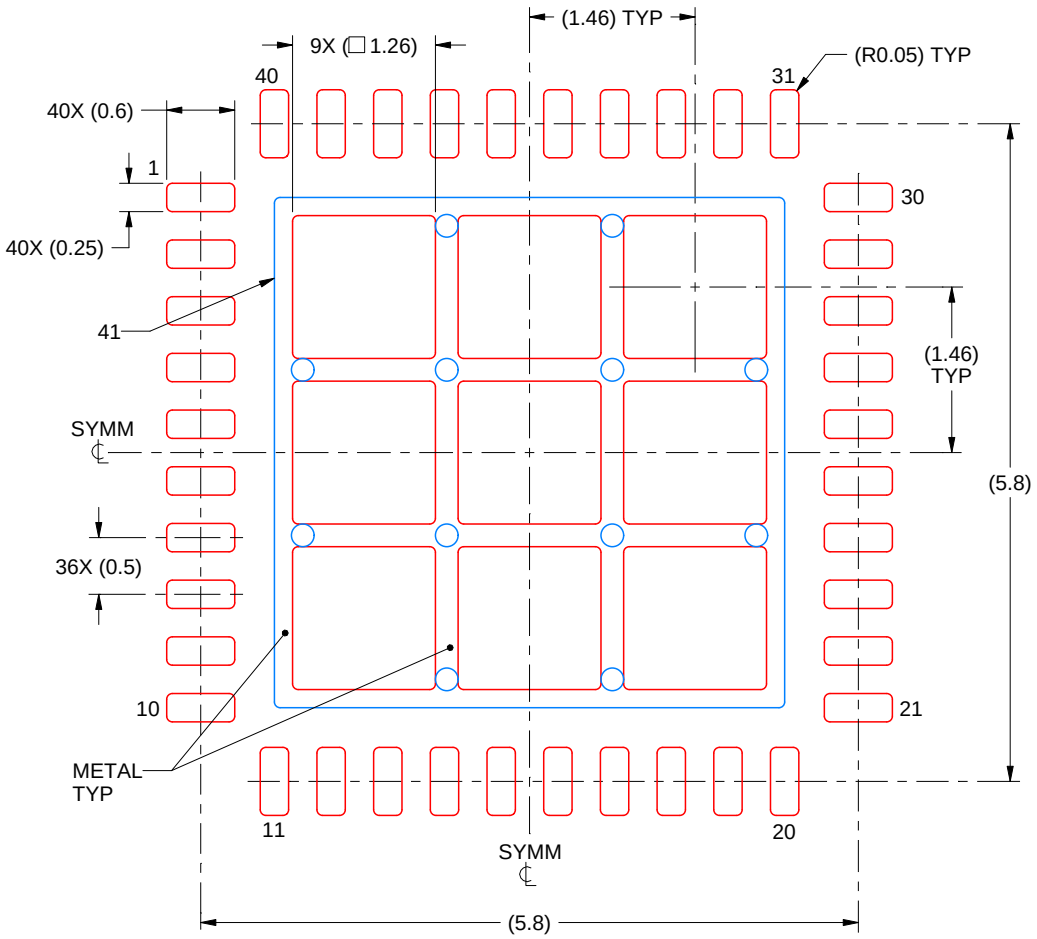


SOLDER MASK DETAILS

4219055/B 08/22/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219055/B 08/22/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月