

BQ756506-Q1 4S 或 6S 独立式精密汽车电池监控器、平衡器和集成电流检测

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
 - 器件温度等级 1：-40°C 至 +125°C 环境工作温度范围
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C4B
- 符合功能安全标准**
 - 专为功能安全应用开发
 - 可帮助进行 ISO 26262 系统设计的文档
 - 系统可满足 ASIL D 级要求
 - 硬件可满足 ASIL D 要求
- $\pm 1.5\text{mV}$ ADC 精度
- 兼容引脚/封装和软件的器件系列：
 - 可堆叠监控器 16S (BQ79616-Q1、BQ79656-Q1)、14S (BQ79614-Q1、BQ79654-Q1) 和 12S (BQ79612-Q1、BQ79652-Q1)
 - 独立式监控器 48V 系统 (BQ75614-Q1)
- 支持电流检测测量
- 支持保险丝和继电器打开和关闭诊断
- 用于电压、温度和电流诊断的内置冗余路径
- 可以在 128 μs 内对所有电池通道执行高度精确的电池电压测量
- 集成式后 ADC 可配置数字低通滤波器
- 主机控制的内置硬件复位功能，可模拟类似于 POR 的器件复位
- 支持内部电芯均衡
 - 240mA 的均衡电流
 - 内置平衡热管理，具有自动暂停和恢复控制功能
- 5V LDO 输出为外部数字隔离器供电
- UART 主机接口
- 内置 SPI 控制器

2 应用

- 汽车类 12V 锂离子电池系统
- 电动自行车、电动踏板车

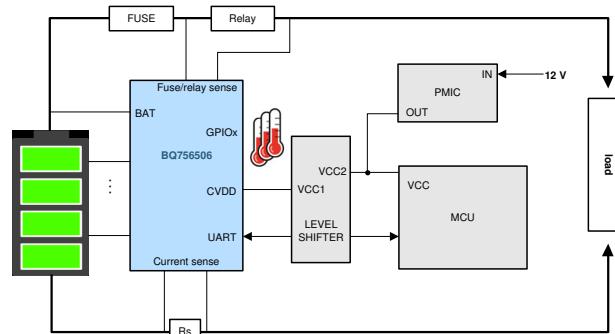
3 说明

BQ756506-Q1 器件可在不到 200 μs 的时间内提供高达 6S 电池模块的高精度电池电压测量，同时该器件还支持分流电阻器电流检测测量。借助集成式前端滤波器，可以在电池输入通道上使用简单、低额定电压的差分 RC 滤波器来实现系统。集成式后 ADC 低通滤波器可以执行经过滤波、类似于直流电的电压测量。该器件还支持集成电流检测功能，可选择与电池电压测量同步，以更好地计算荷电状态 (SOC)。此器件支持自主内部电池平衡，并通过监测温度来自动暂停和恢复平衡，以免出现过热条件。

器件信息

| 器件型号 (1) | 封装 | 封装尺寸 (标称值) |
|-------------|-----------------|-------------------|
| BQ756506-Q1 | HTQFP (64 引脚) | 10.00mm x 10.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品目录。



系统简图



本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本 (控制文档)。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision A (August 2023) to Revision B (October 2023) | Page |
|--|-------------|
| • 将数据表状态从“受限”更改为“公开” | 1 |
| <hr/> | |
| Changes from Revision * (June 2022) to Revision A (August 2023) | Page |
| • Changed Input Voltage parameter MAX value from 45 V to 60 V in Absolute Maximum Ratings..... | 7 |

5 说明 (续)

此器件还包含八个 GPIO 或辅助输入，可执行外部热敏电阻测量。

与 BQ756506-Q1 的主机通信可通过器件的专用 UART 接口连接。

6 Pin Configuration and Functions

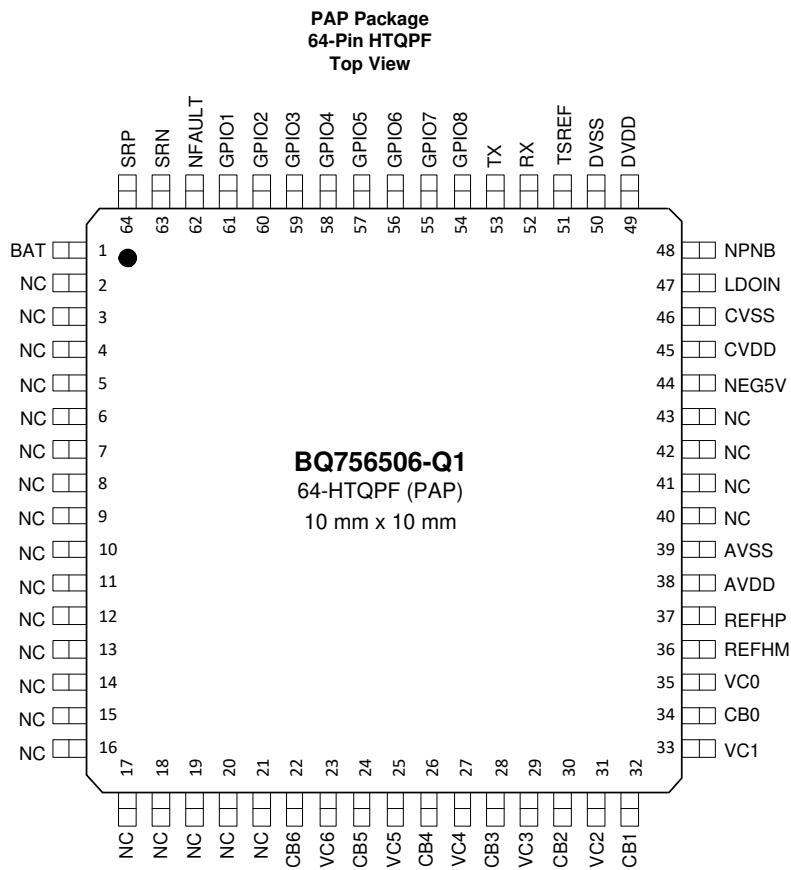


图 6-1.

表 6-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------|-----|---------------------|--|
| NAME | No. | | |
| BAT | 1 | P | Power supply input and top of module measurement input. Connect to the top cell of the battery module. |
| NPNB | 48 | P | Connect to the base of an external NPN transistor. |
| LDOIN | 47 | P | 6-V preregulated analog power supply input/sense pin. Connect to the emitter of the external NPN transistor and connect a 0.1- μ F decoupling capacitor to CVSS. |
| AVDD | 38 | P | 5-V regulated output. AVDD supplies the internal analog circuits. Bypass AVDD with a capacitor to AVSS. |
| AVSS | 39 | GND | Analog ground. Ground connection for internal analog circuits. Connect DVSS, CVSS, REFHM, and AVSS externally. All ground pins must not be left unconnected. |
| NEG5V | 44 | P | Negative 5-V charge pump used for Main ADC. Connect with a capacitor to CVSS. |
| DVDD | 49 | P | 1.8-V regulated output. DVDD supplies the internal digital circuits. Bypass DVDD with a capacitor to DVSS. |
| DVSS | 50 | GND | Digital ground. Ground connection for internal digital logics. Connect DVSS, CVSS, REFHM, and AVSS externally. All ground pins must be connected to ground. |
| CVDD | 45 | P | 5-V I/Os power supply. CVDD supplies the I/O pins. This power supply also supports an additional 10-mA external load in ACTIVE and SLEEP. |
| CVSS | 46 | GND | Ground connection. Connect DVSS, CVSS, REFHM, and AVSS externally. All ground pins must be connected to ground. |

表 6-1. Pin Functions (续)

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------|-----|---------------------|--|
| NAME | No. | | |
| TSREF | 51 | P | 5-V bias voltage for NTC thermistor. Connect TSREF to the top of the NTC resistor divider network to the GPIOs when they are configured for NTC temperature monitoring. Bypass TSREF with a capacitor to CVSS. |
| REFHP | 37 | P | Precision reference output pin. Bypass with a capacitor to REFHFM. |
| REFHM | 36 | GND | Precision reference ground. Ground connection for the internal precision reference. Connect DVSS, CVSS, REFHFM, and AVSS externally. All ground pins must be connected to ground. |
| NC | 3 | I | No connection. Connect pin to BAT. |
| NC | 5 | I | No connection. Connect pin to BAT. |
| NC | 7 | I | No connection. Connect pin to BAT. |
| NC | 9 | I | No connection. Connect pin to BAT. |
| NC | 11 | I | No connection. Connect pin to BAT. |
| NC | 13 | I | No connection. Connect pin to BAT. |
| NC | 15 | I | No connection. Connect pin to BAT. |
| NC | 17 | I | No connection. Connect pin to BAT. |
| NC | 19 | I | No connection. Connect pin to BAT. |
| NC | 21 | I | No connection. Connect pin to BAT. |
| VC6 | 23 | I | Cell voltage sense input. Connect to the positive terminal of cell 6. Connect a differential RC filter to VC5. |
| VC5 | 25 | I | Cell voltage sense input. Connect to the positive terminal of cell 5. Connect a differential RC filter to VC4. |
| VC4 | 27 | I | Cell voltage sense input. Connect to the positive terminal of cell 4. Connect a differential RC filter to VC3. |
| VC3 | 29 | I | Cell voltage sense input. Connect to the positive terminal of cell 3. Connect a differential RC filter to VC2. |
| VC2 | 31 | I | Cell voltage sense input. Connect to the positive terminal of cell 2. Connect a differential RC filter to VC1. |
| VC1 | 33 | I | Cell voltage sense input. Connect to the positive terminal of cell 1. Connect a differential RC filter to VC0. |
| VC0 | 35 | I | Cell voltage sense input. Connect to the negative terminal of cell 1. Connect a differential RC filter to AVSS. |
| NC | 2 | I/O | No connection. Connect pin to BAT. |
| NC | 4 | I/O | No connection. Connect pin to BAT. |
| NC | 6 | I/O | No connection. Connect pin to BAT. |
| NC | 8 | I/O | No connection. Connect pin to BAT. |
| NC | 10 | I/O | No connection. Connect pin to BAT. |
| NC | 12 | I/O | No connection. Connect pin to BAT. |
| NC | 14 | I/O | No connection. Connect pin to BAT. |
| NC | 16 | I/O | No connection. Connect pin to BAT. |
| NC | 18 | I/O | No connection. Connect pin to BAT. |
| NC | 20 | I/O | No connection. Connect pin to BAT. |
| CB6 | 22 | I/O | Cell balance connection. This pin is connected to the internal cell balancing FET. Connect this pin to the positive terminal of cell 6 with a differential RC filter to CB5. The filter resistor also sets the internal balance current. Connect to the BAT pin via a capacitor. |
| CB5 | 24 | I/O | Cell balance connection. This pin is connected to the internal cell balancing FET. Connect this pin to the positive terminal of cell 5 with a differential RC filter to CB4. The filter resistor also sets the internal balance current. |
| CB4 | 26 | I/O | Cell balance connection. This pin is connected to the internal cell balancing FET. Connect this pin to the positive terminal of cell 4 with a differential RC filter to CB3. The filter resistor also sets the internal balance current. |

表 6-1. Pin Functions (续)

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|--------|-------------------|---------------------|---|
| NAME | No. | | |
| CB3 | 28 | I/O | Cell balance connection. This pin is connected to the internal cell balancing FET. Connect this pin to the positive terminal of cell 3 with a differential RC filter to CB2. The filter resistor also sets the internal balance current. |
| CB2 | 30 | I/O | Cell balance connection. This pin is connected to the internal cell balancing FET. Connect this pin to the positive terminal of cell 2 with a differential RC filter to CB1. The filter resistor also sets the internal balance current. |
| CB1 | 32 | I/O | Cell balance connection. This pin is connected to the internal cell balancing FET. Connect this pin to the positive terminal of cell 1 with a differential RC filter to CB0. The filter resistor also sets the internal balance current. |
| CB0 | 34 | I/O | Cell balance connection. This pin is connected to the internal cell balancing FET. Connect to the negative terminal of cell 1 with differential RC filter to AVSS. The filter resistor also sets the internal balance current. |
| SRP | 64 | I | Current sense resistor connection. With SRP and SRN connected to each end of a current sense resistor. |
| SRN | 63 | I | Current sense resistor connection. With SRP and SRN connected to each end of a current sense resistor. |
| RX | 52 | I | UART receiver input. Pull up to CVDD with an external resistor and connect the device RX to the TX output of the host MCU. If unused, connect RX to CVDD. |
| TX | 53 | O | UART transmitter output. Connect device TX to RX input of the host MCU and will be pulled up from the host side. If unused, leave it floating. |
| NC | 40, 41, 42, 43 | I/O | No connection. Leave pin floating. |
| NFAULT | 62 | O | Fault indication output. Active low. Pull up NFAULT to CVDD with a pullup resistor and connect NFAULT to host MCU GPIO. If unused, leave it unconnected. |
| GPIO1 | 61 | I/O | General purpose input/output, configuration options are: <ul style="list-style-type: none"> For external NTC thermistor connection, connect NTC thermistor to the pin and pull up to TSREF. Used as input to ADC and OT and UT hardware comparators. For external DC voltage measurement, configured as input to ADC. Generic digital input/output. Use as I/O for SPI controller. |
| GPIO2 | 60 | I/O | |
| GPIO3 | 59 | I/O | |
| GPIO4 | 58 | I/O | |
| GPIO5 | 57 | I/O | |
| GPIO6 | 56 | I/O | |
| GPIO7 | 55 | I/O | |
| GPIO8 | 54 | I/O | |

(1) GND = Ground, I = Input, I/O = Input/Output, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------------|--|-------|------|------|
| Input Voltage | BAT, VC* (except VC0), CB* (except CB0), NFAULT to AVSS ^{(2) (3)} | - 0.3 | 60 | V |
| Input Voltage | CB0, VC0 to AVSS | - 0.3 | 5.5 | V |
| | SRP, SRN to AVSS | -0.3 | 2.1 | V |
| | VCn to VCn-1, n = 1 to 6 ⁽²⁾ | - 80 | 80 | V |
| | CBn to CBn-1, n = 1 to 6 ⁽³⁾ | - 0.3 | 16 | V |
| | SRP to SRN | -0.3 | 1.8 | V |
| | LDOIN to AVSS | - 0.3 | 9 | V |
| | NPNB to AVSS | - 0.3 | 10 | V |
| | AVDD to AVSS | - 0.3 | 5.5 | V |
| | DVDD to DVSS | - 0.3 | 1.98 | V |
| | CVDD to CVSS | - 0.3 | 6 | V |
| | TSREF to AVSS | - 0.3 | 5.5 | V |
| | REFHP to REFHM | - 0.3 | 5.5 | V |
| | NEG5V to AVSS | - 5.5 | 0 | V |
| | TX, RX to AVSS | - 0.3 | 6 | V |
| | GPIO* to AVSS | - 0.3 | 5.5 | V |
| CB* current | Max of 3 cell in balancing at 75°C ambient | | 240 | mA |
| I/O current | GPIO*, RX, TX current | | 10 | mA |
| T _{OTP_PROG} | Device will not start OTP programming above this temperature | | 55 | °C |
| T _A | Ambient temperature | - 40 | 130 | °C |
| T _J | Junction temperature | - 40 | 150 | °C |
| T _{stg} | Storage temperature | - 65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) VC pin voltage has to meet criteria of both VCn to AVSS as well as VCn to VCn-1.

(3) CB pin voltage has to meet criteria of both CBn to AVSS as well as CBn to CBn-1.

7.2 ESD Ratings

| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002, ⁽¹⁾ HBM ESD classification level H1C | | V | VALUE | UNIT | |
|--------------------|----------------------------|---|--|---|--|------|--|
| | | Charged device model (CDM), per AEC Q100-011, CDM ESD classification level C2a | | | All Pins | ±500 | |
| | | | | | Other pins (1, 16, 17, 32, 33, 48, 49, 64) | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------------------|---|------|------|-----|------|
| V_{BAT_RANGE} | Total module voltage, full functionality, no OTP programming | 9 | 32 | V | |
| $V_{BAT_OTP_RANGE}$ | Total module voltage, full functionality, OTP programming allow | 11 | 32 | V | |
| V_{CELL_RANGE} | $VC_n - VC_{n-1}$, where $n = 2$ to 6 | -1 | 5 | V | |
| | $VC_1 - VC_0$ | 0 | 5 | V | |
| | VC_0, CB_0 to AVSS | -0.3 | 5 | V | |
| | VC_1, VC_2, CB_1, CB_2 to AVSS | -0.3 | 32 | V | |
| | VC_n, CB_n to AVSS, where $n = 3$ to 6 | 3 | 32 | V | |
| V_{CS_RANGE} | Current sense range, $V_{SRP} - V_{SRN}$ | -100 | 100 | mV | |
| V_{CB_RANGE} | $CB_n - CB_{n-1}$, where $n = 1$ to 6 | 0 | 5 | V | |
| V_{IO_RANGE} | RX, TX, NFAULT | 0 | CVDD | V | |
| V_{GPIO_RANGE} | GPIO $_n$ input, where $n = 1$ to 8 | 0.2 | 4.8 | V | |
| I_{IO} | GPIO $_n$, RX, TX, where $n = 1$ to 8 | | 5 | mA | |
| T_A | Operation temperature | -40 | 125 | °C | |

7.4 Thermal Information

| THERMAL METRIC | | BQ7961x-Q1 | UNIT |
|-----------------------------|--|-------------|------|
| | | PAP (HTQFP) | |
| | | 64 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 21.6 | °C/W |
| $R_{\theta JC(\text{top})}$ | Junction-to-case (top) thermal resistance | 8.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 7.9 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter | 0.1 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter | 7.8 | °C/W |
| $R_{\theta JC(\text{bot})}$ | Junction-to-case (bottom) thermal resistance | 2.1 | °C/W |

7.5 Electrical Characteristics

over operating -40°C to 125°C free-air temperature range, $V_{BAT} = 9V$ to 32V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|---------------------------------------|-----|-----|------|
| THERMAL SHUTDOWN | | | | | |
| T_{SHUT} | Thermal shutdown (rising direction) | | 130 | 137 | 152 |
| T_{SHUT_FALL} | Thermal shutdown (falling direction) | | 112 | 129 | °C |
| T_{SHUT_HYS} | Thermal shutdown (rising - falling direction) | | 20 | | °C |
| T_{WARN_RANGE} | Thermal warning Threshold (rising direction) | | 85 | 115 | °C |
| T_{WARN_HYS} | Thermal warning hysteresis (falling direction) | | 10 | | °C |
| T_{WARN_ACC} | Thermal warning accuracy (+/-) | | 5 | | °C |
| SUPPLY CURRENTS | | | | | |
| I_{SHDN} | Supply current in SHUTDOWN mode | Sum of both I_{BAT} and I_{LDOIN} | | 16 | 23 |
| | | | | μA | |

7.5 Electrical Characteristics (续)

over operating -40°C to 125°C free-air temperature range, $\text{VBAT} = 9\text{V}$ to 32V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|---|------|-----|------|---------------|
| $I_{\text{SLP}(\text{IDLE})}$ | Baseline supply current in SLEEP mode. No fault, no protector comparator, no cell balancing | Sum of both I_{BAT} and I_{LDOIN} $T_A = -20^{\circ}\text{C}$ to 65°C | | | 120 | 160 |
| | | Sum of both I_{BAT} and I_{LDOIN} $T_A = -40^{\circ}\text{C}$ to 125°C | | | 220 | μA |
| $I_{\text{ACT}(\text{IDLE})}$ | Baseline supply current in ACTIVE mode | Sum of both I_{BAT} and I_{LDOIN} No fault, no communication, no protector comparator, no cell balancing | | | 10.4 | 11.6 |
| $I_{\text{CB_EN}}$ | Additional supply current when cell balancing is on | At least 1 cell balancing FET is on, OT_{CB} is enabled. Other functions are inactive | | | 1 | 1.5 |
| I_{PROTCOMP} | Additional supply current when protector comparator is on | Either OV/UV/OT/UT protector is enabled. Other functions are inactive | | | 20 | 60 |
| I_{ADC} | Additional supply current when CS/main and aux ADC are enabled | Both CS/Main ADC are on, in continuously mode, Other functions are inactive | | | 1.8 | 2.4 |
| I_{ADC} | Additional supply current when ADC is enabled | Main or Aux ADC on, and conversion is in progress. Other functions are inactive | | | 0.4 | 0.6 |
| | | 2 ADCs on, and conversion is in progress. Other functions are inactive (not applicable if current sense ADC is availibe in this device) | | | 0.6 | 0.9 |
| I_{BAT} | Supply current goes into BAT pin | ACTIVE Mode | | | 150 | μA |
| | | SLEEP Mode | | | 25 | μA |
| | | SHUTDOWN Mode | | | 5 | μA |
| $I_{\text{OW_SINK}}$ | Sink current for open wire test, applies to VC_1 to VC_n and CB_1 to CB_n , where n is the maximum number of channels in the device. | | | 380 | 500 | 600 |
| $I_{\text{OW_SOURCE}}$ | Source current for open wire test, applies to VC_0 and CB_0 | | | 380 | 500 | 600 |
| $I_{\text{LEAK_CS}}$ | Leakage current SRP and SRN pin | Main and CS ADC is off | | | 0.2 | μA |
| I_{LEAK} | Leakage current on VC , CB pins | VC , CB pins with ADC off. | | | 0.1 | μA |
| $V_{\text{SR_OW}}$ | Clamped voltage when $I_{\text{OW_SORUCE}}$ is enabled for SRP and SRN | | | | | 0.9 |
| Supplies (LDOIN) | | | | | | |
| V_{LDOIN} | LDOIN voltage | No OTP programming | 5.9 | 6 | 6.1 | V |
| | | OTP programming | 7.9 | 8 | 8.1 | V |
| Supplies (CVDD) | | | | | | |
| V_{CVDD} | CVDD output voltage | ACTIVE and SLEEP mode | 4.9 | 5 | 5.1 | V |
| | | SHUTDOWN mode, no external lload | 3.95 | | | V |
| | | SHUTDOWN mode, max external lload = 5mA | 3.4 | | | V |
| $V_{\text{CVDD_LDRG}}$ | CVDD load regulation | ACTIVE/SLEEP mode, max external lload = 10mA | - 30 | | | mV |
| $V_{\text{CVDD_OV}}$ | CVDD OV threshold | ACTIVE/SLEEP mode, max external lload = 10mA | 5.3 | 5.5 | 5.7 | V |
| $V_{\text{CVDD_OVHYS}}$ | CVDD OV Hystersis | ACTIVE/SLEEP mode, max external lload = 10mA | 130 | 150 | 170 | mV |

7.5 Electrical Characteristics (续)

over operating -40°C to 125°C free-air temperature range, VBAT = 9V to 32V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|---|-------|------|-------|------|
| V _{CVDD_UV} | CVDD UV threshold | SHUTDOWN mode | | 3.5 | | V |
| | | ACTIVE/SLEEP mode, max external I _{load} = 10mA | 4.3 | 4.45 | 4.65 | V |
| V _{CVDD_UVHYS} | CVDD UV Hystersis | | | 260 | | mV |
| V _{CVDD_ILIMIT} | CVDD current limit | ACTIVE, SLEEP | 35 | 60 | 85 | mA |
| Supplies (AVDD) | | | | | | |
| V _{AVDD} | AVDD output voltage | C _{SUPPLIES} = 1μF, ACTIVE mode | 4.85 | 5 | 5.21 | V |
| V _{AVDD_OV} | AVDD OV threshold | C _{SUPPLIES} = 1μF, ACTIVE mode | 5.25 | 5.5 | 5.7 | V |
| V _{AVDD_OVHYS} | AVDD OV Hystersis | C _{SUPPLIES} = 1μF, ACTIVE mode | 135 | 155 | 165 | mV |
| V _{AVDD_UV} | AVDD UV threshold | C _{SUPPLIES} = 1μF, ACTIVE mode | 4.25 | 4.45 | 4.6 | V |
| V _{AVDD_UVHYS} | AVDD UV Hystersis | C _{SUPPLIES} = 1μF, ACTIVE mode | 235 | 340 | 430 | mV |
| V _{AVDD_ILIMIT} | AVDD current limit | C _{SUPPLIES} = 1μF | 10 | 30 | 50 | mA |
| Supplies (DVDD) | | | | | | |
| V _{DVDD} | DVDD output voltage | C _{SUPPLIES} = 1μF, ACTIVE mode | 1.65 | 1.8 | 1.95 | V |
| V _{DVDD_OV} | DVDD OV threshold | C _{SUPPLIES} = 1μF, ACTIVE mode | 1.95 | 2.1 | 2.3 | V |
| V _{DVDD_OVHYS} | DVDD OV Hystersis | C _{SUPPLIES} = 1μF, ACTIVE mode | 40 | 65 | 120 | mV |
| V _{DVDD_UV} | DVDD UV threshold | C _{SUPPLIES} = 1μF, ACTIVE mode | 1.623 | 1.65 | 1.71 | V |
| V _{DVDD_UVHYS} | DVDD UV Hystersis | C _{SUPPLIES} = 1μF, ACTIVE mode | 15 | 50 | 73 | mV |
| V _{DVDD_ILIMIT} | DVDD current limit | | 13 | 30 | 53 | mA |
| Supplies (TSREF) | | | | | | |
| V _{TSREF} | TSREF output voltage | C _{SUPPLIES} = 1μF, ACTIVE mode | 4.975 | 5 | 5.025 | V |
| V _{TSREF_LDRG} | TSREF load regulation | I _{load} = 4mA, C _{SUPPLIES} = 1μF, ACTIVE mode | -30 | | 30 | mV |
| V _{TSREF_OV} | TSREF OV threshold | I _{load} = 4mA, C _{SUPPLIES} = 1μF, ACTIVE mode | 5.2 | 5.6 | 5.8 | V |
| V _{TSREF_OVHYS} | TSREF OV Hystersis | I _{load} = 4mA, C _{SUPPLIES} = 1μF, ACTIVE mode | 98 | 110 | 120 | mV |
| V _{TSREF_UV} | TSREF UV threshold | I _{load} = 4mA, C _{SUPPLIES} = 1μF, ACTIVE mode | 4.0 | 4.2 | 4.4 | V |
| V _{TSREF_UVHYS} | TSREF UV Hystersis | I _{load} = 4mA, C _{SUPPLIES} = 1μF, ACTIVE mode | 300 | 350 | 400 | mV |
| V _{TSREF_ILIMIT} | TSREF current limit | Device in ACTIVE Mode | 15 | 30 | 52 | mA |
| Negative Charge Pump (NEG5V) | | | | | | |
| V _{NEG5V} | NEG5V pin voltage | C _{NEG5V} = 0.1μF | -5.3 | -4.6 | -4.0 | V |
| V _{NEG5V_UV} | NEG5V UV threshold (rising) | C _{NEG5V} = 0.1μF | -4.1 | -3.5 | -3.0 | V |
| V _{NEG5V_UVRECOV} | NEG5V UV Recovery | C _{NEG5V} = 0.1μF | -4.3 | -3.8 | -3.3 | V |
| CELL BALANCE | | | | | | |
| R _{DSON} | Internal cell balance FET Rdson | VCn > 2.8V, where n = 1 to the maximum number of channels in the device; -40°C < T _A < 125°C | 1.45 | | 4.6 | Ω |
| V _{CB_DONE} | VCB_DONE detection threhsold setting range (not accuracy) | Step of 25mV | | 2.45 | | V |
| V _{MB_DONE} | VMB_DONE detection threhsold setting range (not accuracy) (Not available for standalone device) | Step of 1V | | 18 | | 65 |
| T _{OTCB} | OTCB threshold setting range (not accuracy) | Step of 2% | | 10 | | % |

7.5 Electrical Characteristics (续)

over operating -40°C to 125°C free-air temperature range, VBAT = 9V to 32V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|--------|-----|--------|
| T _{COOLOFF} | COOLOFF threshold setting range (not accuracy) | Step of 2% | 4 | 14 | % |
| T _{CB_WARN} | CB TWARN threshold | | 105 | | °C |
| T _{CB_WARN_HYS} | CB TWARN Hysteresis | | 10 | | °C |
| ADC Resolution | | | | | |
| ENOB _{MAIN} | Main ADC Effective number of bits | | 16 | | bits |
| ENOB _{AUX} | AUX ADC Effective number of bits | | 14 | | bits |
| V _{LSB_ADC} | Main and AUX ADC Resolution for VCELL measurement | | 190.73 | | µV/LSB |
| V _{LSB_CSMAIN} | Main ADC Resolution for (SRP-SRN) measurement | | 30.52 | | µV/LSB |
| V _{LSB_MAIN_DIETEMP} ₁ | DieTemp1 resolution (Main ADC) | ADC measurement is centered with 0x000 = 0°C | 0.025 | | °C/LSB |
| V _{LSB_AUX_DIETEMP2} | DieTemp2 resolution (AUX ADC) | ADC measurement is centered with 0x000 = 0°C | 0.025 | | °C/LSB |
| V _{LSB_AUX_BAT} | BAT resolution (AUX ADC) | Applies to BAT voltage measurement from AUX ADC | 3.05 | | mV/LSB |
| V _{LSB_GPIO} | GPIO resolution (Main & AUX ADC) | | 152.59 | | µV/LSB |
| V _{LSB_TSREF} | TSREF resolution (Main ADC) | | 169.54 | | µV/LSB |
| V _{LSB_DIAG} | Diagnostic measurements resolution | REFL, VBG2, LPBG5, VCM, AVAO_REF, AVDD_REF, all the HW protector DAC | 152.59 | | µV/LSB |
| V _{LSB_CS} | Current Sense ADC resolution (24-bit result) | Reading CURRENT_HI/MID/LO registers | 14.9 | | nV/LSB |
| ADC Accuracy | | | | | |
| I _{VC_DELTA} | VCn to VCn-1 input current delta (when Main ADC is on) | T _A = -20°C to 65°C | | 1.8 | µA |
| | | T _A = -40°C to 105°C | | 2 | µA |
| I _{VC} | VCn input current (when Main ADC is on) | | 8 | 12 | µA |
| R _{CB_INPUT} | CB pin input impedance (when AUX ADC is on) | | 16 | | MΩ |
| V _{ACC_MAIN_CELL} | Total channel accuracy for main ADC VCELL measurement, LPF_VCELL[2:0] = 0x03 setting; | 2V < V _{CELL} < 4.5V; T _A = 25°C | -2.2 | 1.5 | mV |
| | | 2V < V _{CELL} < 4.5V; -20°C < T _A < 65°C | -3.0 | 2.4 | mV |
| | | 2V < V _{CELL} < 4.5V; -40°C < T _A < 105°C | -3.5 | 2.6 | mV |
| | | 2V < V _{CELL} < 4.5V; -40°C < T _A < 125°C | -3.5 | 2.6 | mV |
| | | 1V < V _{CELL} < 5V; -40°C < T _A < 125°C | -3.7 | 2.8 | mV |
| | | -2V < V _{CELL} < 5V; -40°C < T _A < 125°C | -4.5 | 3.2 | mV |
| | | 2V < V _{CELL} < 4.5V; T _A = 25°C | -7.5 | 5.4 | mV |
| V _{ACC_AUX_CELL} | Total channel accuracy for AUX ADC measurement (excluding BAT and GPIO accuracy); | 2V < V _{CELL} < 4.5V; -20°C < T _A < 65°C | -8.0 | 6.3 | mV |
| | | 2V < V _{CELL} < 4.5V; -40°C < T _A < 105°C | -9.0 | 6.3 | mV |
| | | 2V < V _{CELL} < 4.5V; -40°C < T _A < 125°C | -9.0 | 6.5 | mV |
| | | 1V < V _{CELL} < 5V; -40°C < T _A < 125°C | -9.0 | 6.6 | mV |
| | | 0V < V _{CELL} < 5V; -40°C < T _A < 125°C | -9.0 | 6.6 | mV |

7.5 Electrical Characteristics (续)

over operating -40°C to 125°C free-air temperature range, VBAT = 9V to 32V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|---|---|-------|-------|------|
| $V_{(MAIN-AUX)}$ | $2V < V_{CELL} < 4.5V; T_A = 25^\circ C$ | -7.1 | 6.1 | 6.1 | mV |
| | $2V < V_{CELL} < 4.5V; -20^\circ C < T_A < 65^\circ C$ | -7.8 | 6.6 | 6.6 | mV |
| | $2V < V_{CELL} < 4.5V; -40^\circ C < T_A < 105^\circ C$ | -7.8 | 6.6 | 6.6 | mV |
| | $2V < V_{CELL} < 4.5V; -40^\circ C < T_A < 125^\circ C$ | -7.8 | 6.7 | 6.7 | mV |
| | $1V < V_{CELL} < 5V; -40^\circ C < T_A < 125^\circ C$ | -7.9 | 6.9 | 6.9 | mV |
| | $0V < V_{CELL} < 5V; -40^\circ C < T_A < 125^\circ C$ | -7.9 | 6.9 | 6.9 | mV |
| $V_{ACC_MAIN_GPIO_RA_TIO}$ | $0.08V < V_{IN} < 0.2V, 85^\circ C < T_A < 125^\circ C$ | -0.20 | 0.20 | 0.20 | % |
| | $0.2V < V_{IN} < 4.6V, -40^\circ C < T_A < 105^\circ C$ | -0.20 | 0.20 | 0.20 | % |
| | $4.6V < V_{IN} < 4.8V, -40^\circ C < T_A < -20^\circ C$ | -0.30 | 0.30 | 0.30 | % |
| $V_{ACC_AUX_GPIO_RA_TIO}$ | $0.08V < V_{IN} < 0.2V, 85^\circ C < T_A < 125^\circ C$ | -0.20 | 0.20 | 0.20 | % |
| | $0.2V < V_{IN} < 4.6V, -40^\circ C < T_A < 105^\circ C$ | -0.20 | 0.20 | 0.20 | % |
| | $4.6V < V_{IN} < 4.8V, -40^\circ C < T_A < -20^\circ C$ | -0.30 | 0.30 | 0.30 | % |
| $V_{ACC_MAIN_GPIO_AB_S}$ | $0.08V < V_{IN} < 0.2V, 85^\circ C < T_A < 125^\circ C$ | -4.00 | 4.00 | 4.00 | mV |
| | $0.2V < V_{IN} < 4.6V, -40^\circ C < T_A < 105^\circ C$ | -5.00 | 3.00 | 3.00 | mV |
| | $4.6V < V_{IN} < 4.8V, -40^\circ C < T_A < -20^\circ C$ | -4.00 | 4.00 | 4.00 | mV |
| $V_{ACC_AUX_GPIO_AB_S}$ | $0.08V < V_{IN} < 0.2V, 85^\circ C < T_A < 125^\circ C$ | -6.00 | 6.00 | 6.00 | mV |
| | $0.2V < V_{IN} < 4.6V, -40^\circ C < T_A < 105^\circ C$ | -6.00 | 6.00 | 6.00 | mV |
| | $4.6V < V_{IN} < 4.8V, -40^\circ C < T_A < -20^\circ C$ | -6.00 | 6.00 | 6.00 | mV |
| $V_{ACC_MAIN_CS}$ | Total channel accuracy for (SRP-SRN) from Main ADC LPF_SR[2:0] = 0x00 | -1.1 | 1.1 | 1.1 | mV |
| $V_{ACC_AUX_BAT}$ | AUX ADC measurement accuracy for BAT pin Vbat pack range: 16V to 32V, $T_A = -40^\circ C$ to $125^\circ C$ | -270 | 170 | 170 | mV |
| $V_{ACC_AUX_REFL}$ | AUX ADC measurement result | 1.092 | 1.1 | 1.106 | V |
| $V_{ACC_AUX_VBG2}$ | AUX ADC measurement result | 1.092 | 1.1 | 1.106 | V |
| $V_{ACC_AUX_VCM}$ | AUX ADC measurement result | 2.400 | 2.5 | 2.550 | V |
| $V_{ACC_AUX_AVAO_REF}$ | AUX ADC measurement result | 2.400 | 2.47 | 2.550 | V |
| $V_{ACC_AUX_AVDD_REF}$ | AUX ADC measurement result | 2.400 | 2.47 | 2.550 | V |
| $V_{ACC_AUX_OVDAC}$ | AUX ADC measurement result Setting at 4.475V; $T_A = -20^\circ C$ to $65^\circ C$ | 4.450 | 4.500 | 4.500 | V |
| $V_{ACC_AUX_OVDAC}$ | AUX ADC measurement result Setting at 4.475V; $T_A = -40^\circ C$ to $105^\circ C$ | 4.445 | 4.500 | 4.500 | V |
| $V_{ACC_AUX_OVDAC}$ | AUX ADC measurement result Setting at 4.475V; $T_A = -40^\circ C$ to $125^\circ C$ | 4.445 | 4.500 | 4.500 | V |
| $V_{ACC_AUX_OVDAC}$ | AUX ADC measurement result Setting at 3.8V | 3.770 | 3.825 | 3.825 | V |
| $V_{ACC_AUX_OVDAC}$ | AUX ADC measurement result Setting at 3V | 2.970 | 3.030 | 3.030 | V |
| $V_{ACC_AUX_UVDAC}$ | AUX ADC measurement result Setting at 3.1V | 3.095 | 3.1 | 3.150 | V |
| $V_{ACC_AUX_VCBDONE_DAC}$ | AUX ADC measurement result Setting at 4V | 3.950 | 4 | 4.050 | V |
| $V_{ACC_AUX_OTDAC}$ | AUX ADC measurement result Setting at 39% | 1.900 | 1.95 | 2.000 | V |
| $V_{ACC_AUX_UTDAC}$ | AUX ADC measurement result Setting at 80% | 3.950 | 4 | 4.050 | V |
| $V_{ACC_MAIN_TSREF}$ | Main ADC measurement result | 4.975 | 5 | 5.025 | V |
| $V_{ACC_MAIN_DIETEMP_P}$ | Total channel accuracy for Die Temp1 measurement (+/-) | | | 3 | °C |
| $V_{ACC_AUX_DIETEMP}$ | Total channel accuracy for Die Temp2 measurement (+/-) | | | 6 | °C |
| $I_{SRP_N_Diff}$ | Differential SRN/SRP input current (CS and main ADC are on) | Apply 100mV differential across SRP/SRN | | 1.4 | μA |

7.5 Electrical Characteristics (续)

over operating -40°C to 125°C free-air temperature range, VBAT = 9V to 32V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--|---|------|-----|-------------------|
| V _{RANGE_CS} | Effective input range of CS ADC | -100 | 100 | | mV |
| V _{NOISE_CS} | CS ADC input referred noise | CS_DS[1:0] = 11, CS ADC in continuous mode, short SRP/SRN at pins | 0.71 | | uV _{RMS} |
| Gain_error_cs_room_uncal | Gain error of CS ADC @25°C, it could be single temp point calibrated out | T _A = 25°C, CS_DS[1:0] = 01, measured at -75mV and 75mV | -0.6 | 0.6 | % |
| Gain_error_cs_drift1 | Gain error of CS ADC drift over temperature, V _{RANGE_CS} < 100mV | T _A = -20°C to 85°C, CS_DS[1:0] = 01, measured at 50mV and 75mV | 0.3 | | % |
| | | T _A = -40°C to 105°C, CS_DS[1:0] = 01, measured at 50mV and 75mV | 0.3 | | % |
| Offset_cs_room_uncal | Input referred offset error of CS ADC @ 25°C, it could be single temp point calibrated out | T _A = 25°C, CS_DS[1:0] = 01, short SRP/SRN at pins | -6 | 6 | uV |
| Offset_cs_drift | Input referred offset error drift over temperature | T _A = -40°C to -20°C, CS_DS[1:0] = 01, short SRP/SRN at pins | -2.5 | 2.5 | uV |
| | | T _A = -20°C to 105°C, CS_DS[1:0] = 01, short SRP/SRN at pins | -1.8 | 1.8 | uV |

Reference Voltages

| | | | | | |
|-------------------|------------------------|-------|---|-------|---|
| V _{REFH} | REFHP to REFHM voltage | 4.975 | 5 | 5.025 | V |
|-------------------|------------------------|-------|---|-------|---|

HW Voltage Comparator/Protector (CELL OV/UV)

| | | | | | |
|----------------------------|--|---------------------------------|------|------|----|
| V _{OV_COMP_RANGE} | OV comparator detection threshold setting range (not accuracy) | Step of 25mV | 2700 | 3000 | mV |
| | | Step of 25mV | 3600 | 3800 | mV |
| | | Step of 25mV | 4175 | 4500 | mV |
| V _{ov_comp_hys} | OV comparator hysteresis after detection | | 50 | | mV |
| V _{ov_comp_acc} | OV comparator accuracy | T _A = -20°C to 65°C | -24 | 24 | mV |
| | | T _A = -40°C to 105°C | -28 | 28 | mV |
| V _{uv_comp_range} | UV comparator detection threshold setting range (not accuracy) | Step of 50mV | 1200 | 3100 | mV |
| V _{uv_comp_hys} | UV comparator hysteresis after detection | | 50 | | mV |
| V _{uv_comp_acc} | UV comparator accuracy | T _A = -20°C to 65°C | -35 | 35 | mV |
| | | T _A = -40°C to 105°C | -50 | 50 | mV |

HW Temperature Comparator/Protector (NTC OT/UT)

| | | | | | |
|----------------------------|--|---|------|-----|---|
| V _{ot_comp_range} | OT comparator detection threshold setting range (not accuracy) | Step of 1%, ratiometric with respect to TSREF | 10 | 39 | % |
| V _{ot_comp_hys} | OT comparator hysteresis after detection | | 2 | | % |
| V _{ot_comp_acc} | OT comparator accuracy | | -0.5 | 0.5 | % |
| V _{ut_comp_range} | UT comparator detection threshold range | Step of 2%, ratiometric with respect to TSREF | 66 | 80 | % |
| V _{ut_comp_hys} | UT comparator hysteresis after detection | | 2 | | % |
| V _{ut_comp_acc} | UT comparator accuracy | | -0.5 | 0.5 | % |

Digital I/Os (TX, RX, GPIO, SPI CONTROLLER)

| | | | | | |
|-----------------|--|--|-----------------------|-----|---|
| V _{oh} | Output as logic level high (TX, GPIO as output) | GPIO is configured as output. I _{out} = 1mA | V _{cvdd-0.3} | | V |
| V _{ol} | Output as logic level low (TX, NFAULT, GPIO as output) | GPIO is configured as output. I _{out} = 1mA | | 0.3 | V |

7.5 Electrical Characteristics (续)

over operating -40°C to 125°C free-air temperature range, VBAT = 9V to 32V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|---|---|--------------------------|--------------------------|------|
| V _{IH} | Input as logic level high (RX, GPIO as fault input) | GPIO is configured as input. I _{OUT} = 1mA | 0.75 x V _{CVDD} | | V |
| V _{IL} | Input as logic level low (RX, GPIO as fault input) | GPIO is configured as input. I _{OUT} = 1mA | | 0.25 x V _{CVDD} | V |
| R _{WK_PU} | GPIO weak pull-up resistance | | 20 | 37 | 60 |
| R _{WK_PD} | GPIO weak pull-down resistance | | 20 | 40 | 60 |

7.6 Timing Requirements

over operating -40°C to 125°C free-air temperature range, VBAT = 9V to 32V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|--------------------------------|--|--|-----|-----|------|
| POWER STATE TIMING | | | | | |
| t _{SU(WAKE_SHUT)} | Startup from SHUTDOWN to ACTIVE mode | From the end of WAKE ping to ready to accept UART command | 6 | 10 | ms |
| t _{SU(SLP2ACT)} | Startup from SLEEP to ACTIVE mode (with SLEEP2ACTIVE ping/tone) (Not available for standalone device) | From the end of SLEEP2ACTIVE ping to ready to accept UART command | | 230 | μs |
| t _{SU(WAKE_SLP)} | Startup from SLEEP to ACTIVE mode (with WAKE ping/tone)(Not available for standalone device) | From the end of WAKE ping to ready to accept UART command | | 1 | ms |
| t _{SLP} | From ACTIVE to SLEEP mode | From receiving SLEEP entry condition to enter in SLEEP mode | | 100 | μs |
| t _{SHTDN} | From ACTIVE to SHUTDOWN mode | From receiving SHUTDOWN entry condition to enter in SHUTDOWN mode (all LDOs in 10% of their nominal value) | | 20 | ms |
| t _{RST} | Reset time during ACTIVE mode | CONTROL1[SOFT_RST] = 1 is sent to a completion of the digital reset | | 1 | ms |
| t _{HWRST} | The time device will be in HW reset, after HW reset ping/tone issued | | | 75 | ms |
| SUPPLIES TIMING | | | | | |
| t _{TSREF_ON} | TSREF ramp up time (10%-90%) | C _{TSREF} = 1μF | 6 | | ms |
| t _{TSREF_OFF} | TSREF ramp down time (90%-10%) | C _{TSREF} = 1μF | | 8 | ms |
| PING SIGNAL TIMING | | | | | |
| t _{HLD_WAKE} | WAKE ping low time on RX pin; no external load on CVDD | | 2 | 2.5 | ms |
| t _{HLD_SD} | SHUTDOWN ping low time on RX pin; no external load on CVDD | | 7 | 10 | ms |
| t _{UART(SIA)} | SLEEPtoACTIVE ping low time on RX pin | | 250 | 300 | μs |
| t _{HLD_HWRST} | HW_RESET ping low time on RX pin | | 36 | | ms |
| MAIN and AUX ADC TIMING | | | | | |
| t _{SAR_CONV} | Single conversion time (both Main and AUX ADCs) | | 8 | | μs |
| t _{MAIN_ADC_CYCLE} | Single round robin cycle (Main ADC) | | 192 | | μs |
| t _{AUX_ADC_CYCLE} | Single round robin cycle (AUX ADC) | | 192 | | μs |
| t _{AFE_SETTLE} | Analog front end (Level shifters) settling time whenever device enter ACTIVE mode from SLEEP or SHUTDOWN | | 4 | | ms |

7.6 Timing Requirements (续)

over operating -40°C to 125°C free-air temperature range, VBAT = 9V to 32V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT | |
|--|---|--|------|--------|------------|----|
| t_{CS_SETTLE} | CS ADC settling time | | | 62 | μs | |
| $t_{CS_REFRESH}$ | Continious mode refresh rate | CS_DS[1:0] = 11 | | 4.096 | ms | |
| $t_{CS_REFRESH}$ | Continious mode refresh rate | CS_DS[1:0] = 10 | | 1.024 | ms | |
| $t_{CS_REFRESH}$ | Continious mode refresh rate | CS_DS[1:0] = 01 | | 0.512 | ms | |
| $t_{CS_REFRESH}$ | Continious mode refresh rate | CS_DS[1:0] = 00 | | 0.256 | ms | |
| t_{CS_CONV} | Single conversion time on CS ADC | CS_DS[1:0] = 11 | | 12.350 | ms | |
| | | CS_DS[1:0] = 10 | | 3.134 | ms | |
| | | CS_DS[1:0] = 01 | | 1.598 | ms | |
| | | CS_DS[1:0] = 00 | | 0.83 | ms | |
| t_{ADC_ACC} | This includes mux round robin, ADC conversions, and digital filters. | | -1.5 | 1.5 | % | |
| BALANCING TIMING | | | | | | |
| t_{BAL_ACC} | Balancing timer accuracy | | -5 | 5 | % | |
| HW COMPARATORS/PROTECTORS TIMING | | | | | | |
| t_{OV_CYCLE} | OV round robin cycle | | | 8 | ms | |
| t_{UV_CYCLE} | UV round robin cycle | | | 8 | ms | |
| $t_{OVUV_BIST_CYCLE}$ | OV and UV BIST cycle | | 21.8 | 23 | 24.2 | ms |
| t_{OT_CYCLE} | OT round robin cycle | | | 4 | ms | |
| t_{UT_CYCLE} | UT round robin cycle | | | 4 | ms | |
| $t_{PWR_BIST_CYCLE}$ | Time needed for the power supply BIST to complete after the power BIST go command | | 10.9 | 11.5 | 12.1 | ms |
| $t_{OTUT_BIST_CYCLE}$ | OT and UT BIST cycle | | 19 | 20 | 21 | ms |
| $t_{HW_COMP_ACC}$ | OV,UV,OT,UT comparators timing accuracy | | -5 | 5 | % | |
| I/O TIMING (TX, RX, GPIO, NFAULT) | | | | | | |
| t_{RISE} | Rise Time | $V_{CVDD} > \text{MIN } V_{CVDD}$, $C_{LOAD} = 150\text{pF}$, GPIO in output mode | | 12 | ns | |
| t_{FALL} | Fall Time (exclude NFAULT) | $V_{CVDD} > \text{MIN } V_{CVDD}$, $C_{LOAD} = 150\text{pF}$, GPIO in output mode | | 7 | ns | |
| t_{FALL_NFAULT} | Fall Time on NFAULT | $V_{CVDD} > \text{MIN } V_{CVDD}$, $C_{LOAD} = 150\text{pF}$, $R_{PULLUP} = 10\text{k}\Omega$ | | 100 | ns | |
| UART TIMING | | | | | | |
| $UART_{BAUD}$ | UART TX/RX Baud Rate | | | 1 | Mbps | |
| $UART_{ERR_BAUD(RX)}$ | UART RX baud rate error - requirement on the external host | | -1 | 1 | % | |
| $UART_{ERR_BAUD(TX)}$ | UART TX baud rate error | | -1.5 | 1.5 | % | |
| $t_{UART(CLR)}$ | UART Clear low time | | 15 | 20 | bit period | |
| $t_{UART(RX_HIGH)}$ | After COMM CLEAR, wait this time before sending new frame | | 1 | | bit period | |
| OTP NVM TIMING | | | | | | |
| t_{CRC_CUST} | Time to complet a single cycle of CRC check on the customer OTP space | | | 175 | μs | |
| t_{CRC_FACT} | Time to complet a single cycle of CRC check on the factory OTP space | | | 1.6 | ms | |
| SPI CONTROLLER TIMING | | | | | | |

7.6 Timing Requirements (续)

over operating -40°C to 125°C free-air temperature range, VBAT = 9V to 32V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---------------------|--|------------------------------------|-------|-----|-------|------|
| f_{SCLK} | SCLK frequency | | 450 | 500 | 550 | kHz |
| t_{HIGH}, t_{LOW} | SCLK duty cycle | | | 50 | | % |
| $t_{CS(HIGH)}$ | CS HIGH latency time. Time from register write high to CS pin high | | | 4 | | μs |
| $t_{CS(LOW)}$ | CS LOW latency time. Time from register write low to CS pin low | | | 4 | | μs |
| $t_{SU(POCI)}$ | POCI input data setup time - requirement for slave device | POCI stable before SCLK transition | 100 | | | ns |
| $t_{HD(POCI)}$ | POCI input data hold time | POCI stable after SCLK transition | | 0 | | ns |
| OSCILLATOR | | | | | | |
| f_{HFO} | High frequency oscillator | | 31.52 | 32 | 32.48 | MHz |
| f_{LFO} | Low frequency oscillator | | 248.9 | 262 | 275.1 | kHz |

7.7 Typical Characteristics

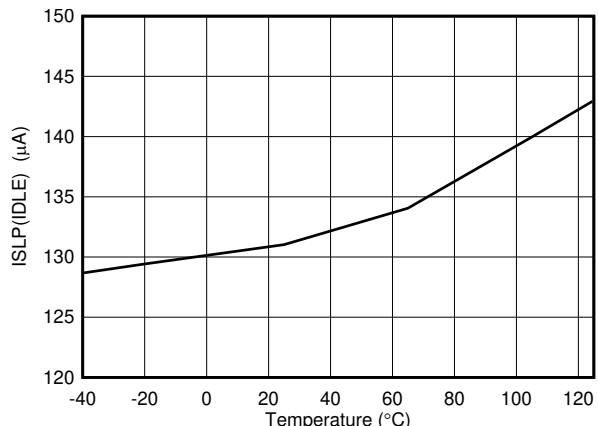


图 7-1. ISLP (IDLE) vs Temperature

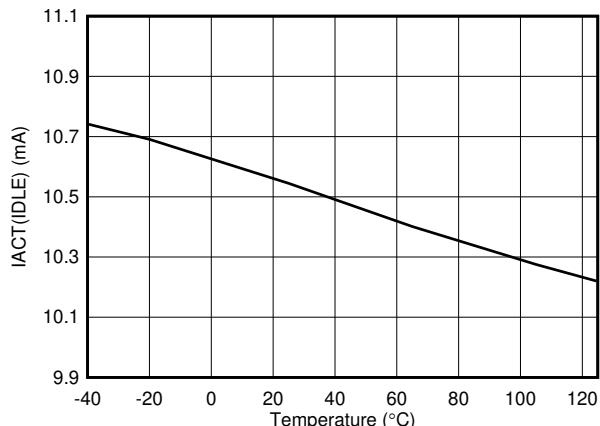


图 7-2. IACT (IDLE) vs Temperature

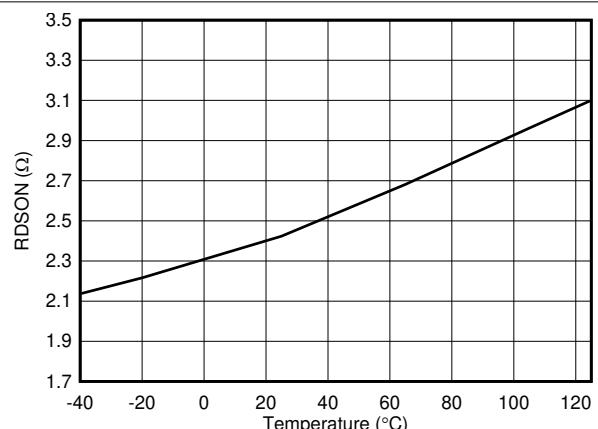


图 7-3. CBFET RDSON vs Temperature

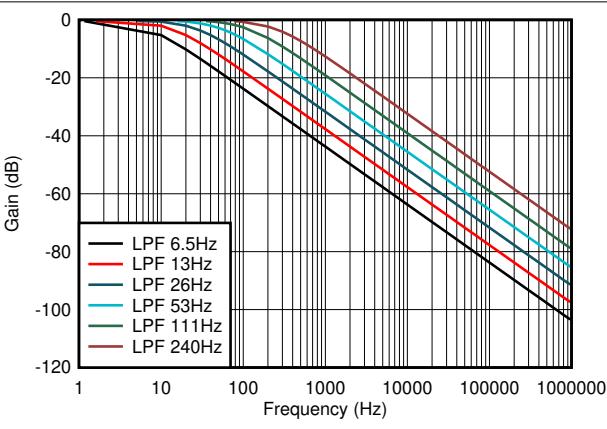


图 7-4. Digital Low Pass Filter

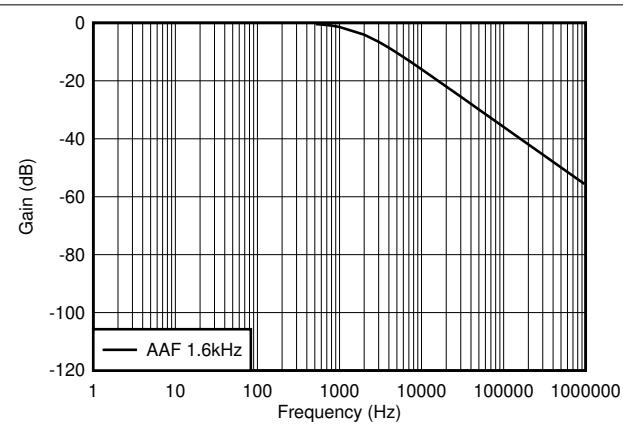


图 7-5. MAIN ADC Filter

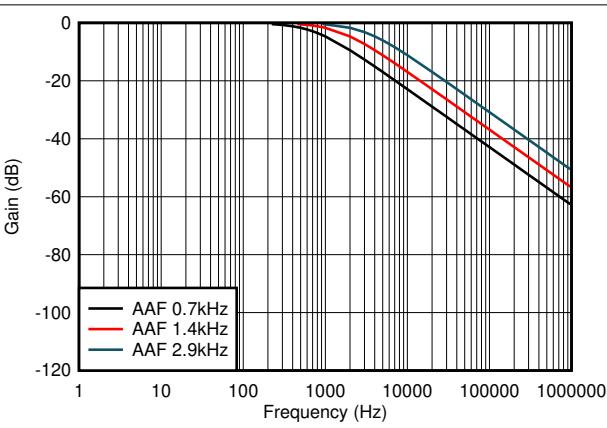


图 7-6. AUX ADC Filter

8 Detailed Description

8.1 Overview

The BQ756506-Q1 device is standalone battery monitor that measures cell voltages, temperature, and current. The device supports 4 series-connected (4S) battery cells with two extra channels to extend for 6 series (6S) cell measurements.

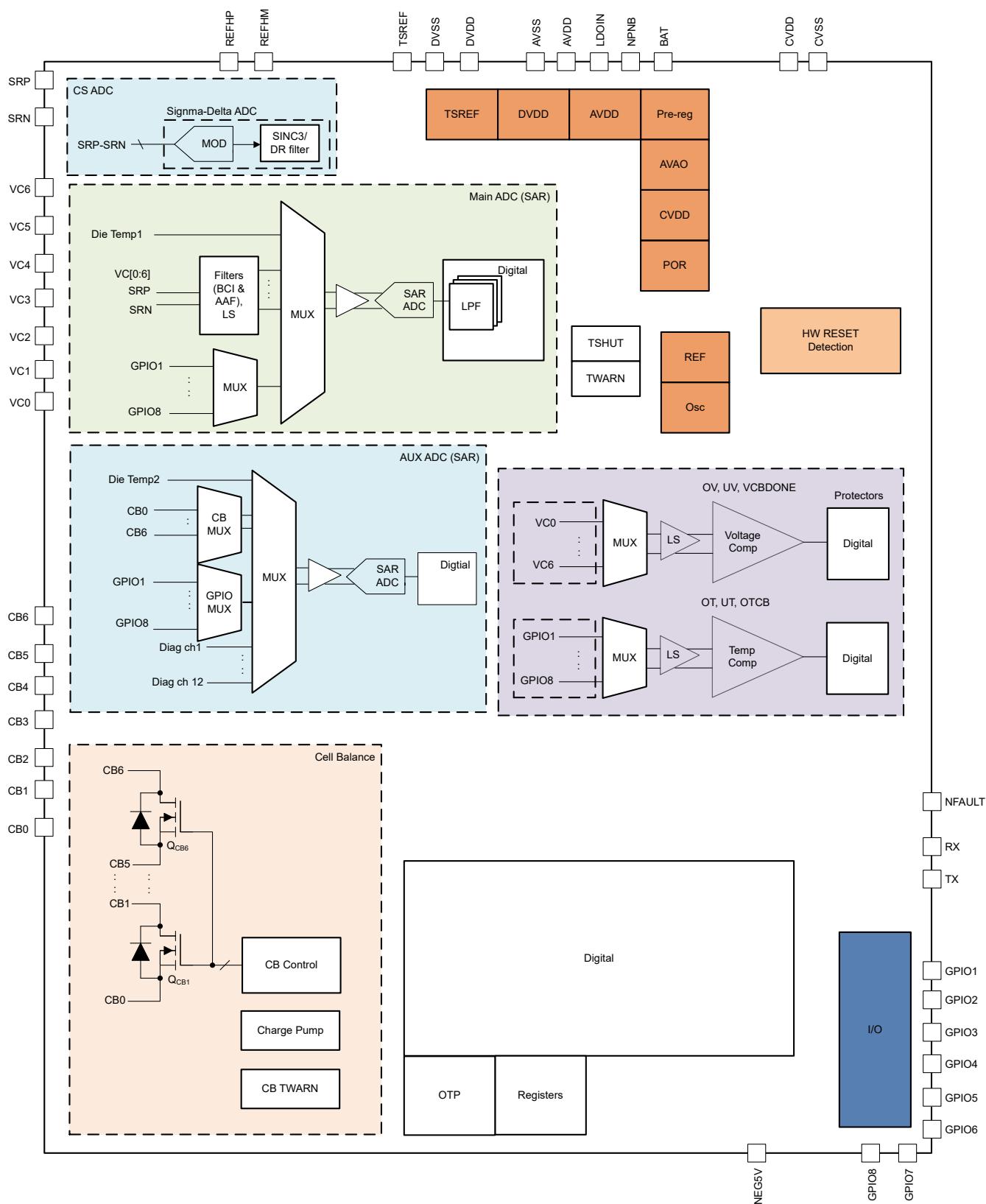
The device is ASIL-D compliant on voltage, temperature, current measurements, and communication. All cell voltages are measured within $128 \mu s$. Each cell sensing channel is included with a post-ADC digital low-pass filter (LPF) for noise reduction as well as providing moving average measurement results. The device has 8 GPIOs, all of which are configurable for NTC thermistor connections. The GPIOs can be used for fuse and relay diagnostics. All 8 GPIOs can be measured within 1.6 ms. An SPI controller is available through GPIO configuration. The device has multiple fault detections. The NFAULT pin can be triggered to alert the MCU when a fault condition is detected.

The device supports passive balancing through an internal cell balancing MOSFET (CBFET) for each cell. The balancing function runs autonomously without microcontroller (MCU) interaction. It includes an option to pause and then resume balancing based on a programmable threshold detected by the external thermistor or if the die temperature is too high (greater than $105^{\circ}C$). Once balancing starts, the device tracks the balancing time on each cell. MCU can read out the remaining balancing time at any time.

The device includes a hardware OVUV comparator and an OTUT comparator with user configurable thresholds. These can be used as a second-level protector for cell over and undervoltage and thermistor over- and undertemperature detections independent of ADC measurements.

The device has SLEEP and SHUTDOWN modes for lower power consumption. All functions work in ACTIVE mode, balancing and hardware comparators for OVUV and OTUT also work in SLEEP mode. While in SHUTDOWN, all active functions are turned off. A HW reset function is available and can be activated by the host MCU. The HW reset provides a POR-like event to the device without actual battery removal. This provides a reliable, low cost, and recoverable option to improve overall system robustness.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Supplies

The device generates directly from the battery stack all required supplies for its operation. The following subsections provide an overview of each internal supply block. See [节 9](#) for recommended component connection. See [节 8.3.6.4](#) for diagnostic control and fault detection on the power supplies block.

8.3.1.1 AVAO_REF and AVDD_REF

The AVAO_REF block (analog voltage always on) is powered from the BAT pin. It powers the always-on low-current circuits that are required for all power modes. This block also generates a preregulated reference, AVAO_REF. The AVAO_REF voltage passes through a load switch controlled by the SHUTDOWN mode. The reference voltage after the load switch is AVDD_REF.

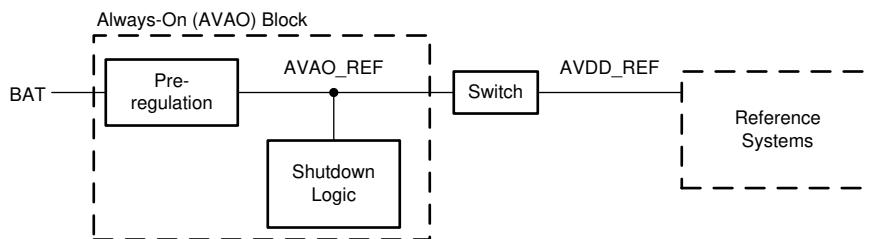


图 8-1. AVAO Block

8.3.1.2 LDOIN

The device is powered from the battery module in which the current draw for each cell is the same. From the top of the battery module, the device generates a 6-V regulated voltage (nominal) on the LDOIN pin through the internal linear regulator and an external NPN transistor. The NPNB pin controls the external NPN transistor of the regulator. The LDOIN output is the preregulated input to the rest of the internal low-dropout regulators (LDOs). During OTP (One-Time Programmable) memory programming, the LDOIN pin will be regulated to 8 V (nominal) to supply the programming voltage internally to the OTP programming. The LDOIN is turned off only during HW reset or a POR event.

8.3.1.3 AVDD

The AVDD LDO is the supply for the analog circuits. It takes the input voltage from LDOIN and generates a nominal 5 V. It will not be used to power any external circuit. This LDO is powered down in SHUTDOWN mode, during HW reset, or a POR event.

8.3.1.4 DVDD

The DVDD LDO is the supply for the digital circuits. It takes the input voltage from LDOIN and generates a nominal 1.8 V. It will not be used to power any external circuit. This LDO is powered down in SHUTDOWN mode, during HW reset, or a POR event.

8.3.1.5 CVDD and NEG5V

The CVDD LDO is the supply for the I/O pins (RX, TX, NFAULT, and GPIOs). It takes the input voltage from LDOIN and generates a nominal 5V. Besides providing power for internal usage, this LDO can support an extra 10mA external load in ACTIVE and SLEEP mode, whereas extra 5mA external load in SHUTDOWN mode.

There is a -5V charge pump used for Main ADC blocks. The NEG5V pin has a -4.6V output (nominal). It will be in a low-power burst mode when the device is in SLEEP or SHUTDOWN mode.

8.3.1.6 TSREF

The TSREF is a 5-V buffered reference that can bias the external thermistor circuits, allowing the ADCs to measure temperature and the OTUT protector to detect temperature faults. This reference is measurable by the

Main ADC. Both TSREF and GPIO measured by the Main ADC give a ratiometric measurement for best temperature measurement.

The TSREF is capable of supplying up to I_{TSREF_ILIMIT} and will not be used to power any external circuit other than the thermistor bias. The TSREF is off by default and can be enabled or disabled through the *CONTROL2[TSREF_EN]* bit. The startup time of TSREF is determined by the external capacitance. The MCU ensures TSREF is stable before making any GPIO measurement or OTUT protector detection. After enabling TSREF LDO, user shall wait 380 μ s before sending the next command.

8.3.2 Measurement System

There are two SAR ADCs in the device, a 16-bit Main ADC and a 14-bit AUX ADC; both use a precision reference (REFH) for high-accuracy measurement. Each ADC has its own independent control and can be enabled or disabled separately. The Main ADC is the main measurement for cell voltages (VCELL) and temperature through thermistors connecting to the GPIOs. It also provides TSREF and die temperature measurements. The AUX ADC is mainly used during diagnostic procedures such as providing measurements on internal reference voltages or DAC output of the OVUV and OTUT comparators. It serves as a redundancy measurement for cell voltage inputs and thermistor temperature input through the GPIOs.

A third ADC, 16-bit sigma-delta current sense ADC (CS ADC), is integrated to the device for dedicated current measurement. It is designed to work with a low-side current sense resistor. The current sense ADC measures the voltage drop across the current sense resistor with a full scale range of V_{CS_RANGE} .

The subsections below provide an overview of the Main, AUX and CS ADCs measurement paths. See [节 9](#) for the recommended external component connection. See [节 8.3.6.4](#) for the diagnostic control function and status of this block.

8.3.2.1 Main ADC

There are total of 24 inputs (slots) multiplexed to the Main ADC ([图 8-2](#)). All inputs are measured in round robin fashion ([图 8-3](#)). Each input takes 8 μ s (nominal) to measure and a single round robin cycle completes in 192 μ s (nominal). The inputs to the Main ADC are:

- Die temperature 1
- TSREF
- Cell1 to Cell6 voltages through differential $V_{C_{n-1}}$ to V_{C_n} , where $n = 1$ to 6
- Current sense input through SRP – SRN pins
- Multiplexed GPIO1 through GPIO8
- Spares (RSVD)

All measurements are reported in 16-bit hexadecimal in 2s complement. Results are reported to the corresponding *_HI (high-byte) and *_LO (low-byte) registers. First, convert the hexadecimal results to decimal values. Follow the equations in [表 8-1](#) to translate the result to μ V or $^{\circ}$ C.

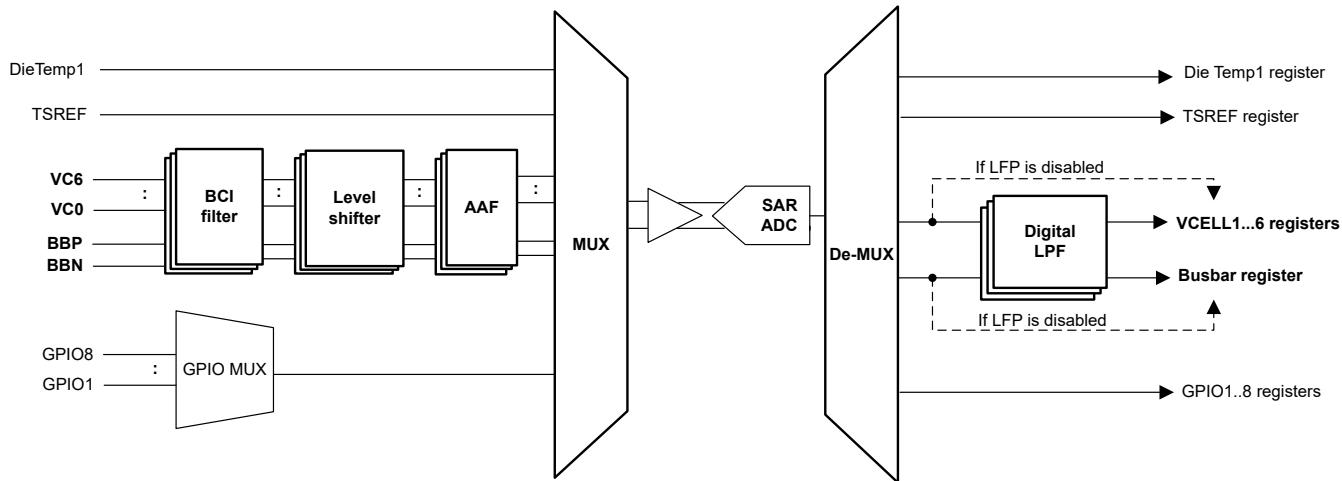
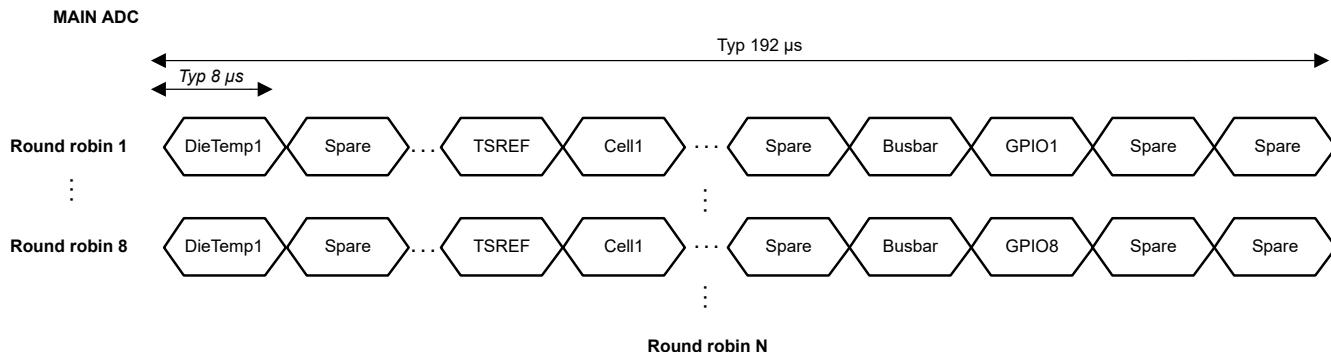
When the Main ADC is enabled, all Main ADC-related result registers shown in [表 8-1](#) are reset to the default value 0x8000. The measured result is populated to the result registers as the main ADC makes its conversion along the round robin cycle. When MCU reads the *_HI register, the device will pause the data refresh to the associated *_LO register until that *_LO register is read.

表 8-1. Main ADC Measurement Conversion Equations

| Main ADC Inputs | Result Registers | Conversion Equations |
|-------------------|--|---|
| Die Temperature 1 | <i>DIETEMP1_HI/LO</i> | Result in $^{\circ}$ C = $V_{LSB_MAIN_DIETEMP1} * \text{Result in decimal}$ 0x0000h is centered to 0 $^{\circ}$ C. |
| TSREF | <i>TSREF_HI/LO</i> | Result in μ V = $V_{LSB_TSREF} * \text{Result in decimal}$ |
| Cell1 to Cell6 | <i>VCELL*_HI/LO</i> , where * = 1 to 6 | Result in μ V = $V_{LSB_ADC} * \text{Result in decimal}$ |
| Current sense | <i>CSMAIN_HI/LO</i> | Result in μ V = $V_{LSB_CSMAIN} * \text{Result in decimal}$ |

表 8-1. Main ADC Measurement Conversion Equations (续)

| Main ADC Inputs | Result Registers | Conversion Equations |
|-----------------|-------------------------------|--|
| GPIO1 to GPIO8 | GPIO*_HI/LO, where * = 1 to 8 | Result in μ V = $V_{LSB_GPIO} * \text{Result in decimal}$ |

**图 8-2. Main ADC Measurement Path****图 8-3. Main ADC Round Robin Measurements**

8.3.2.1.1 Cell Voltage Measurements

8.3.2.1.1.1 Analog Front End

The cell voltage measurements of the Main ADC are taken from the VC0 through VC6 pins. The device allows a minimum of 4 cells to a maximum of 6 cells to be measured. The VC0 through VC6 pins are connected to the analog front end which consists of a BCI filter, level shifter, and an anti-aliasing filter (AAF) on each VC input channel. The BCI filter has a cutoff frequency (f_{cutoff}) of 100 kHz and the AAF has f_{cutoff} of 1.6 kHz. This filters out high-frequency noise on the VC input before going to the high-voltage multiplexer and measured by the Main ADC. The level shifter block is turned off to save power in SLEEP and SHUTDOWN modes.

8.3.2.1.1.2 VC Channel Measurements

The VC pins are the input channels for cell voltage measurements from the Main ADC measured in the Cell1 to Cell6 slots of the round robin. The round robin timing is always the same even if fewer than 6 cells are connected to the device (图 8-4). That is, for the inactive (or unused) VC channel, the device ignores the respective cell slot, but it does not remove the slot from the round robin cycle. This keeps a consistent measurement timing regardless of the cell number configuration. It also provides a consistent sampling time to the post-ADC digital LPF input.

To determine the number of active VCELL channels for ADC measurement, the *ACTIVE_CELL[NUM_CELL3:0]* parameter sets the highest active channel number. The device assumes any VC channel below the setting is also active.

The measurement results are reported in the corresponding *VCELL*_HI* (high-byte) and *VCELL*_LO* (low-byte) registers, where * = 1 to 6. If the digital LPFs are disabled, the result registers are reported with the single ADC conversion values; otherwise, the result registers are reported with filtered measurement values. For an inactive VC channel, the respective *_HI* and *_LO* registers remain with the default value 0x8000.

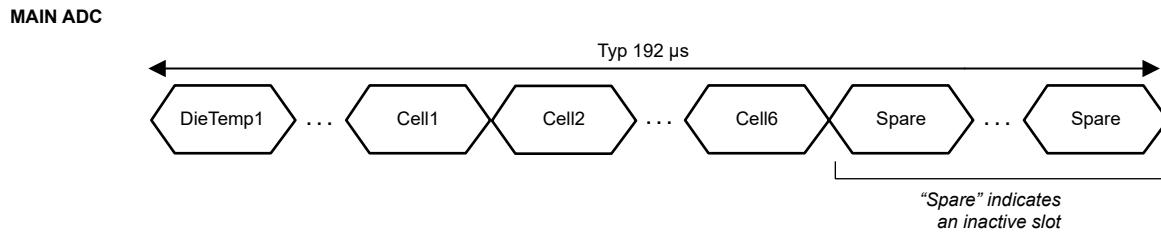


图 8-4. Same ADC Round Robin Timing for all Channel Counts

8.3.2.1.1.3 Post-ADC Digital LPF

Each differential VC channel measurement is equipped with a post-ADC LPF. The LPFs have much lower cutoff frequency (f_{cutoff}). There are 7 f_{cutoff} options: 6.5 Hz, 13 Hz, 26 Hz, 53 Hz, 111 Hz, 240 Hz, and 600 Hz, configurable through the *ADC_CONF1[LPF_VCELL2:0]* setting. Once an f_{cutoff} value is selected and the LPFs are enabled by setting *ADC_CTRL1[LPF_VCELL_EN]* = 1, the same f_{cutoff} setting applies to all VC channel measurements.

The differential SRP – SRN measurement also has its own digital LPF, enabled by *ADC_CTRL1[LPF_SR_EN]* bit. The LPF for the current sense channel through the Main ADC path has 7 f_{cutoff} options, configured using *ADC_CONF1[LPF_SR2:0]*.

The digital LPF is implemented as single-pole filter which responds very similarly as an analog RC circuit. This means the Main ADC will be running in continuous mode for the digital LPFs to produce effective filtered results.

The MCU should take into account the digital filter settling time when there is a step change in the input DC voltage level. Equation below gives a typical estimate of digital filter settling time to hit settling accuracy threshold for a step in VC voltage.

Digital Filter Settling Time $\sim [(\log_{10} (\text{Settling Accuracy Threshold [mV]}) / \text{Voltage Step in Input Voltage [mV]}) / (\log_{10}(1 - \text{Filter Coefficient})) - 1] \times 0.192 \text{ ms}$

| Fcutoff (Hz) | 600 | 240 | 111 | 53 | 26 | 13 | 6.5 |
|--------------------|-----|------|-------|--------|---------|----------|----------|
| Filter Coefficient | 0.5 | 0.25 | 0.125 | 0.0625 | 0.03125 | 0.015625 | 0.007813 |

For example: If VC step by 15mV, and user has to accommodate ~ 27 -ms settling time to within 1 LSB of input step for 26-Hz LPF setting.

When the LPF starts, from disabled to enabled state, it jumps to its first input value and starts the filtering from that point. As compared to starting from 0 V or some mid-level voltage, this implementation allows a fast settling time for Main ADC and LFP is just starting.

8.3.2.1.1.4 SRP and SRN Measurements

The SRP and SRN pins are the inputs for current sense measurement from the Main ADC. The intent of this measurement path is to serve as a redundancy current measurement. The SRP/N inputs have the BCI and AAF filters in the front end. This differential current sense measurement path has an option to pass-through a post-ADC digital LPF.

The Main ADC current sense measurement is reported in the *MAIN_CURRENT_HI* (high-byte) and *MAIN_CURRENT_LO* (low-byte) registers. If the digital LPF is disabled, the result registers are reported with the single ADC conversion value; otherwise, the result is reported in the filtered measurement value.

8.3.2.1.2 Temperature Measurements

8.3.2.1.2.1 DieTemp1 Measurement

There are 2 die temperature sensors, DieTemp1 and DieTemp2. The DieTemp1 is routed to the Main ADC and it is also used for the Main ADC gain and offset correction internally. The measurement is reported in the *DIETEMP1_HI* (high-byte) and *DIETEMP1_LO* (low-byte) registers. The 0°C measurement is centered to hex value 0x0000h, so a positive value represents a positive temperature and a negative value represents a negative temperature. The measurement is also capped off to +200°C and -100°C.

8.3.2.1.2.2 GPIOs and TSREF Measurements

There are eight GPIOs. All GPIO inputs are available to be used for thermistor connections for temperature measurements and be used as a simple, single-ended, voltage input measurement.

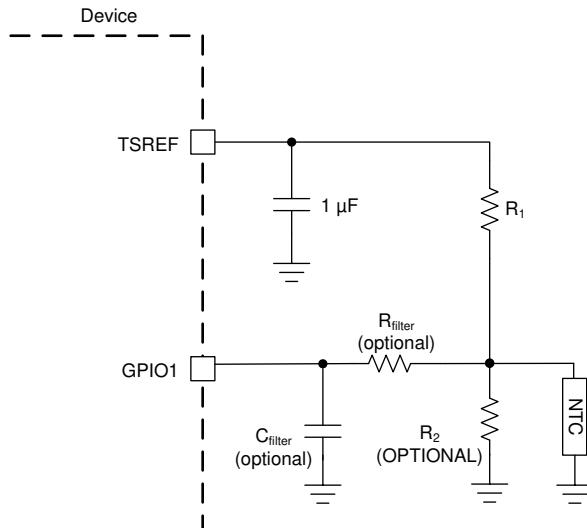


图 8-5. Thermistor Connection

图 8-5 shows the thermistor circuit when GPIO is enabled for thermistor measurements. MCU ensures TSREF is enabled by setting *CONTROL2[TSREF_EN]* = 1 and settled before taking the measurement value.

The GPIOs are multiplexed to one of the Main ADC MUX inputs. That is, in a single round robin cycle, only one GPIO is measured. To complete all eight GPIO measurements, it takes eight round robin cycles.

To enable the GPIO for ADC measurement, the corresponding *GPIO_CONF_n[GPIO*2:0]* (where $n = 1$ to 4, $*$ = 1 to 8 for the corresponding GPIO) register is configured to ADC input or ADC and OTUT input. For example, to enable GPIO1 for ADC measurement only, set *GPIO_CONF1[GPIO12:0]* to ADC input. See [节 8.3.5](#) for more details. If a GPIO is not configured for any ADC measurement, the device will ignore the corresponding GPIO slot but does not remove the slot from the round robin cycle. See [图 8-6](#) for an example when GPIO2 is configured for non-ADC measurement.

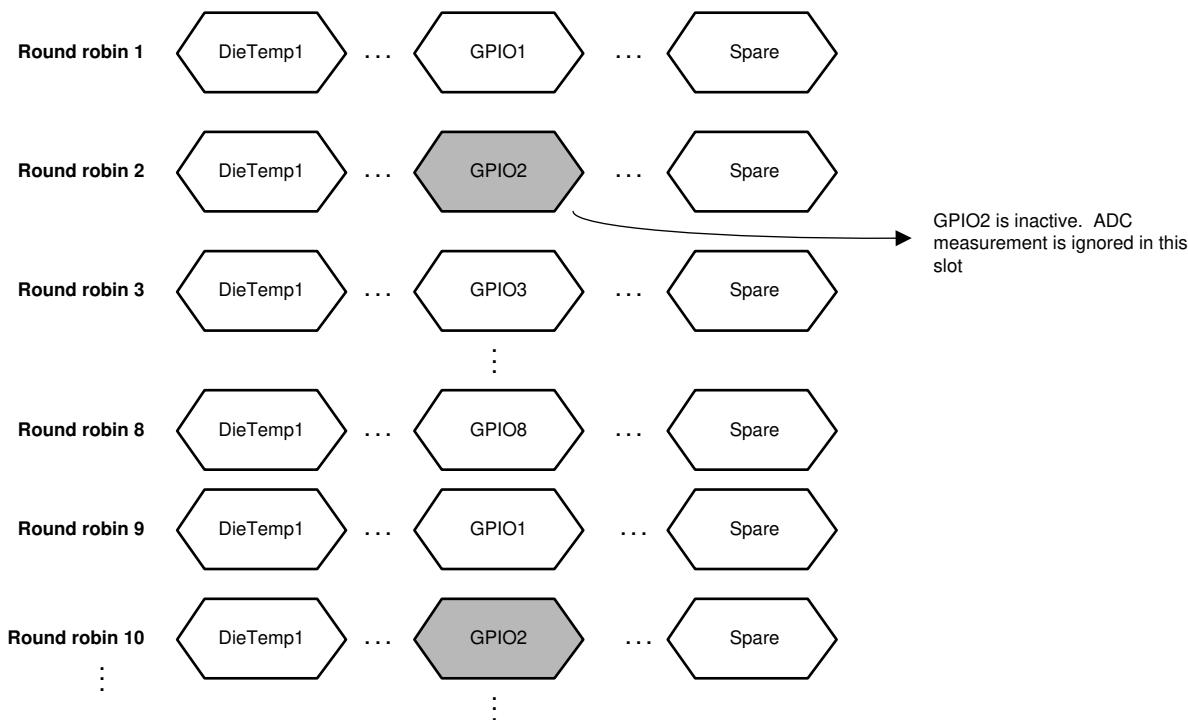
MAIN ADC


图 8-6. GPIO2 Not Configured for ADC Measurement

The measurements are reported in the corresponding *GPIO*_HI* (high-byte) and *GPIO*_LO* (low-byte) registers, where * = 1 to 8. The measurement result is in μ V. To achieve better temperature accuracy, the MCU can use a ratiometric measurement by using both TSREF and GPIO measurement with the following formula: $(\text{GPIO_ADC} / \text{TSREF_ADC}) = \text{RNTC} / (\text{RNTC} + \text{R1})$, where

- *GPIO_ADC* = ADC measurement on GPIO
- *TSREF_ADC* = ADC measurement on TSREF
- *RNTC* = NTC thermistor resistance
- *ACTIVE_CELL* register: Determine the inactive VC channel(s) and keep the result registers to default value 0x8000.
- *R1* is the pull-up resistor as shown in [图 8-5](#) with the assumption the *R2* is not used

For an inactive GPIO channel, the respective *_HI* and *_LO* registers remain with the default value 0x8000.

8.3.2.1.3 Main ADC Operation Control

8.3.2.1.3.1 Operation Modes and Status

The *ADC_CTRL1[CS_MAIN_GO]* = 1 will start both the Main ADC and the CS ADC. When the device receives the GO command, it first samples the following settings to determine and CS ADC configuration and then operates the and CS ADC accordingly. Any change of the settings below requires the MCU to resend another GO command to implement the new settings.

- *ADC_CTRL1[MAIN_MODE1:0]*: three run modes. See [表 8-2](#) for details.
- *ADC_CTRL1[LPF_VCELL_EN]*: LPF for VC channels. Set to *ADC_CONF1[LPF_VCELL2:0]* f_{cutoff} if enabled.
- *ADC_CTRL1[LPF_SR_EN]*: LPF for SRP/N channel. Set to *ADC_CONF1[LPF_SR2:0]* f_{cutoff} if enabled.
- *ADC_CONF2[ADC_DLY5:0]*: Delay the start of the Main ADC.
- *ACTIVE_CELL* register: Determine the inactive VC channel(s) and keep the result registers to default value 0x8000.

- *GPIO_CONF1* to *GPIO_CONF4*: Determine the inactive GPIO channel(s) and keep the result registers to default value 0x8000.

There are two status bits to indicate the Main ADC status:

- *DEV_STAT[MAIN_RUN]*: indicates if the Main ADC is running or not.
- *ADC_STAT1[DRDY_MAIN_ADC]*: set when at least eight round robin cycles have completed indicating all active GPIO channels and all other Main ADC inputs have at least one measurement completed.

表 8-2. Summary of Main ADC Run Modes

| [MAIN_MODE1:0] | Run Mode | Description |
|----------------|-------------------------------------|--|
| 0b00 | Stop Main ADC | Stop the Main ADC |
| 0b01 | 8 RR Run (eight round robin cycles) | Main ADC runs for eight round robin cycles then stops. This gives a single measurement on all cell voltages and all GPIO inputs to the system. Filtered measurements are not effective under run mode. For example, use as a quick burst read when MCU is periodically awake during system idle state. |
| 0b10 | Continuous Run | Main ADC runs in continuous mode and stops if [MAIN_MODE1:0] = 0b00 and a GO is sent. For example, must use this mode if LPF is enabled. Also use in diagnostic operation. |

The level shifter is enabled for the number of channels specified in the *ACTIVE_CELL[*NUM_CELL*3:0]* when device enters ACTIVE mode. MCU shall wait for t_{AFE_SETTLE} time before starting the Main ADC whenever the device enters ACTIVE mode or when [*NUM_CELL*3:0] setting is changed.

The Main and CS ADC operate in ACTIVE mode only. If the ADC is running while the device goes into SLEEP, the Main ADC will be “frozen” (that is, ADC is stopped but device still remembers the operational state). When the device returns to ACTIVE mode without any digital reset event, the Main ADC will restart and continues from its “pre-frozen” state. In this condition, the cell voltage measurements are off during the t_{AFE_SETTLE} time because input voltage to the ADC is not settled yet. MCU can ignore these measurements or send a new GO command to restart the Main ADC after t_{AFE_SETTLE} .

8.3.2.2 AUX ADC

There are a total of 24 inputs (slots) multiplexed to the AUX ADC (图 8-7). All inputs are measured in round robin fashion (图 8-8). Each input takes 8 μ s (nominal) to measure and a single round robin cycle completes in 192 μ s (nominal). The inputs to AUX ADC are:

- Die temperature 2
- Multiplexed differential CB_{n-1} to CB_n (AUXCELL1 to AUXCELL6), where $n = 1$ to 6 and differential current sense input through the SRP to SRN pins.
- MISC measurements:
 - BAT pin
 - REFL, internal reference
 - VBG2, internal bandgap
 - VCM, common voltage on Main ADC
 - AVAO_REF, always-on block reference
 - AVDD_REF
 - OV DAC from OV protector
 - UV DAC from UV protector
 - VCBDONE DAC from UV protector
 - OT or OTCB DAC from OT protector
 - UT DAC from UT protector
- Multiplexed GPIO1 to GPIO8
- Spares (RSVD)

All measurements are reported in 16-bit hexadecimal in 2s complement. Results are reported to the corresponding *_HI (high-byte) and *_LO (low-byte) registers. It first converts the hexadecimal results to decimal values. Follow the equations in 表 8-3 to translate the result to μ V or $^{\circ}$ C.

When the AUX ADC is enabled, all AUX ADC related result registers shown in 表 8-3 are reset to the default value 0x8000. The measured result is populated to the result registers as the AUX ADC makes its conversion along the round robin cycle. When MCU reads the *_HI register, the device will pause the data refresh to the associated *_LO register until that *_LO register is read.

表 8-3. AUX ADC Measurement Conversion Equations

| AUX ADC inputs | Result Registers | Conversion Equations |
|--|---|---|
| Die Temperature 2 | DIETEMP2_HI/LO | Result in $^{\circ}$ C = $V_{LSB_AUX_DIETEMP2} * \text{Result in decimal}$ Note: 0x0000h is centered to 0° C. |
| Multiplexed AUXCELL1 to AUXCELL6 and SRP/N channel | AUX_CELL_HI/LO, when CB MUX is locked to a single channel | Result in μ V = $V_{LSB_ADC} * \text{Result in decimal}$ |
| BAT | AUX_BAT_HI/LO | Result in μ V = $V_{LSB_AUX_BAT} * \text{Result in decimal}$ |
| REFL | AUX_REFL_HI/LO | |
| VBG2 | AUX_VBG2_HI/LO | |
| VCM | AUX_VCM_HI/LO | |
| AVAO_REF | AUX_AVAO_REF_HI/LO | |
| AVDD_REF | AUX_AVDD_REF_HI/LO | |
| OV DAC | AUX_OV_DAC_HI/LO | Result in μ V = $V_{LSB_AUX_DIAG} * \text{Result in decimal}$ |
| UV_DAC | AUX_UV_DAC_HI/LO | |
| VCBDONE DAC | AUX_VCBDONE_DAC_HI/LO | |
| OT or OTCD DAC | AUX_OT_OTCD_DAC_HI/LO | |
| UT DAC | AUX_UT_DAC_HI/LO | |
| Multiplexed GPIO1 to GPIO8 | AUX_GPIO_HI/LO | Result in μ V = $V_{LSB_GPIO} * \text{Result in decimal}$ |

Note that SRP/SRN pins are not connected to AUX ADC, if user selects [AUX_CELL_SEL] = 0x01 (SRP-SRN). In this case the user shall ignore the AUX_CELL_HI/LO results

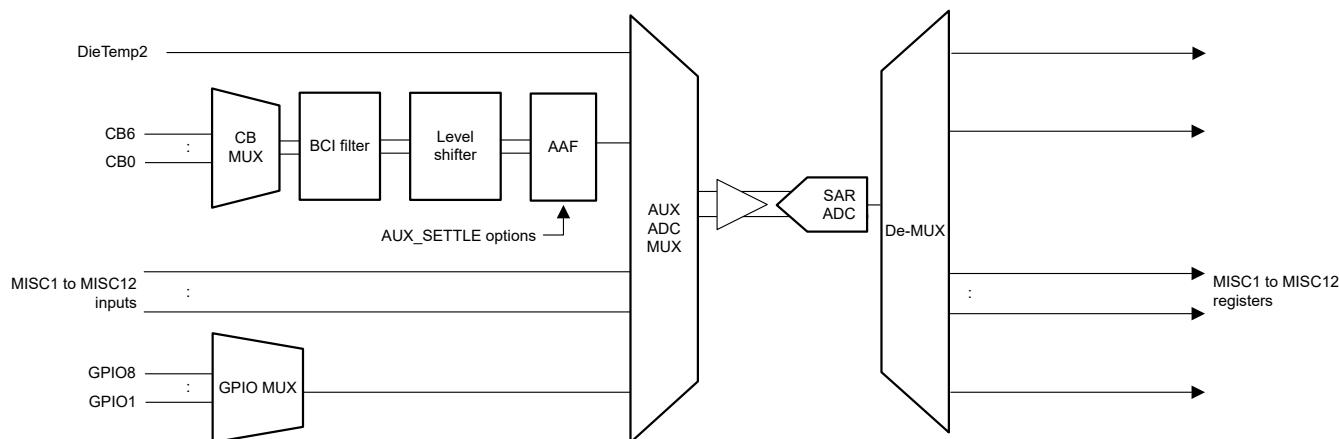


图 8-7. AUX ADC Measurement Path

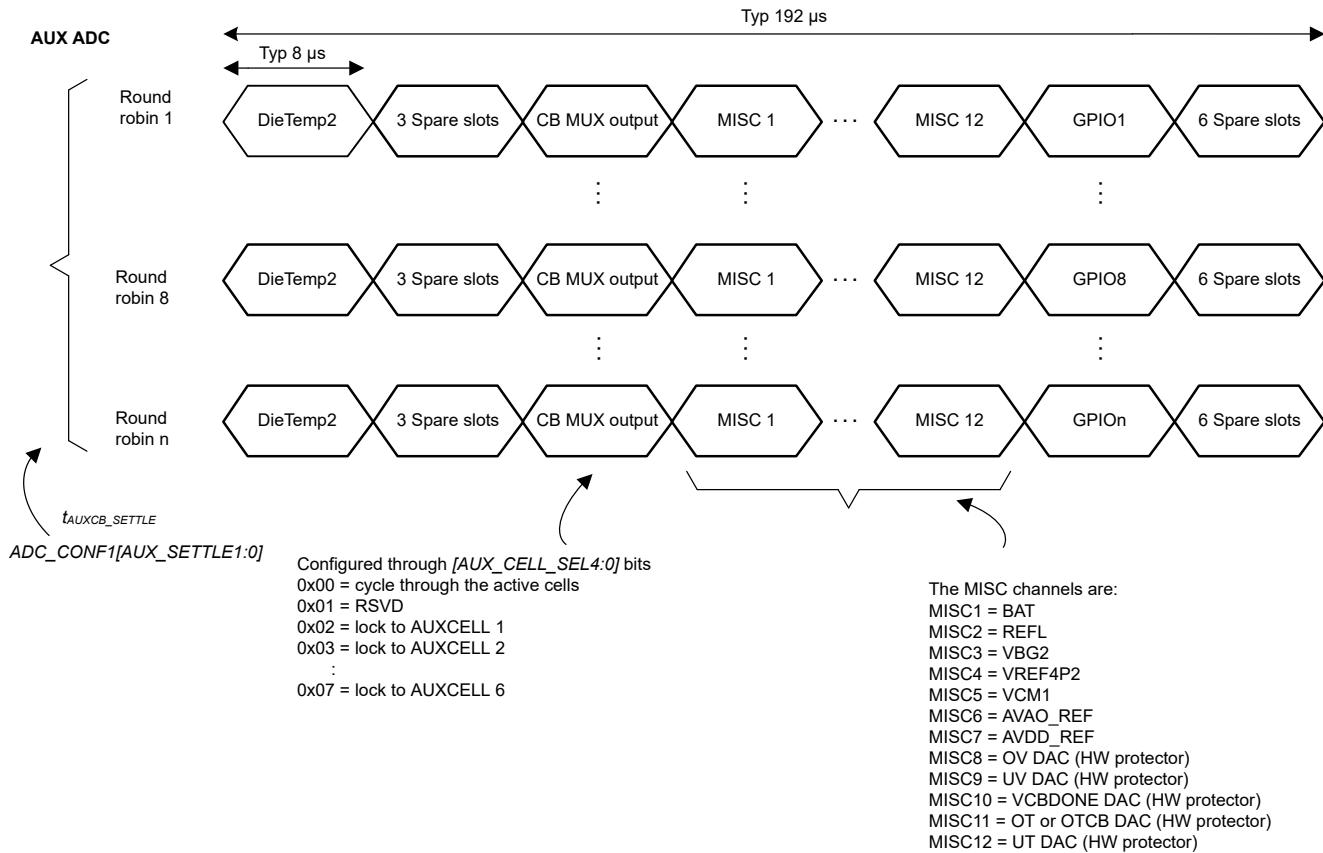


图 8-8. AUX ADC Round Robin Measurements

8.3.2.2.1 AUX Cell Voltage Measurements

8.3.2.2.1.1 AUX Analog Front End

The AUX ADC path serves as a redundancy path to the Main ADC measurement on cell voltage measurements and bus bar measurements. It also has the front end filters of a BCI filter and an AAF filter in the AUX ADC path. The AUXCELL channel and current sense channel (taken from SRP and SRN pins) in the AUX path are multiplexed (shown as the CB MUX in [图 8-7](#)) to share a single BCI filter and AAF filter. The CB MUX output after the front end filters is then going into one of the AUX ADC MUX and to the AUX ADC for measurement.

Because the front end filters are shared, the device has to wait for the AAF filter to settle before making any valid CB channel (AUXCELL) or SRP and SRN channel measurement. The default AAF f_{cutoff} is 1.6 kHz as in the Main ADC path, which translates to additional 4.3ms settling time to complete a single CB channel measurement. The device provides 3 AAF settling time options, 4.3ms (default), 2.3ms, and 1.3ms, configured by the *ADC_CONF1[AUX_SETTLE1:0]* bits. The BCI filter f_{cutoff} is 100 kHz as in the Main ADC path.

8.3.2.2.1.2 CB and Current Sense Channel Measurements

One slot, the CB MUX output slot, is assigned in the AUX ADC round robin cycle for the CB channels (differential $\text{CB}_{n-1} - \text{CB}_n$, where $n = 1$ to 6) and current sense (differential SRP - SRN) channel measurement because these channels are multiplexed to a single input to the AUX ADC multiplexer. For a single CB or current sense channel measurement, it takes multiple round robin cycles because the device has to wait for the AAF settling time as well.

Because of the need to wait for the AAF to settle, the AUX ADC would only measure CB and current sense channels that are active and are selected by the MCU; inactive or unselected channels are skipped.

Active CB channels are determined by the *ACTIVE_CELL[NUM_CELL3:0]* setting. These bits set the highest active channel number.

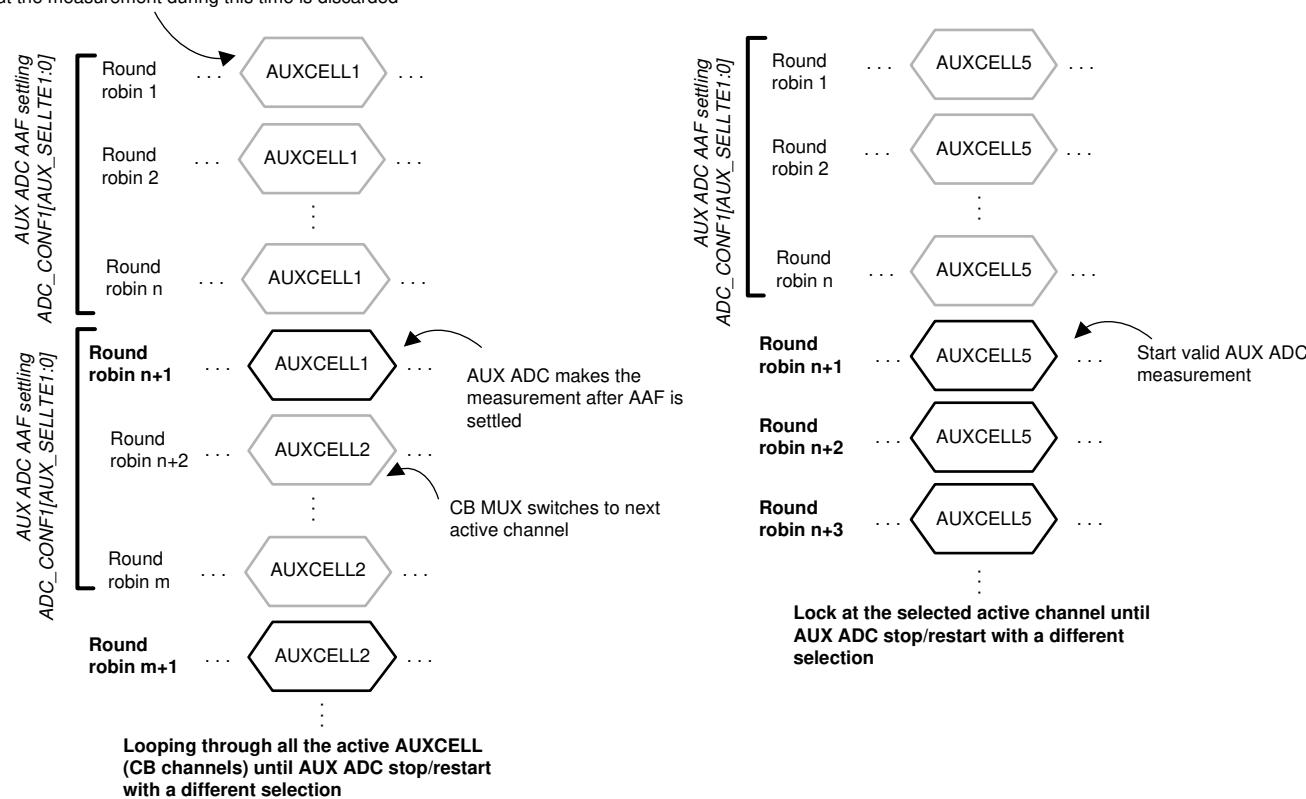
MCU can control which CB and current sense channels to be measured through the AUX ADC. The *ADC_CTRL2[AUX_CELL_SEL4:0]* gives the options to run through all the active CB channel and current sense channels or to lock to a single CB channels or lock to the current sense channel. 图 8-9 shows the example of how the AUXCELL slot is implemented with different *[AUX_CELL_SEL4:0]* setting.

It is recommended to run AUX ADC in continuous mode and all AUX ADC to measure through all the active CB channel once. This enables the device to reduce the common mode error in AUX ADC measurement. MCU shall perform this procedure before running ADC comparison related diagnostic or locking to a single CB or current sense channel measurement.

There is no post-ADC LPF in the AUX ADC path. When the AUX ADC measurements are used during diagnostics, the AUX CELL (CB channel) measurements are compared against the Main ADC prefiltered measurements. While the device performs VCELL (from Main ADC) to AUX CELL (from AUX ADC) measurement comparison internally. See [节 8.3.6.4](#) for more details.

The device makes the CB or current sense channel measurement available to read only when the *[AUX_CELL_SEL4:0]* bits are set to lock on a single CB (must be active) or current sense channel. The measurement is reported in the *AUX_CELL_HI* (high-byte) and *AUX_CELL_LO* (low-byte) registers. The result registers will be updated after the AAF settling time is passed. For any other conditions, including lock to an inactive CB channel, the result registers remain with the default value 0x8000.

CB MUX stays at the selected channel for the AUX ADC AAF settling time, but the measurement during this time is discarded



(a) *[AUX_CELL_SEL4:0]* = loop through all active CB channels

(b) *[AUX_CELL_SEL4:0]* = Lock to CB channel 5 (AUXCELL5)

图 8-9. CB MUX Output Slot with Different *[AUX_CELL_SEL4:0]* Setting

8.3.2.2.2 AUX Temperature Measurements

8.3.2.2.2.1 DieTemp2 Measurement

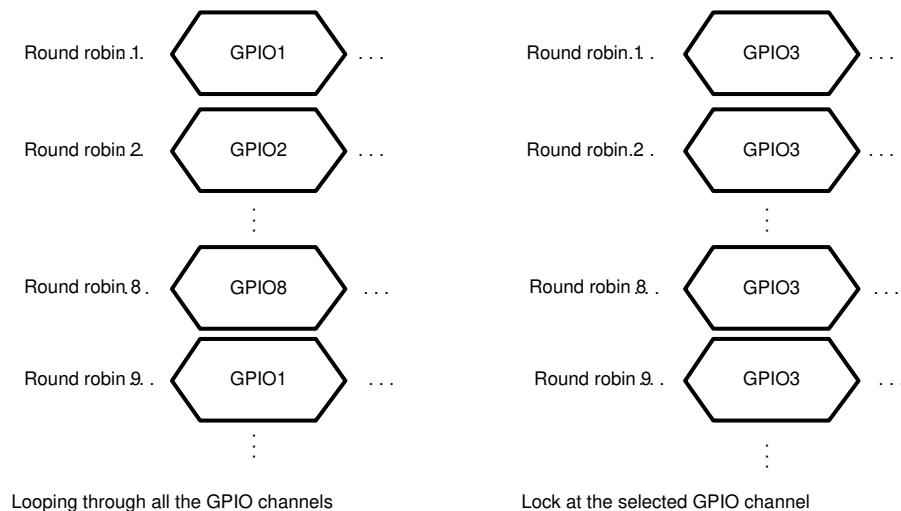
There are 2 die temperature sensors, DieTemp1 and DieTemp2. The DieTemp2 is routed to the AUX ADC and is also used for the AUX ADC gain and offset correction internally. The measurement is reported in the *DIETEMP2_HI* (high-byte) and *DIETEMP2_LO* (low-byte) registers. The 0°C measurement is centered to hex value 0x00, so a positive value represents positive temperature and a negative value represents negative temperature. The measurement is also capped off to +200°C and -100°C.

8.3.2.2.2.2 AUX GPIO Measurements

The AUX GPIO path is the same as the main GPIO path. All eight GPIOs are multiplexed to a single AUX ADC MUX input. There is only one GPIO slot in the AUX ADC round robin cycle. That is, in a single AUX ADC round robin cycle, only one GPIO will be measured. To complete all eight GPIO measurements, it takes eight round robin cycles. If GPIO is connected to the thermistor network, the MCU enables TSREF by setting *CONTROL2[TSREF_EN]* = 1 and ensures TSREF is stable before starting the AUX ADC measurement.

When AUX ADC is enabled, the GPIO slot in the 1st round robin cycle is GPIO1, 2nd round robin cycle is GPIO3, and so on. For the AUX ADC to make a measurement on a GPIO, the GPIO must be configured as ADC input or ADC and OTUT input in the corresponding *GPIO_CONF_n[GPIO*2:0]* bits, where $n = 1$ to 4, * = 1 to 8 for the respective GPIO channel. See [节 8.3.5](#) for more details. If the GPIO is inactive for the ADC measurement, the device ignores the corresponding GPIO slot but does not remove the slot from the AUX ADC round robin cycle.

By default, the AUX ADC loops through all GPIO channels and the measurements do not report out to the result registers. However, if MCU locks to a single GPIO channel, the locked GPIO measurement is reported to the *AUX_GPIO*_HI* (high-byte) and *AUX_GPIO*_LO* (low-byte) registers. This channel lock can be set by the *ADC_CTRL3[AUX_GPIO_SEL3:0]* bits. The result registers will report a GPIO measurement if *[AUX_GPIO_SEL3:0]* is locked to single GPIO channel, any other condition will show default value 0x8000.

(a) $[\text{AUX_GPIO_SEL3:0}] = \text{loop through all GPIO channels}$ (b) $[\text{AUX_GPIO_SEL3:0}] = \text{Lock to GPIO3}$ 图 8-10. GPIO Slot with Different $[\text{AUX_GPIO_SEL3:0}]$ Setting

8.3.2.2.3 MISC Measurements

There are 12 MISC measurements listed at the beginning of the AUX ADC section. When the AUX ADC is enabled, these inputs are measured in every round robin cycle. [表 8-3](#) shows the corresponding result registers.

The DAC inputs of the OVUV and OTUT protectors reflect the real-time DAC values of the device which shows the OVUV and OTUT detection or recovery threshold currently in use in the protectors. It is normal to observe a change of the DAC measurements if there are unused channels or if any cell or GPIO channels detect a fault. See [节 8.3.4](#) for description of the protector architecture and see [节 8.3.6.4](#) for the protector DAC measurement configuration.

8.3.2.2.4 AUX ADC Operation Control

To start the AUX ADC, the host MCU sets $ADC_CTRL3[AUX_GO]$ = 1. When the device receives the GO command, it first samples the following settings to determine the AUX ADC configuration, then operates the AUX ADC accordingly. Any change to the settings below requires the MCU to send another GO command to implement the new settings.

- $ADC_CTRL3[AUX_MODE1:0]$: Four run modes. See [表 8-4](#) for details.
- $ADC_CTRL2[AUX_CELL_SEL4:0]$: Selects which CB channels are measured by AUX ADC.
- $ADC_CONF1[AUX_SETTLE1:0]$: Configures the AUX ADC AAF settling time.
- $ADC_CTRL3[AUX_GPIO_SEL3:0]$: Selects which GPIO channels are measured by AUX ADC.
- $ACTIVE_CELL$ register: Determines the inactive CB channel(s).
- $GPIO_CONF1$ to $GPIO_CONF4$: Determines the inactive GPIO channel(s).

There are four status bits to indicate the AUX ADC status:

- $DEV_STAT[AUX_RUN]$: indicates if the AUX ADC is running or not.
- $ADC_STAT1[DRDY_AUX_MISC]$: set when all MISC inputs are measured at least once.
- $ADC_STAT1[DRDY_AUX_CELL]$: set when the CB channels selected by $[AUX_CELL_SEL4:0]$ are measured at least once.
- $ADC_STAT1[DRDY_AUX_GPIO]$: set when all GPIO channels (active or inactive) have been measured once. Inactive channel measurements will be ignored by the device.

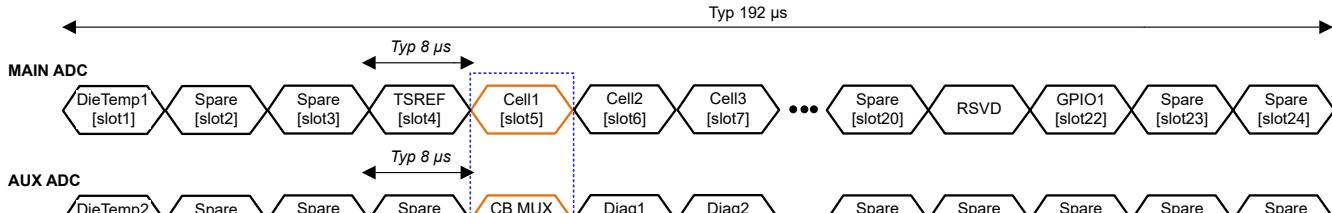
表 8-4. Summary of AUX ADC Run Modes

| [AUX_MODE1:0] | Run Mode | Description |
|----------------------|-------------------------------------|---|
| 0b00 | Stop AUX ADC | Stop the AUX ADC |
| 0b01 | Single Run (1 round robin cycle) | AUX ADC runs for one round robin cycle then stops. This gives a single measurement on all MISC inputs. For example, use as a quick burst read for just the MISC inputs without the need to issue a stop command to the AUX ADC. |
| 0b10 | Continuous Run | AUX ADC runs in continuous mode and stops if $[AUX_MODE1:0]$ = 0b00 and a GO command is sent. For example, must use this mode when ADC diagnostic comparison operation is used. See 节 8.3.6.4 for details. |
| 0b11 | 8 RR Run (eight round robin cycles) | AUX ADC runs for eight round robin cycles then stops. This gives a single measurement on all active GPIO inputs. |

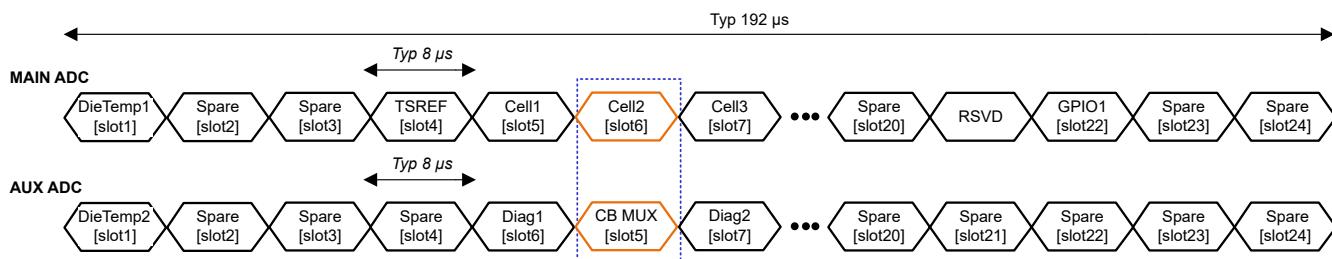
The AUX ADC operates in ACTIVE mode only. If the ADC is running while the device goes into SLEEP mode, the AUX ADC will be “freezed”; that is, the ADC stops but the device still remembers the operational state. When the device returns to ACTIVE mode without any digital reset event, the AUX ADC will restart and continue from its “prefreeze” state.

8.3.2.3 Synchronization Between MAIN and AUX ADC Measurements

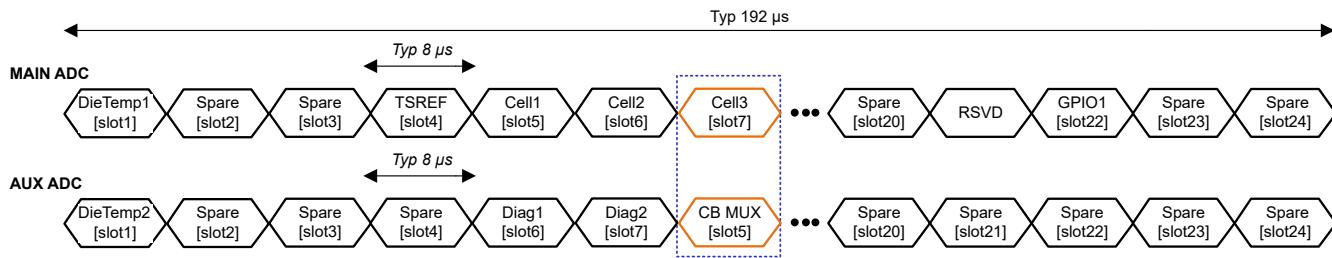
The device aligns AUX cell time slot number 5 with the target VC channel slot on MAIN cell. DieTemp2 starts without any delay, and AUX cell CB MUX slot #5 moves dynamically accordingly to match the selected MAIN cell and the remaining AUX ADC slots adjust accordingly. This ensures that there is no time skew between MAIN VC and AUX CB ADCs sampling. This feature helps improve the ASIL-D accuracy significantly.



a) [AUX_CELL_SEL] = 00h – Running all active cell channels set by ACTIVE_CELL_CONF register. Ch1 conversion.



b) [AUX_CELL_SEL] = 00h – Running all active cell channels set by ACTIVE_CELL_CONF register. Ch2 conversion.



c) [AUX_CELL_SEL] = 04h – Lock to AUX CELL 3. Ch3 conversion.

图 8-11. Synchronization Between MAIN and AUX ADC Sampling

8.3.2.4 CS ADC

The CS ADC is a high accuracy Delta-Sigma ADC with a SINC3 filter, dedicated for current sensing. It is used as divided down precision reference. The same precision reference is also used by the Main and AUX ADCs. The CS ADC block measures current by directly sensing the differential voltage across a sense resistor connecting between SRP and SRN pins. The CS ADC supports only low side sense resistor. The full scale ADC input range is -125mV to +125mV. If current sense ADC input is larger than Full Scale input voltage/125mV, CURRENT_HI/MID/LOW would be clamped around 75mV output reading. To verify, user could read MAIN_CURRENT_HI/LO.

The decimation ratio (DR) directly correlates to how quickly a conversion result is available to be read from the ADC. Lower DR corresponds to faster conversion time and lower effective number of bits (ENOB). The DR setting is controlled by *ADC_CTRL1[CS_DR1:0]*. The CS ADC shares the same start and mode control bits as the Main ADC located in *ADC_CTRL1* register. Both the Main and CS ADCs stop together. Such design is to allow better voltage and current measurement alignment.

The measurement is reported in 24-bit hexadecimal in 2s complement. Results are reported to the corresponding CURRENT_HI (high-byte), CURRENT_MID (mid-byte) and CURRENT_LO (low-byte) registers. It first converts the hexadecimal results to decimal values. Convert the result to μ V, where Result in μ V = $V_{LSB_CS} \cdot \text{Result in decimal}$.

After receiving the GO command, the CS ADC start its first conversion after t_{CS_SETTLE} . Since the CS ADC is using a SINC3 filter, the first conversion takes t_{CS_CONV} time to complete, but any subsequence conversion takes $(t_{CS_CONV} / 3)$ time to complete. If MCU needs to catch every current measurement conversion, GPIO1 has an option to toggle low every time a CS ADC conversion is completed, the pin returns high when MCU read *CURRENT_HI* register. This signal can be used as an interrupt to the MCU to avoid missing a conversion. This function is enabled by setting *GPIO_CONF2[CS_RDY_EN]* = 1.

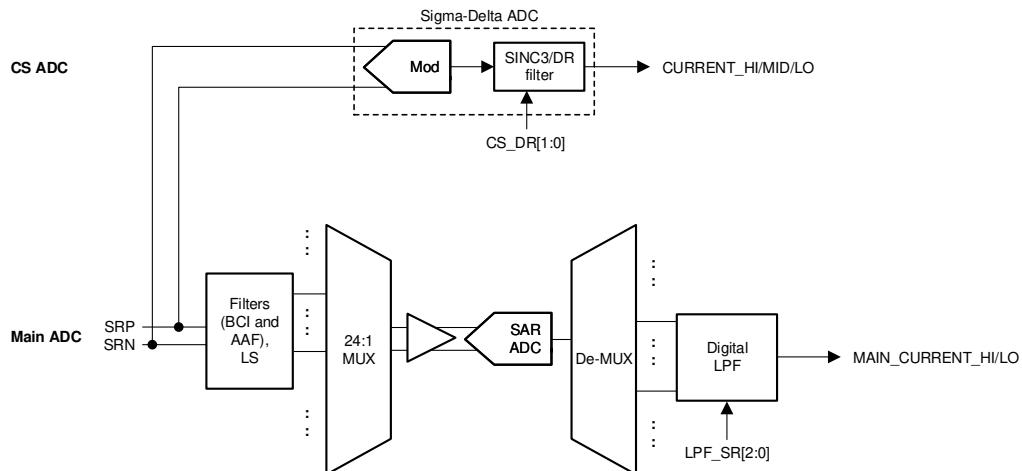


图 8-12. CS ADC

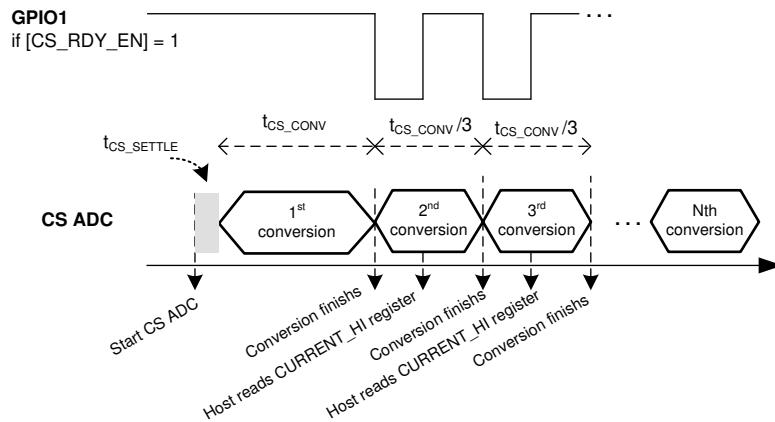


图 8-13. CS ADC Measurement

8.3.3 Cell Balancing

The device integrates internal cell balancing MOSFET (CBFET) across each CB channel to enable passive cell balancing. The balancing current is determined by the cell voltage, the external resistor in series with the CB pin, and the internal CBFET R_{dson} , R_{DSON} parameter. The following equations calculate the effective balancing current with or without adjacent CBFETs being on. Cell balancing can run in ACTIVE or SLEEP mode.

- Balancing with no consecutive CBFET on (图 8-14 (a)): $I_{CB} = V_{Cell} / ((2 \times R_{CB}) + R_{dson_{QCB}})$
- Balancing with two consecutive CBFETs on (图 8-14 (b)): $I_{CB} = (\text{Sum of two } V_{CELL}) / ((2 \times R_{CB}) + R_{dson_{QCBn}} + R_{dson_{(QCBn-1)}})$

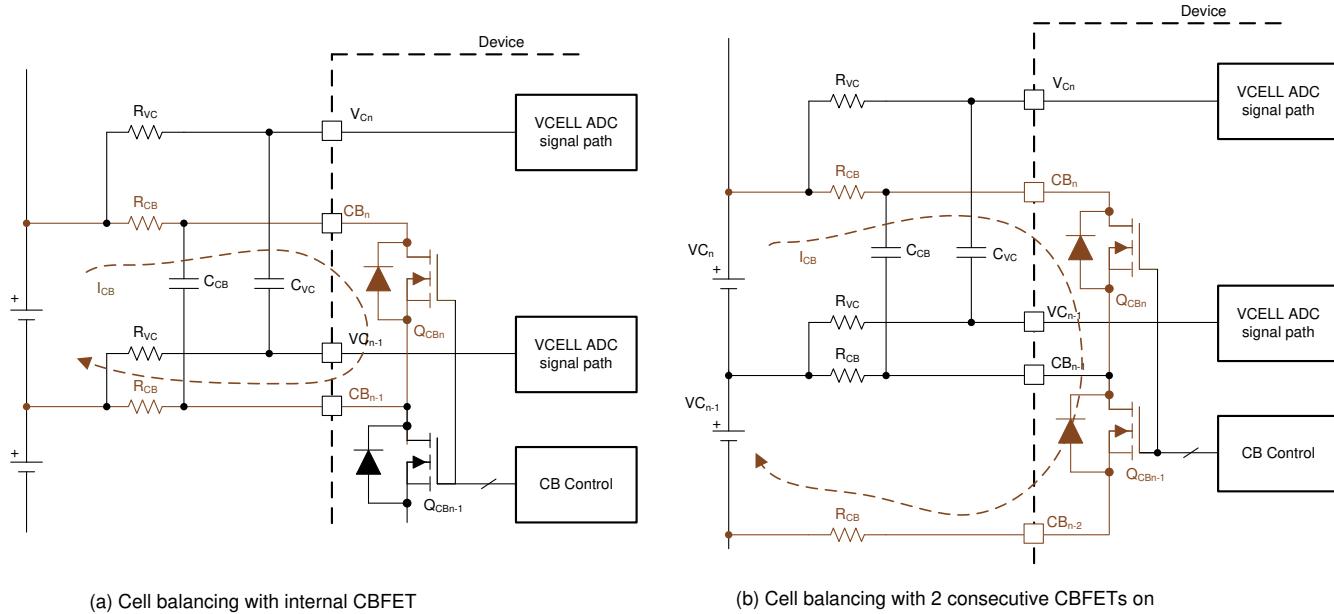


图 8-14. Internal Cell Balancing and the Flow of Balancing Current

8.3.3.1 Set Up Cell Balancing

There are three steps to set up cell balancing. Each step is described in detail in the following subsections. The host MCU follows the steps to configure the balancing control before starting cell balancing. Balancing starts by setting *BAL_CTRL2[BAL_GO]* = 1. The *BAL_STAT[CB_RUN]* = 1 indicates the cell balancing is actively running. Note that channels not selected by *ACTIVE_CELL[NUM_CELL3:0]* are bypassed during cell balancing.

1. Determine which channel to enable for cell balancing.
2. Select the cell balancing control methods, auto or manual balancing control.
3. Decide the additional control configuration:
 - a. Will the thermal management based on thermistor measurement be enabled?
 - b. Is cell balancing stop based on cell voltage?
 - c. Will cell balancing terminate if any unmasked fault is detected?

8.3.3.1.1 Step 1: Determine Balancing Channels

The device provides an individual balancing timer for each channel. The balancing timer is the primary control setting to start and stop the cell balancing on a channel. The balancing timer is configured by *CB_CELL_{*}_CTRL* registers, where * = 1 to 6 corresponding to CBFET 1 (CB channel 1) to CBFET 6 (CB channel 6). A non-zero value in these registers sets up the corresponding channels for balancing, but the CBFETs will not turn on until MCU issues the *BAL_CTRL2[BAL_GO]* = 1. When a channel balancing timer expires, cell balancing on that channel stops. Cell balancing can also stop with other conditions, like cell voltage below a certain threshold, unmasked fault is detected, or a forced stop by the host. 节 8.3.3.3 summarizes the cell balancing stop conditions.

8.3.3.1.2 Step 2: Select Balancing Control Methods

The cell balancing runs autonomously once it is configured. The cell balancing control can be configured in two ways using the *BAL_CTRL2[AUTO_BAL]* bit.

- Auto balancing control (*[AUTO_BAL]* = 1): With this method, host MCU can enable balancing on any channel. Once the host sends a *[BAL_GO]* = 1, balancing starts and the device will automatically duty cycle all enabled CBFETs in an odd and even manner. The duty cycle is configured by *BAL_CTRL1[DUTY2:0]* bits.
 - Example 1: MCU sets up all 6 channels for cell balancing.

Example: Both odd and even CB_CELL*_CTRL registers have non-zero setting

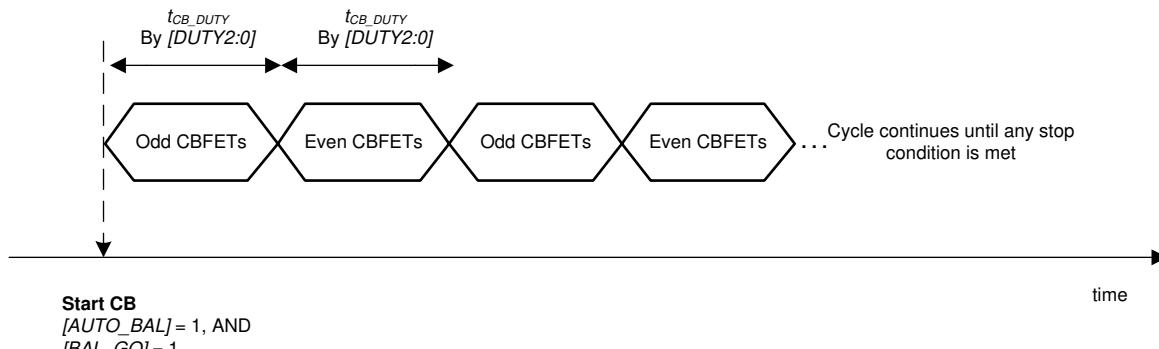


图 8-15. Auto Balancing Control, Example 1

- Example 2: MCU sets up odd or even channels only for cell balancing. The BAL_CTRL1[DUTY2:0] bits setting is ineffective because the device is not switched between odd or even channels.

Example: Odd CB_CELL*_CTRL registers have non-zero value
Even CB_CELL*_CTRL registers are all zero

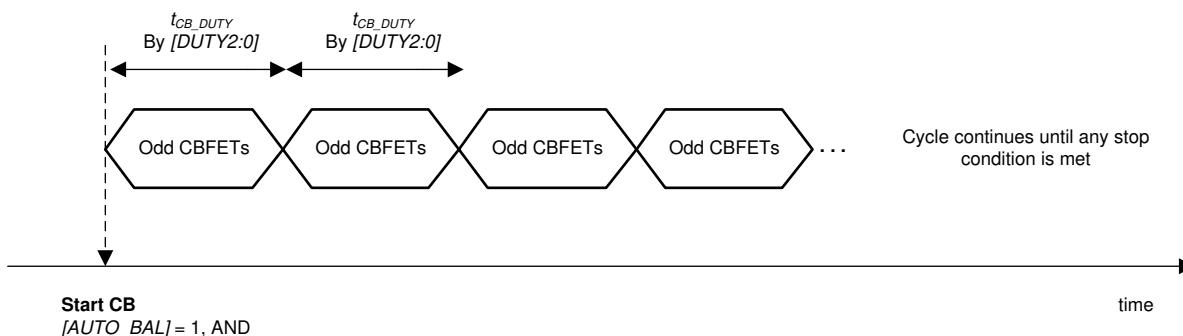


图 8-16. Auto Balancing Control, Example 2

- Manual balancing control ([AUTO_BAL] = 0): With this method, the device will turn on the CBFETs that have non-zero balancing timer settings once [BAL_GO] = 1 is received. There is no odd and even channel switching during the cell balancing and the BAL_CTRL1[DUTY2:0] setting does not apply under this control. Host MCU can enable two consecutive CBFETs with this method. When two consecutive CBFETs are enabled with both channels connected to battery cells, the balancing current is significantly different compared to no adjacent CBFET being on (图 8-14). The DEV_CONF[NO_ADJ_CB] bit is provided to avoid inadvertent enabling of an adjacent CBFET for a system that is not intended to have an adjacent channel on for balancing. In this control method, the device is relying on the MCU to enable the proper channels. If the MCU sends [BAL_GO] = 1 but the CBFETs are enabled with an invalid condition, the device will not start balancing and will set BAL_STAT[INVALID_CBCONF] = 1. Invalid configurations are either:
 - DEV_CONF[NO_ADJ_CB] = 1, but adjacent channels are enabled for balancing,
 - DEV_CONF[NO_ADJ_CB] = 0, but more than two consecutive channels are enabled for balancing:
 - Example: Enabling CBFET 1, 2, 4, 5 is valid.
 - Example: Enabling CBFET 1, 2, and 3 is invalid.

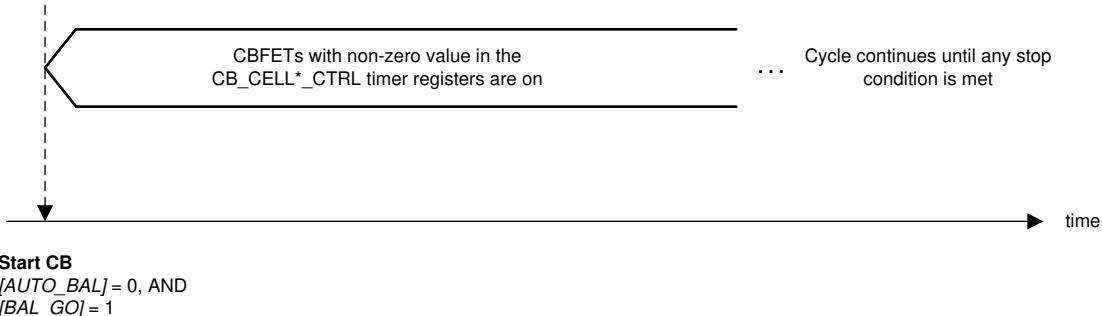


图 8-17. Manual Balancing Control

8.3.3.1.3 Step 3a: Balancing Thermal Management

With passive balancing, heat is generated through the internal CBFETs and the external balancing resistors. This creates 2 hotspots on the PCB, the device and the balancing resistors area. The device is designed to support up to 240mA at 75°C ambient. Higher balancing current can be supported with lower ambient temperature.

Nevertheless, the device provides two thermal management functions to avoid overheating the die as well as managing the PCB temperature. Both functions monitor temperature, either die temperature or thermistor temperature, to automatically pause balancing if temperature exceeds a pause threshold. When temperature falls below a recovery threshold, balancing will automatically resume. In the cell balancing pause state, all balancing timers and balancing settings are “freezed”, balancing will resume with the same configuration when the device is out of the pause state.

- CB TWARN Balancing Pause: There are die temperature sensors built near the internal CBFETs. When $[BAL_GO] = 1$ is sent, these temperature sensors are enabled. If any of the sensors detect a die temperature $>$ than the T_{CB_TWARN} threshold (105°C nominal), balancing on all channels is paused. The device sets the $BAL_STAT[CB_INPAUSE] = 1$ and $BAL_STAT[OT_PAUSE_DET] = 1$. When all sensors detect die temperature $< (T_{CB_TWARN} - T_{CB_HYS})$, cell balancing will resume on the balancing enabled channels.
- Thermistor OTCB Balancing Pause: To manage thermal increases due to external balancing resistors, the device has an option to pause cell balancing on all channels if any of the active thermistors connected to GPIOs detects a temperature greater than a threshold set by $OTCB_THRESH[OTCB_THR3:0]$. Once a OTCB detection is triggered, the $BAL_STAT[CB_INPAUSE] = 1$ and $BAL_STAT[OT_PAUSE_DET] = 1$. The balancing on all enabled channels will resume once all active thermistors detect a temperature less than a recovery threshold set by $(OTCB_THRESH[OTCB_THR3:0] + OTCB_THRESH[COOLOFF2:0])$. The OTCB detection is performed through the integrated OT protector. The protector must be turned on and running in round robin mode before cell balancing starts. See [节 8.3.4](#) for the protector control details. To use the OTCB function, MCU follows the setup sequence state below:
 - Before enabling OT protector:
 - GPIO used for this function will be configured to ADC and OTUT inputs.
 - $[OTCB_THR3:0]$ and $[COOLOFF2:0]$ are configured.
 - Enable the OT protector in round robin mode.
 - Set $[OTCB_EN]$ and $[BAL_GO]$ to 1.

Failure to do so may result in no OTCB pausing action or pausing at the wrong temperature. If a different OTCB or COOLOFF threshold is needed, MCU configures the new threshold values and then re-starts the OT protector to latch in the new setting. It is not required to resend the $[BAL_GO] = 1$.

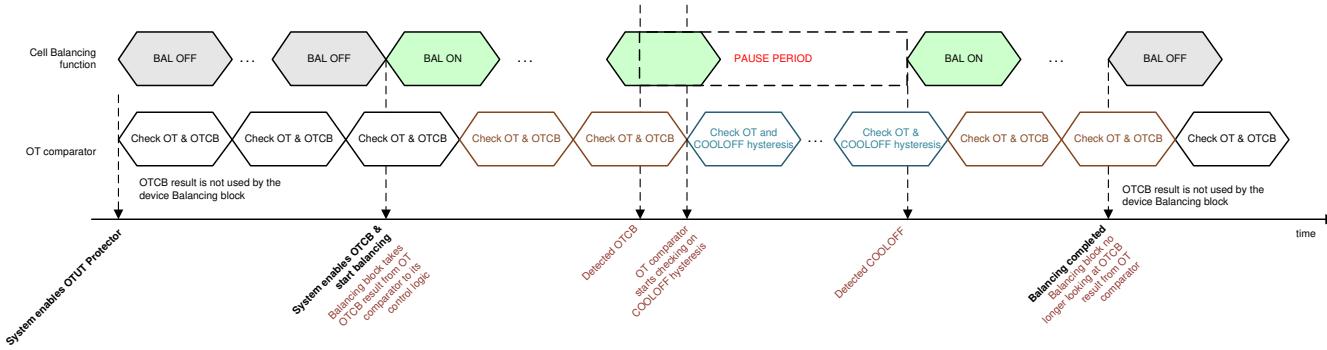


图 8-18. Cell Balancing Pause and Resume by OTCB Detection

8.3.3.1.4 Step 3b: Option to Stop On Cell Voltage Threshold

Besides the balancing timers, cell balancing can stop if the channel voltage is less than a threshold set by the *VCB_DONE_THRESH* register with a non-zero value. This stop voltage threshold applies to all channels. When this stop option is used, a channel will stop its balancing either if its balancing timer expires or its voltage level is less than *VCB_DONE_THRESH* setting.

The detection of the *VCB_DONE_THRESH* setting is performed by the integrated UV protector. The protector must be turned on and running in round robin mode before cell balancing starts. See [节 8.3.4](#) for the protector control details.

When using the *VCB_DONE* detection function, the MCU follows the setup sequence state below:

- Configure the *VCB_DONE_THRESH* register
- Enable the UV protector in round robin mode
- Send *[BAL_GO]* to 1

Failure to do so may result in no *VCB_DONE* detection or cell balancing stops at a wrong channel voltage. If different *VCB_DONE* thresholds are needed, MCU configures the new threshold values and then re-starts the UV protector to latch in the new setting. It is not required to resend the *[BAL_GO]* = 1.

8.3.3.1.5 Step 3c: Option to Stop at Fault

The device provides an option to abort cell balancing if an unmasked fault is detected. To enable this option, MCU sets *BAL_CTRL2[FLTSTOP_EN]* = 1 before starting cell balancing. If cell balancing is aborted under this condition, the *BAL_STAT[ABORTFLT]* = 1.

8.3.3.2 Cell Balancing in SLEEP Mode

Cell balancing can be operated in both ACTIVE and SLEEP modes. To run cell balancing in SLEEP mode, simply configure and start cell balancing in ACTIVE mode first. Once cell balancing is running, put the device in SLEEP mode. Cell balancing will continue autonomously in SLEEP mode. See [节 8.4](#) for description of putting device in SLEEP mode.

When cell balancing is completed with *BAL_STAT[CB_DONE]* = 1, there is an option to put the device in a different power mode by using the *BAL_CTRL2[BAL_ACT1:0]*. For example, setting *[BAL_ACT1:0]* to 0b10 (SHUTDOWN mode) and start cell balancing. When cell balancing is completed in all balancing enabled channels, the device will automatically enter SHUTDOWN mode without MCU interaction. See [节 8.3.3.3](#) for details about the *BAL_STAT[CB_DONE]* bit set conditions.

8.3.3.3 Pause and Stop Cell Balancing

8.3.3.3.1 Cell Balancing Pause

Cell balancing can be paused by one of three methods:

- If die temperature during balancing $> T_{CB_TWARN}$.
- If *[OTCB_EN]* = 1 when any thermistor detects a temperature greater than *OTCB_THR*.

- MCU sets *BAL_CTRL2[CB_PAUSE]* = 1.

The first two conditions are described in [节 8.3.3.1.3](#). The third pause condition is a MCU-controlled pause action usually used during a diagnostic check that involves the CB path. MCU can pause cell balancing through the *[CB_PAUSE]* bit at any given time once balancing starts.

When the cell balancing is paused due to any of the pause methods, the pause activity is the same:

- Turn off CBFETs on all channels.
- All balancing timers are in hold or “freeze” state.
- BAL_STAT[CB_INPAUSE]* = 1.
- Any unmasked fault detected during the pause state does not terminate cell balancing. This is because the pause event can be used during diagnostic and fault insertion can be part of the diagnostic.

Once the device exits the cell balancing pause state, the cell balancing resumes. Cell balancing timers will continue the count down. CB channels with non-zero values in their timers will continue with the balancing.

8.3.3.2 Cell Balancing Stop

Cell balancing stops in one of three conditions summarized in [表 8-5](#).

表 8-5. Cell Balancing Stop Conditions

| Stop Condition | Apply to Individual Channel? | Set <i>BAL_STAT[CB_DONE]</i> = 1? |
|--|---|--|
| Cell balancing timer expires | Yes, this stop condition is monitored per channel | Yes, when all channels meet either stop condition 1 or stop condition 2. |
| CB channel voltage < <i>VCB_DONE_THRESH</i> register value | Yes, this stop condition is monitored per channel | |
| <i>[FLTSTOP_EN]</i> = 1 and unmasked fault is detected | No, this stops cell balancing on all channels | No, instead set <i>BAL_STAT[ABORTFLT]</i> = 1 |

Additionally, MCU can also force stop cell balancing on any particular channel or on all channels by either:

- Zeroing out the balancing timer setting and issuing *[BAL_GO]* = 1.
- Setting a voltage greater than the CB channel voltage in the *VCB_DONE_THRESH* register and issuing *[BAL_GO]* = 1.

Because the cell balancing timer is the primary control to start cell balancing, if the MCU resets all balancing timers to 0 with *[BAL_GO]* = 1, the device does not start balancing and *BAL_STAT[CB_DONE]* remains 0.

On the other hand, if any of the cell balancing timers is non-zero but the *VCB_DONE_THRESH* register is set to a threshold greater than all CB channel voltages with *[BAL_GO]* = 1, the device starts cell balancing because of non-zero values on the balancing timers, but immediately stops because of the *VCB_DONE_THRESH* stop condition. The *BAL_STAT[CB_DONE]* is set to 1 for this condition.

8.3.3.3 Remaining CB Time

Each channel has a balancing timer, when balancing starts, the timers start counting down from the configured balancing time set by *CB_CELLn_CTRL* registers, where n= 1 to 6. When balancing is pause, these timers are paused.

To read the remaining CB time, MCU set *[BAL_TIME_SEL3:0]* to select a single channel, then issue *[BAL_TIME_GO]* = 1 which latch the remaining CB time of the selected channel to *BAL_TIME* register. Repeat the steps to read other remaining CB time on other channels. This timer information is only valid if CB is running, in pause state or in a valid CB stop condition.

If *BAL_TIME* register reports 0x7F or 0xFF, which is not a valid value. This indicates the balancing configuration is keeping the balancing in a stop state, such as *[BAL_GO]* = 1 with all balancing timer set to 0, or MCU never issue *[BAL_GO]* = 1.

表 8-6. BAL_TIME Register Status

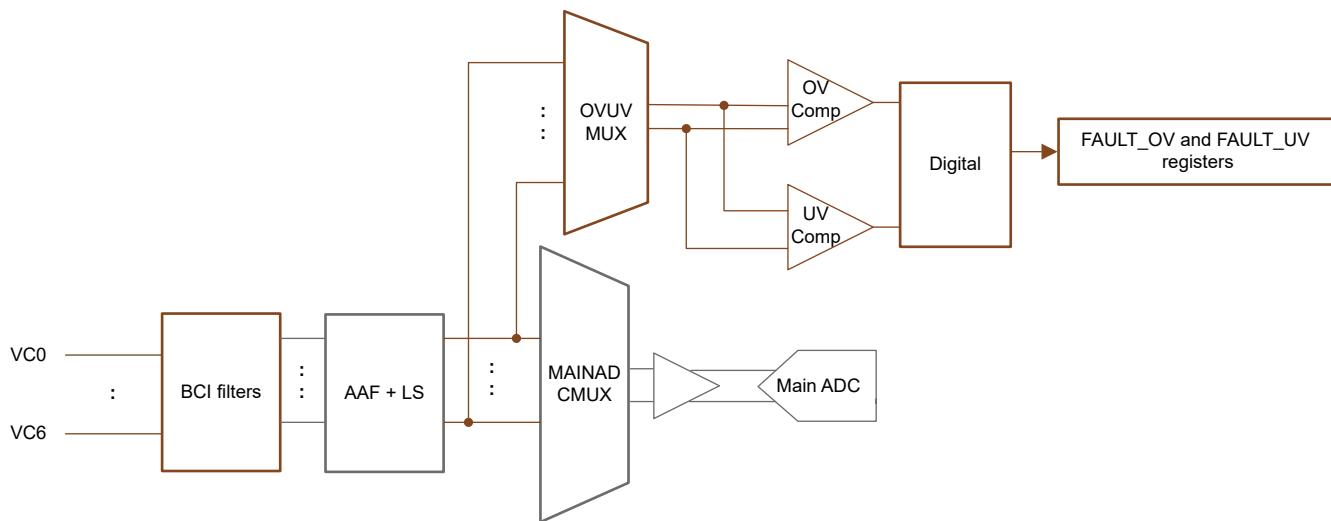
| CB Stop Condition | BAL_TIME Register |
|---|---|
| Cell balancing timer expires | The selected CB channel reports 0-s |
| CB channel voltage < VCB_DONE_THRESH register value | The selected CB channel reports the remaining CB time |
| $[FLTSTOP_EN] = 1$ and unmasked fault is detected | |

8.3.4 Integrated Hardware Protectors

The device integrates cell OV and UV protectors and thermistor OT and UT protectors with programmable thresholds independent of the ADC functionality or the ADC measurements path. The OVUV and OTUT protectors can operate in ACTIVE or SLEEP mode. The subsections below provide an overview of the protectors. See [节 8.3.6.4](#) for diagnostic control function and status of this block.

8.3.4.1 OVUV Protectors

A set window comparator provides cell voltage monitoring for all VC channels. This comparator function is entirely separate from the ADC function and as such, even if the ADC function fails, the analog comparators still flag the crossing of the overvoltage (OV) and undervoltage (UV) comparator thresholds. The programmed thresholds are translated through DACs to the comparators.


图 8-19. OV and UV Protectors

The OV and UV thresholds set by OV_THRESH and UV_THRESH registers are the same for all VC channels. The active channels are defined by the $ACTIVE_CELL[NUM_CELL3:0]$ bits. These bits set the highest active channel number and the device assumes any lower channels are also active.

The $UV_DISABLE1$ and $UV_DISABLE2$ registers setting disable any individual channel for UV detection, such as channel is connected to bus bar.

Otherwise, the OV protector detects an OV fault on a particular channel if the VC channel voltage is greater than the OV_THRESH setting. The UV protector detects a UV fault on a particular channel if the VC channel voltage is less than the UV_THRESH setting.

8.3.4.1.1 OVUV Operation Modes

The OV and UV protectors have several operation modes controlled by $OVUV_CTRL[OVUV_MODE1:0]$ and is summarized in [表 8-7](#). To start the OVUV protectors, MCU sets $OVUV_CTRL[OVUV_GO] = 1$.

表 8-7. OVUV Protector Operation Modes

| [OVUV_MODE1:0] | Operation Mode | Description |
|----------------|---|---|
| 0b00 | Stop OV and UV protectors | Stop OV and UV protectors |
| 0b01 | Round robin run | The OV and UV protectors are looping through all VC inputs. The active channels are checked against the OV and UV thresholds (图 8-19). The round robin cycle timing is always the same regardless of the number of the active channels. For the inactive VC channels, the digital logic simply ignores the detection outcome. The UV protector detects both <i>UV_THRESH</i> and <i>VCB_DONE_THRESH</i> . |
| 0b10 | OV and UV BIST run (diagnostic use, see 节 8.3.6.4 for details) | A BIST (built-in self-test) cycle on the OV and UV comparators and the detection paths. VCELL (VC channels) ADC measurement from the Main ADC and the OV and UV detections through the OVUV protectors are not available during this run. MCU shall stop ADC measurement when performing OVUV BIST. |
| 0b11 | Single channel run (diagnostic use, see 节 8.3.6.4 for details) | Use for checking the OV and UV DACs. The OV and UV comparator is locked to a single VC input channel in this mode. Channel is locked by <i>OVUV_CTRL[OVUV_LOCK3:0]</i> . |

If OVUV BIST run is in progress, but MCU start ADC, the ADC result registers will be held at 0x8000. ADC measurements will resume once OVUV BIST is completed and after t_{AFE_SETTLE} time pass.

If ADC is running, but MCU start OVUV BIST, the ADC result registers will be held at its last measurement. ADC measurement update resumes once OVUV BIST is completed and after t_{AFE_SETTLE} time pass

Note: The round robin cycle time is always the same regardless the number of active channel

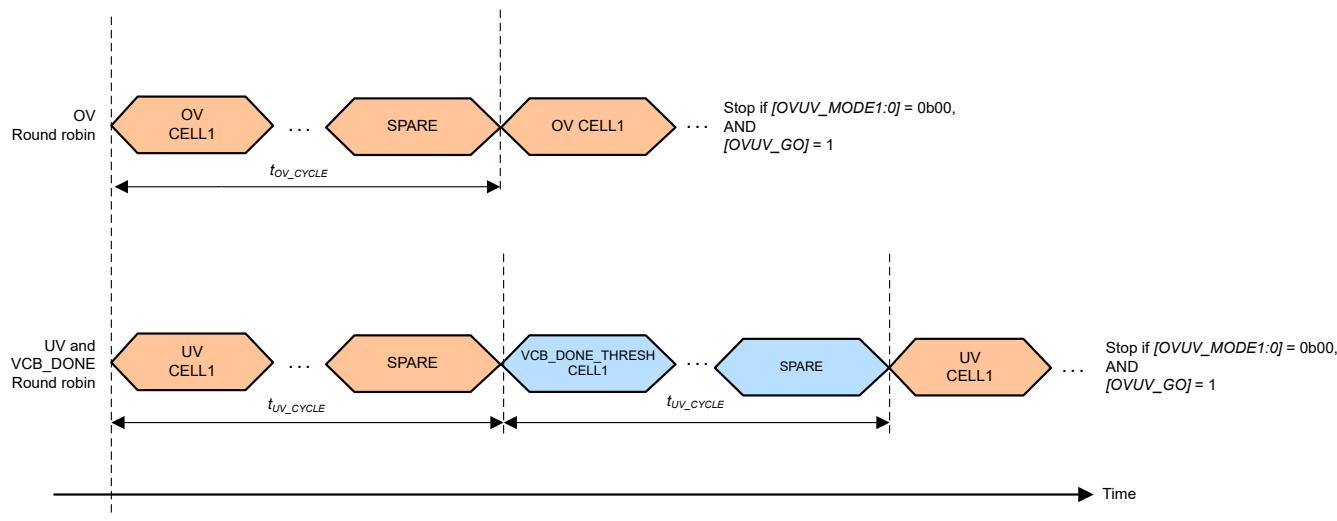


图 8-20. OV and UV Round Robin Mode

8.3.4.1.2 OVUV Control and Status

8.3.4.1.2.1 OVUV Control

To start the OV and UV protectors, MCU sets *OVUV_CTRL[OVUV_GO]* = 1. When the device receives the GO command, it samples the following register settings and then starts the OVUV protectors accordingly. Any change of the settings below requires the MCU to resend another GO command to implement the new settings.

- *OV_THRESH* register: Sets the OV threshold for all VC channels
- *UV_THRESH* register: Sets the UV threshold for all VC channels
- *VCB_DONE_THRESH* register: Sets the VCB_DONE threshold for cell balancing stop condition (if enabled)
- *OVUV_CTRL[OVUV_MODE1:0]*: OVUV operation mode selection

- *ACTIVE_CELL* register: Determines the inactive VC channel(s) and ignores the detection result accordingly
- *UV_DISABLE1* and *UV_DISABLE2* registers: Determines the inactive VC channel(s) and ignores the detection result accordingly.

The OVUV protectors can also operate in SLEEP mode. MCU first starts the protector in ACTIVE mode, then puts the device in SLEEP mode. The OVUV protectors will continue the operation until the MCU commands to stop or if the device shuts down.

8.3.4.1.2.2 OVUV Status

The *DEV_STAT[OVUV_RUN]* = 1 indicates the OVUV protectors are running. The OV detection result is reflected in the *FAULT_OV1* and *FAULT_OV2* registers; the UV detection result is reflected in the *FAULT_UV1* and *FAULT_UV2* registers.

The *VCB_DONE* detection is not a fault but a cell balancing stop condition. The result is reflected in a particular channel stopping cell balancing. See [节 8.3.3](#) for details.

8.3.4.2 OTUT Protector

A set window comparator provides temperature monitoring for all GPIO inputs with the external thermistor network pulled up to TSREF. This comparator function is entirely separate from the ADC function and, as such, even if the ADC function fails, the analog comparators still flag the crossing of the overtemperature (OT) and undertemperature (UT) comparator thresholds. The programmed thresholds are translated through DACs to the comparators.

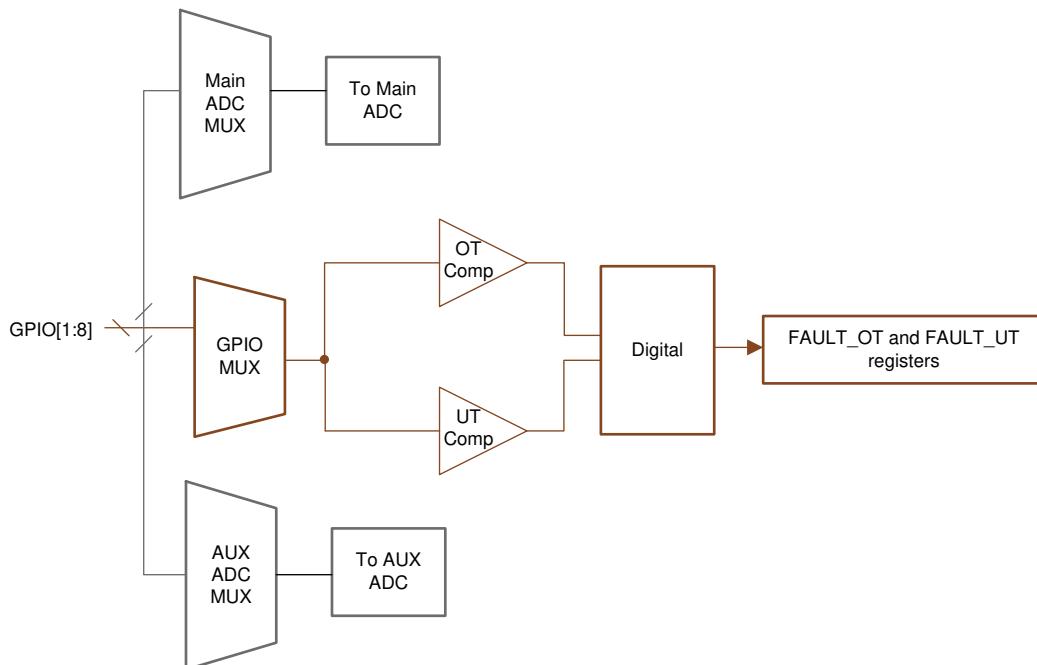


图 8-21. OT and UT Protectors

The OT and UT thresholds set by *OTUT_THRESH[OT_THR4:0]* and *OTUT_THRESH[UT_THR2:0]* bits are the same for all active GPIO inputs. The active GPIO inputs are defined by the *GPIO_CONFn[GPIO*2:0]* (where n = 1 to 4, * = 1 to 8 for the corresponding GPIO input). The GPIO has to be configured as ADC and OTUT inputs to be considered as active GPIO inputs for the OTUT protectors.

The OTUT comparators use TSREF as reference, and so the detection is in ratiometric form. The OT protector detects an OT fault on a particular GPIO if the (GPIO voltage/TSREF) is less than the *OTUT_THRESH[OT_THR4:0]* setting. The UT protector detects a UT fault on a particular GPIO if the (GPIO

voltage/TSREF) is more than the $OTUT_THRESH[UT_THR2:0]$ setting. The OTUT protectors assume the NTC thermistor is used for temperature monitoring.

MCU ensures TSREF is enabled before starting the OTUT protectors. Failing to do so, the OTUT protectors will flag all OT and UT faults on all GPIO inputs as an indication of abnormal detection.

8.3.4.2.1 OTUT Operation Modes

The OT and UT protectors have several operation modes controlled by $OTUT_CTRL[OTUT_MODE1:0]$ and are summarized in [表 8-8](#). To start the OTUT protectors, the MCU sets $OTUT_CTRL[OTUT_GO]=1$.

表 8-8. OTUT Protector Operation Modes

| $[OTUT_MOD1:0]$ | Operation Mode | Description |
|------------------|---|--|
| 0b00 | Stop OT and UT protectors | Stop OT and UT protectors |
| 0b01 | Round robin run | The OT and UT protectors are looping through all GPIO inputs. The active GPIO inputs are checked against the OT and UT thresholds (图 8-22). The round robin cycle timing is always the same regardless of the number of the active GPIOs. For the inactive GPIO inputs, the digital logic simply ignores the detection outcome. The OT protector detects both OT threshold and OTCB threshold. |
| 0b10 | OT and UT BIST run (diagnostic use, see 节 8.3.6.4 for details) | A BIST (built-in self-test) cycle on the OT and UT comparators and the detection paths. Temperature (GPIO channels) ADC measurement from the main or AUX ADC and the OT and UT detections through the OTUT protectors are not available during this run. |
| 0b11 | Single channel run (diagnostic use, see 节 8.3.6.4 for details) | Used for checking the OT and UT DACs. The OT and UT comparator is locked to a single GPIO input channel in this mode. Channel is locked by $OTUT_CTRL[OTUT_LOCK2:0]$. |

Note: The round robin cycle time is always the same regardless of the number of active GPIO inputs

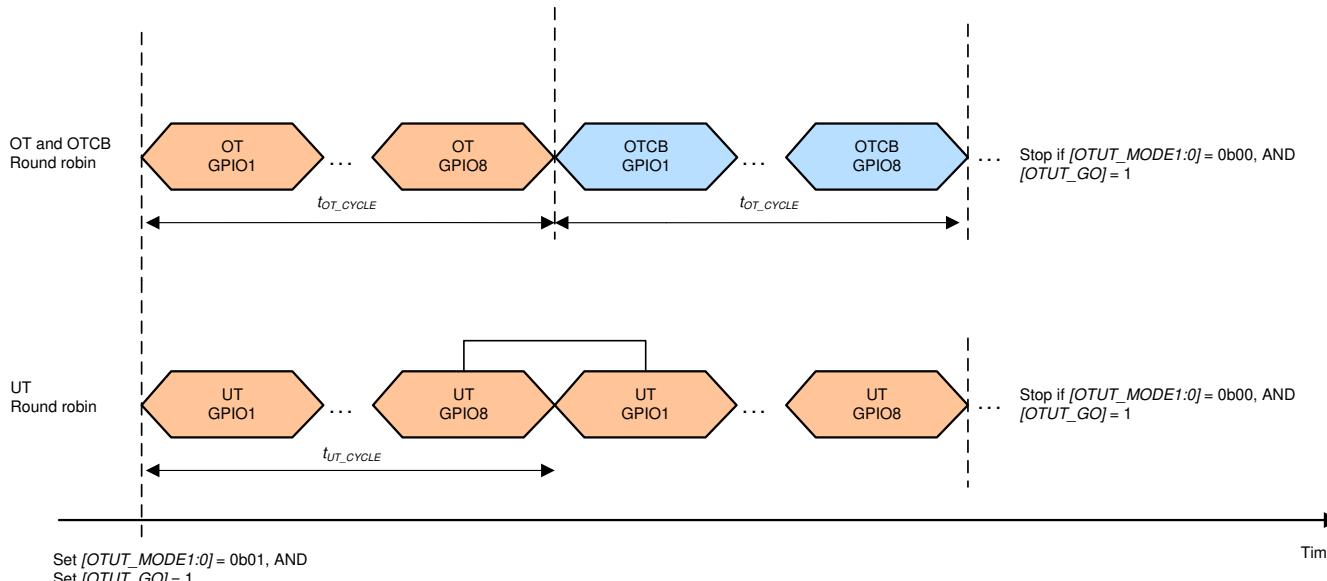


图 8-22. OT and UT Round Robin Modes

8.3.4.2.2 OTUT Control and Status

8.3.4.2.2.1 OTUT Control

Ensure TSREF is enabled. To start the OT and UT protectors, host MCU sets $OTUT_CTRL[OTUT_GO]=1$. When the device receives the GO command, it samples the following register settings and then starts the OTUT protectors accordingly. Any change of the settings below requires the MCU to send another GO command to implement the new settings.

- **OTUT_THRESH[OT_THR4:0]**: Sets the OT threshold for all active GPIO inputs
- **OTUT_THRESH[UT_THR2:0]**: Sets the UT threshold for all active GPIO inputs
- **OTCB_THRESH** register: Sets the OTCB threshold and COOLOFF hysteresis (if enabled)
- **OTUT_CTRL[OTUT_MODE1:0]**: OTUT operation mode selection
- **GPIO_CONF1** to **GPIO_CONF4**: Determines the inactive GPIO channel(s) and ignores the detection result.

The OTUT protectors can also operate in SLEEP mode. MCU first starts the protector in ACTIVE mode, then puts the device in SLEEP mode. The OTUT protectors will continue the operation until the MCU commands them to stop or if device shuts down.

8.3.4.2.2 OTUT Status

The **DEV_STAT[OTUT_RUN]** = 1 indicates the OTUT protectors are running. The OT detection result is reflected in the **FAULT_OT** register; the UT detection result is reflected in the **FAULT_UT** register.

The OTCB detection is not a fault but a cell balancing pause condition. The result is reflected in a particular channel pausing cell balancing. See [节 8.3.3](#) for details.

8.3.5 GPIO Configuration

The device has eight GPIOs. Each GPIO can be programmed to be one of the configurations below through the **GPIO_CONF1** to **GPIO_CONF4** registers.

| GPIO | DISA BLE | | INPUT | | OUTPUT | | WEAK PULL-UP/ DOWN | | Module Balancing <i>MB_TIMER_CTR</i> L is not 0x00 | SPI Controller <i>[SPI_EN]</i> = 1 | Fault Input <i>[FAULT_IN_</i> <i>EN]</i> = 1 | Current Sense Toggle <i>[CD_RDY_</i> <i>EN]</i> = 1 |
|-------|-------------|---------|---------------|-------------|--------|-----|--------------------------|--------------------------------|---|--|--|--|
| | High- Z | Digital | ADC & OTUT | ADC Only | High | Low | ADC & weak pull-up | ADC & weak pull- down | | | | |
| GPIO1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | ✓ (output, Low when conversion is ready) |
| GPIO2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| GPIO3 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ (output, HIGH) | | | |
| GPIO4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ (SS) | | |
| GPIO5 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ (MISO) | | |
| GPIO6 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ (MOSI) | | |
| GPIO7 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ (SCLK) | | |
| GPIO8 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | ✓ (Input, Active Low) | |

| GPIO Configuration | | Description | |
|--------------------|--------------|--|--|
| DISABLE | High-Z | This is the default GPIO configuration at reset if OTP is not programmed | |
| INPUT | Digital | When GPIO is configured as Digital Input, the device detects the input voltage level to determine a 1 or 0 with respect to its V_{IL} and V_{IH} levels. The result is shown in the GPIO_STAT register. | |
| | ADC and OTUT | The GPIO is configured to be measurable by the ADC (both main and AUX ADCs) and also as the input to the OTUT protectors. Example: use this selection for GPIO used for thermistor connection. | |
| | ADC only | The GPIO is configured to be measurable by the ADC (both main and AUX ADCs) only. Example: use this selection to measurement voltage on GPIO. | |
| OUTPUT | High | The GPIO is configured as digital output high (internally pull up to CVDD). The logic state is also shown in the GPIO_STAT register. | |
| | Low | The GPIO is configured as digital output low. The logic state is also shown in the GPIO_STAT register. | |

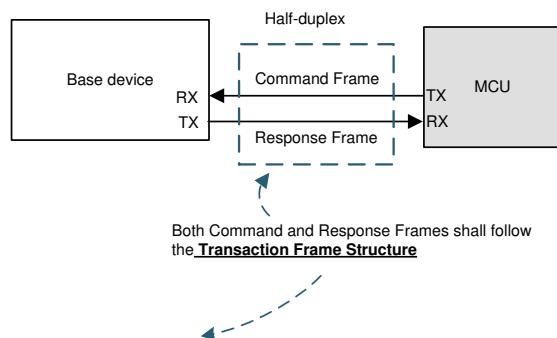
| GPIO Configuration | | Description |
|--------------------|------------------------|---|
| WEAK PULL-UP/DOWN | ADC and Weak Pull-up | The GPIO is pull up internally and is configured to measured by the ADC (both main and AUX ADCs) |
| | ADC and Weak Pull-down | The GPIO is pull down internally and is configured to measured by the ADC (both main and AUX ADCs) |
| SPECIAL | SPI Controller | When $GPIO_CONF1[SPI_EN]$ = 1, GPIO4 to GPIO7 are taken over as the SPI controller communication lines. This configuration has higher priority over any of the INPUT/OUTPUT configurations on GPIO4 to GPIO7. |
| | Fault Input | When $GPIO_CONF1[FAULT_IN_EN]$ = 1, GPIO8 is taken over as an input that if the GPIO was asserted (active low), will set $FAULT_SYS[GPIO]$ = 1 and assert NFAULT (if enabled). |
| | Current Sense Toggle | When $GPIO_CONF2[CS_RDY_EN]$ = 1, GPIO1 is taken over as output. When a conversion is ready from CS ADC, GPIO1 will be LOW. Once CURRENT_HI register is read by host, GPIO1 will return to HIGH. |

8.3.6 Communication, OTP, Diagnostic Control

8.3.6.1 Communication

8.3.6.1.1 Serial Interface

The device has a serial interface which uses UART protocol as the physical layer to communicate between device and host. The communication is specified in a proprietary frame structure.



Transaction Frame Structure (to/from system MCU to the base device):
 A transaction frame consists of 5 types of information as shown above.
 Data are all sent in byte, and each byte is sent through UART protocol.

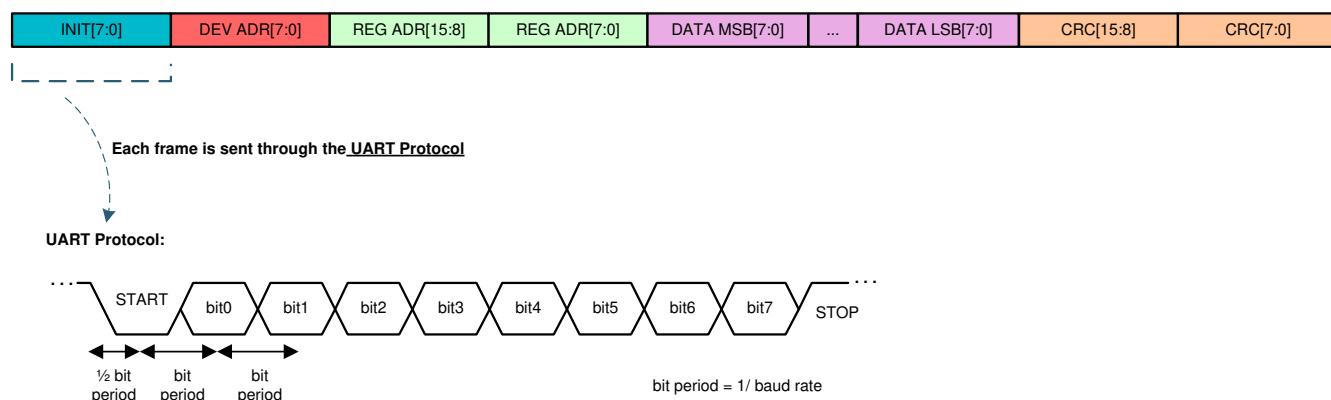


图 8-23. UART Communication to Host

8.3.6.1.1.1 UART Physical Layer

The UART interface follows the standard serial protocol of 8-N-1, where it sends information as a START bit, followed by eight data bits, and then one STOP bit. The STOP bit indicates the end of the byte. If a byte is

received that does not have the STOP bit set, the *FAULT_COMM1[STOP_DET]* bit is set, indicating there may be a baud rate issue between the host and the device. The device supports 1-Mbps baud rate.

The UART sends data on the TX pin and receives data on the RX pin. When idle, the TX and RX pins are high. The UART interface requires that RX is pulled up to CVDD through a resistor on the device. The RX is pulled up on the device side. Do not leave RX unconnected.

The TX pin must be pulled high through a resistor on the host side of device to prevent triggering an invalid communications frame when the communication cable is not attached, or during power-off or SHUTDOWN state when TX is high impedance. TX is always pulled to CVDD internally while in ACTIVE or SLEEP mode.

The UART interface is strictly a half-duplex interface. While transmitting, any attempted communication on RX is ignored. The only exception is COMM CLEAR signal on RX pin, which immediately terminates the communication. See [节 8.3.6.1.1.1.3](#) for details.

Using two STOP bits in UART:

The device can be set up with two stop bits (*DEV_CONF[TWO_STOP_EN]* = 1), the UART response frame transmits from device to host will always return with two STOP bits as shown below. Host is not required to send the command frame to the device with two STOP bits. The device is able to receive one or more stop bits with or without this function enabled.

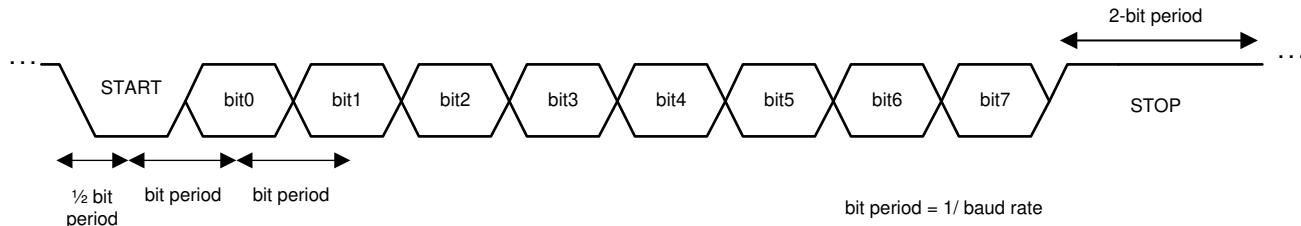


图 8-24. UART Response Frame with Two STOP Bits

Potential use of the two stop bits may be to:

- The host to gain extra time to process the data before receiving next data frame.
- The clock tolerance between device and host might cause the data detection out of sync. Having two STOP bits allows re-synchronization of the communication; hence, improving communication robustness.

8.3.6.1.1.1.1 UART Transmitter

The transmitter is configured to wait a specified number of bit periods after the last bit reception before starting transmissions using the *TX_HOLD_OFF* register. This provides time for the host to switch the bus direction at the end of its transmission.

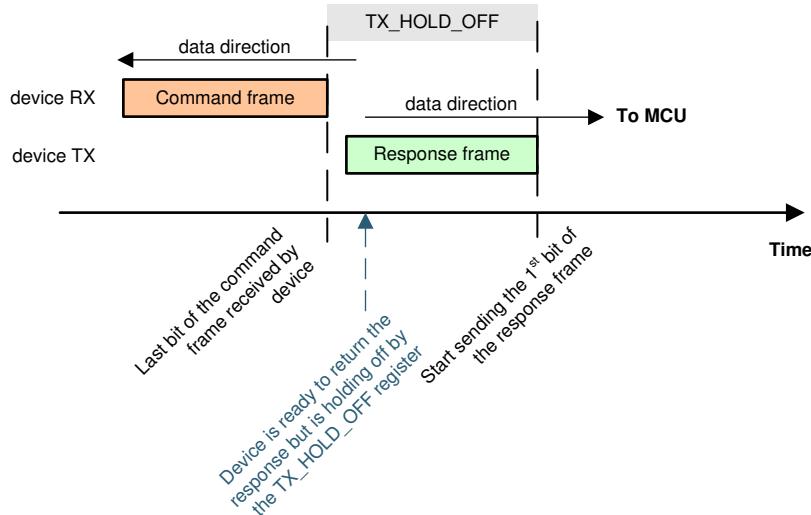


图 8-25. UART TX_HOLD_OFF

8.3.6.1.1.2 UART Receiver

While the device is transmitting data on TX, RX is ignored except when receiving a COMM CLEAR. If the host starts a transmitting without waiting to receive the preceding transaction's response, the communication is not considered reliable and the host must send a COMM CLEAR to restore normal communications to the device.

8.3.6.1.1.3 COMM CLEAR

A COMM CLEAR is sent on the RX pin of the device. RX cannot be disabled and a COMM CLEAR can be sent at any time regardless of the TX status. Ensure that the COMM CLEAR does not exceed the maximum value of $t_{UART(CLR)}$ bit periods, as this may result in recognition of other communication pings.

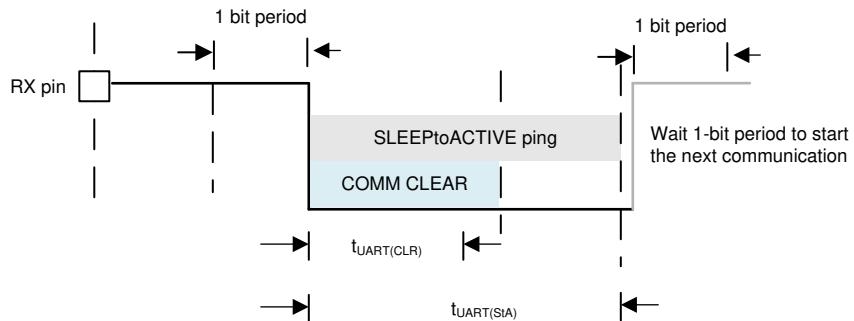


图 8-26. UART COMM CLEAR

Use the COMM CLEAR command to clear the receiver and instruct the UART engine to look for a new start of frame. The next byte following the COMM CLEAR is always considered a start-of-frame byte. When detected, a COMM CLEAR sets the *FAULT_COMM1/COMMCLR_DET* flag. The host must wait at least $t_{UART(RXMIN)}$ after the COMM CLEAR to start sending a new frame. It should be noted that in addition to the *[COMMCLR_DET]* flag, the *FAULT_COMM1/STOP_DET* flag is also set because the COMM CLEAR timing violates the typical byte timing and the STOP bit is seen as 0.

A SLEEPtoACTIVE ping also clears the UART receiver. This ping sets the *[COMMCLR_DET]* flag when transitioning from SLEEP to ACTIVE mode. If this ping is sent during ACTIVE mode, the *[COMMCLR_DET]* and *[STOP_DET]* flags are set.

8.3.6.1.1.2 Command and Response Protocol

The host initiates every transaction between the host and device. The device never transmits data without first receiving a command frame from the host. A command frame is a communication frame sent from host to the device; a response frame is a response (to a read command) from device to host. After a command frame is transmitted, the host must wait for all expected responses to be returned (or a timeout in case of error) before initiating a new command frame. The commands supported by the device are listed in [表 8-9](#):

表 8-9. Commands

| Command | Description |
|---------------------|--|
| Single Device Read | To read a register(s) from a single device |
| Single Device Write | To write a register(s) to a single device |

8.3.6.1.1.2.1 Transaction Frame Structure

The protocol layer is made up of transaction frames. There are two basic types of transaction frames: command frames (transactions from host) and response frames (transactions from device). The transaction frames are made up of the following five field types:

- Frame initialization (INIT, 1-byte)
- Device address (DEV ADR, 1-byte)
- Register address (REG ADR, 2-byte)
- Data (DATA, various byte length)
- Cyclic redundancy check (CRC, 2-byte)

8.3.6.1.1.2.1.1 Frame Initialization Byte

The frame initialization byte is used in both command and response frames. It is always the first byte of the frame. The frame initialization byte performs two functions. First, it defines the frame as either a command frame (host) or a response frame (device). Second, it defines the length of the frame that follows after the frame initialization byte. This provides the receiver an exact number of bytes to expect for a complete command or response.

表 8-10. Command Frame Initialization Byte Definition

| | Bit | Command Frame | | Response Frame | |
|------|-----|---------------|--|----------------|----------------------------|
| | | Bit Name | Description | Bit Name | Description |
| INIT | 7 | FRAME_TYPE | 1 = Define Command Frame | FRAME_TYPE | 0 = Defines Response Frame |
| | 6 | REQ_TYPE | 000 = Single Device Read | RESPONSE_BYTE | Number of the data bytes |
| | 5 | | 001 = Single Device Write | | 0x00 = 1 byte |
| | 4 | | 010 = RSVD | | 0x01 = 2 bytes |
| | | | 011 = RSVD | | : |
| | | | 100 = RSVD | | 0x7F = 128 bytes |
| | | | 101 = RSVD | | |
| | | | 110 = RSVD | | |
| | | | 111 = RSVD | | |
| | 3 | RSVD | Reserved. This bit is ignored | | |
| | 2 | DATA_SIZE | Number of data bytes of the command frame, excluding device address, register address or CRC | | |
| | 1 | | 000 = 1 byte | | |
| | 0 | | 001 = 2 bytes | | |
| | | | : | | |
| | | | 111 = 8 bytes | | |

8.3.6.1.1.2.1.2 Device Address Byte

The device address byte identifies the device targeted by the single device read/write command. All response frames contain the device address byte. In single device read/write commands, the device that contains a

matching value in the *DIR0_ADDR* (used for communication direction with *CONTROL1[DIR_SEL] = 0*) or in *DIR1_ADDR* (used for communication direction with *CONTROL1[DIR_SEL] = 1*) responds to the command.

表 8-11. Device Address Byte Definition

| | | Command Frame | | Response Frame | |
|---------|--------|----------------|----------|--|----------------|
| | | Bit | Bit Name | Description | Bit Name |
| DEV ADR | 7 | RSVD | | Should always write 0 | RSVD |
| | 6 | RSVD | | Should always write 0 | RSVD |
| | 5 to 0 | Device Address | | Set the device address range from 0x00 to 0x3F | Device Address |

8.3.6.1.2.1.3 Register Address Bytes

Register addresses are two bytes in length. Any write command to an invalid register address is ignored. Any read from an invalid register returns a 0x00 response. This is true for command frames sent to an individual register with invalid address, or as part of command sent to multiple registers with invalid addresses. When read/write addresses a block of registers with only some invalid addresses, the valid addresses respond as normal, while the invalid addresses respond as previously described.

表 8-12. Register Address Byte Definition

| | | Command Frame | | Response Frame | |
|---------|--------|------------------------|----------|---|------------------------|
| | | Bit | Bit Name | Description | Bit Name |
| REG_ADR | 7 to 0 | Register Address (MSB) | | Target or beginning of the register address | Register Address (MSB) |
| | 7 to 0 | Register Address (LSB) | | Target or beginning of the register address | Register Address (LSB) |

8.3.6.1.2.1.4 Data Bytes

The number of data bytes and the relevant information they convey is determined by the type of command frame sent and the target register specified in that command frame. When part of a command frame, the data bytes contain the values to be written to the registers. When part of a response frame, the data bytes contain the values returned from the registers.

表 8-13. Data Bytes Definition

| | Command Frame | | | | Response Frame | | | | |
|------|---------------|---------------|---|--|----------------|--|--|--|--|
| | Bit | Bit Name | Description | | Bit Name | Description | | | |
| DATA | 7 | Data Byte[0] | For Write command: Data value to be written to the register(s) is specified in the REG_ADR frame | | Data Byte[0] | Data value return from the register(s) is specified in the REG_ADR frame | | | |
| | 6 | | For Read command: Specify the number of bytes need to be returned by the read command. | | | | | | |
| | 5 | | 0x00 = 1 byte | | | | | | |
| | 4 | | 0x01 = 2 bytes | | | | | | |
| | 3 | | : | | | | | | |
| | 2 | | 0x7F = 128 bytes | | | | | | |
| | 1 | | | | | | | | |
| | 0 | | | | | | | | |
| | ... | | | | | | | | |
| | 7 | Data Byte [n] | For Write command: Data value to be written to the register(s) is specified in the REG_ADR frame | | Data Byte [n] | Data value return from the register(s) is specified in the REG_ADR frame | | | |

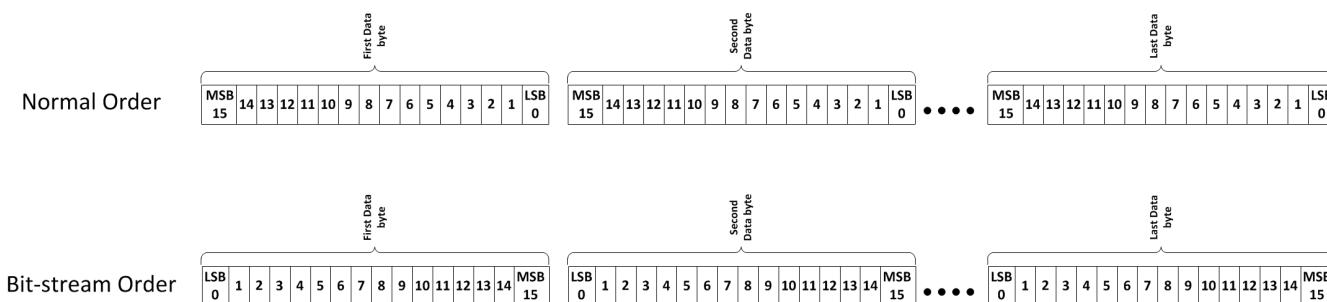
8.3.6.1.1.2.1.5 CRC Bytes

The device uses a CRC (cyclic redundancy check) to protect data integrity during transmission. The CRC represents the remainder of a process analogous to polynomial long division, where the frame being checked is divided by the generator. The CRC appended to the frame is the remainder. Because of this process, when the device receives a frame, the CRC calculated by the receiver across the entire frame including the transmitted CRC will be zero, indicating a correct transmission and reception. A non-zero result indicates a communication error. Specifically, the device uses the CRC-16-IBM polynomial ($x^{16} + x^{15} + x^2 + 1$) with 0xFFFF initialization.

The CRC value is checked as the first step after receiving the communication frame. If the CRC is incorrect, the entire frame is discarded and not processed. Any additional frame errors are not checked and any errors are not indicated other than CRC error.

8.3.6.1.1.2.1.6 Calculating Frame CRC Value

The CRC calculation by the transmitter is in bit-stream order across the entire transmission frame (except for the CRC). When determining bit-stream order for implementing the CRC algorithm, it is important to note that protocol bytes transmit serially, least-significant bit first. [图 8-27](#) illustrates the bit-stream order concept.


图 8-27. Bit-Stream Order Explanation

The CRC (0x0000) is appended to the end of the bit-stream. This bit-stream is then initialized by XOR'ing with 0xFFFF to catch any leading 0 errors. This new bit-stream is then divided by the polynomial (0xC002) until only the 2-byte CRC remains. During this process, the most significant 17 bits of the bit stream are XOR' d with the polynomial. The leading zeroes of the result are removed and that result is XOR' d with the polynomial once again. The process is repeated until only the 2-byte CRC remains. For example:

Example 1: CRC Calculation Using Polynomial Division

```

Command Frame = 0x80 00 02 0F 0B (0b1000 0000 0000 0000 0010 0000 1111 0000 1011)
Command Frame in bit stream order = 0x01 00 40 F0 D0 (0b0000 0001 0000 0000 0100 0000 1111 0000
1101 0000)
After Initialization (XOR with 0xFFFF) = 0b1111 1110 1111 1111 0100 0000 1111 0000 1101 0000
1111 1110 1111 0100 0000 1111 0000 1101 0000 0000 0000 #append 0x0000 for CRC
1100 0000 0000 0010 1 #XOR with polynomial
0011 1110 1111 1101 1100 0000 1111 0000 1101 0000 0000 0000
11 1110 1111 1101 1100 0000 1111 0000 1101 0000 0000 0000 #delete leading zeros from
previous result
11 0000 0000 0000 101 #XOR with polynomial
00 1110 1111 1101 0110 0000 1111 0000 1101 0000
.....
.....
1100 0110 0000 0001 0000 0000
1100 0000 0000 0010 1 #XOR with polynomial
0000 0110 0000 0011 1000 0000
110 0000 0011 1000 0000
110 0000 0000 0001 01 #XOR with polynomial
000 0000 0011 1001 0100
0000 0011 1001 0100 #CRC result in bit stream order
1100 0000 0010 1001 #final CRC result in normal order
CRC final 0xC029

```

8.3.6.1.1.2.1.7 Verifying Frame CRC

There are several methods for checking the CRC of a frame. One method is to simply calculate the CRC for the transmitted command except the last two bytes (CRC bytes) using the method described in the previous section, and then compare that result with the transmitted CRC bytes. A more simple option is to run the entire transmission through the CRC algorithm. If the CRC is correct, the result is 0000. In this case, the initial zero padding of the bit-stream with 16 zeroes is not necessary. Using the previous result and running through the algorithm produces the following results:

Example 1: CRC Verification Using Polynomial Division:

```

Command Frame = 0x80 00 02 0F 0B (0b1000 0000 0000 0000 0010 0000 1111 0000 1011)
CRC to Check = 0xC029
Command Frame w/ CRC in bit stream order = 0x80 00 02 0F 0B C0 29 (0b1000 0000 0000 0000 0000 0010
0000 1111 0000 1011 0000 0011 1001 0100)
After Initialization (XOR with 0xFFFF) = 0b0 1111 1110 1111 1111 0100 0000 1111 0000 1101 0000 0000
0011 1001 0100
1111 1110 1111 1111 0100 0000 1111 0000 1101 0000 0000 0011 1001 010
#delete leading zeros from
previous result
1100 0000 0000 0010 1 #XOR with polynomial
0011 1110 1111 1101 1100 0000 1111 0000 1101 0000 0000 0011 1001 0100
11 1110 1111 1101 1100 0000 1111 0000 1101 0000 0000 0011 1001 0100 #delete leading zeros from
previous result
11 0000 0000 0000 101 #XOR with polynomial
00 1110 1111 1101 0110 0000 1111 0000 1101 0000 0000 0011 1001 0100
.....
.....
1100 0110 0000 0010 1001 0100
1100 0000 0000 0010 1 #XOR with polynomial
0000 0110 0000 0000 0001 0100
1 1000 0000 0000 0101 00
1 1000 0000 0000 0101 #XOR with polynomial
0 0000 0000 0000 00
0x0000 #verfiy that CRC checks out valid

```

备注

The result of ‘0b0000 0000 0000 0000’ for the CRC indicates a successful check.

8.3.6.1.1.2.2 Transaction Frame Examples

Transaction frames are created using the frame structure discussed in the previous sections. The CRC values in the examples are correct and can be used to verify the customer CRC algorithm. The CRC is verified by the device with every received command frame and the command is not executed unless the CRC is valid.

8.3.6.1.1.2.2.1 Single Device Read/Write

Single Device Read:

Device address must be set up before using this command. A single device read generates a response frame whose length depends on the requested number of register bytes read. The command frame send by host must contain the register address to start at (address field) and the number of bytes to return (number of registers to read). The DATA_SIZE field in the initialization byte for the single device read command is always 0b000.

Single Device Write:

Device address must be set up before using this command. A write command for a single device enables the customer to update up to eight consecutive registers with one command. The single device write command frame must contain the register address to start at (address field) and the data bytes to write to the registers. The DATA_SIZE field in the initialization byte for the single device write command is the number of registers to update.

表 8-14. Single Device Read/Write

| Single Read Command Sent by Host | | | Single Write Command Sent by Host | |
|----------------------------------|------------------------------|---|--|---|
| Example | Read 6 Cell Voltages from B0 | | Write OTP Unlock Code to OTP_PROG_UNLOCK1A to 1D Registers | |
| Frame Field | Data | Comments | Data | Comments |
| Initialization Byte | 0x80 | Always 0x80 FRAME_TYPE = 1 REQ_TYPE = 0b000 = Single Read DATA_SIZE = 0b000 | 0x93 | 0x90 for 1 byte data write, 0x91 for 2 bytes data write, 0x92 for 3 bytes data write and so on. For this example: FRAME_TYPE = 1 REQ_TYPE = 0b001 = Single Write DATA_SIZE = 0b11 = 4 bytes |
| Device Address | 0x00 | Device address 0x00 (B0) in this example | 0x00 | Device address 0x00 (B0) in this example |
| Register Address | 0x057C | Start address of the register block to read (address of VCELL6_HI in this example) | 0x0300 | Start address of the register block to write (address of OTP_PROG_UNLOCK1A in this example) |
| Data | 0x0B | Instruct the target device to return 12 bytes of data (that is, from address 0x057C to 0x0587), assuming each VCELLn_HI = 0x80, VCELLn_LO = 0x00, where n = 1 to 6. | 0x02B7 78BC | The unlock value to OTP_PROG_UNLOCK1A to OTP_PROG_UNLOCK1D |
| CRC | 0x54D8 | | 0x9B6E | |

8.3.6.1.2 Communication Timeout

There are two programmable communication timeout thresholds, CTS timer and CTL timer, that monitor the absence of a valid frame. A valid frame is defined as any frame (response or command) that does NOT contain any errors that prevent the frame from being processed. The communication timeouts are only actively counting while in ACTIVE mode. The counters are disabled and reset during SHUTDOWN mode. In SLEEP mode, the last counter values are held frozen.

8.3.6.1.2.1 Short Communication Timeout

The short communication timeout acts like an alert to the host when triggered. The timeout period is programmable through the *COMM_TIMEOUT_CONF[CTS_TIME2:0]* bits. If enabled, the timer is reset every time a valid response or command frame is received. If the timer expires, the *FAULT_SYS[CTS]* bit is set.

8.3.6.1.2.2 Long Communication Timeout

The long communication timeout allows the host to put the device in SLEEP or SHUTDOWN mode for power saving. The timeout period is programmable through *COMM_TIMEOUT_CONF[CTL_TIME2:0]* bits. If enabled, the timer is reset every time a valid response or command frame is received. If the timer expires, host can choose one of the following actions through *COMM_TIMEOUT_CONF[CTL_ACT]* bit.

- Set *FAULT_SYS[CTL]* = 1 and enter SLEEP mode.
- Enter SHUTDOWN mode.

8.3.6.1.3 SPI Controller

The GPIO4 thru GPIO7 are configurable as a SPI controller interface when *GPIO_CONF1[SPI_EN]* = 1. The SPI controller includes four I/Os:

- SCLK: SPI clock, generated by the device and is used for synchronization
- MOSI: Controller data output, driven by the device to output data to peripheral
- MISO: Controller data input, detecting data from peripheral
- SS: Peripheral select, driven by the device during SPI communication.

The *SPI_CONF[CPOL]* (clock polarity) and *[CPHA]* (clock phase) define the SPI clock format. The *[CPOL]* is defined if the SPI clock is inverted or non-inverted. The *[CPHA]* is defined if the MISO and MOSI are sampled on the leading (first) clock edge or on the trailing (second) clock edge, regardless of whether that clock edge is rising or falling. The *SPI_CONF[NUMBIT4:0]* defines how many bits the transaction is (1-bit to 24-bit transaction).

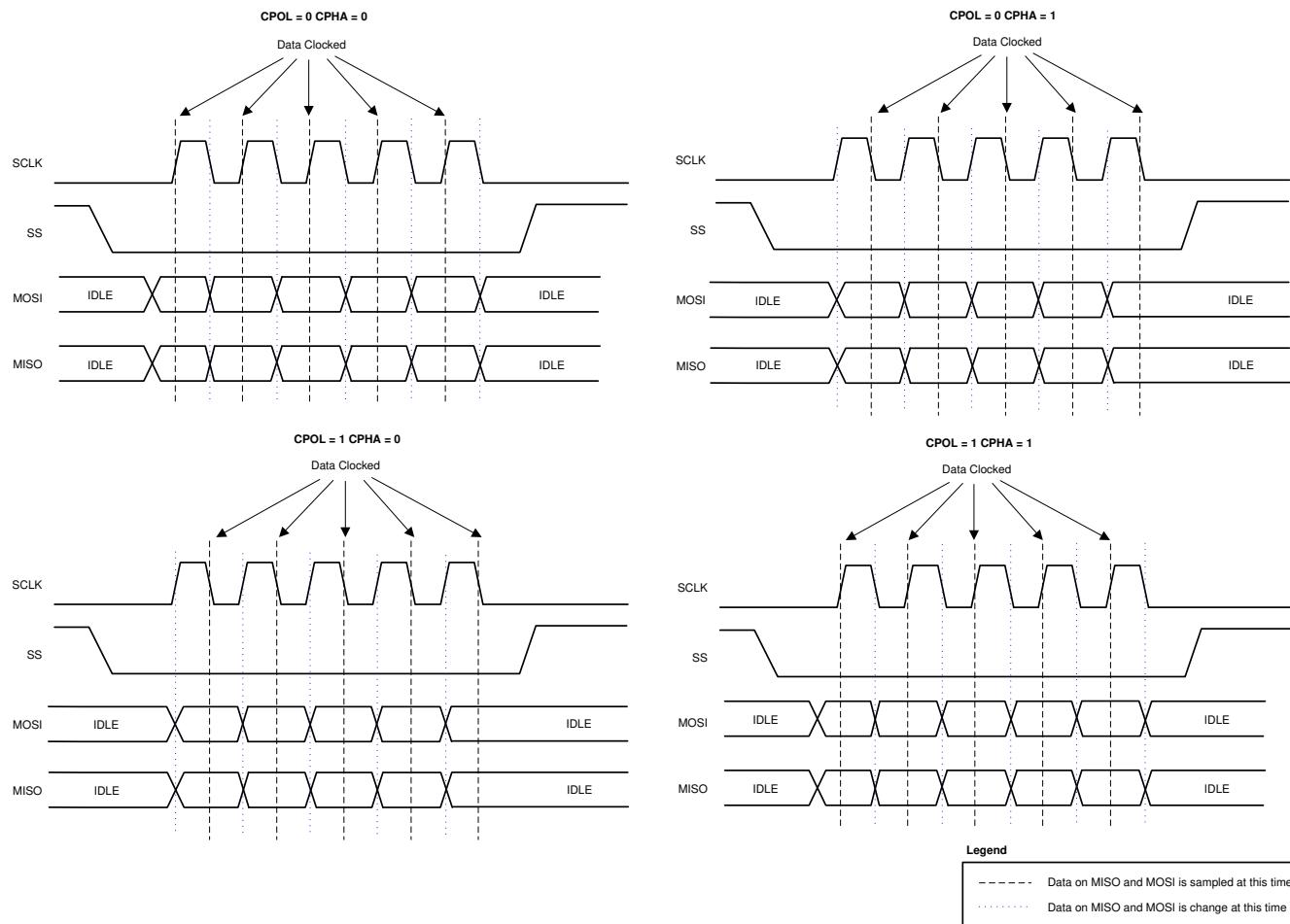


图 8-28. SPI Controller CPOL and CPHA

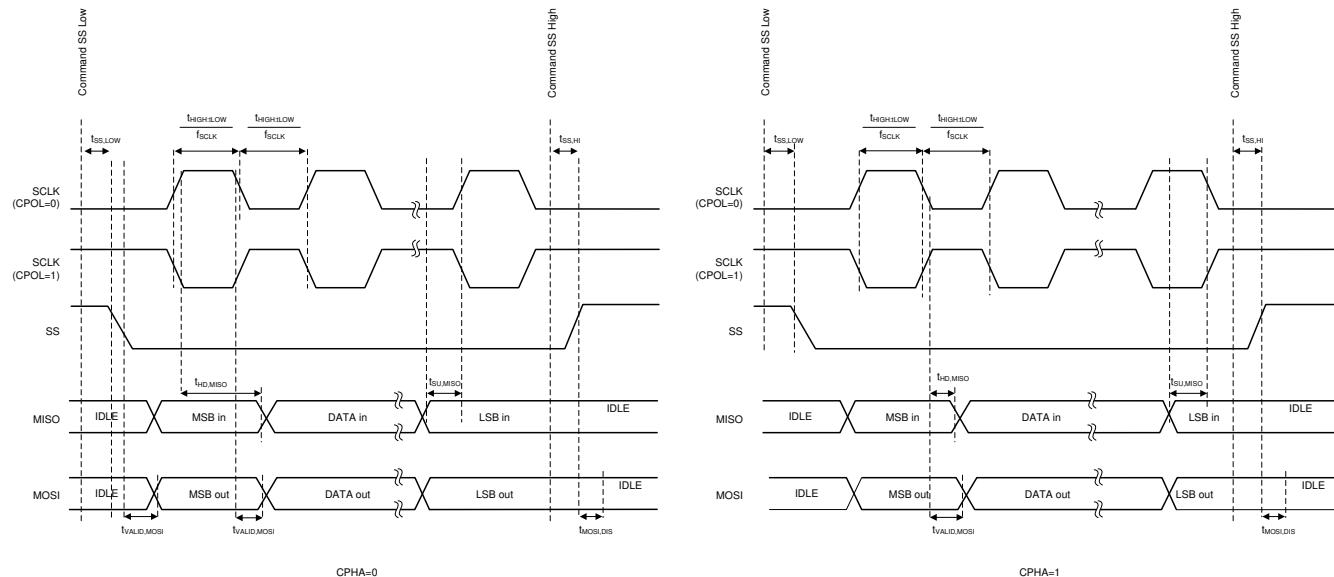


图 8-29. SPI Controller Timing Diagram

表 8-15. Write to External SPI Peripheral

| Step | Description |
|------|--|
| 1 | Configure the SPI clock polarity, clock phase, number of bit transactions: a. Write to <i>SPI_CONF</i> register to configure SPI communication |
| 2 | Write the data (from 1 to 24 bits, specified in the <i>SPI_CONF[NUMBIT4:0]</i> setting): a. Set up the data to send to SPI peripheral to the <i>SPI_TX1</i> to <i>SPI_TX3</i> registers b. <i>SPI_TX1</i> is the LSByte and <i>SPI_TX3</i> is MSByte |
| 3 | Select the peripheral (assuming active low) and execute the SPI write action: a. Send <i>SPI_EXE</i> register = 0x01 (that is, <i>[SS_CTRL]</i> = 0 and <i>[SPI_GO]</i> = 1) |
| 4 | Wait for the SPI communication to complete |
| 5 | Deselect the SS port (assuming active low, so deselecting means pull the SS pin high): a. Send <i>SPI_EXE</i> register = 0x02 (that is, <i>[SS_CTRL]</i> = 1 and <i>[SPI_GO]</i> = 0) |

表 8-16. Read from External SPI Peripheral

| Step | Description |
|------|---|
| 1 | Configure the SPI clock polarity, clock phase, number of bit transactions: a. Write to <i>SPI_CONF</i> register to configure SPI communication |
| 2 | Select the peripheral and execute the SPI communication: a. Send <i>SPI_EXE</i> register = 0x01 (that is, <i>[SS_CTRL]</i> = 0 and <i>[SPI_GO]</i> = 1) |
| 3 | Wait for the data transaction to complete |
| 4 | Read the data (from 1 to 24 bits, specified in the <i>SPI_CONF[NUMBIT4:0]</i> setting): a. Read data from SPI peripheral from the <i>SPI_RX1</i> to <i>SPI_RX3</i> registers b. <i>SPI_RX1</i> is the LSByte and <i>SPI_RX3</i> is MSByte |
| 5 | Deselect the SS port (assuming active low, so deselecting means pull the SS pin high): a. Send <i>SPI_EXE</i> register = 0x02 (that is, <i>[SS_CTRL]</i> = 1 and <i>[SPI_GO]</i> = 0) |

8.3.6.1.4 SPI Loopback

The SPI controller has a loopback function that is enabled using the *DIAG_COMM_CTRL[SPI_LOOPBACK]* bit. When enabled, the byte in the *SPI_TX** registers are clocked directly to the MISO pin of the SPI controller to verify the SPI controller functionality. This is performed internally, so no external connection is needed to run this test. This verifies that the SPI function is working correctly. The *SPI_CFG*, *SPI_TX**, and *SPI_EXE* registers are written as a normal SPI transaction, but the external pins do not toggle during this mode. That is, the external pins stay static in their last state and do not change state during the loopback operation.

The expected result of the test is that the byte in the *SPI_TX** register is read into the *SPI_RX** register. The SS pin is latched to the setting in *SPI_EXE/SS_CTRL* that existed when the LOOPBACK mode was enabled. The CPHA and CPOL parameters must be set before entering LOOPBACK mode to ensure proper operation. Changing the CPOL or CPHA parameters while in LOOPBACK mode may result in errant pulses on the SPI outputs and is not recommended.

8.3.6.2 Fault Handling

8.3.6.2.1 Fault Status Hierarchy

The device monitors multiple types of faults such as:

- Battery cell monitoring through the hardware protector, like cell OV/UV, cell OT/UT, and so on
- System operation driven like device reset, communication timeout, thermal warning, and so on
- Command-based diagnostic check related like the various comparison through the main and AUX ADCs, BIST run, and so on
- Automatic diagnostic check running in the background like the internal power supplies, OTP CRC, and so on
- Communication fault.

Each bit in the *FAULT_SUMMARY* register represents a group of faults which are stored in one or more lower level fault registers. The *FAULT_SUMMARY* register represents the highest hierarchy level of fault status detected by the device. Host system can periodically poll the *FAULT_SUMMARY* register to check the fault status and only read the lower level fault registers if needed (for example, if *FAULT_SUMMARY[FAULT_OVUV]*

= 1, host can read *FAULT_OV1/2* and *FAULT_UV1/2* registers to determine which cell channel triggered the fault).

表 8-17 shows which lower level register corresponds to the *FAULT_SUMMARY* register bit. The description of the register is covered in 节 8.5.

表 8-17. Low-Level Fault Registers

| FAULT_SUMMARY Bit Name | FAULT_PROT | FAULT_COMP_ADC | FAULT OTP | FAULT_COMM | FAULT_OTUT | FAULT_OVUV | FAULT_SYS | FAULT_PWR |
|---------------------------|--------------|-------------------|--------------------------|----------------------------|------------|------------|-----------|------------|
| Lower level register name | FAULT_PROT_1 | FAULT_COMP_GPIO | FAULT OTP ⁽¹⁾ | FAULT_COMM1 ⁽¹⁾ | FAULT_OT | FAULT_OV1 | FAULT_SYS | FAULT_PWR1 |
| | FAULT_PROT_2 | FAULT_COMP_VCCB1 | | | FAULT_UT | FAULT_OV2 | | FAULT_PWR2 |
| | | FAULT_COMP_VCCB2 | | | | FAULT_UV1 | | FAULT_PWR3 |
| | | FAULT_COMP_VCOW1 | | | | FAULT_UV2 | | |
| | | FAULT_COMP_VCOW2 | | | | | | |
| | | FAULT_COMP_CBOW1 | | | | | | |
| | | FAULT_COMP_CBOW2 | | | | | | |
| | | FAULT_COMP_CBFET1 | | | | | | |
| | | FAULT_COMP_CBFET2 | | | | | | |
| | | FAULT_COMP_MISC | | | | | | |

(1) Some of the bits in the *FAULT_COMM1/2* and *FAULT OTP* registers have a lower level of fault information than shown in the *DEBUG_COMM** and *DEBUG OTP* registers.

8.3.6.2.1.1 Debug Registers

The *DEBUG_COMM** and *DEBUG OTP* registers are a form of fault status showing lower hierarchy level of fault information for some of the bits in *FAULT_COMM1* and *FAULT OTP*.

表 8-18 shows the hierarchy relationship. See 节 8.5 for the register description details.

表 8-18. Debug Registers

| Low-level Fault Register | Low-level Register Bit | | Associated DEBUG Registers |
|--------------------------|------------------------|---|----------------------------|
| FAULT_COMM1 | [UART_RC] | Fault related to received command frame from UART | DEBUG_UART_RC |
| | [UART_RR] [UART_TR] | Fault related to received or transmitted response frame from UART | DEBUG_UART_RR_TR |
| FAULT OTP | [SEC_DET] | Single error correction in OTP | DEBUG OTP SEC_BLK |
| | [DED_DET] | Double error correction in OTP | DEBUG OTP DED_BLK |

8.3.6.2.2 Fault Masking and Reset

8.3.6.2.2.1 Fault Masking

When a device detects a fault, the corresponding low-level register bit, including the one in the related bit in the *DEBUG_** registers is set. Based on the fault hierarchy relationship, the fault will be reflected in the *FAULT_SUMMARY* register.

A group of faults can be masked, which the related low-level register flag will still be set, but the fault will not be reflected to the corresponding *FAULT_SUMMARY* register. The faults can be masked through the *FAULT_MSK1* and *FAULT_MSK2* registers.

For example, to mask the *FAULT_SUMMARY*[*FAULT_OTUT*] being set, host sets *FAULT_MSK1*[*MSK_OT*] = 1 and [*MSK_UT*] = 1.

When fault is masked, it will also prevent the device from asserting the *NFAULT* pin when the masked fault occurs. See 节 8.3.6.2.3 for details on *NFAULT* signal.

表 8-19. Fault Masking

| | Masking Bit Name | Related Low-level Register(s) Affected | FAULT_SUMMARY Register Bit That Will Be Masked |
|------------|------------------|---|--|
| FAULT_MSK1 | [MSK_PROT] | FAULT_PROT* | [FAULT_PROT] |
| | [MSK_UT] | FAULT_UT | [FAULT_UTUT] |
| | [MSK_OT] | FAULT_OT | |
| | [MSK_UV] | FAULT_UV* | [FAULT_OVUV] |
| | [MSK_OV] | FAULT_OV* | |
| | [MSK_COMP] | FAULT_COMP_* | [FAULT_COMP] |
| | [MSK_SYS] | FAULT_SYS | [FAULT_SYS] |
| | [MSK_PWR] | FAULT_PWR* | [FAULT_PWR] |
| FAULT_MSK2 | [MSK OTP_CRC] | FAULT OTP[CUST_CRC]/[FACT_CRC] | [FAULT OTP] |
| | [MSK OTP_DATA] | All non-CRC bits in FAULT OTP, DEBUG OTP_* | |
| | [MSK COMM1] | FAULT COMM1, DEBUG UART_* | [FAULT COMM1] |

8.3.6.2.2 Fault Reset

Once fault is detected, the fault status bit is latched until cleared using the reset bit. Similar to fault masking, when the specific fault reset bit is set, the associated low-level fault registers, including the *DEBUG_** registers are cleared. The corresponding bit in the *FAULT_SUMMARY* register will clear if all its associated low-level registers are cleared. If the fault condition persists and the reset bit is written, the fault status bit is not reset. The fault indicator cannot be reset until the underlying fault condition is eliminated.

The fault is reset through the *FAULT_RST1* and *FAULT_RST2* registers; the fault reset bits are structured in the same corresponding fault status registers as the fault masking bits.

8.3.6.2.3 Fault Signaling

Host can acquire the fault status with the following methods:

- Constantly polling the *FAULT_SUMMARY* status. If *FAULT_SUMMARY* is non-zero, read the low-level fault status registers to obtain more information.

The *NFAULT* pin can be masked by configuring *DEV_CONF/NFAULT_EN* = 0. When *NFAULT* is disabled, the device will set the corresponding flag in *FAULT_SUMMARY* register but will not assert *NFAULT*.

8.3.6.3 Nonvolatile Memory

There are memory locations that are programmable in nonvolatile memory (NVM) using OTP (One Time Programmable). The memory space is divided in two groups, factory space and customer space. The factory space stores the device configurations that are essential for normal operation. This space is not accessible by the host. The customer space contains the device default setting that host system can customize for their application configuration. This space is readable and programmable by the host.

When a device reset occurs, factory and customer OTP values are reloaded to their shadow registers. Error check and correction (ECC), single error correction (SEC) and double error detection (DED), are performed during the factory and customer space OTP load. The corresponding *FAULT OTP[SEC_DET]* or *FAULT OTP[DED_DET]* will be set if an error is detected.

Any load errors of the factory OTP space signal a fault using the *FAULT OTP[FACTLDERR]*. Any load errors of the customer OTP space signal a fault using the *FAULT OTP[CUSTLDERR]*. Additionally, the OTP space (factory and customer) are protected from data integrity problems using CRC. The corresponding *FAULT OTP[FACT_CRC]* and *[CUST_CRC]* bits will be set if a CRC error is detected.

If any overvoltage error conditions exist in the OTP pages space (factory and customer) during programming, the *OTP_FAULT[GBLOVERR]* bit is set. Information received from the device with this error must not be considered reliable.

8.3.6.3.1 OTP Page Status

There are two unused pages of OTP memory available for the customer to program. Each page status is held in the *OTP_CUST1_STAT* and *OTP_CUST2_STAT* registers. The registers provide information on the current status of the page such as:

- Load status (if loaded, loaded with error, loaded but failed)
- Programmed successfully or available to be programmed
- Programmed status

When a reset occurs, the device evaluates the OTP page status and chooses the latest and valid OTP page to load. Page 2 has priority over Page 1. If both pages have not been written, the factory OTP default are loaded.

节 8.5.1 shows all customer programmable OTP parameters. The register summary also shows the default values when Customer OTP Page 1 and Page 2 are not programmed.

- A valid page is one where the *OTP_CUST*_STAT[PROGOK]* = 1.
- When the page is selected for loading, the *OTP_CUST*_STAT1[LOADED]* = 1.
- If a single error occurs in the loading of the page, the page is loaded after the single error is corrected and the *OTP_CUST*_STAT1[LOADWRN]* = 1.
 - Additionally, the *DEBUG OTP SEC BLK* register is updated with the location of the error corrected block.
- If a double error occurs, the loading of that block is terminated and the hardware defaults of that block are loaded (as indicated in 节 8.5.1).
 - The overall page loading process is not terminated for a DED, only the affected block is terminated.
 - When a DED occurs, the *OTP_CUST*_STAT1[LOADERR]* = 1. Additionally, the *DEBUG OTP DED BLK* register is updated with the block where the double error occurred.

8.3.6.3.2 OTP Programming

节 8.5.1 shows all parameters that can be programmed to the customer OTP page. There are two pages of OTP memory available for customer to use.

Before programming the OTP, host ensures:

- All OTP shadow registers have the correct settings
- A customer OTP page is valid to be programmed. A valid page is one with *OTP_CUST*_STAT1[TRY]* = 0 and *OTP_CUST*_STAT1[FMTERR]* = 0.

表 8-20. Program the OTP

| Step | Procedure |
|------|---|
| 1 | <p>Unlock the OTP programming:</p> <p>a. Write the following data to <i>OTP_PROG_UNLOCK1A</i> to <i>OTP_PROG_UNLOCK1D</i> registers.</p> <ul style="list-style-type: none"> • <i>OTP_PROG_UNLOCK1A</i> <- data 0x02 • <i>OTP_PROG_UNLOCK1B</i> <- data 0xB7 • <i>OTP_PROG_UNLOCK1C</i> <- data 0x78 • <i>OTP_PROG_UNLOCK1D</i> <- data 0xBC <p>b. Do another write with the following data to <i>OTP_PROG_UNLOCK2A</i> to <i>OTP_PROG_UNLOCK2D</i> registers.</p> <ul style="list-style-type: none"> • <i>OTP_PROG_UNLOCK2A</i> <- data 0x7E • <i>OTP_PROG_UNLOCK2B</i> <- data 0x12 • <i>OTP_PROG_UNLOCK2C</i> <- data 0x08 • <i>OTP_PROG_UNLOCK2D</i> <- data 0x6F <p>Each block of registers must be written in order (that is, A, B, C, then D) with no other writes or reads between. The best practice is to use the same Write command to update. Any attempt to update the registers out of sequence, or if another register is written or read between writes, the entire sequence must be redone.</p> |
| 2 | <p>Check to confirm the OTP unlock procedure is successful:</p> <p>a. Read to confirm <i>OTP_PROG_STAT[UNLOCK]</i> = 1</p> <p>Issuing a Read command after step 1 is ok, but issuing the <i>[PROG_GO]</i> must be the next write command after the unlock procedures.</p> |

表 8-20. Program the OTP (续)

| Step | Procedure |
|------|---|
| 3 | Select the proper OTP page and start the OTP programming: a. To program page1, set <i>OTP_PROG_CTRL[PAGESEL][PROG_GO]</i> = 0x01, or b. To program page2, set <i>OTP_PROG_CTRL[PAGESEL][PROG_GO]</i> = 0x03 |
| 4 | Wait <i>t_{PROG}</i> for the OTP programming to complete |
| 5 | Check to ensure there is no error during OTP programming. The following bits are expected to be 1 after a successful OTP programming: a. <i>OTP_PROG_STAT[DONE]</i> = 1, OTP programming is done. No other bit will be set in this register. b. If page 1 is programmed, <i>OTP_CUST1_STAT[PROGOK], [TRY], [OVOK]</i> , and <i>[UVOK]</i> bits are 1. Other bits are 0. c. If page 2 is programmed, <i>OTP_CUST2_STAT[LOADED], [PROGOK], [TRY], [OVOK]</i> , and <i>[UVOK]</i> bits are 1. Other bits are 0. |
| 6 | Issue a digital reset to reload the registers with the updated OTP values: a. <i>CONTROL1[SOFT_RESET]</i> = 1 |

During programming, if a programming voltage OV or UV event occurs, the *OTP_CUST*_STAT[UVOK]* or *OTP_CUST_STAT2[OVOK]* bit is 0 to indicate the programming voltage under- or overvoltage condition is detected during the programming attempts. In addition, the *[UVERR], [OVERR], [SUVERR]*, and *[SOVERR]* bits in the *OTP_PROG_STAT* register indicate if there is programming voltage error during programming and stability test.

备注

- During the programming procedure, device performs a programming voltage stability test before actually programming the OTP. If a programming voltage fails the stability test, the device will not set the *OTP_CUST*_STAT[TRY]* bit, giving the customer another attempt to program the page again.
- If the host incorrectly selects a page for programming, the *OTP_PROG_STAT[PROGERR]* bit is set. This indicates that the selected page was not available to be programmed. Select the correct page and retry the programming.
- Device will not start OTP programming above 55°C temperature.
- OTP programming time (from *[PROG_GO]* = 1 to *[DONE]* = 1) for LDOIN capacitor of 0.1 μF is 100ms.

8.3.6.4 Diagnostic Control/Status

The device complies with applicable component level requirements for ASIL-D on voltage measurement, temperature measurement and communication. The following sub-sections describe the diagnostic control and fault status that can be used as part of the safety mechanisms.

The Safety Manual for BQ7961x-Q1 and the BQ79606-Q1 FMEDA documents are available separately from Texas Instruments. Contact TI Sales Associate or Applications Engineer for further information.

8.3.6.4.1 Power Supplies Check

8.3.6.4.1.1 Power Supply Diagnostic Check

The internal power supply circuits have overvoltage, undervoltage, oscillation detection, and/or current limit checks. All these detections are continuously running in the background when the device is in ACTIVE or SLEEP mode. If a failure is detected, the corresponding flags in the *FAULT_PWR** registers will be set or in certain failure modes, the device will reset. 表 8-21 summarizes the diagnostics that apply for each power supply and the corresponding action when failure is detected.

表 8-21. Power Supply Diagnostic Checks

| Supply/ Ground Pin | OV Check | UV Check | OSC Check | Current Limit | Pin Open |
|-----------------------|----------|----------|-----------|---------------|----------|
| LDOIN | | | | | |

表 8-21. Power Supply Diagnostic Checks (续)

| Supply/ Ground Pin | OV Check | UV Check | OSC Check | Current Limit | Pin Open |
|-----------------------|---|--|---|---|---|
| AVDD | If this fails, set <i>FAULT_PWR1[AVDD_OV]</i> | If this fails, disable DVDD and trigger a digital reset. After soft reset, device sets <i>[AVDDUV_DRST]</i> to indicate a reset is caused by AVDD UV. | If fails, set <i>FAULT_PWR1[AVDD_OSC]</i> | Limit current to EC table current limit specification | |
| DVDD | If this fails, set <i>FAULT_PWR1[DVDD_OV]</i> | If this fails, trigger a digital reset | | Limit current to EC table current limit specification | |
| CVDD | If this fails, set <i>FAULT_PWR1[CVDD_OV]</i> | If this fails, set <i>FAULT_PWR1[CVDD_UV]</i> | | Limit current to EC table current limit specification | |
| TSREF | If this fails, set <i>FAULT_PWR2[TSREF_OV]</i> and <i>FAULT_OT</i> and <i>FAULT_UT</i> registers to all 1s. | If this fails, set <i>FAULT_PWR2[TSREF_UV]</i> and <i>FAULT_OT</i> and <i>FAULT_UT</i> registers to all 1s. | If fails, set <i>FAULT_PWR2[TSREF_OSC]</i> and <i>FAULT_OT</i> and <i>FAULT_UT</i> registers to all 1s. | Limit current to EC table current limit specification | |
| NEG5V | | If this fails, set <i>FAULT_PWR2[NEG5V_UV]</i> | | | |
| REFHP/REFHM | | | If REFHP fails, set <i>FAULT_PWR2[REFH_OSC]</i> | | If REFHM opens, set the <i>FAULT_PWR1[REFHM_OPEN]</i> |
| DVSS | | | | | If this opens, set the <i>FAULT_PWR1[DVSS_OPEN]</i> |
| CVSS | | | | | If this opens, set the <i>FAULT_PWR1[CVSS_OPEN]</i> |

备注

Due to the detection logic implemented, when AVDD OV or UV is detected, the AVDD OSC fault can also be triggered. Similarly, when TSREF OV or UV, the TSREF OSC fault can also be triggered.

8.3.6.4.1.2 Power Supply BIST

The device implements a power supply BIST (Built-In Self-Test) function to test the primary power supply failure diagnostic paths that cover the following detections:

- *FAULT_PWR1[AVDD_OV]*, *[AVDD_OSC]*, *[DVDD_OV]*, *[CVDD_OV]*, *[CVDD_UV]*, *[REFHM_OPEN]*, *[DVSS_OPEN]*, and *[CVSS_OPEN]*
- *FAULT_PWR2[TSREF_OV]*, *[TSREF_UV]*, *[TSREF_OSC]*, *[NEG5V_UV]*, *[REFHM_OSC]*, and *[PWRBIST_FAIL]*

The power supply BIST is essentially a check on the checker and it is a command base function initiated by host.

The power supply BIST, once started, will force a fault on failure detection path on each supply. Take AVDD OV diagnostic path as an example, when the BIST engine tests the AVDD OV path, the following occur:

1. The BIST engine forces a fail to the AVDD OV comparator
2. The BIST engine then checks to ensure the signal to trigger *FAULT* register is asserted, and the signal to trigger *NFAULT* is also asserted
3. The BIST engine resets the *FAULT* register and *NFAULT* signal (that is, clears the *FAULT_PWR1/2/3* registers and deasserts *NFAULT*)

4. The BIST engine repeats step 1 to step 3 on the next power supply diagnostic path check (for example, AVDD OSC) until all intended diagnostic paths covered by BIST are tested.

备注

- During the BIST run, the NFAULT pin will be toggled on and off. Host ignores the NFAULT pin status or can disable the NFAULT pin output by setting *DEV_CONF[NFAULT_EN]* = 0.
- Among all internal power supplies, TSREF is one that can be enabled or disabled by host. To ensure TSREF diagnostic paths are tested during BIST run, host enables TSREF before starting the power supply BIST. Otherwise, the BIST engine will ignore the TSREF diagnostic paths test result during the BIST run.
- Because other nonpower supply-related faults can also trigger NFAULT, it is recommended to mask all nonpower supply-related faults through *FAULT_MSK1/2* registers before the power supply BIST run.
- Host also ensures there are no power supply faults before starting the power supply BIST run.

Start power supply BIST by sending *DIAG_PWR_CTRL[PWR_BIST_GO]* = 1. The BIST run will not abort even if a failure is detected during the run. At the end of the BIST run, the result is indicated by the *FAULT_PWR2[PWRBIST_FAIL]* flag.

The power supply BIST forces a failure and ensures the diagnostic path triggers the fault accordingly. A failure on the BIST run indicates a diagnostic path is unable to trigger in a fault condition. To further examine which path is unable to indicate a failure, host can set the *DIAG_PWR_CTRL[BIST_NO_RST]* = 1. This bit disables the reset step during the BIST run. Re-start power supply BIST with this option enabled. At the end of the BIST run, examine the *FAULT_PWR1* and *FAULT_PWR2* registers. Any register flag that remains 0 indicates it is unable to flag a failure.

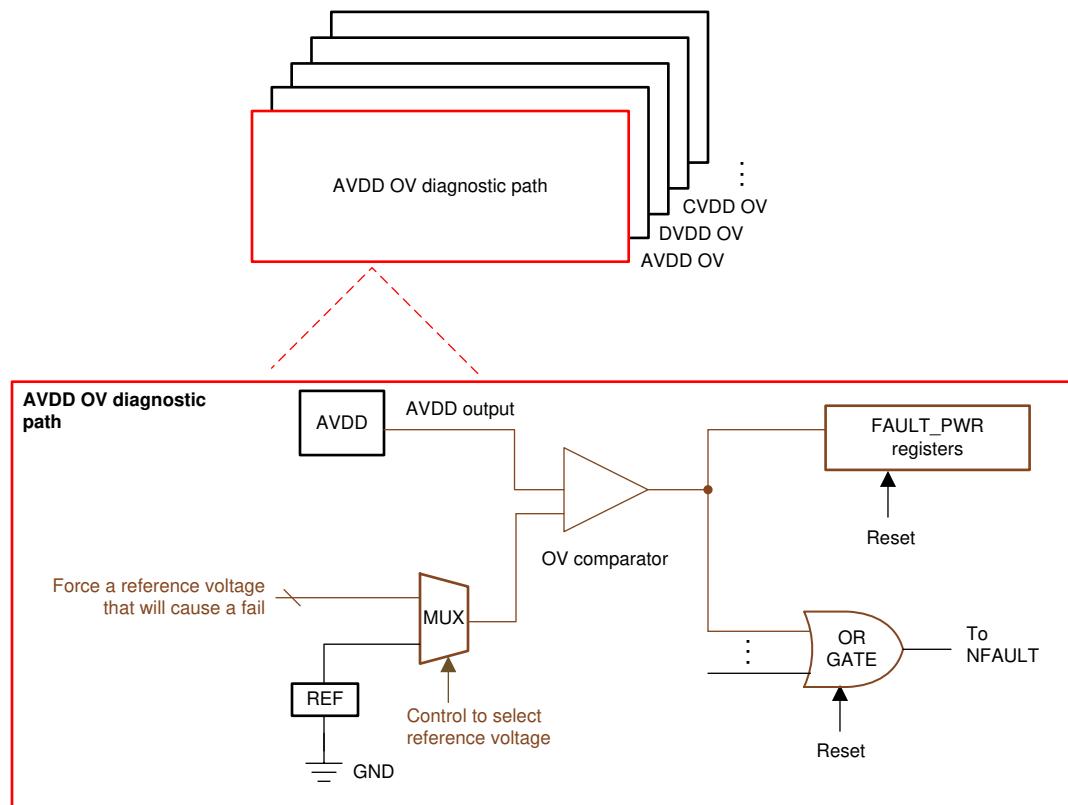


图 8-30. Power Supply BIST

8.3.6.4.2 Thermal Shutdown and Warning Check

8.3.6.4.2.1 Thermal Shutdown

Thermal shutdown occurs when the thermal shutdown sensor senses an overtemperature condition of the device. The sensor operates without interaction and is separated from the ADC measured die sensor. The thermal shutdown function has a register-status indicator flag (*FAULT_SYS[TSHUT]*) that is saved during the shutdown event and can be read after the device is awoken back up. When a TSHUT fault occurs, the part immediately enters the SHUTDOWN mode. Any pending transactions on UART are discarded. There is no fault signaling performed when a thermal shutdown event occurs as the device immediately shuts down.

To awaken the device, host ensures the ambient temperature is below T_{SHUT_FALL} and sends a WAKE ping to the device. Host will not attempt to wake the device if the ambient temperature is still above T_{SHUT_FALL} .

Upon waking up, the *FAULT_SYS[TSHUT]* bit is set. See [节 8.4.1.1](#) for more details. If the system faults are unmasked, *FAULT_MSK1[MSK_SYS]* = 0, the thermal shutdown will be reflected as a fault and will be indicated in the *FAULT_SUMMARY* register and the assertion of the *NFAULT* pin.

8.3.6.4.2.2 Thermal Warning

To warn the host of an impending thermal overload the device includes an overtemperature warning that signals a fault when the die temperature approaches thermal shutdown. The device detects the die temperature through the *TWARN* sensor against the thermal warning threshold. There are four threshold options configured by the *PWR_TRANSIT_CONF[TWARN_THR1:0]* setting.

When the system fault is unmasked, and the temperature warning fault occurs, the *FAULT_SYS[TWARN]* = 1. Host can take action to avoid a thermal shutdown.

8.3.6.4.3 Oscillators Watchdog

The oscillators are monitored by watchdog circuits. There are two oscillators in the device, the HFO and the LFO. If these oscillators are not functioning, the device does not operate. If the HFO or LFO does not transition within the expected time, the watchdog circuits causes a digital reset.

When this unexpected reset occurs, it is recommended that the host sends a SHUTDOWN ping to the problem device and then send a WAKE ping to reset. If the oscillators are truly damaged, the device will not restart and must be replaced.

In addition to the watchdog, the LFO frequency is monitored to ensure it stays within acceptable limits. If the LFO frequency falls outside of the expected range, the *FAULT_SYS_FAULT[LFO]* bit is set.

8.3.6.4.4 OTP Error Check

8.3.6.4.4.1 OTP CRC Test and Faults

CRC Test:

The factory registers and customer OTP shadow registers are covered by a CRC check that constantly runs in the background. The *CUST_CRC_RSLT_HI* and *CUST_CRC_RSLT_LO* registers hold the current device's computed CRC value. This value is compared against the customer programmed value in the CRC registers, *CUST_CRC_HI* and *CUST_CRC_LO*. When updating any customer OTP shadow register covered in the CRC, the host must update a new CRC value to *CUST_CRC_HI* and *CUST_CRC_LO* registers. The CRC calculation is performed in the same manner (including the bit stream ordering) and with the same polynomial as described in [节 8.3.6.1.1.2.1.6](#). The CRC check and comparison for factory and customer spaces is performed periodically and the *DEV_STAT[CUST_CRC_DONE]* and *[FACT_CRC_DONE]* bits are set after the check is complete. If the bit is already set, it remains set until cleared with a read.

CRC Faults:

When *CUST_CRC_HI/LO* and *CUST_CRC_RSLT_HI/LO* do not match, the *FAULT_OTP[CUST_CRC]* flag is set until the condition is corrected. Continuous monitoring of the factory NVM space occurs in a similar fashion, concurrently with the monitoring of the customer space. When a factory register change is detected, the *FAULT_OTP[FACT_CRC]* flag is set. When this fault occurs, the host should reset the fault flag to see if the fault

persists. If the fault persists, the host must perform a reset of the part. If reset does not correct the issue, the device is corrupted and must not be used.

8.3.6.4.4.2 OTP Margin Read

The device provides OTP margin read test modes, with which host can set up to reload the OTP with margin 1 or margin 0. To start the margin read test, host selects the desired test mode through *DIAG OTP_CTRL[MARGIN_MODE2:0]* and sets *DIAG OTP_CTRL[MARGIN_GO]* = 1. The device will reload the OTP per the *[MARGIN_MODE2:0]* setting. Any OTP related error will be flagged to the *FAULT OTP* register.

8.3.6.4.4.3 Error Check and Correct (ECC) OTP

ECC:

Register values for selected registers (0x0000 to 0x002F) are permanently stored in OTP. All registers also exist as volatile storage locations at the same addresses, referred to as shadow registers. The volatile registers are for reading, writing, and device control. For a list of registers included in the OTP, see [节 8.5.1](#).

During wakeup, the device first loads all shadow registers with hardware default values listed in [节 8.5.1](#). Then the device loads the registers conditionally with OTP contents from the results of the Error Check and Correct (ECC) evaluation of the OTP. The OTP is loaded to shadow registers in 64-bit blocks; each block has its own Error Check and Correct (ECC) value stored. The ECC detects a single-bit (Single-Error-Correction) or double-bit (Double-Error-Detection) changes in OTP stored data. The ECC is calculated for each block, individually.

Single-bit errors are corrected, double-bit errors are only detected, not corrected. A block with good ECC is loaded. A block with a single-bit error is corrected, and the *FAULT OTP[SEC_DET]* bit is set to flag the corrected error event. Additionally, the *DEBUG OTP SEC BLK* register is updated with the location of the error corrected block. This enables the host to keep track of potentially damaged memory. The block is loaded to shadow registers after the single-bit error correction. Because the evaluation is on a block-by-block basis, it is possible for multiple blocks to have a single-correctable error and still be loaded correctly. Multiple-bit errors can exist with full correction, as long as they are limited to a single error per block.

A block with a bad ECC comparison (two-bit errors in one block) is not loaded and the *FAULT OTP[DED_DET]* bit is set to flag the failed bit-error event. Additionally, the *DEBUG OTP DED BLK* register is updated with the block where the double error occurred. The hardware default value remains in the register. This allows some blocks to be loaded correctly (no fail or single-bit corrected value) and some blocks not to load. When the *FAULT OTP[SEC_DET]* or *FAULT OTP[DED_DET]* bit is set and the condition is not cleared by a device reset, the device is corrupted and must not be used.

The ECC engine uses the industry standard 72,64 SEC DEC ECC implementation. The OTP is protected by a (72, 64) Hamming code, providing single error correction, double error detection (SECDED). For each 64 bits of data stored in OTP, an additional 8 bits of parity information are stored. The parity bits are designated p0, p1, p2, p4, p8, p16, p32, and p64. Bit p0 covers the entire encoded 72-bit ECC block. The remaining seven parity bits are assigned according to the following rule:

- Parity bit p1 covers odd bit positions, that is, bit positions which have the least significant bit of the bit position equal to 1 (1, 3, 5, and so on), including the p1 bit itself (bit 1).
- Parity bit p2 covers bit positions which have the second least significant bit of the bit position equal to 1 (2, 3, 6, 7, 10, 11, and so on), including the p2 bit itself (bit 2).
- The pattern continues for p4, p8, p16, p32, and p64. [表 8-22](#) specifies the complete encoding.

表 8-22. (72, 64) Parity Encoding

| Bit Position | | 71 | 70 | 69 | 68 | 67 | 66 | 65 | 64 | 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 |
|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Encoded Bits | | d63 | d62 | d61 | d60 | d59 | d58 | d57 | p64 | d56 | d55 | d54 | d53 | d52 | d51 | d50 | d49 | d48 | d47 |
| Parity Bit Coverage | p0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | |
| | p1 | x | | x | | x | | x | | x | | x | | x | | x | | x | |
| | p2 | x | x | | | x | x | | | x | x | | | x | x | | x | x | |
| | p4 | x | x | x | x | | | | | x | x | x | x | | | | x | x | |
| | p8 | | | | | | | | | x | x | x | x | x | x | x | x | | |
| | p16 | | | | | | | | | x | x | x | x | x | x | x | x | x | |
| | p32 | | | | | | | | | x | x | x | x | x | x | x | x | x | |
| | p64 | x | x | x | x | x | x | x | x | | | | | | | | | | |
| Bit Position | | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 |
| Encoded Bits | | d46 | d45 | d44 | d43 | d42 | d41 | d40 | d39 | d38 | d37 | d36 | d35 | d34 | d33 | d32 | d31 | d30 | d29 |
| Parity Bit Coverage | p0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | |
| | p1 | x | | x | | x | | x | | x | | x | | x | | x | | x | |
| | p2 | | | x | x | | | x | x | | | x | x | | | x | x | | |
| | p4 | x | x | | | | | x | x | x | x | | | | | x | x | x | |
| | p8 | | | | | | | x | x | x | x | x | x | x | x | x | | | |
| | p16 | x | x | x | x | x | x | | | | | | | | | | | | |
| | p32 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | |
| | p64 | | | | | | | | | | | | | | | | | | |
| Bit Position | | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 |
| Encoded Bits | | d28 | d27 | d26 | p32 | d25 | d24 | d23 | d22 | d21 | d20 | d19 | d18 | d17 | d16 | d15 | d14 | d13 | d12 |
| Parity Bit Coverage | p0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | |
| | p1 | x | | x | | x | | x | | x | | x | | x | | x | | x | |
| | p2 | x | x | | | x | x | | | x | x | | | x | x | | | x | |
| | p4 | | | | x | x | x | x | | | | | x | x | x | x | | | |
| | p8 | | | | x | x | x | x | x | x | x | x | x | | | | | | |
| | p16 | | | | x | x | x | x | x | x | x | x | x | x | x | x | x | x | |
| | p32 | x | x | x | x | | | | | | | | | | | | | | |
| | p64 | | | | | | | | | | | | | | | | | | |
| Bit Position | | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Encoded Bits | | d11 | p16 | d10 | d9 | d8 | d7 | d6 | d5 | d4 | p8 | d36 | d2 | d1 | p4 | d0 | p2 | p1 | p0 |
| Parity Bit Coverage | p0 | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | |
| | p1 | x | | x | | x | | x | | x | | x | | x | | x | | x | |
| | p2 | | | x | x | | | x | x | | | x | x | | | x | x | | |
| | p4 | | | x | x | x | x | | | | x | x | x | x | | | | | |
| | p8 | | | x | x | x | x | x | x | x | | | | | | | | | |
| | p16 | x | x | | | | | | | | | | | | | | | | |
| | p32 | | | | | | | | | | | | | | | | | | |
| | p64 | | | | | | | | | | | | | | | | | | |

表 8-23. Encoder and Decoder Data IN and OUT Positioning

| ENCODER | | | |
|------------------|--------------|-------------------|---------------|
| DATA IN | Encoded Bits | DATA OUT | Bit Positions |
| OTP_ECC_DATAIN 1 | d0 to d7 | OTP_ECC_DATAOUT 1 | 0 to 7 |
| OTP_ECC_DATAIN 2 | d8 to d15 | OTP_ECC_DATAOUT 2 | 8 to 15 |
| OTP_ECC_DATAIN 3 | d16 to d23 | OTP_ECC_DATAOUT 3 | 16 to 23 |
| OTP_ECC_DATAIN 4 | d24 to d31 | OTP_ECC_DATAOUT 4 | 24 to 31 |
| OTP_ECC_DATAIN 5 | d32 to d39 | OTP_ECC_DATAOUT 5 | 32 to 39 |
| OTP_ECC_DATAIN 6 | d40 to d47 | OTP_ECC_DATAOUT 6 | 40 to 47 |
| OTP_ECC_DATAIN 7 | d48 to d55 | OTP_ECC_DATAOUT 7 | 48 to 55 |
| OTP_ECC_DATAIN 8 | d56 to d63 | OTP_ECC_DATAOUT 8 | 56 to 63 |
| | | OTP_ECC_DATAOUT 9 | 64 to 71 |

| DECODER | | | |
|------------------|---------------|-------------------|--------------|
| DATA IN | Bit Positions | DATA IN | Encoded Bits |
| OTP_ECC_DATAIN 1 | 0 to 7 | OTP_ECC_DATAOUT 1 | d0 to d7 |
| OTP_ECC_DATAIN 2 | 8 to 15 | OTP_ECC_DATAOUT 2 | d8 to d15 |
| OTP_ECC_DATAIN 3 | 16 to 23 | OTP_ECC_DATAOUT 3 | d16 to d23 |
| OTP_ECC_DATAIN 4 | 24 to 31 | OTP_ECC_DATAOUT 4 | d24 to d31 |
| OTP_ECC_DATAIN 5 | 32 to 39 | OTP_ECC_DATAOUT 5 | d32 to d39 |
| OTP_ECC_DATAIN 6 | 40 to 47 | OTP_ECC_DATAOUT 6 | d40 to d47 |
| OTP_ECC_DATAIN 7 | 48 to 55 | OTP_ECC_DATAOUT 7 | d48 to d55 |
| OTP_ECC_DATAIN 8 | 56 to 63 | OTP_ECC_DATAOUT 8 | d56 to d63 |
| OTP_ECC_DATAIN 9 | 64 to 71 | | |

ECC Diagnostic Test: The device provides a diagnostic tool to test the ECC function. There are two modes that are available to run the diagnostic. The first, auto mode (*OTP_ECC_TEST[MANUAL_AUTO]* = 0), uses internal data to run the tests. In auto mode, the *OTP_ECC_TEST[DED_SEC]* bit selects the type of test that is to be performed and the *OTP_ECC_TEST[ENC_DEC]* bit determines if the encoder or decoder function is to be tested. The result of the ECC test is provided in the *OTP_ECC_DATAOUT** registers within 1 μ s delay. The test steps and expected results from each test are shown below.

Automatic Decoding steps:

1. Set ECC Test to automatic *OTP_ECC_TEST[MANUAL_AUTO]* = 0
2. Set decoder setting *OTP_ECC_TEST[ENC_DEC]* = 0
3. Set decoder to single or double encoding setting with *OTP_ECC_TEST[DED_SEC]* (1 for DED or 0 for SEC)
4. Clear all SEC/DED faults by *FAULT_RST2[RST_OTP_DATA]* = 1
5. Enable ECC test *OTP_ECC_TEST[ENABLE]* = 1
6. Read *FAULT_OTP[SEC_DET]* flag for SEC or *FAULT_OTP[DED_DET]* flag for DED
7. Block read *OTP_ECC_DATAOUT1* to *OTP_ECC_DATAOUT8* to verify the decoder test results as in 表 8-24
8. Disable ECC test *OTP_ECC_TEST[ENABLE]* = 0

Automatic Encoding steps:

1. Set ECC TEST to automatic *OTP_ECC_TEST[MANUAL_AUTO]* = 0
2. Set the encoder setting using *OTP_ECC_TEST[ENC_DEC]* = 1
3. Enable the ECC test with *OTP_ECC_TEST[ENABLE]* = 1
4. Block read *OTP_ECC_DATAOUT1* to *OTP_ECC_DATAOUT9* to verify the encoder test results as in 表 8-24
5. Disable ECC test *OTP_ECC_TEST[ENABLE]* = 0

表 8-24. Decoder and Encoder Test Verification

| [DED_SEC] | [ENC_DEC] | [SEC_DET] | [DED_DET] | OTP_DATAOUT* |
|--------------|------------------|-----------|-----------|-----------------------|
| 0 (SEC test) | 0 (Decoder test) | 1 | 0 | 0x18C3 FF8A 68A9 8069 |

表 8-24. Decoder and Encoder Test Verification (续)

| [DED_SEC] | [ENC_DEC] | [SEC_DET] | [DED_DET] | OTP_DATAOUT* |
|--------------|------------------|-----------|-----------|--------------------------|
| 0 (SEC test) | 1 (Encoder test) | N/A | N/A | 0xCD 3968 C140 2EA5 ED6D |
| 1 (DED test) | 0 (Decoder test) | 0 | 1 | 0x0000 0000 0000 0000 |
| 1 (DED test) | 1 (Encoder test) | N/A | N/A | 0xCD 3968 C140 2EA5 ED6D |

8.3.6.4.5 Integrated Hardware Protector Check

8.3.6.4.5.1 Parity Check

When the OVUV and OTUT protectors are enabled, the register settings related to the OVUV and OTUT configurations are latched to protector blocks. The device will check periodically in the background to ensure the latched configurations remain the same throughout the protector operation.

The parity check covers the following latched setting. If a parity fault in the OVUV protector is detected, the device will set the *FAULT_PROT1[VPARITY_FAIL]* = 1. If a parity fault in the OTUT protector is detected, the device will set the *FAULT_PROT1[TPARITY_FAIL]* = 1.

表 8-25. Protector Parity Check Settings

| OVUV Protector | OTUT Protector | Note |
|----------------------------|-----------------------------------|--|
| OV threshold, UV threshold | OT threshold, UT threshold | Ensure threshold settings remains the same during the operation |
| OVUV_MODE setting | OTUT_MODE setting | Ensure the protector doesn't switch to a different operation mode |
| NUM_CELL setting | GPIO_CONF1 to GPIO_CONF4 settings | Ensure the active channel (either cell channels for OVUV or GPIO channel for OTUT) remains the same during operation |

8.3.6.4.5.2 OVUV and OTUT DAC Check

The OV, UV, OT, and UT DAC values are multiplexed to the AUX ADC from which the host can read out the values as part of the diagnostic check on the protector threshold settings.

To measure the protector's DAC value, it is recommended to lock the OVUV or OTUT protectors to a single channel through *OVUV_CTRL[OVUV_LOCK3:0]* for OV and UV DAC measurement; and through *OTUT_CTRL[OTUT_LOCK2:0]* for OT and UT DAC measurement, and restart the OVUV protectors or OTUT protector to run in the single channel run mode. Host ensures the locked cell channel is not under OV or UV fault or the locked GPIO channel is not under OT or UT fault. Otherwise, the DAC measurement will not be reflecting the triggering threshold value. Note that the OV and UV DAC value is (0.8 x the threshold setting).

8.3.6.4.5.3 OVUV Protector BIST

The device implemented an OVUV BIST (Built-In-Self-Test) function to test the primary OVUV protector path. Host can start the BIST run by setting *[OVUV_MODE1:0]* = 0b10 and *[OVUV_GO]* = 1. The BIST run covers:

1. OV and UV comparators thresholds:
 - a. A higher and lower than the set threshold are checked to ensure the comparator is triggered correctly.
 - b. If failure is detected, the corresponding *FAULT_PROT2[OVCOMP_FAIL]* or *[UVCOMP_FAIL]* bit will be set.
2. The path from the OVUV MUX to UV fault status bit and NFAULT pin:
 - a. For each VC channel, a switch is open so that input to the OVUV MUX is open and will lead to a UV detection to the channel under test
 - b. The BIST engine then checks the logic to assert corresponding *FAULT_UV* register bit and the NFAULT is set properly.
 - c. The BIST engine resets the corresponding *FAULT_UV* bit and deasserts the NFAULT, then switches to test the next channel and repeats the process until all active channels are tested.
 - d. If failure is detected, the corresponding *[VPATH_FAIL]* bit is set.
3. OV fault bit and NFAULT path

- a. The BIST engine forces 1 to the *FAULT_OV** register, one bit at time, to ensure each *FAULT_OV** register bit can be set and the NFAULT can be asserted, accordingly.
- b. If failure is detected, the corresponding *[TPATH_FAIL]* bit will be set.

If NFAULT is enabled, host observes NFAULT toggling during the BIST run. Upon completion of the BIST run, the OVUV comparators will be turned off. Host starts the regular OVUV round robin mode by sending *[OVUV_GO]* = 1 with *[OVUV_MODE1:0]* = 0b01 (round robin mode).

备注

- If a *[OVUV_GO]* = 1 is sent during the OVUV BIST run, device will execute the new GO command based on the *[OVUV_MODE1:0]* setting.
- Before starting the OVUV Protector BIST, host masks out all the non-OVUV related faults, and ensures there are no OV and UV faults on any cell channels (recommended all cell voltages to be at least 100 mV apart from the OV or UV threshold during the BIST run). Otherwise, the BIST result is not invalid.
- After BIST starts, if pre-existing fault is detected before starting step 2, the BIST engine will be aborted and the *FAULT_PROT2[BIST_ABORT]* = 1.
- A no reset option, *DIAG_PROT_CTRL[PROT_BIST_NO_RST]* = 1, is available to command the BIST engine not to reset the fault status and NFAULT pin after testing each channel. If a BIST run fails, host can select this option and re-run BIST to detect which cell channel path is unable reflect a fault condition in the fault registers.

8.3.6.4.5.4 OTUT Protector BIST

The device implemented an OTUT BIST function to test the primary OTUT protector path. Host can start the BIST run by setting *[OTUT_MODE1:0]* = 0b10 and *[OTUT_GO]* = 1. The BIST run covers:

1. OT and UT comparator thresholds
 - a. A higher and lower than the set threshold are checked to ensure the comparator is triggering correctly.
 - b. If failure is detected, the corresponding *FAULT_PROT2[OTCOMP_FAIL]* or *[UTCOMP_FAIL]* bit will be set.
2. The path from GPIO MUX to UT fault bit and NFAULT path
 - a. For each GPIO channel, the GPIO is internally pulled up so the input to the OTUT MUX is high and will lead to a UT detection to the channel under test.
 - b. The BIST cycle then checks the logic to assert the corresponding *FAULT_UT* register bit and the NFAULT is set properly.
 - c. The BIST engine resets the corresponding *FAULT_UT* bit and deasserts the NFAULT, then switches to test the next channel.
 - d. If failure is detected, the corresponding *[TPATH_FAIL]* bit will be set.
3. OV fault bit and NFAULT path
 - a. The BIST engine forces 1 to the *FAULT_OT* register, one bit at time, to ensure each *FAULT_OT* register bit can be set and the NFAULT can be asserted, accordingly.
 - b. If failure is detected, the corresponding *[TPATH_FAIL]* bit will be set.

If NFAULT is enabled, host observes NFAULT toggling during the BIST run. Upon completion of the BIST run, the OTUT comparators will be turned off. Host starts the regular OTUT round robin mode by sending *[OTUT_GO]* = 1 with *[OTUT_MODE1:0]* = 0b01 (round robin mode).

备注

- If a *[OTUT_GO]* = 1 is sent during the OTUT BIST run, device will execute the new GO command based on the *[OVUV_MODE1:0]* setting.
- Before starting the OTUT Protector BIST, host masks out all non-OTUT related faults, and ensures there are no OT and UT faults on any GPIO during the BIST run). Otherwise, the BIST result is invalid.
- After BIST starts, if pre-existing fault is detected before starting step 2, the BIST engine will be aborted and the *FAULT_PROT2[BIST_ABORT]* = 1.
- A no reset option, *DIAG_PROT_CTRL[PROT_BIST_NO_RST]* = 1, is available to command the BIST engine not to reset the fault status and NFAULT pin after testing each channel. If a BIST run fails, host can select this option and re-run BIST to detect which GPIO channel path is unable to reflect a fault condition in the fault registers.

8.3.6.4.6 Diagnostic Through ADC Comparison

8.3.6.4.6.1 Cell Voltage Measurement Check

Cell voltage measurement path comparison:

The cell voltage measurement check is performed by comparing the prefiltered measurement result from Main ADC versus measurement result from AUX ADC. To read the compared value measured by Main ADC and AUX ADC, MCU has to set up this diagnostic check to lock on a single channel using *[AUX_CELL_SEL]* setting and start this diagnostic check. In this configuration, the compared values from Main ADC and AUX ADC are reported to *DIAG_MAIN_HI/LO* registers and *DIAG_AUX_HI/LO* registers respectively.

Both Main and AUX ADC has the same front end filters. This diagnostic time is mostly spent on waiting for the AAF on the AUX ADC path to settle. The *[AUX_SETTLE]* setting allows the MCU to make trade-off between diagnostic time and noise filter level. Additionally, when AUX ADC starts, by default, AUXCELL slot always align to the Main ADC Cell1 slot. The *[AUX_CELL_ALIGN]* setting allows MCU to change this alignment to Main ADC Cell8 slot, resulting with less sampling time delta between Main and AUX ADC on the higher channels.

The device does not do on-chip measurement check for SRP/SRN signal.

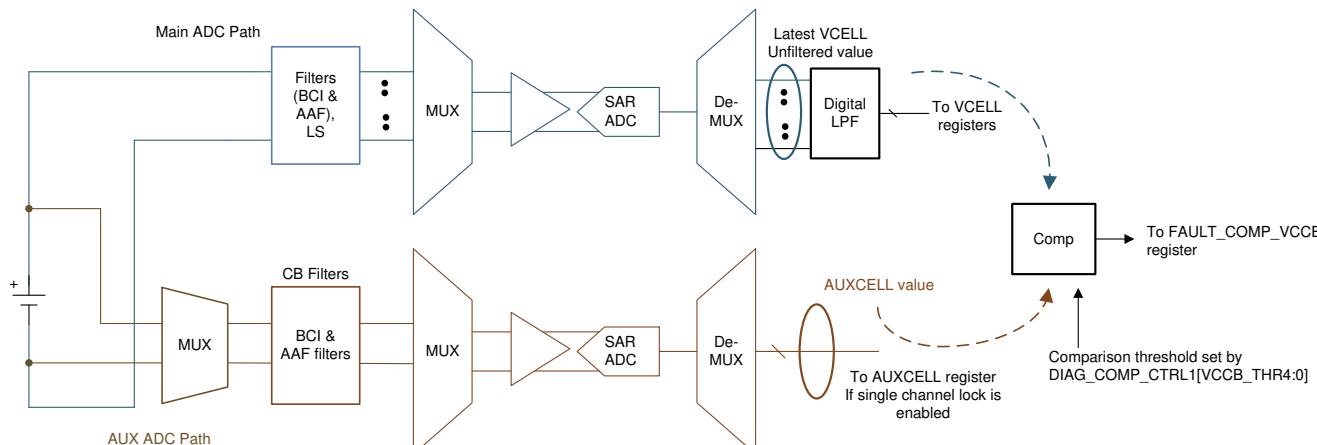


图 8-31. Cell Voltage Measurement Diagnostic

Before starting the cell voltage measurement comparison, host ensures:

- The desired AUXCELL channels to be tested are configured in the *ADC_CTRL2[AUX_CELL_SEL4:0]* setting and AUX ADC is enabled and in continuous mode.
- Allow AUX ADC to run through all AUXCELL channels for the device to compensate for common mode error before starting this diagnostic check.

- Main ADC must be enabled and is in continuous mode.
- Select the (VCELL - AUXCELL) comparison threshold through *DIAG_COMP_CTRL1[VCCB_THR4:0]* setting.
- Select the desired settling time for the AUX CELL channel through *ADC_CONF1[AUX_SETTLE1:0]*.

To start the cell voltage measurement comparison:

1. Set *DIAG_COMP_CTRL3[COMP_ADC_SEL2:0]* = cell voltage measurement check (that is, 0b001) and set *[COMP_ADC_GO]* = 1.
2. For each channel enabled by *[AUX_CELL_SEL4:0]*, the device will compare $\text{abs}[(\text{VCELL} - \text{AUXCELL})] < [\text{VCCB_THR4:0}]$.
3. Wait for the comparison to be accomplished, roughly $[(\text{number of channel}) * (\text{AUXCELL settling time} + \text{one round robin cycle time})]$.
4. The cell voltage measurement comparison is completed when *ADC_STAT2[DRDY_VCCB]* = 1.

Host checks the *FAULT_COMP_VCCB2* register for the comparison result.

ADC comparison abort conditions:

The device will not start the cell voltage measurement comparison under the invalid conditions listed below. When the comparison is aborted, the *FAULT_COMP_MISC[COMP_ADC_ABORT]* = 1, *[DRDY_AUXCEL]* = 1, *[DRDY_VCCB]* = 1, and *FAULT_COMP_VCCB2* register = 0xFF. If *[AUX_CELL_SEL4:0]* is set to locked at a single channel, the *AUX_CELL_HI/LO* registers will be reset to default value 0x8000 if the comparison run is aborted.

Invalid conditions or settings which will prevent the start of the cell voltage measurement comparison:

- Invalid *[AUX_CELL_SEL]* setting: results in no AUX ADC measurement on the selected channel. The *AUX_CELL_HI/LO* registers are kept in default value.
- Channel higher than the *NUM_CELL* configuration is selected.
- Main or AUX ADCs are off or not set in continuous mode.

Post-ADC digital LPF check:

The digital LPF is checked continuous whenever the Main ADC is running. A duplicate diagnostic LPF is implemented to check against each LPF for each VC channel. The check is performed with one LPF at a time.

Example, to test LPF1 for cell channel 1, the input (that is, ADC measurement result from cell 1) is fed to the LPF1 and the diagnostic LPF for a period of time. The output of the LPF1 and the diagnostic LPF are compared against each other. Several outputs from LPF1 and diagnostic LPF will be compared to ensure the operation of the LPF1 before moving to check the next LPF. If any of the LPFs fail the diagnostic check, *FAULT_COMP_MISC[LPF_FAIL]* = 1.

When the LPF for each active cell channels is tested once, *ADC_STAT2[DRDY_LPF]* = 1. This diagnostic check of the LPFs will continuously run in the background as long as the Main ADC is running.

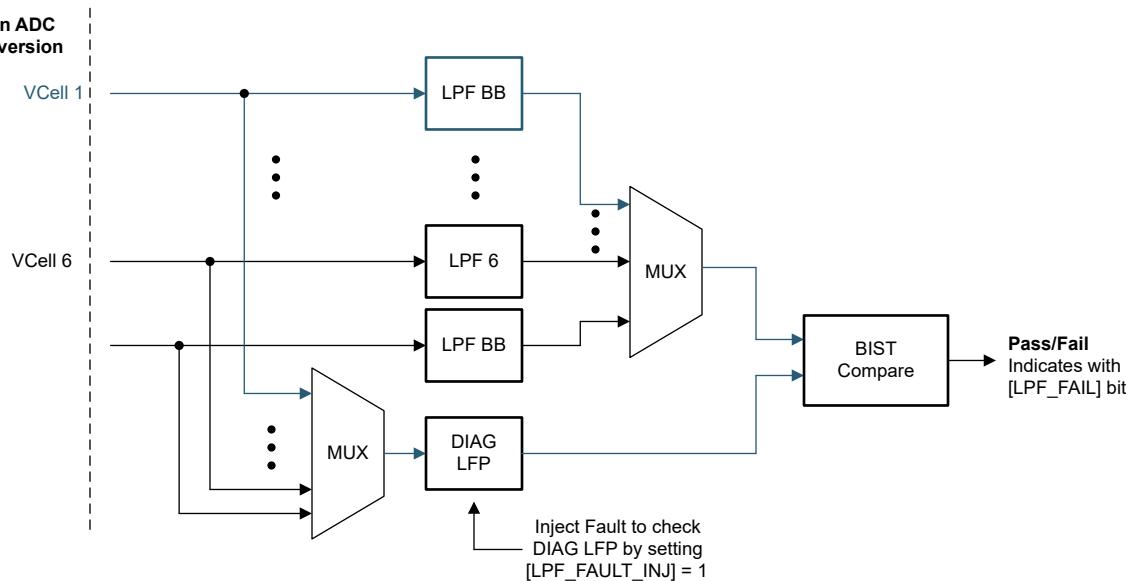


图 8-32. Post-ADC LPF Diagnostic (Blue Path as Example of Checking LPF1)

Furthermore, the device also implements a check to verify the functionality of the diagnostic LPF itself. By setting `DIAG_COMP_CTRL4[LPF_FAULT_INJ] = 1` and restarting the Main ADC, the device will inject a fault into the diagnostic LPF, forcing a failure during the LPF diagnostic check which then sets the `[LPF_FAIL] = 1`. When the test is completed, simply set the `[LPF_FAULT_INJ] = 0`.

8.3.6.4.6.2 Temperature Measurement Check

Similar to the cell voltage measurement check, the device checks the thermistor temperature measurement by comparing the Main ADC measurement to the AUX ADC measurement. To read the compared value measured by Main ADC and AUX ADC, MCU has lock on a single channel using `[AUX_GPIO_SEL]` setting and the start this diagnostic check. In this configuration, the compared values from Main ADC and AUX ADC are reported to `DIAG_MAIN_HI/LO` registers and `DIAG_AUX_HI/LO` registers respectively.

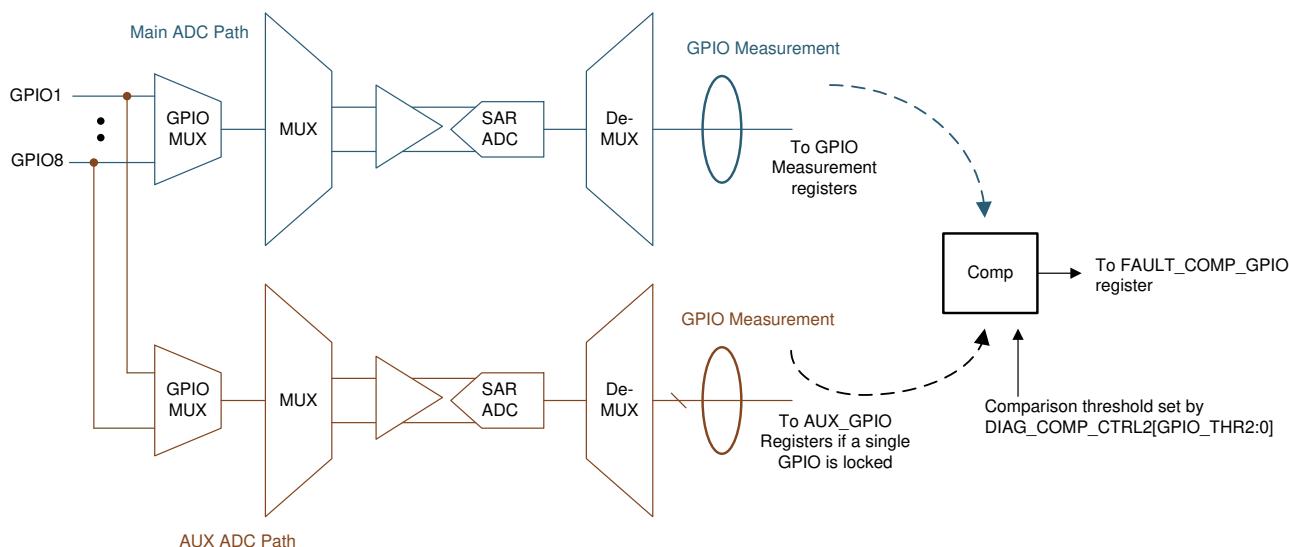


图 8-33. Thermistor Temperature (GPIO) Measurement Diagnostic

Before starting the temperature measurement comparison, host ensures:

- Main ADC must be enabled and is in continuous mode.
- The desired GPIO channels to be tested are configured in the *ADC_CTRL3[AUX_GPIO_SEL3:0]* setting and AUX ADC is enabled and in continuous mode.
- Select the comparison threshold through *DIAG_COMP_CTRL2[GPIO_THR2:0]* setting.

To start the temperature measurement comparison:

1. Set *DIAG_COMP_CTRL3[COMP_ADC_SEL2:0]* = GPIO measurement check (that is, 0b101) and set *[COMP_ADC_GO]* = 1.
2. For each channel enabled by *[AUX_GPIO_SEL4:0]*, the device will compare $\text{abs}[(\text{GPIO from Main} - \text{GPIO from AUX})] < [\text{GPIO_THR2:0}]$.
3. Wait for the comparison to be accomplished which can take up to 64 ADC round robin times.
4. The GPIO measurement comparison is completed when *ADC_STAT2/DRDY_GPIO* = 1.

Host checks the *FAULT_COMP_GPIO* register for the comparison result.

ADC comparison abort conditions:

The device will not start the temperature measurement comparison under the invalid conditions listed below. When the comparison is aborted, the *FAULT_COMP_MISC[COMP_ADC_ABORT]* = 1, *[DRDY_GPIO]* = 1, and *FAULT_COMP_GPIO* = 0xFF. If *[AUX_GPIO_SEL3:0]* is set to locked at a single channel, the *AUX_GPIO_HI/LO* registers will be reset to default value 0x8000 if the comparison run is aborted.

Invalid conditions or settings which will prevent the start of the temperature measurement comparison:

- Invalid `[AUX_GPIO_SEL]` setting which the selected GPIO isn't configured for ADC measurement. The `AUX_GPIO_HI/LO` registers are kept in default value. This also applies to the case if `[AUX_GPIO_SEL]` is selected for all GPIOs but none of the GPIOs are configured for ADC measurement.
- Main or AUX ADCs are off or not set in continuous mode.

8.3.6.4.6.3 Cell Balancing FETs Check

The cell balancing FET check is performed by turning on the balancing FET and comparing the voltage across the FET (through the AUX ADC path) versus the cell voltage (through the Main ADC path). To read the AUXCELL measurement used for the check, MCU has to set up this diagnostic check to lock on a single channel using `[AUX_CELL_SEL]` setting and the start this diagnostic check. The AUXCELL compared value will be reported to `DIAG_AUX_HI/LO` registers.

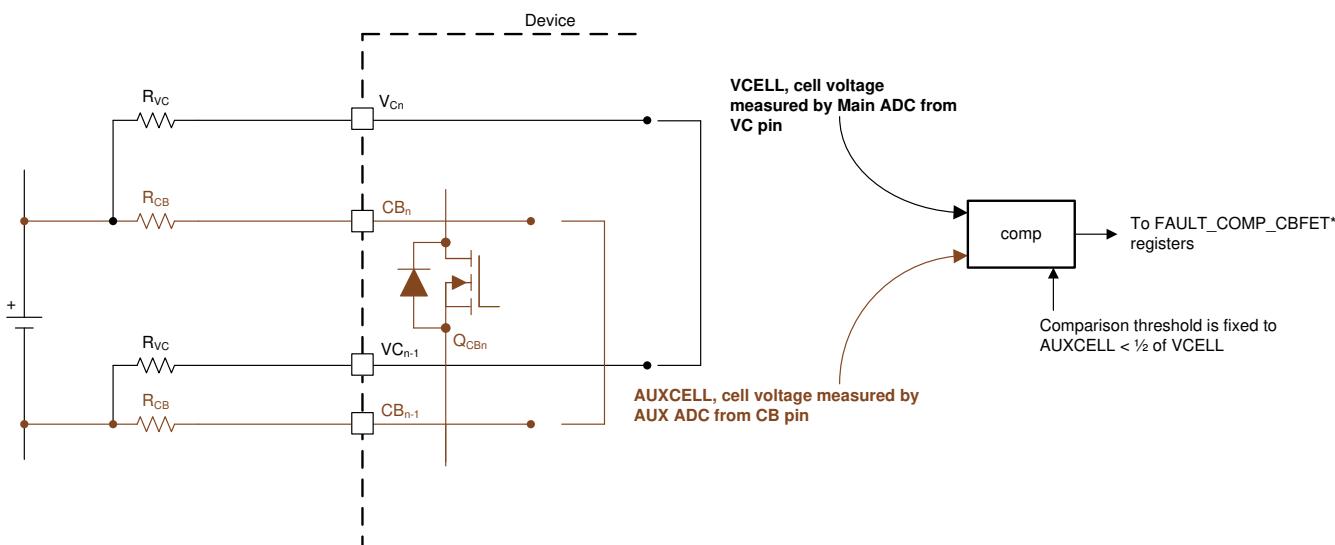


图 8-34. Cell Balancing FET Diagnostic

Before starting the cell balancing FET comparison, host ensures:

- Main ADC is running in continuous mode.
- Configured in the *ADC_CTRL2[AUX_CELL_SEL4:0]* to select the AUXCELL channels which the CB FETs are tested.
- Select the desired settling time for the AUX CELL channel through *ADC_CONF1[AUX_SETTLE1:0]*.
- Pause CB if balancing is running.
- Configured which CBFET to be tested through *DIAG_CBFET_CTRL2* register.
 - The rules of maximum of three CBFETs to be on and turn on no more than two consecutive CBFETs still apply.
 - Recommended to test in odd and even manner.

To start the CBFET comparison:

1. Start AUX ADC in continuous mode.
2. Turn on the selected CBFET by setting *DIAG_COMP_CTRL3[CBFET_CTRL_GO]* = 1 and wait for appropriate dv/dt time.
3. Set *DIAG_COMP_CTRL3[COMP_ADC_SEL2:0]* = CBFET check (that is, 0b100) and set *[COMP_ADC_GO]* = 1.
4. The device turns on the CBFET configured in the above step and compares the AUXCELL measurement (through CB channel) < half of the VCELL measurement (through VC channel). Only the CBFETs that are enabled are checked.
5. The CBFET comparison is completed when *ADC_STAT2[DRDY_CBFET]* = 1.
6. Repeat this procedure for other set of CBFET test. To turn off the CBFET enabled for this test, MCU clear the *DIAG_CBFET1* and *DIAG_CBFET2* registers then set the *[CBFET_CTRL_GO]* = 1. Otherwise, exiting from the CB pause state by sending *[CB_PAUSE]* = 0 will resume the regular balancing which turns off the CBFETs enabled for this test and resume on the CBFETs that are set for balancing.

Host checks the *FAULT_COMP_CBFET1* and *FAULT_COMP_CBFET2* registers for the comparison result. Repeat the steps to compare the remaining CBFETs.

ADC comparison abort conditions:

The device will not start the CBFET comparison under the invalid conditions listed below. When the comparison is aborted, the *FAULT_COMP_MISC[COMP_ADC_ABORT]* = 1, *[DRDY_AUX_CEL]* = 1, *[DRDY_CBFET]* = 1, and *FAULT_COMP_CBFET1/2* = 0xFF. If *[AUX_CELL_SEL4:0]* is set to locked at a single channel, the *AUX_CELL_HI/LO* registers will be reset to default value 0x8000 if the comparison run is aborted.

Invalid conditions or settings which will prevent the start of the cell voltage measurement comparison:

- Invalid *[AUX_CELL_SEL]* setting which results in no AUX ADC measurement on the selected channel. The *AUX_CELL_HI/LO* registers are kept in default value.
- Channel higher than the *NUM_CELL* configuration is selected.
- Main or AUX ADCs are off or not set in continuous mode.
- CB is running and it is not in pause mode.
- More than eight CBFETs are enabled, or more than two consecutive CBFETs are enabled in *DIAG_CBFET_CTRL1/2* registers.

8.3.6.4 VC and CB Open Wire Check

The device can detect an open wire connection on the VC and CB pins. A current sink is connected to each VC and CB pin, except VC0 and CB0 pins which are connected with a current source.

When the current sink (or current source) is enabled and if there is an open wire connection, the external differential capacitor will be depleted and the cell voltage measurement will drop to an abnormal level over time. Similar detection concept applies to the VC0 and CB0 pins with a current source. If there is an open wire connection, the VC0 or CB0 will be pulled up by the current source, resulting in a reduced cell voltage measurement over time.

When the diagnostic comparison is enabled, the device will compare the cell voltage measurement from Main ADC (for VC pins open wire detection) against a host-programmed threshold; or comparing the AUX CELL measurement from the AUX ADC (for CB pins open wire detection) against a host-programmed threshold.

If MCU lock to a single CB channel though *[AUX_CELL_SEL]* before starting the CB open wire check. The device will report the AUXCELL measurement used for the check comparison. The value is reported in *DIAG_AUX_HI/LO* registers. Since there is no single channel lock mechanism in Main ADC, VC channel measurement used for VC open wire will not be reported in *DIAG_MAIN_HI/LO* registers.

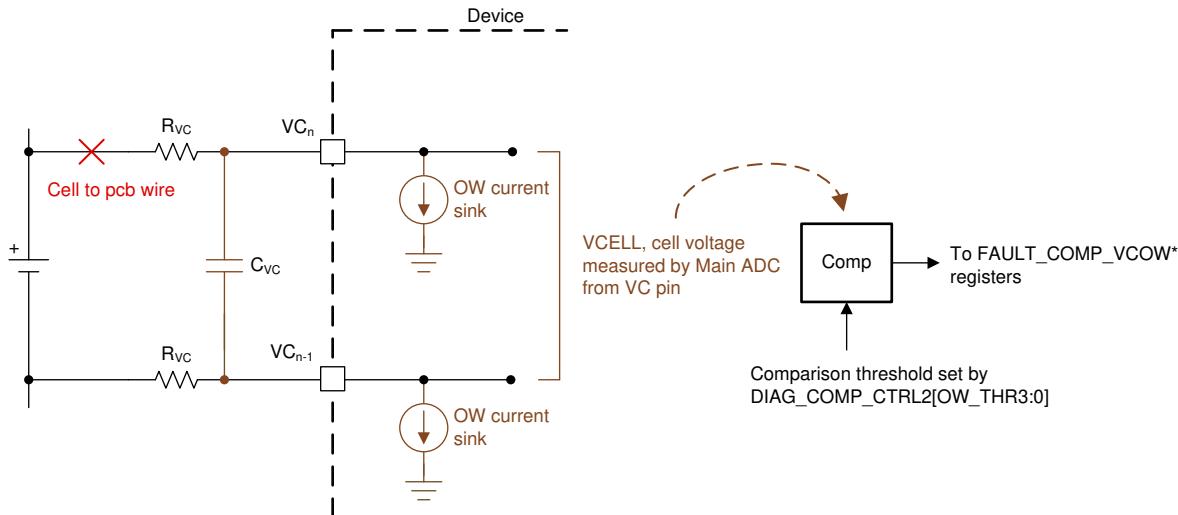


图 8-35. Open Wire Detection

Before starting the open wire comparison, host ensures:

- For VC open wire detection, Main ADC is running in continuous mode.
- For CB open wire detection, AUX ADC is running in continuous mode
 - Configured in the *ADC_CTRL2[AUX_CELL_SEL4:0]* to select the AUXCELL channels
 - Select the desired settling time for the AUX CELL channel through *ADC_CONF1[AUX_SETTLE1:0]*.
- Configure the open wire detection threshold through *DIAG_COMP_CTRL2[OW_THR3:0]*.

To start the open wire comparison:

1. Turn on the VC pins (or CB pins) current sink or source through *DIAG_COMP_CTRL3[OW_SNK1:0]*.
2. Wait for dV/dt time of the external capacitor to deplete to the detection threshold if there is an open wire fault.
3. For VC open wire detection, select *DIAG_COMP_CTRL3[COMP_ADC_SEL2:0]* = OW VC check (that is, 0b010) and set *[COMP_ADC_GO]* = 1. Or for CB open wire detection, *[COMP_ADC_SEL2:0]* = OW CB check (that is, 0b011).
4. The device compares all active VCELL measurement (for VC open wire) or AUX CELL measurement (for CB open wire) against the *[OW_THR3:0]* threshold setting.
5. When the comparison is completed, *ADC_STAT2[DRDY_VCOW]* = 1 for VC open wire (or *[DRDY_CBOW]* = 1 for CB open wire).
6. Host then turns off all current sinks and sources through *DIAG_COMP_CTRL3[OW_SNK1:0]*.

Host checks the *FAULT_COMP_VCOW2* register or the *FAULT_COMP_CBOW2* register for the comparison result.

8.4 Device Functional Modes

The device has three power modes plus an POR state.

- POR: This is not a power mode. This is a condition in which the voltage at the BAT pin is less than VBAT min, and all circuits including the AVAO_REF block in the device are powered off.
- SHUTDOWN: This is the lowest power mode. AVDD, DVDD and CVDD supplies are off. Only a gross regulation at LDOIN pin is maintained. CVDD pin will have a similar voltage as the LDOIN pin through internal circuit in order to support WAKE detection.
- SLEEP: This is the low power operation mode. Only limited functions are available.
- ACTIVE: This is the full power operation mode. All functions are supported under this state.

The various functions supported under different power modes are summarized in 表 8-26 and the power state diagram is shown in 图 8-36.

表 8-26. Active Functions Summary

| Functional Block | SHUTDOWN | SLEEP | ACTIVE | POR |
|---|----------|------------------|--------|---|
| Main ADC and CS ADC | | | ✓ | This is not a power state. All circuits are off. A sufficient voltage on VBAT will POR the device and put it to SHUTDOWN mode |
| AUX ADC | | | ✓ | |
| OV/UV protector | | ✓ ⁽¹⁾ | ✓ | |
| OT/UT protector | | ✓ ⁽¹⁾ | ✓ | |
| Cell Balancing | | ✓ ⁽¹⁾ | ✓ | |
| OTCB Detection | | ✓ ⁽¹⁾ | ✓ | |
| UART | | | ✓ | |
| Comm Vertical Communication | | | ✓ | |
| Fault Status and NFAULT Communication | | ✓ | ✓ | |
| Comm timeout | | | ✓ | |
| SLEEP timeout | | ✓ | | |
| Thermal Shutdown Detection | | ✓ | ✓ | |
| SPI Controller | | | ✓ | |
| OTP programming | | | ✓ | |
| Always-on block to detect POR of the device | ✓ | ✓ | ✓ | |

(1) To enable cell balancing, OV/UV or OT/UT protector(s) in SLEEP mode, host must enable the function(s) in ACTIVE mode first, then put the device to SLEEP.

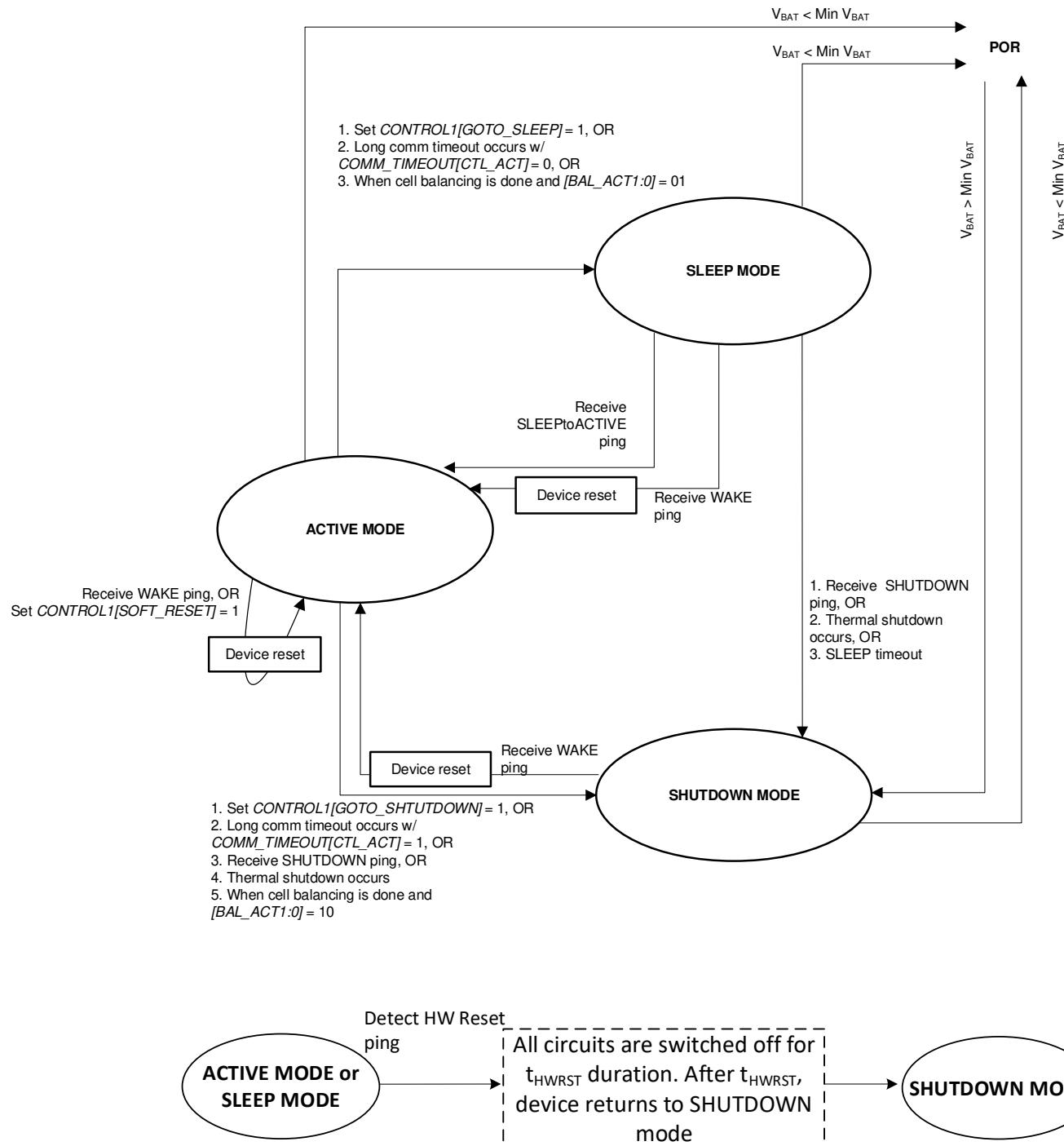


图 8-36. Power State Diagram

8.4.1 Power Modes

8.4.1.1 SHUTDOWN Mode

This is the lowest power mode. In SHUTDOWN mode, most of the functions are off. The device remains idle to simply monitor the WAKE ping (see [节 8.4.3](#) for details) to wake up from this state. Only a gross regulation on LDOIN and CVDD pins are maintained for WAKE ping detection.

8.4.1.1.1 Exit SHUTDOWN Mode

Communication is not supported in SHUTDOWN mode, host must send a WAKE ping to enter ACTIVE mode. Once device transitions from SHUTDOWN mode to ACTIVE mode, the following table indicates the expected fault bits being set under such transition has occurred.

表 8-27. Expected Fault Bit After Device Wake From SHUTDOWN

| Expected fault bits after waking up from SHUTDOWN | |
|---|--------------------------------|
| <i>FAULT_SYS[DRST]</i> = 1 | Digital reset by the wake ping |
| <i>FAULT_COMM1[COMMCLR_DET]</i> = 1 | UART engine is reset |

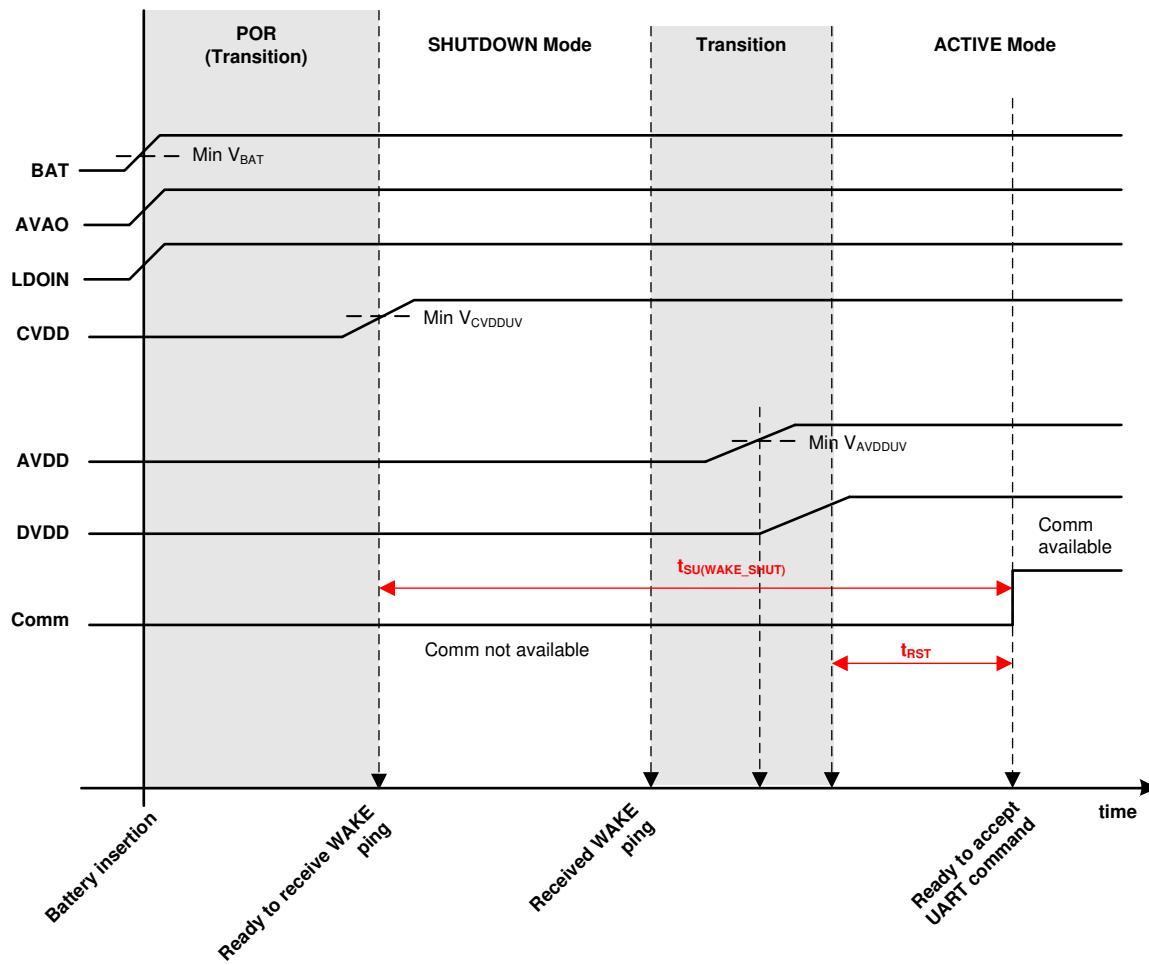


图 8-37. SHUTDOWN to ACTIVE Mode Transition

8.4.1.1.2 Enter SHUTDOWN Mode

During normal operation, host puts the device in SHUTDOWN mode through communication by sending *CONTROL1[GOTO_SHUTDOWN]* = 1.

The device can also enter SHUTDOWN mode by one of the following conditions:

- Communication timeout: automatically transitions from ACTIVE mode to SHUTDOWN mode if there is no valid communication for the configured time. Host can enable this option through the *COMM_TIMEOUT_CONF* register.

- SLEEP mode timeout: automatically transitions from SLEEP mode to SHUTDOWN mode if device is in SLEEP mode for the configured time. Host can enable this option through `PWR_TRANSIT_CONF[SLP_TIME2:0]`.
- Upon balancing completion: automatically enter SHUTDOWN mode when all balancing of the devices is completed. See [节 8.3.3](#) for details.
- Thermal shutdown: shuts down the device when the internal die temperature is greater than T_{SHUT}
- SHUTDOWN or HW_RESET ping: These pings are used as a recovery attempt on a loss communication situation. A SHUTDOWN ping puts the device into SHUTDOWN mode without using communication, forcing most of the circuits to be off. A more aggressive recovery attempt uses HW_RESET ping which turns off all circuits except a bandgap and restarts the device in SHUTDOWN mode.

8.4.1.2 SLEEP Mode

This is the low power operation mode. In SLEEP mode, all internal power supplies are still on, but functions are limited to cell balancing, OVUV and OTUT protectors.

8.4.1.2.1 Exit SLEEP Mode

Because host cannot communicate to the device, to exit SLEEP mode, host must send either a WAKE ping or SLEEPtoACTIVE ping to transition to ACTIVE mode. A WAKE wakes up and resets the device, which host will need to reconfigure the device setting; a SLEEPtoACTIVE only wakes up the device.

8.4.1.2.2 Enter SLEEP Mode

The device can enter SLEEP mode from ACTIVE mode only. During normal operation, host puts the device to SLEEP mode through communication by sending `CONTROL1[GOTO_SLEEP] = 1`.

The device can also enter SLEEP mode in the following condition:

- Communication timeout: automatically transitions from ACTIVE mode to SLEEP mode if there is no valid communication for the configured time. Host can enable this option through the `COMM_TIMEOUT_CONF` register.

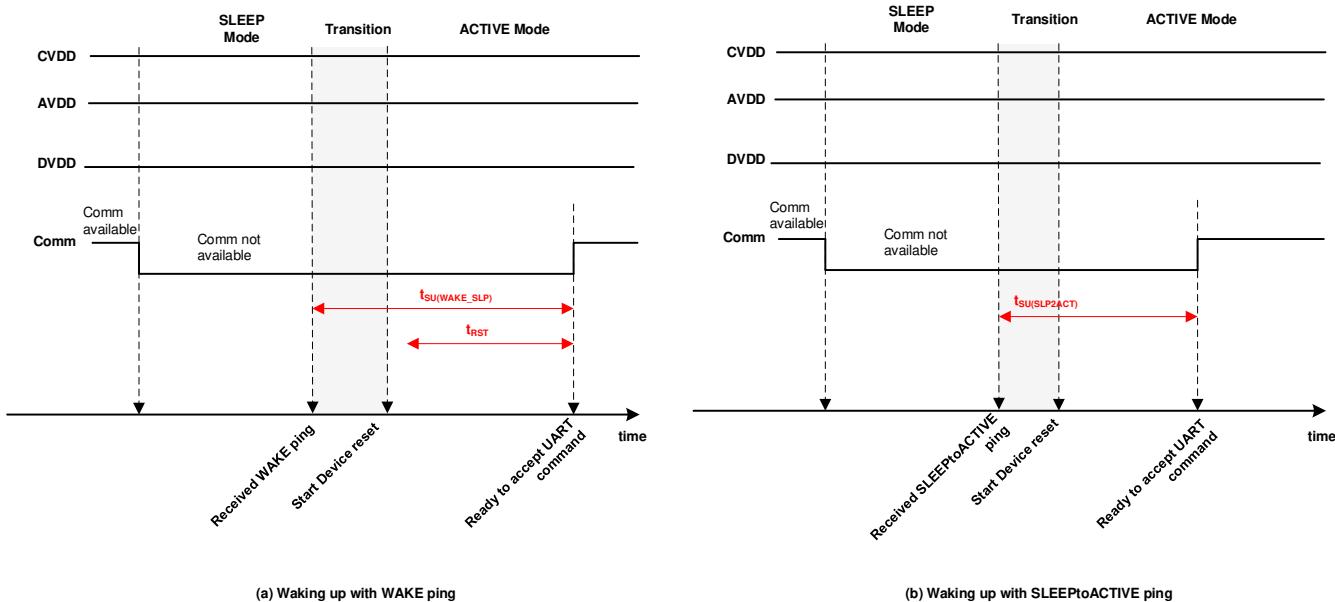


图 8-38. SLEEP to ACTIVE Mode Transition

8.4.1.3 ACTIVE Mode

This is the operation mode with full functionality support. Host can communicate to the device with full control on various features as well as performance diagnostic in this mode.

8.4.1.3.1 Exit ACTIVE Mode

From ACTIVE mode, device can enter SLEEP mode or SHUTDOWN mode through command, ping, timer, or specific event. See [节 8.4.1.1](#) and [节 8.4.1.2](#) for details.

8.4.1.3.2 Enter ACTIVE Mode From SHUTDOWN Mode

Device can transition to ACTIVE mode from SHUTDOWN mode only through a WAKE ping. Once in ACTIVE mode, host clears some of the reset-related faults which are expected faults (see [节 8.4.1.1](#) for details) indicating a POR on certain blocks due to the transition from SHUTDOWN mode to ACTIVE mode. Registers are reset to default; the OTP shadow registers are reloaded with the OTP programmed values.

8.4.1.3.3 Enter ACTIVE Mode From SLEEP Mode

From SLEEP mode, either a WAKE or SLEEPtoACTIVE ping can put the device in ACTIVE mode. A WAKE ping will generate a digital reset to the device. Because the LDO supplies remain on during SLEEP mode, only the $FAULT_{SYS}[DRST]$ = 1 is set, indicating a digital reset has occurred. Certain expected faults related to being reset are set. See SHUTDOWN mode for detail. Registers are reset to default, the OTP shadow registers are reloaded with the OTP programmed values.

If a SLEEPtoACTIVE ping is used to wake up the device from SLEEP mode to ACTIVE mode, device will simply enter ACTIVE mode without digital resetting but the UART engine will be reset. Hence, in the device, the $FAULT_{COMM1}[COMMCLR_DET]$ = 1 and host clears it after entering ACTIVE mode.

8.4.2 Device Reset

There are several conditions which the device will go through: a digital reset, putting the registers to their default settings and reloading the OTP.

- A WAKE ping is sent to transition from SHUTDOWN mode or SLEEP mode to ACTIVE mode.
- A WAKE ping is received in ACTIVE mode.
- The $CONTROL1[SOFT_RESET]$ = 1 command is sent in ACTIVE mode.
- A HW_RESET ping is sent under any power mode. This generates a POR-like event to the device. Upon the detection of a HW_RESET ping, the device will turn off all internal blocks except a bandgap for t_{HWRST} duration. Afterward, the device will restart in SHUTDOWN mode.
- Internal power supply faults. See [节 8.3.6.4](#) for details.
 - AVDD UV, DVDD UV is detected.
- A HFO or LFP watchdog fault will reset the digital.

Apart from the full reset cases, the following conditions will only reset the UART engine. In the device, the $FAULT_{COMM1}[COMMCLR_DET]$ = 1 will be set.

- A SLEEPtoACTIVE ping is sent to transition from SLEEP mode to ACTIVE mode.
- The following conditions not only clear the UART engine and set the $[COMMCLR_DET]$ = 1, they also set $FAULT_{COMM1}[STOP_DET]$ = 1 as an indication that an unexpected UART STOP is detected.
 - A SLEEPtoACTIVE ping is sent in ACTIVE mode.
 - A COMM CLEAR signal is sent. This is a dedicated signal to clear the UART engine and instruct the engine to look for a new start of communication frame. See [节 8.3.6.1.1.1](#) for more details.

8.4.3 Ping

In the noncommunicable conditions such as in SHUTDOWN or SLEEP mode, or in the loss of communication situations when host would like to instruct for a reset or power down as a communication recovery attempt, a Ping is used as a form of communication to the device for a specific action.

表 8-28. Supported Ping in Different Power Modes

| Ping Detection | Detected Pin(s) | SHUTDOWN | SLEEP | ACTIVE |
|--------------------|-----------------|----------|-------|--------|
| SHUTDOWN ping | RX | | ✓ | ✓ |
| SLEEPtoACTIVE ping | RX | | ✓ | ✓ |
| WAKE ping | RX | ✓ | ✓ | ✓ |

表 8-28. Supported Ping in Different Power Modes (续)

| Ping Detection | Detected Pin(s) | SHUTDOWN | SLEEP | ACTIVE |
|----------------|-----------------|----------|-------|--------|
| HW_RESET ping | RX | | ✓ | ✓ |

8.4.3.1 Ping

A ping is a specific high-low-high signal to the RX pin of the device. The device detects different low times of the ping signal to differentiate the different ping signals.

The communication pings are referring to the WAKE ping, SLEEPtoACTIVE ping, SHUTDOWN ping, and HW_RESET ping. These pings instruct the device to a specific power mode when normal communication is not available. By definition, a COMM CLEAR signal on the RX pin is a form of a ping. Because a COMM_CLR is to clear the UART engine, this signal is covered in [节 8.3.6.1.1.1](#).

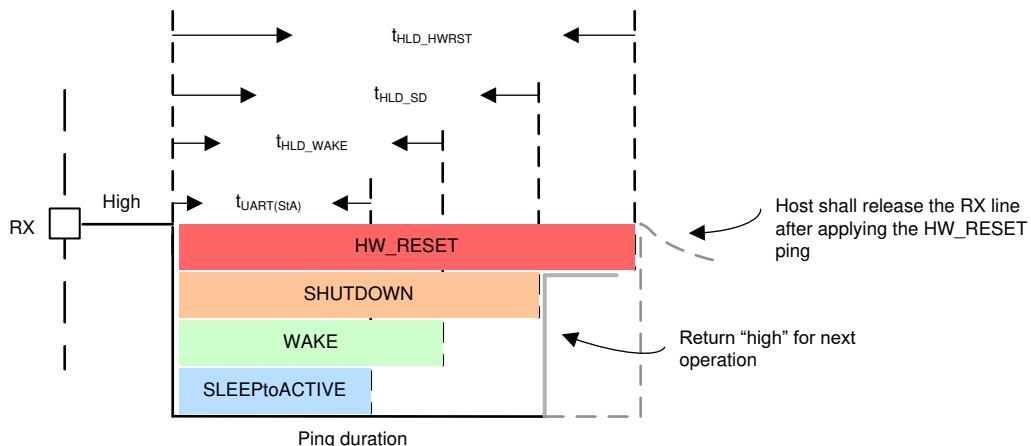


图 8-39. Communication Pings

8.5 Register Maps

This section has three register map summary tables with registers listed per the order of the register address:

- The NVM (OTP) shadow registers. These read/write-able shadow registers are reset with OTP values programmed in the customer OTP space. To program the custom OTP space, host writes the desired values to these OTP shadow registers and follows the programming procedure. These registers are included in the OTP CRC check. If customer OTP space is not programmed. The shadow registers are loaded with factory configuration default value. If the OTP (either factory configuration default or value programmed in customer OTP space) is failing to load after a device reset, the shadow registers will be loaded with the hardware reset default value instead. The hardware reset default value and the factory configuration default values are the same for the majority of the OTP shadow registers. Only the *DIR0_ADDR OTP*, *DIR1_ADD OTP*, *PWR_TRANSIT_CONF*, *CUST_CRC_HI/LO* registers have a reset value versus factory default, and are specified in [节 8.5.1](#) and their register field descriptions.
- The Read/Write registers. These are registers that the host can read/write to during runtime. A device reset will put these registers back to their reset value.
- The Read registers. These are registers that the host only has read access. A device reset will put these registers back to their reset value.

The register summary tables use the following key:

- Addr = Register address
- Hex = Hexadecimal value
- NVM = Non-volatile memory (OTP) shadow registers
- RSVD = Reserved. Reserved register addresses or bits are not implemented in the device. Any write to these bits is ignored. Reads to these bits always return 0.
- REG_INT_RSVD = Reserved register or bits for internal device usage. Host must have write to this register, other it may interrupt normal operation. Value display in this register shall be ignored.
- OTP_SPARE: These are spare OTP and shadow register bits that are implemented in the device. These spare bits are included as part of the CRC calculation. These bits are read/write as normal, but do not perform any function or influence any device behaviors.
- OTP_RSVDn = OTP and shadowed registers that are implemented but are reserved for device internal usage, where n refers to the register address. MCU must keep these registers in their default value
- HW Reset default is the value loaded when digital resets (POR like event) whereas Factory Configuration Default is the default value loaded into the OTP cell if customer doesn't program it themselves. Customer cannot read the HW Reset value.

[节 8.5.4](#) describes the definition of each bit in the registers. The registers in this section are grouped per functional blocks.

8.5.1 OTP Shadow Register Summary

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | |
|----------------------|----------|---------|---|-------------------------|------|------|------|------|------|------|------|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| <i>DIR0_ADDR OTP</i> | 0 | NVM | HW Reset Default = 0x00 Factory Configuration Default = 0x01 | SPARE[1:0] ADDRESS[5:0] | | | | | | | |
| <i>DIR1_ADDR OTP</i> | 1 | NVM | HW Reset Default = 0x00 Factory Configuration Default = 0x01 | SPARE[1:0] ADDRESS[5:0] | | | | | | | |

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | | | | | | | | | | | |
|---------------|----------|---------|--|--|--------------|--------------|-------------|----------------|---------------|---------------|-----------|--|--|--|--|--|--|--|--|--|--|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | | | | | | | | | |
| DEV_CONF | 2 | NVM | 0x54 | RSVD | NO_ADJ_CB | RSVD | FCOMM_EN | TWO_STOP_EN | NFAULT_EN | FTONE_EN_RSVD | RSVD | | | | | | | | | | |
| ACTIVE_CE_LL | 3 | NVM | HW Reset Default = 0x00 Factory Configuration Default = 0x00 | SPARE[3:0] | | | | | NUM_CELL[3:0] | | | | | | | | | | | | |
| OTP_SPARE_15 | 4 | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | |
| OTP_RSVD_5 | 5 | NVM | 0x00 | INTERNAL USE. DO NOT WRITE TO THIS ADDRESS | | | | | | | | | | | | | | | | | |
| OTP_RSVD_6 | 6 | NVM | 0x00 | INTERNAL USE. DO NOT WRITE TO THIS ADDRESS | | | | | | | | | | | | | | | | | |
| ADC_CONF_1 | 7 | NVM | 0x00 | AUX_SETTLE[1:0] | LPF_SR[2:0] | | | LPF_VCELL[2:0] | | | | | | | | | | | | | |
| ADC_CONF_2 | 8 | NVM | 0x00 | SPARE[1:0] | ADC_DLY[5:0] | | | | | | | | | | | | | | | | |
| OV_THRESH | 9 | NVM | 0x3F | SPARE | SPARE | OV_THR[5:0] | | | | | | | | | | | | | | | |
| UV_THRESH | A | NVM | 0x00 | SPARE | SPARE | UV_THR[5:0] | | | | | | | | | | | | | | | |
| OTUT_THRESH | B | NVM | 0xE0 | UT_THR[2:0] | | | OT_THR[4:0] | | | | | | | | | | | | | | |
| RSVD | C | NVM | 0x00 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | | | | | | | | | | |
| UV_DISABLE | D | NVM | 0x00 | RSVD | RSVD | CELL6 | CELL5 | CELL4 | CELL3 | CELL2 | CELL1 | | | | | | | | | | |
| GPIO_CONF_1 | E | NVM | 0x00 | FAULT_IN_EN | SPI_EN | GPIO2[2:0] | | | GPIO1[2:0] | | | | | | | | | | | | |
| GPIO_CONF_2 | F | NVM | 0x00 | SPARE | CS_DRDY | GPIO4[2:0] | | | GPIO3[2:0] | | | | | | | | | | | | |
| GPIO_CONF_3 | 10 | NVM | 0x00 | SPARE[1:0] | GPIO6[2:0] | | | GPIO5[2:0] | | | | | | | | | | | | | |
| GPIO_CONF_4 | 11 | NVM | 0x00 | SPARE[1:0] | GPIO8[2:0] | | | GPIO7[2:0] | | | | | | | | | | | | | |
| OTP_SPARE_14 | 12 | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | |
| OTP_SPARE_13 | 13 | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | |
| OTP_SPARE_12 | 14 | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | |
| OTP_SPARE_11 | 15 | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | |
| FAULT_MSK_1 | 16 | NVM | 0x00 | MSK_PROT | MSK_UT | MSK_OT | MSK_UV | MSK_OV | MSK_COMP | MSK_SYS | MSK_PWR | | | | | | | | | | |
| FAULT_MSK_2 | 17 | NVM | 0x00 | SPARE[1] | MSK OTP_CRC | MSK OTP DATA | SPARE | SPARE | SPARE | SPARE | MSK COMM1 | | | | | | | | | | |

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | | | | | | | | | | | | | |
|--|----------|---------|---|--|---------------|------|----------------|---------------|---------------|------|------|--|--|--|--|--|--|--|--|--|--|--|--|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | | | | | | | | | | | |
| PWR_TRAN_SIT_CONF | 18 | NVM | HW Reset Default = 0x18 Factory Configuration Default = 0x10 | SPARE[2:0] | | | TWARN_THR[1:0] | | SLP_TIME[2:0] | | | | | | | | | | | | | | |
| COMM_TIM_EOUT_CONF | 19 | NVM | 0x00 | SPARE | CTS_TIME[2:0] | | CTL_ACT | CTL_TIME[2:0] | | | | | | | | | | | | | | | |
| TX_HOLD_OFF | 1A | NVM | 0x00 | DLY[7:0] | | | | | | | | | | | | | | | | | | | |
| MAIN_ADC_CAL1 | 1B | NVM | 0x00 | GAINL[7:0] | | | | | | | | | | | | | | | | | | | |
| MAIN_ADC_CAL2 | 1C | NVM | 0x00 | GAINH | OFFSET[6:0] | | | | | | | | | | | | | | | | | | |
| AUX_ADC_CAL1 | 1D | NVM | 0x00 | GAINL[7:0] | | | | | | | | | | | | | | | | | | | |
| AUX_ADC_CAL2 | 1E | NVM | 0x00 | GAINH | OFFSET[6:0] | | | | | | | | | | | | | | | | | | |
| CS_ADC_CAL1 | 1F | NVM | 0x00 | GAINL[7:0] | | | | | | | | | | | | | | | | | | | |
| CS_ADC_CAL2 | 20 | NVM | 0x00 | GAINH[2:0] | | | OFFSET[4:0] | | | | | | | | | | | | | | | | |
| CUST_MISC 1 through CUST_MISC 8 | 21 | NVM | 0x00 | DATA[7:0] | | | | | | | | | | | | | | | | | | | |
| | 22 | NVM | 0x00 | DATA[7:0] | | | | | | | | | | | | | | | | | | | |
| | 23 | NVM | 0x00 | DATA[7:0] | | | | | | | | | | | | | | | | | | | |
| | 24 | NVM | 0x00 | DATA[7:0] | | | | | | | | | | | | | | | | | | | |
| | 25 | NVM | 0x00 | DATA[7:0] | | | | | | | | | | | | | | | | | | | |
| | 26 | NVM | 0x00 | DATA[7:0] | | | | | | | | | | | | | | | | | | | |
| | 27 | NVM | 0x00 | DATA[7:0] | | | | | | | | | | | | | | | | | | | |
| | 28 | NVM | 0x00 | DATA[7:0] | | | | | | | | | | | | | | | | | | | |
| OTP_RSVD_29 | 29 | NVM | 0x00 | INTERNAL USE. DO NOT WRITE TO THIS ADDRESS | | | | | | | | | | | | | | | | | | | |
| OTP_RSVD_2A | 2A | NVM | 0x00 | INTERNAL USE. DO NOT WRITE TO THIS ADDRESS | | | | | | | | | | | | | | | | | | | |
| OTP_RSVD_2B | 2B | NVM | 0x00 | INTERNAL USE. DO NOT WRITE TO THIS ADDRESS | | | | | | | | | | | | | | | | | | | |
| OTP_SPARE_10 | 2C | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | | | |
| OTP_SPARE_9 | 2D | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | | | |
| OTP_SPARE_8 | 2E | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | | | |
| OTP_SPARE_7 | 2F | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | | | |
| OTP_SPARE_6 | 30 | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | | | |
| OTP_SPARE_5 | 31 | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | | | |
| OTP_SPARE_4 | 32 | NVM | 0x00 | SPARE[7:0] | | | | | | | | | | | | | | | | | | | |

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | |
|---------------|----------|---------|--|------------|------|------|------|------|------|------|------|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| OTP_SPARE_3 | 33 | NVM | 0x00 | SPARE[7:0] | | | | | | | |
| OTP_SPARE_2 | 34 | NVM | 0x00 | SPARE[7:0] | | | | | | | |
| OTP_SPARE_1 | 35 | NVM | 0x00 | SPARE[7:0] | | | | | | | |
| CUST_CRC_HI | 36 | NVM | HW Reset Default = 0x57 Factory Configuration Default = 0x31 | CRC[7:0] | | | | | | | |
| CUST_CRC_LO | 37 | NVM | HW Reset Default = 0x89 Factory Configuration Default = 0xF3 | CRC[7:0] | | | | | | | |

8.5.2 Read/Write Register Summary

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | | | |
|--|----------|---------|-------------|--|-------------------|-----------------|-------------------|----------------|--------------|-------------------|----------------|--|--|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | |
| OTP_PROG_UNL OCK1A through OTP_PROG_UNL OCK1D | 300 | RW | 0x00 | | | | | | | | CODE[7:0] | | |
| | 301 | RW | 0x00 | | | | | | | | CODE[7:0] | | |
| | 302 | RW | 0x00 | | | | | | | | CODE[7:0] | | |
| | 303 | RW | 0x00 | | | | | | | | CODE[7:0] | | |
| DIR0_ADDR | 306 | RW | 0x00 | RSVD | | ADDRESS[5:0] | | | | | | | |
| DIR1_ADDR | 307 | RW | 0x00 | RSVD | | ADDRESS[5:0] | | | | | | | |
| COMM_CTRL | 308 | RW | 0x00 | RSVD | | | | | | | STACK_DEV_RSVD | | |
| CONTROL1 | 309 | RW | 0x00 | DIR_SEL | SEND_SHUT_DOWN | SEND_WAKE | SEND_SLPTO_ACT | GOTO_SHUT_DOWN | GOTO_SLEEP | SOFT_RESET | RSVD | | |
| CONTROL2 | 30A | RW | 0x00 | RSVD | | | | | | | RSVD | | |
| OTP_PROG_CTR_L | 30B | RW | 0x00 | RSVD | | | | | | | PAGE_SEL | | |
| ADC_CTRL1 | 30D | RW | 0x00 | RSVD | CS_DR[1:0] | | LPF_SR_EN | LPF_VCELL_EN | CS_MAIN_GO | CS_MAIN_MODE[1:0] | | | |
| ADC_CTRL2 | 30E | RW | 0x00 | RSVD | | AUX_CEL_L_ALIGN | AUX_CELL_SEL[4:0] | | | | | | |
| ADC_CTRL3 | 30F | RW | 0x00 | RSVD | AUX_GPIO_SEL[3:0] | | | | AUX_GO | AUX_MODE[1:0] | | | |
| REG_INT_RSVD | 310 | RW | 0x00 | INTERNAL USE. DO NOT WRITE TO THIS ADDRESS | | | | | | | | | |
| CB_CELL6_CTRL through CB_CELL1_CTRL | 322 | RW | 0x00 | RSVD | | | TIME[4:0] | | | | | | |
| | 323 | RW | 0x00 | RSVD | | | TIME[4:0] | | | | | | |
| | 324 | RW | 0x00 | RSVD | | | TIME[4:0] | | | | | | |
| | 325 | RW | 0x00 | RSVD | | | TIME[4:0] | | | | | | |
| | 326 | RW | 0x00 | RSVD | | | TIME[4:0] | | | | | | |
| | 327 | RW | 0x00 | RSVD | | | TIME[4:0] | | | | | | |
| VCB_DONE_THRESH | 32A | RW | 0x00 | RSVD | | CB_THR[5:0] | | | | | | | |
| OTCB_THRESH | 32B | RW | 0x0F | RSVD | COOLOFF[2:0] | | | OTCB_THR[3:0] | | | | | |
| OVUV_CTRL | 32C | RW | 0x00 | VCB_DONE_THRESH_LOCK | OVUV_LOCK[3:0] | | | | OVUV_GO | OVUV_MODE[1:0] | | | |
| OTUT_CTRL | 32D | RW | 0x00 | RSVD | OTCB_THR_LOCK | OTUT_LOCK[2:0] | | | OTUT_GO | OTUT_MODE[1:0] | | | |
| BAL_CTRL1 | 32E | RW | 0x00 | RSVD | | | | | | DUTY[2:0] | | | |
| BAL_CTRL2 | 32F | RW | 0x00 | RSVD | CB_PAUSE | FLTSTOP_EN | OTCB_EN | BAL_ACT[1:0] | | BAL_GO | AUTO_BAL | | |
| BAL_CTRL3 | 330 | RW | 0x00 | RSVD | | | BAL_TIME_SEL[3:0] | | | | BAL_TIME_GO | | |
| FAULT_RST1 | 331 | RW | 0x00 | RST_PROT | RST_UT | RST_OT | RST_UV | RST_OV | RST_COMP | RST_SYS | RST_PWR | | |
| FAULT_RST2 | 332 | RW | 0x00 | RSVD | RST OTP_CRC | RST OTP_DATA | REG_INT_RSVD | REG_INT_RSVD | REG_INT_RSVD | REG_INT_RSVD | RST_COMM1 | | |

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | | | | | | |
|--|----------|---------|-------------|--|---------------|-------------|---------------|-------------------|------------------|---------------|-------------|--|--|--|--|--|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | | | | |
| DIAG OTP_CTRL | 335 | RW | 0x00 | RSVD | | | FLIP_FACT_CRC | MARGIN_MODE[2:0] | | | MARGIN_GO | | | | | |
| DIAG_COMM_CTRL | 336 | RW | 0x00 | RSVD | | | RSVD | | | SPI_LOOPBACK | FLIP_TR_CRC | | | | | |
| DIAG_PWR_CTRL | 337 | RW | 0x00 | RSVD | | | RSVD | | | BIST_NO_RST | PWR_BIST_GO | | | | | |
| RSVD | 338 | RW | 0x00 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | | | | | |
| DIAG_CBFET_CTRL2 | 339 | RW | 0x00 | RSVD | RSVD | CBFET6 | CBFET5 | CBFET4 | CBFET3 | CBFET2 | CBFET1 | | | | | |
| DIAG_COMP_CTRL1 | 33A | RW | 0x00 | VCCB_THR[4:0] | | | | REG_INT_RSVD | | | | | | | | |
| DIAG_COMP_CTRL2 | 33B | RW | 0x00 | RSVD | GPIO_THR[2:0] | | | OW_THR[3:0] | | | | | | | | |
| DIAG_COMP_CTRL3 | 33C | RW | 0x00 | RSVD | CBFET_CTRL_GO | OW_SNK[1:0] | | COMP_ADC_SEL[2:0] | | | COMP_ADC_GO | | | | | |
| DIAG_COMP_CTRL4 | 33D | RW | 0x00 | RSVD | | | | | COMP_FAULT_INJ | LPF_FAULT_INJ | | | | | | |
| DIAG_PROT_CTR | 33E | RW | 0x00 | RSVD | | | | | PROT_BIST_NO_RST | | | | | | | |
| OTP_ECC_DATA1 N1 through OTP_ECC_DATA1 N9 | 343 | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| | 344 | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| | 345 | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| | 346 | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| | 347 | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| | 348 | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| | 349 | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| | 34A | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| | 34B | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| OTP_ECC_TEST | 34C | RW | 0x00 | RSVD | | | | DED_SEC | MANUAL_AUTO | ENC_DEC | ENABLE | | | | | |
| SPI_CONF | 34D | RW | 0x00 | RSVD | CPOL | CPHA | NUMBIT[4:0] | | | | | | | | | |
| SPI_TX3, SPI_TX2, and SPI_TX1 | 34E | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| | 34F | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| | 350 | RW | 0x00 | DATA[7:0] | | | | | | | | | | | | |
| SPI_EXE | 351 | RW | 0x02 | RSVD | | | | SS_CTRL | | SPI_GO | | | | | | |
| OTP_PROG_UNL OCK2A through OTP_PROG_UNL OCK2D | 352 | RW | 0x00 | CODE[7:0] | | | | | | | | | | | | |
| | 353 | RW | 0x00 | CODE[7:0] | | | | | | | | | | | | |
| | 354 | RW | 0x00 | CODE[7:0] | | | | | | | | | | | | |
| | 355 | RW | 0x00 | CODE[7:0] | | | | | | | | | | | | |
| REG_INT_RSVD | 700 | RW | 0x00 | INTERNAL USE. DO NOT WRITE TO THIS ADDRESS | | | | | | | | | | | | |
| REG_INT_RSVD | 701 | RW | 0x00 | INTERNAL USE. DO NOT WRITE TO THIS ADDRESS | | | | | | | | | | | | |
| REG_INT_RSVD | 702 | RW | 0x00 | INTERNAL USE. DO NOT WRITE TO THIS ADDRESS | | | | | | | | | | | | |

8.5.3 Read-Only Register Summary

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | |
|--|----------|---------|-------------|----------------|--------------|------------|-------------|---------------|----------------|----------------|---------------|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| PARTID | 500 | R | 0x00 | REV[7:0] | | | | | | | |
| DEV_REVID | E00 | R | 0x00 | DEV_REVID[7:0] | | | | | | | |
| DIE_ID1 through DIE_ID9 | 501 | R | 0x00 | ID[7:0] | | | | | | | |
| | 502 | R | 0x00 | ID[7:0] | | | | | | | |
| | 503 | R | 0x00 | ID[7:0] | | | | | | | |
| | 504 | R | 0x00 | ID[7:0] | | | | | | | |
| | 505 | R | 0x00 | ID[7:0] | | | | | | | |
| | 506 | R | 0x00 | ID[7:0] | | | | | | | |
| | 507 | R | 0x00 | ID[7:0] | | | | | | | |
| | 508 | R | 0x00 | ID[7:0] | | | | | | | |
| | 509 | R | 0x00 | ID[7:0] | | | | | | | |
| CUST_CRC_RSLT_HI | 50C | R | 0x31 | CRC[7:0] | | | | | | | |
| CUST_CRC_RSLT_LO | 50D | R | 0xF3 | CRC[7:0] | | | | | | | |
| OTP_ECC_DATA OUT1 through OTP_ECC_DATA OUT9 | 510 | R | 0x00 | DATA[7:0] | | | | | | | |
| | 511 | R | 0x00 | DATA[7:0] | | | | | | | |
| | 512 | R | 0x00 | DATA[7:0] | | | | | | | |
| | 513 | R | 0x00 | DATA[7:0] | | | | | | | |
| | 514 | R | 0x00 | DATA[7:0] | | | | | | | |
| | 515 | R | 0x00 | DATA[7:0] | | | | | | | |
| | 516 | R | 0x00 | DATA[7:0] | | | | | | | |
| | 517 | R | 0x00 | DATA[7:0] | | | | | | | |
| | 518 | R | 0x00 | DATA[7:0] | | | | | | | |
| OTP_PROG_STAT | 519 | R | 0x00 | UNLOCK | OTERR | UVERR | OVERR | SUVERR | SOVERR | PROG_ERR | DONE |
| OTP_CUST1_STAT | 51A | R | 0x00 | LOADED | LOAD WRN | LOAD ERR | FMTERR | PROGOK | UVOK | OVOK | TRY |
| OTP_CUST2_STAT | 51B | R | 0x00 | LOADED | LOAD WRN | LOAD ERR | FMTERR | PROGOK | UVOK | OVOK | TRY |
| SPI_RX3, SPI_RX2, and SPI_RX1 | 520 | R | 0x00 | DATA[7:0] | | | | | | | |
| | 521 | R | 0x00 | DATA[7:0] | | | | | | | |
| | 522 | R | 0x00 | DATA[7:0] | | | | | | | |
| DIAG_STAT | 526 | R | 0x00 | RSVD | | | DRDY_OTUT | DRDY_OVUV | DRDY_BIST_OTUT | DRDY_BIST_OVUV | DRDY_BIST_PWR |
| ADC_STAT1 | 527 | R | 0x00 | RSVD | | | DRDY_CS_ADC | DRDY_AUX_GPIO | DRDY_AUX_CELL | DRDY_AUX_MISC | DRDY_MAIN_ADC |
| ADC_STAT2 | 528 | R | 0x00 | RSVD | | DRDY_LPF | DRDY_GPIO | DRDY_VCOW | DRDY_CBOW | DRDY_CBFET | DRDY_VCCB |
| GPIO_STAT | 52A | R | 0x00 | GPIO8 | GPIO7 | GPIO6 | GPIO5 | GPIO4 | GPIO3 | GPIO2 | GPIO1 |
| BAL_STAT | 52B | R | 0x00 | INVALID_CBCONF | OT_PAUSE_DET | CB_INPAUSE | MB_RUN | CB_RUN | ABORT_FLT | MB_DONE | CB_DONE |

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | | |
|-------------------|----------|---------|-------------|------------|----------------|---------------|-------------|-------------|-------------|----------------|--------------|--|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| DEV_STAT | 52C | R | 0x00 | RSVD | FACT_CRC_DONE | CUST_CRC_DONE | OTUT_RUN | OVUV_RUN | CS_RUN | AUX_RUN | MAIN_RUN | |
| FAULT_SUMMARY | 52D | R | 0x00 | FAULT_PROT | FAULT_COMP_ADC | FAULT OTP | FAULT_COMM | FAULT_OTUT | FAULT_OVUV | FAULT_SYS | FAULT_PWR | |
| FAULT_COMM1 | 530 | R | 0x00 | RSVD | | | UART_TR | UART_RR | UART_RC | COMM_CLR_DET | STOP_DET | |
| FAULT OTP | 535 | R | 0x00 | RSVD | DED_DET | SEC_DET | CUST_CRC | FACT_CRC | CUSTLD_ERR | FACTLD_ERR | GBLOV_ERR | |
| FAULT_SYS | 536 | R | 0x00 | LFO | RSVD | GPIO | DRST | CTL | CTS | TSHUT | TWARN | |
| FAULT_PROT1 | 53A | R | 0x00 | RSVD | | | | | | TPARITY_FAIL | VPARITY_FAIL | |
| FAULT_PROT2 | 53B | R | 0x00 | RSVD | BIST_ABORT | TPATH_FAIL | VPATH_FAIL | UTCOMP_FAIL | OTCOMP_FAIL | OVCOMP_FAIL | UVCOMP_FAIL | |
| RSVD | 53C | R | 0x00 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | |
| FAULT_OV2 | 53D | R | 0x00 | RSVD | RSVD | OV6_DET | OV5_DET | OV4_DET | OV3_DET | OV2_DET | OV1_DET | |
| RSVD | 53E | R | 0x00 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | |
| FAULT_UV2 | 53F | R | 0x00 | RSVD | RSVD | UV6_DET | UV5_DET | UV4_DET | UV3_DET | UV2_DET | UV1_DET | |
| FAULT_OT | 540 | R | 0x00 | OT8_DET | OT7_DET | OT6_DET | OT5_DET | OT4_DET | OT3_DET | OT2_DET | OT1_DET | |
| FAULT_UT | 541 | R | 0x00 | UT8_DET | UT7_DET | UT6_DET | UT5_DET | UT4_DET | UT3_DET | UT2_DET | UT1_DET | |
| FAULT_COMP_GPIO | 543 | R | 0x00 | GPIO8_FAIL | GPIO7_FAIL | GPIO6_FAIL | GPIO5_FAIL | GPIO4_FAIL | GPIO3_FAIL | GPIO2_FAIL | GPIO1_FAIL | |
| RVSD | 545 | R | 0x00 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | |
| FAULT_COMP_V_CCB2 | 546 | R | 0x00 | RSVD | RSVD | CELL6_FAIL | CELL5_FAIL | CELL4_FAIL | CELL3_FAIL | CELL2_FAIL | CELL1_FAIL | |
| RSVD | 548 | R | 0x00 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | |
| FAULT_COMP_V_COW2 | 549 | R | 0x00 | RSVD | RSVD | VCOW6_FAIL | VCOW5_FAIL | VCOW4_FAIL | VCOW3_FAIL | VCOW2_FAIL | VCOW1_FAIL | |
| RSVD | 54B | R | 0x00 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | |
| FAULT_COMP_VBOW2 | 54C | R | 0x00 | RSVD | RSVD | CBOW6_FAIL | CBOW5_FAIL | CBOW4_FAIL | CBOW3_FAIL | CBOW2_FAIL | CBOW1_FAIL | |
| RSVD | 54E | R | 0x00 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | |
| FAULT_COMP_CBFET2 | 54F | R | 0x00 | RSVD | RSVD | CBFET6_FAIL | CBFET5_FAIL | CBFET4_FAIL | CBFET3_FAIL | CBFET2_FAIL | CBFET1_FAIL | |
| FAULT_COMP_MIMSC | 550 | R | 0x00 | RSVD | | | | | | COMP_ADC_ABORT | LPF_FAIL | |
| FAULT_PWR1 | 552 | R | 0x00 | CVSS_OPEN | DVSS_OPEN | REFHM_OPEN | CVDD_UV | CVDD_OV | DVDD_OV | AVDD_OSC | AVDD_OV | |
| FAULT_PWR2 | 553 | R | 0x00 | RSVD | PWRBIST_FAIL | RSVD | REFH_OSC | NEG5V_UV | TSREF_OSC | TSREF_UV | TSREF_OV | |
| FAULT_PWR3 | 554 | R | RSVD | RSVD | | | | | RSVD | RSVD | AVDDUV_DRST | |
| RSVD | 556 | R | 0x00 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | |
| CB_COMPLETE2 | 557 | R | 0x00 | RSVD | RSVD | CELL6_DONE | CELL5_DONE | CELL4_DONE | CELL3_DONE | CELL2_DONE | CELL1_DONE | |
| BAL_TIME | 558 | R | 0x00 | TIME_UNI | TIME[6:0] | | | | | | | |

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | |
|--------------------|----------|---------|-------------|------|------|------|------|------|------|------|-------------|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| RSVD | 568 | R | 0x80 | | | | | | | | RSVD |
| | 569 | R | 0x00 | | | | | | | | RSVD |
| RSVD | 56A | R | 0x80 | | | | | | | | RSVD |
| | 56B | R | 0x00 | | | | | | | | RSVD |
| RSVD | 56C | R | 0x80 | | | | | | | | RSVD |
| | 56D | R | 0x00 | | | | | | | | RSVD |
| RSVD | 56E | R | 0x80 | | | | | | | | RSVD |
| | 56F | R | 0x00 | | | | | | | | RSVD |
| RSVD | 570 | R | 0x80 | | | | | | | | RSVD |
| | 571 | R | 0x00 | | | | | | | | RSVD |
| RSVD | 572 | R | 0x80 | | | | | | | | RSVD |
| | 573 | R | 0x00 | | | | | | | | RSVD |
| RSVD | 574 | R | 0x80 | | | | | | | | RSVD |
| | 575 | R | 0x00 | | | | | | | | RSVD |
| RSVD | 576 | R | 0x80 | | | | | | | | RSVD |
| | 577 | R | 0x00 | | | | | | | | RSVD |
| RSVD | 578 | R | 0x80 | | | | | | | | RSVD |
| | 579 | R | 0x00 | | | | | | | | RSVD |
| RSVD | 57A | R | 0x80 | | | | | | | | RSVD |
| | 57B | R | 0x00 | | | | | | | | RSVD |
| VCELL6_HI/LO | 57C | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 57D | R | 0x00 | | | | | | | | RESULT[7:0] |
| VCELL5_HI/LO | 57E | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 57F | R | 0x00 | | | | | | | | RESULT[7:0] |
| VCELL4_HI/LO | 580 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 581 | R | 0x00 | | | | | | | | RESULT[7:0] |
| VCELL3_HI/LO | 582 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 583 | R | 0x00 | | | | | | | | RESULT[7:0] |
| VCELL2_HI/LO | 584 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 585 | R | 0x00 | | | | | | | | RESULT[7:0] |
| VCELL1_HI/LO | 586 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 587 | R | 0x00 | | | | | | | | RESULT[7:0] |
| MAIN_CURRENT_HI/LO | 588 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 589 | R | 0x00 | | | | | | | | RESULT[7:0] |
| TSREF_HI/LO | 58C | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 58D | R | 0x00 | | | | | | | | RESULT[7:0] |
| GPIO1_HI/LO | 58E | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 58F | R | 0x00 | | | | | | | | RESULT[7:0] |
| GPIO2_HI/LO | 590 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 591 | R | 0x00 | | | | | | | | RESULT[7:0] |
| GPIO3_HI/LO | 592 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 593 | R | 0x00 | | | | | | | | RESULT[7:0] |
| GPIO4_HI/LO | 594 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 595 | R | 0x00 | | | | | | | | RESULT[7:0] |

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | |
|-----------------------|----------|---------|-------------|------|------|------|------|------|------|------|-------------|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| GPIO5_HI/LO | 596 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 597 | R | 0x00 | | | | | | | | RESULT[7:0] |
| GPIO6_HI/LO | 598 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 599 | R | 0x00 | | | | | | | | RESULT[7:0] |
| GPIO7_HI/LO | 59A | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 59B | R | 0x00 | | | | | | | | RESULT[7:0] |
| GPIO8_HI/LO | 59C | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 59D | R | 0x00 | | | | | | | | RESULT[7:0] |
| DIETEMP1_HI/LO | 5AE | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5AF | R | 0x00 | | | | | | | | RESULT[7:0] |
| DIETEMP2_HI/LO | 5B0 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5B1 | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_CELL_HI/LO | 5B2 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5B3 | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_GPIO_HI/LO | 5B4 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5B5 | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_BAT_HI/LO | 5B6 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5B7 | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_REFI_HI/LO | 5B8 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5B9 | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_VBG2_HI/LO | 5BA | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5BB | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_AVAO_REF_HI/LO | 5BE | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5BF | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_AVDD_REF_HI/LO | 5C0 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5C1 | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_OV_DAC_HI/LO | 5C2 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5C3 | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_UV_DAC_HI/LO | 5C4 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5C5 | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_OT_OTCB_DAC_HI/LO | 5C6 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5C7 | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_UT_DAC_HI/LO | 5C8 | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5C9 | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_VCBDONE_DAC_HI/LO | 5CA | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5CB | R | 0x00 | | | | | | | | RESULT[7:0] |
| AUX_VCM_HI/LO | 5CC | R | 0x80 | | | | | | | | RESULT[7:0] |
| | 5CD | R | 0x00 | | | | | | | | RESULT[7:0] |
| REFOVDAC_HI/LO | 5D0 | R | 0x00 | | | | | | | | RESULT[7:0] |
| | 5D1 | R | 0x00 | | | | | | | | RESULT[7:0] |
| DIAG_MAIN_HI/LO | 5D2 | R | 0x00 | | | | | | | | RESULT[7:0] |
| | 5D3 | R | 0x00 | | | | | | | | RESULT[7:0] |
| DIAG_AUX_HI/LO | 5D4 | R | 0x00 | | | | | | | | RESULT[7:0] |
| | 5D5 | R | 0x00 | | | | | | | | RESULT[7:0] |

| Register Name | Addr Hex | RW Type | Reset Value | Data | | | | | | | |
|----------------------------|----------|---------|-------------|--|---------|----------|---------|-----------|-----------|--------|------|
| | | | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| CURRENT_HI/MI D/LO | 5D6 | R | 0x80 | RESULT[7:0] | | | | | | | |
| | 5D7 | R | 0x00 | RESULT[7:0] | | | | | | | |
| | 5D8 | R | 0x00 | RESULT[7:0] | | | | | | | |
| REG_INT_RSVD | 780 | R | 0x33 | INTERNAL USE. IGNORE VALUE FROM THIS ADDRESS | | | | | | | |
| DEBUG_UART_RC | 781 | R | 0x00 | RSVD | RC_IERR | RC_TXDIS | RC_SOF | RC_BYTERR | RC_UNEXP | RC_CRC | |
| DEBUG_UART_RR_TR | 782 | R | 0x00 | RSVD | | TR_SOF | TR_WAIT | RR_SOF | RR_BYTERR | RR_CRC | |
| DEBUG_UART_DI SCARD | 789 | R | 0x00 | COUNT[7:0] | | | | | | | |
| DEBUG_UART_V ALID_HI/LO | 78C | R | 0x00 | COUNT[7:0] | | | | | | | |
| | 78D | R | 0x00 | COUNT[7:0] | | | | | | | |
| DEBUG OTP_SE C_BLK | 7A0 | R | 0x00 | BLOCK[7:0] | | | | | | | |
| DEBUG OTP_DE D_BLK | 7A1 | R | 0x00 | BLOCK[7:0] | | | | | | | |

8.5.4 Register Field Descriptions

8.5.4.1 Device Addressing Setup

8.5.4.1.1 DIR0_ADDR OTP

| Address | 0x0000 | | | | | | | |
|--|------------|-------|-------|-------|-------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | SPARE[1:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SPARE[1:0] = Spare | | | | | | | | |
| ADDRESS[5:0] = This register shows the default device address used when [DIR_SEL] = 0 and programmed in the OTP. Writing to this register won't change the device address actively in use. The [DIR_SEL] setting has no impact on BQ756506-Q1 since it is a standalone device using UART communication to host system. This register is used for the system to program the device address to OTP, which will be loaded to the DIR0_ADDR register at POR. For programming, follow the OTP programming procedure. | | | | | | | | |

8.5.4.1.2 DIR1_ADDR OTP

| Address | 0x0001 | | | | | | | |
|--|------------|-------|-------|-------|-------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | SPARE[1:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SPARE[1:0] = Spare | | | | | | | | |
| ADDRESS[5:0] = This register shows the default device address used when [DIR_SEL] = 1 and programmed in the OTP. Writing to this register won't change the device address actively in use. The [DIR_SEL] setting has no impact on BQ756506-Q1 since it is a standalone device using UART communication to host system. This register is used for the system to program the device address to OTP, which will be loaded to the DIR1_ADDR register at POR. For programming, follow the OTP programming procedure. | | | | | | | | |

8.5.4.1.3 CUST_MISC1 through CUST_MISC8

| Address | 0x0021 to 0x0028 | | | | | | | |
|----------------------------------|------------------|-------|-------|-------|-------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | DATA[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DATA[7:0] = Customer scratch pad | | | | | | | | |

8.5.4.1.4 DIR0_ADDR

| Address | 0x0306 | | | | | | | |
|---|--------|-------|-------|-------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| ADDRESS[5:0] = Always shows the current device address used by the device when [DIR_SEL] = 0. At POR, this register is loaded from the device address value in the OTP (same OTP device address loaded to DIR0_ADDR OTP register). The [DIR_SEL] setting has no impact on BQ756506-Q1 since it is a standalone device using UART communication to host system. Host can re-address the device by writing a different device address to this register, and the device will take on the new address immediately. Note: CONTROL1[ADDR_WR] = 1 is required to write to this register. See 8.5.4.3.7 for details. | | | | | | | | |

8.5.4.1.5 DIR1_ADDR

| Address | 0x0307 | | | | | | | |
|---------|--------|-------|-------|-------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

| Name | RSVD | | ADDRESS[5:0] | | | | | |
|---|------|---|--------------|---|---|---|---|---|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| ADDRESS[5:0] = Always shows the current device address used by the device when <i>[DIR_SEL]</i> = 1. At POR, this register is loaded from the device address value in the OTP (same OTP device address loaded to <i>DIR1_ADDR OTP</i> register). The <i>[DIR_SEL]</i> setting has no impact on BQ756506-Q1 since it is a standalone device using UART communication to host system. Host can re-address the device by writing a different device address to this register, and the device will take on the new address immediately. | | | | | | | | |
| Note: <i>CONTROL1[ADDR_WR]</i> = 1 is required to write to this register. See 节 8.5.4.3.7 for details. | | | | | | | | |

8.5.4.2 Device ID and Scratch Pad

8.5.4.2.1 PARTID

| Address | 0x0500 | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | PARTID[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PARTID[7:0] Device Identification: = 0xA = BQ756506 All other codes = Reserved | | | | | | | | |

8.5.4.2.2 DEV_REVID

| Address | 0xE00 | | | | | | | |
|-----------|--|------|------|------|------|------|------|------|
| Read Only | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | A value of 0x00 indicates that the device is in normal operating mode. If a fault activates the Factory Testmode Detection, the value will be non-zero. Refer Safety Manual for details on SM426: Fact Testmode Detection. | | | | | | | |

8.5.4.2.3 DIE_ID1 through DIE_ID9

| Address | 0x0501 | | | | | | | |
|---|---------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | ID[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID[7:0] = Device Revision 0x10 = Revision A0 0x11 = Revision A1 0x20 = Revision B0 0x21 = Revision B1 0x22 = Revision B2 All other codes = Reserved | | | | | | | | |

| Address | 0x0502 to 0x0509 | | | | | | | |
|-------------------------------------|------------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | ID[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ID[7:0] = Die ID for TI factory use | | | | | | | | |

8.5.4.3 General Configuration and Control

8.5.4.3.1 DEV_CONF

| Address | 0x0002 | | | | | | | |
|---|--------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | NO_ADJ_CB | RSVD | FCOMM_EN | TWO_STOP_EN | NFAULT_EN | RSVD | RSVD |
| Reset | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| NO_ADJ_CB = Indicates the device will not allow an adjacent CB FET to be turned on in manual CB control. If MCU has enabled an adjacent CB FET, device will not start CB even if host sends <i>[BAL_GO]</i> = 1. 0 = Device will allow two adjacent CB FETs to be enabled. 1 = Device will not allow adjacent CB FET to be enabled. | | | | | | | | |
| RSVD = Reserved — The bit should leave as default in BQ756506-Q1 since it is a standalone device using UART communication to host system. | | | | | | | | |
| FCOMM_EN = Enables the fault state detection through communication in ACTIVE mode. 0 = Disable 1 = Enable | | | | | | | | |
| TWO_STOP_EN = Enables two stop bits for the UART in case of severe oscillator error in the host and device. 0 = One STOP bit 1 = Two STOP bits | | | | | | | | |
| NFAULT_EN = Enables the NFAULT function. 0 = NFAULT always pulled up 1 = NFAULT pulled low to indicate an unmasked fault is detected. Note: This bit setting does not affect the <i>FAULT_SUMMARY</i> register. | | | | | | | | |
| RSVD = Reserved — The bit has no significant impact in BQ756506-Q1 since it is a standalone device which a fault can directly trigger NFAULT pin. | | | | | | | | |
| RSVD = Reserved — The bit should leave as default in BQ756506-Q1 since it is a standalone device using UART communication to host system. | | | | | | | | |

8.5.4.3.2 ACTIVE_CELL

| Address | 0x0003 | | | | | | | |
|--|------------|--------------|--------------|--------------|---------------|--------------|--------------|--------------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | SPARE[3:0] | | | | NUM_CELL[3:0] | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Factory OTP Reset | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| SPARE[3:0] = Spare | | | | | | | | |
| NUM_CELL[3:0] = Configures the number of cells in series. 0x0 = 6S 0x1 = 6S 0x2 = 6S : 0xA = 6S Unused code defaults to <i>CHIP_TYPE[MAX_CH1:0]</i> setting (in factory trim). If the NUM_CELL setting has more channels than the device offers, it would be capped to highest number of channel the device offers. Note: The minimum number of active channels is 6. For applications with fewer than 6 series cells, the software should ignore faults on unused channels. These will not automatically be masked. Refer to NFAULT in the application section for more details. | | | | | | | | |

8.5.4.3.3 PWR_TRANSIT_CONF

| Address | 0x0018 | | | | | | | |
|---------|--------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

| Name | SPARE[2:0] | | | TWARN_THR[1:0] | | SLP_TIME[2:0] | | |
|--|------------|---|---|----------------|---|---------------|---|---|
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| Factory Configuration default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| SPARE[2:0] = Spare | | | | | | | | |
| TWARN_THR[1:0] = Sets the TWARN threshold. 00 = 85°C 01 = 95°C 10 = 105°C (default) 11 = 115°C | | | | | | | | |
| SLP_TIME[2:0] = A timeout in SLEEP mode. This timer starts counting when device enters SLEEP mode. When the timer expires, the device enters SHUTDOWN mode. The timer resets if device wakes up to ACTIVE mode. 000 = No timeout. Device remains in SLEEP mode (default at reset) 001 = 5 s 010 = 10 s 011 = 1 min 100 = 10 min 101 = 30 min 110 = 1 hour 111 = 2 hour | | | | | | | | |

8.5.4.3.4 COMM_TIMEOUT_CONF

| Address | 0x0019 | | | | | | | |
|--|--------|---------------|-------|-------|-------|---------|---------------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | SPARE | CTS_TIME[2:0] | | | | CTL_ACT | CTL_TIME[2:0] | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SPARE = Spare | | | | | | | | |
| CTS_TIME[2:0] = Sets the short communication timeout. When this timer expires, the device sets the <i>FAULT_SYS[CTL]</i> bit. This can be used as an alert to the system to prevent a long communication timeout. 000 = Disables short communication timeout (default at reset) 001 = 100 ms 010 = 2 s 011 = 10 s 100 = 1 min 101 = 10 min 110 = 30 min 111 = 1 hr | | | | | | | | |
| CTL_ACT = Configures the device action when long communication timeout timer expires. 0 = Sets <i>FAULT_SYS[CTL]</i> and sends device to SLEEP mode (default at reset) 1 = Sends the device to SHUTDOWN. <i>FAULT_SYS[CTL]</i> bit will not be set. | | | | | | | | |
| CTL_TIME[2:0] = Sets the long communication timeout. When this timer expires, the device takes the action configured by the <i>[CTL_ACT]</i> bit. 000 = Disables long communication timeout (default at reset) 001 = 100 ms 010 = 2 s 011 = 10 s 100 = 1 min 101 = 10 min 110 = 30 min 111 = 1 hr | | | | | | | | |

8.5.4.3.5 TX_HOLD_OFF

| Address | 0x001A | | | | | | | |
|---------|----------|-------|-------|-------|-------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | DLY[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| |
|---|
| DLY[7:0] = Sets the number of bit periods from 0 to 255 to delay after receiving the STOP bit of a command frame and before transmitting the 1st bit of response frame. |
|---|

8.5.4.3.6 COMM_CTRL

| Address | 0x0308 | | | | | | | |
|-----------------|--------|-------|-------|-------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |

8.5.4.3.7 CONTROL1

| Address | 0x0309 | | | | | | | |
|---|--------|-------|-------|-------|---------------|------------|------------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | GOTO_SHUTDOWN | GOTO_SLEEP | SOFT_RESET | RSVD |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved — The bit has no impact in BQ756506-Q1 since it is a standalone device which the host can send the ping signal directly | | | | | | | | |
| GOTO_SHUTDOWN = Transitions device to SHUTDOWN mode. Bit is cleared on read. 0 = Ready 1 = Enter SHUTDOWN mode | | | | | | | | |
| GOTO_SLEEP = Transitions device to SLEEP mode. Bit is cleared on read. 0 = Ready 1 = Enter SLEEP mode | | | | | | | | |
| SOFT_RESET = Resets the digital to OTP default. Bit is cleared on read. 0 = Ready 1 = Reset device | | | | | | | | |
| RSVD = Reserved | | | | | | | | |

8.5.4.3.8 CONTROL2

| Address | 0x030A | | | | | | | |
|---|--------|-------|-------|-------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved — The bit has no impact in BQ756506-Q1 since it is a standalone device which the host can send the ping signal directly | | | | | | | | |

8.5.4.3.9 CUST_CRC_HI

| Address | 0x0036 | | | | | | | |
|---|----------|-------|-------|-------|-------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | CRC[7:0] | | | | | | | |
| Reset | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| Factory Configuration Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| CRC[7:0] = High-byte of the host-calculated CRC for customer OTP space. | | | | | | | | |

8.5.4.3.10 CUST_CRC_LO

| Address | 0x0037 | | | | | | | |
|---------|--------|--|--|--|--|--|--|--|
| | | | | | | | | |

| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|----------|-------|-------|-------|-------|-------|-------|-------|
| Name | CRC[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| Factory Configuration Reset | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| CRC[7:0] = Low-byte of the host-calculated CRC for customer OTP space. | | | | | | | | |

8.5.4.3.11 CUST_CRC_RSLT_HI

| Address | 0x050C | | | | | | | |
|---|----------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | CRC[7:0] | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| CRC[7:0] = High-byte of the device-calculated CRC for customer OTP space. | | | | | | | | |

8.5.4.3.12 CUST_CRC_RSLT_LO

| Address | 0x050D | | | | | | | |
|--|----------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | CRC[7:0] | | | | | | | |
| Reset | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| CRC[7:0] = Low-byte of the device-calculated CRC for customer OTP space. | | | | | | | | |

8.5.4.4 Operation Status

8.5.4.4.1 DIAG_STAT

| Address | 0x0526 | | | | | | | |
|--|--------|-------|-------|-----------|-----------|----------------|----------------|---------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | DRDY_OTUT | DRDY_OVUV | DRDY_BIST_OTUT | DRDY_BIST_OVUV | DRDY_BIST_PWR |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| <p>DRDY_OTUT = Indicates the OTUT round robin has run at least once. This bit is cleared when [OTUT_GO] = 1 with [OTUT_MODE1:0] = 01 (start the OTUT round robin run) and set when at least 1 cycle of round robin is completed.</p> <p>0 = OTUT has not started or first round robin has not completed yet.</p> <p>1 = At least 1 cycle of round robin has completed.</p> | | | | | | | | |
| <p>DRDY_OVUV = Indicates the OVUV round robin has at least run once. This bit is cleared when [OVUV_GO] = 1 with [OVUV_MODE1:0] = 01 (start the OVUV round robin run) and set when at least 1 cycle of round robin is completed.</p> <p>0 = OVUV has not started or first round robin has not completed yet.</p> <p>1 = At least 1 cycle of round robin has completed.</p> | | | | | | | | |
| <p>DRDY_BIST_OTUT = Indicates the status of the OTUT protector diagnostic. This bit is cleared when [OTUT_GO] = 1 with [OTUT_MODE1:0] = 10 (start the BIST run) and set when the BIST cycle is completed.</p> <p>0 = Not started or still running.</p> <p>1 = BIST cycle completed.</p> | | | | | | | | |
| <p>DRDY_BIST_OVUV = Indicates the status of the OVUV protector diagnostic. This bit is cleared when [OVUV_GO] = 1 with [OVUV_MODE1:0] = 10 (start the BIST run) and set when the BIST cycle is completed.</p> <p>0 = Not started or still running.</p> <p>1 = BIST cycle completed.</p> | | | | | | | | |

DRDY_BIST_PWR = Indicates the status of the power supplies diagnostic. This bit is cleared when [PWR_BIST_GO] = 1 (start the BIST run) and set when the BIST cycle is completed.
 0 = Not started or still running.
 1 = BIST cycle completed.

8.5.4.4.2 ADC_STAT1

| Address | 0x0527 | | | | | | | |
|--|--------|-------|-------|-------------|---------------|---------------|---------------|---------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | DRDY_CS_ADC | DRDY_AUX_GPIO | DRDY_AUX_CELL | DRDY_AUX_MISC | DRDY_MAIN_ADC |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| DRDY_CS_ADC = CS ADC has completed at least a single measurement. This bit is cleared when [CS_MAIN_GO] is changed from 0 to 1. | | | | | | | | |
| DRDY_AUX_GPIO = AUX ADC has completed at least a single measurement on all active GPIO channels configured for ADC measurement. This bit is cleared when [AUX_GO] is changed from 0 to 1. 0 = Not ready 1 = All GPIO inputs have completed at least a single measurement by the AUX ADC | | | | | | | | |
| DRDY_AUX_CELL = Device has completed at least a single measurement on all AUXCELL channel(s) set by [AUX_CELL_SEL4:0]. This bit is cleared when [AUX_GO] is changed from 0 to 1. 0 = Not ready 1 = All [AUX_CELL_SEL4:0] configured channels have completed at least a single measurement | | | | | | | | |
| DRDY_AUX_MISC = Device has completed at least a single measurement on all AUX ADC MISC input channels (that is, completed a single round robin run). This bit is cleared when [AUX_GO] is changed from 0 to 1. 0 = Not ready 1 = All AUX ADC MISC inputs have completed at least a single measurement | | | | | | | | |
| DRDY_MAIN_ADC = Device has completed at least a single measurement on all Main ADC input channels, including all GPIOs (that is, completed a single round robin run). This bit is cleared when [CS_MAIN_GO] is changed from 0 to 1. 0 = Not ready 1 = All Main ADC inputs have completed at least a single measurement | | | | | | | | |

8.5.4.4.3 ADC_STAT2

| Address | 0x0528 | | | | | | | |
|--|--------|-------|----------|-----------|-----------|-----------|------------|-----------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | DRDY_LPF | DRDY_GPIO | DRDY_VCOW | DRDY_CBOW | DRDY_CBFET | DRDY_VCCB |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| DRDY_LPF = Device has finished at least 1 round of LPF checks on all active cell channels. The comparison continues in the background as long as the Main ADC is running. This bit is cleared when [CS_MAIN_GO] = 1. This data ready bit is also used when a fault is injected to test the DIAG_LPF engine using the [LPF_FLT_INJ] bit. When [LPF_FLT_INJ] = 1, this bit is cleared to 0 and the device will restart the VC and BB channel LPF checks from the beginning using the fault inject [DIAG_LPF]. Once all channel LPFs are checked, the [DRDY_LPF] = 1. 0 = Not ready 1 = Diagnostic comparison finished | | | | | | | | |
| DRDY_GPIO = Device has finished the GPIO Main and AUX ADC diagnostic comparisons on all active channels and the comparisons are stopped. This bit is cleared when [COMP_ADC_GO] = 1. 0 = Not ready 1 = Diagnostic comparison finished | | | | | | | | |
| DRDY_VCOW = Device has finished VC OW diagnostic comparison on all active channels and the comparison is stopped. This bit is cleared when [COMP_ADC_GO] = 1. 0 = Not ready 1 = Diagnostic comparison finished | | | | | | | | |

| |
|---|
| DRDY_CBOW = Device has finished CB OW diagnostic comparison on all active channels and the comparison is stopped. This bit is cleared when $[COMP_ADC_GO] = 1$. 0 = Not ready 1 = Diagnostic comparison finished |
| DRDY_CBFET = Device has finished CB FET diagnostic comparison on all active channels and the comparison is stopped. This bit is cleared when $[COMP_ADC_GO] = 1$. 0 = Not ready 1 = Diagnostic comparison finished |
| DRDY_VCCB = Device has finished VCELL vs. AUXCELL diagnostic comparison on all active channels. This bit is cleared when $[COMP_ADC_GO] = 1$. 0 = Not ready 1 = Diagnostic comparison finished |

8.5.4.4.4 GPIO_STAT

| Address | 0x052A | | | | | | | |
|---|--------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | GPIO8 | GPIO7 | GPIO6 | GPIO5 | GPIO4 | GPIO3 | GPIO2 | GPIO1 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GPIO1 through GPIO8 = When GPIO is configured as digital input or output, this register shows the GPIO status. 0 = Low 1 = High | | | | | | | | |

8.5.4.4.5 BAL_STAT

| Address | 0x052B | | | | | | | |
|------------------|--|--------------|------------|-------|--------|----------|-------|---------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | INVALID_CBCONF | OT_PAUSE_DET | CB_INPAUSE | RSVD | CB_RUN | ABORTFLT | RSVD | CB_DONE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | R | R | R | R | R | R | R | R |
| INVALID_CBCONF = | Indicates CB is unable to start (after $[BAL_GO] = 1$) due to improper CB control settings. Incorrect settings include: <ul style="list-style-type: none">More than three cells are enabled for CB.More than two adjacent cells are enabled for CB if $DEVICE_CONF[NO_ADJ_CB] = 0$.Any adjacent cells are enabled for CB if $DEVICE_CONF[NO_ADJ_CB] = 1$. This bit is updated every time $[BAL_GO] = 1$. 0 = Valid CB setting 1 = Invalid CB setting | | | | | | | |
| OT_PAUSE_DET = | Indicates the OTCB is detected if $[OTCB_EN] = 1$. The bit is also set if CB TWARN is detected, which will also pause CB. Valid only after $[BAL_GO] = 1$ 0 = No OTCB or CB TWARN is detected 1 = Any NTC thermistor measurement is greater than $OTCB_THR[3:0]$ setting, or die (CBFET) temperature is greater than CB TWARN | | | | | | | |
| CB_INPAUSE = | Indicates the cell balancing pause status. 0 = CB is running or not started 1 = Paused (can be caused by OTCB detection, or host sets $[CB_PAUSE] = 1$) | | | | | | | |
| RSVD = | Reserved | | | | | | | |
| CB_RUN = | Indicates cell balancing is running. Only valid after $[BAL_GO] = 1$. Does not indicate the module balancing status. This bit remains as 1 even if CB is in pause state. 0 = Completed or not started 1 = At least 1 cell is in active cell balancing | | | | | | | |
| ABORTFLT = | Indicates cell balancing is aborted due to detection of unmasked fault. Cleared when $BAL_CTRL1[BAL_GO] = 1$. CB abort does not trigger if CB is in pause ($[CB_INPAUSE] = 1$) even if an unmasked fault is detected. The abort at fault function will resume if CB is no longer in pause state. 0 = Not aborted or cell balancing not running 1 = Aborted | | | | | | | |

RSVD = Reserved

CB_DONE = Indicates all cell balancing is completed. Cleared when *BAL_CTRL1[BAL_GO]* = 1.
0 = Cell balancing is still running or has not started
1 = All cell balancing is completed

8.5.4.4.6 DEV_STAT

| Address | 0x052C | | | | | | | |
|---|--------|---------------|---------------|----------|----------|--------|---------|----------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | FACT_CRC_DONE | CUST_CRC_DONE | OTUT_RUN | OVUV_RUN | CS_RUN | AUX_RUN | MAIN_RUN |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| FACT_CRC_DONE = Indicates the status of the factory CRC state machine. This bit is set when the factory CRC is calculated and verified internally at least once. A read from this register will clear this bit. 0 = Not complete 1 = Complete (cleared on read) | | | | | | | | |
| CUST_CRC_DONE = Indicates the status of the customer CRC state machine. This bit is set when the CRC is calculated and compared to the <i>CUST_CRC</i> * registers at least once. A read from this register will clear this bit. 0 = Not complete 1 = Complete (cleared on read) | | | | | | | | |
| OTUT_RUN = Shows the status of the OTUT protector comparators. This bit is set when OTUT BIST starts. When BIST is completed or aborted, the device will turn off the OT and UT comparators automatically, and then this bit will be cleared. 0 = off (that is, OTUT is not started or when <i>[OTUT_GO]</i> = 1 and <i>[OTUT_MODE1:0]</i> = 0) 1 = on (that is, when <i>[OTUT_GO]</i> = 1 and <i>[OTUT_MODE1:0]</i> is non-zero) | | | | | | | | |
| OVUV_RUN = Shows the status of the OVUV protector comparators. This bit is set when OVUV BIST starts. When BIST is completed or aborted, the device will turn off the OV and UV comparators automatically, and then this bit will be cleared. 0 = off (that is, OVUV is not started or when <i>[OVUV_GO]</i> = 1 and <i>[OVUV_MODE1:0]</i> = 0) 1 = on (that is, when <i>[OVUV_GO]</i> = 1 and <i>[OVUV_MODE1:0]</i> is non-zero) | | | | | | | | |
| CS_RUN = Shows the status of the CS ADC. 0 = off 1 = on | | | | | | | | |
| AUX_RUN = Shows the status of the AUX ADC. 0 = off 1 = on | | | | | | | | |
| MAIN_RUN = Shows the status of the Main ADC. 0 = off 1 = on | | | | | | | | |

8.5.4.5 ADC Configuration and Control

8.5.4.5.1 ADC_CONF1

| Address | 0x0007 | | | | | | | |
|--|-----------------|-------|-------|-------------|-------|-------|----------------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | AUX_SETTLE[1:0] | | | LPF_SR[2:0] | | | LPF_VCELL[2:0] | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| AUX_SETTLE[1:0] = The AUXCELL configures the AUX CELL settling time. Each AUXCELL has to wait for the anti-aliasing filter (AAF) settling time in order to consider as a valid measurement. These bits provide the option to use different AAF or bypass an AAF to trade for a fast measurement. 00 = 4.3 ms 01 = 2.3 ms 10 = 1.3 ms 11 = Reserved | | | | | | | | |
| LPF_SR[2:0] = Configures the post main SAR ADC low-pass filter cut-off frequency for SRP/N measurement. Same options as the <i>LPF_VCELL[2:0]</i> . | | | | | | | | |

LPF_VCELL[2:0] = Configures the post ADC low-pass filter cut-off frequency for VCELL measurement.
0x0 = 6.5 Hz (154 ms average)
0x1 = 13 Hz (77 ms average)
0x2 = 26 Hz (38 ms average)
0x3 = 53 Hz (19 ms average)
0x4 = 111 Hz (9 ms average)
0x5 = 240 Hz (4 ms average)
0x6 = 600 Hz (1.6 ms average)
0x7 = 240 Hz

8.5.4.5.2 ADC_CONF2

| Address | 0x0008 | | | | | | | | |
|---|------------|-------|--------------|-------|-------|-------|-------|-------|--|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| Name | SPARE[1:0] | | ADC_DLY[5:0] | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| SPARE[1:0] = Spare | | | | | | | | | |
| ADC_DLY[5:0] = If [CS_MAIN/N_GO] bit is written to 1, bit Main ADC (applies to CS ADC too) is delayed for this setting time before being enabled to start the conversion. The option ranges from 0 μ s (no delay) to 200 μ s in 5- μ s steps. Undefined code = 0 μ s (no delay) | | | | | | | | | |

8.5.4.5.3 MAIN_ADC_CAL1

| Address | 0x001B | | | | | | | | |
|--|--------|-------|------------|-------|-------|-------|-------|-------|--|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| Name | | | GAINL[7:0] | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| GAINL[7:0] = Main ADC 25°C gain calibration result (lower 8-bit). If customer performs gain calibration during production flow, the gain result can be programmed to OTP and will be sent to this gain register at device reset. The device automatically applies this data during ADC correction step. Range from -0.78125% to 0.7782% in 0.0031% steps. | | | | | | | | | |

8.5.4.5.4 MAIN_ADC_CAL2

| Address | 0x001C | | | | | | | | |
|--|--------|-------------|-------|-------|-------|-------|-------|-------|--|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| Name | GAINH | OFFSET[6:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| GAINH = Main ADC 25°C gain calibration result (MS bit). If customer performs gain calibration during production flow, the gain result can be programmed to OTP and will be sent to this gain register at device reset. The device automatically applies this data during ADC correction step. Range from -0.78125% to 0.7782% in 0.0031% steps. | | | | | | | | | |
| OFFSET[6:0] = Main ADC 25°C offset calibration result. If customer performs offset calibration during production flow, the offset result can be programmed to OTP and will be sent to this offset register at device reset. The device automatically applies this data during ADC correction step. Range from -12.20703-mV to 12.01630-mV in 0.19073-mV steps | | | | | | | | | |

8.5.4.5.5 AUX_ADC_CAL1

| Address | 0x001D | | | | | | | | |
|---------|--------|-------|------------|-------|-------|-------|-------|-------|--|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| Name | | | GAINL[7:0] | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

GAINL[7:0] = AUX ADC 25°C gain calibration result (lower 8-bit). If customer performs gain calibration during production flow, the gain result can be programmed to OTP and will be sent to this gain register at device reset. The device automatically applies this data during ADC correction step.
 Range from -0.78125% to 0.7782% in 0.0031% steps.

8.5.4.5.6 AUX_ADC_CAL2

| Address | 0x001E | | | | | | | |
|---|--------|-------------|-------|-------|-------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | GAINH | OFFSET[6:0] | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GAINH AUX ADC 25°C gain calibration result (MS bit). If customer performs gain calibration during production flow, the gain result can be programmed to OTP and will be sent to this gain register at device reset. The device automatically applies this data during ADC correction step. Range from -0.78125% to 0.7782% in 0.0031% steps. | | | | | | | | |
| OFFSET[6:0] = AUX ADC 25°C offset calibration result. If customer performs offset calibration during production flow, the offset result can be programmed to OTP and will be sent to this offset register at device reset. The device automatically applies this data during ADC correction step. Range from -12.20703-mV to 12.01630-mV in 0.19073-mV steps | | | | | | | | |

8.5.4.5.7 CS_ADC_CAL1

| Address | 0x001F | | | | | | | |
|---|--------|-------|-------|-------|------------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | | | | | GAINL[7:0] | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| GAINL[7:0] = CS ADC gain correction, lower 8-bits Range from -0.78125% to 0.78049% in 0.0008% steps. | | | | | | | | |

8.5.4.5.8 CS_ADC_CAL2

| Address | 0x0020 | | | | | | | |
|--|--------|------------|-------|-------|-------|-------------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | | GAINH[2:0] | | | | OFFSET[4:0] | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| OFFSET[4:0] = 8-bit register for CS ADC offset correction. Range from -3.8147- μ V to 3.57628- μ V in 0.23842- μ V steps. | | | | | | | | |
| GAINH[2:0] CS ADC gain correction, upper 3-bits Range from -0.78125% to 0.78049% in 0.0008% steps. | | | | | | | | |

8.5.4.5.9 ADC_CTRL1

| Address | 0x030D | | | | | | | |
|---|--------|------------|-------|-----------|--------------|------------|-------------------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | CS_DR[1:0] | | LPF_SR_EN | LPF_VCELL_EN | CS_MAIN_GO | CS_MAIN_MODE[1:0] | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| CS_DR[1:0] = Configures the desired single measurement time of the CS ADC. 00 = 768 μ s 01 = 1.536 ms 10 = 3.072 ms 11 = 12.288 ms | | | | | | | | |
| LPF_SR_EN = Enables digital low-pass filter post-ADC conversion. LPF applies to SRP/N measurements only. The cut-off frequency is configured by ADC_CONF/G1[LPF_SR[2:0]]. | | | | | | | | |

| | | | | | | | | |
|---|--|--|--|--|--|--|--|--|
| LPF_VCELL_EN = Enables digital low-pass filter post-ADC conversion. LPF applies to VCELL measurements only. The cut-off frequency is configured by <i>ADC_CONFIG1[LPF_VCELL[2:0]</i> . | | | | | | | | |
| CS_MAIN_GO = Starts main ADC conversion. When this bit is written to 1, all Main ADC inputs are sampled. Once the Main ADC is started, any change to the Main ADC control setting has no effect until this bit is written to 1 again. This bit is cleared to 0 in read. 0 = Ready. Writing 0 has no effect 1 = Start Main ADC This control also applies to the CS ADC. In sleep mode, CS ADC need to be disabled, otherwise, it consumes extra current ICS_ADC | | | | | | | | |
| CS_MAIN_MODE[1:0] = Sets the Main ADC run mode. 00 = Main ADC not running 01 = Single run. Run the main ADC round robin 8 times and then stop 10 = Continuous run. Continuous running the Main ADC round robin until host sends command to stop 11 = Reserved This control also applies to the CS ADC. | | | | | | | | |

8.5.4.5.10 ADC_CTRL2

| Address | 0x030E | | | | | | | |
|---|--------|----------------|----------------|-------------------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | MAINBB_AFE_DIS | AUX_CELL_ALIGN | AUX_CELL_SEL[4:0] | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| MAINBB_AFE_DIS = Disconnected main ADC SRP/SRN AFE from SRP/SRN pin, this would leave SRP/SRN sensed by CS ADC stand alone. 0 = Connected 1 = Disconnected | | | | | | | | |
| AUX_CELL_ALIGN = Align the AUX ADC AUXCELL measurement to Main ADC CELL1 or CELL8 0 = Align to Main ADC CELL1 1 = RSVD | | | | | | | | |
| AUX_CELL_SEL[4:0] = Selects which AUXCELL channel(s) will be multiplexed through the AUX ADC. 0x00 = Run all active cell channels set by <i>ACTIVE_CELL_CONF</i> register 0x01 = SRP/SRN are not connected to AUX ADC 0x02 = Lock to AUXCELL1 0x03 = Lock to AUXCELL2 0x04 = Lock to AUXCELL3 : 0x = 07 Lock to AUXCELL6 0x08 to 0x1F = RSVD NOTE: If inactive channel or RSVD code is selected, device will not perform AUX ADC conversion on the AUXCELL slot and the <i>AUX_CELL_HI/LO</i> registers will be kept in reset value. | | | | | | | | |

8.5.4.5.11 ADC_CTRL3

| Address | 0x030F | | | | | | | |
|--|--------|-------------------|-------|-------|-------|-------|--------|---------------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | AUX_GPIO_SEL[3:0] | | | | | AUX_GO | AUX_MODE[1:0] |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| AUX_GPIO_SEL[3:0] = Selects which GPIO channel(s) will be multiplexed through the AUX ADC to use for temperature measurement diagnostic. If this selection is not set to 0x00, the AUX ADC will lock onto a single GPIO channel and the measurement result is output to the <i>AUX_GPIO_HI/LO</i> registers. 0x00 = AUX ADC cycles through all GPIO channel(s) that are configured as ADC only or ADC and OTUT. 0x01 = Lock to GPIO1 0x02 = Lock to GPIO2 : 0x08 = Lock to GPIO8 All other codes are RSVD. NOTE: If GPIO is not configured for ADC measurement or RSVD codes are selected, device will not perform AUX ADC conversion on the GPIO slot and the <i>AUX_GPIO_HI/LO</i> registers will be kept in reset value. | | | | | | | | |

AUX_GO = Starts AUX ADC conversion. When this bit is written to 1, all AUX ADC inputs are sampled. Once the AUX ADC is started, any change to the AUX ADC control setting has no effect until this bit is written to 1 again. This bit is cleared to 0 in read.
0 = Ready. Writing 0 has no effect.
1 = Start AUX ADC

AUX_MODE[1:0] = Sets the Main ADC run mode.
00 = AUX ADC not running
01 = Single run. Run the AUX ADC round robin once and then stop.
10 = Continuous run. Continually run the AUX ADC round robin until host sends command to stop.
11 = 8-round-robin run to measure all eight GPIOs once.

8.5.4.6 ADC Measurement Results

8.5.4.6.1 VCELL6_HI/LO

VCELL6_HI

| Address | 0x057C | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement result of the high-byte of the Cell6 voltage in 2s complement. When host reads this register, the device locks the Cell6 voltage low-byte from updating until the high-byte and low-byte registers are read.

VCELL6_LO

| Address | 0x057D | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement result of the low-byte of the Cell6 voltage in 2s complement.

8.5.4.6.2 VCELL5_HI/LO

VCELL5_HI

| Address | 0x057E | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement result of the high-byte of the Cell5 voltage in 2s complement. When host reads this register, the device locks the Cell5 voltage low-byte from updating until the high-byte and low-byte registers are read.

VCELL5_LO

| Address | 0x057F | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement result of the low-byte of the Cell5 voltage in 2s complement.

8.5.4.6.3 VCELL4_HI/LO

VCELL4_HI

| Address | 0x0580 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement result of the high-byte of the Cell4 voltage in 2s complement. When host reads this register, the device locks the Cell4 voltage low-byte from updating until the high-byte and low-byte registers are read.

VCELL4_LO

| Address | 0x0581 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement result of the low-byte of the Cell4 voltage in 2s complement.

8.5.4.6.4 VCELL3_HI/LO
VCELL3_HI

| Address | 0x0582 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement result of the high-byte of the Cell3 voltage in 2s complement. When host reads this register, the device locks the Cell3 voltage low-byte from updating until the high-byte and low-byte registers are read.

VCELL3_LO

| Address | 0x0583 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement result of the low-byte of the Cell3 voltage in 2s complement.

8.5.4.6.5 VCELL2_HI/LO
VCELL2_HI

| Address | 0x0584 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement result of the high-byte of the Cell2 voltage in 2s complement. When host reads this register, the device locks the Cell2 voltage low-byte from updating until the high-byte and low-byte registers are read.

VCELL2_LO

| Address | 0x0585 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement result of the low-byte of the Cell2 voltage in 2s complement.

8.5.4.6.6 VCELL1_HI/LO
VCELL1_HI

| | | | | | | | | |
|--|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Address | 0x0586 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement result of the high-byte of the Cell1 voltage in 2s complement. When host reads this register, the device locks the Cell1 voltage low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

VCELL1_LO

| | | | | | | | | |
|---|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Address | 0x0587 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement result of the low-byte of the Cell1 Voltage in 2s complement. | | | | | | | | |

8.5.4.6.7 MAIN_CURRENT_HI/LO

MAIN_CURRENT_HI

| | | | | | | | | |
|---|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Address | 0x0588 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement result of the high-byte of the differential (SRP - SRN) in 2s complement. When host reads this register, the device locks the low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

MAIN_CURRENT_LO

| | | | | | | | | |
|--|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Address | 0x0589 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement result of the low-byte of the differential (SRP - SRN) in 2s complement. | | | | | | | | |

8.5.4.6.8 CURRENT_HI/MID/LO

CURRENT_HI

| | | | | | | | | |
|--|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Address | 0x0506 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte of the differential (SRP - SRN) in 2s complement from CS ADC. When host reads this register, the device locks the mid- and low-byte from update until the high-byte and low-byte registers are read. | | | | | | | | |

CURRENT_MID

| | | | | | | | | |
|----------------|---------------|--|--|--|--|--|--|--|
| Address | 0x0507 | | | | | | | |
|----------------|---------------|--|--|--|--|--|--|--|

| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The mid-byte of the differential (SRP - SRN) in 2s complement from CS ADC. | | | | | | | | |

CURRENT_LO

| Address | 0x0508 | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte of the differential (SRP - SRN) in 2s complement from CS ADC. | | | | | | | | |

8.5.4.6.9 TSREF_HI/LO

TSREF_HI

| Address | 0x058C | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The TSREF high-byte result from Main ADC. When host reads this register, the device locks the TSREF low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

TSREF_LO

| Address | 0x058D | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The TSREF low-byte result from Main ADC | | | | | | | | |

8.5.4.6.10 GPIO1_HI/LO

GPIO1_HI

| Address | 0x058E | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement high-byte result of the GPIO1. When host reads this register, the device locks the GPIO1 low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

GPIO1_LO

| Address | 0x058F | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement low-byte result of the GPIO1. | | | | | | | | |

8.5.4.6.11 GPIO2_HI/LO

GPIO2_HI

| | | | | | | | | |
|--|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x0590 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement high-byte result of the GPIO2. When host reads this register, the device locks the GPIO2 low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

GPIO2_LO

| | | | | | | | | |
|---|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x0591 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement low-byte result of the GPIO2. | | | | | | | | |

8.5.4.6.12 GPIO3_HI/LO

GPIO3_HI

| | | | | | | | | |
|--|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x0592 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement high-byte result of the GPIO3. When host reads this register, the device locks the GPIO3 low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

GPIO3_LO

| | | | | | | | | |
|---|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x0593 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement low-byte result of the GPIO3. | | | | | | | | |

8.5.4.6.13 GPIO4_HI/LO

GPIO4_HI

| | | | | | | | | |
|----------------|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x0594 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement high-byte result of the GPIO4. When host reads this register, the device locks the GPIO4 low-byte from updating until the high-byte and low-byte registers are read.

GPIO4_LO

| | | | | | | | | |
|----------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Address | 0x0595 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement low-byte result of the GPIO4.

8.5.4.6.14 GPIO5_HI/LO

GPIO5_HI

| | | | | | | | | |
|----------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Address | 0x0596 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement high-byte result of the GPIO5. When host reads this register, the device locks the GPIO5 low-byte from updating until the high-byte and low-byte registers are read.

GPIO5_LO

| | | | | | | | | |
|----------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Address | 0x0597 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement low-byte result of the GPIO5.

8.5.4.6.15 GPIO6_HI/LO

GPIO6_HI

| | | | | | | | | |
|----------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Address | 0x0598 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement high-byte result of the GPIO6. When host reads this register, the device locks the GPIO6 low-byte from updating until the high-byte and low-byte registers are read.

GPIO6_LO

| | | | | | | | | |
|----------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Address | 0x0599 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The ADC measurement low-byte result of the GPIO6.

8.5.4.6.16 GPIO7_HI/LO

GPIO7_HI

| Address | 0x059A | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement high-byte result of the GPIO7. When host reads this register, the device locks the GPIO7 low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

GPIO7_LO

| Address | 0x059B | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement low-byte result of the GPIO7. | | | | | | | | |

8.5.4.6.17 GPIO8_HI/LO

GPIO8_HI

| Address | 0x059C | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement high-byte result of the GPIO8. When host reads this register, the device locks the GPIO8 low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

GPIO8_LO

| Address | 0x059D | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The ADC measurement low-byte result of the GPIO8. | | | | | | | | |

8.5.4.6.18 DIETEMP1_HI/LO

DIETEMP1_HI

| Address | 0x05AE | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The DieTemp1 high-byte result from Main ADC. When host reads this register, the device locks the DIETEMP1 low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

DIETEMP1_LO

| Address | 0x05AF | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

8.5.4.6.19 DIETEMP2_HI/LO

DIETEMP2_HI

| Address | 0x05B0 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DIETEMP2_LO

| Address | 0x05B1 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

8.5.4.6.20 AUX_CELL_HI/LO

AUX_CELL_HI

| Address | 0x05B2 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

AUX_CELL_LO

| Address | 0x05B3 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

8.5.4.6.21 AUX_GPIO_HI/LO

AUX_GPIO_HI

| Address | 0x05B4 | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The AUX ADC measurement high-byte result of the GPIO that is locked by the [AUXGPIO_SEL3:0] bits. When host reads this register, the device locks the AUX_GPIO low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_GPIO_LO

| Address | 0x05B5 | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The AUX ADC measurement low-byte result of the GPIO that is locked by the [AUXGPIO_SEL3:0] bits. | | | | | | | | |

8.5.4.6.22 AUX_BAT_HI/LO

AUX_BAT_HI

| Address | 0x05B6 | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the BAT pin measurement from AUX ADC. When host reads this register, the device locks the AUX_BAT low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_BAT_LO

| Address | 0x05B7 | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the BAT pin measurement from AUX ADC. | | | | | | | | |

8.5.4.6.23 AUX_REFI_HI/LO

AUX_REFI_HI

| Address | 0x05B8 | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the internal reference, REFL, measurement from AUX ADC. When host reads this register, the device locks the AUX_REL low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_REFI_LO

| | | | | | | | | |
|--|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05B9 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the internal reference, REFL, measurement from AUX ADC. | | | | | | | | |

8.5.4.6.24 AUX_VBG2_HI/LO

AUX_VBG2_HI

| | | | | | | | | |
|--|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05BA | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the internal reference, VBG2, measurement from AUX ADC. When host reads this register, the device locks the AUX_VBG2 low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_VBG2_LO

| | | | | | | | | |
|--|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05BB | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the internal reference, VBG2, measurement from AUX ADC. | | | | | | | | |

8.5.4.6.25 AUX_AVAO_REF_HI/LO

AUX_AVAO_REF_HI

| | | | | | | | | |
|---|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05BE | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the AVAO_REF measurement from AUX ADC. When host reads this register, the device locks the AUX_AVAO_REF low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_AVAO_REF_LO

| | | | | | | | | |
|---|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05BF | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the AVAO_REF measurement from AUX ADC. | | | | | | | | |

8.5.4.6.26 AUX_AVDD_REF_HI/LO

AUX_AVDD_REF_HI

| | | | | | | | | |
|----------------|---------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05C0 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

| | | | | | | | | |
|---|-------------|---|---|---|---|---|---|---|
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the AVDD_REF measurement from AUX ADC. When host reads this register, the device locks the AUX_AVDD_REF low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_AVDD_REF_LO

| | | | | | | | | |
|---|--------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05C1 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the AVDD_REF measurement from AUX ADC. | | | | | | | | |

8.5.4.6.27 AUX_OV_DAC_HI/LO

AUX_OV_DAC_HI

| | | | | | | | | |
|--|--------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05C2 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the OV comparator DAC measurement, which is (0.8 x OV threshold), from AUX ADC. When host reads this register, the device locks the AUX_OV_DAC low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_OV_DAC_LO

| | | | | | | | | |
|--|--------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05C3 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the OV comparator DAC measurement, which is (0.8 x OV threshold), from AUX ADC. | | | | | | | | |

8.5.4.6.28 AUX_UV_DAC_HI/LO

AUX_UV_DAC_HI

| | | | | | | | | |
|--|--------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05C4 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the UV comparator DAC measurement, which is (0.8 x UV threshold), from AUX ADC. When host reads this register, the device locks the AUX_UV_DAC low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_UV_DAC_LO

| | | | | | | | | |
|--|--------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x05C5 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the UV comparator DAC measurement, which is (0.8 x UV threshold), from AUX ADC. | | | | | | | | |

8.5.4.6.29 AUX_OT_OTCB_DAC_HI/LO

AUX_OT_OTCB_DAC_HI

| Address | 0x05C6 | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the OT comparator (either OT or OTCB threshold based on [OTCB_THR_LOCK] setting) DAC measurement from AUX ADC. When host reads this register, the device locks the AUX_OT_OTCB_DAC low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_OT_OTCB_DAC_LO

| Address | 0x05C7 | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the OT comparator (either OT or OTCB threshold based on [OTCB_THR_LOCK] setting) DAC measurement from AUX ADC. | | | | | | | | |

8.5.4.6.30 AUX_UT_DAC_HI/LO

AUX_UT_DAC_HI

| Address | 0x05C8 | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the UT comparator DAC measurement from AUX ADC. When host reads this register, the device locks the AUX_UT_DAC low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_UT_DAC_LO

| Address | 0x05C9 | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the UT comparator DAC measurement from AUX ADC. | | | | | | | | |

8.5.4.6.31 AUX_VCBDONE_DAC_HI/LO

AUX_VCBDONE_DAC_HI

| Address | 0x05CA | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the UV comparator (VCBDONE Threshold) DAC measurement from AUX ADC. When host reads this register, the device locks the AUX_VCBDONE_DAC low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_VCBDONE_DAC_LO

| Address | 0x05CB | | | | | | | |
|---------|--------|--|--|--|--|--|--|--|
| | | | | | | | | |

| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the UV comparator (VCBDONE Threshold) DAC measurement from AUX ADC. | | | | | | | | |

8.5.4.6.32 AUX_VCM_HI/LO

AUX_VCM_HI

| Address | 0x05CC | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the VCM (common mode voltage on Main ADC) measurement from AUX ADC. When host reads this register, the device locks the AUX_VCM low-byte from updating until the high-byte and low-byte registers are read. | | | | | | | | |

AUX_VCM_LO

| Address | 0x05CD | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the VCM (common mode voltage on Main ADC) measurement from AUX ADC. | | | | | | | | |

8.5.4.6.33 REFOVDAC_HI/LO

REFOVDAC_HI

| Address | 0x05D0 | | | | | | | |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of the recorded OVDAC reference voltage trimmed at factory. | | | | | | | | |

REFOVDAC_LO

| Address | 0x05D1 | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The low-byte result of the recorded OVDAC reference voltage trimmed at factory. | | | | | | | | |

8.5.4.6.34 DIAG_MAIN_HI/LO

DIAG_MAIN_HI

| Address | 0x05D2 | | | | | | | |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RESULT[7:0] = The high-byte result of reported Main ADC comparison value used in the diagnostic ADC comparison. Valid if the diagnostic ADC comparison is run when a single channel is locked | | | | | | | | |

DIAG_MAIN_LO

| Address | 0x05D3 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The low-byte result of reported Main ADC comparison value used in the diagnostic ADC comparison. Valid if the diagnostic ADC comparison is run when a single channel is locked

8.5.4.6.35 DIAG_AUX_HI/LO**DIAG_AUX_HI**

| Address | 0x05D4 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The high-byte result of reported AUX ADC comparison value used in the diagnostic ADC comparison. Valid if the diagnostic ADC comparison is run when a single channel is locked

DIAG_AUX_LO

| Address | 0x05D5 | | | | | | | |
|-----------|-------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RESULT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RESULT[7:0] = The low-byte result of reported AUX ADC comparison value used in the diagnostic ADC comparison. Valid if the diagnostic ADC comparison is run when a single channel is locked

8.5.4.7 Balancing Configuration, Control and Status**8.5.4.7.1 CB_CELL6_CTRL through CB_CELL1_CTRL**

| Address | 0x0322 to 0x0327 | | | | | | | | |
|---------|------------------|-------|-------|-----------|-------|-------|-------|-------|--|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| Name | RSVD | | | TIME[4:0] | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

RSVD = Reserved

TIME[4:0] = Sets the timer for cell* balancing. The selection is sampled whenever [BAL_GO] = 1 is set by the host MCU.

- 0x00 = 0 s = stop balancing
- 0x01 = 10 s
- 0x02 = 30 s
- 0x03 = 60 s
- 0x04 = 300 s
- 0x05 to 0x10 = range from 10 min to 120 min in 10-min steps
- 0x11 to 0x1F = range from 150 min to 540 min in 30-min steps and 600 min

8.5.4.7.2 VCB_DONE_THRESH

| Address | 0x032A | | | | | | | | |
|---------|--------|-------|-------|-------------|-------|-------|-------|-------|--|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| Name | RSVD | | | CB_THR[5:0] | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

RSVD = Reserved

CB_THR[5:0] = If a cell voltage is less than this threshold, the cell balancing on that cell stops. This threshold setting applies to all cells. The selection is sampled whenever *[OVUV_GO]* = 1 is set by the host MCU.
 Note: To use the VCB_DONE detection feature, host sets this threshold, then issues *[OVUV_GO]* = 1 before starting CB (that is, sending *[BAL_GO]* = 1).
 To change the VCB_DONE threshold detection, set a new threshold then re-issue *[OVUV_GO]* = 1 for the new threshold to take effect. It is not necessary to re-issue *[BAL_GO]* = 1 to restart balancing in this case.
 Range from 2.45-V to 4-V with 25-mV steps, where
 0x00 = Disables voltage based on CB_DONE comparison
 0x01 = threshold of 2.45-V
 0x3F = threshold of 4-V

8.5.4.7.3 OTCB_THRESH

| Address | 0x032B | | | | | | | |
|---|--------|--------------|-------|-------|-------|-------|------------------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | COOLOFF[2:0] | | | | | OTCB_THRESH[3:0] | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| RSVD = Reserved | | | | | | | | |
| COOLOFF[2:0] = Sets the COOLOFF hysteresis (resume temperature = OTCB_THRESH - COOLOFF hysteresis) to resume CB when <i>BAL_CTRL1[OTCB_EN]</i> = 1 and OTCB is detected. The MCU configures the corresponding GPIO(s) to the ADC and OTUT option. Range from 4% to 14% in steps of 2%. Unused code is set to 14%. | | | | | | | | |
| OTCB_THRESH[3:0] = Sets the OTCB threshold when <i>BAL_CTRL1[OTCB_EN]</i> = 1. The MCU configures the corresponding GPIO(s) to the ADC and OTUT option. Range from 10% to 24% in steps of 2%. Unused code is set to 24%. | | | | | | | | |

8.5.4.7.4 BAL_CTRL1

| Address | 0x032E | | | | | | | |
|---|--------|-------|-------|-------|-------|-----------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | DUTY[2:0] | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| DUTY[2:0] = Selection is sampled whenever <i>[BAL_GO]</i> = 1 is set by the host MCU. 0x0 = 5 s 0x1 = 10 s 0x2 = 30 s 0x3 = 60 s 0x4 = 5 min 0x5 = 10 min 0x6 = 20 min 0x7 = 30 min | | | | | | | | |

8.5.4.7.5 BAL_CTRL2

| Address | 0x032F | | | | | | | |
|---|--------|----------|------------|---------|--------------|-------|--------|----------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | CB_PAUSE | FLTSTOP_EN | OTCB_EN | BAL_ACT[1:0] | | BAL_GO | AUTO_BAL |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| CB_PAUSE = Pauses cell balancing on all cells to allow diagnostics to run. 0 = Normal cell balancing operation 1 = Pause all cell balancing | | | | | | | | |

| | |
|---|--|
| <p>FLTSTOP_EN = Stops cell balancing if unmasked fault occurs. The selection is sampled whenever <i>[BAL_GO]</i> = 1 is set by the host MCU.</p> <p>0 = Balancing is continuous regardless of fault condition (excluding thermal shutdown)</p> <p>1 = All CB balancing stops when any unmasked fault occurs</p> | |
| <p>OTCB_EN = Enables the OTCB detection during cell balancing. The selection is sampled whenever <i>[BAL_GO]</i> = 1 is set by the host MCU.</p> <p>0 = Disable OTCB detection</p> <p>1 = Enable OTCB detection</p> | |
| <p>BAL_ACT[1:0] = Controls the device action when the MB and CB are completed. These bits are samples whenever <i>[BAL_GO]</i> = 1 is set by the host MCU. The action is valid.</p> <p>00 = No action</p> <p>01 = Enters SLEEP</p> <p>10 = Enters SHUTDOWN</p> <p>11 = Reserved</p> | |
| <p>BAL_GO = Starts cell balancing. When written to 1, all balancing configuration registers are sampled. Any change to the configuration registers has no effect until this bit is written to 1 again. The bit is self-clearing.</p> <p>0 = Ready</p> <p>1 = Start balancing</p> | |
| <p>AUTO_BAL = Selects between auto or manual cell balance control. The selection is sampled whenever <i>[BAL_GO]</i> = 1 is set by the host MCU.</p> <p>0 = Manual cell balancing</p> <p>1 = Auto cell balancing</p> | |

8.5.4.7.6 BAL_CTRL3

| Address | 0x0330 | | | | | | | |
|--|--------|-------|-------|-------------------|-------|-------|-------|-------------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | BAL_TIME_SEL[3:0] | | | | BAL_TIME_GO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| BAL_TIME_GO Instruct the device to report the selected CB channel (set by <i>[BAL_TIME_SEL3:0]</i>) remaining balancing time to <i>BAL_TIME</i> register | | | | | | | | |
| <p>BAL_TIME_SEL[3:0] = Select a single CB channel to report its remaining balancing time</p> <p>0x0 = CB Channel 1</p> <p>0x1 = CB Channel 2</p> <p>:</p> <p>0x5 = CB Channel 6;</p> <p>0x6 - 0xF = RSVD</p> | | | | | | | | |

8.5.4.7.7 CB_COMPLETE2

| Address | 0x0557 | | | | | | | |
|---|--------|-------|------------|------------|------------|------------|------------|------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | RSVD | CELL6_DONE | CELL5_DONE | CELL4_DONE | CELL3_DONE | CELL2_DONE | CELL1_DONE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CELL1_DONE to Cell balance completion for cell1 to cell.6 This register is cleared when MCU sets <i>[BAL_GO]</i> = 1. | | | | | | | | |
| CELL_6DONE = 0 = Balancing on the particular cell is still running or has not started | | | | | | | | |
| 1 = Balancing completed on the particular cell | | | | | | | | |

8.5.4.7.8 BAL_TIME

| Address | 0x0558 | | | | | | | |
|-----------|-----------|-----------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | TIME_UNIT | TIME[6:0] | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TIME_UNIT = Indicates the unit reported by[TIME6:0]

0 = sec

1 = min

TIME[6:0] = Report the selected CB channel remaining balancing time

If [TIME_UNIT] = 0. Time report in sec with 5sec step

If [TIME_UNIT] = 1. Time report in min with 5min step

8.5.4.8 Protector Configuration and Control

8.5.4.8.1 OV_THRESH

| Address | 0x0009 | | | | | | | |
|--|--------|-------|-------------|-------|-------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | SPARE | SPARE | OV_THR[5:0] | | | | | |
| Reset | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| SPARE = Spare | | | | | | | | |
| <p>OV_THR[5:0] = Sets the overvoltage threshold for the OV comparator. Changes on these bits require host to send another [OVUV_GO] = 1 command. All settings are at 25-mV steps. 0x02 to 0x0E: range from 2700 mV to 3000 mV 0x12 to 0x1E: range from 3500 mV to 3800 mV 0x22 to 0x2E: range from 4175 mV to 4475 mV All other settings will default to 2700 mV.</p> | | | | | | | | |

8.5.4.8.2 UV_THRESH

| Address | 0x000A | | | | | | | |
|---|--------|-------|-------------|-------|-------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | SPARE | SPARE | UV_THR[5:0] | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SPARE = Spare | | | | | | | | |
| <p>UV_THR[5:0] = Sets the undervoltage threshold for the UV comparator. Changes on these bits require host to send another [OVUV_GO] = 1 command. All settings are at 50-mV steps. 0x00 to 0x26: range from 1200 mV to 3100 mV All other settings will default to 3100 mV.</p> | | | | | | | | |

8.5.4.8.3 UV_DISABLE2

| Address | 0x000D | | | | | | | |
|---|--------|-------|-------|-------|-------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | RSVD | CELL6 | CELL5 | CELL4 | CELL3 | CELL2 | CELL1 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <p>CELL 6to Indicate which channels shall be excluded from UV and VCB_DONE detection CELL1 = 0 = UV and VCB_DONE monitoring apply to the channel 1 = UV and VCB_DONE monitoring are excluded from the channel</p> | | | | | | | | |

8.5.4.8.4 OTUT_THRESH

| Address | 0x000B | | | | | | | |
|---|-------------|-------|-------|-------|-------------|-------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | UT_THR[2:0] | | | | OT_THR[4:0] | | | |
| Reset | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| <p>UT_THR[2:0] = Sets the UT threshold for the UT comparator. Changes on these bits require host to send another [OTUT_GO] = 1 command. The MCU configures the corresponding GPIO(s) to ADC and OTUT input. Range from 66% to 80% in steps of 2%</p> | | | | | | | | |

OT_THR[4:0] = Sets the OT threshold for the OT comparator. Changes on these bits require host to send another [OTUT_GO] = 1 command. The MCU configures the corresponding GPIO(s) to ADC and OTUT input.
Range from 10% to 39% in steps of 1%
Unused code defaults to 39%.

8.5.4.8.5 OVUV_CTRL

| Address | 0x032C | | | | | | | |
|---|------------------|----------------|-------|-------|-------|-------|---------|----------------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | VCBDONE_THR_LOCK | OVUV_LOCK[3:0] | | | | | OVUV_GO | OVUV_MODE[1:0] |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VCBDONE_THR_LOCK = As the UV comparator is switching between UV threshold and VCBDONE threshold to measure the UV DAC or the VCBDONE DAC result for diagnostics, the UV comparator has to lock onto only one threshold before starting the AUX ADC measurement. This bit selects which threshold is locked to the UV comparator. The bit is sampled when OVUV_MODE[1:0] is 0b11 which is locked to a single channel mode. 0 = UV threshold is selected 1 = VCBDONE threshold is selected | | | | | | | | |
| OVUV_LOCK[3:0] = Configures a particular single channel as the OV and UV comparators input when [OVUV_MODE1:0] = 0b11. Changes on these bits require host to send another [OVUV_GO] = 1 command. 0x0 = Lock to Cell1 0x1 = Lock to Cell2 0x2 = Lock to Cell3 : 0x5 = Lock to Cell6; 0x6 - 0xF = RSVD | | | | | | | | |
| OVUV_GO = Starts the OV and UV comparators. When written to 1, all OVUV configuration settings are sampled. This bit is self-clearing. 0 = Ready 1 = Start OV and UV comparators | | | | | | | | |
| OVUV_MODE[1:0] = Sets the OV and UV comparators operation mode when [OVUV_GO] = 1. Changes on these bits require host to send another [OVUV_GO] = 1 command. 00 = Do not run OV and UV comparators 01 = Run the OV and UV round robin with all active cells 10 = Run the OV and UV BIST cycle. 11 = Lock OV and UV comparators to a single channel configured by [OVUV_LOCK3:0] Note: Active cells are defined by the ACTIVE_CELL[NUM_CELL3:0] register. | | | | | | | | |

8.5.4.8.6 OTUT_CTRL

| Address | 0x032D | | | | | | | |
|---|--------|---------------|----------------|-------|-------|-------|-------|---------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | OTCB_THR_LOCK | OTUT_LOCK[2:0] | | | | | OTUT_GO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| OTCB_THR_LOCK = As the OT comparator is switching between OT threshold and OTCB threshold to measure the OT or OTCB DAC threshold result for diagnostics, the OT comparator has to lock onto only one threshold before starting the AUX ADC measurement. This bit selects which threshold is locked to the OT comparator. The bit is sampled when OTUT_MODE[1:0] = 0b11 which is locked to a single channel mode. 0 = OT threshold is selected 1 = OTCB threshold is selected | | | | | | | | |
| OTUT_LOCK[2:0] = Configures a particular single channel as the OT and UT comparators input when [OTUT_MODE1:0] = 0b11. Changes on these bits require host to send another [OTUT_GO] = 1 command. 0x0 = Lock to GPIO1A 0x1 = Lock to GPIO2A : 0x7 = Lock to GPIO8A | | | | | | | | |

| | | | | | | | | |
|---|--|--|--|--|--|--|--|--|
| OTUT_GO = Starts the OT and UT comparators. When written to 1, all OTUT configuration settings are sampled. This bit is self-clearing. 0 = Ready 1 = Start OT and UT comparators | | | | | | | | |
| OTUT_MODE[1:0] = Sets the OT and UT comparators operation mode when [OTUT_GO] = 1. Changes on these bits require host to send another [OTUT_GO] = 1 command. 00 = Do not run OT and UT comparators 01 = Run the OT and UT round robin with all active cells 10 = Run the OT and UT BIST cycle. 11 = Lock OT and UT comparators to a single channel configured by [OTUT_LOCK3:0] | | | | | | | | |

8.5.4.9 GPIO Configuration

8.5.4.9.1 GPIO_CONF1

| Address | 0x000E | | | | | | | |
|--|-------------|--------|------------|-------|-------|------------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | FAULT_IN_EN | SPI_EN | GPIO2[2:0] | | | GPIO1[2:0] | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FAULT_IN_EN = Enables GPIO8 as an active-low input to trigger the NFAULT pin when the input signal is low. 0 = No fault input function. GPIO8 is configured based on [GPIO8_CONF2:0] setting. 1 = GPIO8 is set as active-low input to trigger NFAULT pin, [GPIO8_CONF2:0] setting is ignored. | | | | | | | | |
| SPI_EN = Enables SPI controller on GPIO4, GPIO5 and GPIO6, GPIO7. 0 = SPI controller disabled. 1 = SPI controller enabled. Overwrite the [GPIO4_CONF2:0], [GPIO5_CONF2:0], [GPIO6_CONF2:0], and [GPIO7_CONF2:0] settings. | | | | | | | | |
| GPIO2[2:0] = Configures GPIO2. 000 = As disabled, high-Z 001 = As ADC and OTUT inputs 010 = As ADC only input 011 = As digital input 100 = As output high 101 = As output low 110 = As ADC input and weak pull-up enabled 111 = As ADC input and weak pull-down enabled | | | | | | | | |
| GPIO1[2:0] = Configures GPIO1. 000 = As disabled, high-Z 001 = As ADC and OTUT inputs 010 = As ADC only input 011 = As digital input 100 = As output high 101 = As output low 110 = As ADC input and weak pull-up enabled 111 = As ADC input and weak pull-down enabled | | | | | | | | |

8.5.4.9.2 GPIO_CONF2

| Address | 0x000F | | | | | | | |
|---|--------|-----------|------------|-------|-------|------------|-------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | SPARE | CS_RDY_EN | GPIO4[2:0] | | | GPIO3[2:0] | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SPARE = Spare | | | | | | | | |
| CS_RDY_EN = Enables GPIO1 as digital output to toggle low when CS ADC conversion is complete. Reset to high when host reads CURRENT_HI register. 0 = No CS ADC toggle function. GPIO1 is configured based on [GPIO1_CONF2:0] setting. 1 = GPIO1 is used for CS ADC conversion toggle function, [GPIO1_CONF2:0] setting is ignored. | | | | | | | | |

GPIO4[2:0] = Configures GPIO4. If [SPI_EN] = 1, these configuration bits are ignored and the pin is used as SS for SPI controller. See [节 8.3.6.1.3](#) for details.

000 = As disabled, high-Z
 001 = As ADC and OTUT inputs
 010 = As ADC only input
 011 = As digital input
 100 = As output high
 101 = As output low
 110 = As ADC input and weak pull-up enabled
 111 = As ADC input and weak pull-down enabled

GPIO3[2:0] = Configures GPIO3.

000 = As disabled, high-Z
 001 = As ADC and OTUT inputs
 010 = As ADC only input
 011 = As digital input
 100 = As output high
 101 = As output low
 110 = As ADC input and weak pull-up enabled
 111 = As ADC input and weak pull-down enabled

8.5.4.9.3 GPIO_CONF3

| Address | 0x0010 | | | | | | | |
|--|------------|-------|------------|-------|-------|-------|------------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | SPARE[1:0] | | GPIO6[2:0] | | | | GPIO5[2:0] | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SPARE[1:0] = Spare | | | | | | | | |
| GPIO6[2:0] = Configures GPIO6. If [SPI_EN] = 1, these configuration bits are ignored and the pin is used as MOSI for SPI controller. See 节 8.3.6.1.3 for details. <p>000 = As disabled, high-Z 001 = As ADC and OTUT inputs 010 = As ADC only input 011 = As digital input 100 = As output high 101 = As output low 110 = As ADC input and weak pull-up enabled 111 = As ADC input and weak pull-down enabled</p> | | | | | | | | |
| GPIO5[2:0] = Configures GPIO5. If [SPI_EN] = 1, these configuration bits are ignored and the pin is used as MISO for SPI controller. See 节 8.3.6.1.3 for details. <p>000 = As disabled, high-Z 001 = As ADC and OTUT inputs 010 = As ADC only input 011 = As digital input 100 = As output high 101 = As output low 110 = As ADC input and weak pull-up enabled 111 = As ADC input and weak pull-down enabled</p> | | | | | | | | |

8.5.4.9.4 GPIO_CONF4

| Address | 0x0011 | | | | | | | |
|--------------------|------------|-------|------------|-------|-------|-------|------------|-------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | SPARE[1:0] | | GPIO8[2:0] | | | | GPIO7[2:0] | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SPARE[1:0] = Spare | | | | | | | | |

GPIO8[2:0] = Configures GPIO8. If *[FAULT_IN_EN]* = 1, these configuration bits are ignored and the pin is used as an input such that an active low will trigger NFAULT.
000 = As disabled, high-Z
001 = As ADC and OTUT inputs
010 = As ADC only input
011 = As digital input
100 = As output high
101 = As output low
110 = As ADC input and weak pull-up enabled
111 = As ADC input and weak pull-down enabled

GPIO7[2:0] = Configures GPIO7. If *[SPI_EN]* = 1, these configuration bits are ignored and the pin is used as SCLK for SPI controller. See [节 8.3.6.1.3](#) for details.
000 = As disabled, high-Z
001 = As ADC and OTUT inputs
010 = As ADC only input
011 = As digital input
100 = As output high
101 = As output low
110 = As ADC input and weak pull-up enabled
111 = As ADC input and weak pull-down enabled

8.5.4.10 SPI Controller

8.5.4.10.1 SPI_CONF

| Address | 0x034D | | | | | | | |
|---|--------|-------|-------|-------------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | CPOL | CPHA | NUMBIT[4:0] | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| CPOL = Sets the SCLK polarity. 0 = Idles low and clocks high 1 = Idles high and clocks low | | | | | | | | |
| CPHA = Sets the edge of SCLK where data is sampled on MISO. 0 = Leading clock transition 1 = Trailing clock transition | | | | | | | | |
| NUMBIT[4:0] = SPI transaction length. Set the number of SPI bits to read/write. 00000 = 24-bit 00001 = 1-bit 00010 = 2-bit : 10111 = 23-bit All others = 23-bit | | | | | | | | |

8.5.4.10.2 SPI_EXE

| Address | 0x0351 | | | | | | | |
|--|--------|-------|-------|-------|-------|---------|-------|--------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | SS_CTRL | | SPI_GO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| RSVD = Reserved | | | | | | | | |
| SS_CTRL = Programs the state of SS. 0 = Output low 1 = Output high | | | | | | | | |
| SPI_GO = Executes the SPI transaction. This bit is self-clearing. 0 = Idle 1 = Execute the SPI | | | | | | | | |

8.5.4.10.3 SPI_TX3, SPI_TX2, and SPI_TX1

| | | | | | | | | |
|---------|------------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x034E to 0x0350 | | | | | | | |
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | DATA[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DATA[7:0] = Data to be used to write to SPI peripheral device. The bits are programmed by using *SPI_CONF[NUMBIT4:0]* and are clocked out of MOSI starting from the LSB *SPI_TX1* -> LSB *SPI_TX2* -> LSB *SPI_TX3*.

8.5.4.10.4 SPI_RX3, SPI_RX2, and SPI_RX1

| | | | | | | | | |
|-----------|-----------------|-------|-------|-------|-------|-------|-------|-------|
| Address | 0x0520 to 0x522 | | | | | | | |
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | DATA[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | R | R | R | R | R | R | R | R |

DATA[7:0] = Data returned from a read during SPI transaction. Updated, starting with LSB *SPI_RX1* -> LSB *SPI_RX2* -> LSB *SPI_RX3*, with the number of bits set by *SPI_CONF[NUMBIT4:0]* clocked in from MISO.

8.5.4.11 Diagnostic Control

8.5.4.11.1 DIAG OTP_CTRL

| | | | | | | | | |
|---------|--------|-------|-------|---------------|------------------|-------|-------|-----------|
| Address | 0x0335 | | | | | | | |
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | FLIP_FACT_CRC | MARGIN_MODE[2:0] | | | MARGIN_GO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RSVD = Reserved

FLIP_FACT_CRC = An enable bit to flip the factory CRC value. This is for factory CRC diagnostic.
 0 = Normal operation. No modification of the factory CRC
 1 = Flip the CRC value. This causes a factory CRC fault, *FAULT OTP[FACT_CRC]*.

MARGIN_MODE[2:0] = Configures OTP Margin read mode:
 0b000 = Normal Read
 0b001 = Reserved
 0b010 = Margin 1 Read
 0b011 to 0b111 = Reserved

MARGIN_GO = Starts OTP Margin test set by the *[MARGIN_MOD]* bit. This bit self-clears and always reads 0.
 0 = Ready
 1 = Start the test

8.5.4.11.2 DIAG_COMM_CTRL

| | | | | | | | | |
|---------|--------|-------|-------|-------|-------|--------------|-------------|-------|
| Address | 0x0336 | | | | | | | |
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | SPI_LOOPBACK | FLIP_TR_CRC | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RSVD = Reserved

SPI_LOOPBACK = Enables SPI loopback function to verify SPI functionality. See the [节 8.3.6.1.3](#) for more details.
 0 = Disable
 1 = Enable

FLIP_TR_CRC = Sends a purposely incorrect communication (during transmitting response) CRC by inverting all of the calculated CRC bits.
0 = Send CRC as calculated
1 = Send inverted CRC

8.5.4.11.3 DIAG_PWR_CTRL

| Address | 0x0337 | | | | | | | |
|---|--------|-------|-------|-------|-------|-------|-------------|-------------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | | BIST_NO_RST | PWR_BIST_GO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| <p>BIST_NO_RST = Use for further diagnostic if the power supply BIST detects a failure. When this bit is set to 1, and then BIST cycle is run using [PWR_BIST_GO], the device will not clear the FAULT_PWR1 and FAULT_PWR2 register, and does not deassert the NFAULT signal at the end of BIST cycle.</p> <p>0 = Cycle through BIST on the LDO comparators. The FAULT_PWR* registers are reset to 0 and NFAULT is deasserted at the end of each LDO BIST run.</p> <p>1 = Cycle through BIST on the LDO comparators. The FAULT_PWR* registers are not reset to 0, and NFAULT remains asserted at the end of each LDO BIST run.</p> | | | | | | | | |
| <p>PWR_BIST_GO = When written to 1, the power supply BIST diagnostic will start. Any change in [BIST_NO_RST] has no effect until this bit is written to 1 again. The bit self-clears.</p> <p>0 = Ready</p> <p>1 = Start power supply BIST diagnostic.</p> | | | | | | | | |

8.5.4.11.4 DIAG_CBFET_CTRL2

| Address | 0x0339 | | | | | | | |
|---|------------------|-------|-------|-------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | CBFET6 to CBFET1 | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <p>CBFET 6to CBFET1 = Enables CBFET for CBFET diagnostic. This register is only sampled when [COMP_ADC_SEL2:0] = 0b100.</p> <p>0 = CBFET off</p> <p>1 = CBFET on;</p> <p>Bit 7 and Bit 6 RSVD</p> | | | | | | | | |

8.5.4.11.5 DIAG_COMP_CTRL1

| Address | 0x033A | | | | | | | |
|---|---------------|-------|-------|-------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | VCCB_THR[4:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <p>VCCB_THR[4:0] = Configures the VCELL vs. AUXCELL delta. The VCELL vs. AUXCELL check is considered pass if the measured delta is less than this threshold. This threshold applies to the bus bar comparison from Main to AUX ADC as well. Range from 6 to 99mV in 3mV step</p> | | | | | | | | |

8.5.4.11.6 DIAG_COMP_CTRL2

| Address | 0x033B | | | | | | | | |
|--|--------|---------------|-------|-------|-------|-------------|-------|-------|--|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| Name | RSVD | GPIO_THR[2:0] | | | | OW_THR[3:0] | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| <p>RSVD = Reserved</p> <p>GPIO_THR[2:0] = Configures the GPIO comparison delta threshold between Main and AUX ADC measurements. Range is from 4-mV to 32-mV in 4-mV steps</p> | | | | | | | | | |

OW_THR[3:0] = Configures the OW detection threshold for diagnostic comparison. This threshold applies to the CB OW and VC OW diagnostics.
 Range is from 500 mV to 5 V in 300-mV steps.

8.5.4.11.7 DIAG_COMP_CTRL3

| Address | 0x033C | | | | | | | |
|---|--------|---------------|-------------|-------|-------|-------------------|-------|-------------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | CBFET_CTRL_GO | OW_SNK[1:0] | | | COMP_ADC_SEL[2:0] | | COMP_ADC_GO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| <p>CBFET_CTRL_GO = When this GO bit = 1, device turns on the CBFET configured and turns off whichever CBFET is clear in DIAG_CBFET_CTRL2 register. This GO action is executed only if CB is not running or it's in pause, otherwise, CBFETs are controlled by regular CB control. If CBFET are turned on by this GO bit, once CB is started or resume, the CBFET controls returns to the regular CB control (and not by this GO bit action)</p> | | | | | | | | |
| <p>OW_SNK[1:0] = Turns on current sink on VC pins, CB pins. Changes to these bits take effect immediately. Host MCU is responsible to turn on the correct sink current before performing open wire (OW) test and to turn off the sink current after OW test is completed. 00 = All VC, , CB pins current sink is off. SRP/N current source is off 01 = Turn on current sink on all VC pins 10 = Turn on current sink on all CB pins 11 = Turn on current source on SRP/N pins</p> | | | | | | | | |
| <p>COMP_ADC_SEL[2:0] = Enables the device diagnostic comparison through the ADC measurements. Host enables the corresponding ADCs in continuous mode before enabling this diagnostic. These bits are sampled when [COMP_ADC_GO] = 1. 000 = No ADC comparison is performed 001 = Cell voltage measurement check. Device compares the cell channels specified by [AUX_CELL_SEL4:0] against the following criteria: VCELL (from Main ADC) vs. AUXCELL (from AUX ADC) delta is less than [VCCB_THR4:0]. The [DRDY_VCCB] = 1 when this comparison is completed. 010 = Open wire (OW) check on VC pins. MCU enables the current sink on all VC pins through the [OW_SNK1:0] before enabling this comparison. Device compares corresponding VC pins specified by ACTIVE_CELL register against the following criteria: VCELL (from Main ADC) is less than DIAG_COMP_CTRL2 [OW_THR3:0]. The [DRDY_VC_OW] = 1 when the comparison is completed. 011 = Open wire (OW) check on CB pins MCU enables the current sink on all VC pins through the [OW_SNK1:0] before enabling this comparison. Device compares corresponding CB pins specified by [AUX_CELL_SEL4:0] against the following criteria: AUXCELL (from AUX ADC) is less than DIAG_COMP_CTRL2 [OW_THR3:0]. The [DRDY_CBOW] = 1 when the comparison is completed. 100 = CBFET check. MCU preconfigures the following before starting this check:<ul style="list-style-type: none"> Pause cell balancing if balancing is enabled. Enable the CBFET configured by DIAG_CBFET_CTRL2 register. Configure the [EXTD_CBFET] to decide if all CBFET returns to pause state (that is, turn off all CBFET) or remains their status as specified by DIAG_CBFET_CTRL2 register. When this test starts, device will turn on CBFET specified by DIAG_CBFET_CTRL2 register and then compares the channel specified by [AUX_CELL_SEL4:0] with the following criteria: AUXCELL (from AUX ADC) < 1/3 of VCELL (from Main ADC). [DRDY_CBFET] = 1 when the comparison is completed. 101 = GPIO measurement check (applies to GPIO configured as ADC and OTUT inputs or ADC only input). Device compares main GPIO measurement vs. AUX GPIO measurements delta is less than [GPIO_THR2:0]. The [DRDY_GPIO] = 1 when the comparison is completed. Other codes: No ADC comparison is performed</p> | | | | | | | | |

COMP_ADC_GO = Device starts diagnostic test specified by [COMP_ADC_SEL2:0] setting. When this bit is written to 1, the selected [COMP_ADC_SEL2:0] is sampled. Change of [COMP_ADC_SEL2:0] setting has no effect unless this GO bit is written to 1 again.
This bit is cleared to 0 in read.
0 = Ready. Writing 0 has no effect
1 = Start diagnostic selected by [COMP_ADC_SEL2:0]

8.5.4.11.8 DIAG_COMP_CTRL4

| Address | 0x033D | | | | | | | |
|---|--------|-------|-------|-------|-------|-------|----------------|---------------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | | COMP_FAULT_INJ | LPF_FAULT_INJ |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| <p>COMP_FAULT_INJ = Injects fault to the ADC comparison logic. If any ADC comparison diagnostic is run with this bit set, the comparison result is expected to fail. 0 = Disable 1 = Enable</p> | | | | | | | | |
| <p>LPF_FAULT_INJ = Injects fault condition to the diagnostic LPF during LPF diagnostic. The FAULT_COMP_MISC[LPF_FAIL] is expected to be set. 0 = Disable 1 = Enable</p> | | | | | | | | |

8.5.4.11.9 DIAG_PROT_CTRL

| Address | 0x033E | | | | | | | |
|--|--------|-------|-------|-------|-------|-------|------------------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | | PROT_BIST_NO_RST | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| <p>PROT_BIST_NO_RST = Use for further diagnostic if the protector BIST detects a failure. When this bit is set to 1, the device will not clear the FAULT_OV2, FAULT_UV2, FAULT_OT, and FAULT_UT registers. The NFAULT signal will be latched once it is asserted. Note: Host ensures there is no fault before starting the BIST run with this bit set to 0. 0 = During BIST run, when the device asserts a fault to check the protector comparators and MUX and asserts the correct OV, UV, OT, and UT fault bits the NFAULT pin. When this bit is 0, the device clears the fault and deasserts NFAULT before switching to the next channel. 1 = During BIST run, the fault created during the test will not be cleared before switching to next cell or GPIO channel. The NFAULT pin is latched once it is asserted.</p> | | | | | | | | |

8.5.4.12 Fault Configuration and Reset

8.5.4.12.1 FAULT_MSK1

| Address | 0x0016 | | | | | | | |
|--|----------|--------|--------|--------|--------|----------|---------|---------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | MSK_PROT | MSK_UT | MSK_OT | MSK_UV | MSK_OV | MSK_COMP | MSK_SYS | MSK_PWR |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <p>MSK_PROT = Masks the FAULT_PROT* registers to trigger NFAULT. 0 = Assert NFAULT if any bit from FAULT_PROT* is set to 1. 1 = No NFAULT action regardless of FAULT_PROT* bit status.</p> | | | | | | | | |
| <p>MSK_UT = Masks the FAULT_UT* registers to trigger NFAULT. 0 = Assert NFAULT if any bit from FAULT_UT* is set to 1. 1 = No NFAULT action regardless of FAULT_UT* bit status.</p> | | | | | | | | |
| <p>MSK_OT = Masks the FAULT_OT* registers to trigger NFAULT. 0 = Assert NFAULT if any bit from FAULT_OT* is set to 1. 1 = No NFAULT action regardless of FAULT_OT* bit status.</p> | | | | | | | | |

| | |
|----------|--|
| MSK_UV | Masks the <i>FAULT_UV*</i> registers to trigger NFAULT. 0 = Assert NFAULT if any bit from <i>FAULT_UV*</i> is set to 1. 1 = No NFAULT action regardless of <i>FAULT_UV*</i> bit status. |
| MSK_OV | Masks the <i>FAULT_OV*</i> registers to trigger NFAULT. 0 = Assert NFAULT if any bit from <i>FAULT_OV*</i> is set to 1. 1 = No NFAULT action regardless of <i>FAULT_OV*</i> bit status. |
| MSK_COMP | Masks the <i>FAULT_COMP_*</i> registers to trigger NFAULT. 0 = Assert NFAULT if any bit from <i>FAULT_COMP_*</i> is set to 1. 1 = No NFAULT action regardless of <i>FAULT_COMP_*</i> bit status. |
| MSK_SYS | To mask the NFAULT assertion from any <i>FAULT_SYS</i> register bit. 0 = Assert NFAULT if any bit from <i>FAULT_SYS</i> is set to 1. 1 = No NFAULT action regardless of <i>FAULT_SYS</i> bit status. |
| MSK_PWR | To mask the NFAULT assertion from any <i>FAULT_PWR1</i> to <i>FAULT_PWR3</i> register bit. 0 = Assert NFAULT if any bit from <i>FAULT_PWR1</i> to <i>FAULT_PWR3</i> is set to 1. 1 = No NFAULT action regardless of <i>FAULT_PWR1</i> to <i>FAULT_PWR3</i> bit status. |

8.5.4.12.2 FAULT_MSK2

| Address | 0x0017 | | | | | | | |
|---|----------|------------------|-------------------|-------|-------|-------|-------|-----------|
| NVM | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | SPARE[1] | MSK OTP _ CRC | MSK OTP _ DATA | RSVD | RSVD | RSVD | RSVD | MSK COMM1 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SPARE[1] = Spare | | | | | | | | |
| MSK OTP_CRC = Masks the <i>FAULT_OTP</i> register ([<i>CUST_CRC</i>] and [<i>FACT_CRC</i>] only) on NFAULT triggering. 0 = Assert NFAULT if any bit described above is set to 1. 1 = No NFAULT action regardless of the status of the bits described above. | | | | | | | | |
| MSK OTP DATA = Masks the <i>FAULT_OTP</i> register (all bits except [<i>CUST_CRC</i>] and [<i>FACT_CRC</i>]) on NFAULT triggering. 0 = Assert NFAULT if any bit described above is set to 1. 1 = No NFAULT action regardless of the status of the bits described above. | | | | | | | | |
| RSVD = Reserved | | | | | | | | |
| RSVD = Reserved | | | | | | | | |
| RSVD = Reserved | | | | | | | | |
| RSVD = Reserved | | | | | | | | |
| MSK COMM1 = Masks <i>FAULT_COMM1</i> register on NFAULT triggering. 0 = Assert NFAULT if any bit from <i>FAULT_COMM1</i> register is set to 1. 1 = No NFAULT action regardless of <i>FAULT_COMM1</i> register bit status. | | | | | | | | |

8.5.4.12.3 FAULT_RST1

| Address | 0x0331 | | | | | | | |
|---|----------|--------|--------|--------|--------|----------|---------|---------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RST_PROT | RST_UT | RST_OT | RST_UV | RST_OV | RST_COMP | RST_SYS | RST_PWR |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RST_PROT = Resets the <i>FAULT_PROT1</i> and <i>FAULT_PROT2</i> registers to 0x00. 0 = No reset 1 = Reset registers to 0x00 | | | | | | | | |
| RST_UT = Resets all <i>FAULT_UT</i> registers to 0x00. 0 = No reset 1 = Reset registers to 0x00 | | | | | | | | |
| RST_OT = Resets all <i>FAULT_OT</i> registers to 0x00. 0 = No reset 1 = Reset registers to 0x00 | | | | | | | | |
| RST_UV = Resets all <i>FAULT_UV*</i> registers to 0x00. 0 = No reset 1 = Reset registers to 0x00 | | | | | | | | |

| | | | | | | | | |
|--|--|--|--|--|--|--|--|--|
| <p>RST_OV = Resets all <i>FAULT_OV</i>* registers to 0x00. 0 = No reset 1 = Reset registers to 0x00</p> | | | | | | | | |
| <p>RST_COMP = Resets all <i>FAULT_COMP</i>* registers to 0x00. 0 = No reset 1 = Reset registers to 0x00</p> | | | | | | | | |
| <p>RST_SYS = To reset the <i>FAULT_SYS</i> register to 0x00. This bit self-clears to 0 after writing to 1. 0 = Do not reset 1 = Reset to 0x00</p> | | | | | | | | |
| <p>RST_PWR = To reset the <i>FAULT_PWR1</i> to <i>FAULT_PWR3</i> registers to 0x00. This bit self-clears to 0 after writing to 1. 0 = Do not reset 1 = Reset to 0x00</p> | | | | | | | | |

8.5.4.12.4 FAULT_RST2

| Address | 0x0332 | | | | | | | |
|--|--------------|-----------------|------------------|--------------|--------------|--------------|--------------|--------------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | RST OTP _CRC | RST OTP _DATA | RSVD | RSVD | RSVD | RSVD | RST_COMM1 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| <p>RST_OTP_CRC = Resets the <i>FAULT_OTP</i> register (<i>[CUST_CRC]</i> and <i>[FACT_CRC]</i> only). 0 = No reset 1 = Reset the register to 0x00</p> | | | | | | | | |
| <p>RST_OTP_DATA = Resets the <i>FAULT_OTP</i> register (<i>[SEC_DETECT]</i> and <i>[DED_DETECT]</i> only). 0 = No reset 1 = Reset the register to 0x00</p> | | | | | | | | |
| RSVD= Reserved | | | | | | | | |
| RSVD= Reserved | | | | | | | | |
| RSVD= Reserved | | | | | | | | |
| RSVD= Reserved | | | | | | | | |
| <p>RST_COMM1 = Resets <i>FAULT_COMM1</i> and <i>DEBUG_COMM_UART</i>* registers. 0 = No reset 1 = Reset registers to 0x00</p> | | | | | | | | |

8.5.4.13 Fault Status

8.5.4.13.1 FAULT_SUMMARY

This register is the soft version of the NFAULT.

| Address | 0x052D | | | | | | | |
|---|----------------|-------------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | FAULT_PRO T | FAULT COMP_ADC | FAULT_OTP | FAULT_COMM | FAULT_OTUT | FAULT_OVUV | FAULT_SYS | FAULT_PWR |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <p>FAULT_PROT = This bit is set if <i>[MSK_PROT]</i> = 0 and any of the <i>FAULT_PROT1</i> or <i>FAULT_PROT2</i> register bits is set. 0 = No protector (OVUV, OTUT comparators) fault. 1 = Protector fault is detected</p> | | | | | | | | |

| | |
|---|---|
| FAULT_COMP_ADC = This bit is set if $[MSK_COMP] = 1$ and any of the following registers is set: | |
| | <ul style="list-style-type: none"> • $FAULT_COMP_VCCB2$ • $FAULT_COMP_VCOW2$ • $FAULT_COMP_CBOW2$ • $FAULT_COMP_CBFET2$ • $FAULT_COMP_GPIO$ • $FAULT_COMP_MISC$ |
| 0 = No ADC comparison fault (that is, none of the $FAULT_COMP_*$ registers are set). 1 = ADC comparison fault is detected. | |
| FAULT_OTP = | This bit is set if $[MSK_OTP] = 0$ and any of the $FAULT_OTP$ register bits is set. 0 = No OTP-related fault detected or OTP faults are masked. 1 = OTP-related fault is detected. |
| FAULT_COMM = | This bit is set if any of the following is true: <ul style="list-style-type: none"> • $[MSK_COMM1] = 0$ and any of the $FAULT_COMM1$ register bits is set. 0 = No UART fault is detected, or UART fault is masked. 1 = UART fault is detected. |
| FAULT_OTUT = | This bit is set if any of the following is true: <ul style="list-style-type: none"> • $[MSK_OT] = 0$ and any of the $FAULT_OT2$ bits is set. • $[MSK_UT] = 0$ and any of the $FAULT_UT2$ bits is set. 0 = No OT or UT fault is detected, or OT and UT faults are masked. 1 = OT or UT fault is detected |
| FAULT_OVUV = | This bit is set if any of the following is true: <ul style="list-style-type: none"> • $[MSK_OV] = 0$ and any of the $FAULT_OV1$ or $FAULT_OV2$ bits is set. • $[MSK_UV] = 0$ and any of the $FAULT_UV1$ or $FAULT_UV2$ bits is set. 0 = No OV or UV fault is detected, or OV and UV faults are masked. 1 = OV or UV fault is detected. |
| FAULT_SYS = | This bit is set if $[MSK_SYS] = 0$ and any of the $FAULT_SYS$ register bits is set. 0 = No system related fault detected or system faults are masked. 1 = System related fault is detected. |
| FAULT_PWR = | This bit is set if $[MSK_PWR] = 0$ and any of the $FAULT_PWR1$ to $FAULT_PWR3$ register bits is set. 0 = No power rail related fault is detected or power rail faults are masked. 1 = Power rail related fault is detected. |

8.5.4.13.2 FAULT_COMM1

| Address | 0x0530 | | | | | | | |
|---|--------|-------|-------|---------|---------|---------|-------------|----------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | UART_TR | UART_RR | UART_RC | COMMCLR_DET | STOP_DET |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| UART_TR = Indicates a UART FAULT is detected when transmitting a response frame. Further details of the fault information are available in the <i>DEBUG_UART_RR_TR</i> register. 0 = No fault 1 = Fault | | | | | | | | |
| UART_RR = Indicates a UART FAULT is detected when receiving a response frame. Further details of the fault information are available in the <i>DEBUG_UART_RR_TR</i> register. 0 = No fault 1 = Fault | | | | | | | | |
| UART_RC = Indicates a UART FAULT is detected during receiving a command frame. Further details of the fault information are available in the <i>DEBUG_UART_RC</i> register. 0 = No fault 1 = Fault | | | | | | | | |

| |
|--|
| COMMCLR_DET = A UART communication clear signal is detected. A detection of SLEEPtoACTIVE ping in ACTIVE or SLEEP mode or detection of WAKE pin in ACTIVE mode will also set this bit. 0 = No UART Clear 1 = UART Clear detected |
| STOP_DET = Indicates an unexpected STOP condition is received. A detection of SLEEPtoACTIVE signal in ACTIVE mode will also set this bit. 0 = No fault 1 = Fault |

8.5.4.13.3 FAULT OTP

| Address | 0x0535 | | | | | | | |
|--|--------|---------|---------|----------|----------|-----------|-----------|----------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | DED_DET | SEC_DET | CUST_CRC | FACT_CRC | CUSTLDERR | FACTLDERR | GBLOVERR |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| DED_DET = Indicates a DED error has occurred during the OTP load. (Unknown during encoding) 0 = No fault 1 = Fault | | | | | | | | |
| SEC_DET = Indicates a SEC error has occurred during the OTP load. (Unknown during encoding) 0 = No fault 1 = Fault | | | | | | | | |
| CUST_CRC = Indicates a CRC error has occurred in the customer register space. 0 = No fault 1 = Fault | | | | | | | | |
| FACT_CRC = Indicates a CRC error has occurred in the factory register space. 0 = No fault 1 = Fault | | | | | | | | |
| CUSTLDERR = Indicates errors during the customer space OTP load process. Read <i>OTP_CUST1_STAT</i> and <i>OTP_CUST2_STAT</i> registers for the specific error condition. This error bit is set if one of the following is true: <ul style="list-style-type: none">• No Customer OTP page is programmed.• The highest Customer OTP page has a <i>[FMTERR]</i>.• The highest Customer OTP page has <i>[TRY]</i> = 1 and is not <i>[PROGOK]</i>.• LOADERR happened on the selected Customer OTP page. Information received from the device with this error must not be considered reliable. Writing <i>[RST OTP DATA]</i> = 1 does not reset this bit. To recheck this error, a device reset or HW_RESET is needed. 0 = No fault 1 = Fault | | | | | | | | |
| FACTLDERR = Indicates errors during the factory space OTP load process. This error bit is set if one of the following is true: <ul style="list-style-type: none">• No factory OTP page is programmed.• The highest factory OTP page has a <i>[FMTERR]</i>.• The highest factory OTP page has <i>[TRY]</i> = 1 and is not <i>[PROGOK]</i>.• LOADERR happened on the selected factory OTP page. Information received from the device with this error must not be considered reliable. Writing <i>[RST OTP DATA]</i> = 1 does not reset this bit. To recheck this error, a device reset or HW_RESET is needed. 0 = No fault 1 = Fault | | | | | | | | |

GBLOVERR = Indicates that an overvoltage error is detected on one of the OTP pages. Read *OTP_CUST1_STAT* and *OTP_CUST2_STAT* registers to determine the specific page(s). Information received from the device with this error must not be considered reliable.
 Writing *[RST_OTP_DATA]* = 1 does not reset this bit. To clear this bit, a device reset or *HW_RESET* is needed.
 Repeat the programming procedure on a different page (if available) will force the device to re-evaluate the condition.
 0 = No fault
 1 = Fault

8.5.4.13.4 FAULT_SYS

| Address | 0x0536 | | | | | | | |
|---|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | LFO | RSVD | GPIO | DRST | CTL | CTS | TSHUT | TWARN |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| LFO = Indicated LFO frequency is outside an expected range 0 = No fault detected 1 = Fault detected | | | | | | | | |
| RSVD = Reserved | | | | | | | | |
| GPIO = Indicates GPIO8 detects a FAULT input when <i>GPIO_CONF1[FAULT_IN_EN]</i> = 1. 0 = No fault detected 1 = FAULT input detected | | | | | | | | |
| DRST = Indicates a digital reset has occurred. 0 = No digital reset 1 = Digital reset has occurred | | | | | | | | |
| CTL = Indicates a long communication timeout occurred. Device action is configured by <i>[CTL_ACT]</i> . This bit is not observable if the action is set to device shutdown. 0 = No fault 1 = Long communication timeout occurs. Observable if long timeout action is set to SLEEP. | | | | | | | | |
| CTS = Indicates a short communication timeout occurred. No action from the device. This can be served as an alert to system before reaching long communication timeout. 0 = No fault 1 = Short communication timeout occurs | | | | | | | | |
| TSHUT = Indicates the previous shutdown was a thermal shutdown, in which the die temperature (die temp 2) is higher than the thermal shutdown threshold. 0 = Die temperature is less than thermal shutdown threshold 1 = The previous shutdown was a thermal shutdown | | | | | | | | |
| TWARN = Indicates the die temperature (die temp 2) is higher than the <i>TWARN_THR[1:0]</i> setting. No action is taken by the device at the moment yet. This serves as a warning signal that the die temperature is approaching thermal shutdown. 0 = Die temperature is less than <i>TWARN_THR[1:0]</i> 1 = Die temperature is greater than <i>TWARN_THR[1:0]</i> | | | | | | | | |

8.5.4.13.5 FAULT_PROT1

| Address | 0x053A | | | | | | | |
|-----------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | | | TPARITY_FAIL |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |

TPARITY_FAIL = Indicates a parity fault is detected on any of the following OTUT related configurations:

- OT or UT threshold setting
- *[OTUT_MODE1:0]* setting
- *GPIO_CONF1...4* settings

0 = No fault
1 = Fault

VPARITY_FAIL = Indicates a parity fault is detected on any of the following OVUV related configurations:

- OV or UV threshold setting
- *[OVUV_MODE1:0]* setting
- *[NUM_CELL3:0]* setting

0 = No fault
1 = Fault

8.5.4.13.6 FAULT_PROT2

| Address | 0x053B | | | | | | | |
|--|--------|------------|------------|------------|-------------|-------------|-------------|-------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | BIST_ABORT | TPATH_FAIL | VPATH_FAIL | UTCOMP_FAIL | OTCOMP_FAIL | OVCOMP_FAIL | UVCOMP_FAIL |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| BIST_ABORT = Indicates either OVUV or OTUT BIST run is aborted. 0 = BIST runs to completion 1 = BIST abort | | | | | | | | |
| TPATH_FAIL = Indicates a fault is detected along the OTUT signal path during BIST test. 0 = No fault 1 = Fault | | | | | | | | |
| VPATH_FAIL = Indicates a fault is detected along the OVUV signal path during BIST test. 0 = No fault 1 = Fault | | | | | | | | |
| UTCOMP_FAIL = Indicates the UT comparator fails during BIST test. 0 = No fault 1 = Fault | | | | | | | | |
| OTCOMP_FAIL = Indicates the OT comparator fails during BIST test. 0 = No fault 1 = Fault | | | | | | | | |
| OVCOMP_FAIL = Indicates the OV comparator fails during BIST test. 0 = No fault 1 = Fault | | | | | | | | |
| UVCOMP_FAIL = Indicates the UV comparator fails during BIST test. 0 = No fault 1 = Fault | | | | | | | | |

8.5.4.13.7 FAULT_OV2

| Address | 0x053D | | | | | | | |
|--|--------|-------|---------|---------|---------|---------|---------|---------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | RSVD | OV6_DET | OV5_DET | OV4_DET | OV3_DET | OV2_DET | OV1_DET |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| OV1_DET to OV6_DET = OV fault status for Cell1 to Cell6, results are from the OV comparator detection. | | | | | | | | |

8.5.4.13.8 FAULT_UV2

| Address | 0x053F | | | | | | | |
|-----------|--------|-------|---------|---------|---------|---------|---------|---------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | RSVD | UV6_DET | UV5_DET | UV4_DET | UV3_DET | UV2_DET | UV1_DET |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

UV1_DET to UV6_DET = UV fault status for Cell1 to Cell6, results are from the UV comparator detection.

8.5.4.13.9 FAULT_OT

| Address | 0x0540 | | | | | | | |
|-----------|---------|---------|---------|---------|---------|---------|---------|---------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | OT8_DET | OT7_DET | OT6_DET | OT5_DET | OT4_DET | OT3_DET | OT2_DET | OT1_DET |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

OT1_DET to OT8_DET = OT fault status for GPIO1 to GPIO8, results are from the OT comparator detection.

8.5.4.13.10 FAULT_UT

| Address | 0x0541 | | | | | | | |
|-----------|---------|---------|---------|---------|---------|---------|---------|---------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | UT8_DET | UT7_DET | UT6_DET | UT5_DET | UT4_DET | UT3_DET | UT2_DET | UT1_DET |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

UT1_DET to UT8_DET = UT fault status for GPIO1 to GPIO8, results are from the UT comparator detection.

8.5.4.13.11 FAULT_COMP_GPIO

| Address | 0x0543 | | | | | | | |
|-----------|------------|------------|------------|------------|------------|------------|------------|------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | GPIO8_FAIL | GPIO7_FAIL | GPIO6_FAIL | GPIO5_FAIL | GPIO4_FAIL | GPIO3_FAIL | GPIO2_FAIL | GPIO1_FAIL |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

GPIO1_FAIL to Indicates ADC vs. AUX ADC GPIO measurement diagnostic results for GPIO1 to GPIO8.

GPIO8_FAIL = 0 = Diagnostic pass

1 = Diagnostic fail. GPIO from Main ADC vs. AUX ADC measurement is greater than [GPIO_THR2:0]

8.5.4.13.12 FAULT_COMP_VCCB2

| Address | 0x0546 | | | | | | | |
|-----------|--------|-------|------------|------------|------------|------------|------------|------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | RSVD | CELL6_FAIL | CELL5_FAIL | CELL4_FAIL | CELL3_FAIL | CELL2_FAIL | CELL1_FAIL |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

CELL1_FAIL to Indicates voltage diagnostic results for cell1 to cell6.

CELL6_FAIL = 0 = Diagnostic pass

1 = Diagnostic fail. VCELL vs. AUXCELL measurement is greater than [VCCB_THR4:0]

8.5.4.13.13 FAULT_COMP_VCOW2

| Address | 0x0549 | | | | | | | |
|-----------|--------|-------|------------|------------|------------|------------|------------|------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | RSVD | VCOW6_FAIL | VCOW5_FAIL | VCOW4_FAIL | VCOW3_FAIL | VCOW2_FAIL | VCOW1_FAIL |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VCOW1_FAIL to Indicates VC OW diagnostic results for cell1 to cell 6.
 VCOW6_FAIL = 0 = Diagnostic pass
 1 = Diagnostic fail. VCELL measurement is less than [OW_THR3:0]

8.5.4.13.14 FAULT_COMP_CBOW2

| Address | 0x054C | | | | | | | |
|--|--------|-------|------------|------------|------------|------------|------------|------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | RSVD | CBOW6_FAIL | CBOW5_FAIL | CBOW4_FAIL | CBOW3_FAIL | CBOW2_FAIL | CBOW1_FAIL |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CBOW1_FAIL to Results of the CB OW diagnostic for CB FET1 to CB FET6. CBOW6_FAIL = 0 = Pass 1 = Fail | | | | | | | | |

8.5.4.13.15 FAULT_COMP_CBFET2

| Address | 0x054F | | | | | | | |
|---|--------|-------|-------------|-------------|-------------|-------------|-------------|-------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | RSVD | CBFET6_FAIL | CBFET5_FAIL | CBFET4_FAIL | CBFET3_FAIL | CBFET2_FAIL | CBFET1_FAIL |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CBFET1_FAIL to Results of the CB FET diagnostic for CB FET1 to CB FET6. CBFET6_FAIL = 0 = Pass 1 = Fail | | | | | | | | |

8.5.4.13.16 FAULT_COMP_MISC

| Address | 0x0550 | | | | | | | |
|--|--------|-------|-------|-------|-------|-------|----------------|----------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | | COMP_ADC_ABORT | LPF_FAIL |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved COMP_ADC_ABORT = Indicates the most recent ADC comparison diagnostic is aborted due to improper setting. Valid only if one of the ADC comparison diagnostics has started. 0 = ADC comparison diagnostic run to completion 1 = ADC comparison diagnostic is aborted LPF_FAIL = Indicates LPF diagnostic result. 0 = Pass 1 = Fail | | | | | | | | |

8.5.4.13.17 FAULT_PWR1

| Address | 0x0552 | | | | | | | |
|--|------------|-----------|------------|---------|---------|---------|----------|---------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | CVSS_OPE_N | DVSS_OPEN | REFHM_OPEN | CVDD_UV | CVDD_OV | DVDD_OV | AVDD_OSC | AVDD_OV |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CVSS_OPEN = Indicates an open condition on CVSS pin. 0 = No fault 1 = Fault DVSS_OPEN = Indicates an open condition on DVSS pin. 0 = No fault 1 = Fault | | | | | | | | |

| | | | | | | | | |
|------------|--|--|--|--|--|--|--|--|
| REFHM_OPEN | Indicates an open condition on REFHM pin. 0 = No fault 1 = Fault | | | | | | | |
| CVDD_UV | Indicates an undervoltage fault on the CVDD LDO. 0 = No fault 1 = Fault | | | | | | | |
| CVDD_OV | Indicates an overvoltage fault on the CVDD LDO. 0 = No fault 1 = Fault | | | | | | | |
| DVDD_OV | Indicates an overvoltage fault on the DVDD LDO. 0 = No fault 1 = Fault | | | | | | | |
| AVDD_OSC | Indicates AVDD is oscillating outside of acceptable limits. 0 = No fault 1 = Fault This fault could trigger when transitioning from SLEEP to ACTIVE mode. So, if this fault is set, please ignore it and reset the fault. | | | | | | | |
| AVDD_OV | Indicates an overvoltage fault on the AVDD LDO. 0 = No fault 1 = Fault | | | | | | | |

8.5.4.13.18 FAULT_PWR2

| Address | 0x0553 | | | | | | | |
|---|--------|--------------|-------|----------|----------|-----------|----------|----------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | PWRBIST_FAIL | RSVD | REFH_OSC | NEG5V_UV | TSREF_OSC | TSREF_UV | TSREF_OV |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| PWRBIST_FAIL = Indicates a fail on the power supply BIST run. 0 = No fault 1 = Fault | | | | | | | | |
| REFH_OSC = Indicates REGH reference is oscillating outside of an acceptable limit. 0 = No fault 1 = Fault | | | | | | | | |
| NEG5V_UV = Indicates an undervoltage fault on the NEG5V charge pump. 0 = No fault 1 = Fault | | | | | | | | |
| TSREF_OSC = Indicates TSREF is oscillating outside of an acceptable limit. 0 = No fault 1 = Fault | | | | | | | | |
| TSREF_UV = Indicates an undervoltage fault on the TSREF LDO. 0 = No fault 1 = Fault | | | | | | | | |
| TSREF_OV = Indicates an overvoltage fault on the TSREF LDO. 0 = No fault 1 = Fault | | | | | | | | |

8.5.4.13.19 FAULT_PWR3

| Address | 0x0554 | | | | | | | |
|-----------------|--------|-------|-------|-------|-------|-------|-------|-------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | RSVD | RSVD | AVDDUV_DRST |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |

| | | | | | | | | |
|-------------|---|--|--|--|--|--|--|--|
| AVDDUV_DRST | = Indicates a digital reset occurred due to AVDD UV detected. This also applies when device wakes up after a SHUTDOWN or HW Reset event. 0 = No reset 1 = Digital reset occurred due to AVDD UV | | | | | | | |
|-------------|---|--|--|--|--|--|--|--|

8.5.4.14 Debug Control and Status

8.5.4.14.1 DEBUG_UART_RC

| Address | 0x0781 | | | | | | | |
|---|--------|-------|---------|----------|--------|-------------|-------|--------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | RC_IERR | RC_TXDIS | RC_SOF | RC_BYTE_ERR | RSVD | RC_CRC |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| <p>RC_IERR = Detects initialization byte error in the received command frame. This may be due to the frame initialization byte has a stop error, incorrect frame type is set, or reserved command type bit is set. All bytes that follow are ignored until a communication CLEAR is received.</p> <p>When a communication frame is ignored, the device will not attempt to detect any communication error in the ignored frame nor counting it as valid/discard in the frame counters.</p> <p>0 = No error 1 = Error detected</p> | | | | | | | | |
| <p>RC_TXDIS = Detects if UART TX is disabled, but the host MCU has issued a command to read data from the device.</p> <p>0 = No error 1 = Error detected</p> | | | | | | | | |
| <p>RC_SOF = Detects a start-of-frame (SOF) error. That is, an UART CLEAR is received on the UART before the current frame is finished.</p> <p>0 = No error 1 = Error detected</p> | | | | | | | | |
| <p>RC_BYTE_ERR = Detects any byte error, other than the error in the initialization byte, in the received command frame. All bytes that follow are ignored until a communication CLEAR is received.</p> <p>When a communication frame is ignored, the device will not attempt to detect any communication error in the ignored frame nor counting it as valid/discard in the frame counters.</p> <p>0 = No error 1 = Error detected</p> | | | | | | | | |
| RSVD = Reserved | | | | | | | | |
| <p>RC_CRC = Detects a CRC error in the received command frame from UART. The frame will be considered as discarded frame.</p> <p>0 = No error 1 = Error detected</p> | | | | | | | | |

8.5.4.14.2 DEBUG_UART_RR_TR

| Address | 0x0782 | | | | | | | |
|---|--------|-------|-------|--------|---------|--------|-------------|--------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | TR_SOF | TR_WAIT | RR_SOF | RR_BYTE_ERR | RR_CRC |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| <p>TR_SOF = Indicates that a UART CLEAR is received while the device is still transmitting data.</p> <p>0 = No error 1 = Error detected</p> | | | | | | | | |

| | | | | | | | | |
|--|--|--|--|--|--|--|--|--|
| TR_WAIT = The device is waiting for its turn to transfer a response out but the action is terminated because either: | | | | | | | | |
| <ul style="list-style-type: none"> • The device receives a UART CLEAR signal. • The device receives a new command. | | | | | | | | |
| 0 = No error | | | | | | | | |
| 1 = Error detected | | | | | | | | |
| RR_SOF = Indicates a UART CLEAR is received while receiving the response frame. Response frames on the UART only apply in multidrop mode. | | | | | | | | |
| 0 = No error | | | | | | | | |
| 1 = Error detected | | | | | | | | |
| RR_BYTE_ERR = Detects any byte error, other than the error in the initialization byte, in the received response frame. All bytes that follow are ignored until a communication CLEAR is received. When a communication frame is ignored, the device will not attempt to detect any communication error in the ignored frame nor counting it as valid/discard in the frame counters. | | | | | | | | |
| 0 = No error | | | | | | | | |
| 1 = Error detected | | | | | | | | |
| RR_CRC = Detects are CRC error in the received response frame from UART. The frame will be considered as a discarded frame. | | | | | | | | |
| 0 = No error | | | | | | | | |
| 1 = Error detected | | | | | | | | |

8.5.4.14.3 DEBUG_UART_DISCARD

| Address | 0x0789 | | | | | | | |
|---|------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | COUNT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| COUNT[7:0] = UART frame counter to track the number of discard frames received or transmitted. The registers of the DEBUG_UART_DISCARD and DEBUG_UART_VALID* are latched and the related counters are reset when this register is read. | | | | | | | | |

8.5.4.14.4 DEBUG_UART_VALID_HI/LO

DEBUG_UART_VALID_HI

| Address | 0x078C | | | | | | | |
|--|------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | COUNT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| COUNT[7:0] = The high-byte of UART frame counter to track the number of valid frames received or transmitted. Counter saturates when both DEBUG_UART_VALID_HI/LO is 0xFF. This register is latched and the related counter is reset when DEBUG_UART_DISCARD is read. | | | | | | | | |

DEBUG_UART_VALID_LO

| Address | 0x078D | | | | | | | |
|---|------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | COUNT[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| COUNT[7:0] = The low-byte of UART frame counter to track the number of valid frames received or transmitted. Counter saturates when both DEBUG_UART_VALID_HI/LO is 0xFF. This register is latched and the related counter is reset when DEBUG_UART_DISCARD is read. | | | | | | | | |

8.5.4.14.5 DEBUG OTP SEC_BLK

| Address | 0x07A0 | | | | | | | |
|--|------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | BLOCK[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BLOCK[7:0] = Holds last OTP block address where SEC occurred. Valid only when <i>FAULT OTP[SEC DET]</i> = 1. | | | | | | | | |

8.5.4.14.6 DEBUG OTP DED_BLK

| Address | 0x07A1 | | | | | | | |
|--|------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | BLOCK[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BLOCK[7:0] = Holds last OTP block address where DED occurred. Valid only when <i>FAULT OTP[DED DET]</i> = 1. | | | | | | | | |

8.5.4.15 OTP Programming Control and Status

8.5.4.15.1 OTP_PROG_UNLOCK1A through OTP_PROG_UNLOCK1D

| Address | 0x0300 to 0x0303 | | | | | | | |
|--|------------------|-------|-------|-------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | CODE[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CODE[7:0] = The first 32-bit OTP programming unlock code is required as part of the OTP programming unlock sequence before performing OTP programming. This 32-bit code is entered in the sequence from <i>OTP_PROG_UNLOCK1A</i> to <i>OTP_PROG_UNLOCK1D</i> . These registers always read back 0. | | | | | | | | |

8.5.4.15.2 OTP_PROG_UNLOCK2A through OTP_PROG_UNLOCK2D

| Address | 0x0352 to 0x0355 | | | | | | | |
|---|------------------|-------|-------|-------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | CODE[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CODE[7:0] = The second 32-bit OTP programming unlock code, required as part of the OTP programming unlock sequence before performing OTP programming. This 32-bit code is entered in the sequence from <i>OTP_PROG_UNLOCK2A</i> to <i>OTP_PROG_UNLOCK2D</i> . These registers always read back 0. | | | | | | | | |

8.5.4.15.3 OTP_PROG_CTRL

| Address | 0x030B | | | | | | | |
|---|--------|-------|-------|-------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| PAGESEL = Selects which customer OTP page to be programmed. 0 = page 1 1 = page 2 | | | | | | | | |
| PROG_GO = Enables programming for the OTP page selected by <i>OTP_PROG_CTRL[PAGESEL]</i> . Requires <i>OTP_PROG_UNLOCK1*</i> and <i>OTP_PROG_UNLOCK2*</i> registers are set to the correct codes. 0 = Ready 1 = Start OTP programming | | | | | | | | |

8.5.4.15.4 OTP_ECC_TEST

| Address | 0x034C | | | | | | | |
|--|--------|-------|-------|-------|---------|-------------|---------|--------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | RSVD | | | | DED_SEC | MANUAL_AUTO | ENC_DEC | ENABLE |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| RSVD = Reserved | | | | | | | | |
| <p>DED_SEC = Sets the decoder function (SEC or DED) to test. This bit is ignored during encoder testing.</p> <p>0 = Test SEC functionality. Sets the <i>FAULT_OTP[SEC_DETECT]</i> flag and outputs test result to <i>OTP_ECC_DATAOUT*</i> registers.</p> <p>1 = Test DED functionality. Sets the <i>FAULT_OTP[DED_DETECT]</i> flag and outputs test result <i>OTP_ECC_DATAOUT*</i>.</p> <p>Note: If SEC or DEC fault is detected, host sets <i>[RST_OTP_DATA]</i> = 1 to reset the corresponding fault. Switch to run SEC test does not clear DEC fault or vice versa.</p> | | | | | | | | |
| <p>MANUAL_AUTO = Sets the location of the data to use for the ECC test.</p> <p>0 = Auto mode. Use the internal data for test.</p> <p>1 = Manual mode. Uses data in <i>ECC_DATAIN_n</i> registers for test. Use for MPF test.</p> | | | | | | | | |
| <p>ENC_DEC = Sets the encoder/decoder test to run when <i>OTP_ECC_TEST[ENABLE]</i> = 1.</p> <p>0 = Run decoder test</p> <p>1 = Run encoder test</p> | | | | | | | | |
| <p>ENABLE = Executes the OTP ECC test configured by <i>[ENC_DEC]</i> and <i>[DED_SEC]</i> bits.</p> <p>0 = Normal operation, ECC test disabled</p> <p>1 = Initiate test</p> | | | | | | | | |

8.5.4.15.5 OTP_ECC_DATAIN1 through OTP_ECC_DATAIN9

| Address | 0x0343 to 0x034B | | | | | | | |
|---|------------------|-------|-------|-------|-------|-------|-------|-------|
| RW | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | DATA[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <p>DATA[7:0] = When ECC is enabled in manual mode, <i>CUST_ECC_TEST[MANUAL_AUTO]</i> = 1, <i>OTP_ECC_DATAIN1</i>...9 registers are used to test the ECC encoder/decoder.</p> <p>If <i>CUST_ECC_TEST[ENC_DEC]</i> = 1, <i>ECC_DATAIN8</i> through <i>ECC_DATAIN1</i> are fed to the encoder.</p> <p>If <i>CUST_ECC_TEST[ENC_DEC]</i> = 0, <i>ECC_DATAIN9</i> through <i>ECC_DATAIN1</i> are fed to the decoder. The <i>ECC_DATAOUT0</i>...8 bytes must be read back to verify functionality.</p> | | | | | | | | |

8.5.4.15.6 OTP_ECC_DATAOUT1 through OTP_ECC_DATAOUT9

| Address | 0x0510 to 0x0518 | | | | | | | |
|--|------------------|-------|-------|-------|-------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | DATA[7:0] | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <p>DATA[7:0] = <i>OTP_ECC_DATAOUT*</i> bytes output the results of the ECC decoder and encoder tests.</p> <p>If <i>CUST_ECC_TEST[ENC_DEC]</i> = 0, <i>ECC_DATAOUT8</i> through <i>ECC_DATAOUT1</i> are read to determine a successful decoder test.</p> <p>If <i>CUST_ECC_TEST[ENC_DEC]</i> = 1, <i>ECC_DATAOUT9</i> through <i>ECC_DATAOUT1</i> are read to determine a successful encoder test. The correct result depends on the input to the test.</p> | | | | | | | | |

8.5.4.15.7 OTP_PROG_STAT

| Address | 0x0519 | | | | | | | |
|-----------|--------|-------|-------|-------|--------|--------|---------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | UNLOCK | OTERR | UVERR | OVERR | SUVERR | SOVERR | PROGERR | DONE |

| | | | | | | | | |
|--|---|---|---|---|---|---|---|---|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| UNLOCK = Indicates the OTP programming function unlock status. After this bit is set (that is, OTP programming is enabled), the host writes to the <i>OTP_PROG_CTRL</i> register to start the OTP programming. Writing to any other register relocks the OTP programming function and clears this bit to 0. <i>[PROG_GO]</i> = 1 also clears this bit to 0. | | | | | | | | |
| 0 = OTP programming locked 1 = OTP programming is unlocked | | | | | | | | |
| OTERR = Indicates the die temperature is greater than T_{OTP_PROG} and device does not start OTP programming. 0 = No fault 1 = Detected die temperature is greater than T_{OTP_PROG} . Abort OTP programming. | | | | | | | | |
| UVERR = Indicates an undervoltage error detected on the programming voltage during OTP programming. This bit is cleared with <i>[PROG_GO]</i> = 1. 0 = No error 1 = UV error detected | | | | | | | | |
| OVERR = Indicates an overvoltage error detected on the programming voltage during OTP programming. This bit is cleared with <i>[PROG_GO]</i> = 1. Information received from the device with this error must not be considered reliable. 0 = No error 1 = OV error detected | | | | | | | | |
| SUVERR = A programming voltage stability test is performed before starting the actual OTP programming. This bit indicates an undervoltage error is detected during the voltage stability test. This bit is cleared with <i>[PROG_GO]</i> = 1. 0 = No error 1 = UV error detected during OTP programming voltage stability test | | | | | | | | |
| SOVERR = A programming voltage stability test is performed before starting the actual OTP programming. This bit indicates an overvoltage error is detected during the voltage stability test. This bit is cleared with <i>[PROG_GO]</i> = 1. 0 = No error 1 = OV error detected during OTP programming voltage stability test | | | | | | | | |
| PROGERR Indicates when an error is detected due to incorrect page setting caused by any of the following: = • Trying to program but OTP programming <i>[UNLOCK]</i> = 0. • Trying to program a page that has <i>[TRY]</i> = 1. • Trying to program a page which has <i>[FMTERR]</i> = 1. This bit is cleared with <i>[PROG_GO]</i> = 1. 0 = No error or programming not attempted 1 = Error detected | | | | | | | | |
| DONE = Indicates the status of the OTP programming for the selected page. This bit is cleared with <i>[PROG_GO]</i> = 1. 0 = Not completed or programming not attempted 1 = Complete. | | | | | | | | |

8.5.4.15.8 OTP_CUST1_STAT

| Address | 0x051A | | | | | | | |
|---|--------|---------|---------|--------|--------|-------|-------|-------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | LOADED | LOADWRN | LOADERR | FMTERR | PROGOK | UVOK | OVOKE | TRY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| LOADED = Indicates OTP page 1 has been selected for loading into the related registers. See <i>[LOADERR]</i> and <i>[LOADWRN]</i> for error and warning status. 0 = Not selected for loading 1 = Page 1 selected and loaded | | | | | | | | |
| LOADWRN Indicates OTP page 1 was loaded but with one or more SEC warnings. = 0 = No warning, or no load attempted 1 = Warning | | | | | | | | |
| LOADERR = Indicates an error while attempting to load OTP page 1; that is, DED is detected while loading the selected page. 0 = No error, or no load was attempted. 1 = Error detected | | | | | | | | |
| FMTERR = Indicates a formatting error in OTP page 1; that is, when <i>[UVOK]</i> or <i>[OVOKE]</i> is set, but <i>[TRY]</i> = 0. Do not program if this bit is set. 0 = No error 1 = Error detected | | | | | | | | |

| | | | | | | | | |
|---|--|--|--|--|--|--|--|--|
| PROGOK = Indicates the validity for loading for OTP page 1. A valid page indicates that successful programming occurred. 0 = Not valid 1 = Valid | | | | | | | | |
| UVOK = Indicates an OTP programming voltage undervoltage condition is detected during programming attempt for OTP page 1. The OV condition may also trigger the UV as part of the shutdown process. 0 = UV condition detected. Also reads as 0 if no programming attempt is performed. 1 = No UV condition detected | | | | | | | | |
| OVOK = Indicates an OTP programming voltage overvoltage condition is detected during programming attempt for OTP page 1. The OV condition will trigger the UV as part of the shutdown process. The device must be taken out of service. 0 = OV condition detected. Also reads as 0 if no programming attempt is performed. 1 = No OV condition detected | | | | | | | | |
| TRY = Indicates a first programming attempt for OTP page 1. 0 = No first attempt made 1 = First attempt made | | | | | | | | |

8.5.4.15.9 OTP_CUST2_STAT

| Address | 0x051B | | | | | | | |
|---|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Read Only | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Name | LOADED | LOADWRN | LOADERR | FMTER | PROGOK | UVOK | OVOK | TRY |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| LOADED = Indicates OTP page 2 has been selected for loading into the related registers. See [LOADERR] and [LOADWRN] for error and warning status. 0 = Not selected for loading 1 = Page 2 selected and loaded | | | | | | | | |
| LOADWRN Indicates OTP page 2 was loaded but with one or more SEC warnings. = 0 = No warning, or no load attempted 1 = Warning | | | | | | | | |
| LOADERR Indicates an error while attempting to load OTP page 2; that is, DED is detected while loading the selected page. = 0 = No error, or no load was attempted. 1 = Error detected | | | | | | | | |
| FMTER = Indicates a formatting error in OTP page 2; that is, when [UVOK] or [OVOK] is set, but [TRY] = 0. Do not program if this bit is set. 0 = No error 1 = Error detected | | | | | | | | |
| PROGOK = Indicates the validity for loading for OTP page 2. A valid page indicates that successful programming occurred. 0 = Not valid 1 = Valid | | | | | | | | |
| UVOK = Indicates an OTP programming voltage undervoltage condition is detected during programming attempt for OTP page 2. The OV condition may also trigger the UV as part of the shutdown process. 0 = UV condition detected. Also reads as 0 if no programming attempt is performed. 1 = No UV condition detected | | | | | | | | |
| OVOK = Indicates an OTP programming voltage overvoltage condition is detected during programming attempt for OTP page 2. The OV condition will trigger the UV as part of the shutdown process. The device must be taken out of service. 0 = OV condition detected. Also reads as 0 if no programming attempt is performed. 1 = No OV condition detected | | | | | | | | |
| TRY = Indicates a first programming attempt for OTP page 2. 0 = No first attempt made 1 = First attempt made | | | | | | | | |

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The BQ756506-Q1 device provides high-accuracy, cell voltages, temperature and current measurements for 4-series up to 6-series battery modules.

9.2 Typical Applications

9.2.1 Application Circuits

The following application circuits are based on connecting to a 6S and 4S module.

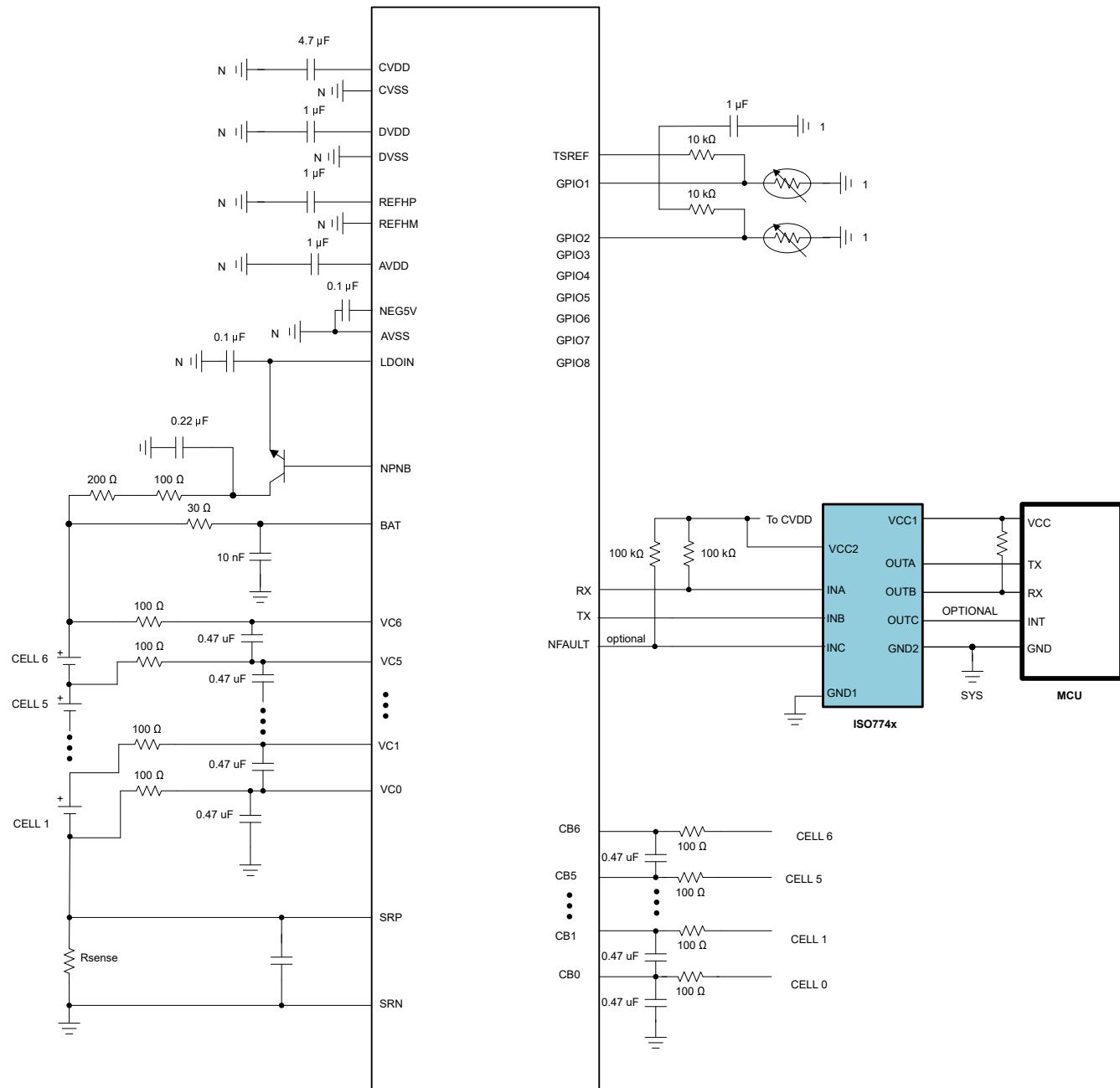


图 9-1. Typical Application Circuit - 6S

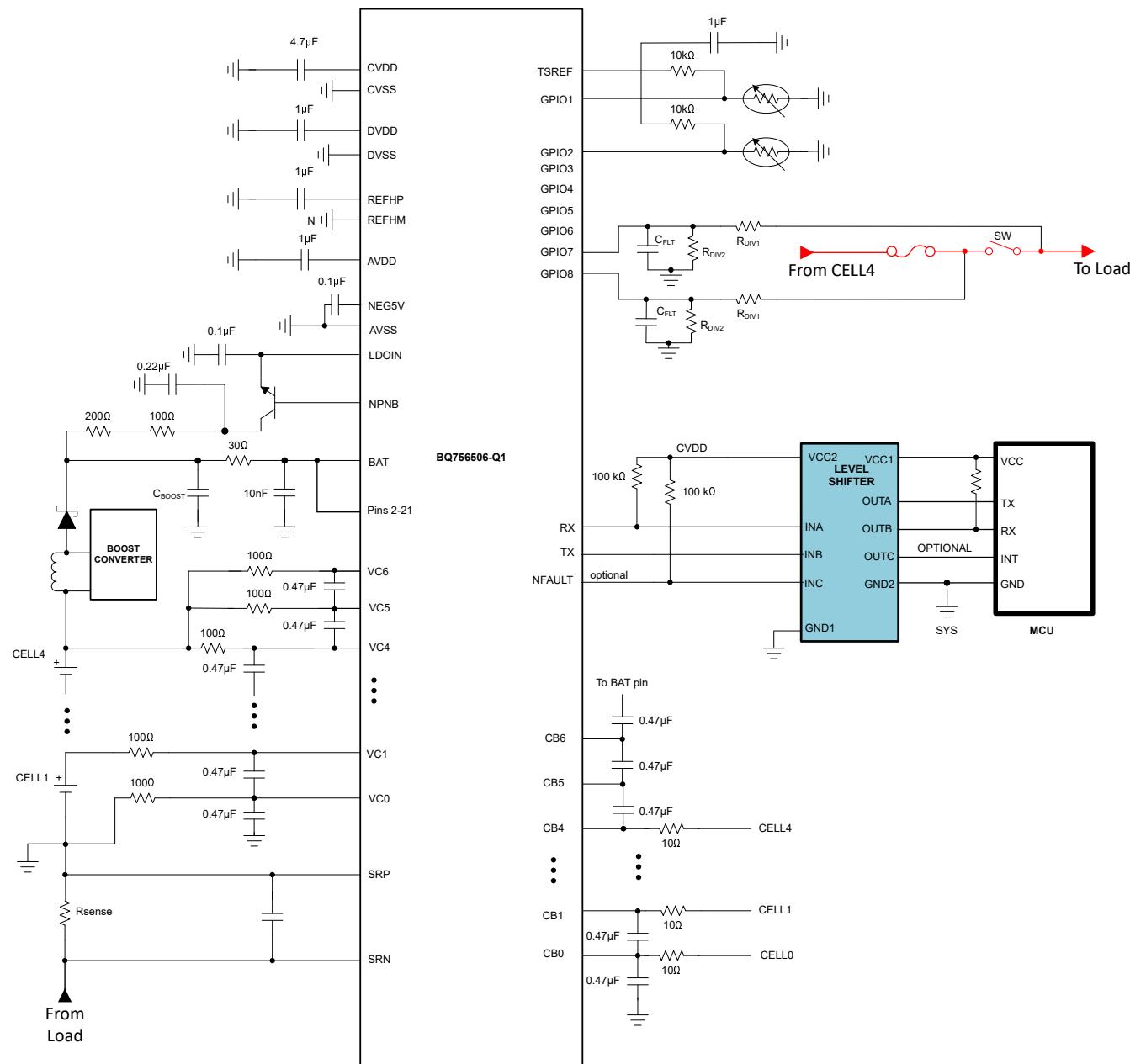


图 9-2. Typical Application Circuit - 4S

9.2.1.1 Design Requirements

表 9-1 below shows the design parameters.

表 9-1. Recommended Design Requirements

| PARAMETER | VALUE |
|---|-----------|
| Module Voltage Range (Voltage at the BAT pin) | 9V to 32V |
| Number of cells | 6 cells |
| Cell voltage range | 0V to 5V |

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Cell Sensing and Balancing Inputs

表 9-2. Cell Sensing and Balancing Inputs

| Related Pins | Components | Value | Description |
|--------------|------------------|--|---|
| VC0 to VC6 | Filter resistor | 100 Ω | Only differential RC filters are needed for VC channels. Besides serving for input signal filtering, these components are required to support hot-plug events during cell module insertion. Hence, it is highly recommended to use the component values as suggested. |
| | Filter capacitor | 0.47 μ F/16 V or 1 μ F/16 V | |
| CB0 to CB6 | Filter resistor | Depends on system's balancing current requirements | The filter resistor on CB pins sets the maximum balancing current. See 节 8.3.3 for details. Only differential RC filters are needed for CB channels. |
| | Filter capacitor | 0.47 μ F/16 V or 1 μ F/16 V | Besides serving for input signal filtering, these components are required to support hot-plug events during cell module insertion. Hence, it is highly recommended to use the component values as suggested. |

Cell Connections

It is recommended to populate the battery cells from bottom channels (both VC and CB channels) and up, leaving upper channels as unused channels if cell module size is smaller than the maximum channel size of the device. Unused channel(s) will be connected as shown in [图 9-3](#).

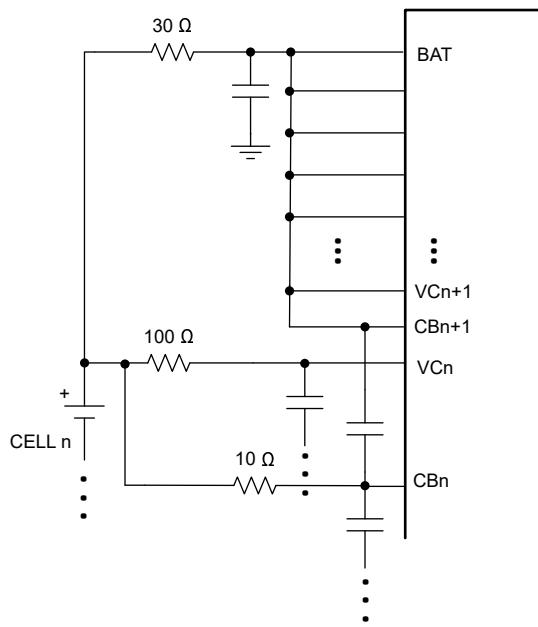
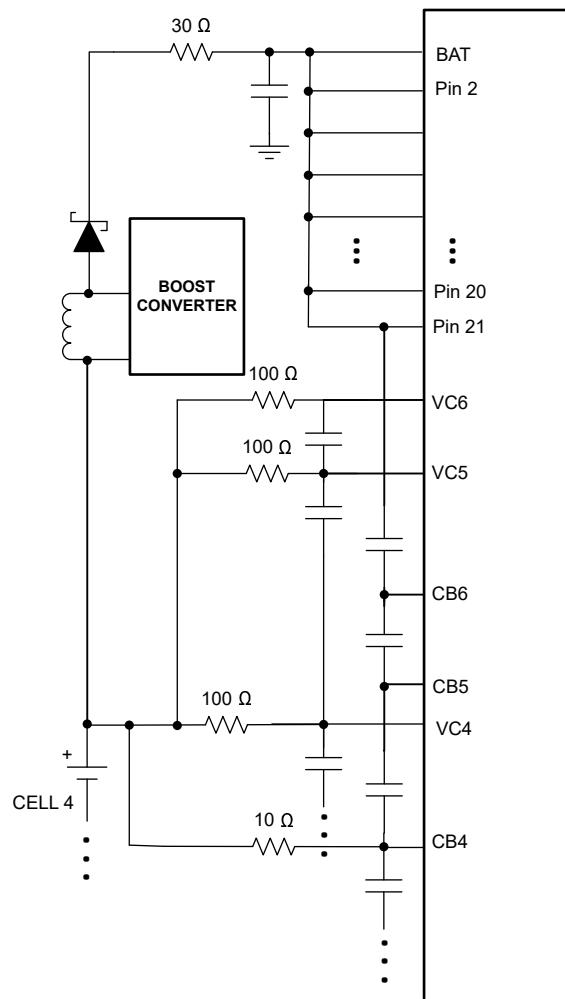


图 9-3. Unused VC and CB Channels - 6S



For 4S applications, short NC pins to BAT Pin and short VC5-6 to VC4

图 9-4. Unused VC and CB Channels - 4S

Fuse and Relay Status Detection

For systems that require fuse and relay monitoring, the GPIOs can be used for this measurement, as shown in [图 9-5](#). The GPIOs provide single-ended ADC measurements of the fuse and relay nodes via a resistor divider, and the difference between these measurements can be used to determine the status of the fuse and the relay. See the fuse and relay diagnostics table for how to detect each case.

R_{DIV1} and R_{DIV2} should be sized so that the maximum module voltage does not cause the GPIO voltages to exceed 5V.

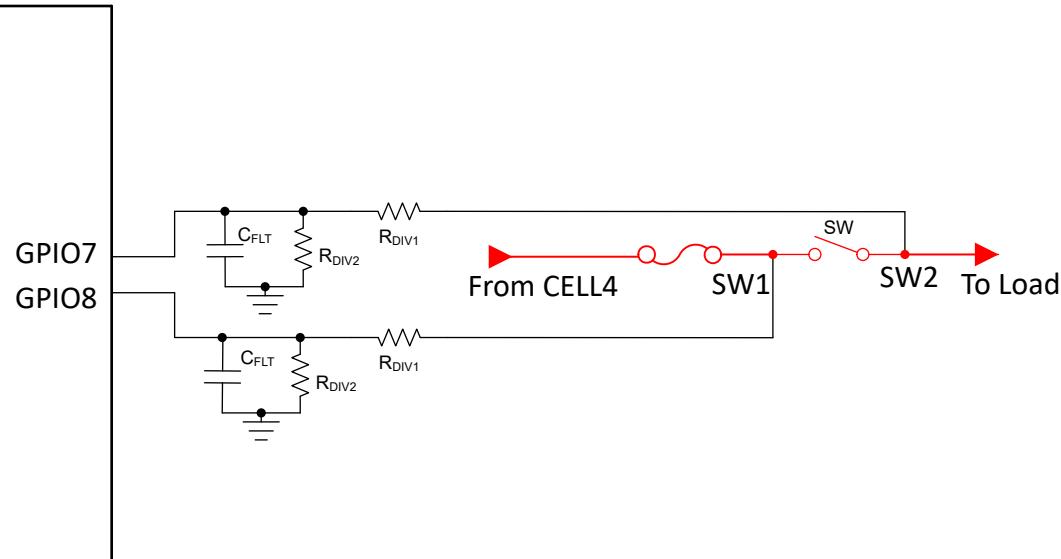


图 9-5. Fuse and Relay Status Detection

Fuse and Relay Diagnostic

In the table below, GPIO8 is used for fuse diagnostics and GPIO7 is used for relay diagnostics. SW1 and SW2 are real voltages at the fuse and relay nodes, calculated from the GPIO resistor dividers. VC4 is the cell voltage measurement of cell 4.

表 9-3. Fuse and Relay Diagnostic

| Diagnostic | Open/Blown | Close |
|------------|---|---|
| Fuse | Indicated when $(SW1-VC4) << 0V$. Open Fuse causes SW1 to be pulled down towards ground by the load. | Indicated when $(SW1-VC4) = \sim 0V$ This IR drop depends on current flow and fuse impedance (e.g. $\pm 0.3V$) |
| Relay | Indicated when $(SW2-SW1) << 0V$ Open Relay causes SW2 to be pulled down towards ground by the load. | Indicated when $(SW2-VC4) = \sim 0V$ This IR drop depends on current flow and fuse impedance (e.g. $\pm 0.3V$) |

9.2.1.2.2 Synchronize Voltage and Current Measurements

It is possible to synchronize the current and voltage measurements in the device. Both Voltage and current ADC start at the same time. CSADC conversion rate (Tconv) and ADC mode of operation (continuous or single run mode), time between reading voltage and current registers are some factors to consider when synchronizing the measurements.

Single run mode

图 9-6 shows the case where single conversion happens at $3 \times T_{cs_conv}$ where $T_{cs_conv} = 512 \mu S$ and the CSADC stops. In this mode, the voltage ADC completes 8 round robin cycles and stops. The voltage and the current data conversions stop within $128 \mu S$ of each other. This can be considered the VI sync time in single conversion mode with above settings. The entire single run mode duration is much less than the settling of the voltage low pass filters. Hence the effect of filters can be ignored for this mode of operation.

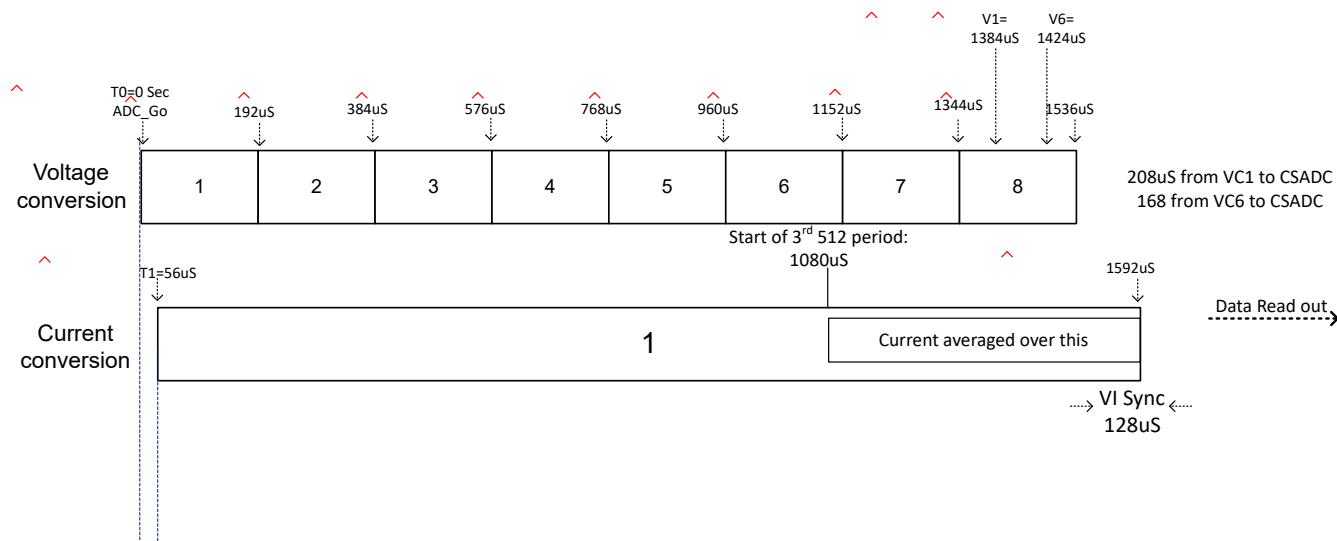


图 9-6. Single Conversion

Continuous run mode

When in continuous conversion mode, the voltage and the current ADCs are continuously running and constantly refreshing the contents of the results register after every conversion. The voltage and the current results registers have 89 registers between them. If the voltage and current are read out in a single read burst, the time that elapses between reading the voltage registers to reading the current register could be 1 mS. Hence for any $T_{cs_conv} \leq 1$ mS, the VI sync time between voltage and current conversion can be considered 1 mS.

Effect of Voltage Low Pass Filter in continuous run mode

The Low pass filter in the voltage ADC path has fcutoff options of 6.5 Hz, 13 Hz, 26 Hz, 53 Hz, 111 Hz, 240 Hz, and 600 Hz, configurable through the ADC_CONF1[LPF_VCELL2:0] setting. The filters ensure that the voltage measurement is stable over a long period of time determined by the fcutoff. Since the voltage does not vary much within the filter time constant, it relaxes the requirement to read back the voltage and the current registers as close to each other as possible and gives MCU more time to read the results register. This is shown in [图 9-7](#). Here the current conversion ‘M’ in the figure can be considered synced with voltage cycles around ‘M’ within ‘N-23’ and ‘N+23’ round robin cycles. The low pass filters are available in the voltage path, but not the current path which causes the two paths to have different frequency response. This needs to be accounted for in selection of filter fcutoff options and CSADC conversion rates.

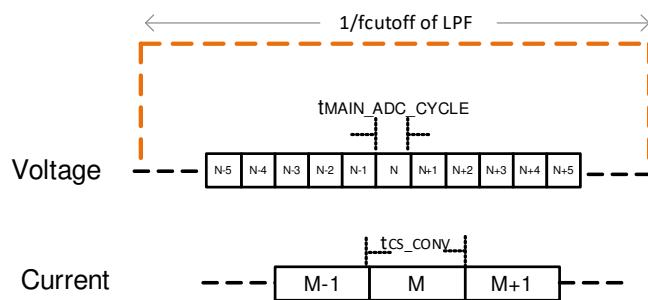


图 9-7. Effect of Voltage Low Pass Filter in Continuous Run Mode

9.2.1.2.3 BAT and External NPN

表 9-4. BAT and External NPN

| Related Pins | Components | Value | Description |
|--------------|--|---|---|
| BAT | Filter resistor | 30 Ω | Single-ended RC filter, recommended values must be used for hot-plug performance. |
| | Filter capacitor | 10 nF/100 V Can use lower voltage rating based on module size | |
| NPNB | NPN (Q1) | Collector - emitter breakdown voltage 80 V to 100 V, but can use lower rating based on module size Power rating ≥ 1 W Gain > 80 at the expected load current Current handling >100 mA | The external NPN is used to form a pre-regulation circuit to provide a 6-V (typical) input to the LD0IN pin. The voltage rating of the NPN can be optimized by the following equation: NPN voltage rating = Max VModule - Min VLDOIN + Margin Where: Max VModule = maximum module voltage with fully charged cells Min VLDOIN = the minimum spec of the VLDOIN parameter Margin = system transient voltage + design margin per application requirement |
| | Resistor on external NPN collector (R_{NPN}) | Various based on module voltage | The resistor has a couple purposes: (a) For an RC filter for the NPN pre-regulation circuit (b) Share the thermal dissipation with the NPN |
| | Capacitor on external NPN collector | 0.22 μF/100 V Can use lower voltage rating based on module size | The capacitor forms the RC filter for the NPN pre-regulation circuit The capacitor rating is based on peak voltage spike seen on the module. For smaller module size, <100-V rated capacitor can be used. System designer selects the optimized voltage-rated capacitor per their system tolerance and requirements. |

To reduce the power rating needed for the external NPN (Q1), system designer can put power resistors on the NPN collector to create IR drop from the module voltage (VModule). 图 9-8 shows the current paths to power the BQ756506 device.

Typical ISTARTUP current i.e. Inrush startup current when device enters from SHUTDOWN to ACTIVE is 20mA for TI recommended components. This current is sum of IBAT + ILDOIN, and is dependent on PCB board components and layout, so recommend user to characterize on their end.

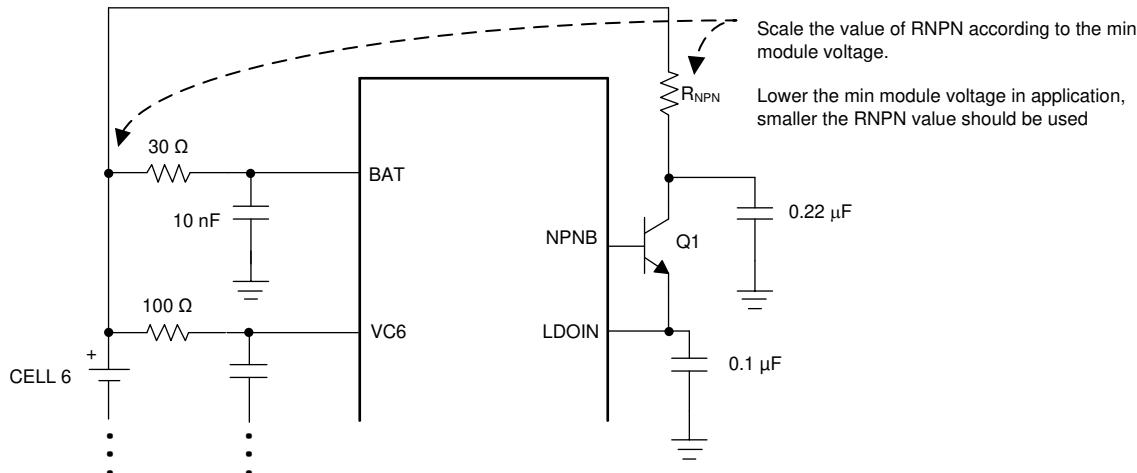


图 9-8. Power Consumption Paths

To ensure there is sufficient headroom to maintain 6 V (typical) regulated voltage on LD0IN pin, system designer ensures VCollector has ≥ 8 V at any time with the assumption of about 2-V drop across the NPN.

Hence, maximum allowable R_{NPN} value = $((\text{Min VModule}) - (\text{VCollector})) / (\text{Max peak current})$

Where:

Min VModule: based on module size and minimum cell voltage per application

VCollector: 8 V with the assumption of about 2-V drop across NPN

Max peak current: highest operation current, which is the active current with all functions turned on. Note that different communication isolation components (for example, capacitor isolation versus transformer, or the type of transformer) contribute different loading to the total power consumption.

Power the device separately from the top of the battery stack:

The device is designed to be powered by the battery stack. If there is a need to power the device from a separately source such as in [图 9-9](#), the following relationship between the voltage on the BAT pin and the highest VC pin voltage (with respect to ground): BAT voltage $\geq (0.5 * \text{highest VC voltage}) + 2$

For example, if the device is connected to a 4S module with max cell voltage of 4.2V/cell, the highest VC pin is VC4, and the highest VC4 voltage is $(4.2V * 4) = 16.8V$. If the BAT pin is powered separately, BAT voltage must be $\geq 10.4V$.

For <6s modules, it is recommended to use an external boost between the top cell and the BAT path. This boost converter should be sized so that BAT meets all of the above requirements. See the following figure.

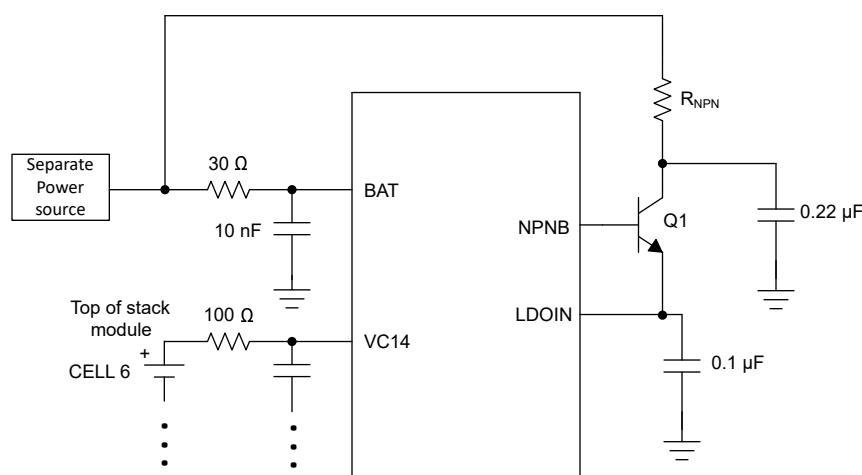


图 9-9. Separate Power Source to BAT

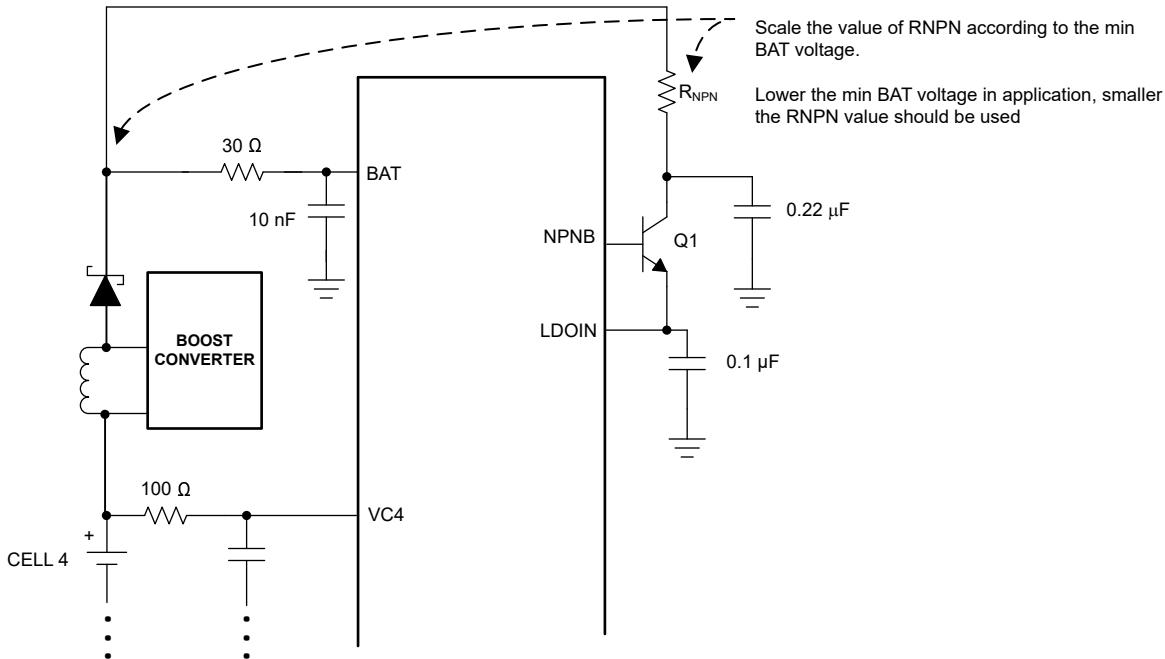


图 9-10. Boost Converter to Supply BAT in 4S Applications

9.2.1.2.4 Power Supplies, Reference Input

表 9-5. Power Supplies, Reference Input

| Related Pins | Components | Value | Description |
|-------------------|------------------|------------------|---|
| AVDD, DVDD, TSREF | Bypass capacitor | 1 μ F/10 V | Bypass capacitor for the internal LDOs |
| CVDD | Bypass capacitor | 4.7 μ F/10 V | Bypass capacitor for CVDD |
| NEG5V | Bypass capacitor | 0.1 μ F/10 V | Bypass capacitor for the negative charge pump |

9.2.1.2.5 GPIO For Thermistor Inputs

When using external thermistor, for ADC measurement only, there is no limitation of what type of thermistors (NTC or PTC) or the bias resistor (R_1) value or whether the thermistor is placed on high side or low side with respect to the bias resistor.

However, when using with the integrated OTUT comparators, the programmable OT and UT threshold ranges are designed to work with a 103NTC (10 k Ω at 25°C) type of NTC thermistor, following the connection shown in [图 9-11](#) with different options for the R_1 and R_2 resistors.

- Option 1: $R_1 = 10 \text{ k}\Omega$, and no R_2
- Option 2: $R_1 = 10 \text{ k}\Omega$, and $R_2 = 100 \text{ k}\Omega$ for better linearity at cold temperature
- Option 3: $R_1 = 3.6 \text{ k}\Omega$, and $R_2 = 15 \text{ k}\Omega$. This base option can be used for NTC used for the OTCB feature assuming system designer allows the PCB temperature to be higher than the cell temperature during balancing. Because the device does not differentiate which NTC is used on the cells versus the PCB, NTC biasing with this option scales the NTC's hot temperature curve differently, allowing the threshold set for OT comparator to be triggered at a lower GPIO voltage. Thus, making the device to only trigger OTCB threshold on this NTC.

The device does not require external RC for temperature measurement. However, it is common for system designer to add an RC filter on the GPIO pin for the NTC circuit. System designer can select the RC values for the application need. Example: $R_{\text{GPIO}} = 1 \text{ k}\Omega$, $C_{\text{GPIO}} = 0.1 \mu\text{F}$ to $1 \mu\text{F}$.

Unused GPIO must be grounded to AVSS with a 10-k Ω resistor.

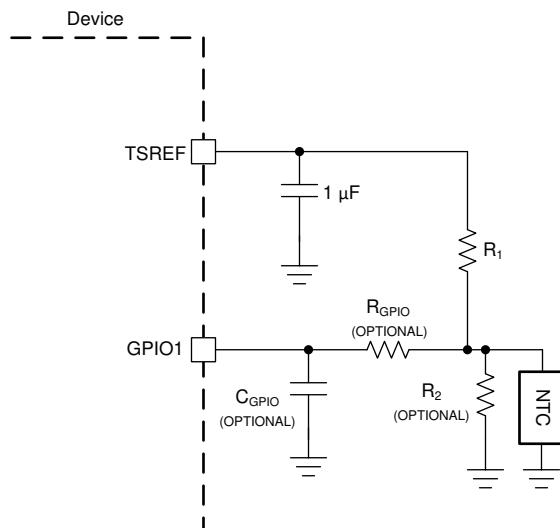


图 9-11. NTC Connection

9.2.1.2.6 Internal Balancing Current

When internal cell balancing is used, the max balancing current the device can support (before going into thermal pause) can vary based on the ambient temperature.

9.2.1.2.7 UART, NFAULT

The UART interface requires the TX and RX pins are pulled up through a 10-k Ω to 100-k Ω resistor. Do not leave TX and RX unconnected. The TX must be pulled high to prevent triggering an invalid communications frame during the idle state. When using a serial cable to connect to the host controller, connect the TX pull-up on the host side and the RX pull-up to the CVDD on the device side.

NFAULT pin for device, if not used, must be left floating. Otherwise, pull it up with 100-k Ω to CVDD.

Important note for NFAULT with <6S applications:

The number of active channels cannot be reduced below six. This means that unmasked faults on unused channels can cause NFAULT to assert. Follow the subsequent directions in order to prevent unused channels from causing unnecessary NFAULT assertions.

Disable the undervoltage checks on unused channels via the UV_DISABLE register. If this isn't used, the channels will always flag UV faults when the OVUV protector is enabled.

To disable the cell balancing diagnostic, set the balancing timer (registers CB_CELLn_CTRL) to 0s on unused channels. This will prevent the diagnostic from running on these channels.

There is no way to prevent open wire diagnostics from triggering faults on unused channels. If a system uses NFAULT, the open wire faults must be masked before running the diagnostics and the results must be read manually. Then the faults must be cleared and the masks disabled. Follow this procedure to run open wire checks:

1. Mask comparison faults via the MSK_COMP register
2. Turn on the VC pins (or CB pins) current sink or source through DIAG_COMP_CTRL3[OW_SNK1:0]
3. Wait for the expected dV/dt time of the external capacitor to deplete to the detection threshold if there is an open wire fault.
4. For VC open wire detection, select DIAP_COMP_CTRL3[COMP_ADC_SEL2:0] = OW CB check (that is, 0b011).
5. The device compares all active VCELL measurements (for VC open wire) or AUX CELL measurements (for CB open wire) against the [OW_THR3:0] threshold setting.

6. When the comparison is completed, $\text{ADC_STAT2}[\text{DRDY_VCOW}] = 1$ for VC open wire (or $[\text{DRDY_CBOW}] = 1$ for CB open wire). Host then turns off all current sinks and sources through $\text{DIAG_COMP_CTRL3}[\text{OW_SNK}1:0]$
7. Manually read the open wire fault registers ($\text{FAULT_COMP_VCOW}x$ or $\text{FAULT_COMP_CBOW}x$)
8. The MCU should take action if used VC/CB channels indicate faults; ignore faults on unused VC/CB channels.
9. Clear faults
10. Unmask comparison faults via MSK_COMP

9.2.1.2.8 Current Sense Input

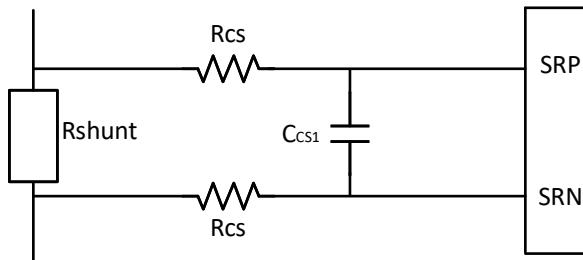


图 9-12. Current Sense Input Connection

It is recommended to add analog RC filter between shut resistor and device current sensing pins (SPR/SRN). This filter helps remove the high frequency components and improves the performance of current sensing ADC remove.

The selection of shut sensing resistor has many system level considerations, a few related to this device:

- Maximum current multiplied with R-shunt should be within Vcs_range absmax range.
- Maximum normal current multiplied with R-shunt should be within $\text{Vcs_range recommended}$ range.
- To fully utilize the current sense ADC input range thus better resolution, it is preferred to choose higher value resistance, this is a tradeoff to thermal dissipation on the shut resistor.
- User can do room temp two points calibration to trim out room temp offset and gain error and store the coefficient in the device. Through this way, the residual error is offset drift and gain error drift.

表 9-6. Current Sense Components

| Related Pins | Components | Value | Description |
|--------------|-----------------------|--------------|--|
| SRP, SRN | Filter Resistor Rcs | 10 Ohm | To avoid inducing large gain error, the value of this resistor needs to be less than 10ohm. |
| | Filter Capacitor Ccs1 | 0.47uF / 16V | Differential filtering capacitor, serves the purpose of filter differential noise. It is recommended to use value not less than 1uF. |

It is not recommended to place a common mode capacitor between ground and SRP/SRN pins since this would couple ground noise to the input pin.

9.2.1.3 Application Curve



图 9-13. UART Write Command

10 Power Supply Recommendations

The device is powered by BAT pin and the LDOIN pin, with which the LDOIN pin is regulated by the preregulation circuit form with an external NPN. The device can be powered by a battery module as low as 9 V (without OTP programming) on the BAT pin. However, system designer must scale the R_{NPN} resistor accordingly to ensure there is sufficient headroom to have 6 V on the LDOIN pin after the IR drop across R_{NPN} and the external NPN. Example, if BAT voltage is at 9 V, the R_{NPN} reduces to 10 Ω to allow sufficient voltage at the LDOIN pin.

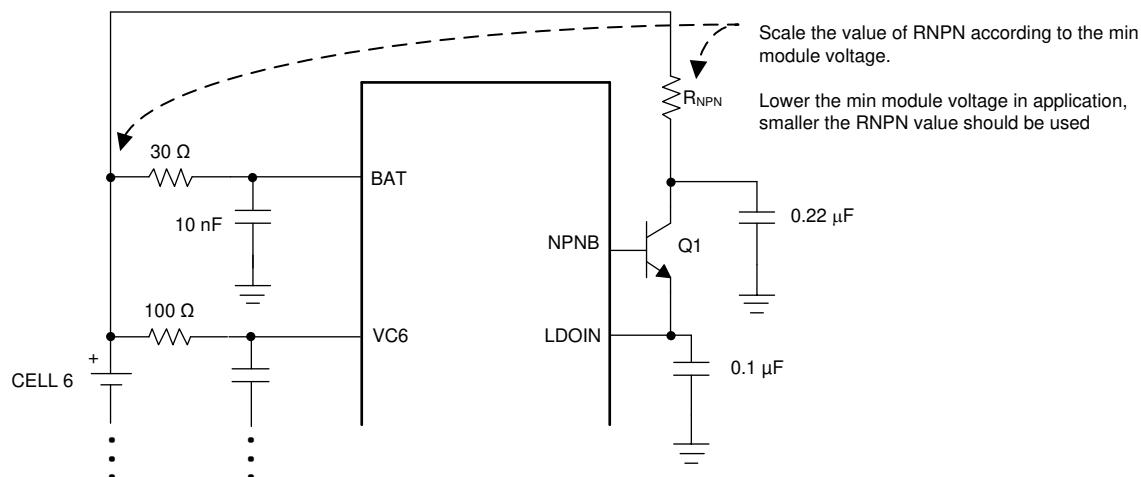


图 10-1. Device Powering Path

11 Layout

The layout for this device must be designed carefully. Any design outside these guidelines can affect the ADC accuracy and EMI performance. Care must be taken in the layout of signals to and from the device to avoid coupling noise onto sensitive inputs. The layout of ground and power connections, as well as communication signals, should also be made carefully.

11.1 Layout Guidelines

11.1.1 Ground Planes

It is very important to establish a clean grounding scheme to ensure best performance of the device. There are three ground pins (AVSS, DVSS, CVSS) for the device's internal power supplies and one ground reference (REFHM) for the precision reference. There are noisy grounds and quiet grounds that must be separated in the layout initially and re-joined together in a lower PCB layer. The external components (for example, bypass capacitors) must be tied to the proper grounding group if possible to keep the separation of noisy and quiet grounds apart.

- AVSS ground:
 - Bypass capacitor for these pins: BAT, VC0, CB0, and AVDD.
 - Package power pad.
- DVSS ground:
 - Bypass capacitor for DVDD.
 - GPIO filter capacitor (if used). It can also connect to AVSS ground plane, if needed.
- CVSS ground:
 - Bypass capacitor for GPIOs, CVDD, TSREF, NEG5V, LDOIN.
- REFHM ground:
 - Bypass capacitor for REFHP.
 - If possible, separate out REFHM from AVSS on the signal connection layer and re-connect REFHM to AVSS ground plane in the lower layer.

Even on a PCB layer that is mainly for signal routing, it is good practice to pour have a small island of ground pour if possible to provide a low-impedance ground, rather than simply a via through the ground trace to an lower ground plane.

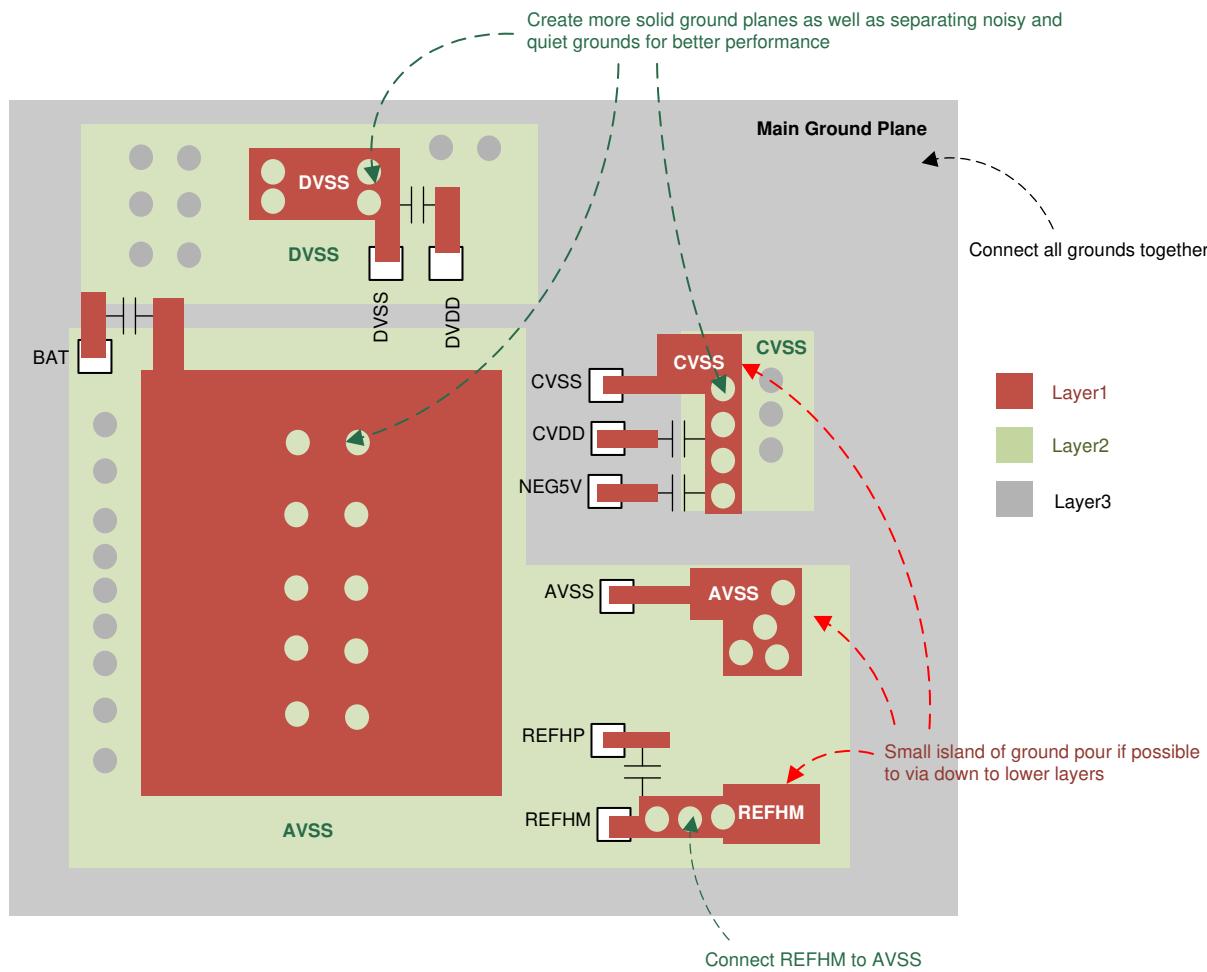


图 11-1. Grounding Layout Consideration

11.1.2 Bypass Capacitors for Power Supplies and Reference

The bypass capacitors of the following pins must be placed as close to the device pins as possible to ensure proper performance, especially for the REFHP capacitor.

- REFHP, BAT, LDOIN, AVDD, DVDD, CVDD, TSREF, and NEG5V

11.1.3 Cell Voltage Sensing

Cell voltage sensing traces (VC pins and CB pins) must be placed in parallel with impedance matching. The balancing traces (CB pins) must be sized properly to carry the maximum balancing current and proper thermal performance for the application.

It is recommended to use separate cables, connect tabs, and PCB traces for the BAT pin and top VC pin connections. Same applies to AVSS and VC0 connections. This avoids the device current impact on the top and bottom cell voltage measurements.

If the same cable and connector tab is used for BAT/top VC pins connection and AVSS/VC0 pins connection, the PCB trace going to BAT/top VC pins and AVSS/VC0 pins must be separated at the connector tabs. Note the device current will still go through the cell to the PCB cable, which may introduce IR errors across the cable connection to the top and bottom cell measurements.

11.2 Layout Example

This section presents the BQ79616-Q1 Evaluation Module (EVM) design as a layout example.

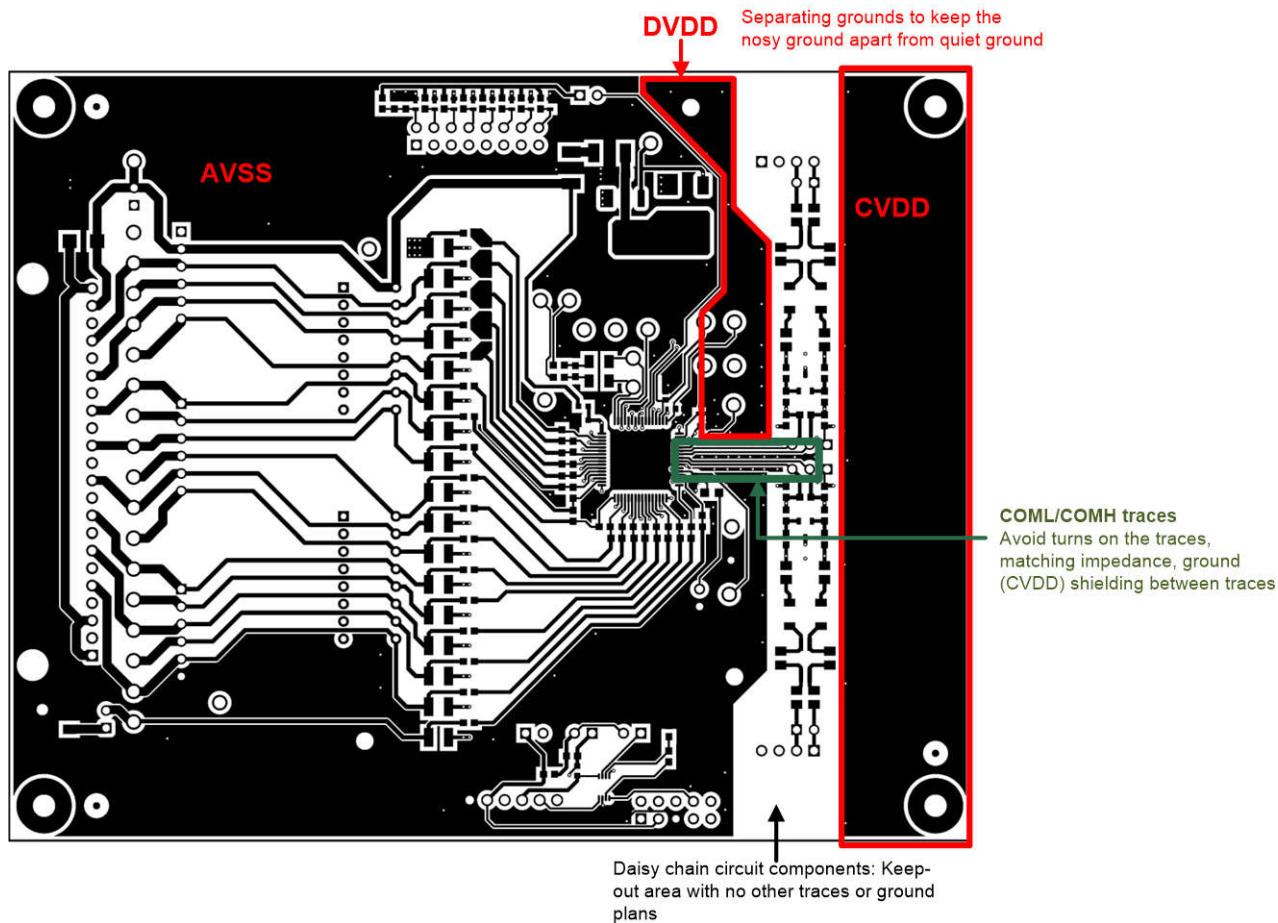


图 11-2. Top Signal Layer

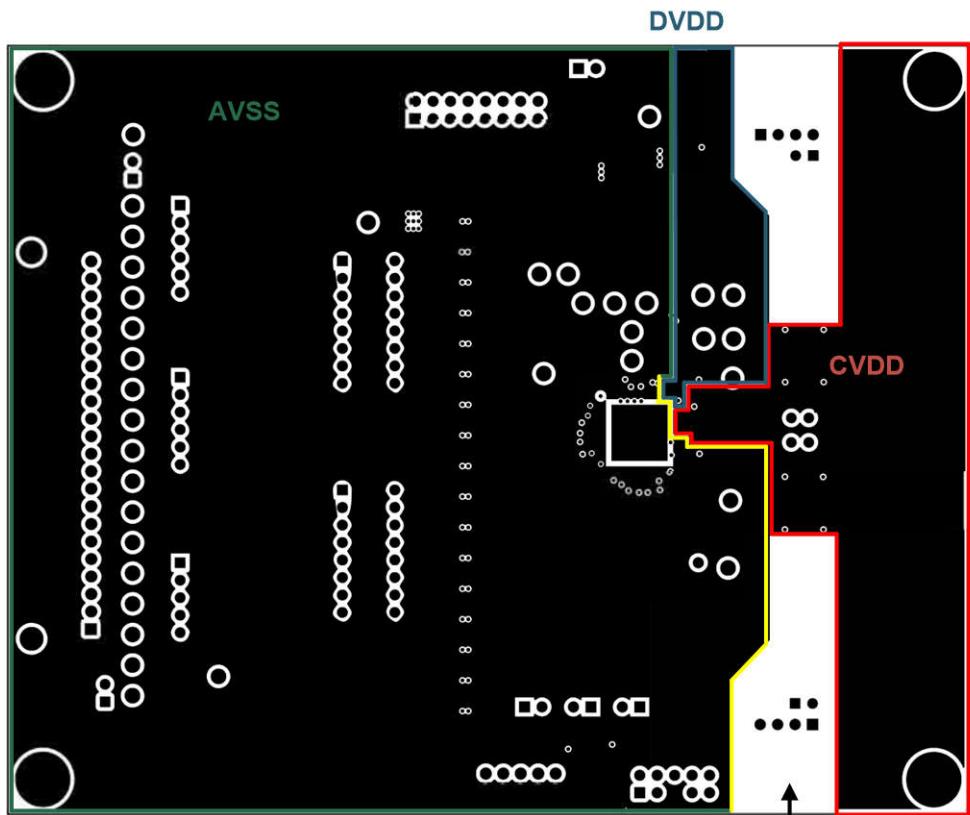


图 11-3. Second Layer with Solid, Separate Ground Planes

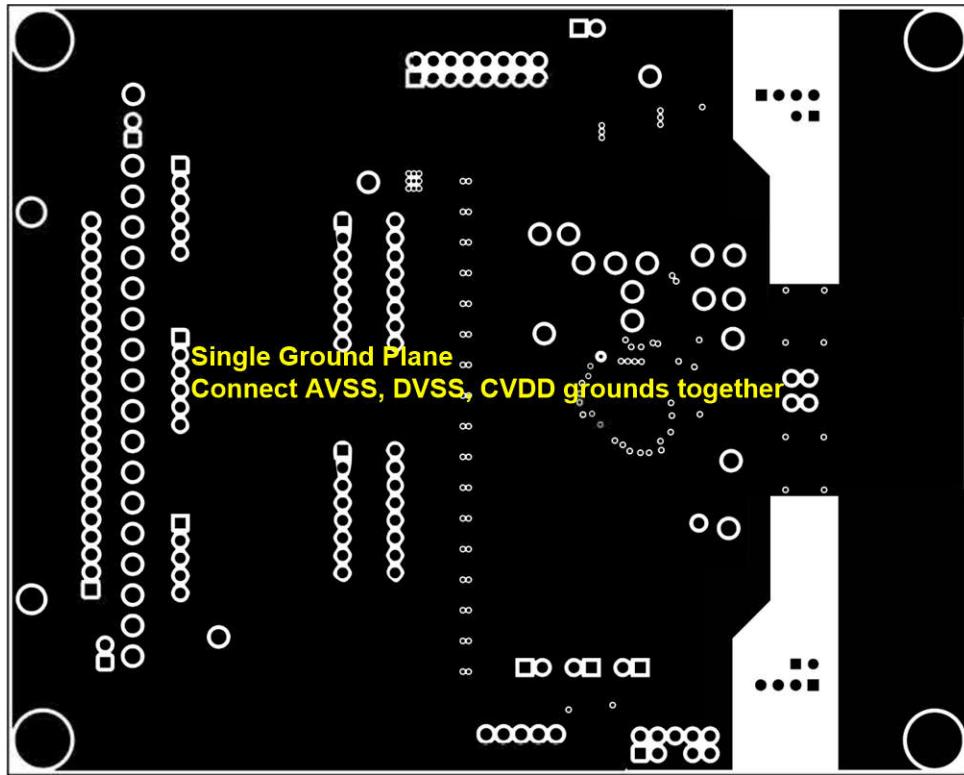


图 11-4. Third Layer with Single Ground Plane

12 Device and Documentation Support

12.1 Device Support

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| BQ756506PAPRQ1 | Active | Production | HTQFP (PAP) 64 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | BQ756506 |
| BQ756506PAPRQ1.A | Active | Production | HTQFP (PAP) 64 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | BQ756506 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

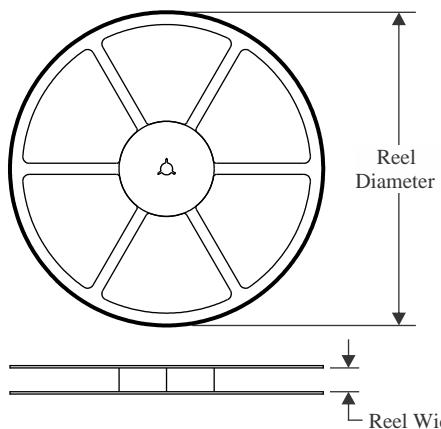
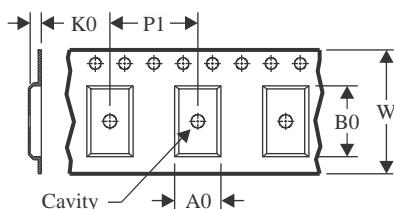
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

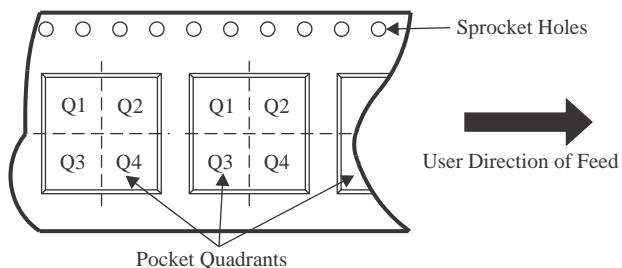
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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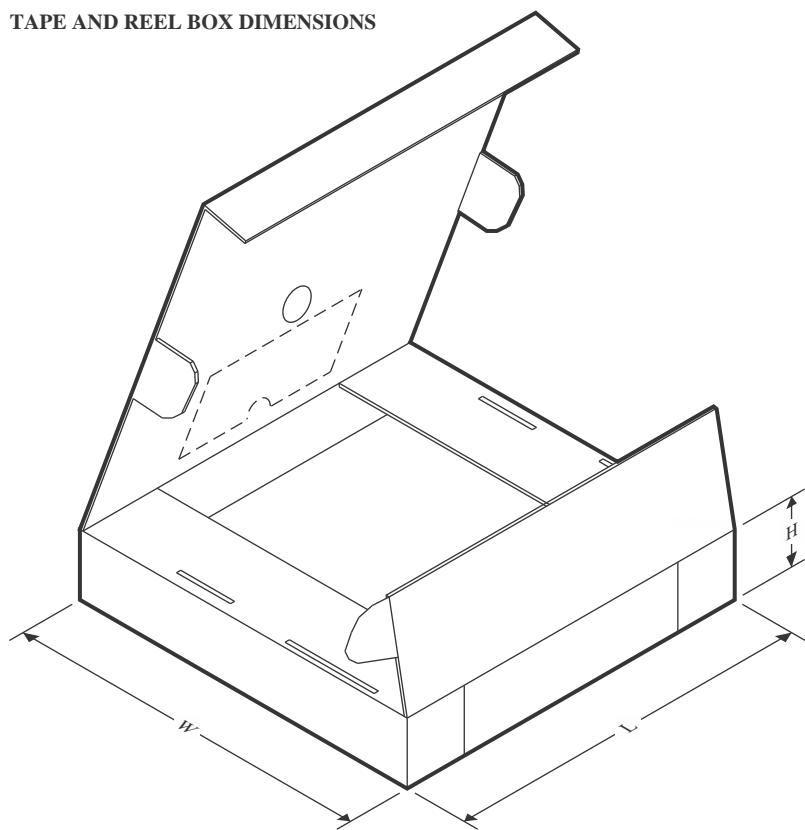
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ756506PAPRQ1 | HTQFP | PAP | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ756506PAPRQ1 | HTQFP | PAP | 64 | 1000 | 367.0 | 367.0 | 55.0 |

GENERIC PACKAGE VIEW

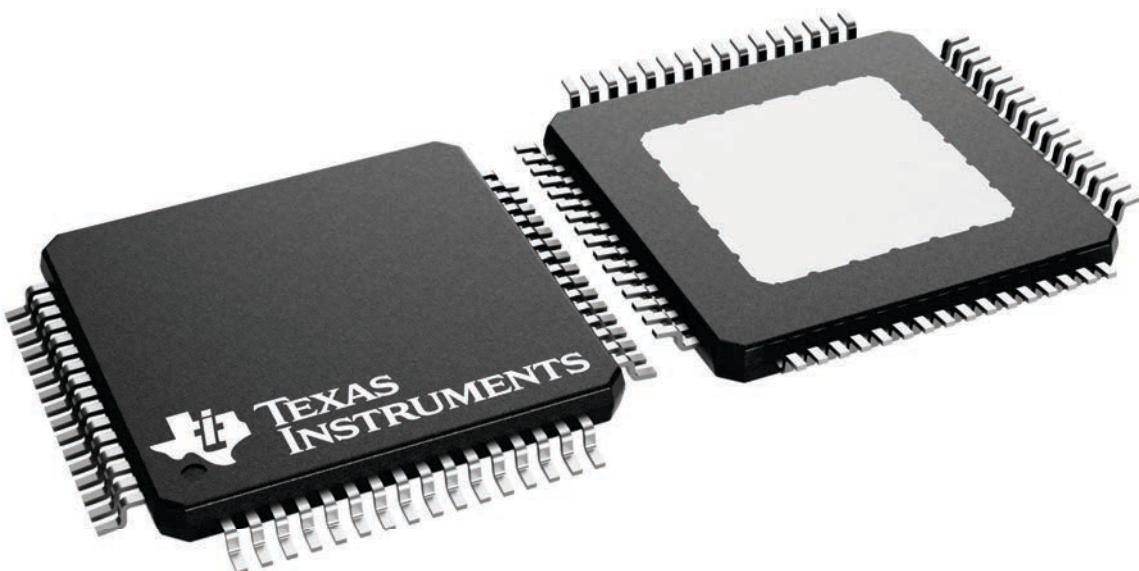
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



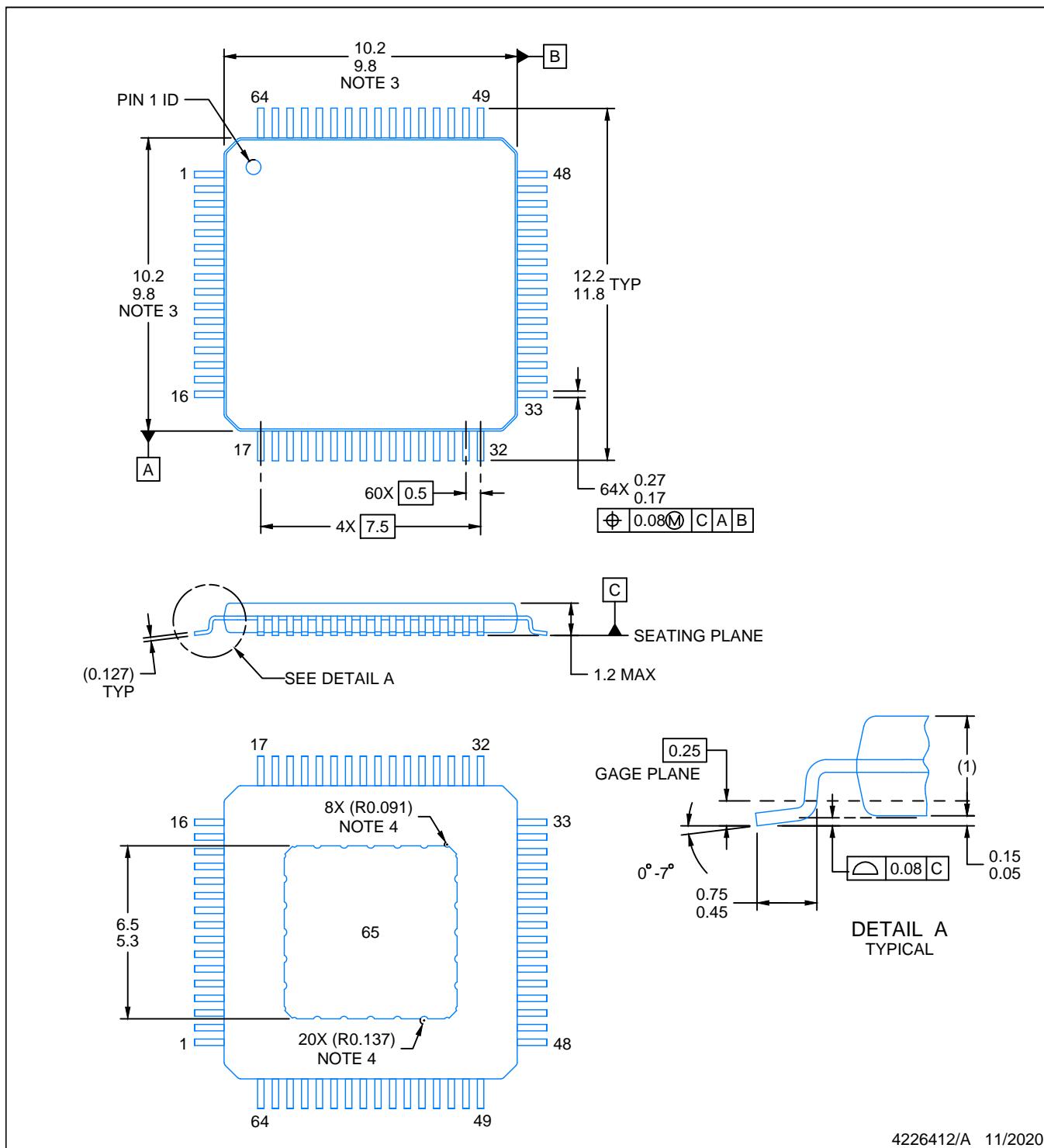
4226442/A

PACKAGE OUTLINE

PAP0064F

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES:

PowerPAD is a trademark of Texas Instruments.

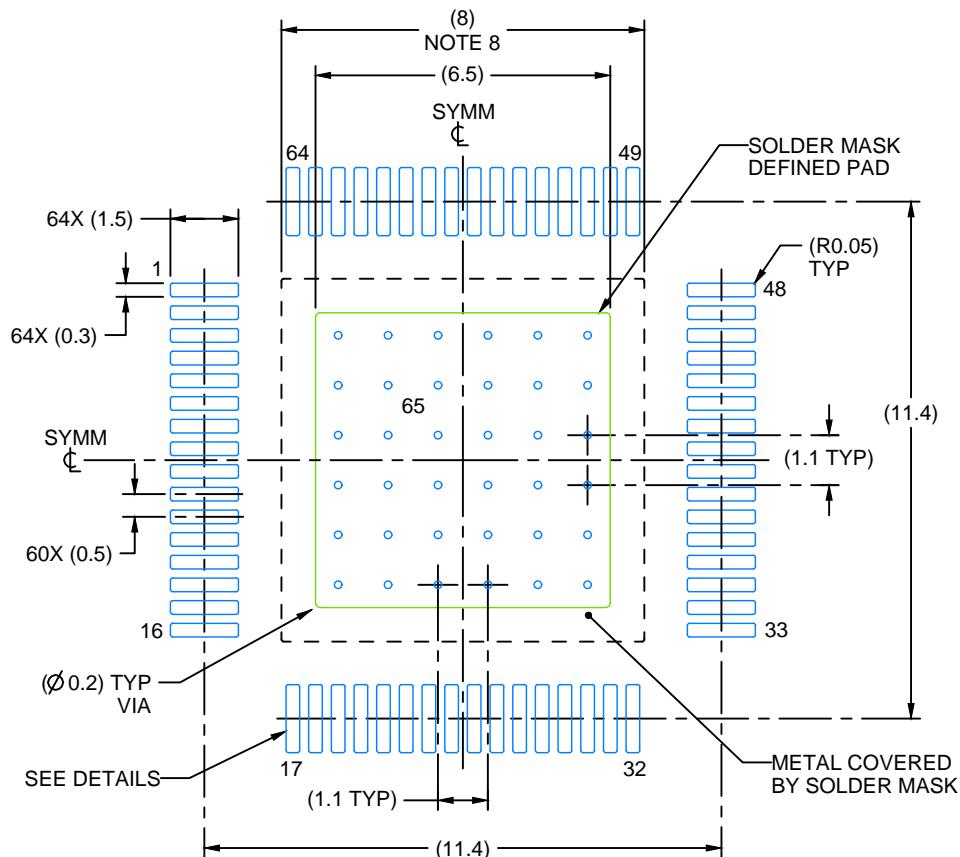
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

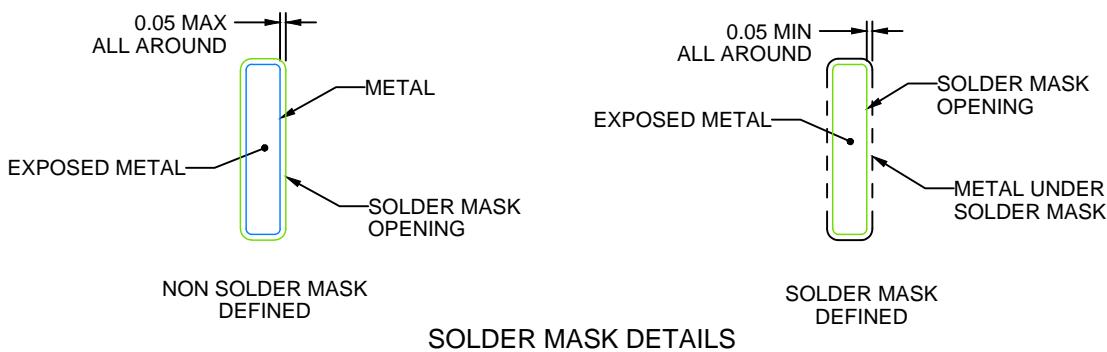
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LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



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NOTES: (continued)

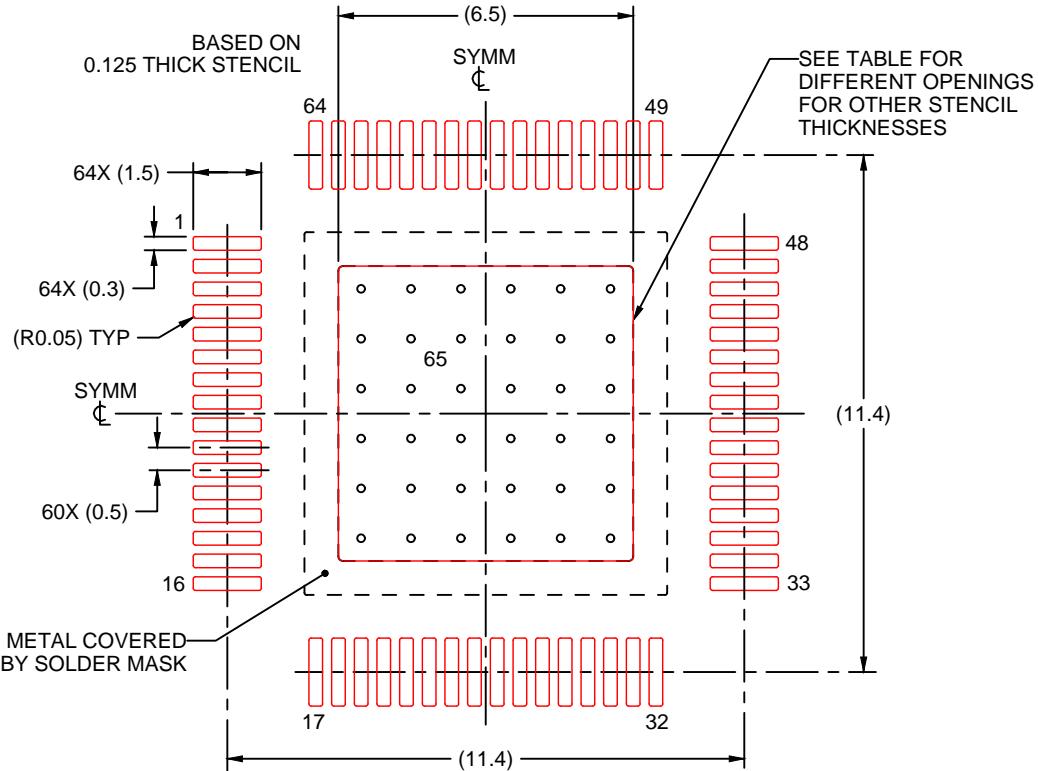
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

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SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1 | 7.27 X 7.27 |
| 0.125 | 6.5 X 6.5 (SHOWN) |
| 0.15 | 5.93 X 5.93 |
| 0.175 | 5.49 X 5.49 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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