AMC3330-Q1 具有集成式直流/直流转换器的汽车级、±1V 输入、增强型隔离式精密放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 125°C，T_A
- 3.3V 或 5V 单电源运行，具有集成直流/直流转换器
- ±1V 输入电压范围，针对使用高输入阻抗的电压测量进行了优化
- 固定增益：2.0
- 低直流误差：
  - 增益误差：±0.2%（最大值）
  - 增益漂移：±45ppm/°C（最大值）
  - 失调电压误差：±0.3mV（最大值）
  - 失调电压温漂：±4μV/°C（最大值）
  - 非线性度：±0.02%（最大值）
- 高 CMTI：85kV/μs（最小值）
- 系统级诊断功能
- 安全相关认证：
  - 符合 DIN EN IEC 60747-17 (VDE 0884-17) 的 6000V_{PK} 增强型隔离
  - 4250V_{RMS} 隔离，符合 UL1577 标准且持续时长为 1 分钟
- 符合 CISPR-11 和 CISPR-25 EMI 标准

2 应用

- 可用于以下应用的隔离式电压感应：
  - 混合动力汽车/电动汽车车载充电器 (OBC)
  - 混合动力汽车/电动汽车直流/直流转换器
  - 混合动力汽车/电动汽车牵引逆变器
  - 混合动力汽车/电动汽车电池管理系统 (BMS)

3 说明

AMC3330-Q1 是一款具有完全集成的隔离式直流/直流转换器的精密隔离式放大器，能实现器件低侧的单电源运行。该增强型电容隔离层通过了 DIN EN IEC 60747-17 (VDE 0884-17) 和 UL1577 标准认证，将以不同共模电压电平运行的系统各部分隔开，并保护低压域免受损坏。

AMC3330-Q1 的输入针对直接连接高阻抗电压信号源（例如电阻分压器网络）的情况进行了优化，以感应高压信号。集成式隔离直流/直流转换器可测量非接地信号，并使该器件成为嘈杂空间受限应用的独特解决方案。

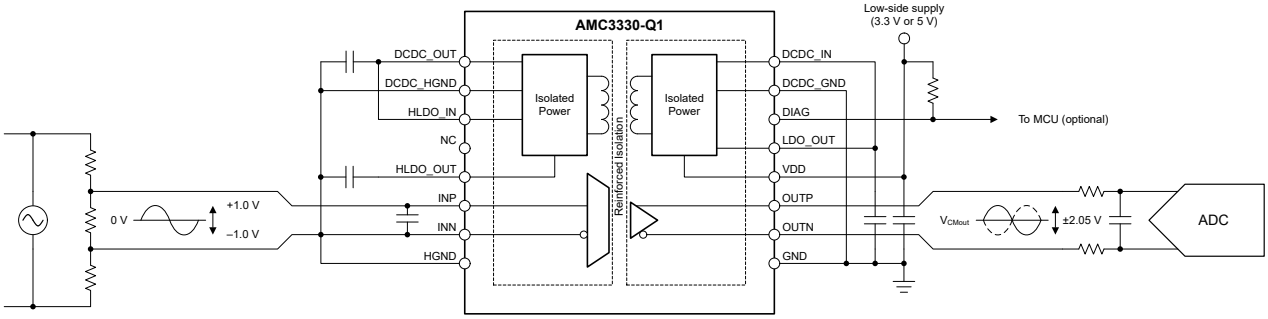
该器件性能出色，支持进行精确的电压监控。AMC3330-Q1 的集成直流/直流转换器故障检测和诊断输出引脚可简化系统级设计和诊断。

AMC3330-Q1 的额定工作温度范围为 -40°C 至 +125°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
AMC3330-Q1	DWE（SOIC，16）	10.3mm × 10.3mm

(1) 如需更多信息，请参阅*机械、封装和可订购信息*。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



应用示例

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

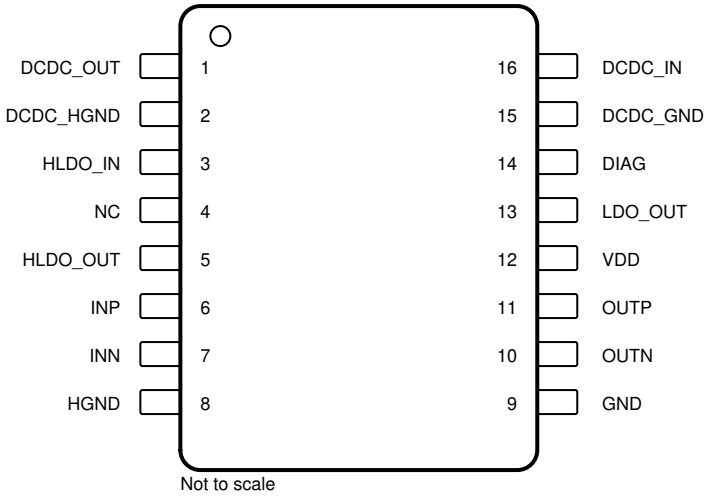


图 4-1. DWE Package, 16-Pin SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DCDC_OUT	Power	High-side output of the isolated DC/DC converter; connect this pin to the HLDO_IN pin.(1)
2	DCDC_HGND	Power Ground	High-side ground reference for the isolated DC/DC converter; connect this pin to the HGND pin.
3	HLDO_IN	Power	Input of the high-side low-dropout (LDO) regulator; connect this pin to the DCDC_OUT pin.(1)
4	NC	—	No internal connection. Connect this pin to the high-side ground or leave this pin unconnected (floating).
5	HLDO_OUT	Power	Output of the high-side LDO.(1)
6	INP	Analog Input	Noninverting analog input.
7	INN	Analog Input	Inverting analog input. Connect this pin to HGND.
8	HGND	Signal Ground	High-side analog ground; connect this pin to the DCDC_HGND pin.
9	GND	Signal Ground	Low-side analog ground; connect this pin to the DCDC_GND pin.
10	OUTN	Analog Output	Inverting analog output.
11	OUTP	Analog Output	Noninverting analog output.
12	VDD	Power	Low-side power supply.(1)
13	LDO_OUT	Power	Output of the low-side LDO; connect this pin to the DCDC_IN pin.(1)
14	DIAG	Digital Output	Active-low, open-drain status indicator output; connect this pin to the pullup supply (for example, VDD) using a resistor or leave this pin floating if not used.
15	DCDC_GND	Power Ground	Low-side ground reference for the isolated DC/DC converter; connect this pin to the GND pin.
16	DCDC_IN	Power	Low-side input of the isolated DC/DC converter; connect this pin to the LDO_OUT pin.(1)

(1) See the *Power Supply Recommendations* section for power-supply decouplng recommendations.

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5 Specifications

5.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	6.5	V
Analog input voltage	INP, INN	HGND – 6	$V_{HLDOout}$ + 0.5	V
Analog output voltage	OUTP, OUTN	GND – 0.5	VDD + 0.5	V
Digital output voltage	DIAG	GND – 0.5	6.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), HBM ESD classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification Level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Low-side supply voltage	VDD to GND	3.0	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} - V_{INN}$		±1.25		V
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} - V_{INN}$	–1		1	V
	Absolute common-mode input voltage(1)	$(V_{INP} + V_{INN}) / 2$ to HGND	–2		3	V
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to HGND, $V_{INP} = V_{INN}$	–1.4		1.6	V
		$(V_{INP} + V_{INN}) / 2$ to HGND, $\lvert V_{INP} - V_{INN} \rvert$ = 1.0 V (2)	–0.925		0.725	
		$(V_{INP} + V_{INN}) / 2$ to HGND, $\lvert V_{INP} - V_{INN} \rvert$ = 1.25 V	–0.8		0.6	
ANALOG OUTPUT						
C_{LOAD}	Capacitive load	On OUTP or OUTN to GND2, Without any series resistance			500	pF
C_{LOAD}	Capacitive load	OUTP to OUTN, Without any series resistance			250	pF
R_{LOAD}	Resistive load	On OUTP or OUTN to GND2		10	1	kΩ
DIGITAL OUTPUT						
	Pull-up supply-voltage for DIAG pin		0		VDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40	25	125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.
(2) Linear response.

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5.4 Thermal Information

THERMAL METRIC(1)		AMC3330-Q1 DWE (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	VDD = 5.5 V			236.5	mW
		VDD = 3.6 V			155	

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5.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	⩾ 8	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	⩾ 8	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance - capacitive signal isolation)	⩾ 21	µm
DTI	Distance through insulation	Minimum internal gap (internal clearance - transformer power isolation)	⩾ 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	⩾ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ⩽ 600V_{RMS}	I-III	
		Rated mains voltage ⩽ 1000V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1700	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1200	V_{RMS}
		At DC voltage	1700	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification test), V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production test)	6000	V_{PK}
V_{IMP}	Maximum impulse voltage(2)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)}$ = V_{IOTM}, t_{ini} = 60s, $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10s	⩽ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)}$ = V_{IOTM}, t_{ini} = 60s, $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	⩽ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)}$ = 1.2 x V_{IOTM}, t_{ini} = 1s, $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1s	⩽ 5	
		Method b2, at routine test (100% production)(6), $V_{pd(ini)}$ = $V_{pd(m)}$ = 1.2 x V_{IOTM}, t_{ini} = t_m = 1s	⩽ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 V_{PP} at 1MHz	~4.5	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ⩽ T_A ⩽ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO}, t = 60s (qualification test), V_{TEST} = 1.2 × V_{ISO}, t = 1s (100% production test)	4250	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application.Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) Testing is carried out in air to determine the surge immunity of the package.
(3) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.
(6) Either method b1 or b2 is used in production.

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5.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

5.8 Safety Limiting Values

Safety limiting (1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 73.5°C/W, VDD = 5.5 V, T_J = 150°C, T_A = 25°C			309	mA
		$R_{\theta JA}$ = 73.5°C/W, VDD = 3.6 V, T_J = 150°C, T_A = 25°C			472	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 73.5°C/W, T_J = 150°C, T_A = 25°C			1700	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum low-side voltage.

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5.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, INP = –1 V to +1 V, and INN = HGND = 0 V; typical specifications are at T_A = 25°C, and VDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
R_{IN}	Single-ended input resistance	INN = HGND	0.1	0.8		GΩ
R_{IND}	Differential input resistance		0.1	1.2		
I_{IB}	Input bias current	INP = INN = HGND, I_{IB} = (I_{IBP} + I_{IBN}) / 2	–10	2.5	10	nA
TCI_{IB}	Input bias current drift			–14		pA/°C
I_{IO}	Input offset current	I_{IO} = I_{INP} – I_{INN}; INP = INN = HGND	–10	-0.8	10	nA
C_{IN}	Single-ended input capacitance	INN = HGND, f_{IN} = 310 kHz		2		pF
C_{IND}	Differential input capacitance	f_{IN} = 310 kHz		2		
ANALOG OUTPUT						
	Nominal gain			2		V/V
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	V_{OUT} = (V_{OUTP} – V_{OUTN}); $\lvert V_{IN}\rvert$ = $\lvert V_{INP} – V_{INN}\rvert$ > $V_{Clipping}$		±2.49		V
$V_{Failsafe}$	Failsafe differential output voltage	V+ = (V_{OUTP} – V_{OUTN}); $V_{DCDCout} \leqslant V_{DCDCUV}$ or $V_{HLDOout} \leqslant V_{HLDOUV}$		–2.57	–2.5	V
BW_{OUT}	Output bandwidth		300	375		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, INP = INN = HGND, outputs shorted to either GND or VDD		14		mA
CMTI	Common-mode transient immunity	|HGND – GND| = 2 kV	85	135		kV/µs
ACCURACY						
V_{OS}	Input offset voltage(1) (2)	T_A = 25°C, INP = INN = HGND	–0.3	±0.05	0.3	mV
TCV_{OS}	Input offset drift(1) (2) (4)		–4	±1	4	µV/°C
E_G	Gain error	T_A = 25°C	–0.2%	–0.08%	0.2%	
TCE_G	Gain error drift(1) (5)		–45	±7	45	ppm/°C
	Nonlinearity		–0.02%	0.01%	0.02%	
	Nonlinearity drift			0.4		ppm/°C
SNR	Signal-to-noise ratio	V_{IN} = 2 V_{PP}, f_{IN} = 1 kHz, BW = 10 kHz, 10 kHz filter	81	85		dB
		V_{IN} = 2 V_{PP}, f_{IN} = 10 kHz, BW = 100 kHz, 1 MHz filter		72		
THD	Total harmonic distortion(3)	V_{IN} = 2 Vpp, f_{IN} = 10 kHz, BW = 100 kHz		–84		dB
	Output noise	INP = INN = HGND, f_{IN} = 0 Hz, BW = 100 kHz		250		$µV_{RMS}$
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \leqslant V_{CM} \leqslant V_{CM\ max}$		–100		dB
		f_{IN} = 10 kHz, $V_{CM\ min} \leqslant V_{CM} \leqslant V_{CM\ max}$		–86		
PSRR	Power-supply rejection ratio	VDD from 3.0 V to 5.5 V, at dc, input referred		–98		dB
		INP = INN = HGND, VDD from 3.0 V to 5.5 V, 10 kHz / 100 mV ripple, input referred		–86		
DIGITAL OUTPUT (DIAG)						

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5.9 Electrical Characteristics（续）

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, INP = –1 V to +1 V, and INN = HGND = 0 V; typical specifications are at T_A = 25°C, and VDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{SINK}= 4 mA		80	250	mV
I_{LKG}	Open-drain output leakage current	VDD = 5V		5	100	nA
POWER SUPPLY						
IDD	Low-side supply current	No external load on HLDO		28.5	41	mA
		1 mA external load on HLDO		30.5	43	mA
VDD_{UV}	VDD analog undervoltage detection threshold	VDD rising			2.9	V
		VDD falling			2.8	
VDD_{POR}	VDD digital reset threshold	VDD rising			2.5	V
		VDD falling			2.4	
V_{DCDC_OUT}	DC/DC output voltage	DCDC_OUT to HGND	3.1	3.5	4.65	V
V_{DCDCUV}	DC/DC output undervoltage detection threshold voltage	DCDC output falling	2.1	2.25		V
V_{HLDO_OUT}	High-side LDO output voltage	HLDO to HGND, up to 1 mA external load	3	3.2	3.4	V
V_{HLDOUV}	High-side LDO output undervoltage detection threshold voltage	HLDO output falling	2.4	2.6		V
I_H	High-side supply current for auxiliary circuitry	3 V ≤ VDD < 4.5 V, load connected from HLDO_OUT to HGND, non-switching			1	mA
		4.5 V ≤ VDD ≤ 5.5 V, load connected from HLDO_OUT to HGND, non-switching			4.3	
t_{AS}	Analog settling time	VDD step to 3.0 V, to OUTP and OUTN valid, 0.1% settling		0.6	1.1	ms

(1) The typical value includes one standard deviation ("sigma") at nominal operating conditons.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation: $TCV_{OS} = (V_{OS,MAX} - V_{OS,MIN}) / TempRange$ where $V_{OS,MAX}$ and $V_{OS,MIN}$ refer to the maximum and minimum V_{OS} values measured within the temperature range (–40 to 125℃).
(5) Gain error temperature drift is calculated using the box method, as described by the following equation: $TCE_G\ (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125℃).

5.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.3		µs
t_f	Output signal fall time			1.3		µs
	V_{INx} to V_{OUTx} signal delay (50% – 10%)	Unfiltered output		1.2	1.3	µs
	V_{INx} to V_{OUTx} signal delay (50% – 50%)	Unfiltered output		1.6	2.1	µs
	V_{INx} to V_{OUTx} signal delay (50% – 90%)	Unfiltered output		2.2	2.6	µs

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5.11 Timing Diagram

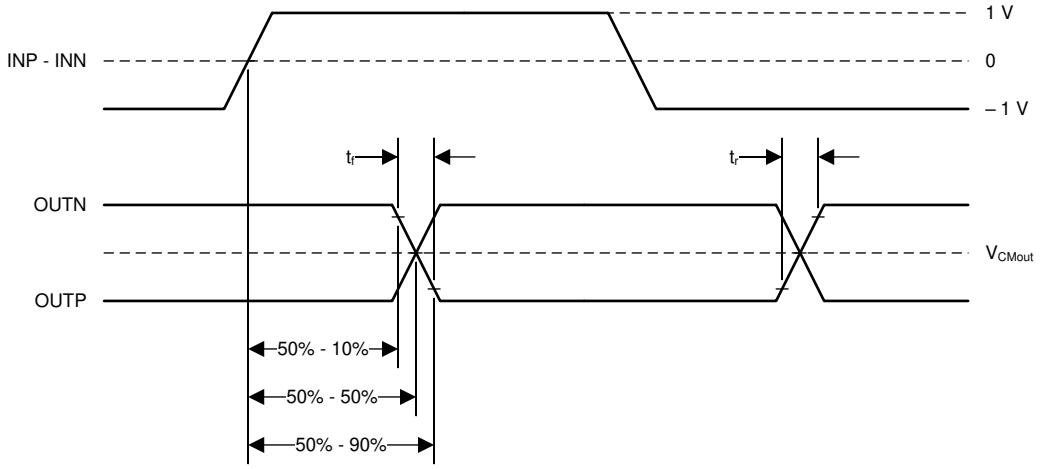


图 5-1. Rise, Fall, and Delay Time Waveforms

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5.12 Insulation Characteristics Curves

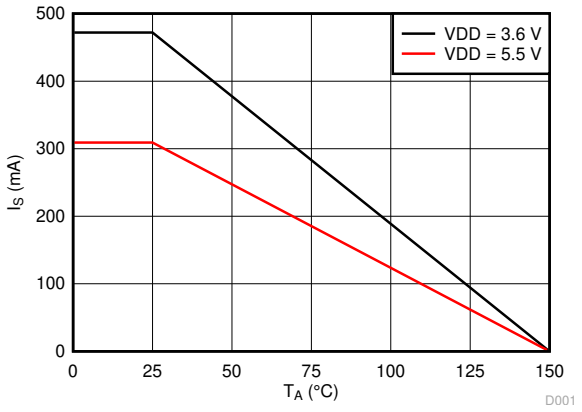


图 5-2. Thermal Derating Curve for Safety-Limiting Current per VDE

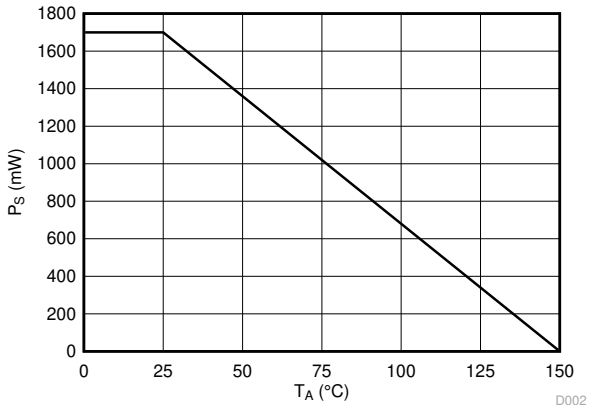


图 5-3. Thermal Derating Curve for Safety-Limiting Power per VDE

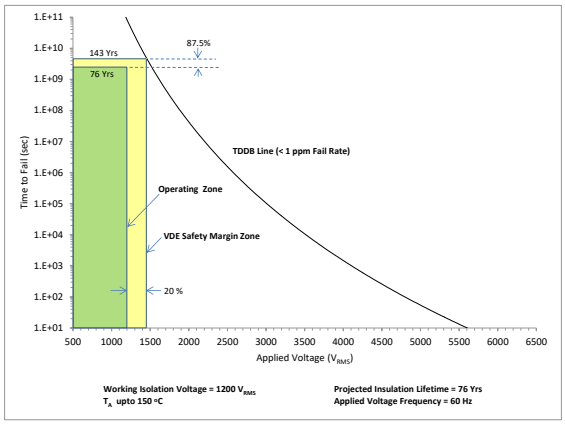


图 5-4. Reinforced Isolation Capacitor Lifetime Projection

5.13 Typical Characteristics

at VDD = 3.3 V, INP = – 1 V to 1 V, INN = HGND = 0V, and f_{IN} = 10 kHz (unless otherwise noted)

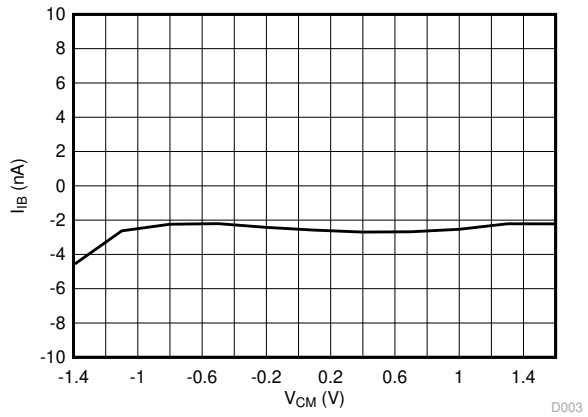


图 5-5. Input Bias Current vs Common-Mode Input Voltage

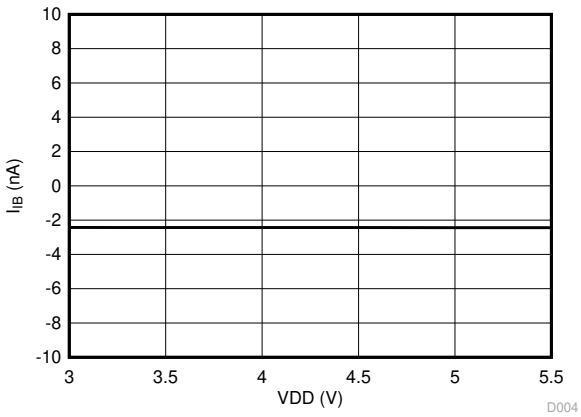


图 5-6. Input Bias Current vs Supply Voltage

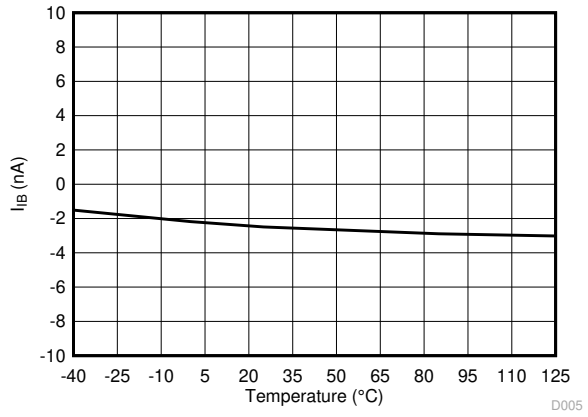


图 5-7. Input Bias Current vs Temperature

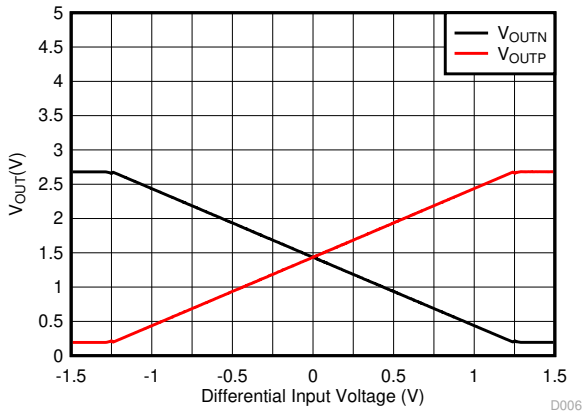


图 5-8. Output vs Differential Input Voltage

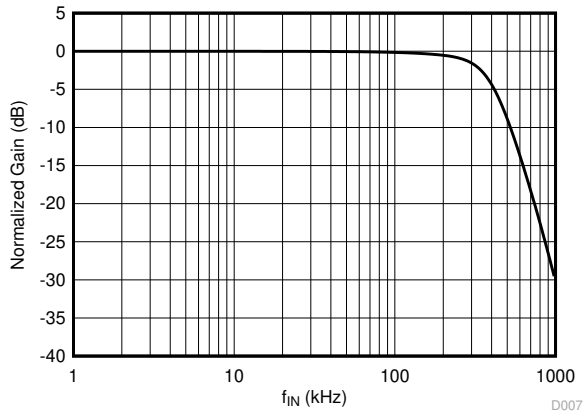


图 5-9. Normalized Gain vs Input Frequency

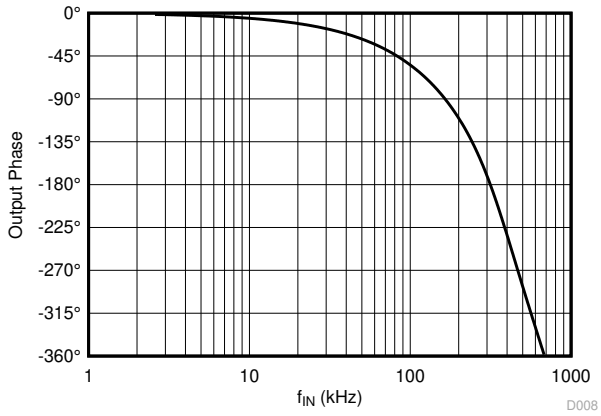


图 5-10. Output Phase vs Input Frequency

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5.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V, INN = HGND = 0V, and f_{IN} = 10 kHz (unless otherwise noted)

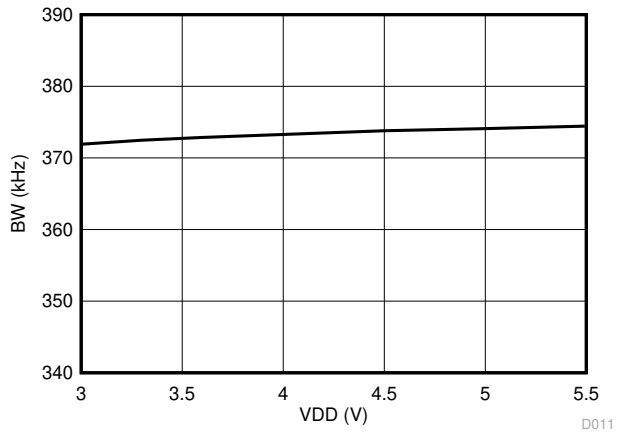


图 5-11. Output Bandwidth vs Supply Voltage

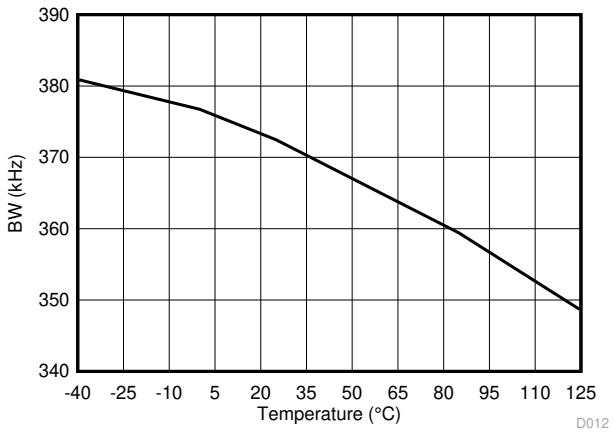


图 5-12. Output Bandwidth vs Temperature

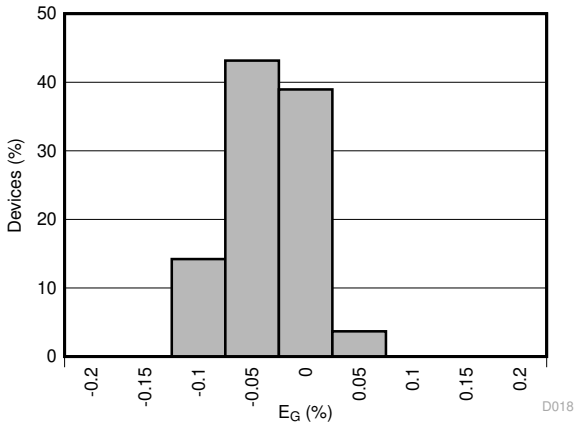


图 5-13. Gain Error Histogram

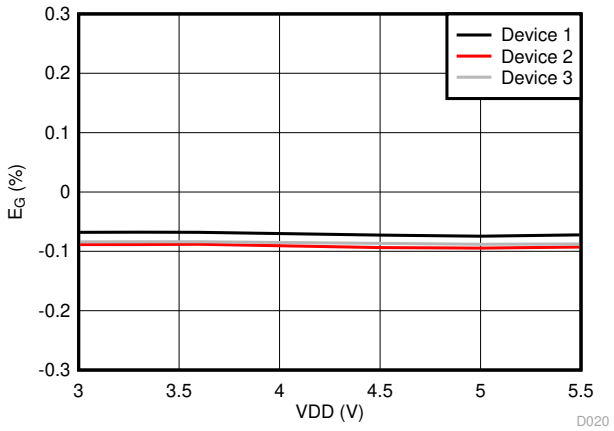


图 5-14. Gain Error vs Supply Voltage

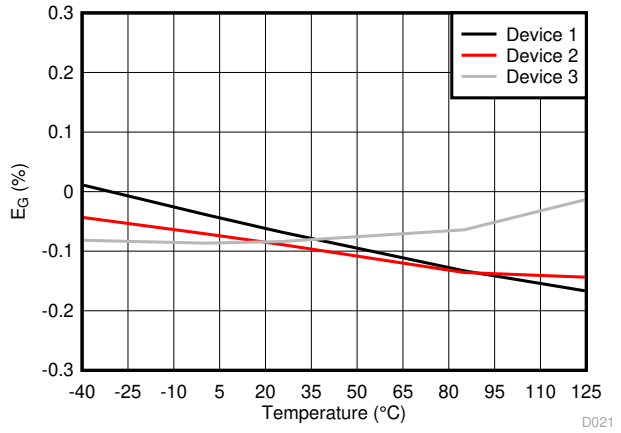


图 5-15. Gain Error vs Temperature

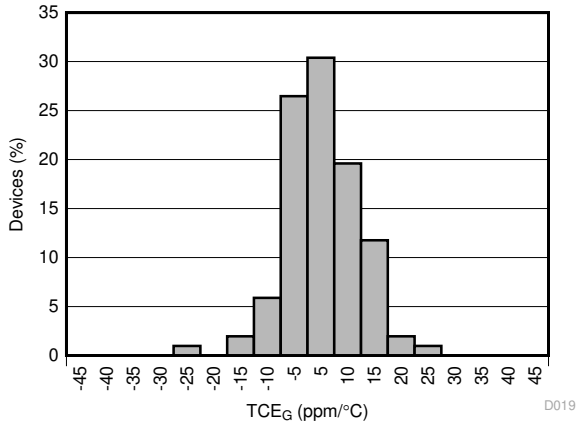


图 5-16. Gain Error Drift Histogram

5.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V, INN = HGND = 0V, and f_{IN} = 10 kHz (unless otherwise noted)

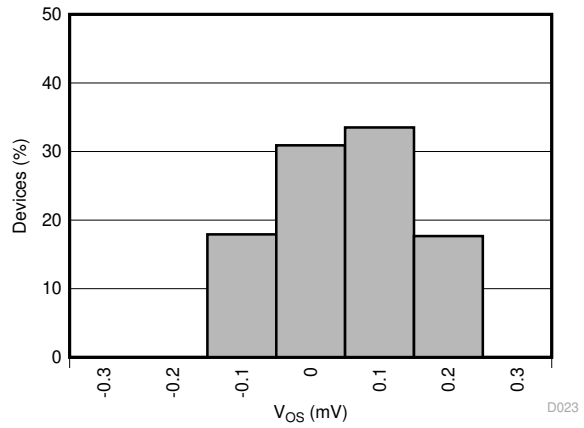


图 5-17. Offset Error Histogram

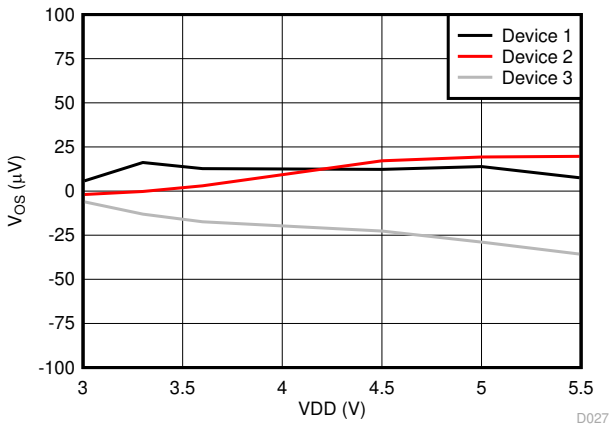


图 5-18. Offset Error vs Supply Voltage

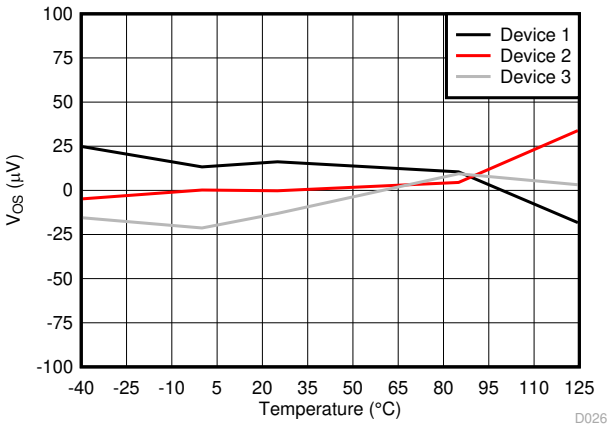


图 5-19. Offset Error vs Temperature

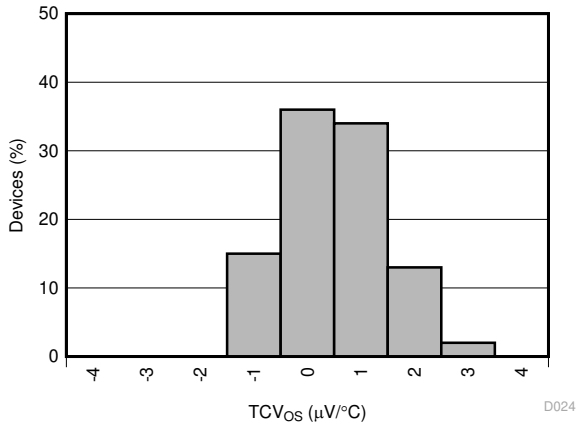


图 5-20. Offset Error Drift Histogram

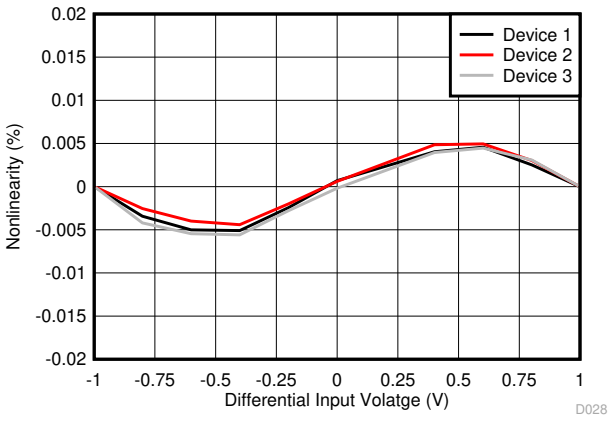


图 5-21. Nonlinearity vs Differential Input Voltage

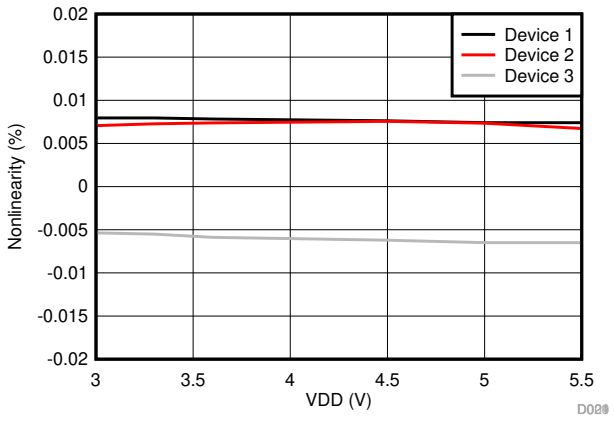


图 5-22. Nonlinearity vs Supply Voltage

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5.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V, INN = HGND = 0V, and f_{IN} = 10 kHz (unless otherwise noted)

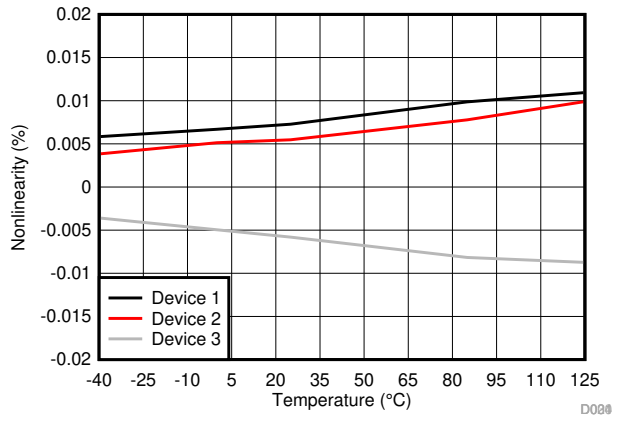


图 5-23. Nonlinearity vs Temperature

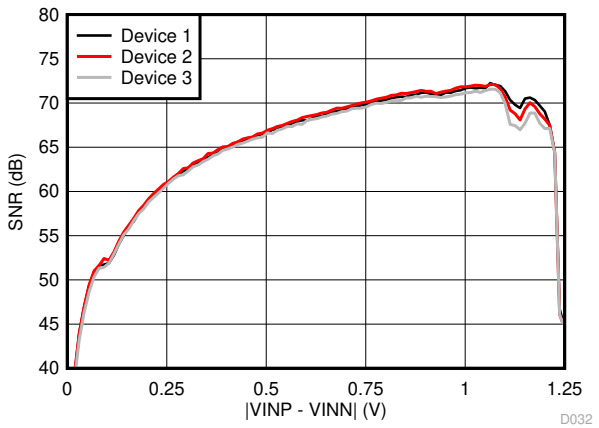


图 5-24. Signal to Noise Ratio vs Differential Input Voltage

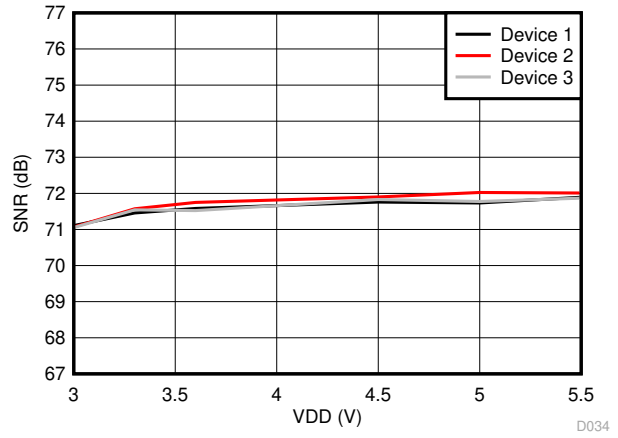


图 5-25. Signal to Noise Ratio vs Supply Voltage

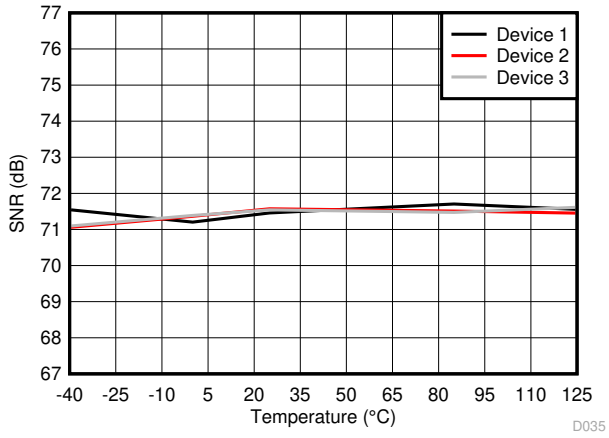


图 5-26. Signal to Noise Ratio vs Temperature

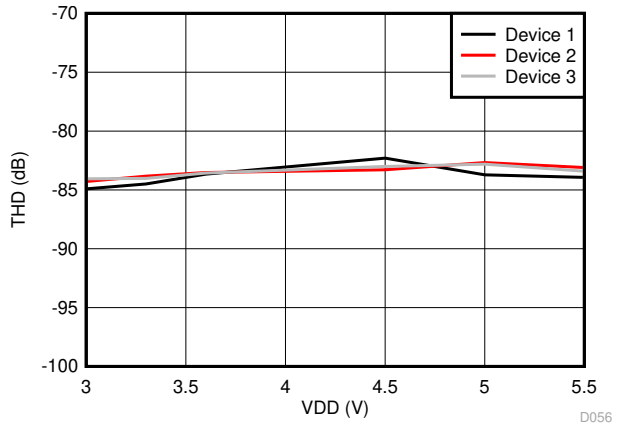


图 5-27. Total Harmonic Distortion vs Supply Voltage

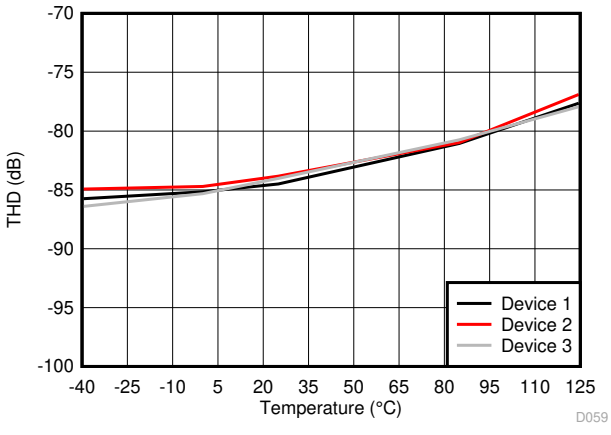


图 5-28. Total Harmonic Distortion vs Temperature

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5.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V, INN = HGND = 0V, and f_{IN} = 10 kHz (unless otherwise noted)

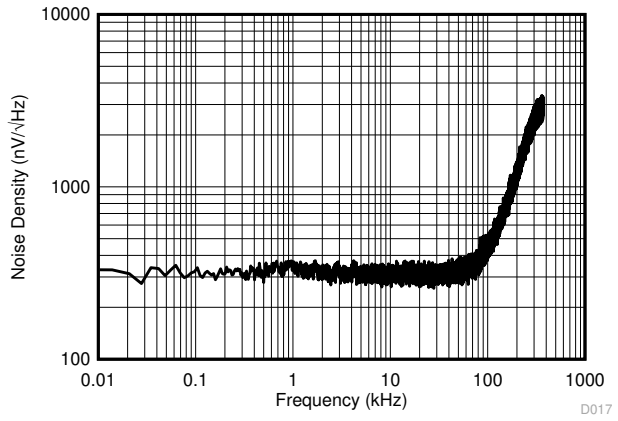


图 5-29. Input-Referred Noise Density vs Frequency

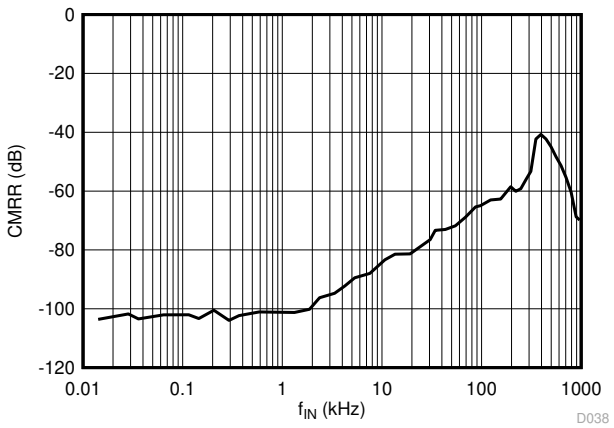


图 5-30. Common-Mode Rejection Ratio vs Input Frequency

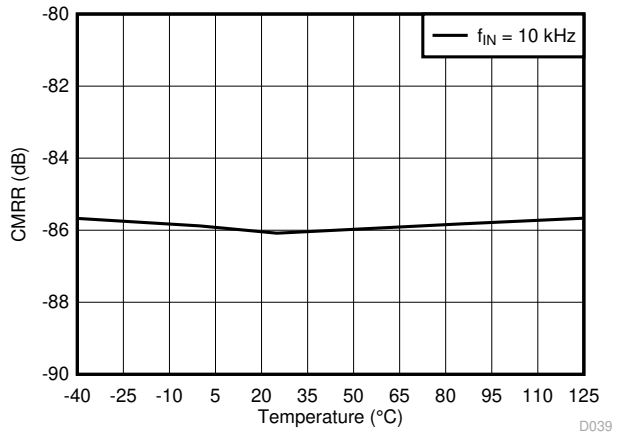


图 5-31. Common-Mode Rejection Ratio vs Temperature

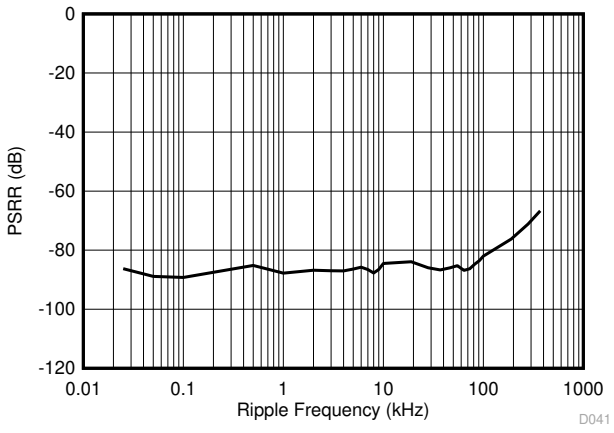


图 5-32. Power-Supply Rejection Ratio vs Ripple Frequency

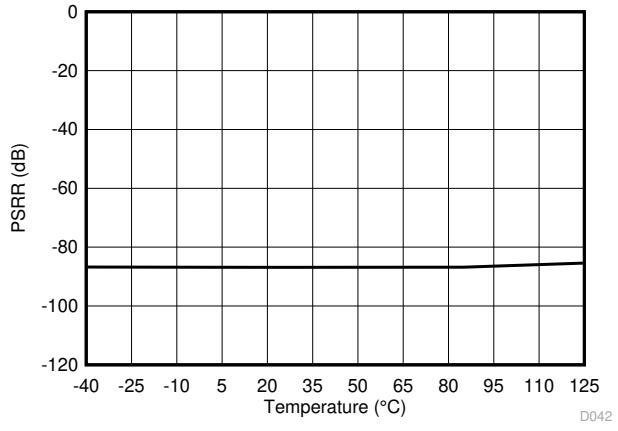


图 5-33. Power-Supply Rejection Ratio vs Temperature

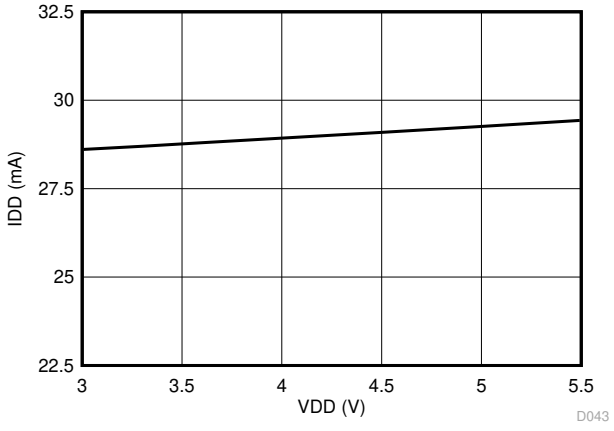


图 5-34. Input-Supply Current vs Supply Voltage

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5.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = – 1 V to 1 V, INN = HGND = 0V, and f_{IN} = 10 kHz (unless otherwise noted)

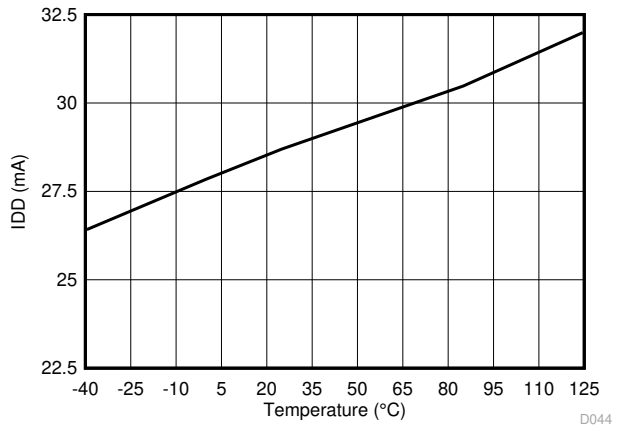


图 5-35. Input-Supply Current vs Temperature

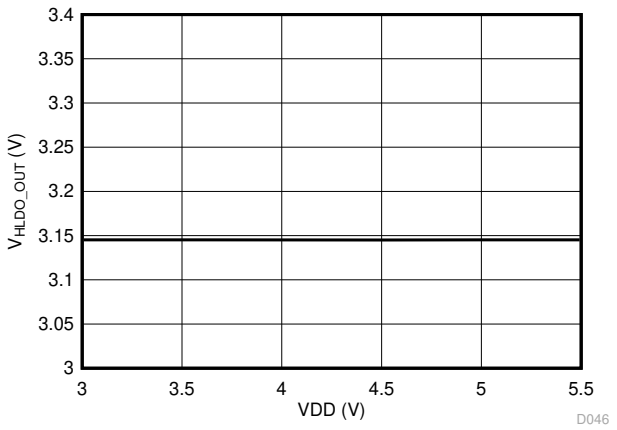


图 5-36. High-Side LDO Line Regulation

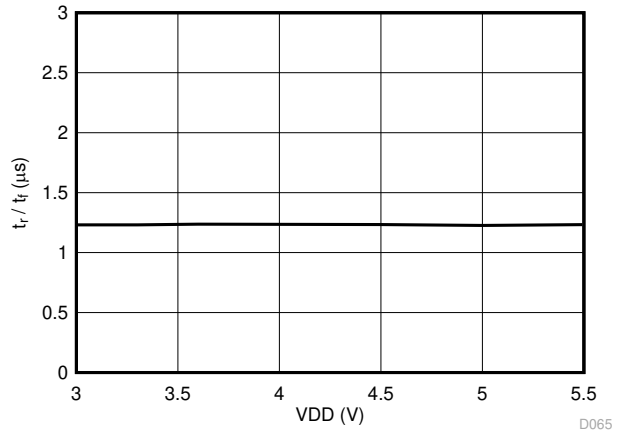


图 5-37. Output Rise And Fall Time vs Supply Voltage

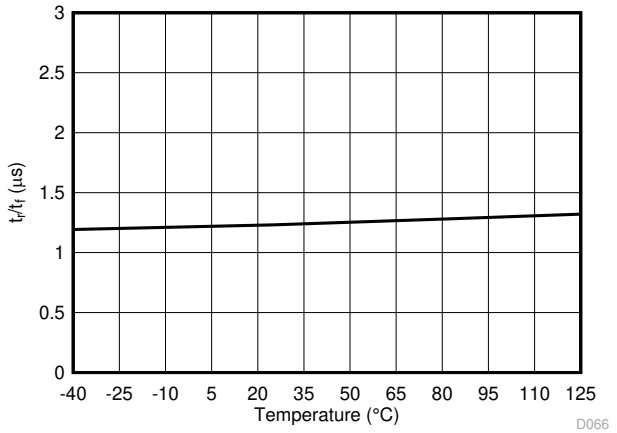


图 5-38. Output Rise And Fall Time vs Temperature

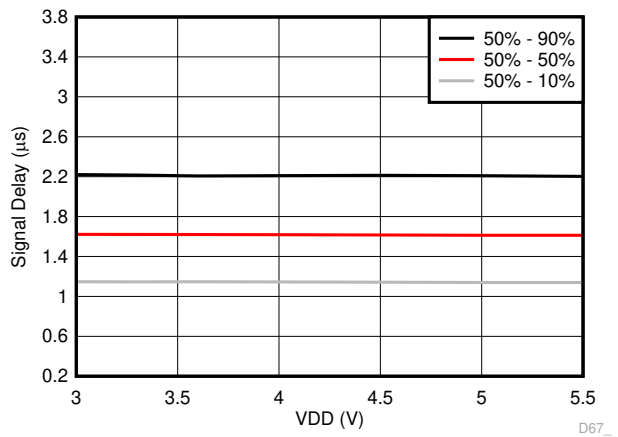


图 5-39. V_{IN} to V_{OUT} Signal Delay Time vs Supply Voltage

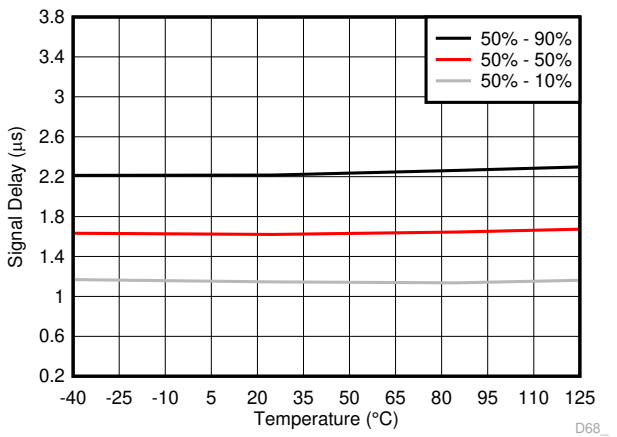


图 5-40. V_{IN} to V_{OUT} Signal Delay Time vs Temperature

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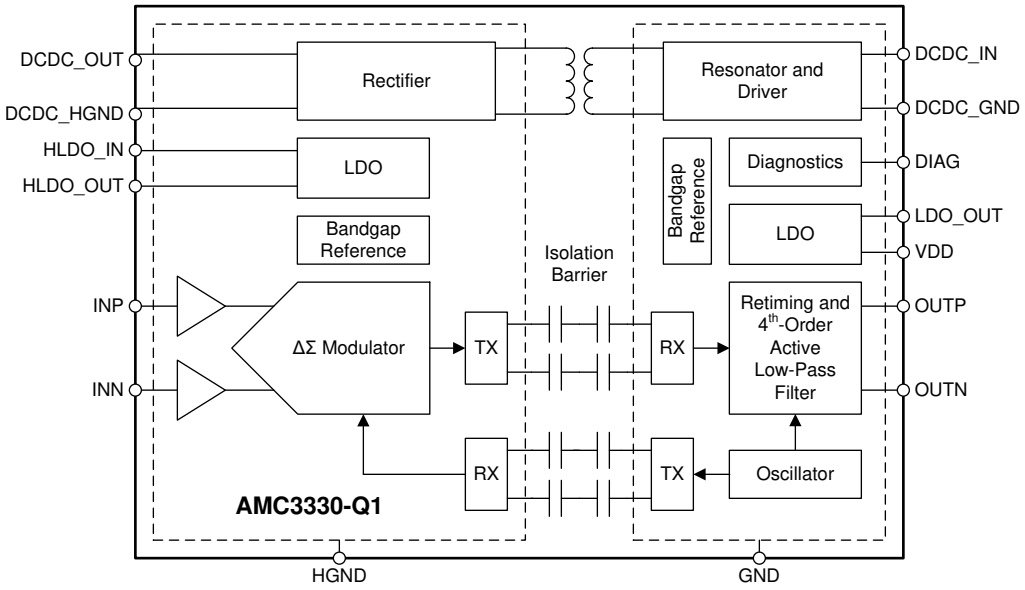
6 Detailed Description

6.1 Overview

The AMC3330-Q1 is a fully-differential, precision, isolated amplifier with high input impedance, and an integrated DC/DC converter that allows the device to be supplied from a single 3.3-V or 5-V voltage supply source on the low side. The input stage of the device drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator uses an internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (termed TX in the *Functional Block Diagram*) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential analog output.

The *Functional Block Diagram* shows a block diagram of the AMC3330-Q1. The 1.2-GΩ differential input impedance of the analog input stage supports low gain-error signal-sensing in high-voltage applications using high-impedance resistor dividers.
The signal path is isolated by a double capacitive silicon-dioxide (SiO_2) insulation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Input

The input stage of the AMC3330-Q1 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Isolation Channel Signal Transmission* section. The high-impedance, and low bias-current input of the AMC3330-Q1 makes the device suitable for isolated, high-voltage-sensing applications that typically employ high-impedance resistor dividers.

There are two restrictions on the analog input signals (INP and INN). First, if the input voltage exceeds the input range specified in the *Absolute Maximum Ratings* table, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. Second, the linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range V_{FSR} and within the specified input common-mode voltage range V_{CM} as specified in the *Recommended Operating Conditions* table.

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6.3.2 Isolation Channel Signal Transmission

The AMC3330-Q1 uses an on-off keying (OOK) modulation scheme to transmit the modulator output-bitstream across the capacitive SiO_2-based isolation barrier. 图 6-1 shows the block diagram of an isolation channel. The transmitter modulates the bitstream at TX IN with an internally generated, 480-MHz carrier and sends a burst across the isolation barrier to represent a digital *one* and sends a *no signal* to represent the digital *zero*. The receiver demodulates the signal after advanced signal conditioning and produces the output. The symmetrical design of each isolation channel improves the common-mode transient immunity (CMTI) performance and reduces the radiated emissions caused by the high-frequency carrier.

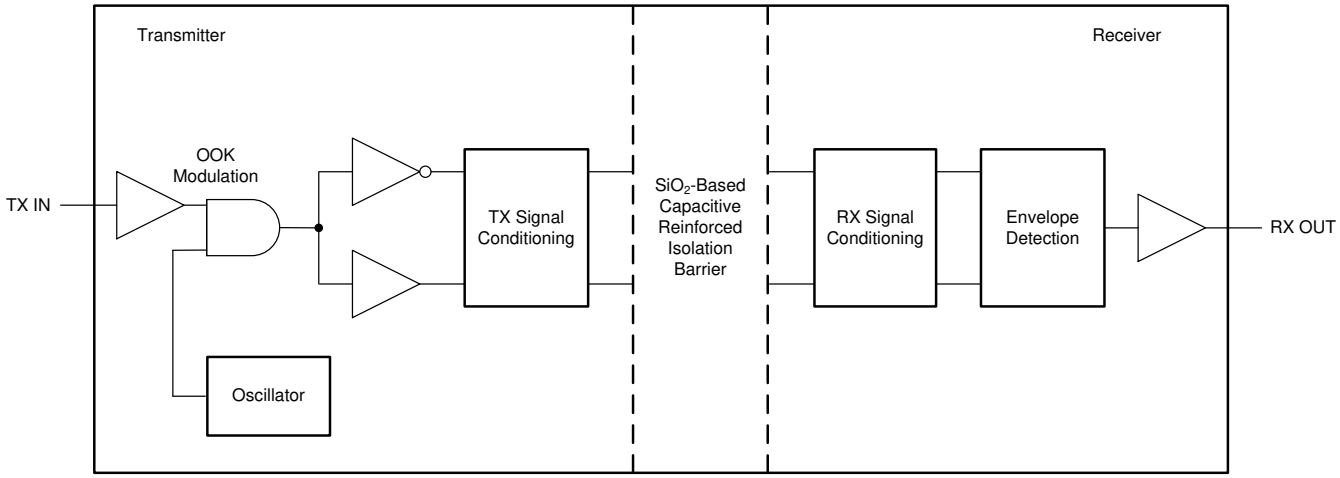


图 6-1. Block Diagram of an Isolation Channel

图 6-2 shows the concept of the on-off keying scheme.

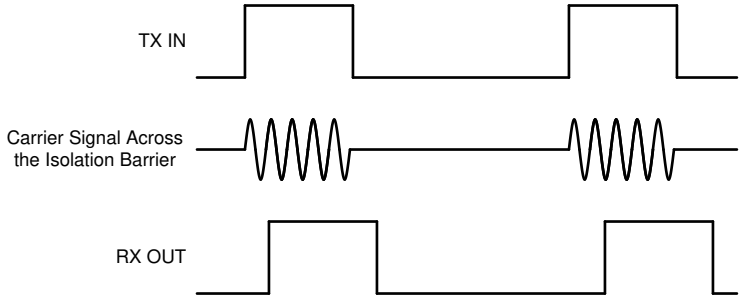


图 6-2. OOK-Based Modulation Scheme

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6.3.3 Analog Output

The AMC3330-Q1 offers a differential analog output comprised of the OUTP and OUTN pins. For differential input voltages (V_{INP} – V_{INN}) in the range from –1 V to 1 V, the device provides a linear response with a nominal gain of 2. For example, for a differential input voltage of 1 V, the differential output voltage (V_{OUTP} – V_{OUTN}) is 2 V. At zero input (INP shorted to INN), both pins output the same voltage, V_{CMout}, as specified in the *Electrical Characteristics* table. For absolute differential input voltages greater than 1.0 V but less than 1.25 V, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate as shown in 图 6-3 if the differential input voltage exceeds the $V_{Clipping}$ value.

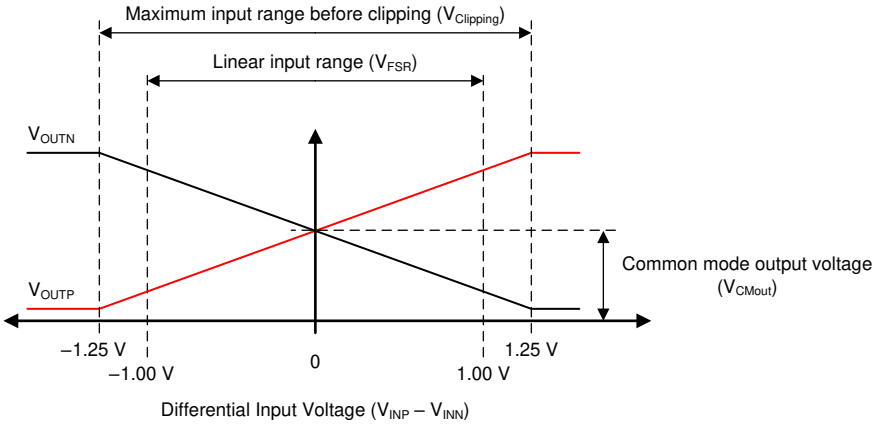


图 6-3. AMC3330-Q1 Output Behavior

The AMC3330-Q1 provides a fail-safe output that simplifies diagnostics on system level. The fail-safe output is active when the integrated DC/DC converter or hgh-side LDO don't deliver the required supply voltage for the high-side of the device. 图 6-4 and 图 6-5 illustrate the fail-safe output of the AMC3330-Q1 that is a negative differential output voltage value that does not occur under normal operating conditions. Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for the fail-safe detection on system level.

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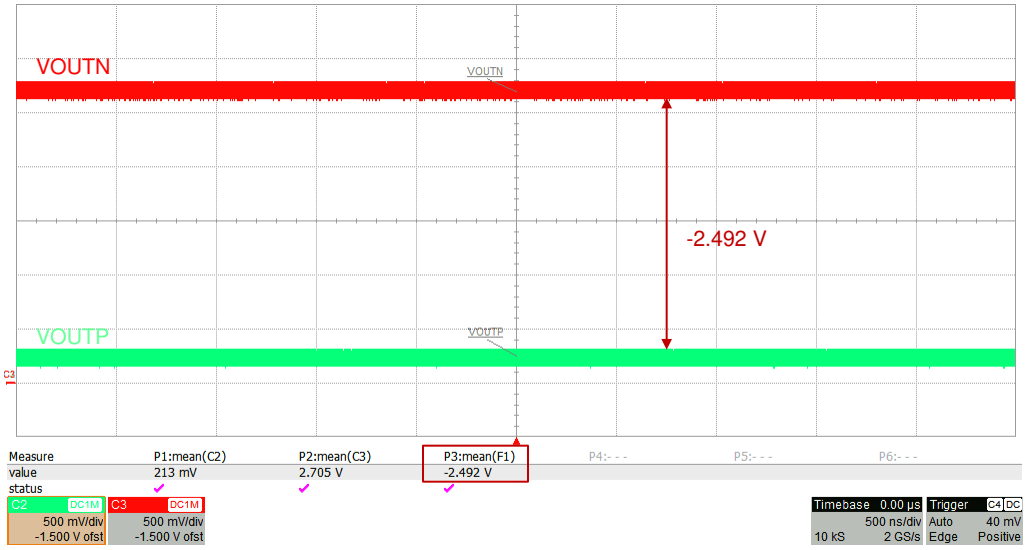


图 6-4. Typical Negative Clipping Output of the AMC3330-Q1



图 6-5. Typical Fail-Safe Output of the AMC3330-Q1

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6.3.4 Isolated DC/DC Converter

The AMC3330-Q1 offers a fully integrated isolated DC/DC converter that includes the following components illustrated in the *Functional Block Diagram*:

- Low-dropout regulator (LDO) on the low-side to stabilize the supply voltage VDD that drives the low-side of the DC/DC converter
- Low-side full-bridge inverter and drivers
- Laminate-based, air-core transformer for high immunity to magnetic fields
- High-side full-bridge rectifier
- High-side LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path

The DC/DC converter uses a spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronous to the operation of the $\Delta\Sigma$ modulator to minimize interference with data transmission and support the high analog performance of the device.

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC3330-Q1 and can source up to 1 mA of additional current (I_H) for an optional auxiliary circuit such as an active filter, pre-amplifier, or comparator.

6.3.5 Diagnostic Output and Fail-Safe Behavior

The open-drain DIAG pin can be monitored to confirm the device is operational, and the output voltage is valid. During power-up, the DIAG pin is actively held low until the high-side supply is in regulation and the device operates properly. The DIAG pin is actively pulled low if:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high-side). The amplifier outputs are driven to negative full-scale.
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds V_{DCDCUV} and V_{HLDOUV} as sepecified in the *Electrical Characteristics* table. In this case, the low-side may still receive data from the high-side but the data may not be valid. The amplifier outputs are driven to negative full-scale.

During normal operation, the DIAG pin is in a high-impedance state. Connect the DIAG pin to a pull-up supply through a resistor or leave open if not used.

6.4 Device Functional Modes

The AMC3330-Q1 is operational when the power supply VDD is applied, as specified in the *Recommended Operating Conditions* table.

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7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The low input bias current, AC and DC errors, and temperature drift make the AMC3330-Q1 a high-performance solution for applications where voltage measurement with high common-mode levels is required.

7.2 Typical Application

Isolated amplifiers are widely used for voltage measurements in high-voltage applications that must be isolated from a low-voltage domain. Typical applications are AC line voltage measurements at the input of a power factor correction (PFC) stage of an onboard charger (OBC). Other applications are DC measurements at the output of a PFC stage or DC/DC converter, or phase voltage measurements in traction inverters. The AMC3330-Q1 integrates an isolated power supply for the high-voltage side and therefore is particularly easy to use in applications that do not have a high-side supply readily available or where a high-side supply is referenced to a different ground potential than the signal to be measured.

图 7-1 illustrates a simplified schematic of the AMC3330-Q1 in an OBC where the AC phase voltage on the grid-side must to be measured. At that location in the system, there is no supply readily available for powering the isolated amplifier. The integrated isolated power supply, together with its bipolar input voltage range, makes the AMC3330-Q1 ideally suited for AC line-voltage sensing. In this example, the output current of the PFC is sensed by the AMC3301-Q1 across a shunt resistor on the positive DC-link rail where there is also no suitable supply available for powering the isolated amplifier. The integrated power-supply of the AMC3301-Q1 eliminates that problem and enables current sensing at optimal locations for the system.

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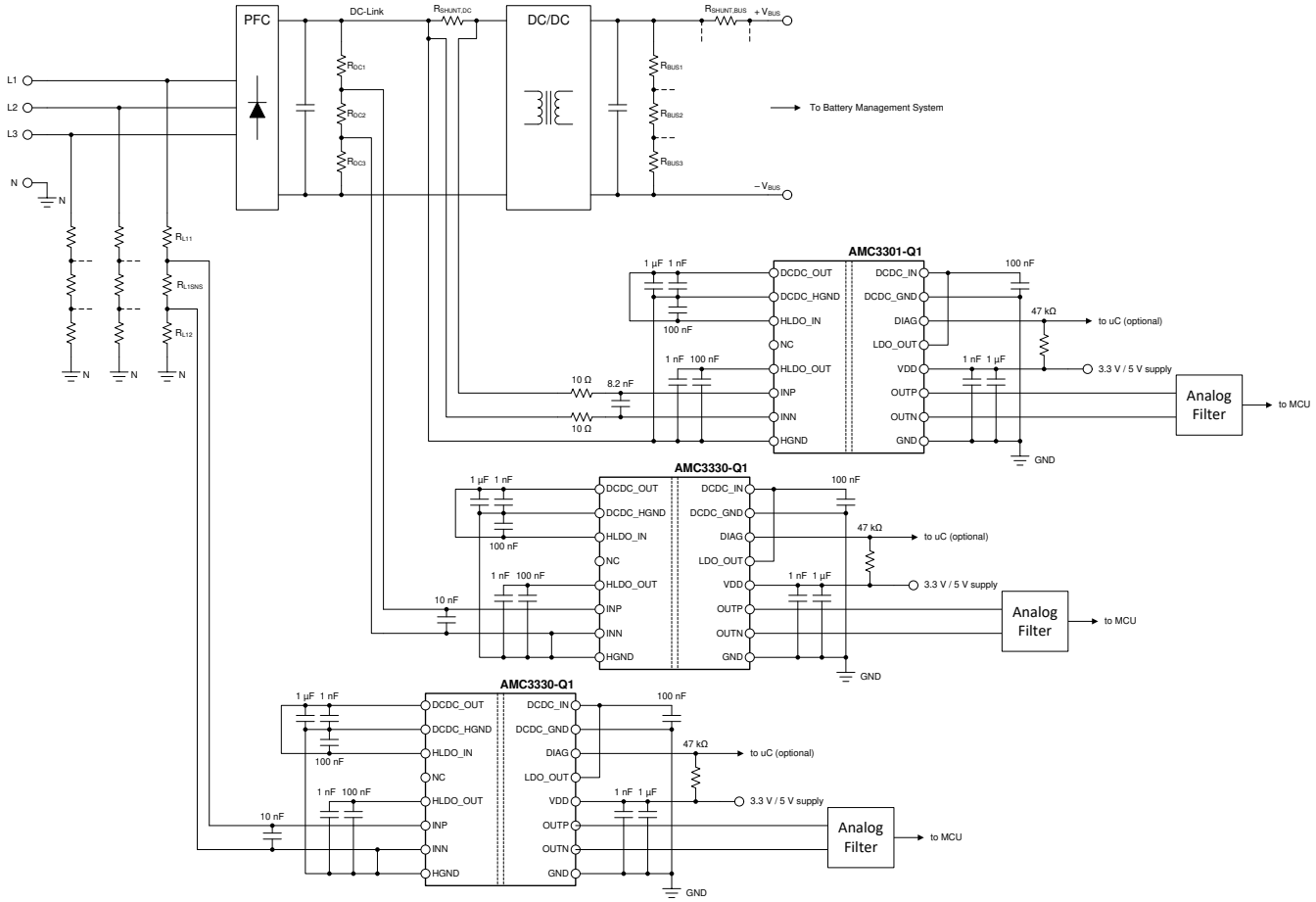


图 7-1. The AMC3330-Q1 in an OBC Application

7.2.1 Design Requirements

表 7-1 lists the parameters for this typical application.

表 7-1. Design Requirements

PARAMETER	VALUE
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the sensing resistor for a linear response	1 V (maximum)
Current through the resistive divider, I_{CROSS}	100 µA (maximum)

7.2.2 Detailed Design Procedure

Use Ohm's Law to calculate the minimum total resistance of the resistive divider to limit the cross current to the desired value ($R_{TOTAL} = V_{Lx} / I_{CROSS}$) and the required sense resistor value to be connected to the AMC3330-Q1 input: $R_{SNS} = V_{FSR} / I_{CROSS}$.

Consider the following two restrictions to choose the proper value of the sense resistor R_{SNS}:

- The voltage drop on R_{SNS} caused by the nominal voltage range of the system must not exceed the recommended input voltage range: $V_{SNS} \leqslant V_{FSR}$
- The voltage drop on R_{SNS} caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output: $V_{SNS} \leqslant V_{Clipping}$

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表 7-2 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 120-V and 230-V AC line voltages.

表 7-2. Resistor Value Examples

PARAMETER	120-V_{RMS} LINE VOLTAGE	230-V_{RMS} LINE VOLTAGE
Peak voltage	170 V	325 V
Resistive divider resistors R_{L11}, R_{L12}	845 kΩ	1.62 MΩ
Sense resistor R_{SNS}	10 kΩ	10 kΩ
Current through resistive divider I_{CROSS}	100 µA	100 µA
Resulting voltage drop on sense resistor V_{SNS}	1.00 V	1.00 V

7.2.2.1 Input Filter Design

TI recommends placing an RC filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the internal ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

Most voltage sensing applications use high-impedance resistor dividers in front of the isolated amplifier to scale down the input voltage. In this case, a single capacitor as given in 图 7-2 is sufficient to filter the input signal.

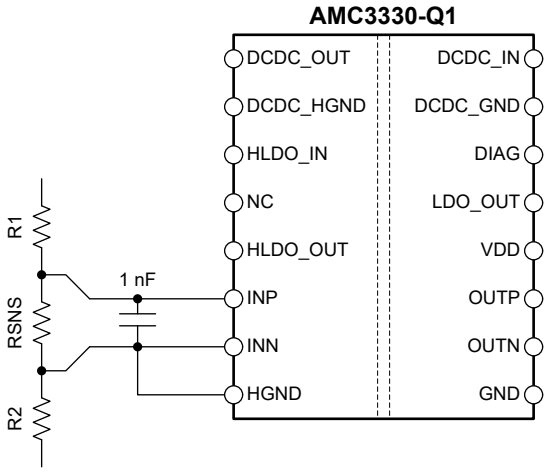


图 7-2. Differential Input Filter

7.2.2.2 Differential to Single-Ended Output Conversion

For systems using single-ended input ADCs to convert the analog output voltage into digital, 图 7-3 shows an example of a TLV313-Q1 -based signal conversion and filter circuit. With R1 = R2 = R3 = R4, the output voltage equals (V_{OUTP} – V_{OUTN}) + V_{REF}. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, R1 = R2 = R3 = R4 = 10 kΩ and C1 = C2 = 1000 pF yields good performance.

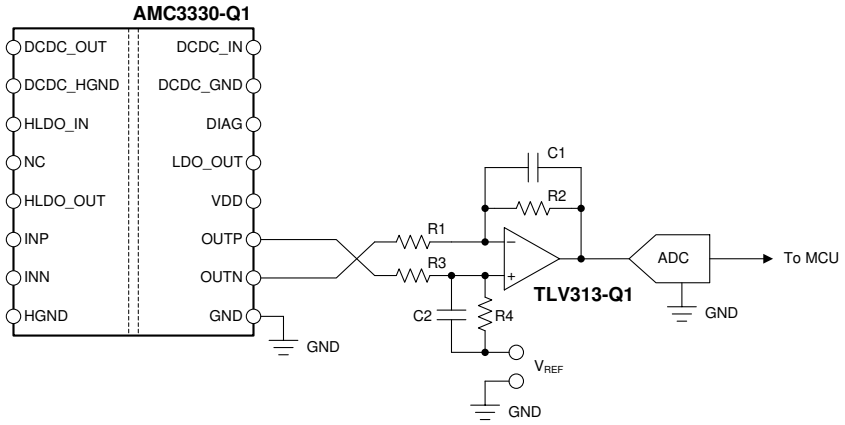


图 7-3. Connecting the AMC3330-Q1 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

7.2.3 Application Curve

图 7-4 shows the typical full-scale step response of the AMC3330-Q1.

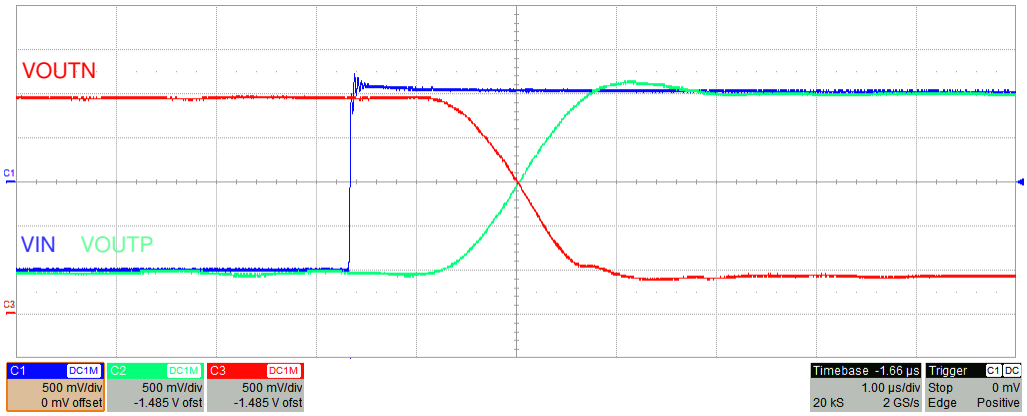


图 7-4. Step Respose of the AMC3330-Q1

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7.3 Best Design Practices

Do not leave the analog inputs INP and INN of the AMC3330-Q1 unconnected (floating) when the device is powered up on the high-side. If the device input is left floating, the bias current may generate a negative input voltage that exceeds the specified input voltage range and the output of the device is invalid.

Connect the high-side ground (HGND) to INN, either directly or through a resistive path. A DC current path between INN and HGND is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the *Recommended Operating Conditions* table.

The high-side LDO sources a limited amount of current (I_H) to power external circuitry. Do not overload the high-side LDO.

The low-side LDO does not output a constant voltage and is not intended for powering any external circuitry. Do not connect any external load to the LDO_OUT pin.

7.4 Power Supply Recommendations

The AMC3330-Q1 is powered from the low-side power supply (VDD) with a nominal value of 3.3 V (or 5 V). TI recommends a low-ESR decoupling capacitor of 1 nF (C8 in 图 7-5) placed as close as possible to the VDD pin, followed by a 1-µF capacitor (C9) to filter this power-supply path.

The low-side of the DC/DC converter is decoupled with a low-ESR 100-nF capacitor (C4) positioned close to the device between the DCDC_IN and DCDC_GND pins. Use a 1-µF capacitor (C2) to decouple the high-side in addition to a low-ESR, 1-nF capacitor (C3) placed as close as possible to the device and connected to the DCDC_OUT and DCDC_HGND pins.

For the high-side LDO, use low-ESR capacitors of 1-nF (C6), placed as close as possible to the AMC3330-Q1, followed by a 100-nF decoupling capacitor (C5).

The ground reference for the high-side (HGND) is derived from the terminal of the sense resistor which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace to make this connection but shorting HGND to INN directly at the device input is also acceptable. The high-side DC/DC ground terminal(DCDC_HGND) is shorted to HGND directly at the device pins.

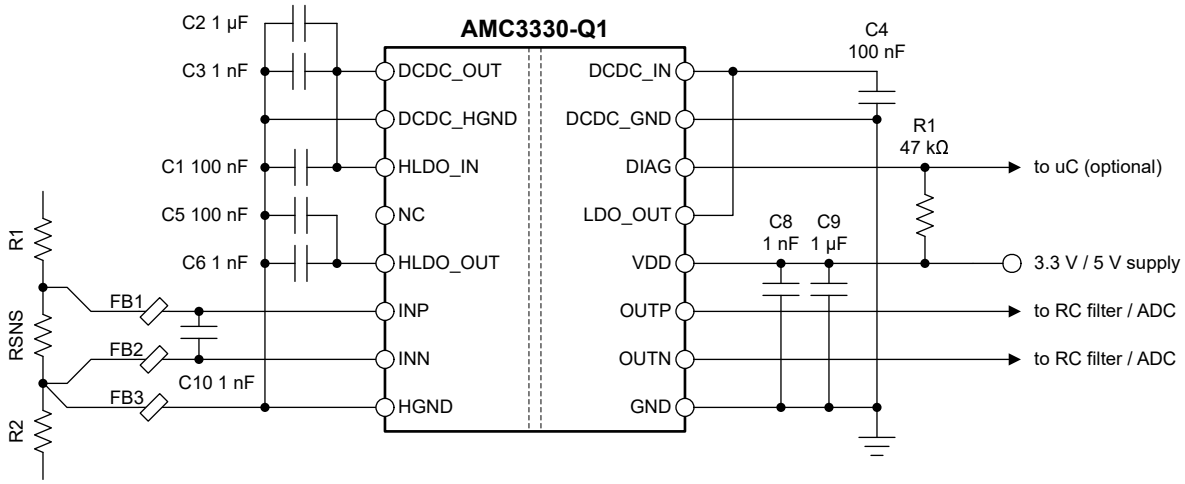


图 7-5. Decoupling the AMC3330-Q1

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) capacitors typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

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The *Best Practices to Attenuate AMC3301 Family Radiated Emissions EMI* application note is available for download at www.ti.com.

表 7-3 lists components suitable for use with the AMC3330-Q1. This list is not exhaustive. Other components may exist that are equally suitable (or better), however these listed components have been validated during the development of the AMC3330-Q1.

表 7-3. Recommended External Components

DESCRIPTION		PART NUMBER	MANUFACTURER	SIZE (EIA, L x W)
VDD				
C8	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm
C9	1 µF ± 10%, X7R, 25 V	12063C105KAT2A	AVX	1206, 3.2 mm x 1.6 mm
DC/DC CONVERTER				
C4	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C3	1 nF ± 10%, X7R, 50 V	C0603C102K5RACTU	Kemet	0603, 1.6 mm x 0.8 mm
C2	1 µF ± 10%, X7R, 25 V	CGA3E1X7R1E105K080AC	TDK	0603, 1.6 mm x 0.8 mm
HLDO				
C1	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C5	100 nF ± 5%, NP0, 50 V	C3216NP01H104J160AA	TDK	1206, 3.2 mm x 1.6 mm
C6	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm
FERRITE BEADS				
FB1, FB2, FB3	Ferrite bead(1)	74269244182	Wurth Elektronik	0402, 1.0mm × 0.5mm
		BLM15HD182SH1	Murata	0402, 1.0mm × 0.5mm
		BKH1005LM182-T	Taiyo Yuden	0402, 1.0mm × 0.5mm

(1) No ferrite beads are used for parametric validation.

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7.5 Layout

7.5.1 Layout Guidelines

图 7-6 shows a layout recommendation with the critical placement of the decoupling capacitors. The same component reference designators are used as in the *Power Supply Recommendations* section. Decoupling capacitors are placed as close as possible to the AMC3330-Q1 supply pins. For best performance, place the sense resistor close to the INP and INN inputs of the AMC3330-Q1 and keep the layout of both connections symmetrical.

This layout is used on the AMC3330-Q1 EVM and supports CISPR-25 compliant electromagnetic radiation levels.

7.5.2 Layout Example

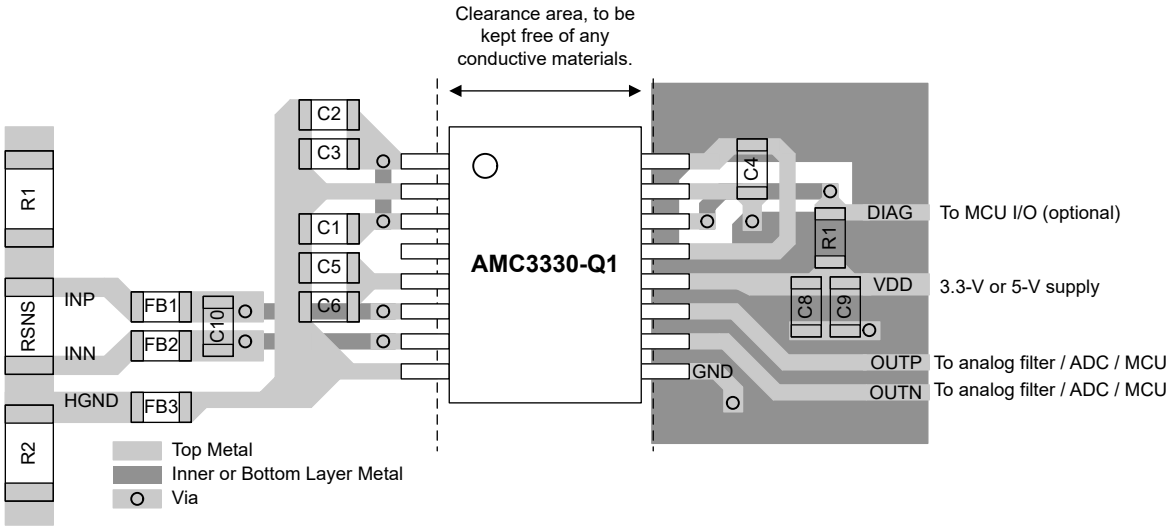


图 7-6. Recommended Layout of the AMC3330-Q1

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Texas Instruments, *Isolation Glossary*

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application note
- Texas Instruments, *AMC3301-Q1 Precision, ±250-mV Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter* data sheet
- Texas Instruments, *TLVx313-Q1 Low-Power, Rail-to-Rail In/Out, 750- μV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

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9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (October 2020) to Revision B (September 2024) **Page**

- 通篇将增强型隔离安全相关认证从 *VDE V 0884-11* 更改为 *DIN EN IEC 60747-17 (VDE 0884-17)* 1
- 添加了最后一个*应用*要点....1
- 更改了*应用示例* 图....1
- Changed Absolute Maximum Ratings: changed max for DIAG pin from 5.5 V to 6.5 V....4
- Added analog output capacitive and resistive drive capability specification....4
- Updated Barrier capacitance specification from 3.5 pF to 4.5 pF....6
- Changed isolation standard from DIN VDE V 0884-11 (VDE V 0884-11) to DIN EN IEC 60747-17 (VDE 0884-17) and updated the Insulation Specifications and Safety-Related Certifications tables accordingly....7
- THD footnote added....8
- Added DIGITAL OUTPUT (DIAG) electrical specifications....8
- Added VDD_{UV} and VDD_{POR} specifications....8
- Added I_H specification for 4.5 V ⩽ VDD ⩽ 5.5 V....8
- Deleted duplicate column in *Resistor Value Examples* table....24
- Changed *Differential Input Filter* figure....25
- Added high-side and low-side LDO external load discussion to *Best Design Practices* section....27
- Changed *Power Supply Recommendations* section: Changed *Decoupling the AMC3330-Q1* figure, added *Best Practices to Attenuate AMC3301 Family Radiated Emissions EMI* reference and added ferrite bead section to *Recommended External Components* table....27
- Changed OUTP, OUTN, and VDD routing in *Recommended Layout of the AMC3330-Q1* figure....29

Changes from Revision * (June 2020) to Revision A (October 2020) **Page**

- 将文档状态从“预告信息”更改为“量产数据”....1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC3330QDWERQ1	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3330Q
AMC3330QDWERQ1.A	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3330Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AMC3330-Q1 :

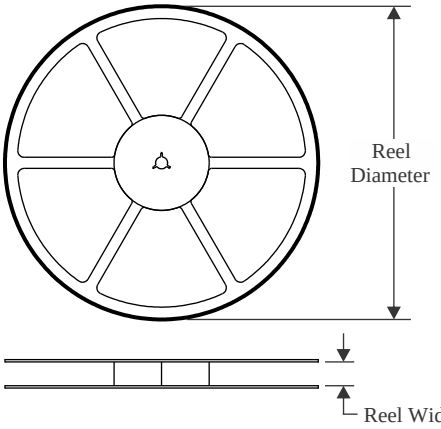
- Catalog : AMC3330

NOTE: Qualified Version Definitions:

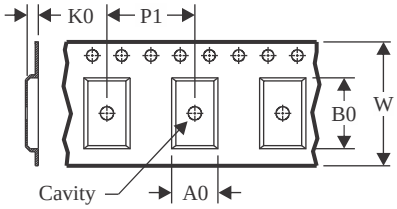
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

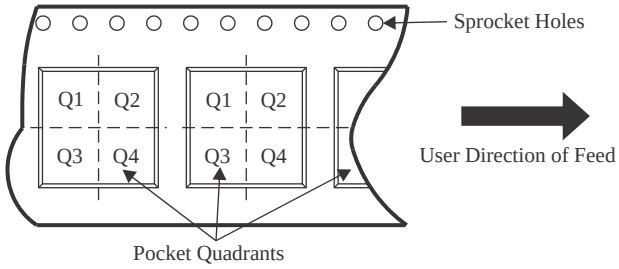


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

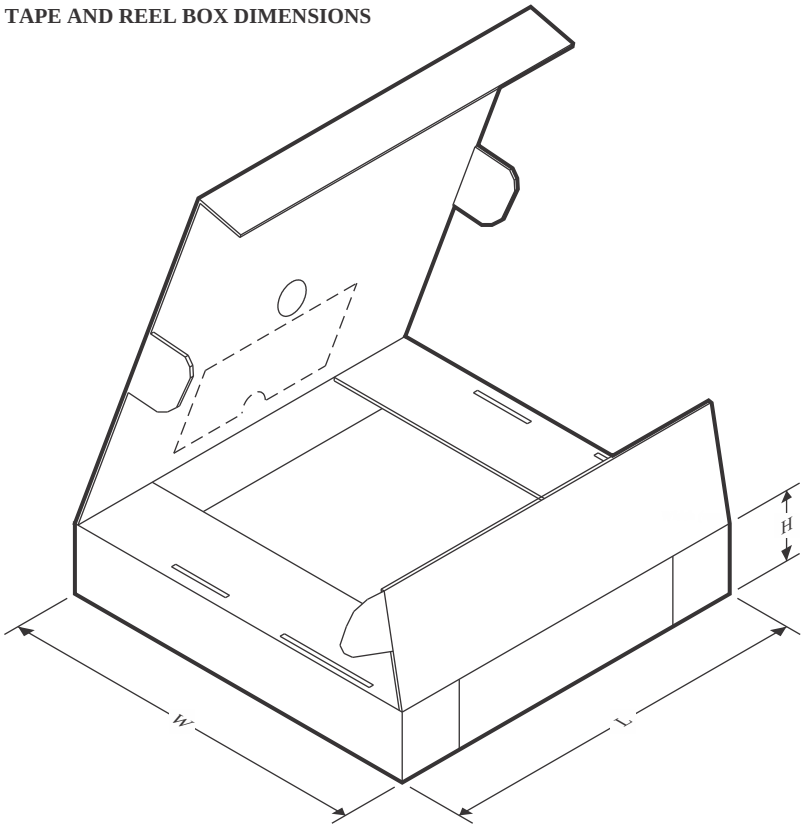
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

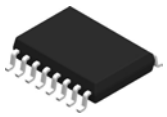
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC3330QDWERQ1	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC3330QDWERQ1	SOIC	DWE	16	2000	350.0	350.0	43.0

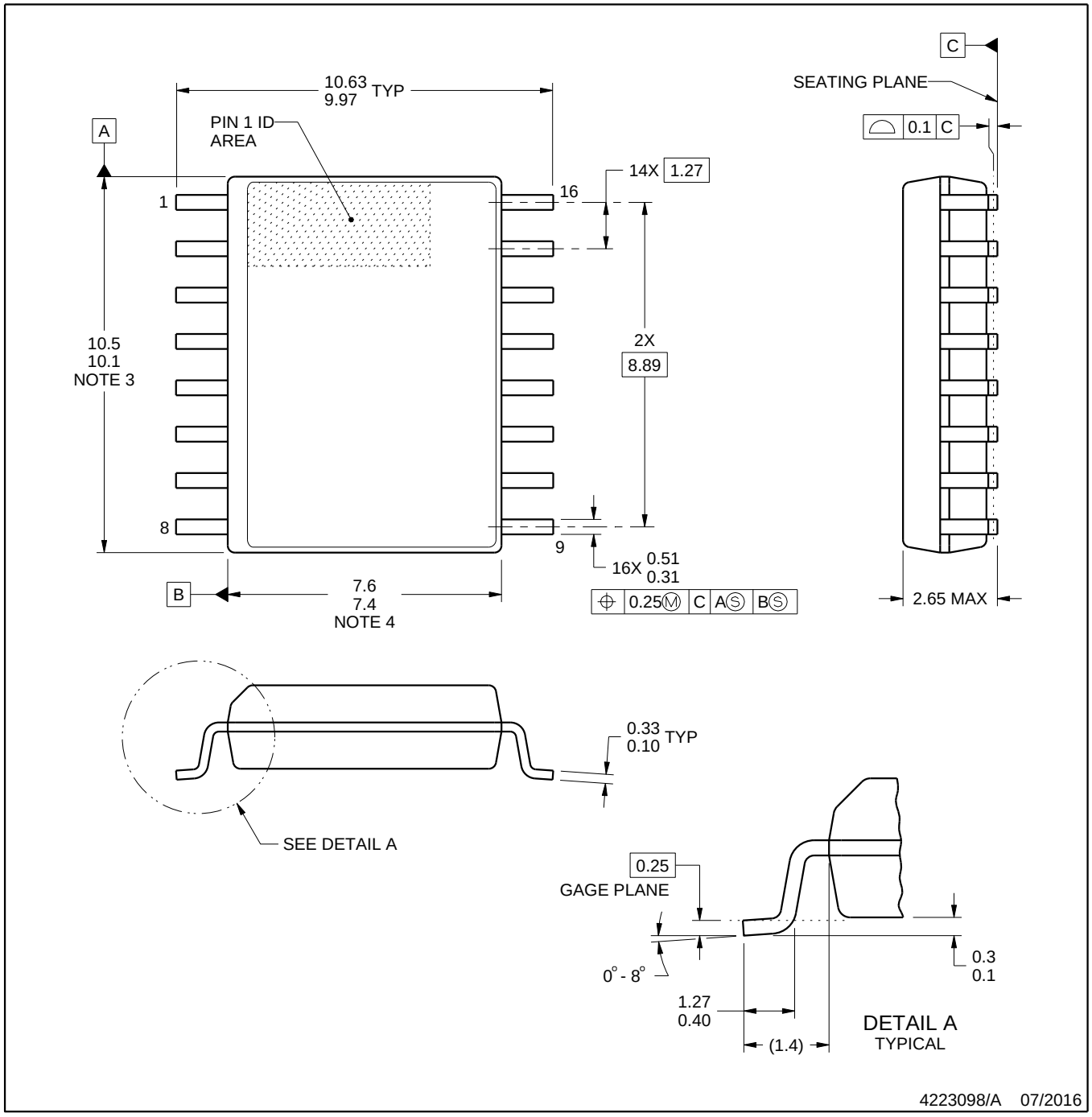


PACKAGE OUTLINE

DWE0016A

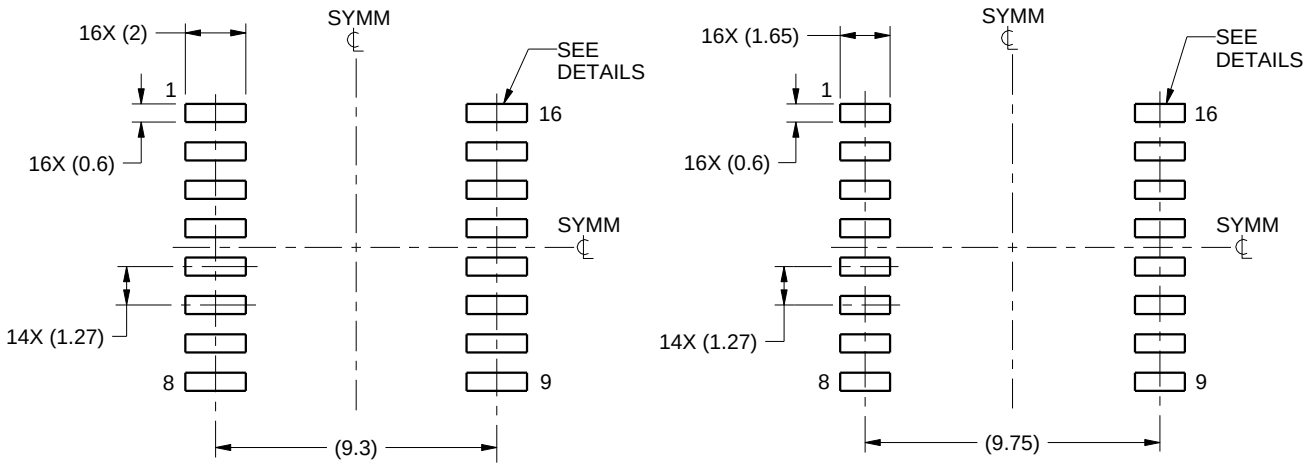
SOIC - 2.65 mm max height

SOIC



NOTES:

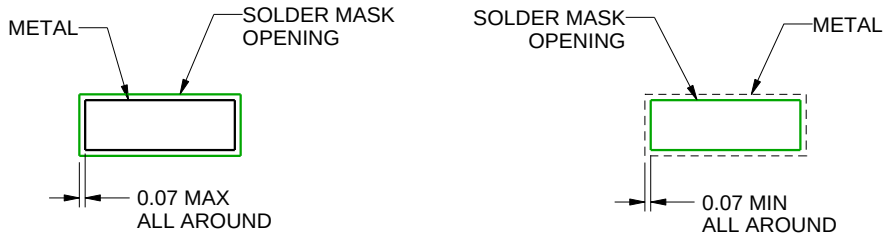
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

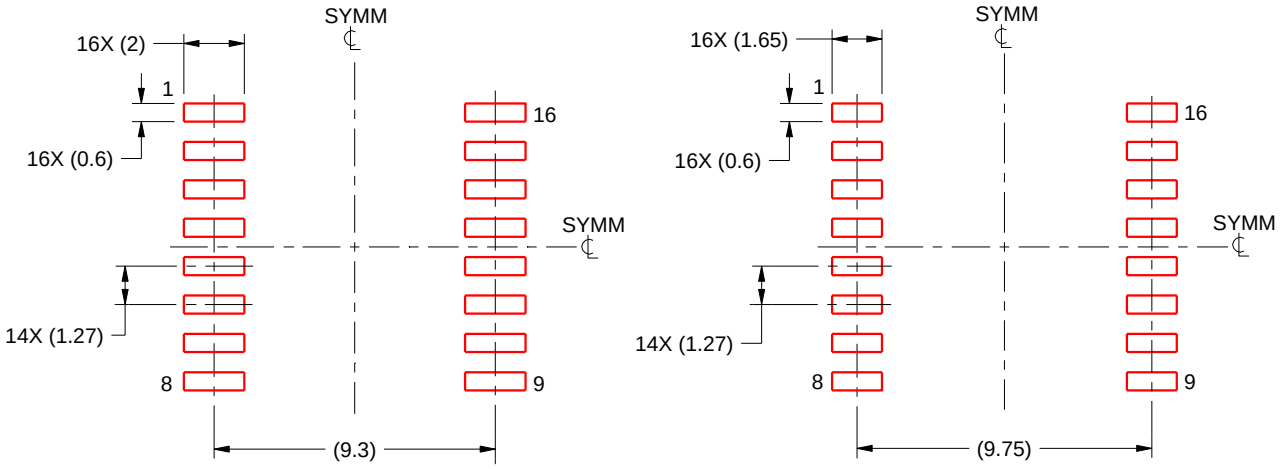
SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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