双通道 12 位 500Msps 接收器和反馈集成电路 (IC)

查询样片: ADS54T04

特性

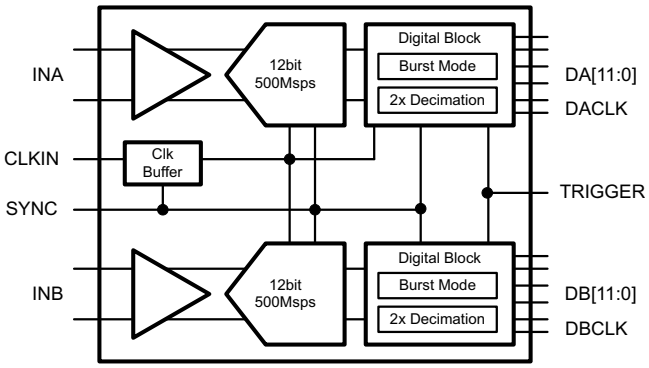
- 双通道
- **12** 位分辨率
- 最大时钟速率：**500Msps**
- 低摆幅满刻度输入：**1.0Vpp**
- 支持高阻抗输入的模拟输入缓冲器
- 输入带宽 **(3dB)**：**>1.2GHz**
- 数据输出接口：**DDR** 低压差分信令 **(LVDS)**
- **196** 引脚球状引脚栅格阵列 **(BGA)** 封装 **(12x12mm)**
- 功率耗散：每通道 **800mW**
- **f_{in} = 230MHz IF** 时的性能
  - 信噪比 **(SNR)**：**60.6dBFS**
  - 无杂散动态范围 **(SFDR)**：**77dBc**
- **f_{in} = 700MHz IF** 时的性能
  - **SNR**：**59.4dBFS**
  - **SFDR**：**70dBc**
- 接收模式：具有低通或高通滤波器的 **2** 倍抽取
- 反馈模式：针对满带宽数字预失真 **(DPD)** 反馈的猝发模式输出

应用范围

- 通信接收器
- 功率放大器线性化

说明

ADS54T04 是一款高线性双通道 12 位，500MSPS 模数转换器 (ADC)，此器件简化了针对宽带宽接收器的前端滤波器设计。 模拟输入缓冲器使片载跟踪和保持的内部切换不会干扰信号源并提供一个高阻抗输入。有两个针对输出数据的输出模式 - 它可被两倍抽取或此数据可在猝发模式中被输出。 猝发模式输出特别设计用于 DPD 反馈应用，在此类应用中，短期时间内高分辨率输出数据可用。 设计用于高 SFDR，此 ADC 在宽输入频率范围内具有低噪声性能以及出色的无杂散动态范围。 此器件采用 196 引脚 BGA 封装并且特定于整个工业温度范围内（-40°C 至 85°C）。



器件部件号	通道数量	速度等级
ADS54T02	2	750Msps
ADS54T01	1	750Msps
ADS54T04	2	500Msps

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012–2014, Texas Instruments Incorporated

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DETAILED BLOCK DIAGRAM

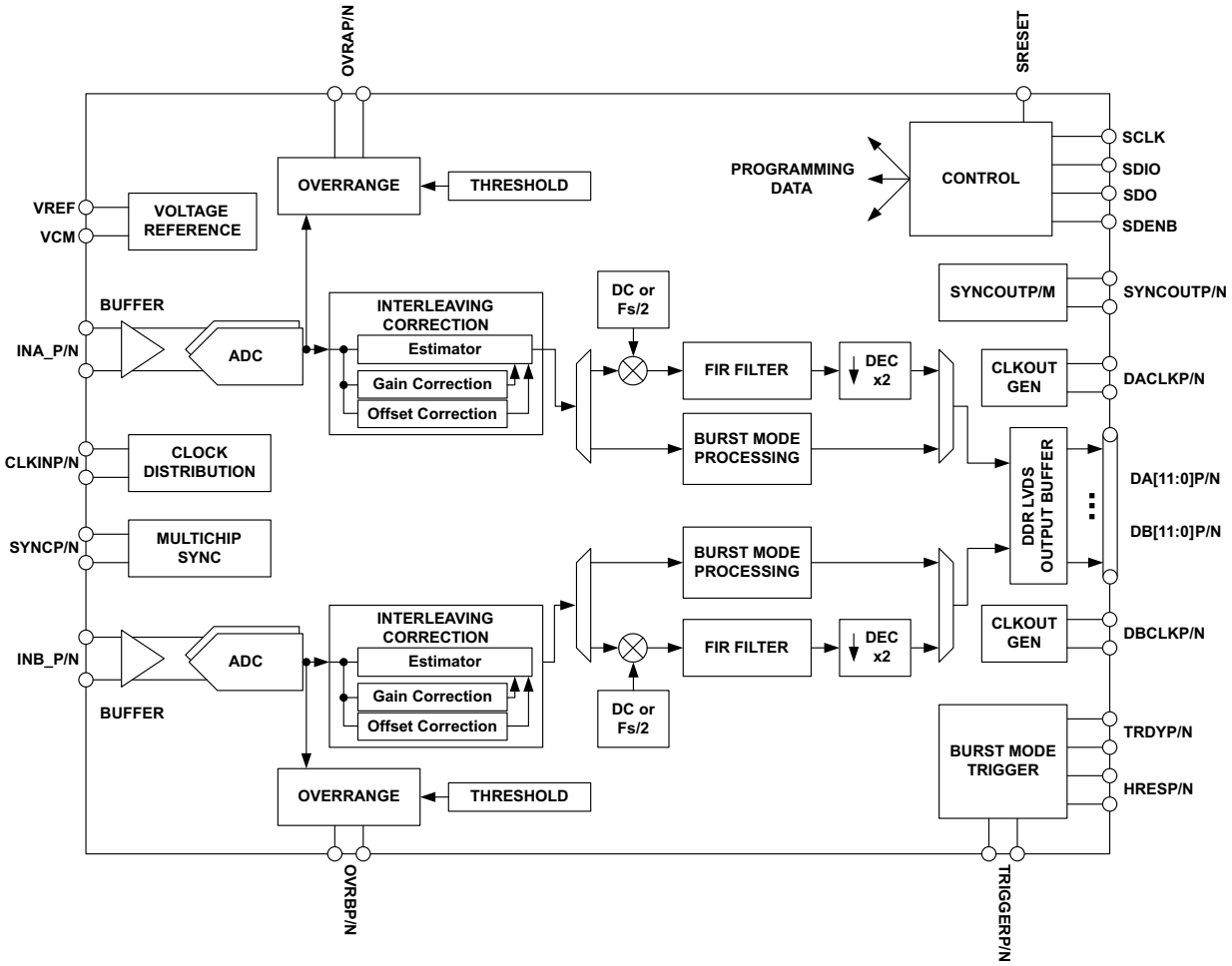


Figure 1. Detailed Block Diagram

Copyright © 2012–2014, Texas Instruments Incorporated

PINOUT INFORMATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	VREF	VCM	GND	INB_N	INB_P	GND	AVDDC	AVDDC	GND	INA_P	INA_N	GND	GND	CLKINP	14
13	SDENB	TEST MODE	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	CLKINN	13
12	SCLK	SRESET	GND	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	AVDD33	GND	AVDD33	AVDD33	12
11	SDIO	ENABLE	GND	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	AVDD18	GND	AVDD18	AVDD18	11
10	SDO	IOVDD	GND	AVDD18	GND	GND	GND	GND	GND	GND	AVDD18	GND	TRIGGERN	TRIGGERP	10
9	DVDD	DVDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	SYNCN	SYNCP	9
8	DVDD	DVDD	DVDD	DVDD	GND	GND	GND	GND	GND	GND	DVDD	DVDD	DVDD	DVDD	8
7	DB0N	DB0P	DVDD LVDS	DVDD LVDS	GND	GND	GND	GND	GND	GND	DVDD LVDS	DVDD LVDS	TRDYN	TRDYP	7
6	DB1N	DB1P	DVDD LVDS	DVDD LVDS	GND	GND	GND	GND	GND	GND	DVDD LVDS	DVDD LVDS	HRESN	HRESP	6
5	DB2N	DB2P	OVRBN	OVRBP	GND	GND	GND	GND	GND	GND	OVRAN	OVRAP	SYNC OUTN	SYNC OUTP	5
4	DB3N	DB3P	DB8P	DB10P	NC	HRESP	TRDYP	DA0P	DA2P	DA4P	DA6P	DA8P	NC	NC	4
3	DB4N	DB4P	DB8N	DB10N	NC	HRESN	TRDYN	DA0N	DA2N	DA4N	DA6N	DA8N	DA11N	DA11P	3
2	DB5N	DB5P	DB7P	DB9P	DB11P	SYNC OUTP	DBCLKP	DACLKP	DA1P	DA3P	DA5P	DA7P	DA10N	DA10P	2
1	DB6N	DB6P	DB7N	DB9N	DB11N	SYNC OUTN	DBCLKN	DACLKN	DA1N	DA3N	DA5N	DA7N	DA9N	DA9P	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 2. Pinout in DDR output mode (top down view)

PIN ASSIGNMENTS

PIN		I/O	DESCRIPTION
NAME	NUMBER		
INPUT/REFERENCE			
INA_P/N	K14, L14	I	Analog ADC A differential input signal.
INB_P/N	E14, D14	I	Analog ADC B differential input signal.
VCM	B14	O	Output of the analog input common mode (nominally 1.9V). A 0.1µF capacitor to AGND is recommended.
VREF	A14	I	Reference voltage input. A 0.1µF capacitor to AGND is recommended, but not required.
CLOCK/SYNC			
CLKINP/N	P14, P13	I	Differential input clock
SYNCP/N	P9, N9	I	Synchronization input. Inactive if logic low. When clocked in a high state initially, this is used for resetting internal clocks and digital logic and starting the SYNCOUT signal. Internal 100Ω termination.
CONTROL/SERIAL			
SRESET	B12	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Asynchronous. Internal 50kΩ pull up resistor to IOVDD.

Copyright © 2012–2014, Texas Instruments Incorporated

PIN ASSIGNMENTS (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
ENABLE	B11	I	Chip enable – active high. Power down function can be controlled through SPI register assignment. Internal 50kΩ pull up resistor to IOVDD.
SCLK	A12	I	Serial interface clock. Internal 50kΩ pull-down resistor.
SDIO	A11	I/O	Bi-directional serial data in 3 pin mode (default). In 4-pin interface mode (register x00, D16), the SDIO pin in an input only. Internal 50kΩ pull-down.
SDENB	A13	I	Serial interface enable. Internal 50kΩ pull-down resistor.
SDO	A10	O	Uni-directional serial interface data in 4 pin mode (register x00, D16). The SDO pin is tri-stated in 3-pin interface mode (default). Internal 50kΩ pull-down resistor.
TESTMODE	B13	–	Factory internal test, do not connect
DATA INTERFACE			
DA[11:0]P/N	P3, N3, P2, N2, P1, N1, M4, M3, M2, M1, L4, L3, L2, L1, K4, K3, K2, K1, J4, J3, J2, J1, H4, H3	O	ADC A Data Bits 11 (MSB) to 0 (LSB) in DDR output mode. Standard LVDS output.
DB[11:0]P/N	E2, E1, D4, D3, D2, D1, C4, C3, C2, C1, B1, A1, B2, A2, B3, A3, B4, A4, B5, A5, B6, A6, B7, A7	O	ADC B Data Bits 11 (MSB) to 0 (LSB) in DDR output mode. Standard LVDS output.
DACLKP/N	H2, H1	O	DDR differential output data clock for Bus A. Register programmable to provide either rising or falling edge to center of stable data nominal timing.
DBCLKP/N	G2, G1	O	DDR differential output data clock for Bus B. Register programmable to provide either rising or falling edge to center of stable data nominal timing. Optionally Bus B can be latched with DACLKP/N.
SYNCOUTP/N	F2, F1, P5, N5	O	Synchronization output signal for synchronizing multiple ADCs. Can be disabled via SPI.
OVRAP/N	M5, L5	O	Bus A, Overrange indicator, LVDS output. A logic high signals an analog input in excess of the full-scale range. Optional SYNC output.
OVRBP/N	D5, C5	O	Bus B, Overrange indicator, LVDS output. A logic high signals an analog input in excess of the full-scale range. Optional SYNC output.
TRIGGERP/N	P10, N10	I	Trigger used for High resolution output data in feedback mode. Internal 100Ω termination
TRDYP/N	G4, G3, P7, N7	O	Trigger ready output indicator. Outputs for chA and chB are identical and one output can be shared for both channels.
HRESP/N	F4, F3, P6, N6	O	Indicator for high resolution output data– logic high signals 12bit output data. Outputs for chA and chB are identical and one output can be shared for both channels.
NC	E3, E4, N4, P4	–	Don’t connect to pin
POWER SUPPLY			
AVDD33	D12, E12, F12, G12, H12, J12, K12, L12, N12, P12	I	3.3V analog supply
AVDDC	G14, H14	I	1.8V supply for clock input
AVDD18	D10, D11, E11, F11, G11, H11, J11, K11, L10, L11, N11, P11	I	1.8V analog supply
DVDD	A8, A9, B8, B9, C8, D8, L8, M8, N8, P8	I	1.8V supply for digital block
DVDDLVDS	C6, C7, D6, D7, L6, L7, M6, M7	I	1.8V supply for LVDS outputs
IOVDD	B10	I	1.8V for digital I/Os
GND		I	Ground

Copyright © 2012–2014, Texas Instruments Incorporated

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD/ BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS54T04	196-BGA	ZAY	–40C to 85C	GREEN (RoHS & no Sb/Br)		ADS54T04I	ADS54T04IZAY	Tray
							ADS54T04IZAYR	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range, AVDD33		–0.5	4	V
Supply voltage range, AVDDC		–0.5	2.3	V
Supply voltage range, AVDD18		–0.5	2.3	V
Supply voltage range, DVDD		–0.5	2.3	V
Supply voltage range, DVDDLVDS		–0.5	2.3	V
Supply voltage range, IOVDD		–0.5	4	V
Voltage applied to input pins	INA/B_P, INA/B_N	–0.5	AVDD33 + 0.5	V
	CLKINP, CLKINN	–0.5	AVDDC + 0.5	V
	SYNCP, SYNCN	–0.5	AVDD33 + 0.5	V
	SRESET, SDENB, SCLK, SDIO, SDO, ENABLE	–0.5	IOVDD + 0.5	V
Operating free-air temperature range, T_A		–40	85	°C
Operating junction temperature range, T_J			150	°C
Storage temperature range		–65	150	°C
ESD, Human Body Model			2	kV

THERMAL INFORMATION

THERMAL METRIC(1)		ADS54T04	UNITS
		nFBGA (196-PIN)	
θ_{JA}	Junction-to-ambient thermal resistance(2)	37.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	6.8	
θ_{JB}	Junction-to-board thermal resistance(4)	16.8	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	16.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

Copyright © 2012–2014, Texas Instruments Incorporated

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Recommended operating junction temperature			105	°C
	Maximum rated operating junction temperature(1)	125			
T_A	Recommended free-air temperature	–40	25	85	°C

(1) Prolonged use at this junction temperature may increase the device failure-in-time (FIT) rate.

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ADC Clock Frequency			40		500	MSPS
Resolution			12			Bits
SUPPLY						
AVDD33			3.15	3.3	3.45	V
AVDDC, AVDD18, DVDD, DVDDLVDS			1.7	1.8	1.9	V
IOVDD			1.7	1.8	3.45	V
POWER SUPPLY						
I_{AVDD33}	3.3V Analog supply current			297	330	mA
I_{AVDD18}	1.8V Analog supply current			84	100	mA
I_{AVDDC}	1.8V Clock supply current			26	45	mA
I_{DVDD}	1.8V Digital supply current	Auto Correction Enabled		230	260	mA
I_{DVDD}	1.8V Digital supply current	Auto Correction Disabled		106		mA
I_{DVDD}	1.8V Digital supply current	Auto Correction Disabled, decimation filter enabled		135		mA
$I_{DVDDLVDS}$	1.8V LVDS supply current			120	150	mA
I_{IOVDD}	1.8V I/O Voltage supply current			1	2	mA
P_{dis}	Total power dissipation	Auto Correction Enabled, decimation filter disabled		1.78	2.3	W
P_{dis}	Total power dissipation	Auto Correction Disabled, decimation filter disabled		1.6		W
PSRR		250kHz to 500MHz	40			dB
Shut-down power dissipation				7		mW
Shut-down wake up time				2.5		ms
Standby power dissipation				7		mW
Standby wake up time				100		µs
Deep-sleep mode power dissipation		Auto correction disabled		282		mW
		Auto correction enabled		370		mW
Deep-sleep mode wakeup time				20		µs
Light-sleep mode power dissipation		Auto correction disabled		549		mW
		Auto correction enabled		650		mW
Light-sleep mode wakeup time				2		µs

Copyright © 2012–2014, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD3V = 3.3V, AVDD/DRVDD/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS					
Differential input full-scale			1.0	1.25	Vpp
Input common mode voltage			1.9	±0.1	V
Input resistance	Differential at DC		1		kΩ
Input capacitance	Each input to GND		2		pF
VCM common mode voltage output			1.9		V
Analog input bandwidth (3dB)			1200		MHz
DYNAMIC ACCURACY					
Offset Error	Auto Correction Disabled	–20	–7.5	20	mV
	Auto Correction Enabled	–1	0	1	mV
Offset temperature coefficient			–611		µV/°C
Gain error		–5		5	%FS
Gain temperature coefficient			0.005		%FS/°C
Differential nonlinearity	f_{IN} = 230 MHz	–1	±0.9	2	LSB
Integral nonlinearity	f_{IN} = 230 MHz	–5	±1.5	5	LSB
CLOCK INPUT					
Input clock frequency		40		500	MHz
Input clock amplitude			2		Vpp
Input clock duty cycle		40%	50%	60%	
Internal clock biasing			0.9		V

Copyright © 2012–2014, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Auto Correction				Enabled			Disabled		Vpp
DYNAMIC AC CHARACTERISTICS(1) – Burst Mode Enabled: 12bit High Resolution Output Data									
SNR	Signal to Noise Ratio	f_{IN} = 10 MHz		60.8			60.8		dBFS
		f_{IN} = 100 MHz		60.7			60.8		
		f_{IN} = 230 MHz	59	60.6			60.7		
		f_{IN} = 450 MHz		60.2			60.6		
		f_{IN} = 700 MHz		59.4			60.1		
HD2,3	Second and third harmonic distortion	f_{IN} = 10 MHz		84			86		dBc
		f_{IN} = 100 MHz		84			82		
		f_{IN} = 230 MHz	70	80			83		
		f_{IN} = 450 MHz		82			84		
		f_{IN} = 700 MHz		76			74		
Non HD2,3	Spur Free Dynamic Range (excluding second and third harmonic distortion)	f_{IN} = 10 MHz		77			78		dBc
		f_{IN} = 100 MHz		77			78		
		f_{IN} = 230 MHz	70	77			77		
		f_{IN} = 450 MHz		74			75		
		f_{IN} = 700 MHz		70			71		
IL	Fs/2-Fin interleaving spur	f_{IN} = 10 MHz		92			80		dBc
		f_{IN} = 100 MHz		83			79		
		f_{IN} = 230 MHz	70	83			79		
		f_{IN} = 450 MHz		79			76		
		f_{IN} = 700 MHz		75			73		
SINAD	Signal to noise and distortion ratio	f_{IN} = 10 MHz		60.6			60.7		dBc
		f_{IN} = 100 MHz		60.6			60.7		
		f_{IN} = 230 MHz	57.5	60.5			60.7		
		f_{IN} = 450 MHz		60.1			60.5		
		f_{IN} = 700 MHz		59.3			60		
THD	Total Harmonic Distortion	f_{IN} = 10 MHz		76.3			79.0		dBc
		f_{IN} = 100 MHz		76.5			77.6		
		f_{IN} = 230 MHz	68	77.4			78.1		
		f_{IN} = 450 MHz		76.3			77.9		
		f_{IN} = 700 MHz		73.4			72.9		
IMD3	Inter modulation distortion	F_{in} = 129.5 and 130.5MHz, -7dBFS		82			82		dBFS
		F_{in} = 349.5 and 350.5MHz, -7dBFS		80			80		
	Crosstalk			90			90		dB
ENOB	Effective number of bits	f_{IN} = 230 MHz		9.8			9.8		LSB

(1) SFDR and SNR calculations do not include the DC or Fs/2 bins when Auto Correction is disabled.

Copyright © 2012–2014, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, –1dBFS differential input (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVER-DRIVE RECOVERY ERROR						
	Input overload recovery	Recovery to within 5% (of final value) for 6dB overload with sine wave input		2		ns
SAMPLE TIMING CHARACTERISTICS						
rms	Aperture Jitter	Sample uncertainty		100		fs rms
	Data Latency	ADC sample to digital output, auto correction disabled		38		Clock Cycles
		ADC sample to digital output, auto correction enabled		50		
		ADC sample to digital output, Decimation filter enabled, Auto correction disabled		74		Sampling clock Cycles
	Over-range Latency	ADC sample to over-range output		12		Clock Cycles

ELECTRICAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS – SRESET, SCLK, SDENB, SDIO, ENABLE						
	High-level input voltage	All digital inputs support 1.8V and 3.3V logic levels.	0.7 x IOVDD			V
	Low-level input voltage				0.3 x IOVDD	V
	High-level input current		–50		200	µA
	Low-level input current		–50		50	µA
	Input capacitance			5		pF
DIGITAL OUTPUTS – SDO						
	High-level output voltage	Iload = -100uA	IOVDD – 0.2			V
		Iload = -2mA	0.8 x IOVDD			
	Low-level output voltage	Iload = 100uA			0.2	V
		Iload = 2mA			0.22 x IOVDD	
DIGITAL INPUTS – SYNCP/N, TRIGGERP/N						
V_{ID}	Differential input voltage		250	350	450	mV
V_{CM}	Input common mode voltage		1.125	1.2	1.375	V
t_{SU}			500			ps
DIGITAL OUTPUTS – DA[11:0]P/N, DACLKP/N, OVRAP/N, SYNCOUTP/N, TRDYP/N, HRESP/N, DB[11:0]P/N, DBCLKP/N, OVRBP/N,						
V_{OD}	Output differential voltage	Iout = 3.5mA	250	350	450	mV
V_{OCM}	Output common mode voltage	Iout = 3.5mA	1.125	1.25	1.375	V
t_{suA}		F_S = 500Msps, Data valid to zero-crossing of DACLK	600	800		ps
t_{hA}		F_S = 500Msps, Zero-crossing of DACLK to data becoming invalid	600	790		ps
t_{suB}		F_S = 500Msps, Data valid to zero-crossing of DBCLK	700	900		ps
t_{hB}		F_S = 500Msps, Zero-crossing of DBCLK to data becoming invalid	500	600		ps

Copyright © 2012–2014, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{PD}	F_S = 500Msps, CLKIN falling edge to DACLK, DBCLK rising edge	3.28	3.48	3.74	ns
t_{RISE}	10% - 90%	100	150	200	ps
t_{FALL}	90% - 10%	100	150	200	ps

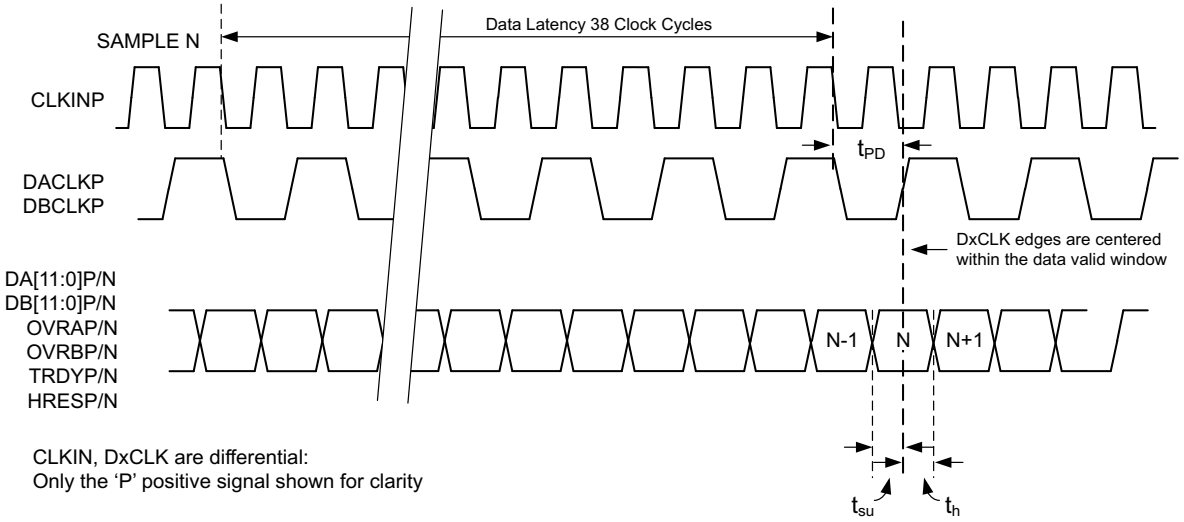


Figure 3. Timing Diagram for 12-bit DDR Output

Copyright © 2012–2014, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

FFT FOR 10 MHz INPUT SIGNAL (auto on)

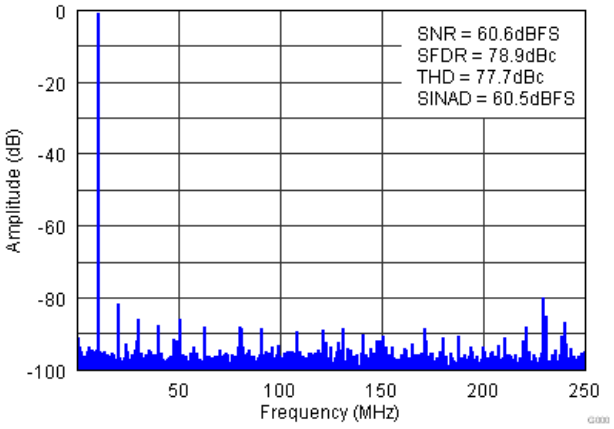


Figure 4.

FFT FOR 10 MHz INPUT SIGNAL (auto off)

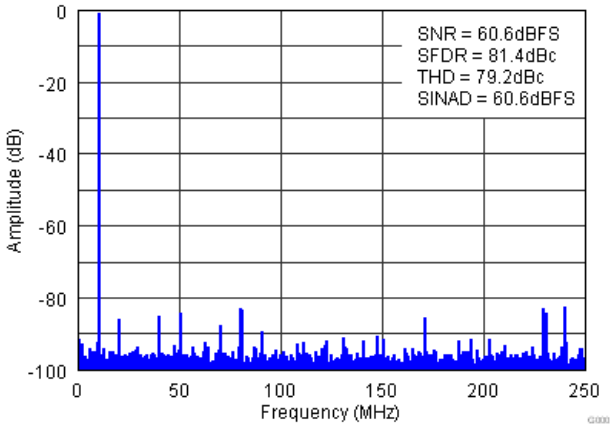


Figure 5.

FFT FOR 230 MHz INPUT SIGNAL (auto on)

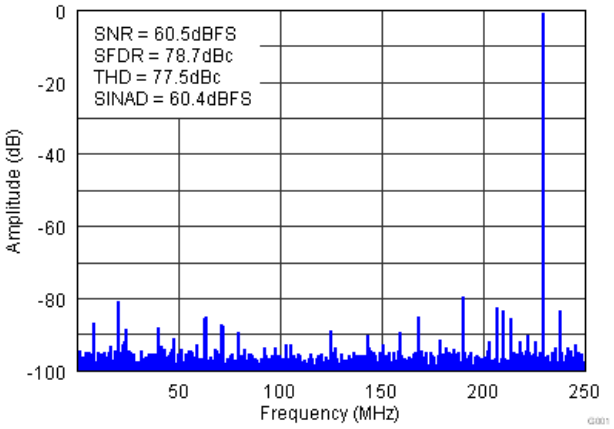


Figure 6.

FFT FOR 230 MHz INPUT SIGNAL (auto off)

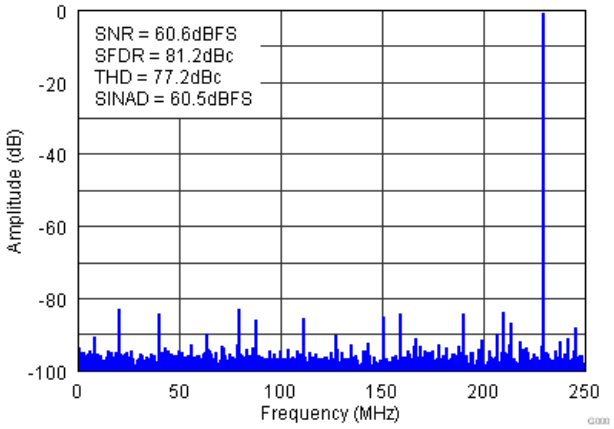


Figure 7.

FFT FOR 450 MHz INPUT SIGNAL (auto on)

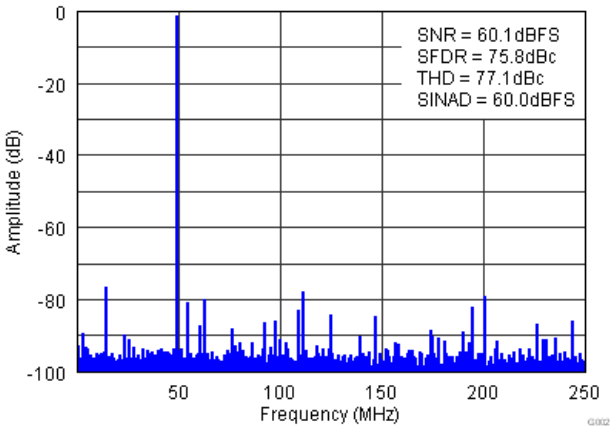


Figure 8.

FFT FOR 450 MHz INPUT SIGNAL (auto off)

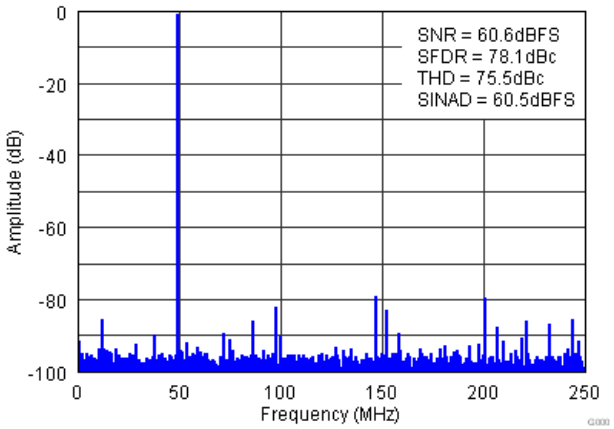


Figure 9.

Copyright © 2012–2014, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

FFT FOR 700 MHz INPUT SIGNAL (auto on)

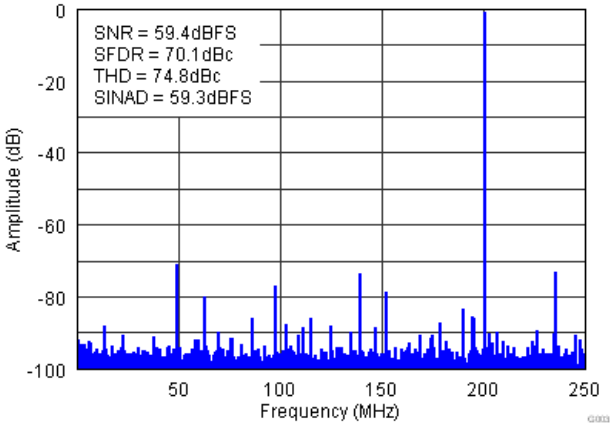


Figure 10.

FFT FOR 700 MHz INPUT SIGNAL (auto off)

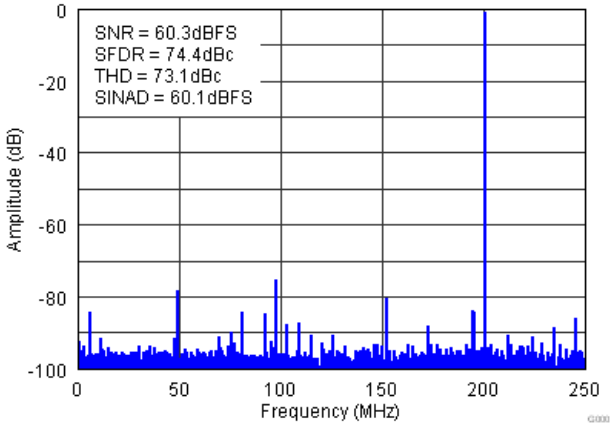


Figure 11.

SFDR vs INPUT FREQUENCY

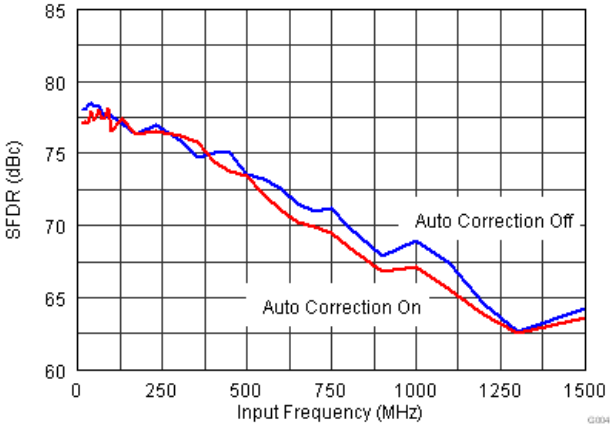


Figure 12.

SNR vs INPUT FREQUENCY

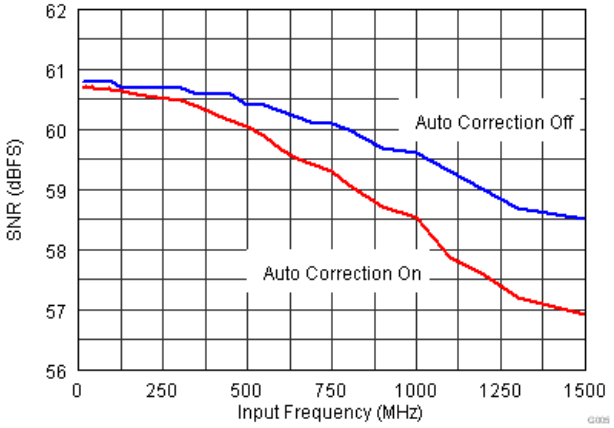


Figure 13.

SFDR vs AMPLITUDE (fin = 230MHz)

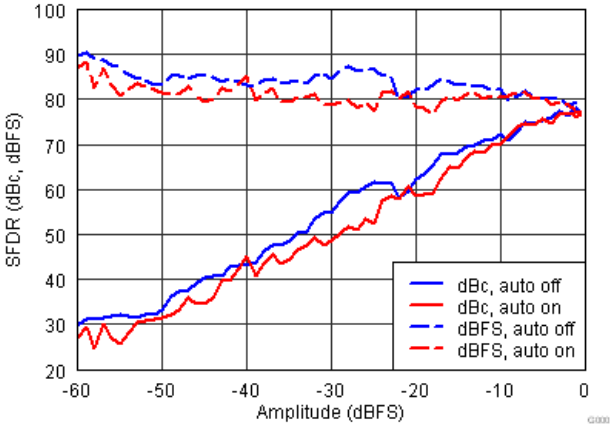


Figure 14.

SNR vs Amplitude (fin = 230 MHz)

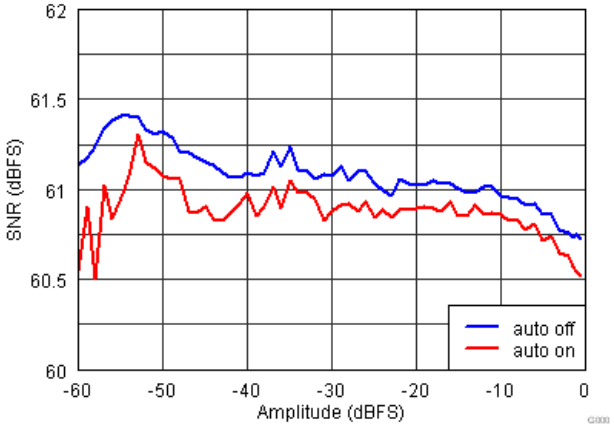


Figure 15.

Copyright © 2012–2014, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

Tow Tone Performance Across Input Amplitude (fin = 130MHz)

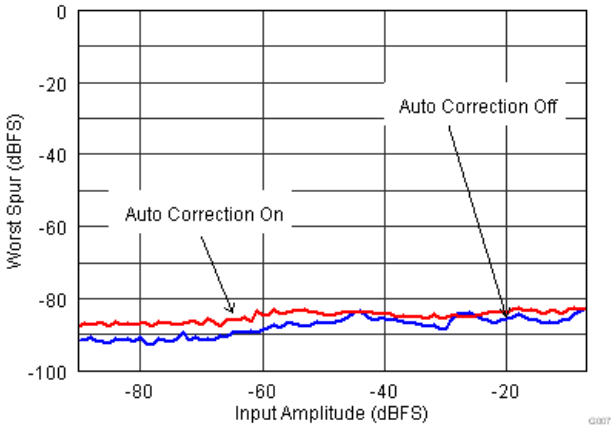


Figure 16.

SFDR vs Vref (auto on)

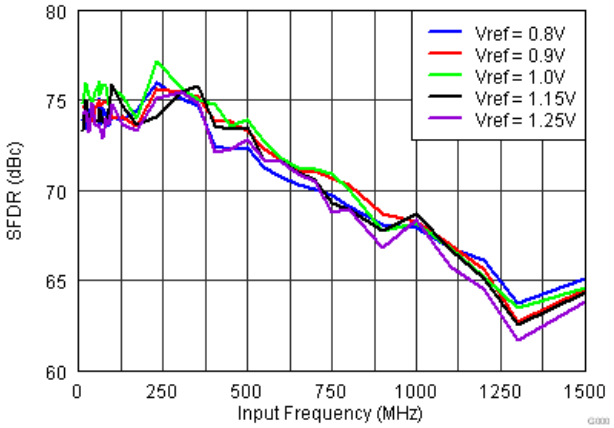


Figure 17.

SFDR vs Vref (auto off)

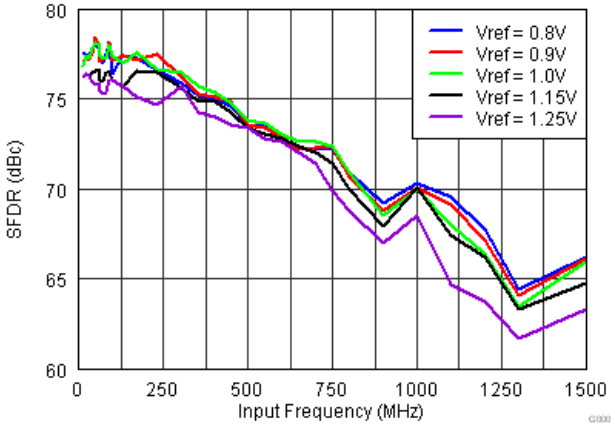


Figure 18.

SNR vs Vref (auto on)

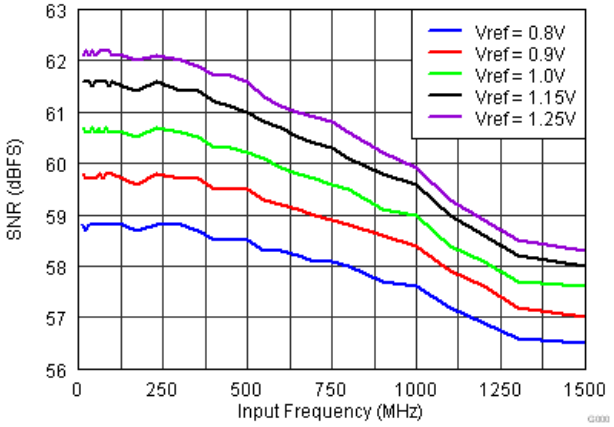


Figure 19.

Copyright © 2012–2014, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

SNR vs Vref (auto off)

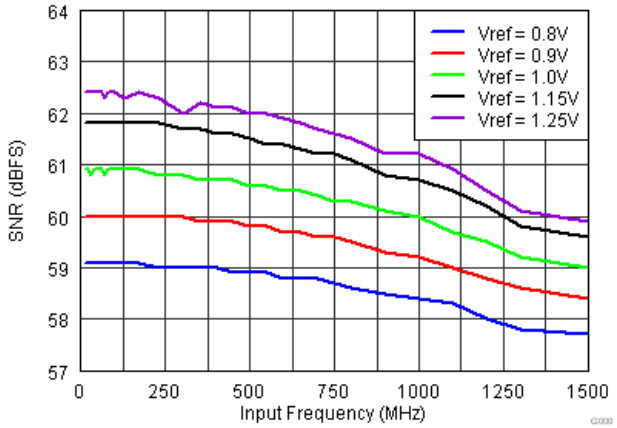


Figure 20.

Performance Across Input Common Mode Voltage

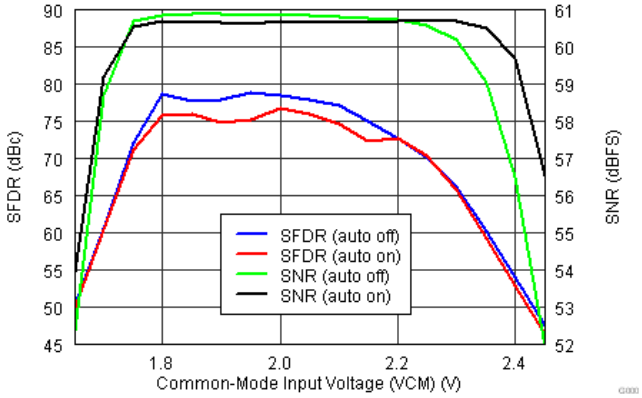


Figure 21.

Performance Across Temperature (fin = 230MHz)

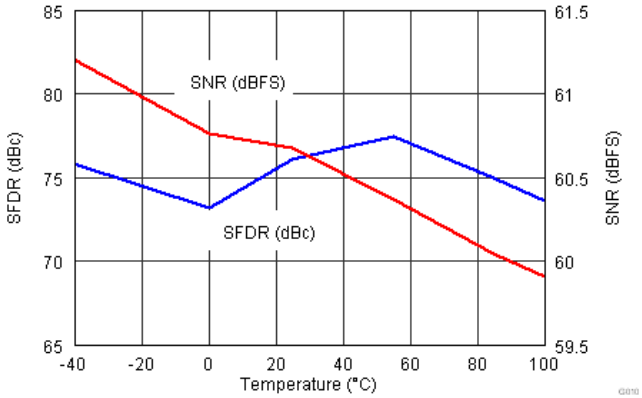


Figure 22.

Performance Across AVDD33 (fin = 230MHz)

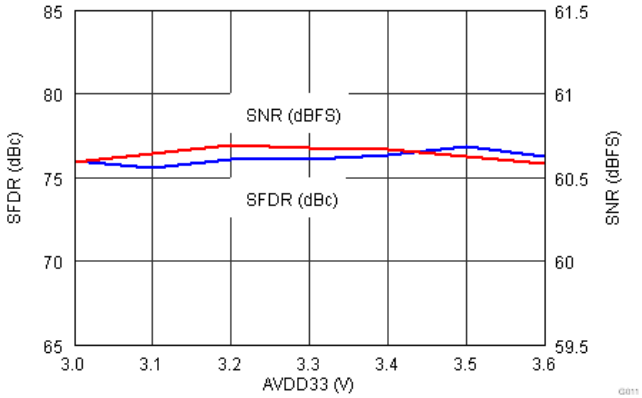


Figure 23.

Performance Across AVDD18 (fin = 230MHz)

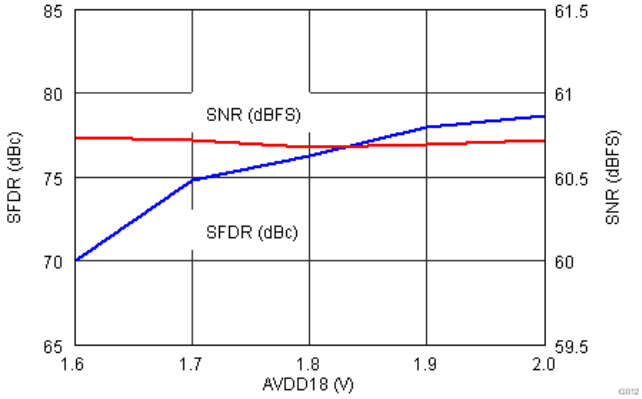


Figure 24.

Performance Across Clock Amplitude

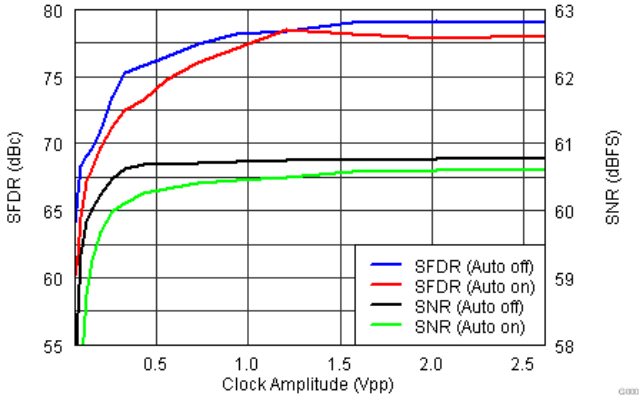


Figure 25.

Copyright © 2012–2014, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

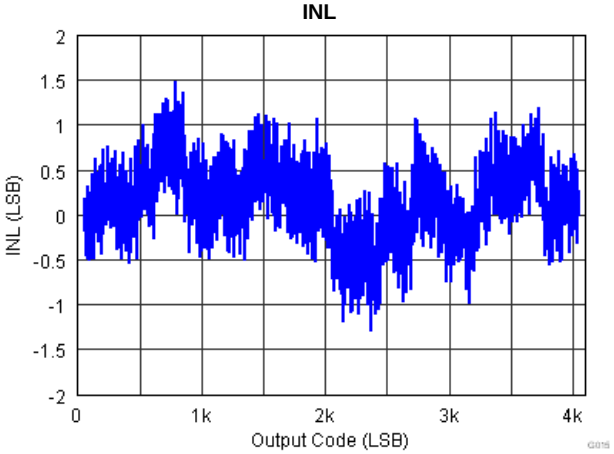


Figure 26.

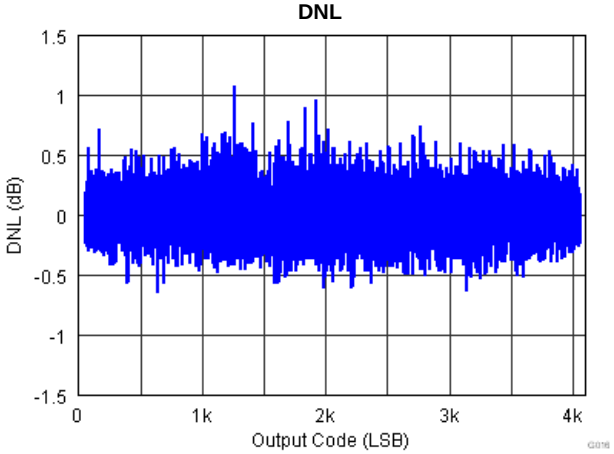


Figure 27.

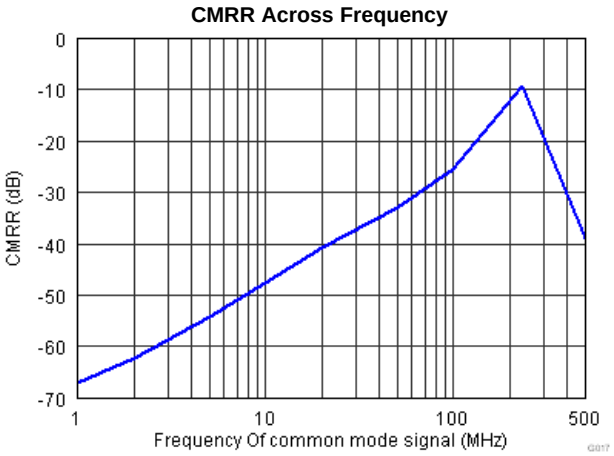


Figure 28.

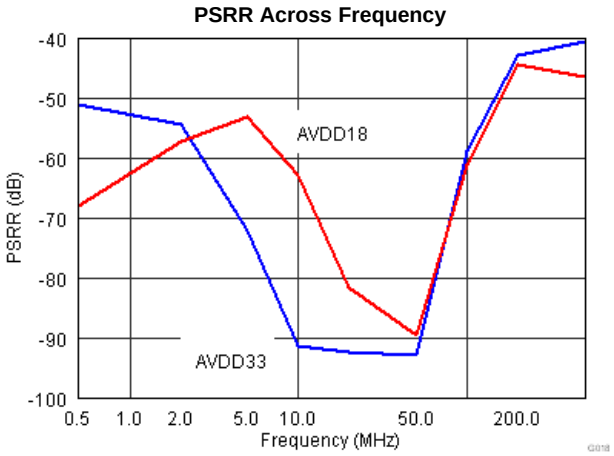


Figure 29.

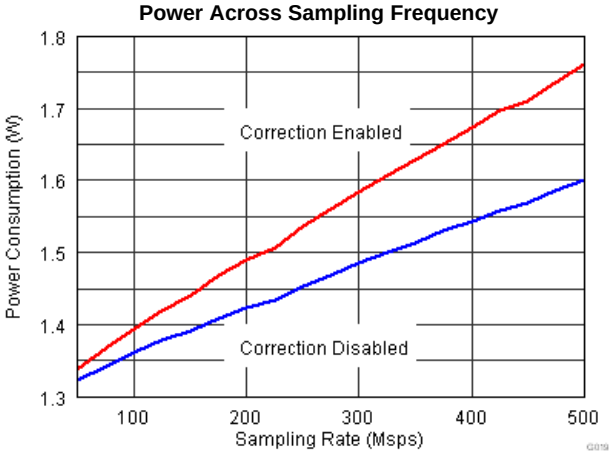


Figure 30.

Copyright © 2012–2014, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

SFDR Across Input and Sampling Frequencies (auto on)

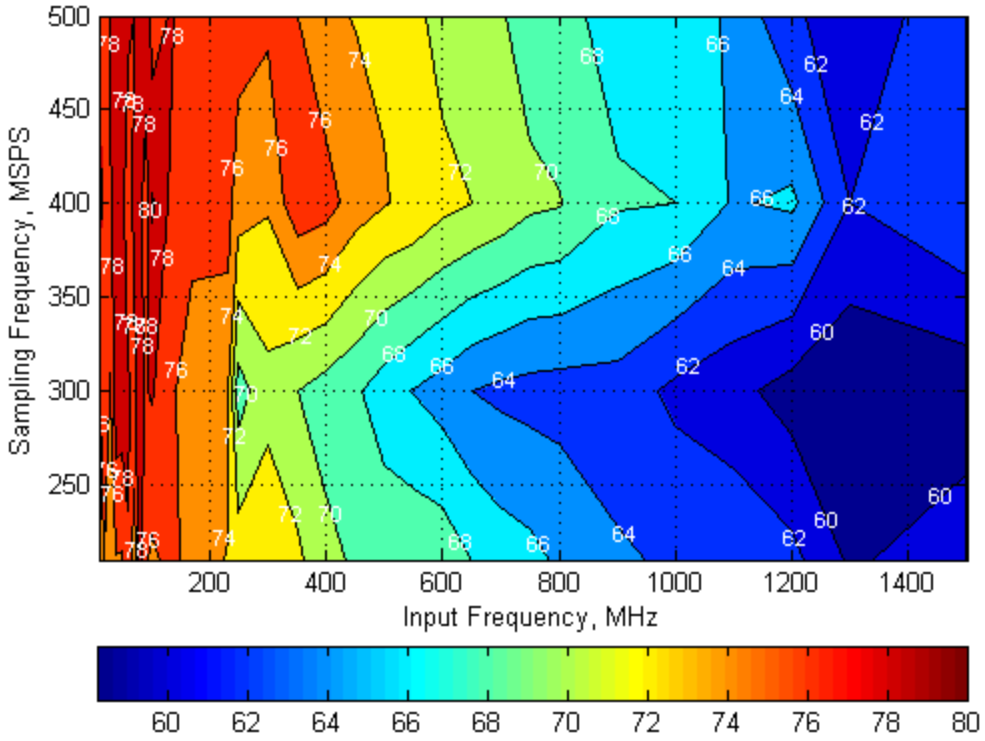


Figure 31.

Copyright © 2012–2014, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

SFDR Across Input and Sampling Frequencies (auto off)

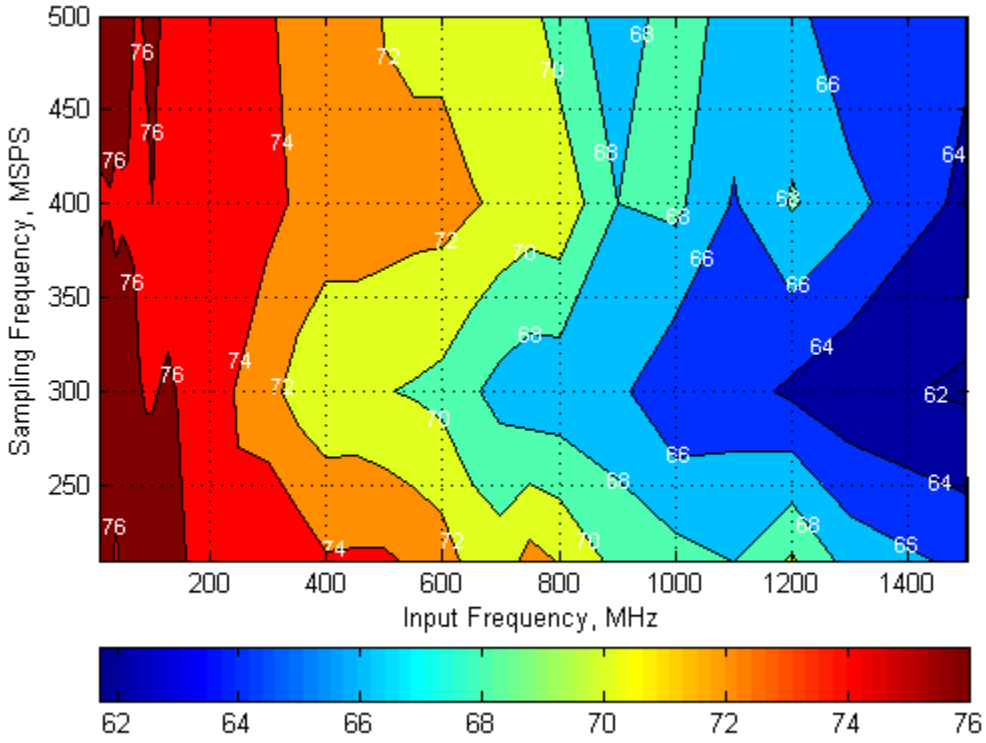


Figure 32.

Copyright © 2012–2014, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

SNR Across Input and Sampling Frequencies (auto on)

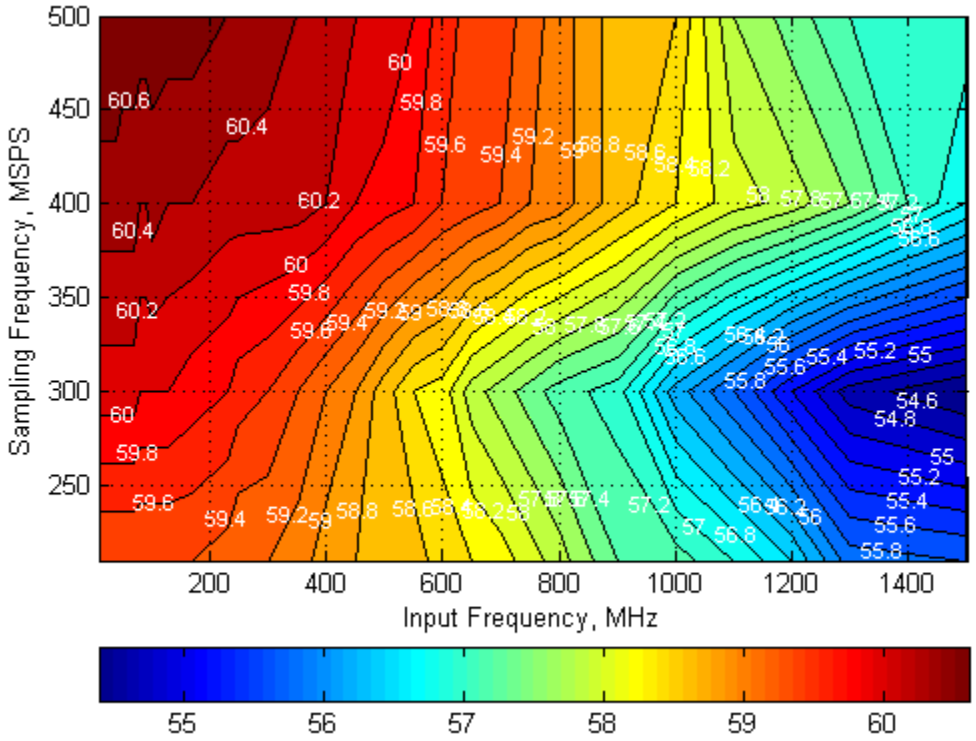


Figure 33.

Copyright © 2012–2014, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

Typical values at TA = +25°C, full temperature range is T_{MIN} = -40°C to T_{MAX} = +85°C, ADC sampling rate = 500Msps, 50% clock duty cycle, AVDD33 = 3.3V, AVDDC/AVDD18/DVDD/DVDDLVDS/IOVDD = 1.8V, -1dBFS differential input, unless otherwise noted.

SNR Across Input and Sampling Frequencies (auto on)

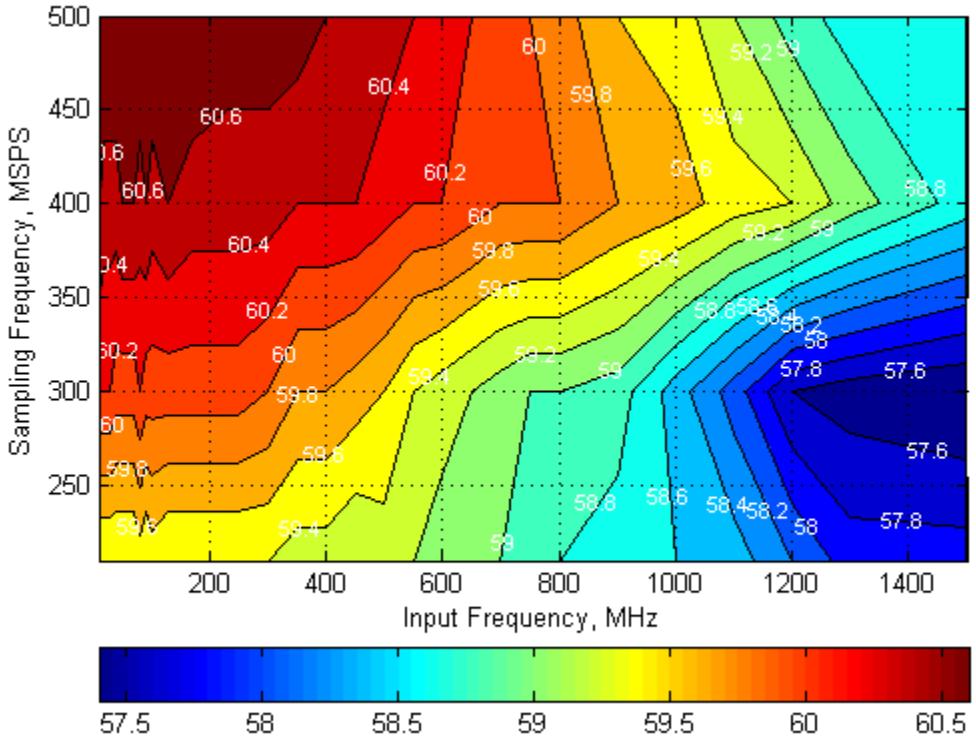


Figure 34.

FEATURES

POWER DOWN MODES

The ADS54T04 can be configured via SPI write (address x37) to a stand-by, light or deep sleep power mode which is controlled by the ENABLE pin. The sleep modes are active when the ENABLE pin goes low. Different internal functions stay powered up which results in different power consumption and wake up time between the two sleep modes.

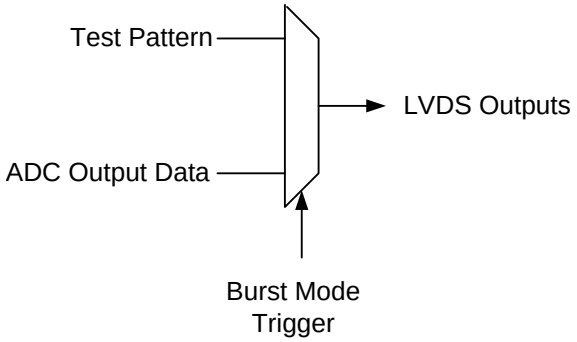
Sleep mode	Wake up time	Power Consumption Auto correction disabled	Power Consumption Auto correction enabled
Complete Shut Down	2.5 ms	7mW	7mW
Stand-by	100µs	7mW	7mW
Deep Sleep	20µs	282mW	370mW
Light Sleep	2µs	549mW	650mW

TEST PATTERN OUTPUT

The ADS54T04 can be configured to output different test patterns that can be used to verify the digital interface is connected and working properly. To enable the test pattern mode, the high performance mode 1 has to be disabled first via SPI register write. Then different test patterns can be selected by configuring registers x3C, x3D and x3E. All three registers must be configured for the test pattern to work properly.

First set HP1 = 0 (Addr 0x01, D01)

Internally the test pattern replaces the sampled data from the ADC. However at the LVDS outputs the output data is still subject to burst mode operation. In low resolution output the LSBs of the test pattern are replaced with 0s.



Register Address	All 0s	All 1s	Toggle (0xAAA => 0x555)	Toggle (0xFFF => 0x000)
0x3C	0x8000	0xBFFC	0x9554	0xBFFC
0x3D	0x0000	0x3FFC	0x2AA8	0x0000
0x3E	0x0000	0x3FFC	0x1554	0x3FFC

Register Address	Custom Pattern															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x3C	1	0													0	0
x3D	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0
x3E	0	0													0	0

For normal operation, set HP1 = 1 (Addr 0x01, D01) and 0x3C, 0x3D, 0x3E all to 0.

Copyright © 2012–2014, Texas Instruments Incorporated

CLOCK INPUT

The ADS54T04 clock input can be driven differentially with a sine wave, LVPECL or LVDS source with little or no difference in performance. The common mode voltage of the clock input is set to 0.9V using internal 2kΩ resistors. This allows for AC coupling of the clock inputs. The termination resistors should be placed as close as possible to the clock inputs in order to minimize signal reflections and jitter degradation.

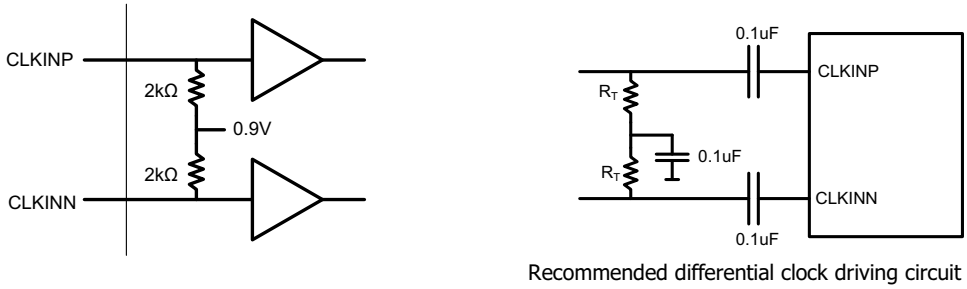


Figure 35. Recommended Differential Clock Driving Circuit

SNR AND CLOCK JITTER

The signal to noise ratio of the ADC is limited by three different factors: the quantization noise is typically not noticeable in pipeline converters and is 72dB for a 12bit ADC. The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \times \log\sqrt{\left(10^{-\frac{SNR_{Quantization_Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{ThermalNoise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation due to sample clock jitter can be calculated as following:

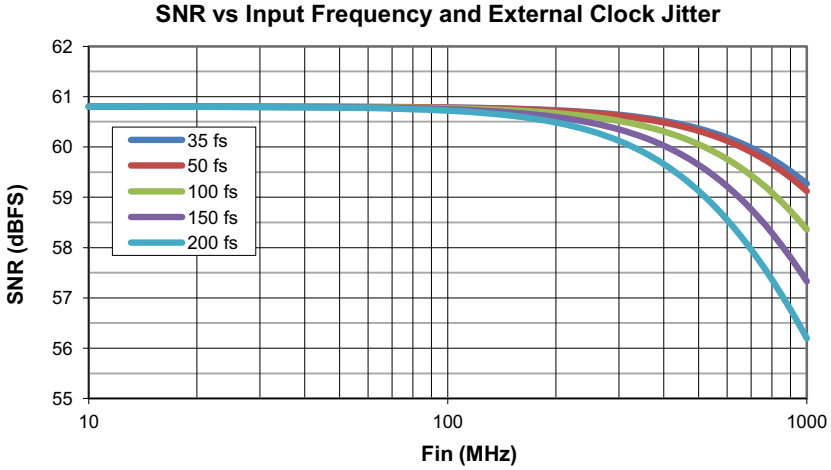
$$SNR_{Jitter}\,[dBc] = -20 \times \log(2\pi \times f_{IN} \times t_{Jitter}) \quad (2)$$

The total clock jitter (TJitter) has three components – the internal aperture jitter (100fs for ADS54T04) which is set by the noise of the clock input buffer, the external clock jitter and the jitter from the analog input signal. It can be calculated as following:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock_Input})^2 + (T_{Aperture_ADC})^2} \quad (3)$$

External clock jitter can be minimized by using high quality clock sources and jitter cleaners as well as bandpass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter.

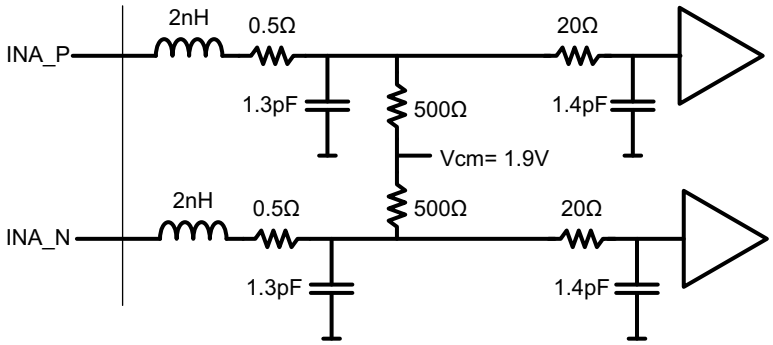
The ADS54T04 has a thermal noise of 60.8 dBFS and internal aperture jitter of 100fs. The SNR depending on amount of external jitter for different input frequencies is shown in the following figure.



ANALOG INPUTS

The ADS54T04 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source which enables great flexibility in the external analog filter design as well as excellent 50Ω matching for RF applications. The buffer also helps to isolate the external driving circuit from the internal switching currents of the sampling circuit which results in a more constant SFDR performance across input frequencies.

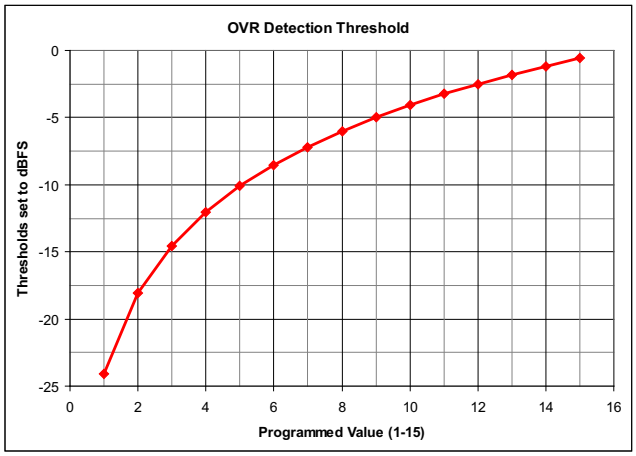
The common-mode voltage of the signal inputs is internally biased to 1.9V using 500Ω resistors which allows for AC coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.25V) and (VCM – 0.25V), resulting in a 1.0Vpp (default) differential input swing. The input sampling circuit has a 3dB bandwidth that extends up to 1.2GHz.



OVER-RANGE INDICATION

The ADS54T04 provides a fast over-range indication on the OVRA/B pins. The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and it gets presented after just 12 clock cycles enabling a quicker reaction to an overrange event. The OVR threshold can be configured using SPI register writes.

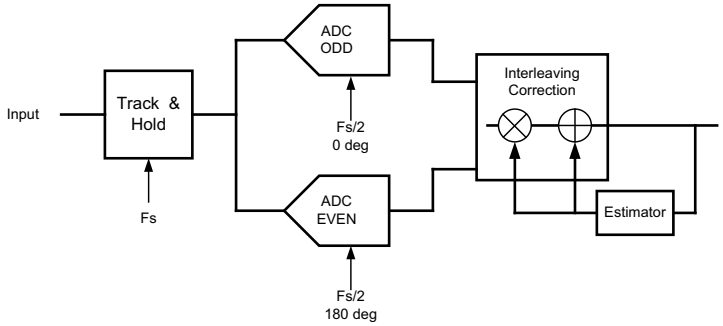
The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the Over-range threshold bits. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESH bits] /16). After reset, the default value of the over-range threshold is set to 15 (decimal) which corresponds to a threshold of 0.56dB below full scale (20*log(15/16)).



Copyright © 2012–2014, Texas Instruments Incorporated

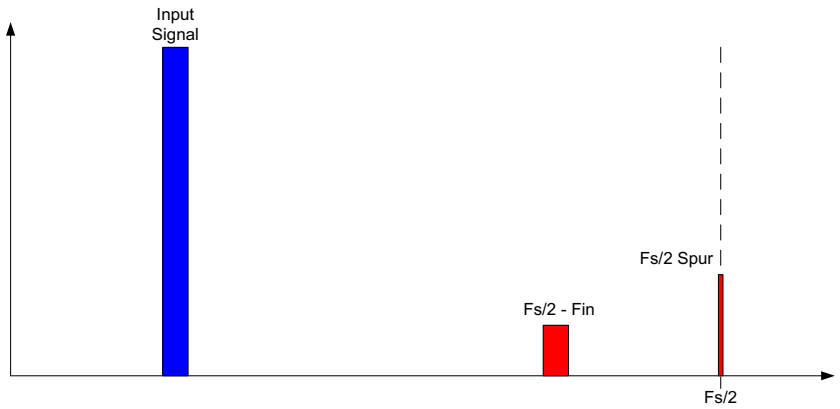
INTERLEAVING CORRECTION

Each of the two data converter channels consists of two interleaved ADCs each operating at half of the ADC sampling rate but 180º out of phase from each other. The front end track and hold circuitry is operating at the full ADC sampling rate which minimizes the timing mismatch between the two interleaved ADCs. In addition the ADS54T04 is equipped with internal interleaving correction logic that can be enabled via SPI register write.



The interleaving operation creates 2 distinct and interleaving products:

- Fs/2 – Fin: this spur is created by gain timing mismatch between the ADCs. Since internally the front end track and hold is operated at the full sampling rate, this component is greatly improved and mostly dependent on gain mismatch.
- Fs/2 Spur: due to offset mismatch between ADCs



The auto correction loop can be enabled via SPI register write in address 0x01. By default it is disabled for lowest possible power consumption. The DC correction function can be enabled in 0x03 & 0x1A for chA and chB respectively. The default settings for the auto correction function should work for most applications. However please contact Texas Instruments if further fine tuning of the algorithm is required.

The auto correction function yields best performance for input frequencies below 250MHz.

Copyright © 2012–2014, Texas Instruments Incorporated

RECEIVE MODE: DECIMATION FILTER

Each channel has a digital filter in the data path as shown in Figure 36. The filter can be programmed as a low-pass or a high-pass filter and the normalized frequency response of both filters is shown in Figure 37.

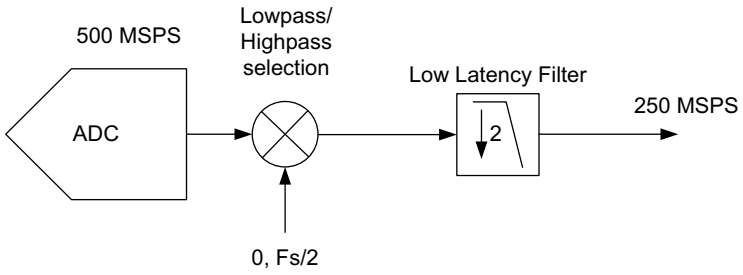


Figure 36.

The decimation filter response has a 0.1dB pass band ripple with approximately 41% pass-band bandwidth. The stop-band attenuation is approximately 40dB.

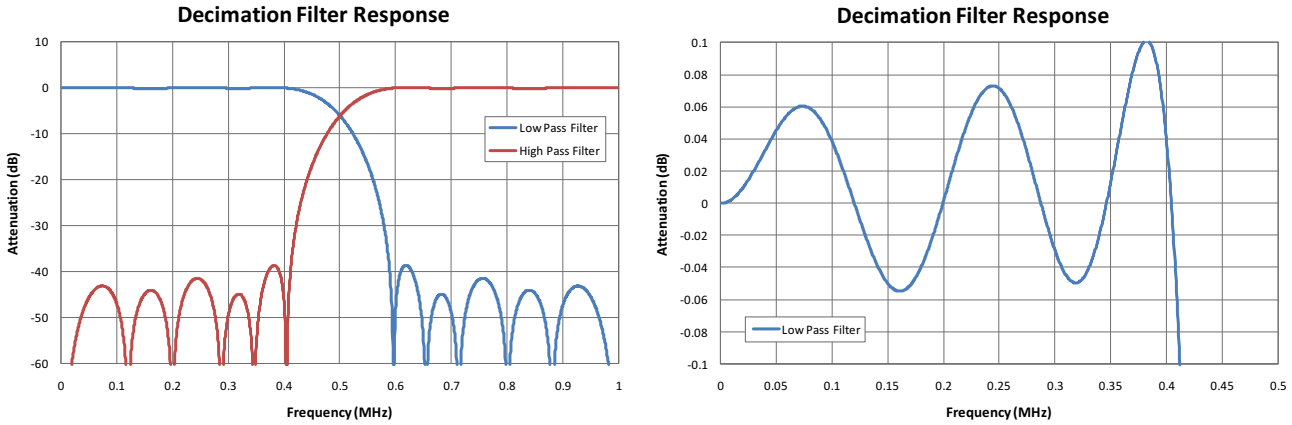


Figure 37.

Copyright © 2012–2014, Texas Instruments Incorporated

FEEDBACK MODE: BURST MODE

In burst mode the output data is alternated between a high resolution 12bit output of 2N samples and a low resolution 9 or 11bit output of 2^{N+3} samples. Burst mode is enabled through SPI register write and there are two basic operating modes available – a manual trigger mode where the high resolution output is initiated through external trigger and an auto trigger mode where the internal logic transitions to high resolution output immediately after transmitting the last low resolution sample. Upon enabling burst mode through a SPI register write, the ADS54T04 transmits 2^{13} low resolution samples and the trigger command is locked out until completion.

The parameter N can be changed via SPI at any time. It will go in effect with the next output cycle starting with transmission of low resolution samples. The default value for N after reset is N=10.

N limit	10 (minimum)	25 (maximum)
Number of low resolution samples per cycle (2^{N+3})	8,192	268,435,456
Number of high resolution samples per cycle (2^{N})	1,024	33,554,432
Total amount of samples per cycle	9,216	301,989,888
Maximum number of high resolution (12-bit) samples per 1 second	55.6M	55.6M

Manual Trigger Mode

The control of the high resolution output is shown below along with the two output flags (TRDY and HRES).

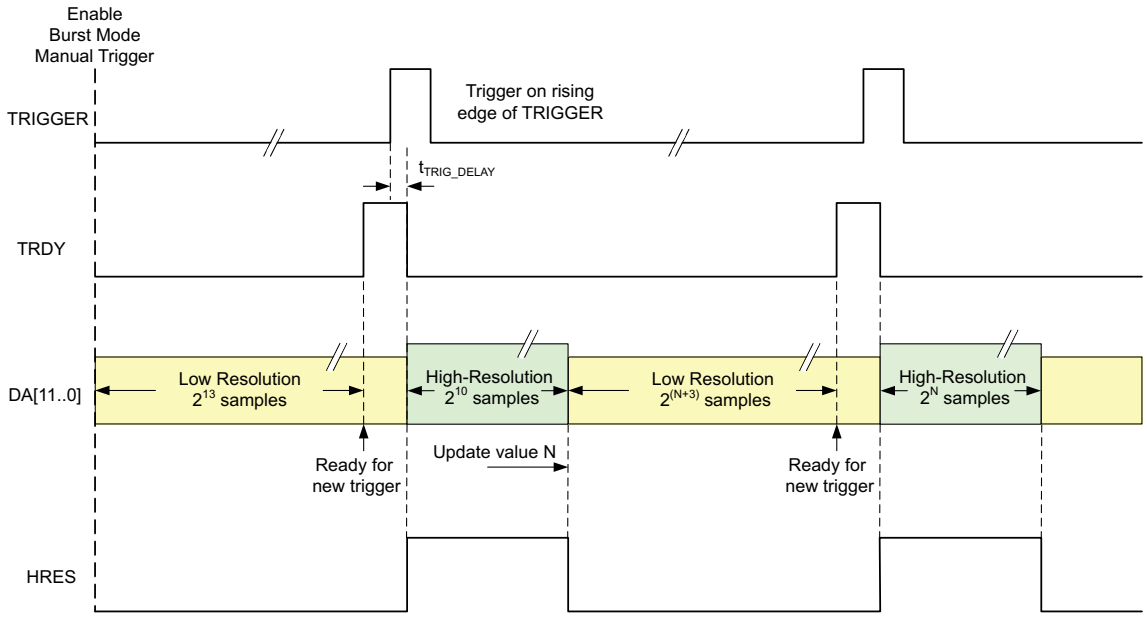


Figure 38. Triggering High Resolution Mode and Lockout Time

After enabling burst mode, the output data DA[11..0] and DB[11..0] are forced to low resolution mode for 2^{13} samples. During that period any trigger signal is ignored. The completion of the low resolution sample cycle is signaled by a logic high on the TRDY output pins indicating that a high resolution (12-bit) data output burst can be triggered by a low to high transition on the TRIGGER input. The ADC monitors the TRIGGER input at each rising edge of the input clock.

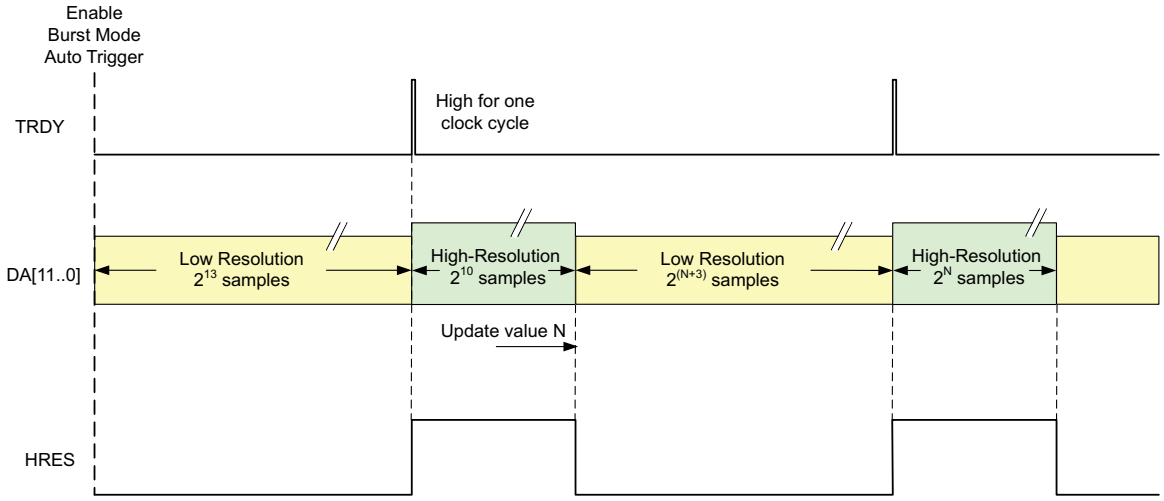
The high resolution output data starts with a delay of t_{TRIG_DELAY} = 1-2 DA/BCLK clock cycles and is indicated through the HRES data flag which stays high for all 2^{N} high resolution samples. At completion the register value for N is verified and transmission of $2^{(N+3)}$ low resolution data immediately follows. Once the last low resolution sample is output on the output data bus, the flag TRDY is asserted high again indicating the end of the lockout period and the next 2^{N} high resolution samples can be triggered again.

Copyright © 2012–2014, Texas Instruments Incorporated

Auto Trigger Mode

This mode is enabled by setting the auto trigger bit via SPI register write and the DA/DB data outputs start in low resolution for 2^{13} samples. Immediately following completion of transmission of the last low resolution sample, the outputs automatically start transmitting 2^{10} high resolution samples without the need for external trigger ensuring maximum efficiency. Any input signal on the TRIGGER pins is ignored and the TRDY flag will go high only for one clock cycle with the start of the high resolution data.

The output flag HRES is aligned with the 2^N high resolution output samples and the parameter N can be changed until the next output cycle starts again with low resolution output data.



High Resolution Output Data

After trigger, the data outputs DA[11..0]/DB[11..0] are 12-bit resolution for 2^N samples, where N is a programmable register with a range 10 ≤N≤25 (corresponding to 1024 to 33554432 samples).

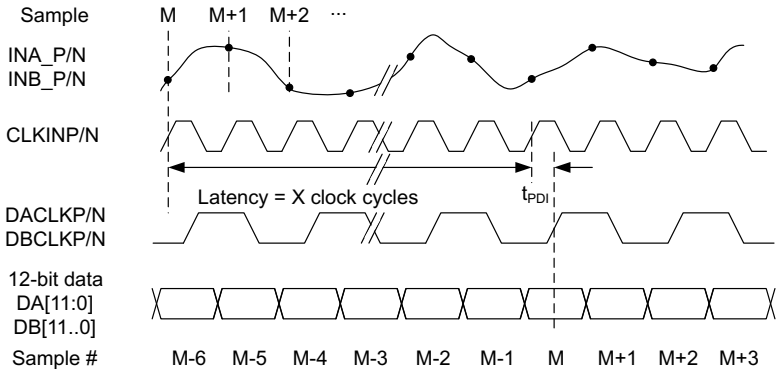


Figure 39. High Resolution Data Output Timing

After the high resolution data, the data output returns to low resolution mode, the logic level of the HRES flag returns low and the trigger is locked out for $2^{(N+3)}$ samples. N is the sample integer resulting in a maximum output duty cycle of 1/9. During the trigger lockout time, a low to high transition on TRIGGERP/N will be ignored. After the 2^{N+3} low resolution samples, the TRIGGERP/N is re-enabled for the next valid data burst.

Low Resolution Output Data

There are two different options for the low resolution output data and the selection is made through SPI register control. The data can either be output at full speed (ADC sampling rate) with the output resolution limited to 9bit (9 MSBs). Alternatively the output resolution can be selected to 11bit (11 MSBs) but at a reduced effective data rate where every 4th sample gets repeated four times.

Copyright © 2012–2014, Texas Instruments Incorporated

Full Speed – 9bit

The output data rate and timing is exactly the same as the high resolution data – only the output resolution is limited to the 9 MSBs.

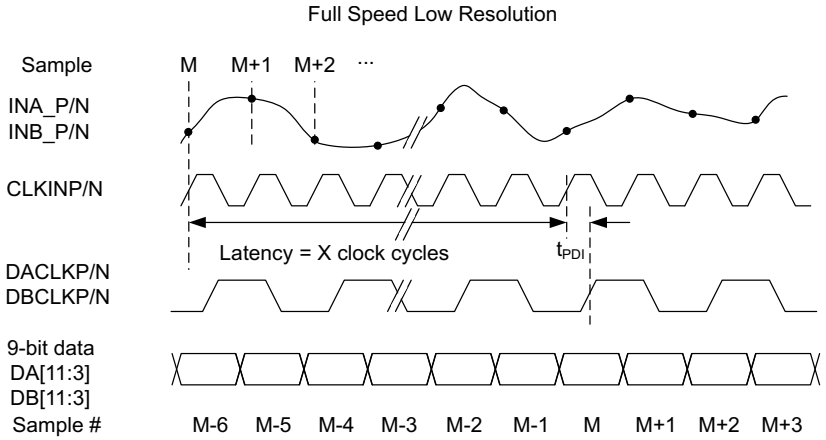


Figure 40. Full Rate Low Resolution Output Data Timing

Decimated Low Resolution Output Data

In decimated low resolution mode the output data is limited to 11-bits and every sample is repeated four times so the effective data rate is 1/4 of ADC sampling rate. The latency of the ADC sample to output sample is exactly the same as for high resolution data – there is no uncertainty in which conversion sample results in the valid output data. This is because the output continues to run at the ADC sample rate – only the resolution is changed and three out of four samples are deleted.

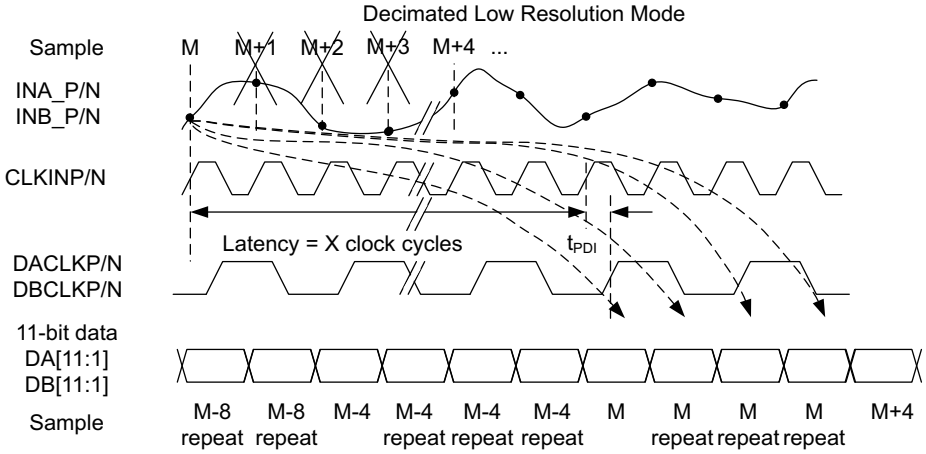
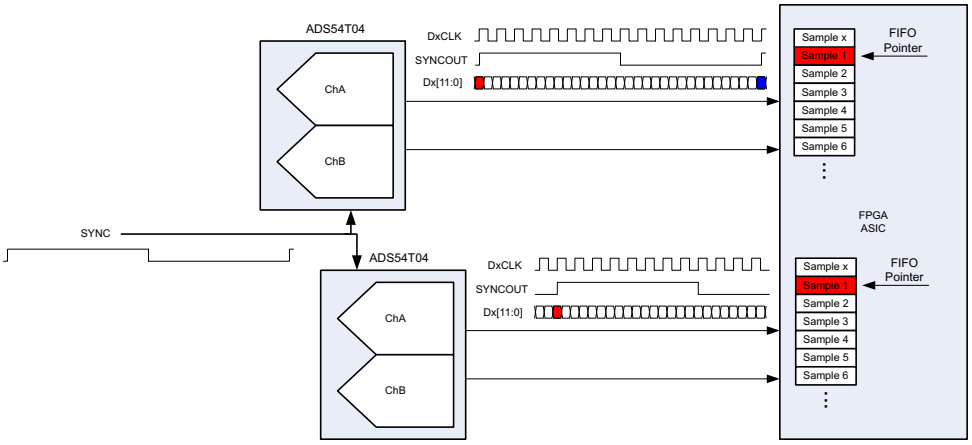


Figure 41. Decimated Low Resolution Output Data Timing Diagram

Copyright © 2012–2014, Texas Instruments Incorporated

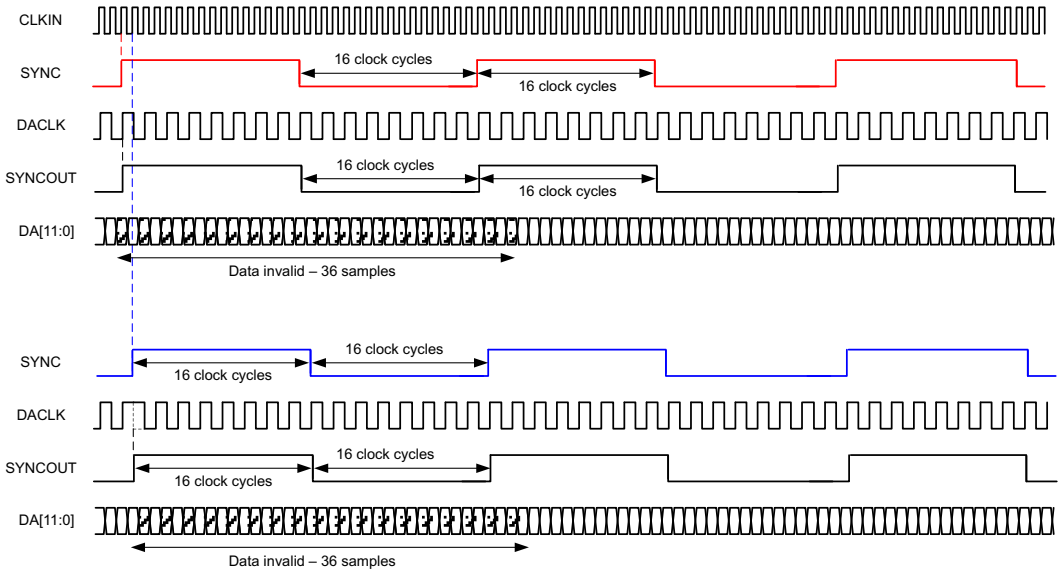
MULTI DEVICE SYNCHRONIZATION

The ADS54T04 simplifies the synchronization of data from multiple ADCs in one common receiver. Upon receiving the initial SYNC input signal, the ADS54T04 resets all the internal clocks and digital logic while also starting a SYNCOUT signal which operates on a 5bit counter (32 clock cycles). Therefore by providing a common SYNC signal to multiple ADCs their output data can be synchronized as the SYNCOUT signal marks a specific sample with the same latency in all ADCs. The SYNCOUT signal then can be used in the receiving device to synchronize the FIFO pointers across the different input data streams. Thus the output data of multiple ADCs can be aligned properly even if there are different trace lengths between the different ADCs.



The SYNC input signal should be a one time pulse to trigger the periodic 5-bit counter for SYNCOUT or a periodic signal repeating every 32 CLKIN clock cycles. It gets registered on the rising edge of the ADC input clock (CLKIN). Upon registering the initial rising edge of the SYNC signal, the internal clocks and logic get reset which results in invalid output data for 36 samples (1 complete sync cycle and 4 additional samples). The SYNCOUT signal starts with the next output clock (DACLK) rising edge and operates on a 5-bit counter. If a SYNCIN rising edge gets registered at a new position, the counter gets reset and SYNCOUT starts from the new position.

Since the ADS54T04 output interface operates with a DDR clock, the synchronization can happen on the rising edge or falling edge sample. Synchronization on the falling edge sample will result in a half cycle clock stretch of DA/BCLK. For convenience the SYNCOUT signal is available on the ChA/B output LVDS bus. When using decimation the SYNCOUT signal still operates on 32 clock cycles of CLKIN but since the output data is decimated by 2, only the first 18 samples should be discarded.



Copyright © 2012–2014, Texas Instruments Incorporated

PROGRAMMING INTERFACE

The serial interface (SIF) included in the ADS54T04 is a simple 3 or 4 pin interface. In normal mode, 3 pins are used to communicate with the device. There is an enable (SDENB), a clock (SCLK) and a bi-directional IO port (SDIO). If the user would like to use the 4 pin interface one write must be implemented in the 3 pin mode to enable 4 pin communications. In this mode, the SDO pin becomes the dedicated output. The serial interface has an 8-bit address word and a 16-bit data word. The first rising edge of SCLK after SDENB goes low will latch the read/write bit. If a high is registered then a read is requested, if it is low then a write is requested. SDENB must be brought high again before another transfer can be requested. The signal diagram is shown below:

Device Initialization

After power up, it is recommended to initialize the device through a hardware reset by applying a logic low pulse on the SRESETb pin (of width greater than 20ns), as shown in Figure 42. This resets all internal digital blocks (including SPI registers) to their default condition.

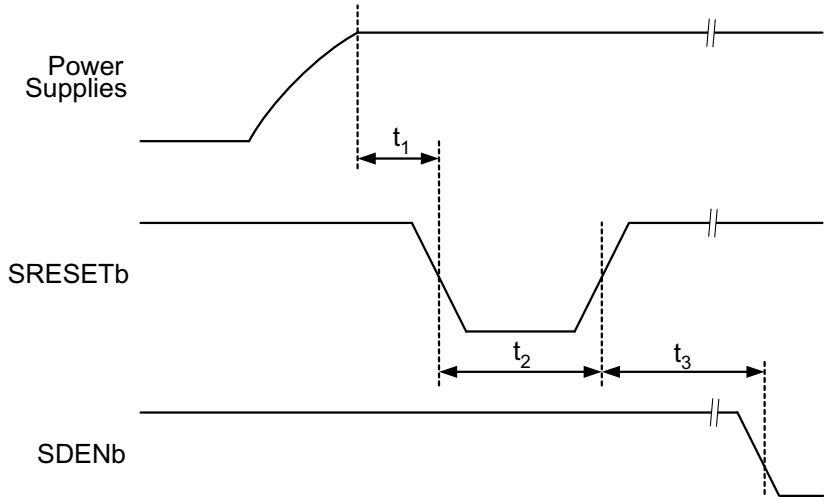


Figure 42. Device Initialization Timing Diagram

Table 1. Reset Timing

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power up to active low RESET pulse	3			ms
t_2	Reset pulse width	Active low RESET pulse width	20			ns
t_3	Register write delay	Delay from RESET disable to SDENb active	100			ns

Recommended Device Initialization Sequence:

1. Power up
2. Reset ADS54T04 using hardware reset.
3. Apply clock and input signal.
4. Set register 0x01 bit D15 to ”1” (ChA Corr EN) and bit D9 to ”1” (ChB Corr EN) to enable gain/offset correction circuit and other desired registers.
5. Set register 0x03 and 0x1A bit D14 to “1” (Start Auto Corr ChA/B). This clears and resets the accumulator values in the DC and gain correction loop.
6. Set register 0x03 and 0x1A bit D14 to “0” (Start Auto Corr ChA/B). This starts the DC and gain auto-correction loop.

Copyright © 2012–2014, Texas Instruments Incorporated

Serial Register Write

The internal register of the ADS54T04 can be programmed following these steps:

1. Drive SDENB pin low
2. Set the R/W bit to ‘0’ (bit A7 of the 8 bit address)
3. Initiate a serial interface cycle specifying the address of the register (A6 to A0) whose content has to be written
4. Write 16bit data which is latched on the rising edge of SCLK

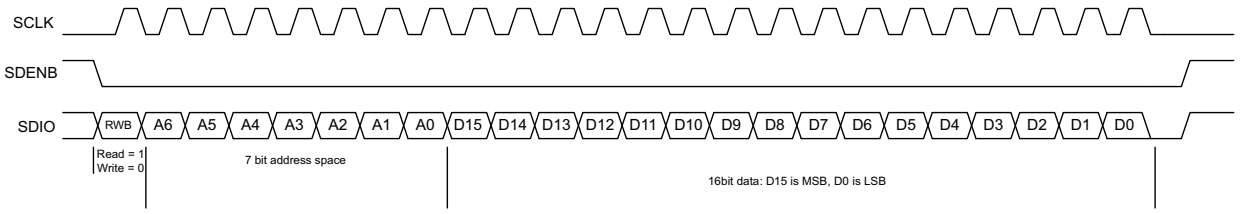


Figure 43. Serial Register Write Timing Diagram

PARAMETER		MIN	TYP(1)	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1/tSCLK)	>DC		20	MHz
t_{SLOADS}	SDENB to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SDENB hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: TMIN = –40°C to TMAX = +85°C, AVDD3V = 3.3V, AVDD, DRVDD = 1.9V, unless otherwise noted.

Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDO/SDIO pins. This read-back mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Drive SDENB pin low
2. Set the RW bit (A7) to '1'. This setting disables any further writes to the registers
3. Initiate a serial interface cycle specifying the address of the register (A6 to A0) whose content has to be read.
4. The device outputs the contents (D15 to D0) of the selected register on the SDO/SDIO pin
5. The external controller can latch the contents at the SCLK rising edge.
6. To enable register writes, reset the RW register bit to '0'.

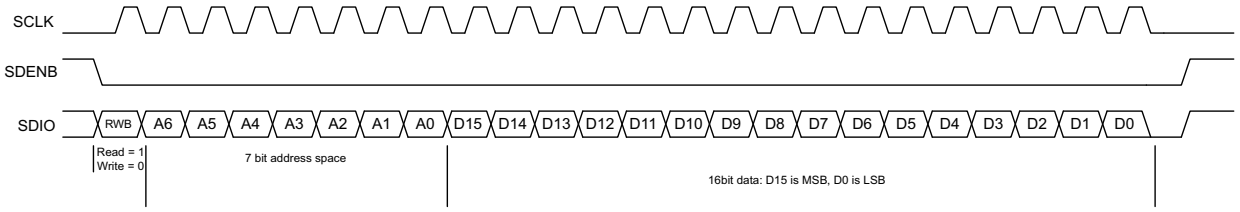


Figure 44. Serial Register Read Timing Diagram

Copyright © 2012–2014, Texas Instruments Incorporated

SERIAL REGISTER MAP(2)

(2) Multiple functions in a register can be programmed in a single write operation.

Register Address	Register Data															
A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	3/4 Wire SPI	DecFil/ Burst	0	ChA High/ Low Pass	0	0	ChB High/ Low Pass	0	0	0	Burst rate	0	0	Auto Trigger	0	0
1	ChA Corr EN	0	0	0	0	0	ChB Corr EN	0	0	0	0	0	Data Format	0	Hp Mode1	0
2	0	1	0	0	0	Over-range threshold				0	0	0	0	0	0	0
3	0	DC Offset Corr ChA	0	0	1	0	1	1	0	0	0	1	1	0	0	0
E	Sync Select														0	0
F	Sync Select				0	0	0	0	0	VREF Set			0	0	0	0
1A	0	DC Offset Corr ChB	0	0	1	0	1	1	0	0	0	1	1	0	0	0
2B	0	0	0	0	0	0	0	Temp Sensor								
2C	Reset															
34	0	0	Burst Mode N				0	0	0	0	0	0	0	0	0	0
37	Sleep Modes						0	0	0	0	0	0	0	0	0	0
38	HP Mode2									BIAS EN	SYNC EN	TRIGEN	1	1	1	1
3A	LVDS Current Strength			LVDS SW		Internal LVDS Termination		0	0	0	0	DACLK EN	DBCLK EN	0	OVRA EN	OVRB EN
66	LVDS Output Bus A EN															
67	LVDS Output Bus B EN															

DESCRIPTION OF SERIAL INTERFACE REGISTERS

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	3/4 Wire SPI	Dec Fil/ Burst	0	ChA High/ Low Pass	0	0	ChB High/ Low Pass	0	0	0	Burst rate	0	0	Auto Trigger	0	0

D15 **3/4 Wire SPI** Enables 4-bit serial interface when set
Default 0

0 3 wire SPI is used with SDIO pin operating as bi-directional I/O port

1 4 wire SPI is used with SDIO pin operating as data input and SDO pin as data output port.

D14 **DecFil/ Burst** 2x decimation filter (Receive Mode) is enabled when bit is set
Default 0

0 Burst mode enable

1 2x decimation filter enabled

D12 **ChA High/Low Pass** (Decimation filter must be enabled first: set bit D14)
Default 0

0 Low Pass

1 High Pass

Copyright © 2012–2014, Texas Instruments Incorporated

D9 **ChB High/Low Pass** (Decimation filter must be enabled first: set bit D14)
Default 0

0 Low Pass

1 High Pass

D5 **Burst Rate** Low resolution output data rate in burst mode
Default 0

0 Low resolution (9bit) full output rate

1 Decimated low resolution output (4x decimation, 11bit resolution)

D2 **Auto Trigger** Enables auto trigger mode in burst mode without the need to control the trigger pin.
Default 0

0 Manual trigger mode using the external trigger input pin

1 Auto trigger mode enabled

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	ChA Corr EN	0	0	0	0	0	ChB Corr EN	0	0	0	0	0	Data Format	0	HP Mode1	0

D15 **ChA Corr EN (should be enabled for maximum performance)**
Default 0

0 auto gain correction disabled

1 auto gain correction enabled

D9 **ChB Corr EN (should be enabled for maximum performance)**
Default 0

0 auto gain correction disabled

1 auto gain correction enabled

D3 **Data Format**
Default 0

0 Two's complement

1 Offset Binary

D1 **HP Mode 1**
Default 0

1 Must be set to 1 for optimum performance

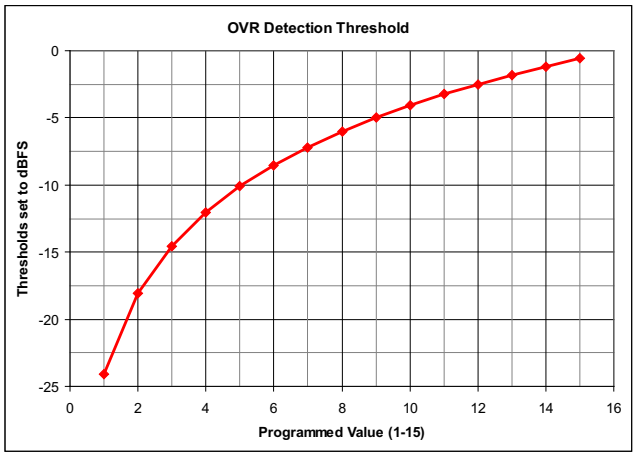
Copyright © 2012–2014, Texas Instruments Incorporated

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2	0	1	0	0	0	Over-range threshold				0	0	0	0	0	0	0

D14 Read back 1.

D10-D7 **Over-range threshold** The over-range detection is triggered 12 output clock cycles after the overload condition occurs. The threshold at which the OVR is triggered = 1.0V x [decimal value of <Over-range threshold>]/16. After power up or reset, the default value is 15 (decimal) which corresponds to a OVR threshold of 0.56dB below fullscale (20*log(15/16)). This OVR threshold is applicable to both channels.

Default 1111



Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3	0	DC Offset Coff ChA	0	0	1	0	1	1	0	0	0	1	1	0	0	0

D14 **DC Offset Corr ChA** Starts DC offset correction loop for ChA
Default 1

0 Starts offset correction loop for ChA

1 DC offset correction loop is cleared

D11, 9, 8, 4, 3 Must be set to 1 for maximum performance
Default 1

Copyright © 2012–2014, Texas Instruments Incorporated

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
E	Sync Select														0	0

D15-D2	**Sync Select** Default 1010 1010 1010 10	Sync selection for the clock generator block (also need to see address 0x0F)
0000 0000 0000 00	Sync is disabled	
0101 0101 0101 01	Sync is set to one shot (one time synchronization only)	
1010 1010 1010 10	Sync is derived from SYNC input pins	
1111 1111 1111 11	not supported	

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F	Sync Select				0	0	0	0	0	VREF Sel			0	0	0	0

D15-D12	**Sync Select** Default 1010	Sync selection for the clock generator block
0000	Sync is disabled	
0101	Sync is set to one shot (one time synchronization only)	
1010	Sync is derived from SYNC input pins	
1111	not supported	
D6-D4	**VREF SEL** Default 000	Internal voltage reference selection
000	1.0V	
001	1.25V	
010	0.9V	
011	0.8V	
100	1.15V	
Others	external reference	

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1A	0	DC Offset Corr ChB	0	0	1	0	1	1	0	0	0	1	1	0	0	0

D14	**DC Offset Corr ChB** Default 1	Starts DC offset correction loop for ChB
0	Starts offset correction loop for ChB	
1	DC offset correction loop is cleared	
D11, 9, 8, 4, 3	Must be set to 1 for maximum performance Default 1	

Copyright © 2012–2014, Texas Instruments Incorporated

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2B	0	0	0	0	0	0	0	Temp Sensor								

D8-D0 **Temp Sensor** Internal temperature sensor value – read only

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2C	Reset															

D15-D0 **Reset** Default 0000 This is a software reset to reset all SPI registers to their default value. Self clears to 0.

1101001011110000 Perform software reset

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
34	0	0	Burst Mode N				0	0	0	0	0	0	0	0	0	0

D13-D10 **Burst Mode N** Default 0000 This is the parameter that sets the amount of high resolution samples in burst mode

0000 N = 10

0001 N = 11

... ...

1111 N = 25

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
37	Sleep Modes						0	0	0	0	0	0	0	0	0	0

D15-D14 **Sleep Modes** Default 00 Sleep mode selection which is controlled by the ENABLE pin. Sleep modes are active when ENABLE pin goes low.

000000 Complete shut down Wake up time 2.5 ms

100000 Stand-by mode Wake up time 100 µs

110000 Deep sleep mode Wake up time 20 µs

110101 Light sleep mode Wake up time 2 µs

Copyright © 2012–2014, Texas Instruments Incorporated

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38	HP Mode 2									Bias EN	SYNC EN	TRIG EN	1	1	1	1

D15-D7	**HP Mode 2** Default 111111111	
1	Set to 1 for normal operation	
D6	**BIAS EN** Default 1	Enables internal fuse bias voltages – can be disabled after power up to save power.
0	Internal bias powered down	
1	Internal bias enabled	
D5	**SYNC EN** Default 1	Enables the SYNC input buffer.
0	SYNC input buffer disabled	
1	SYNC input bffer enabled	
D4	**TRIG EN** Default 1	Enables the TRIGGER input buffer.
0	TRIGGER input buffer disabled	
1	TRIGGER input bffer enabled	
D3-D0	Read back 1	

Copyright © 2012–2014, Texas Instruments Incorporated

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3A	LVDS Current Strength			LVDS SW		Internal LVDS Termination		0	0	0	0	DACLK EN	DBCLK EN	0	OVRA EN	OVRB EN

D15-D13 **LVDS Current Strength** LVDS output current strength.
Default 000

000	2 mA	100	3 mA
001	2.25 mA	101	3.25 mA
010	2.5 mA	110	3.5 mA
011	2.75 mA	111	3.75 mA

D12-D11 **LVDS SW** LVDS driver internal switch setting – correct range must be set for setting in D15-D13
Default 01

01 2 mA to 2.75 mA
11 3mA to 3.75mA

D10-D9 **Internal LVDS Termination** Internal termination
Default 00

00 2 kΩ
01 200 Ω
10 200 Ω
11 100 Ω

D4 **DACLK EN** Enable DACLK output buffer
Default 1

0 DACLK output buffer powered down
1 DACLK output buffer enabled

D3 **DBCLK EN** Enable DBCLK output buffer
Default 1

0 DBCLK output buffer powered down
1 DBCLK output buffer enabled

D1 **OVRA EN** Enable OVRA output buffer
Default 1

0 OVRA output buffer powered down
1 OVRA output buffer enabled

D0 **OVRB EN** Enable OVRB output buffer
Default 1

0 OVRB output buffer powered down
1 OVRB output buffer enabled

Copyright © 2012–2014, Texas Instruments Incorporated

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
66	LVDS Output Bus A EN															

D15-D0	**LVDS Output Bus A EN** Default FFFF	Individual LVDS output pin power down for channel A
0	Output is powered down	
1	Output is enabled	
D15	corresponds to TRDYP/N (pins N7, P7)	
D14	corresponds to HRESP/N (pins N6, P6)	
D13	SYNCOUTP/N (pins N5, P5)	
D12	Pins N4, P4 (no connect pins) which are not used and should be powered down for power savings	
D11-D0	corresponds to DA11-DA0	

Register Address	Register Data															
A7-A0 in hex	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
67	LVDS Output Bus B EN															

D15-D0	**LVDS Output Bus B EN** Default FFFF	Individual LVDS output pin power down for channel B
0	Output is powered down	
1	Output is enabled	
D15	corresponds to TRDYP/N (pins G3, G4)	
D14	corresponds to HRESP/N (pins F3, F4)	
D13	SYNCOUTP/N (pins F1, F2)	
D12	Pins E3, E4 (no connect pins) which are not used and should be powered down for power savings	
D11-D0	corresponds to DB11-DB0	

Copyright © 2012–2014, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision A (August 2013) to Revision B **Page**

- Added text to TRDYP/N description 4
- Added text to HRESP/N description 4
- Changed package from QFN to nFBGA in THERMAL INFORMATION 5
- Added text and figure to TEST PATTERN OUTPUT section 20
- Deleted from last paragraph in INTERLEAVING CORRECTION section 23
- Changed second paragraph in MULTI DEVICE SYNCHRONIZATION section 28
- Deleted Register Initialization section and added Device Initialization section 29
- Changed Register Address E Bits D1 and D0 to 0 in SERIAL REGISTER MAP 31
- Changed Register Address 38 Bits D3 to D0 from 0 to 1 in SERIAL REGISTER MAP 31
- Changed Register Address 1 Bit D14 from 1 to 0 32
- Changed Register Address E Bit D1 and D0 to 0 34
- Changed Register Address 38 Bits D3 to D0 from 0 to 1 and add D3 to D0 Read back 1 36
- Changed Register Address 66 D15-D10 to D15-D0 and DA11-D0 to DA11-DA0 38
- Changed Register Address 67 D15-D10 to D15-D0 38

Changes from Original (Decmber 2012) to Revision A **Page**

- Changed D15-10 in register 66 From: Individual LVDS output pin power down for channel B To: Individual LVDS output pin power down for channel A 38
- Changed D15 in register 66 From: corresponds to TRDYP/N (pins G3, G4) To: corresponds to TRDYP/N (pins N7, P7) 38
- Changed D14 in register 66 From: corresponds to HRESP/N (pins F3, F4) To: corresponds to HRESP/N (pins N6, P6) 38
- Changed D13 in Register 66 From: SYNCOUTP/N (pins F1, F2) To: SYNCOUTP/N (pins N5, P5) 38
- Changed D12 in Register 66 From: "Pins E3, E4..." To: "Pins N4, P4..." 38
- Changed D11-D10 - corresponds to DB11-DB0 in Register 66 To: D11-D0 - corresponds to DA11-D0 38
- Changed D11-D10 - corresponds to DB11-DB0 in Register 67 To: D11-D0 - corresponds to DB11-DB0 38

Copyright © 2012–2014, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS54T04IZAY	Active	Production	NFBGA (ZAY) | 196	160 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS54T04I
ADS54T04IZAY.B	Active	Production	NFBGA (ZAY) | 196	160 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS54T04I
ADS54T04IZAYR	Active	Production	NFBGA (ZAY) | 196	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS54T04I
ADS54T04IZAYR.B	Active	Production	NFBGA (ZAY) | 196	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADS54T04I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

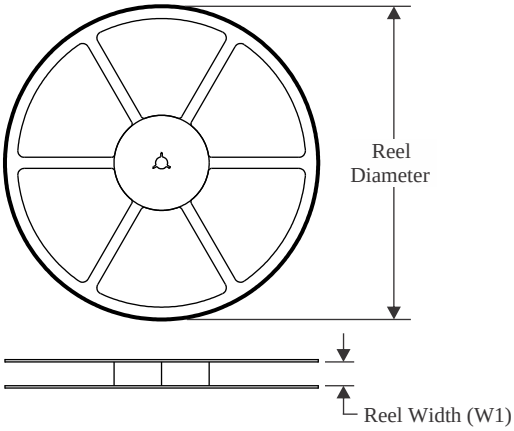
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

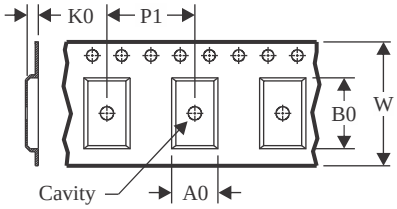
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

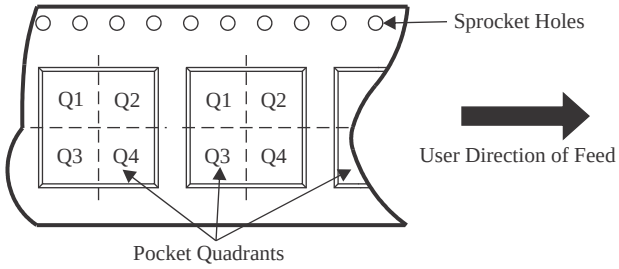


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

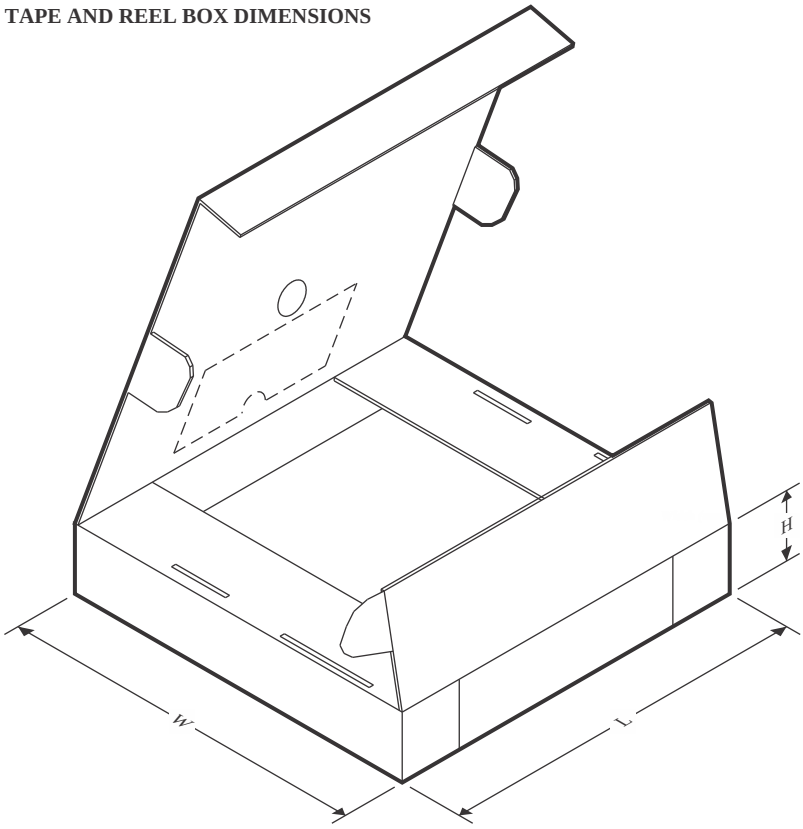
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS54T04IZAYR	NFBGA	ZAY	196	1000	330.0	24.4	12.3	12.3	2.3	16.0	24.0	Q1

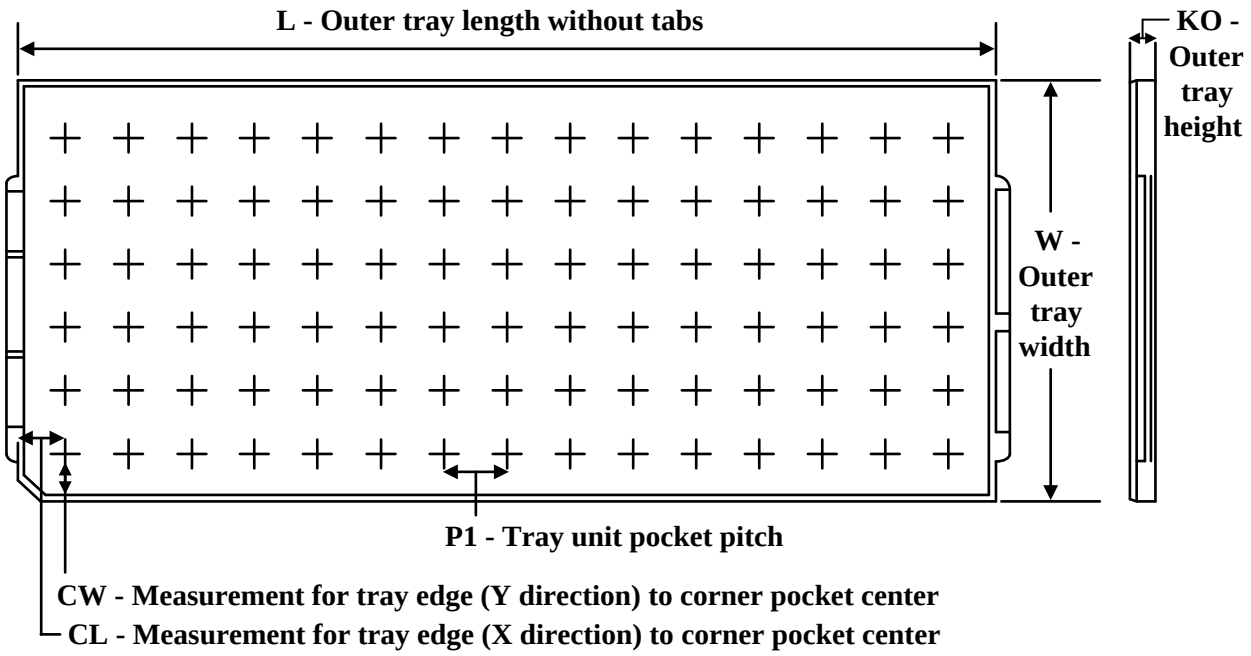
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS54T04IZAYR	NFBGA	ZAY	196	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

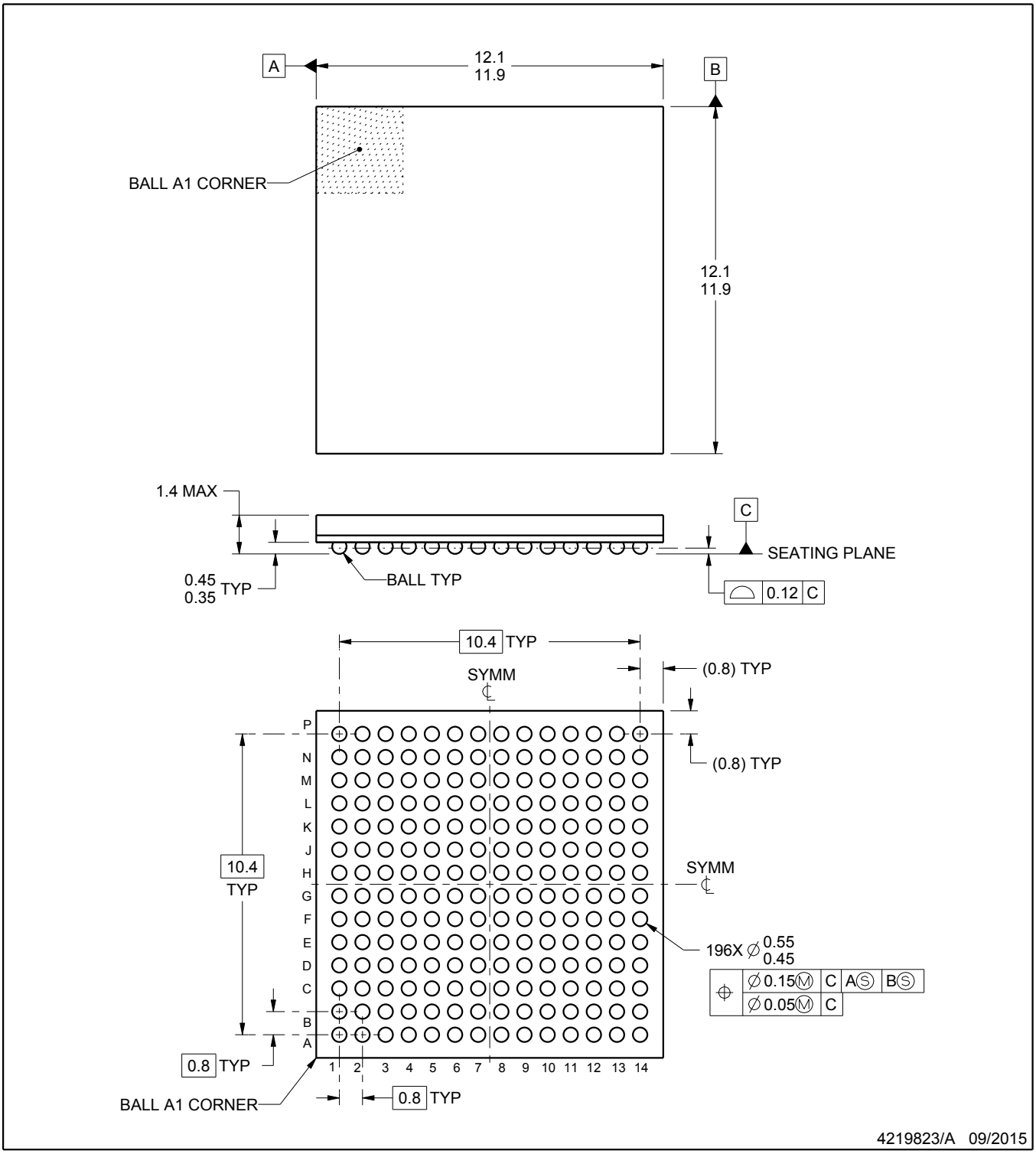
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS54T04IZAY	ZAY	NFBGA	196	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65
ADS54T04IZAY.B	ZAY	NFBGA	196	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65

PACKAGE OUTLINE

ZAY0196A

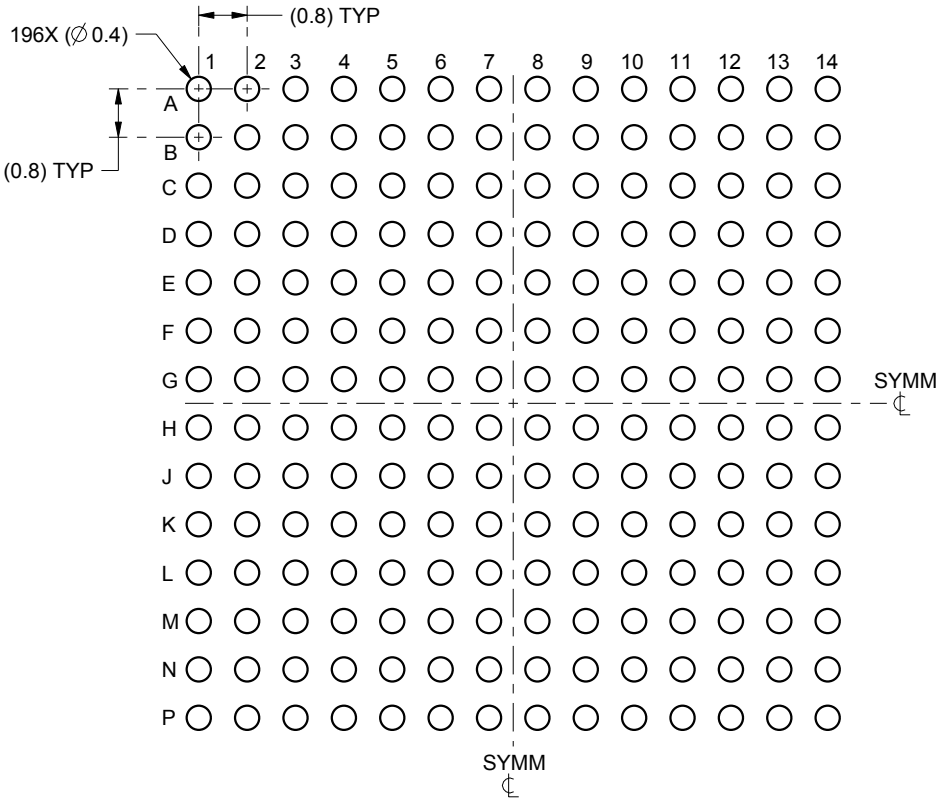
NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY

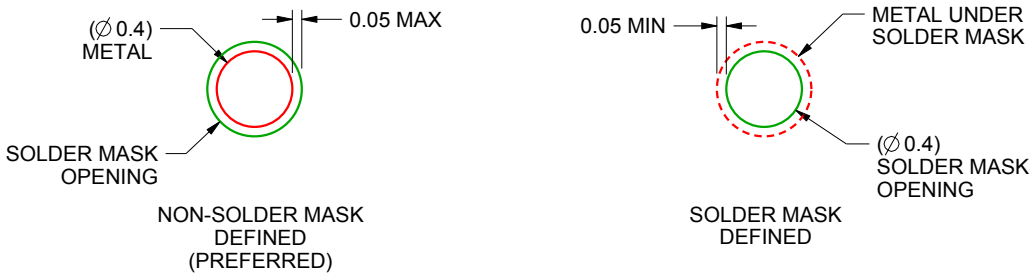


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

4219823/A 09/2015

NOTES: (continued)

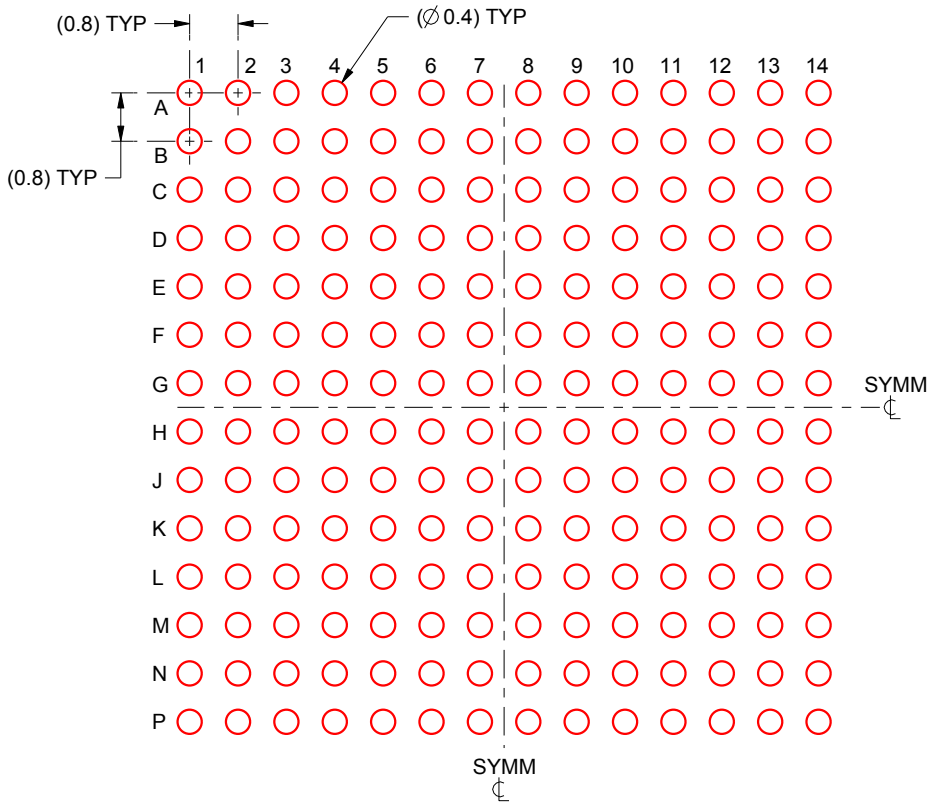
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZAY0196A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4219823/A 09/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月