# ADS54J64 四通道、14 位、1GSPS、2 倍过采样模数转换器

## 1 特性

- 四通道、14 位分辨率
- 最大采样率：1GSPS
- 最大输出采样率：500MSPS
- 高阻抗模拟输入缓冲器
- 模拟输入带宽 (–3 dB)：1GHz
- 输出选项：
  - 使用 16 位 NCO 的数字下变频器
  - 全速率输出高达 500MSPS 的 DDC 旁路
- 差分满量程输入：1.1$V_{PP}$
- JESD204B 接口：
  - 支持子类 1
  - 每个 ADC 一条信道，速率高达 10Gsps
  - 专用于通道对的 SYNC 引脚
- 支持多芯片同步
- 频谱性能：
  - $f_{IN}$ = 190-MHz IF（–1dBFS 时）：
    - 信噪比 (SNR)：69dBFS
    - 噪声频谱密度 (NSD)：-153dBFS/Hz
    - 无杂散动态范围 (SFDR)：86dBc（HD2，HD3），95dBFS（非 HD2，HD3）
  - $f_{IN}$ = 370-MHz IF（–3dBFS 时）：
    - SNR：68.5dBFS
    - NSD：–152.5dBFS/Hz
    - SFDR：80dBc（HD2，HD3），86dBFS（非 HD2，HD3）
- 72 引脚 VQFN 封装 (10mm × 10mm)
- 功耗：625 mW/通道，共 2.5W
- 电源：1.15V、1.15V、1.9V

## 2 应用

- 多载波多模式 GSM 蜂窝基础设施基站
- 电信接收器
- 雷达和天线阵列
- 电缆 CMTS，DOCSIS 3.1 接收器
- 通信测试设备
- 微波接收器
- 软件定义无线电 (SDR)
- 数字转换器
- 医疗成像和诊断功能

## 3 说明

ADS54J64 器件是四通道、14 位、1GSPS 模数转换器 (ADC)，提供宽带宽、2倍过采样和高 SNR。ADS54J64 支持 JESD204B 串行接口，每个通道上具有 1 条信道，数据速率高达 10Gbps。经缓冲的模拟输入可在较宽频率范围内提供一致的阻抗，并最大程度降低采样保持干扰能量。ADS54J64 以超低功耗在较大输入频率范围内提供出色的无杂散动态范围 (SFDR)。数字信号处理块包含复频混频器，后接低通滤波器，低通滤波器具有 2 倍抽取率和 4 倍抽取率两个选项，支持高达 200MHz 的接收带宽。ADS54J64 还支持 DDC 旁路模式的 14 位、500MSPS 输出。

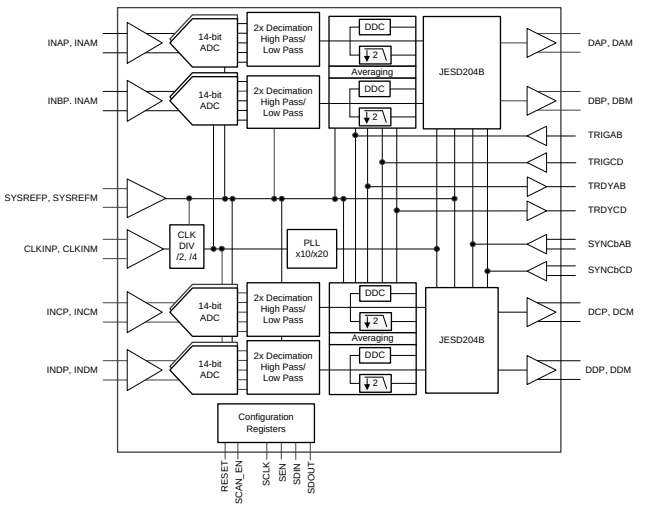
四通道 JESD204B 接口简化了连接，可实现高系统集成密度。内部锁相环 (PLL) 会将传入的 ADC 采样时钟加倍，以获得串行输出各通道的 14 位数据时所使用的位时钟。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| ADS54J64 | VQFN (72) | 10.00mm x 10.00mm |

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化框图




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# 目录

**1** 特性 ... 1
**2** 应用 ... 1
**3** 说明 ... 1
**4** 修订历史记录 ... 2
**5** **Pin Configuration and Functions** ... 3
**6** **Specifications** ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 6
6.5 Electrical Characteristics ... 7
6.6 AC Performance ... 8
6.7 Digital Characteristics ... 10
6.8 Timing Characteristics ... 11
6.9 Typical Characteristics: DDC Bypass Mode ... 12
6.10 Typical Characteristics: Mode 2 ... 18
6.11 Typical Characteristics: Mode 0 ... 19
6.12 Typical Characteristics: Dual ADC Mode ... 20
**7** **Detailed Description** ... 21
7.1 Overview ... 21
7.2 Functional Block Diagram ... 21
7.3 Feature Description ... 22
7.4 Device Functional Modes ... 23
7.5 Programming ... 31
7.6 Register Maps ... 38
**8** **Application and Implementation** ... 64
8.1 Application Information ... 64
8.2 Typical Application ... 71
**9** **Power Supply Recommendations** ... 72
**10** **Layout** ... 73
10.1 Layout Guidelines ... 73
10.2 Layout Example ... 73
**11** 器件和文档支持 ... 74
11.1 接收文档更新通知 ... 74
11.2 社区资源 ... 74
11.3 商标 ... 74
11.4 静电放电警告 ... 74
11.5 Glossary ... 74
**12** 机械、封装和可订购信息 ... 74

## 4 修订历史记录

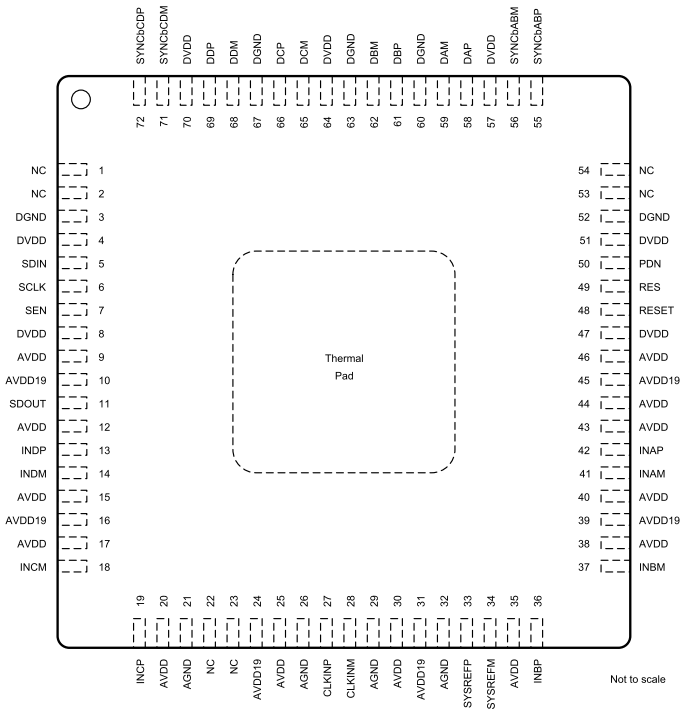
注：之前版本的页码可能与当前版本有所不同。

| 日期 | 修订版本 | 说明 |
|---|---|---|
| 2017 年 10 月 | * | 初始发行版。 |


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# 5 Pin Configuration and Functions

**RMP Package**
**72-Pin VQFN**
**Top View**




## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **INPUT, REFERENCE** | | | |
| INAM | 41 | I | Differential analog input pin for channel A, internal bias via a 2-kΩ resistor to $V_{CM}$ |
| INAP | 42 | | |
| INBM | 37 | I | Differential analog input pin for channel B, internal bias via a 2-kΩ resistor to $V_{CM}$ |
| INBP | 36 | | |
| INCM | 18 | I | Differential analog input pin for channel C, internal bias via a 2-kΩ resistor to $V_{CM}$ |
| INCP | 19 | | |
| INDM | 14 | I | Differential analog input pin for channel D, internal bias via a 2-kΩ resistor to $V_{CM}$ |
| INDP | 13 | | |
| **CLOCK, SYNC** | | | |
| CLKINM | 28 | I | Differential clock input pin for the ADC with internal 100-Ω differential termination; requires external ac coupling |
| CLKINP | 27 | | |
| SYSREFM | 34 | I | External SYSREF input; requires dc coupling and external termination |
| SYSREFP | 33 | | |

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## Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **CONTROL, SERIAL** | | | |
| NC | 1, 2, 22, 23, 53, 54 | — | No connection |
| PDN | 50 | I/O | Power down. This pin can be configured via an SPI register setting. This pin has an internal 10-kΩ pulldown resistor. |
| RES | 49 | — | Reserved pin, connect to GND |
| RESET | 48 | I | Hardware reset; active high. This pin has an internal 10-kΩ pulldown resistor. |
| SCLK | 6 | I | Serial interface clock input. This pin has an internal 10-kΩ pulldown resistor. |
| SDIN | 5 | I | Serial interface data input. This pin has an internal 10-kΩ pulldown resistor. |
| SDOUT | 11 | O | 1.8-V logic serial interface data output |
| SEN | 7 | I | Serial interface enable. This pin has an internal 10-kΩ pullup resistor to DVDD. |
| **DATA INTERFACE** | | | |
| DAM | 59 | O | JESD204B serial data output pin for channel A |
| DAP | 58 | | |
| DBM | 62 | O | JESD204B serial data output pin for channel B |
| DBP | 61 | | |
| DCM | 65 | O | JESD204B serial data output pin for channel C |
| DCP | 66 | | |
| DDM | 68 | O | JESD204B serial data output pin for channel D |
| DDP | 69 | | |
| SYNCbABM | 56 | I | Synchronization input pin for JESD204B port channels A and B. This pin can be configured via SPI to a SYNCb signal for all four channels. This pin has an internal differential termination of 100 Ω. |
| SYNCbABP | 55 | | |
| SYNCbCDM | 71 | I | Synchronization input pin for JESD204B port channels C and D. This pin can be configured via SPI to a SYNCb signal for all four channels. This pin has an internal differential termination of 100 Ω. |
| SYNCbCDP | 72 | | |
| **POWER SUPPLY** | | | |
| AGND | 21, 26, 29, 32 | I | Analog ground |
| AVDD | 9, 12, 15, 17, 20, 25, 30, 35, 38, 40, 43, 44, 46 | I | Analog 1.15-V power supply |
| AVDD19 | 10, 16, 24, 31, 39, 45 | I | Analog 1.9-V supply for analog buffer |
| DGND | 3, 52, 60, 63, 67 | I | Digital ground |
| DVDD | 4, 8, 47,51, 57, 64, 70 | I | Digital 1.15-V power supply |
| Thermal pad | Pad | — | Connect to GND |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | AVDD19 | –0.3 | 2.1 | V |
| | AVDD | –0.3 | 1.4 | |
| | DVDD | –0.3 | 1.4 | |
| Voltage between AGND and DGND | | –0.3 | 0.3 | V |
| Voltage applied to input pins | INAP, INBP, INAM, INBM, INCP, INDP, INCM, INDM | –0.3 | 2.1 | V |
| | CLKINP, CLKINM | –0.3 | AVDD + 0.3 | |
| | SYSREFP, SYSREFM | –0.3 | 1.9 | |
| | SCLK, SEN, SDIN, RESET, SYNCbABP, SYNCbABM, SYNCbCDP, SYNCbCDM, PDN, TRIGAB, TRIGCD | –0.2 | AVDD19 + 0.3 | |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage range | AVDD19 | | 1.8 | 1.9 | 2 | V |
| | AVDD | | 1.1 | 1.15 | 1.2 | |
| | DVDD | | 1.1 | 1.15 | 1.2 | |
| Analog inputs | Differential input voltage range | | | 1.1 | | $V_{PP}$ |
| | Input common-mode voltage (VCM) | | | 1.3 | | V |
| Clock inputs | Input clock frequency, device clock frequency | | 400 | | 1000 | MHz |
| | Input clock amplitude differential ($V_{CLKP} – V_{CLKM}$) | Sine wave, ac-coupled | | 1.5 | | $V_{PP}$ |
| | | LVPECL, ac-coupled | | 1.6 | | |
| | | LVDS, ac-coupled | | 0.7 | | |
| | Input device clock duty cycle, default after reset | | 45% | 50% | 55% | |
| Temperature | Operating free-air, $T_A$ | | –40 | | 100(1) | °C |
| | Operating junction, $T_J$ | | | | 105(2) | |
| | Specified maximum, measured at the device footprint thermal pad on the printed circuit board, $T_{P-MAX}$ | | | | 104.5(3) | |

(1) Assumes system thermal design meets the $T_J$ specification.
(2) Prolonged use above this junction temperature can increase the device failure-in-time (FIT) rate.
(3) The recommended maximum temperature at the PCB footprint thermal pad assumes the junction-to-package bottom thermal resistance, $R_{\theta JC(bot)}$ = 0.2°C/W, the thermal resistance of the device thermal pad connection to the PCB footprint is negligible, and the device power consumption is 2.5 W.

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## 6.4 Thermal Information

| THERMAL METRIC(1) | | ADS54J64 RMP (VQFNP) 72 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (2) | 22.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance (3) | 5.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance (3) | 2.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter (4) | 0.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter (5) | 2.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance (6) | 0.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψJT, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θJA, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψJB, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θJA , using a procedure described in JESD51-2a (sections 6 and 7).


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## 6.5 Electrical Characteristics

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, input clock frequency = 1 GHz, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **GENERAL** | | | | | | |
| | ADC sampling rate | | | | 1 | GSPS |
| | Resolution | | 14 | | | Bits |
| **POWER SUPPLY** | | | | | | |
| AVDD19 | 1.9-V analog supply | | 1.85 | 1.9 | 1.95 | V |
| AVDD | 1.15-V analog supply | | 1.1 | 1.15 | 1.2 | V |
| DVDD | 1.15-V digital supply | | 1.1 | 1.15 | 1.2 | V |
| $I_{AVDD19}$ | 1.9-V analog supply current | 100-MHz, full-scale input on all four channels | | 618 | | mA |
| $I_{AVDD}$ | 1.15-V analog supply current | 100-MHz, full-scale input on all four channels | | 415 | | mA |
| $I_{DVDD}$ | 1.15-V digital supply current | DDC bypass mode (mode 8), 100-MHz, full-scale input on all four channels | | 629 | | mA |
| | | Mode 3, 100-MHz, full-scale input on all four channels | | 730 | | |
| | | Mode 0 and 2, 100-MHz, full-scale input on all four channels | | 674 | | |
| | | Mode 1, 4, 6, and 7, 100-MHz, full-scale input on all four channels | | 703 | | |
| $P_{DIS}$ | Total power dissipation | DDC bypass mode (mode 8), 100-MHz, full-scale input on all four channels | | 2.37 | | W |
| | | Mode 3, 100-MHz, full-scale input on all four channels | | 2.49 | | |
| | | Mode 0 and 2, 100-MHz, full-scale input on all four channels | | 2.42 | | |
| | | Mode 1, 4, 6, and 7, 100-MHz, full-scale input on all four channels | | 2.46 | | |
| | Global power-down power dissipation | Full-scale input on all four channels | | 120 | | mW |
| **ANALOG INPUTS** | | | | | | |
| | Differential input full-scale voltage | | | 1.1 | | $V_{PP}$ |
| | Input common-mode voltage | | | 1.3 | | V |
| | Differential input resistance | At $f_{IN}$ = dc | | 4 | | kΩ |
| | Differential input capacitance | | | 2.5 | | pF |
| | Analog input bandwidth (3 dB) | | | 1000 | | MHz |
| **ISOLATION** | | | | | | |
| | Crosstalk(1) isolation between near channels (channels A and B are near to each other, channels C and D are near to each other) | $f_{IN}$ = 10 MHz | | 75 | | dBFS |
| | | $f_{IN}$ = 100 MHz | | 75 | | |
| | | $f_{IN}$ = 170 MHz | | 74 | | |
| | | $f_{IN}$ = 270 MHz | | 72 | | |
| | | $f_{IN}$ = 370 MHz | | 71 | | |
| | | $f_{IN}$ = 470 MHz | | 70 | | |
| | Crosstalk(1) isolation between far channels (channels A and B are far from channels C and D) | $f_{IN}$ = 10 MHz | | 110 | | dBFS |
| | | $f_{IN}$ = 100 MHz | | 110 | | |
| | | $f_{IN}$ = 170 MHz | | 110 | | |
| | | $f_{IN}$ = 270 MHz | | 110 | | |
| | | $f_{IN}$ = 370 MHz | | 110 | | |
| | | $f_{IN}$ = 470 MHz | | 110 | | |

(1) Crosstalk is measured with a –1-dBFS input signal on the aggressor channel and no input on the victim channel.

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## Electrical Characteristics (continued)

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, input clock frequency = 1 GHz, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **CLOCK INPUT** | | | | | |
| Internal clock biasing | CLKINP and CLKINM pins are connected to the internal biasing voltage through a 5-kΩ resistor | | 0.7 | | V |

## 6.6 AC Performance

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, input clock frequency = 1 GHz, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DDC BYPASS MODE MIN | DDC BYPASS MODE TYP | DDC BYPASS MODE MAX | DECIMATE-BY-4 (DDC Mode 2) MIN | DECIMATE-BY-4 (DDC Mode 2) TYP | DECIMATE-BY-4 (DDC Mode 2) MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| SNR | Signal-to-noise ratio | $f_{IN}$ = 10 MHz, $A_{IN}$ = –1 dBFS | | 69.9 | | | 72.2 | | dBFS |
| | | $f_{IN}$ = 70 MHz, $A_{IN}$ = –1 dBFS | | 69.6 | | | 71.8 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS | | 69.2 | | | 71.8 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –3 dBFS | 66.5 | 69.6 | | | 71 | | |
| | | $f_{IN}$ = 300 MHz, $A_{IN}$ = –3 dBFS | | 69.3 | | | 71.7 | | |
| | | $f_{IN}$ = 370 MHz, $A_{IN}$ = –3 dBFS | | 68.7 | | | 71.3 | | |
| | | $f_{IN}$ = 470 MHz, $A_{IN}$ = –3 dBFS | | 68.4 | | | 69.8 | | |
| NSD | Noise spectral density | $f_{IN}$ = 10 MHz, $A_{IN}$ = –1 dBFS | | –153.9 | | | –153.2 | | dBFS/Hz |
| | | $f_{IN}$ = 70 MHz, $A_{IN}$ = –1 dBFS | | –153.6 | | | –152.8 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS | | –153.2 | | | –152.7 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –3 dBFS | –150.5 | –153.6 | | | –153.2 | | |
| | | $f_{IN}$ = 300 MHz, $A_{IN}$ = –3 dBFS | | –152.8 | | | –152.7 | | |
| | | $f_{IN}$ = 370 MHz, $A_{IN}$ = –3 dBFS | | –152.5 | | | –152.2 | | |
| | | $f_{IN}$ = 470 MHz, $A_{IN}$ = –3 dBFS | | –151.5 | | | –151 | | |
| SFDR (1) | Spurious-free dynamic range | $f_{IN}$ = 10 MHz, $A_{IN}$ = –1 dBFS | | 83 | | | 83 | | dBc |
| | | $f_{IN}$ = 70 MHz, $A_{IN}$ = –1 dBFS | | 81 | | | 100 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS | | 87 | | | 100 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –3 dBFS | 78 | 88 | | | 98 | | |
| | | $f_{IN}$ = 300 MHz, $A_{IN}$ = –3 dBFS | | 79 | | | 98 | | |
| | | $f_{IN}$ = 370 MHz, $A_{IN}$ = –3 dBFS, input clock frequency = 983.04 MHz | | 82 | | | 70 | | |
| | | $f_{IN}$ = 470 MHz, $A_{IN}$ = –3 dBFS | | 78 | | | 76 | | |
| SINAD | Signal-to-noise and distortion ratio | $f_{IN}$ = 10 MHz, $A_{IN}$ = –1 dBFS | | 68.5 | | | 70.6 | | dBFS |
| | | $f_{IN}$ = 70 MHz, $A_{IN}$ = –1 dBFS | | 68.5 | | | 70.6 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS | | 68.2 | | | 72.2 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –3 dBFS | | 68.5 | | | 73 | | |
| | | $f_{IN}$ = 300 MHz, $A_{IN}$ = –3 dBFS | | 68.9 | | | 72.3 | | |
| | | $f_{IN}$ = 370 MHz, $A_{IN}$ = –3 dBFS | | 68 | | | 68.2 | | |
| | | $f_{IN}$ = 470 MHz, $A_{IN}$ = –3 dBFS | | 68 | | | 69 | | |

(1) Harmonic distortion performance can be significantly improved by using the frequency planning explained in the *Frequency Planning* section.


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## AC Performance (continued)

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, input clock frequency = 1 GHz, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DDC BYPASS MODE MIN | DDC BYPASS MODE TYP | DDC BYPASS MODE MAX | DECIMATE-BY-4 (DDC Mode 2) MIN | DECIMATE-BY-4 (DDC Mode 2) TYP | DECIMATE-BY-4 (DDC Mode 2) MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| HD2[1] | Second-order harmonic distortion | $f_{IN}$ = 10 MHz, $A_{IN}$ = –1 dBFS | | –83 | | | –90 | | dBc |
| | | $f_{IN}$ = 70 MHz, $A_{IN}$ = –1 dBFS | | –82 | | | –100 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS | | –85 | | | –98 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –3 dBFS | –78 | –86 | | | –100 | | |
| | | $f_{IN}$ = 300 MHz, $A_{IN}$ = –3 dBFS | | –82 | | | –100 | | |
| | | $f_{IN}$ = 370 MHz, $A_{IN}$ = –3 dBFS input clock frequency = 983.04 MHz | | –82 | | | –69 | | |
| | | $f_{IN}$ = 470 MHz, $A_{IN}$ = –3 dBFS | | –100 | | | –94 | | |
| HD3[1] | Third-order harmonic distortion | $f_{IN}$ = 10 MHz, $A_{IN}$ = –1 dBFS | | –83 | | | –85 | | dBc |
| | | $f_{IN}$ = 70 MHz, $A_{IN}$ = –1 dBFS | | –81 | | | –100 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS | | –92 | | | –100 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –3 dBFS | –78 | –92 | | | –100 | | |
| | | $f_{IN}$ = 300 MHz, $A_{IN}$ = –3 dBFS | | –90 | | | –100 | | |
| | | $f_{IN}$ = 370 MHz, $A_{IN}$ = –3 dBFS | | –90 | | | –100 | | |
| | | $f_{IN}$ = 470 MHz, $A_{IN}$ = –3 dBFS | | –80 | | | –79 | | |
| Non HD2, HD3 | Spurious-free dynamic range (excluding HD2, HD3) | $f_{IN}$ = 10 MHz, $A_{IN}$ = –1 dBFS | | 95 | | | –100 | | dBFS |
| | | $f_{IN}$ = 70 MHz, $A_{IN}$ = –1 dBFS | | 95 | | | –92 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS | | 95 | | | –100 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –3 dBFS | 87 | 95 | | | –98 | | |
| | | $f_{IN}$ = 300 MHz, $A_{IN}$ = –3 dBFS | | 95 | | | –100 | | |
| | | $f_{IN}$ = 370 MHz, $A_{IN}$ = –3 dBFS | | 95 | | | –100 | | |
| | | $f_{IN}$ = 470 MHz, $A_{IN}$ = –3 dBFS | | 93 | | | –100 | | |
| THD[1] | Total harmonic distortion | $f_{IN}$ = 10 MHz, $A_{IN}$ = –1 dBFS | | –81 | | | –83 | | dBc |
| | | $f_{IN}$ = 70 MHz, $A_{IN}$ = –1 dBFS | | –79 | | | –100 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS | | –83 | | | –100 | | |
| | | $f_{IN}$ = 190 MHz, $A_{IN}$ = –3 dBFS | | –85 | | | –100 | | |
| | | $f_{IN}$ = 300 MHz, $A_{IN}$ = –3 dBFS | | –81 | | | –100 | | |
| | | $f_{IN}$ = 370 MHz, $A_{IN}$ = –3 dBFS | | –76 | | | –68 | | |
| | | $f_{IN}$ = 470 MHz, $A_{IN}$ = –3 dBFS | | –82 | | | –80 | | |
| IMD3 | Two-tone, third-order intermodulation distortion | $f_1$ = 185 MHz, $f_2$ = 190 MHz, $A_{IN}$ = –10 dBFS | | –90 | | | –87 | | dBFS |
| | | $f_1$ = 365 MHz, $f_2$ = 370 MHz, $A_{IN}$ = –10 dBFS | | –90 | | | –94 | | |
| | | $f_1$ = 465 MHz, $f_2$ = 470 MHz, $A_{IN}$ = –10 dBFS | | –85 | | | –85 | | |

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## 6.7 Digital Characteristics

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, input clock frequency = 1 GHz, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS (RESET, SCLK, SEN, SDIN, PDN, TRIGAB, TRIGCD)(1)** | | | | | | |
| $V_{IH}$ | High-level input voltage | All digital inputs support 1.2-V and 1.8-V logic levels | 0.8 | | | V |
| $V_{IL}$ | Low-level input voltage | All digital inputs support 1.2-V and 1.8-V logic levels | | | 0.4 | V |
| $I_{IH}$ | High-level input current | SEN | | 0 | | µA |
| | | RESET, SCLK, SDIN, PDN, TRIGAB, TRIGCD | | 50 | | |
| $I_{IL}$ | Low-level input current | SEN | | 50 | | µA |
| | | RESET, SCLK, SDIN, PDN, TRIGAB, TRIGCD | | 0 | | |
| | Input capacitance | | | 4 | | pF |
| **DIGITAL INPUTS** | | | | | | |
| $V_D$ | Differential input voltage | SYSREFP, SYSREFM | 0.35 | 0.45 | 0.55 | V |
| | | SYNCbABM, SYNCbABP, SYNCbCDM, SYNCbCDP | 0.35 | 0.45 | 0.8 | |
| $V_{(CM_DIG)}$ | Common-mode voltage for SYSREF | SYSREFP, SYSREFM | 0.9 | 1.2 | 1.4 | V |
| | | SYNCbABM, SYNCbABP, SYNCbCDM, SYNCbCDP | 0.9 | 1.2 | 1.4 | |
| **DIGITAL OUTPUTS (SDOUT, TRDYAB, TRDYCD)** | | | | | | |
| $V_{OH}$ | High-level output voltage | 100-µA current | AVDD19 – 0.2 | | | V |
| $V_{OL}$ | Low-level output voltage | 100-µA current | | | 0.2 | V |
| **DIGITAL OUTPUTS (JESD204B Interface: DxP, DxM)(2)** | | | | | | |
| $V_{OD}$ | Output differential voltage | With default swing setting | | 700 | | $mV_{PP}$ |
| $V_{OC}$ | Output common-mode voltage | | | 450 | | mV |
| | Transmitter short-circuit current | Transmitter pins shorted to any voltage between –0.25 V and 1.45 V | –100 | | 100 | mA |
| $z_{os}$ | Single-ended output impedance | | | 50 | | Ω |
| | Output capacitance | Output capacitance inside the device, from either output to ground | | 2 | | pF |

(1) The RESET, SCLK, SDIN, and PDN pins have a 10-kΩ (typical) internal pulldown resistor to ground, and the SEN pin has a 10-kΩ (typical) pullup resistor to DVDD.
(2) 50-Ω, single-ended external termination to DVDD.


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## 6.8 Timing Characteristics

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, input clock frequency = 1 GHz, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)

| | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SAMPLE TIMING CHARACTERISTICS** | | | | | | |
| | Aperture delay | | 0.55 | | 0.92 | ns |
| | Aperture delay matching between two channels on the same device | | | ±100 | | ps |
| | Aperture delay matching between two devices at the same temperature and supply voltage | | | ±100 | | ps |
| | Aperture jitter | | | 100 | | $f_S$ rms |
| | Wake-up time | Global power-down | | 10 | | ms |
| | | Pin power-down (fast power-down) | | 5 | | µs |
| | Data latency: ADC sample to digital output | DDC bypass mode | | 116 | | Input clock cycles |
| | | DDC mode 0 | | 204 | | |
| $t_{SU_SYSREF}$ | Setup time for SYSREF, referenced to input clock rising edge | | 350 | | 900 | ps |
| $t_{H_SYSREF}$ | Hold time for SYSREF, referenced to input clock rising edge | | 100 | | | ps |
| **JESD OUTPUT INTERFACE TIMING CHARACTERISTICS** | | | | | | |
| | Unit interval | | 100 | | | ps |
| | Serial output data rate | | | | 10 | Gbps |
| | Total jitter for BER of 1E-15 and lane rate = 10 Gbps | | | 24 | | ps |
| | Random jitter for BER of 1E-15 and lane rate = 10 Gbps | | | 0.95 | | ps rms |
| | Deterministic jitter for BER of 1E-15 and lane rate = 10 Gbps | | | 8.8 | | ps, pk-pk |
| $t_R$, $t_F$ | Data rise time, data fall time: rise and fall times measured from 20% to 80%, differential output waveform, 2.5 Gbps ≤ bit rate ≤ 10 Gbps | | | 35 | | ps |

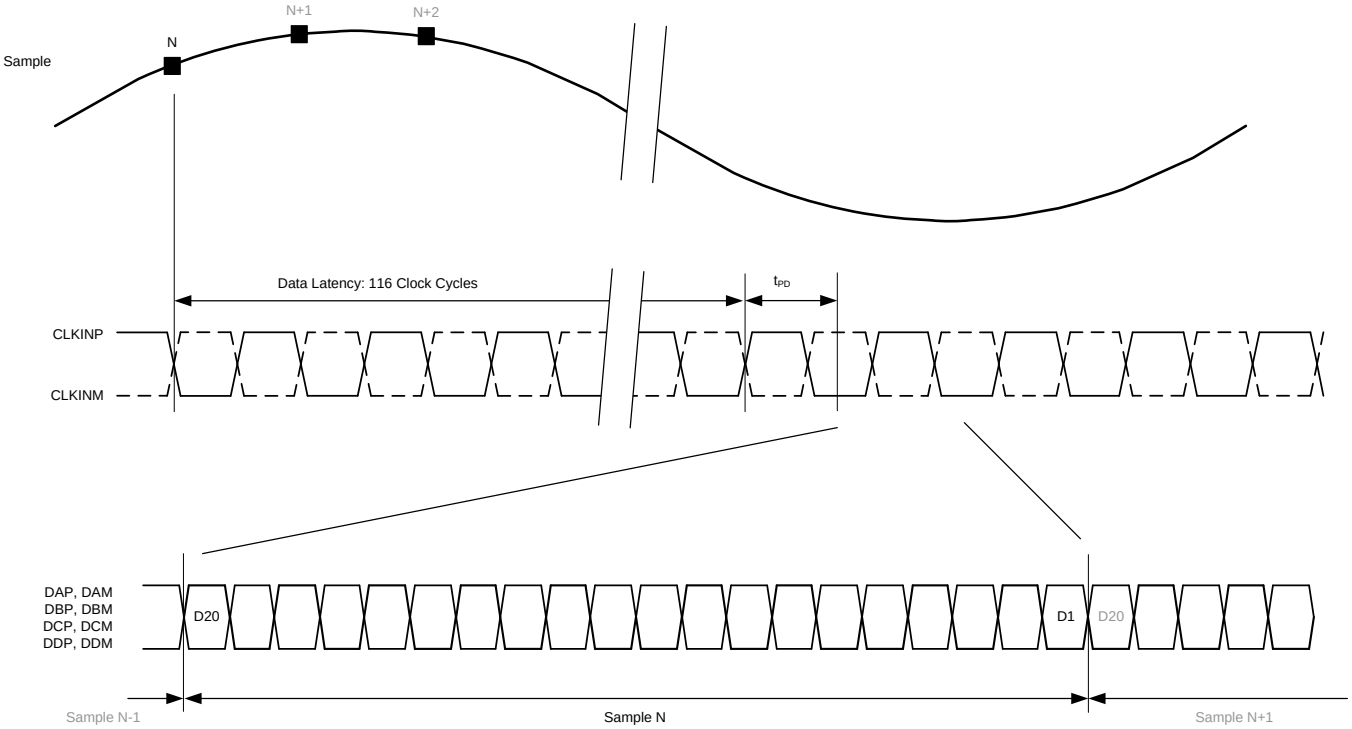
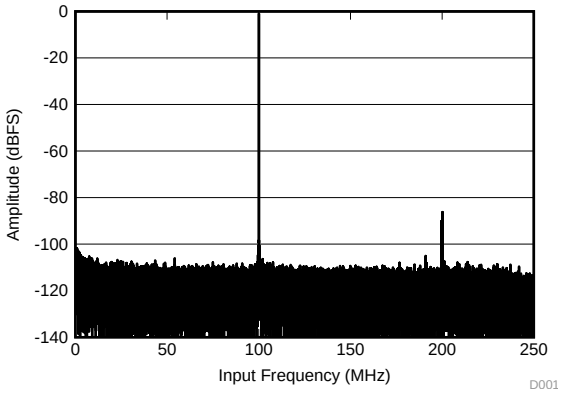



**图 1. Latency Timing Diagram in DDC Bypass Mode**

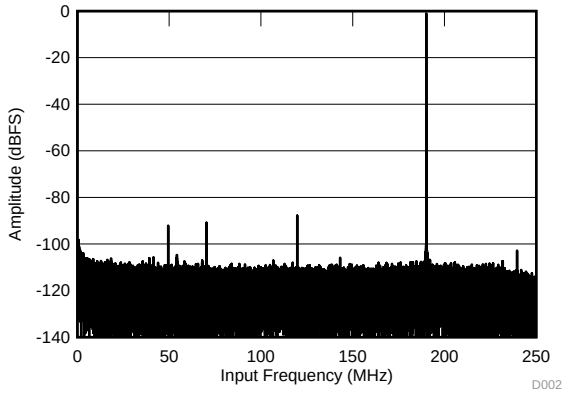
## 6.9 Typical Characteristics: DDC Bypass Mode

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, device sampling frequency = 1 GSPS, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)



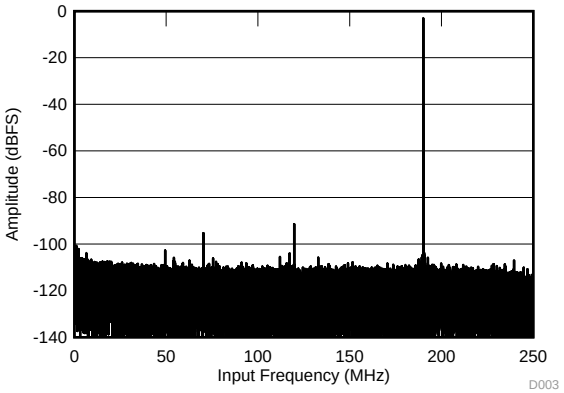

$f_{IN}$ = 100 MHz, $A_{IN}$ = –1 dBFS, SNR = 69.57 dBFS, SFDR = 85.23 dBc, SFDR = 102.09 dBc (non 23)

**图 2. FFT for 100-MHz Input Signal**



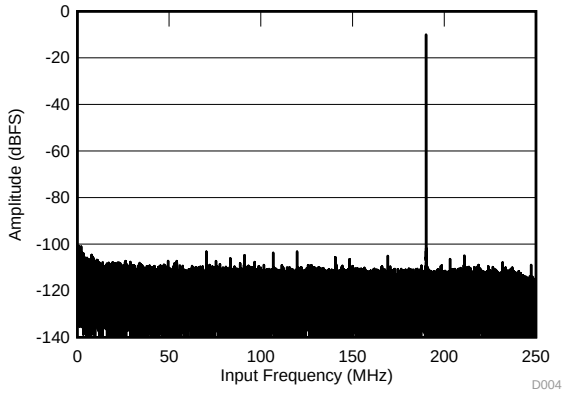

$f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS, SNR = 69.23 dBFS, SFDR = 86.83 dBc, SFDR = 91.23 dBc (non 23)

**图 3. FFT for 190-MHz Input Signal**



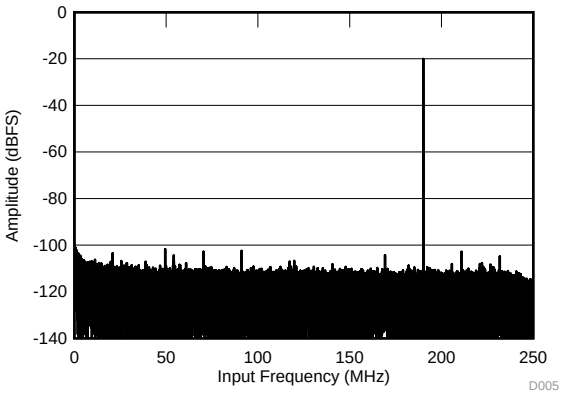

$f_{IN}$ = 190 MHz, $A_{IN}$ = –3 dBFS, SNR = 69.60 dBFS, SFDR = 88.45 dBc, SFDR = 99.78 dBc (non 23)

**图 4. FFT for 190-MHz Input Signal**



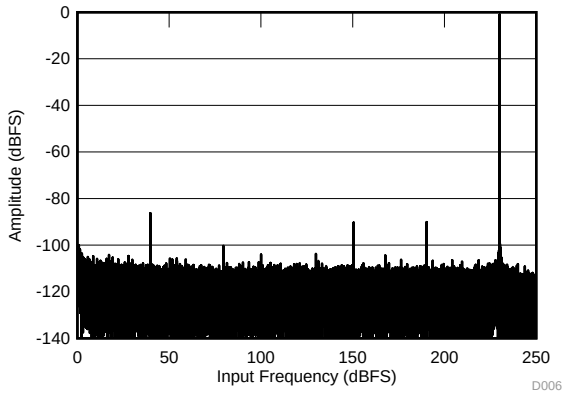

$f_{IN}$ = 190 MHz, $A_{IN}$ = –10 dBFS, SNR = 70.05 dBFS, SFDR = 93.27 dBc, SFDR = 97.26 dBc (non 23)

**图 5. FFT for 190-MHz Input Signal**




$f_{IN}$ = 190 MHz, $A_{IN}$ = –20 dBFS, SNR = 70.23 dBFS, SFDR = 81.71 dBc, SFDR = 81.71 dBc (non 23)

**图 6. FFT for 190-MHz Input Signal**



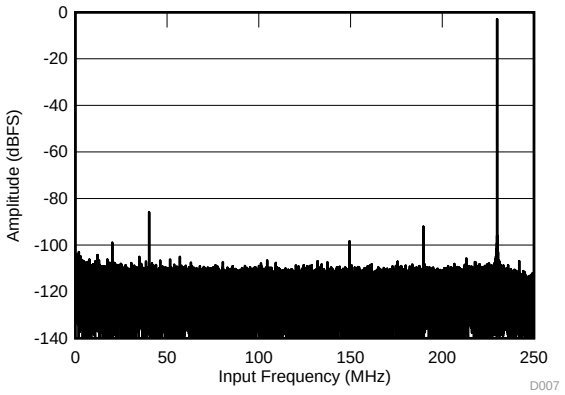

$f_{IN}$ = 230 MHz, $A_{IN}$ = –1 dBFS, SNR = 69.17 dBFS, SFDR = 85.29 dBc, SFDR = 89.30 dBc (non 23)

**图 7. FFT for 230-MHz Input Signal**


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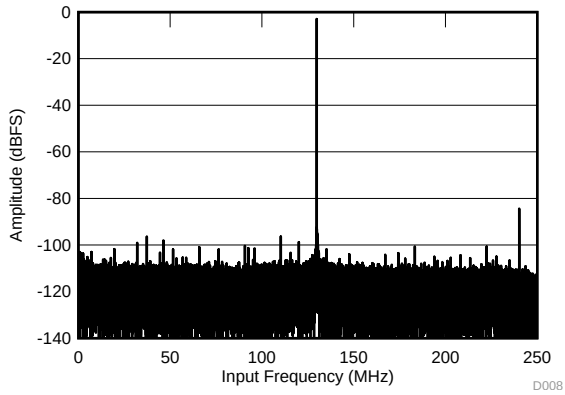
## Typical Characteristics: DDC Bypass Mode (接下页)

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, device sampling frequency = 1 GSPS, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)



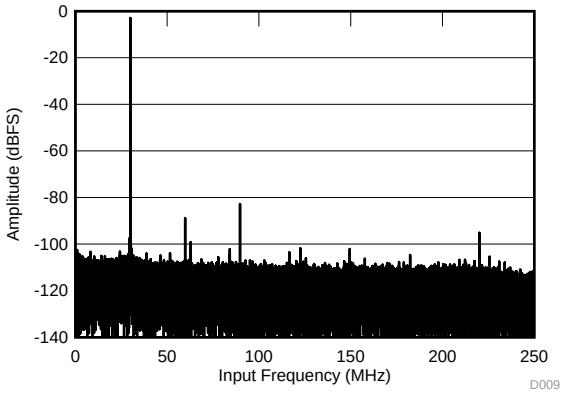

$f_{IN}$ = 270 MHz, $A_{IN}$ = –3 dBFS, SNR = 69.27 dBFS, SFDR = 82.98 dBc, SFDR = 95.4 dBc (non 23)

**图 8. FFT for 270-MHz Input Signal**



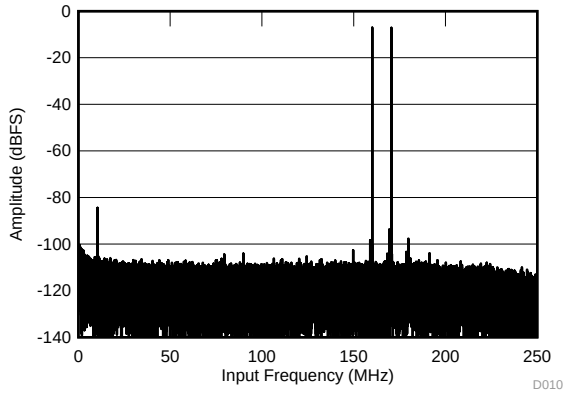

$f_{IN}$ = 370 MHz, $A_{IN}$ = –3 dBFS, SNR = 68.36 dBFS, SFDR = 81.37 dBc, SFDR = 97.28 dBc (non 23)

**图 9. FFT for 370-MHz Input Signal**



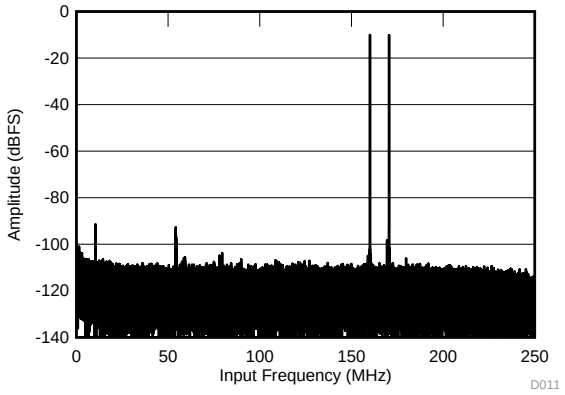

$f_{IN}$ = 470 MHz, $A_{IN}$ = –3 dBFS, SNR = 68.21 dBFS, SFDR = 79.85 dBc, SFDR = 99.12 dBc (non 23)

**图 10. FFT for 470-MHz Input Signal**



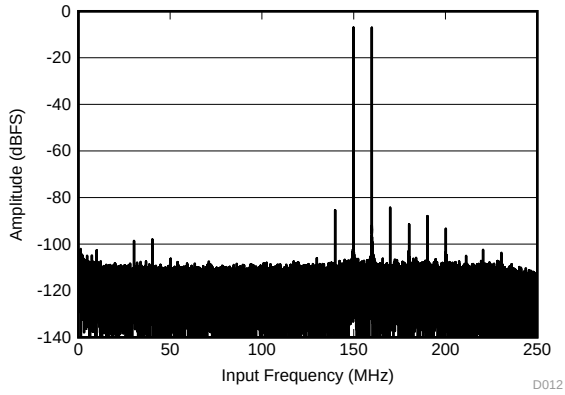

$f_{IN1}$ = 160 MHz, $f_{IN2}$ = 170 MHz, IMD = 102.68 dBFS, each tone at –7 dBFS

**图 11. FFT for Two-Tone Input Signal**




$f_{IN1}$ = 160 MHz, $f_{IN2}$ = 170 MHz, IMD = 103.44 dBFS, each tone at –10 dBFS

**图 12. FFT for Two-Tone Input Signal**

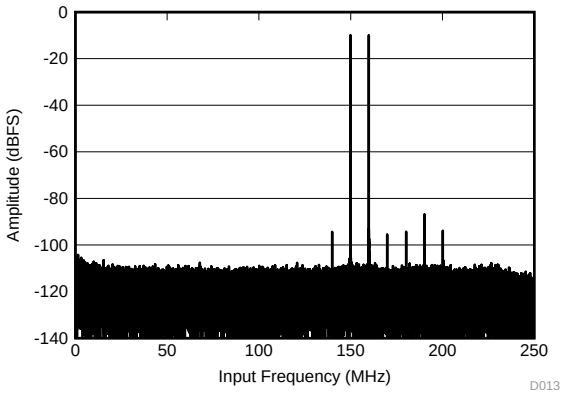



$f_{IN1}$ = 340 MHz, $f_{IN2}$ = 350 MHz, IMD = 84.34 dBFS, each tone at –7 dBFS

**图 13. FFT for Two-Tone Input Signal**

## Typical Characteristics: DDC Bypass Mode (接下页)

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, device sampling frequency = 1 GSPS, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)




$f_{IN1}$ = 340 MHz, $f_{IN2}$ = 350 MHz, IMD = 95.08 dBFS, each tone at –10 dBFS

**图 14. FFT for Two-Tone Input Signal**

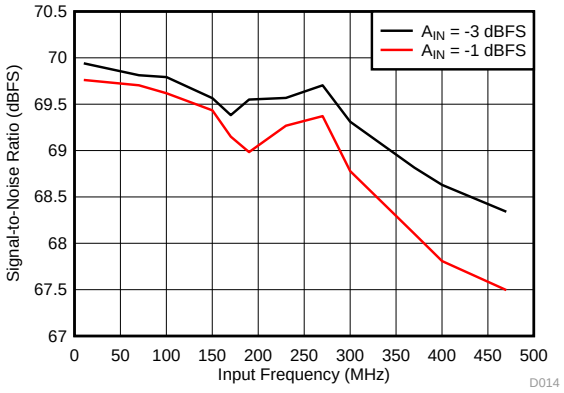



**图 15. SNR vs Input Frequency**

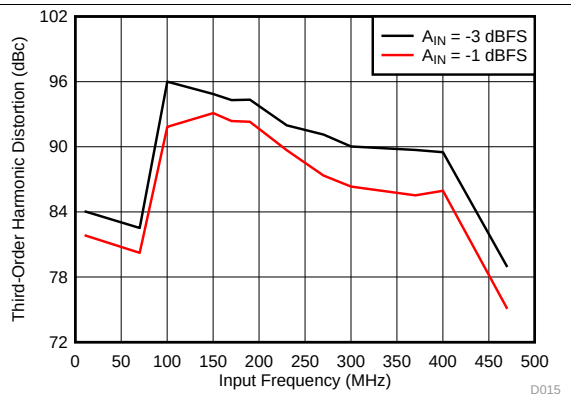



**图 16. HD3 vs Input Frequency**

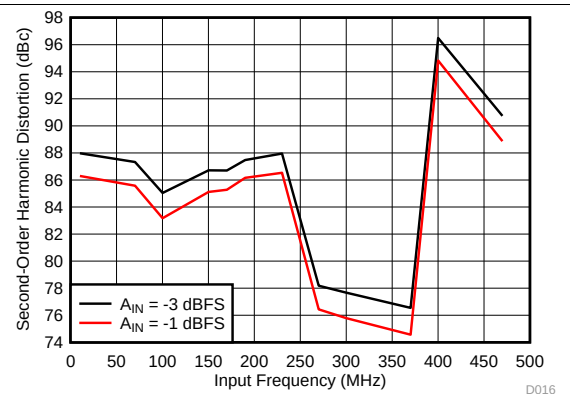



**图 17. HD2 vs Input Frequency**

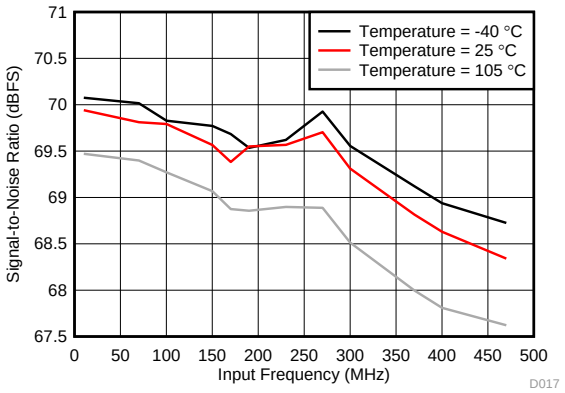



**图 18. SNR vs Input Frequency and Temperature**

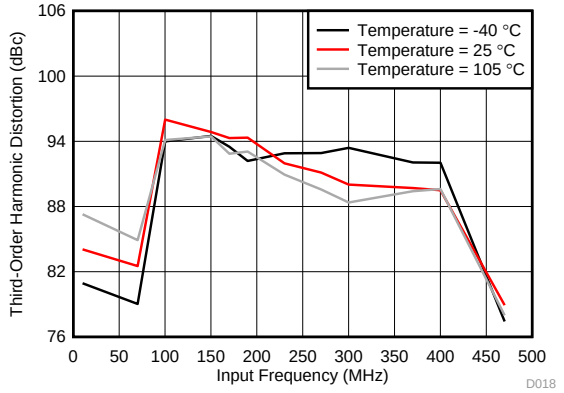



**图 19. HD3 vs Input Frequency and Temperature**


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## Typical Characteristics: DDC Bypass Mode (接下页)

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, device sampling frequency = 1 GSPS, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)

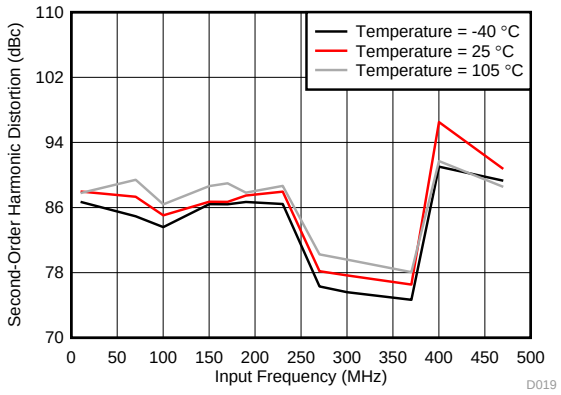



图 20. HD2 vs Input Frequency and Temperature

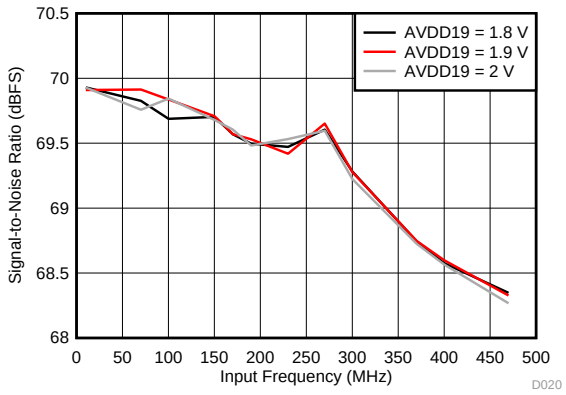



图 21. SNR vs Input Frequency and AVDD19 Supply

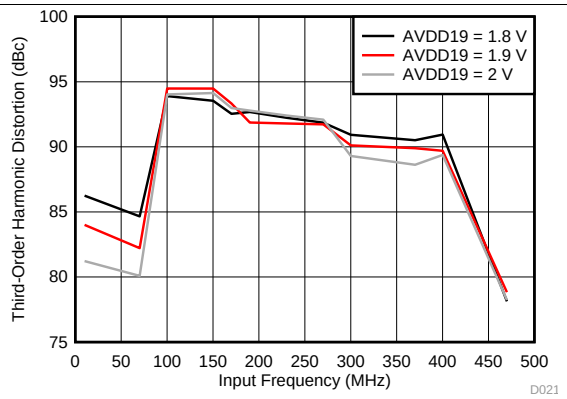



图 22. HD3 vs Input Frequency and AVDD19 Supply

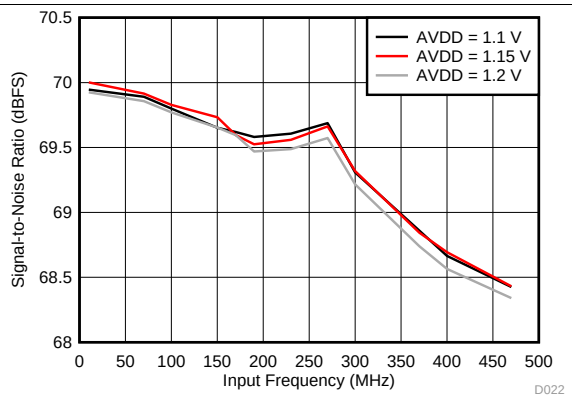



图 23. SNR vs Input Frequency and AVDD Supply

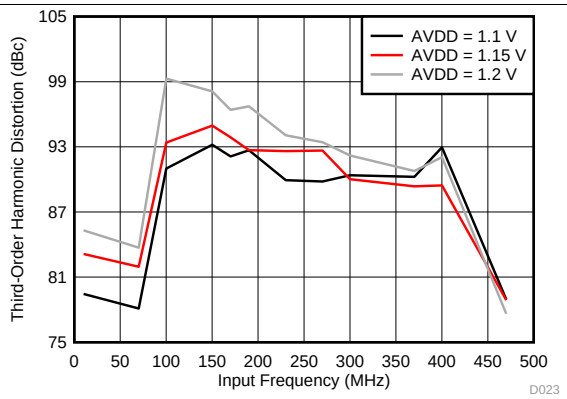



图 24. HD3 vs Input Frequency and AVDD Supply

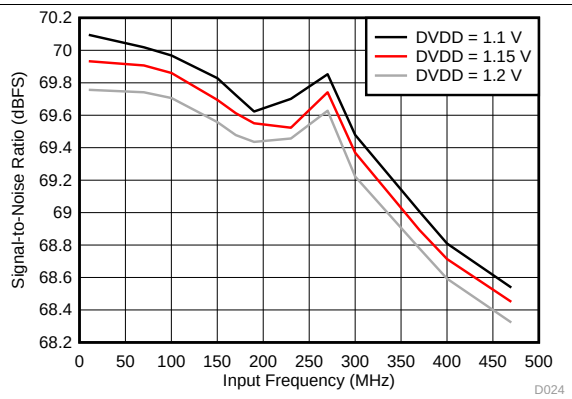



图 25. SNR vs Input Frequency and DVDD Supply

## Typical Characteristics: DDC Bypass Mode (接下页)

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, device sampling frequency = 1 GSPS, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)

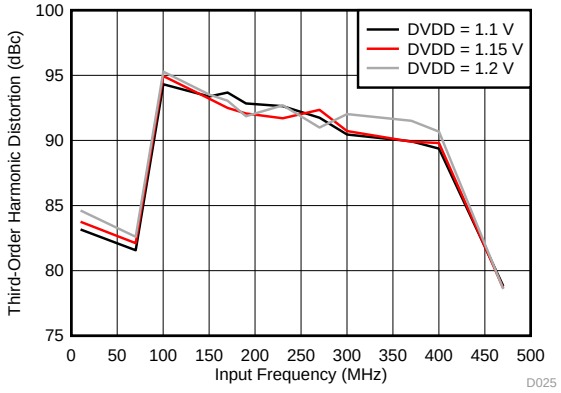
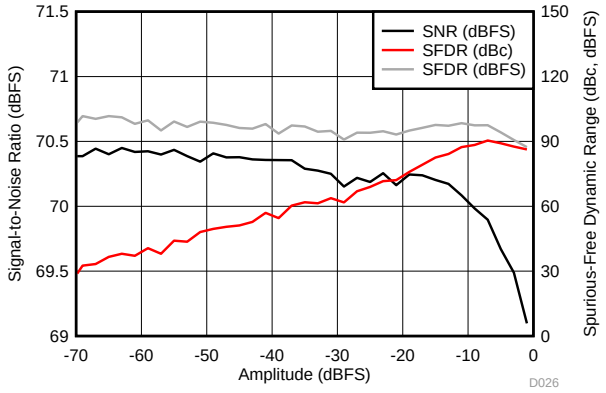
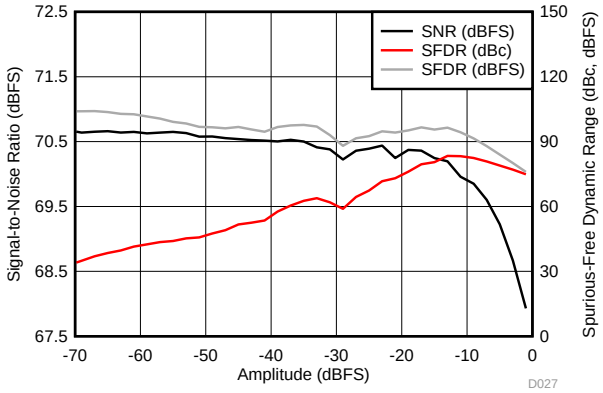



**图 26. HD3 vs Input Frequency and DVDD Supply**



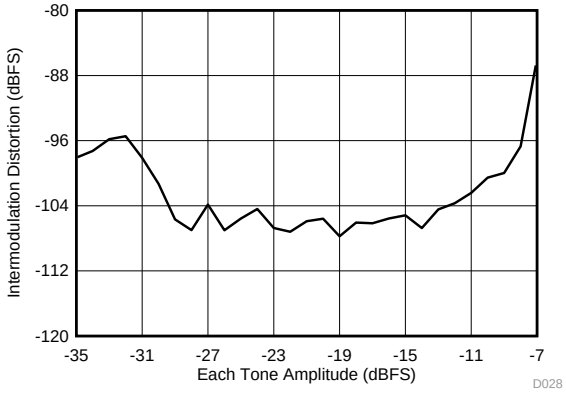

$f_{IN}$ = 190 MHz

**图 27. Performance vs Input Signal Amplitude**



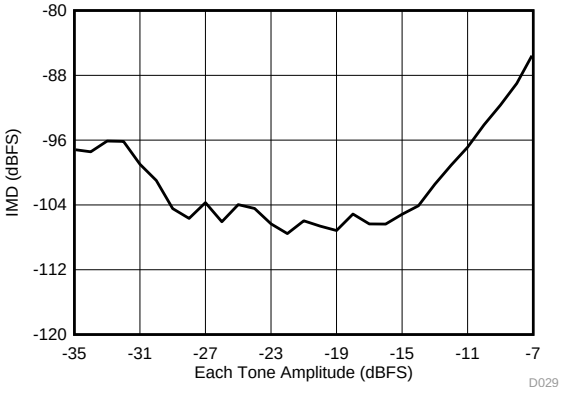

$f_{IN}$ = 370 MHz

**图 28. Performance vs Input Signal Amplitude**



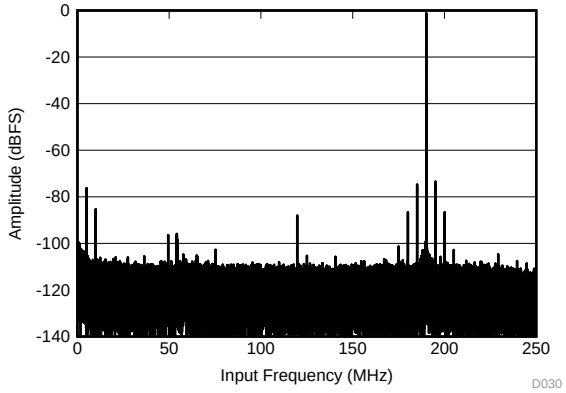

$f_{IN1}$ = 160 MHz, $f_{IN2}$ = 170 MHz

**图 29. IMD vs Input Amplitude**




$f_{IN1}$ = 340 MHz, $f_{IN2}$ = 350 MHz

**图 30. IMD vs Input Amplitude**



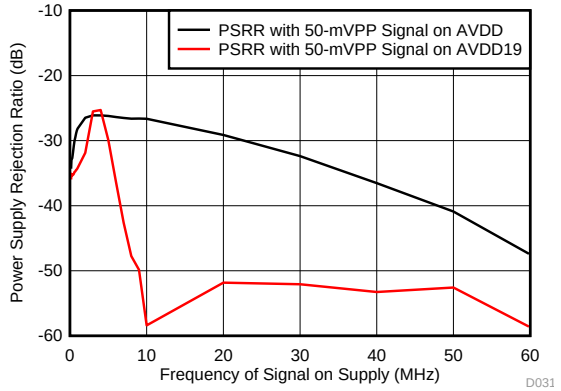

$f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS, $f_{Noise}$ = 5 MHz, $A_{Noise}$ = 50 $mV_{PP}$, SFDR = 73.5 dBFS

**图 31. Power-Supply Rejection Ratio FFT for 50-mV Noise on AVDD Supply**


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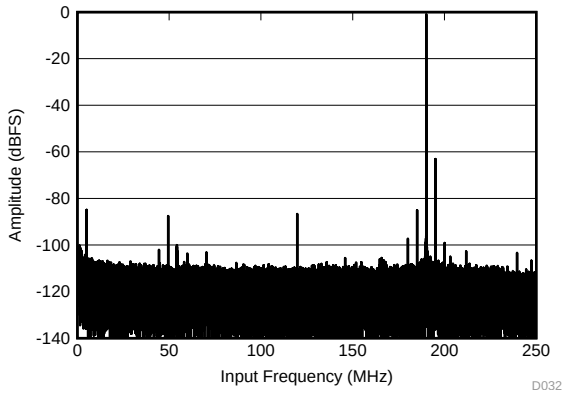
## Typical Characteristics: DDC Bypass Mode (接下页)

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, device sampling frequency = 1 GSPS, 50% clock duty cycle, output sample rate = 500 MSPS, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)



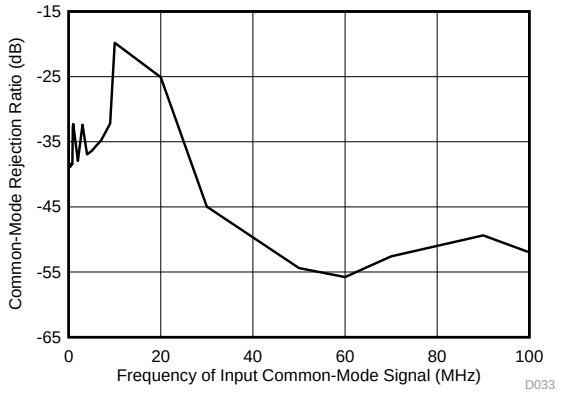

$f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS, $f_{Noise}$ = 5 MHz, $A_{Noise}$ = 50 $mV_{PP}$

**图 32. PSRR vs Power-Supply Noise Frequency**




$f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS, $f_{Noise}$ = 5 MHz, $A_{Noise}$ = 50 $mV_{PP}$, SFDR = 63.12 dBFS

**图 33. Common-Mode Rejection Ratio FFT**




$f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS, $f_{Noise}$ = 5 MHz, $A_{Noise}$ = 50 $mV_{PP}$

**图 34. CMRR vs Common-Mode Noise Frequency**

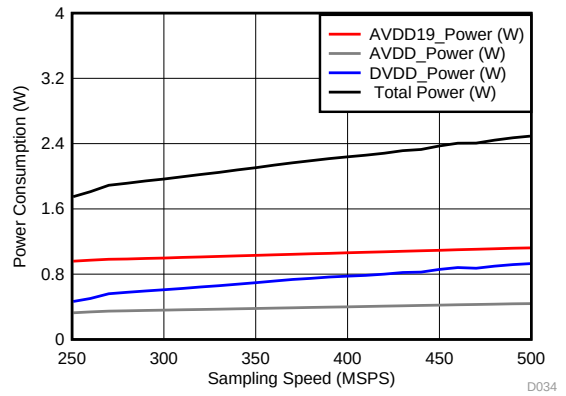
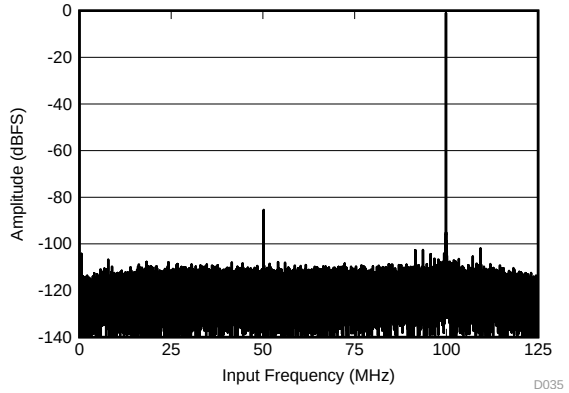



**图 35. Power Consumption vs Sampling Speed**

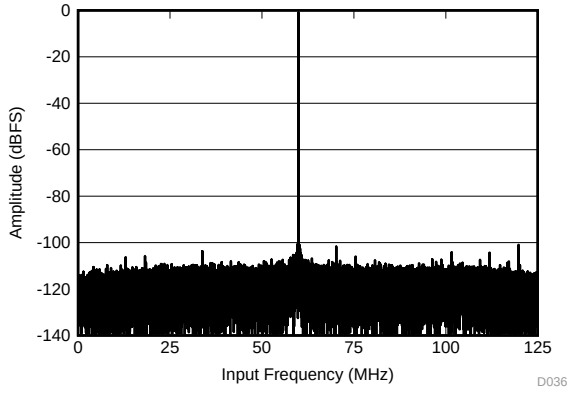
## 6.10 Typical Characteristics: Mode 2

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, device sampling frequency = 1 GSPS, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)



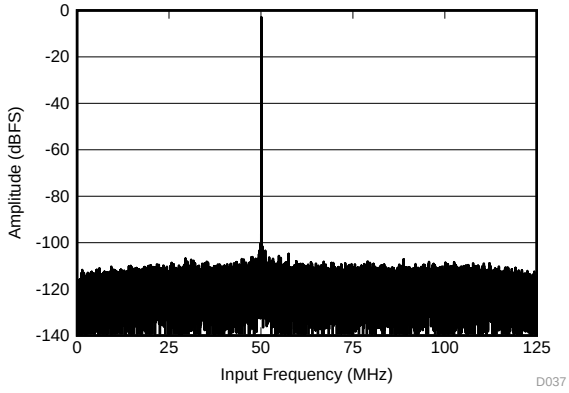

$f_{IN}$ = 150 MHz, $A_{IN}$= –1 dBFS, SNR = 72.85 dBFS, SFDR = 84.41 dBc, SFDR = 100.99 dBc (non 23)

**图 36. FFT for 150-MHz Input Signal**



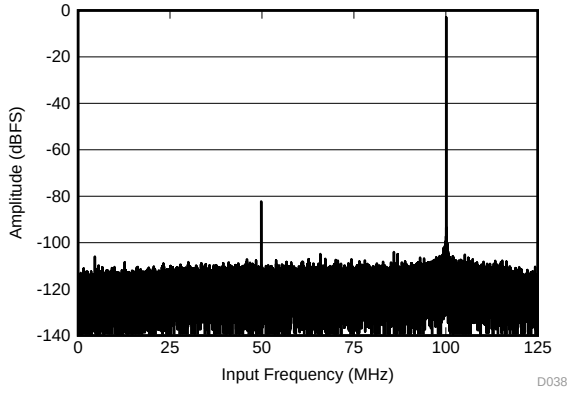

$f_{IN}$ = 190 MHz, $A_{IN}$= –1 dBFS, SNR = 72.37 dBFS, SFDR = 99.95 dBc, SFDR = 100.76 dBc (non 23)

**图 37. FFT for 190-MHz Input Signal**




$f_{IN}$ = 300 MHz, $A_{IN}$= –3 dBFS, SNR = 72.3 dBFS, SFDR = 100.31 dBc, SFDR = 100.75 dBc (non 23)

**图 38. FFT for 300-MHz Input Signal**



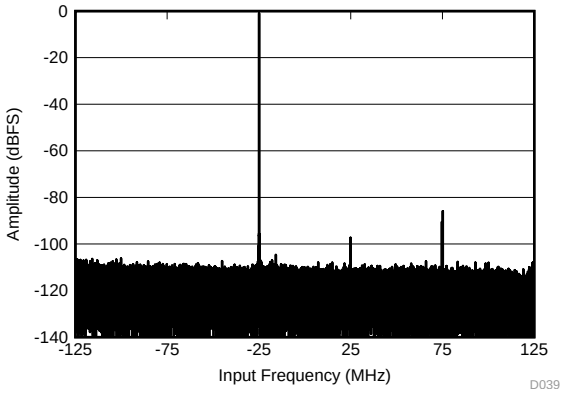

$f_{IN}$ = 350 MHz, $A_{IN}$= –3 dBFS, SNR = 72.02 dBFS, SFDR = 79.23 dBc, SFDR = 96.42 dBc (non 23)

**图 39. FFT for 350-MHz Input Signal**


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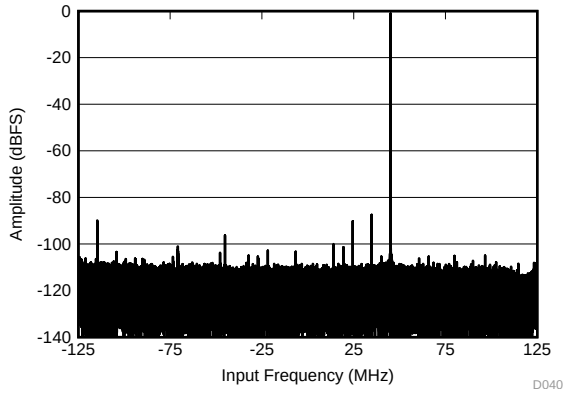
## 6.11 Typical Characteristics: Mode 0

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, device sampling frequency = 1 GSPS, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)



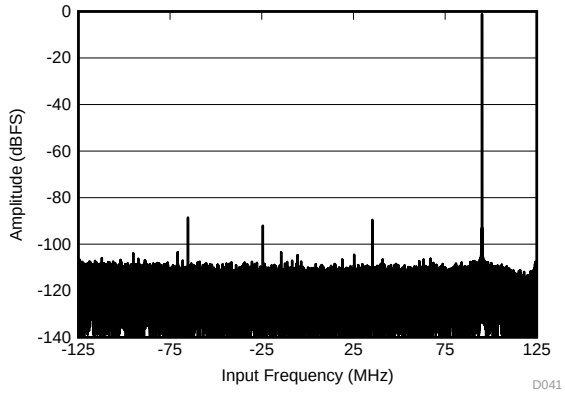

$f_{IN}$ = 100 MHz, $A_{IN}$= –1 dBFS, SNR = 70.16 dBFS, SFDR = 84.95 dBc, SFDR = 95.41 dBc (non 23)

**图 40. FFT for 100-MHz Input Signal**




$f_{IN}$ = 170 MHz, $A_{IN}$= –1 dBFS, SNR = 69.35 dBFS, SFDR = 86.46 dBc, SFDR = 89.27 dBc (non 23)

**图 41. FFT for 170-MHz Input Signal**

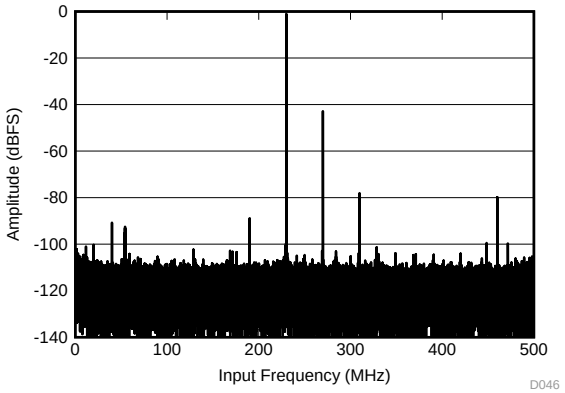



$f_{IN}$ = 220 MHz, $A_{IN}$= –1 dBFS, SNR = 69.27 dBFS, SFDR = 87.66 dBc, SFDR = 91.04 dBc (non 23)

**图 42. FFT for 220-MHz Input Signal**

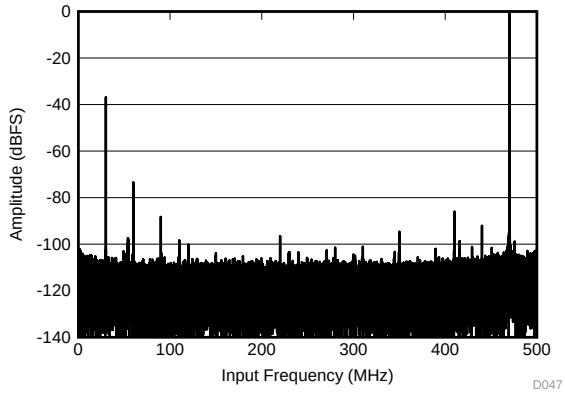
## 6.12 Typical Characteristics: Dual ADC Mode

typical values are at $T_A$ = 25°C, full temperature range is from $T_{MIN}$ = –40°C to $T_{MAX}$ = +100°C, device sampling frequency = 1 GSPS, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and $f_{IN}$ = 190 MHz (unless otherwise noted)




$f_{IN}$ = 230 MHz, $A_{IN}$= –1 dBFS, SNR = 68.11 dBFS, SFDR = 77.01 dBc, interleaving spur = –42.85 dBFS

**图 43. FFT for 230-MHz Input Signal**




$f_{IN}$ = 470 MHz, $A_{IN}$= –1 dBFS, SNR = 66.56 dBFS, SFDR = 72.32 dBc, interleaving spur = –36.96 dBFS

**图 44. FFT for 470-MHz Input Signal**

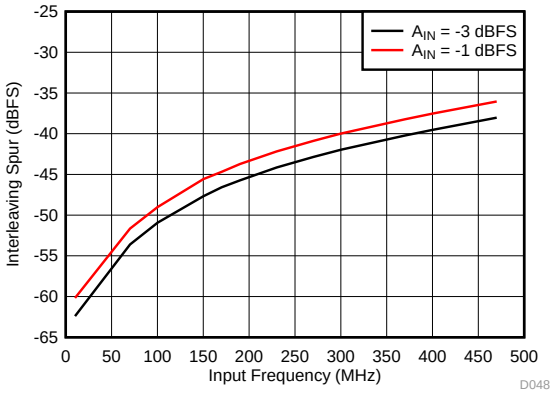



**图 45. Interleaving Spur vs Input Frequency**


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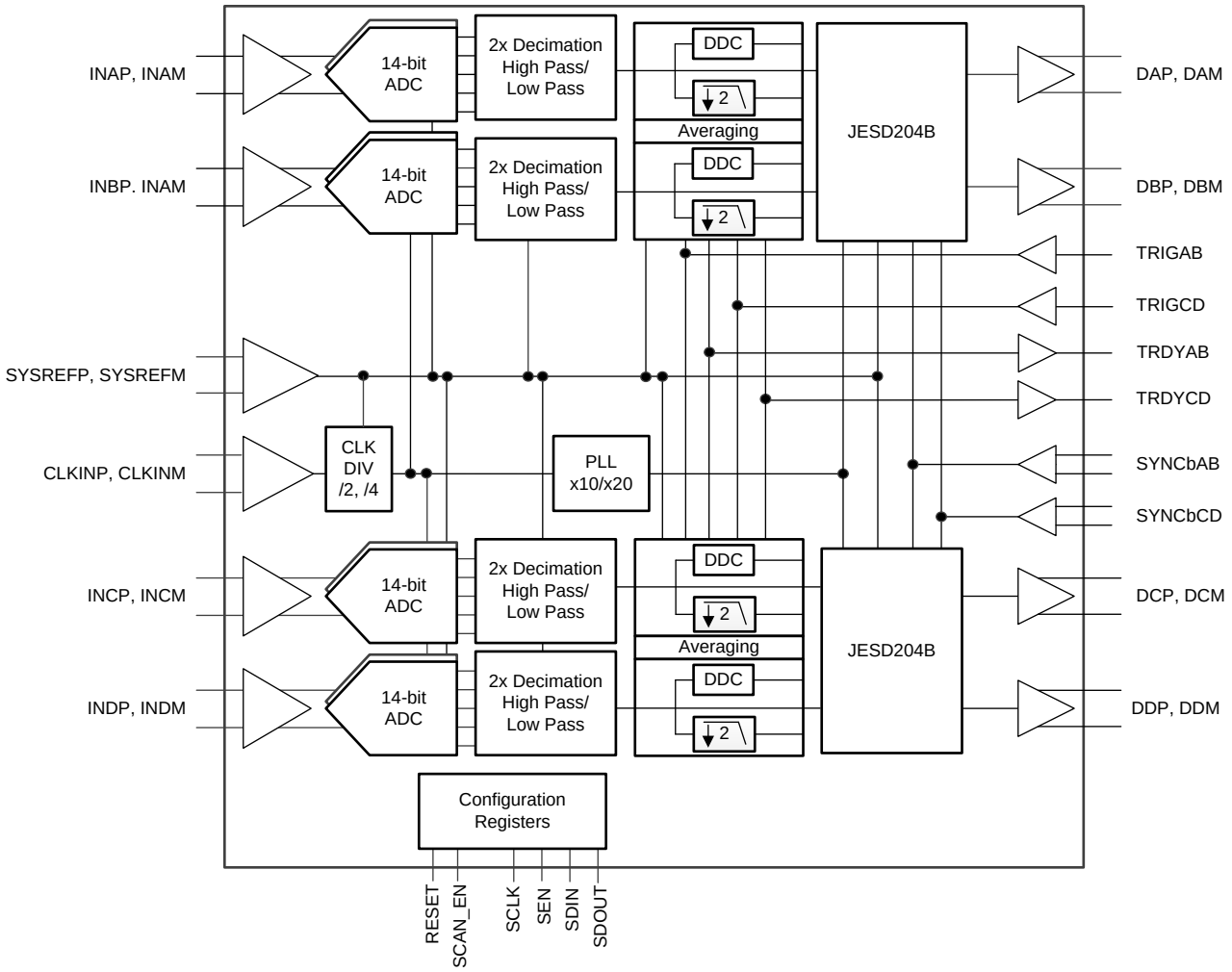
# 7 Detailed Description

## 7.1 Overview

The ADS54J64 is a quad-channel device with a complex digital down-converter (DDC) and digital decimation to allow flexible signal processing to suit different usage cases. Each channel is composed of two interleaved analog-to-digital converters (ADCs) sampling at half the input clock rate. The 2x interleaved data are decimated by 2 to provide a processing gain of 3 dB. The decimation filter has a programmable option to be configured as low pass (default) or high pass. In default mode, the device operates in DDC mode 0, where the input is mixed with a constant frequency of $–f_S$ / 4 and transmitted as complex IQ. In DDC bypass mode (mode 8), the DDC is bypassed and the 2x decimated data are available on the JESD output. The different operational modes of the ADS54J64 are listed in 表 1.

The ADS54J64 can also be operated in a dual-channel interleaved mode (dual mode), in which two channels are averaged and the 2x interleaved and averaged data are available directly at the JESD output.

## 7.2 Functional Block Diagram




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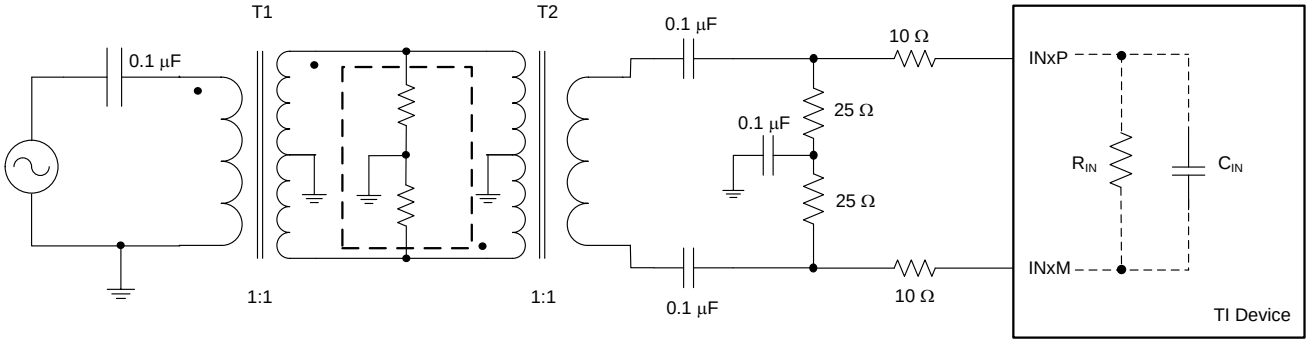
## 7.3 Feature Description

### 7.3.1 Analog Inputs

The ADS54J64 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high-impedance input across a very wide frequency range to the external driving source that enables great flexibility in the external analog filter design as well as excellent 50-Ω matching for RF applications. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit, resulting in a more constant SFDR performance across input frequencies. The common-mode voltage of the signal inputs is internally biased to 1.3 V using 2-kΩ resistors to allow for ac-coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between ($V_{CM}$ + 0.275 V) and ($V_{CM}$ – 0.275 V), resulting in a 1.1-$V_{PP}$ (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 1000 MHz.

### 7.3.2 Recommended Input Circuit

In order to achieve optimum ac performance, the following circuitry (shown in 图 46) is recommended at the analog inputs.

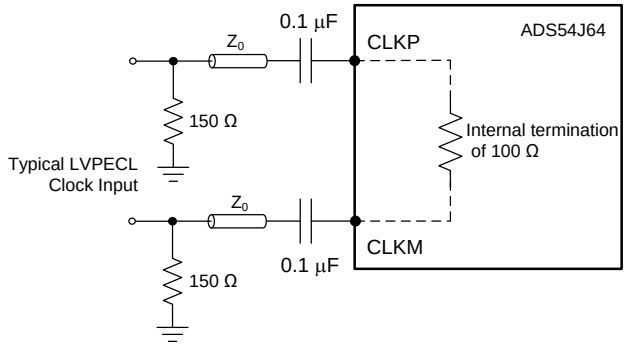



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**图 46. Analog Input Driving Circuit**

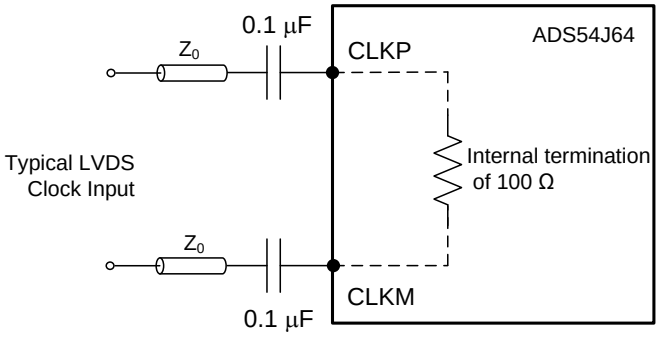
### 7.3.3 Clock Input

The clock inputs of the ADS54J64 supports LVDS and LVPECL standards. The CLKP, CLKM inputs have an internal termination of 100 Ω. The clock inputs must be ac-coupled, as shown in 图 47 and 图 48, because the input pins are self-biased to a common-mode voltage of 0.7 V.




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**图 47. LVPECL Clock Driving Circuit**




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**图 48. LVDS Clock Driving Circuit**


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## 7.4 Device Functional Modes

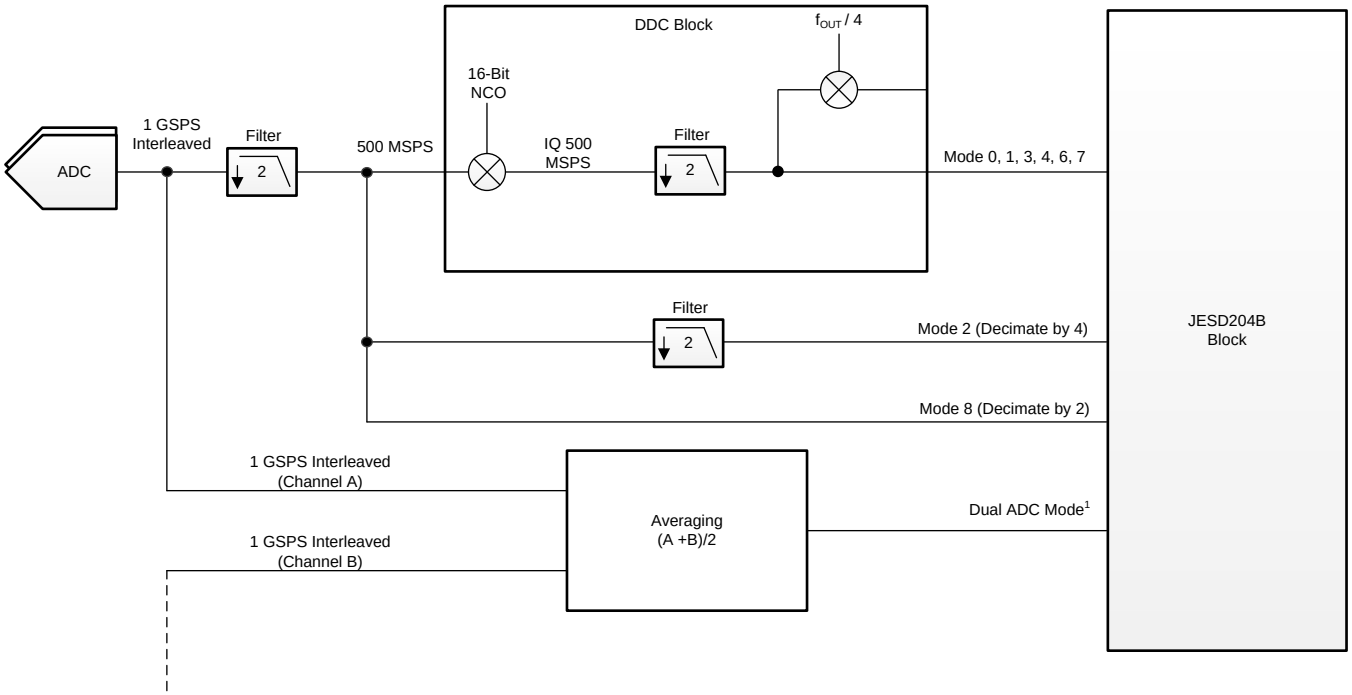
### 7.4.1 Digital Functions

图 49 shows the various operational modes available in the ADS54J64. In quad mode, the maximum output rate is half the sampling rate. The 2x interleaved data are filtered using a half-band filter (HBF) that can be configured as a low-pass or high-pass filter using register writes. In dual mode, the device can be operated at a full sampling rate with 2x interleaving and averaging of two channels.

Quad mode supports a maximum complex and a real bandwidth of 200 MHz. The HBF output can be brought directly on the JESD lines at half rate. The complex data are obtained through a digital down-converter (DDC) that is comprised of a 16-bit numerically controlled oscillator (NCO) and a 100-MHz or 200-MHz filter. The DDC also has a real output mode where the data are decimated by 2 and mixed to $f_{OUT}$ / 4 to support a bandwidth of 100 MHz. In addition to the DDC modes, the HBF output can be decimated by 2 to obtain an overall decimation by 4 on the 2x interleaved data.

Dual mode supports a maximum sampling rate of 1 GSPS. The 2x interleaved data from channel A and channel B (and likewise channels C and D) can be averaged and given on the JESD lanes.

表 1 lists all modes of operation with the maximum bandwidth provided at a sample rate of 491.52 MSPS and 368.64 MSPS.




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(1) 1-GSPS data are transmitted using two JESD lanes.

**图 49. ADS54J64 Channel Operating Modes**

## Device Functional Modes (接下页)

**表 1. ADS54J64 Operating Modes**

| OPERATING MODE | DESCRIPTION | 1ST-STAGE DECIMATION | DIGITAL MIXER | 2ND-STAGE DECIMATION | BANDWIDTH AT 491.52 MSPS | BANDWIDTH AT 368.64 MSPS | OUTPUT MIXER | OUTPUT FORMAT | MAX OUTPUT RATE |
|---|---|---|---|---|---|---|---|---|---|
| 0 | Decimation | 2 | $\pm f_S$ / 4 | 2 | 200 MHz | 150 MHz | — | Complex | 250 MSPS |
| 1 | | 2 | 16-bit NCO | 2 | 200 MHz | 150 MHz | — | Complex | 250 MSPS |
| 2 | | 2 | — | 2 | 100 MHz (LP, LP or HP, HP), 75 MHz (HP, LP or LP, HP) | 75 MHz, 56.25 MHz | — | Real | 250 MSPS |
| 3 | | 2 | 16-bit NCO | Bypass | 200 MHz | 150 MHz | $f_{OUT}$ / 4 | Real | 500 MSPS |
| 4 | | 2 | 16-bit NCO | 2 | 100 MHz | 75 MHz | $f_{OUT}$ / 4 | Real | 250 MSPS |
| 5 | | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 6 | | 2 | 16-bit NCO | 4 | 100 MHz | 75 MHz | — | Complex | 125 MSPS |
| 7 | | 2 | 16-bit NCO | 2 | 100 MHz | 75 MHz | $f_{OUT}$ / 4 | Real with zero insertion | 500 MSPS |
| 8 | DDC bypass mode | 2 | — | — | 223 MHz | 167 MHz | — | Real | 500 MSPS |
| 8 | Dual ADC mode | — | — | — | — | — | — | — | 1000 MSPS |

### *7.4.1.1 Numerically Controlled Oscillators (NCOs) and Mixers*

The ADS54J64 is equipped with a complex numerically-controlled oscillator. The oscillator generates a complex exponential sequence: $x[n] = e^{j\omega n}$. The frequency ($\omega$) is specified by the 16-bit register setting. The complex exponential sequence is multiplied by the real input from the ADC to mix the desired carrier down to 0 Hz.

The NCO frequency setting is set by the 16-bit register value, NCO_FREQ[n]:

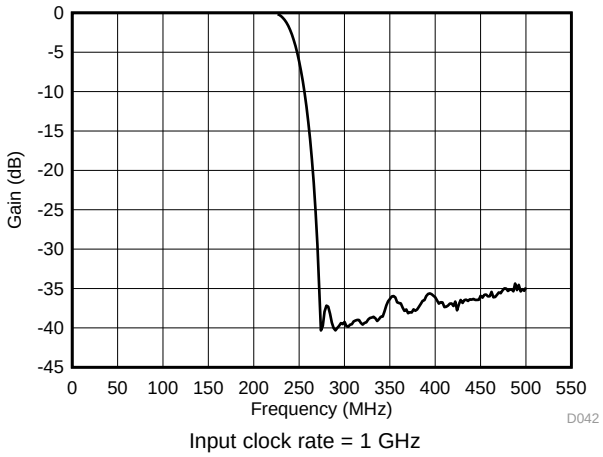
$$f_{NCO} = \frac{\text{NCO Frequency [n]} \times f_S}{2^{16}} \quad (1)$$

### *7.4.1.2 Decimation Filter*

The ADS54J64 has two decimation filters (decimate-by-2) in the data path. The first stage of the decimation filter is non-programmable and is used in all functional modes. The second stage of decimation, available in DDC mode 2 and 6, can be used to obtain noise and linearity improvement for low bandwidth applications.

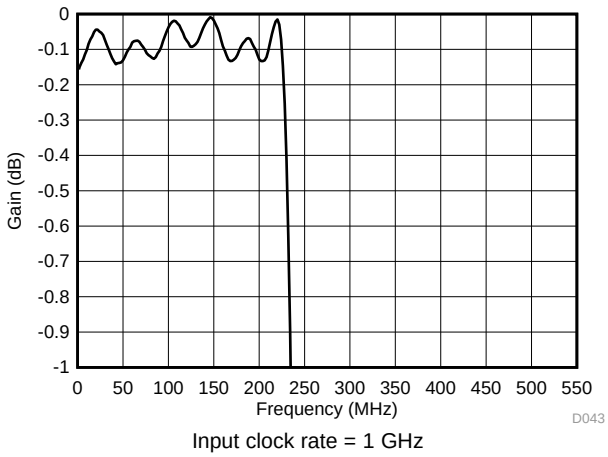
#### 7.4.1.2.1 Stage-1 Filter

The first-stage filter is used for decimation of the 2x interleaved data from $f_{CLK}$ to $f_{CLK}$ / 2. 图 50 and 图 51 show the frequency response and pass-band ripple of the first-stage decimation filter, respectively.




Input clock rate = 1 GHz

**图 50. Decimation Filter Response vs Frequency**




Input clock rate = 1 GHz

**图 51. Decimation Filter Pass-Band Ripple vs Frequency**


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#### 7.4.1.2.2 Stage-2 Filter

The second-stage filter is used for decimating the data from a sample rate of $f_{CLK}$ / 2 to $f_{CLK}$ / 4. 图 52 and 图 53 show the frequency response and pass-band ripple of the second-stage filter, respectively.

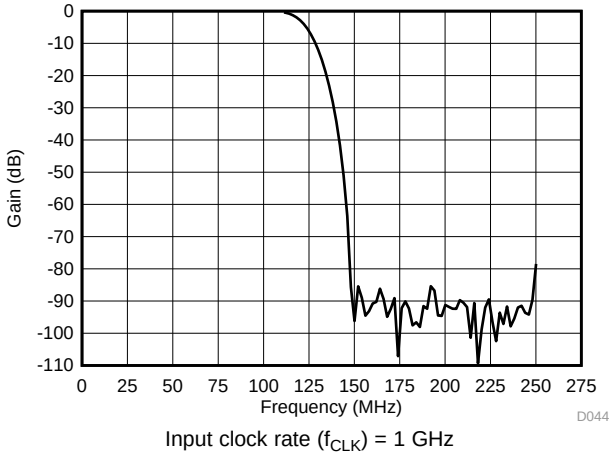



图 52. Decimation Filter Response vs Frequency

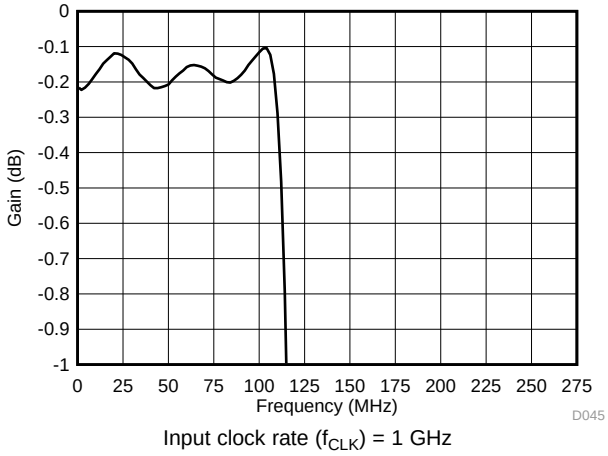



图 53. Decimation Filter Pass-Band Ripple vs Frequency

### *7.4.1.3 Mode 0: Decimate-by-4 With IQ Outputs and $f_S$ / 4 Mixer*

In mode 0, the DDC block includes a fixed frequency ±$f_S$ / 4 complex digital mixer preceding the second-stage decimation filters. 图 54 shows that the IQ pass band is approximately ±100 MHz centered at $f_S$ / 8 or 3$f_S$ / 8.

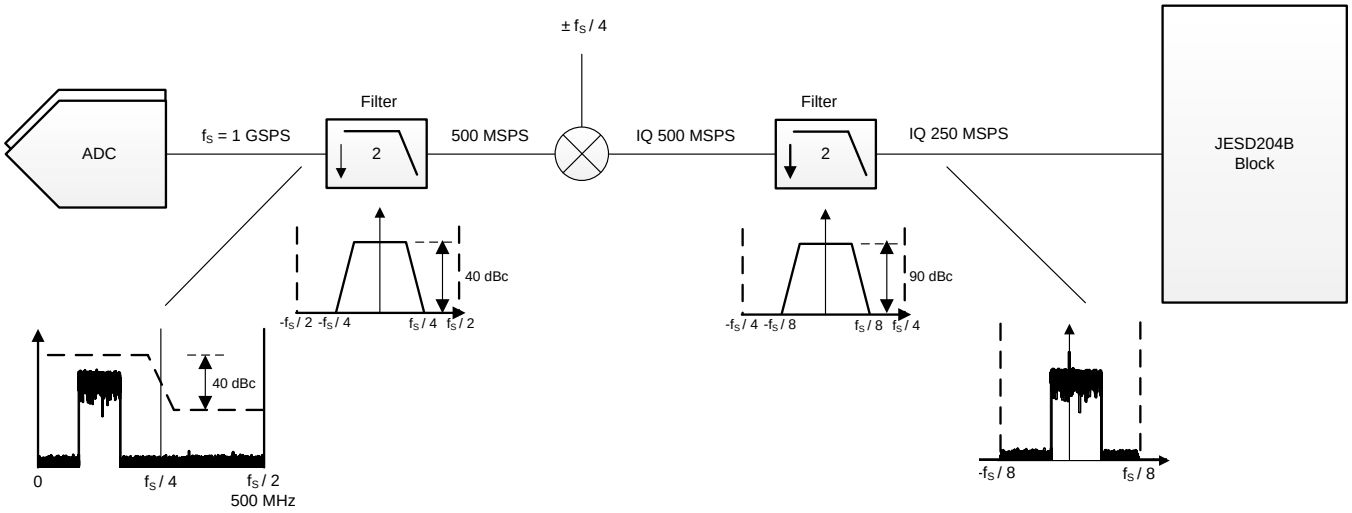



图 54. Operating Mode 0

### 7.4.1.4 Mode 1: Decimate-by-4 With IQ Outputs and 16-Bit NCO

In mode 1, the DDC block includes a 16-bit frequency resolution complex digital mixer, as shown in 图 55, preceding the second-stage decimation filters.

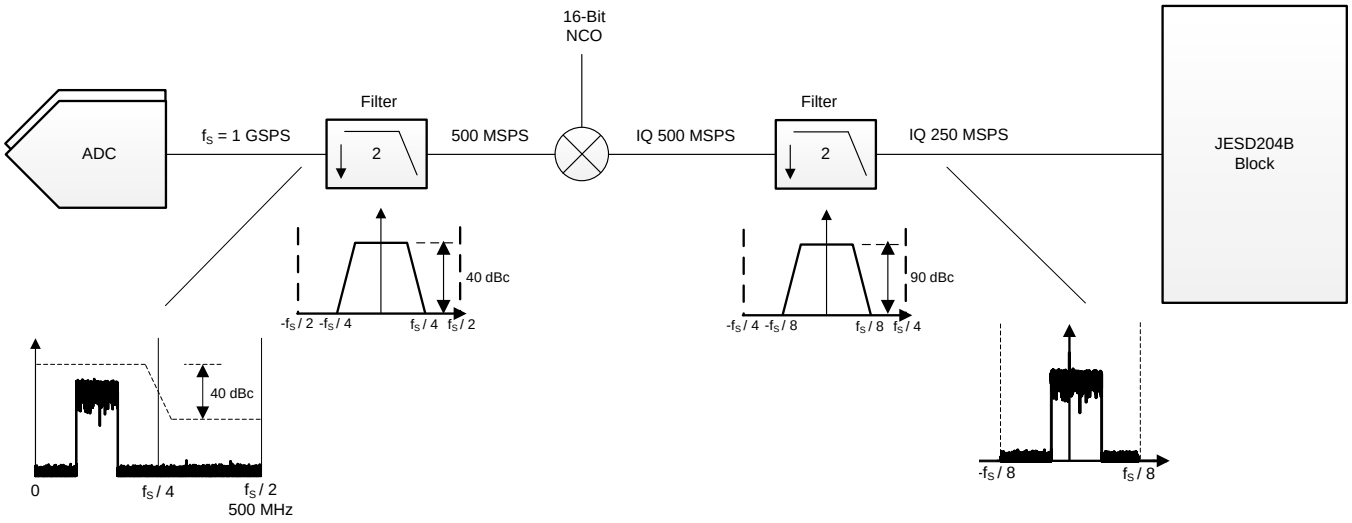



**图 55. Operating Mode 1**

### 7.4.1.5 Mode 2: Decimate-by-4 With Real Output

In mode 2, the DDC block cascades two decimate-by-2 filters. Each filter can be configured as low pass (LP) or high pass (HP), as shown in 表 2, to allow down conversion of different frequency ranges. 图 56 shows that the LP, HP and HP, LP output spectra are inverted.

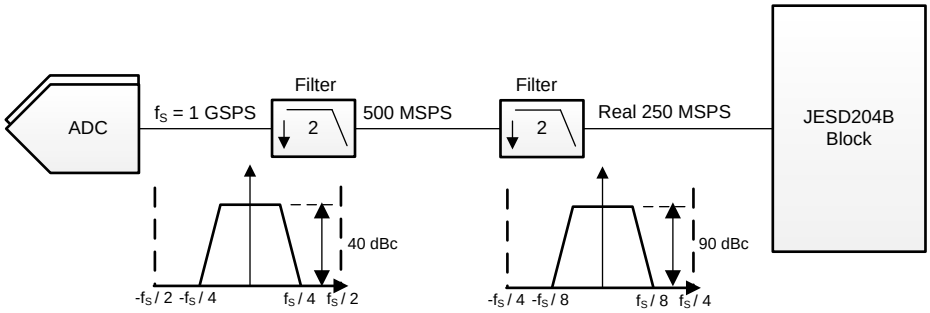



**图 56. Operating in Mode 2**

**表 2. ADS54J64 Operating Mode 2, Down-Converted Frequency Ranges**

| 1ST-STAGE FILTER | 2ND-STAGE FILTER | FREQUENCY RANGE WITH CLOCK RATE OF 983.04 MHz | BANDWIDTH WITH CLOCK RATE OF 983.04 MHz | FREQUENCY RANGE WITH CLOCK RATE OF 737.28 MHz | BANDWIDTH WITH CLOCK RATE OF 737.28 MHz |
|---|---|---|---|---|---|
| LP | LP | 0 MHz–100 MHz | 100 MHz | 0 MHz–75 MHz | 75 MHz |
| LP | HP | 150 MHz–223 MHz | 73 MHz | 112.5 MHz–167.25 MHz | 54.75 MHz |
| HP | LP | 268.52 MHz–341.52 MHz | 73 MHz | 201.39 MHz–256.14 MHz | 54.75 MHz |
| HP | HP | 391.52 MHz–491.52 MHz | 100 MHz | 293.64 MHz–368.64 MHz | 75 MHz |


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#### 7.4.1.6 Mode 3: Decimate-by-2 Real Output With Frequency Shift

In mode 3, the DDC block includes a 16-bit complex NCO digital mixer followed by a $f_S$ / 4 mixer with a real output to center the band at $f_S$ / 4. As shown in 图 57, the NCO must be set to a value different from ±$f_S$ / 4, or else the samples are zeroed.

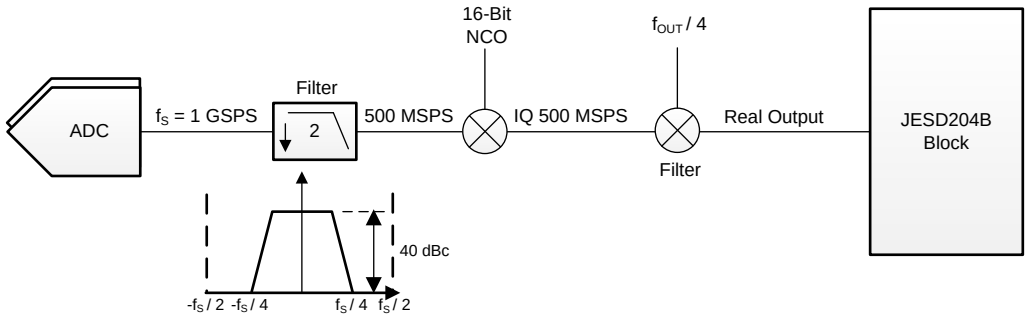



**图 57. Operating Mode 3**

#### 7.4.1.7 Mode 4: Decimate-by-4 With Real Output

In mode 4, the DDC block includes a 16-bit complex NCO digital mixer preceding the second-stage decimation filter. As shown in 图 58, the signal is then mixed with $f_{OUT}$ / 4 to generate a real output. The bandwidth available in this mode is 100 MHz.

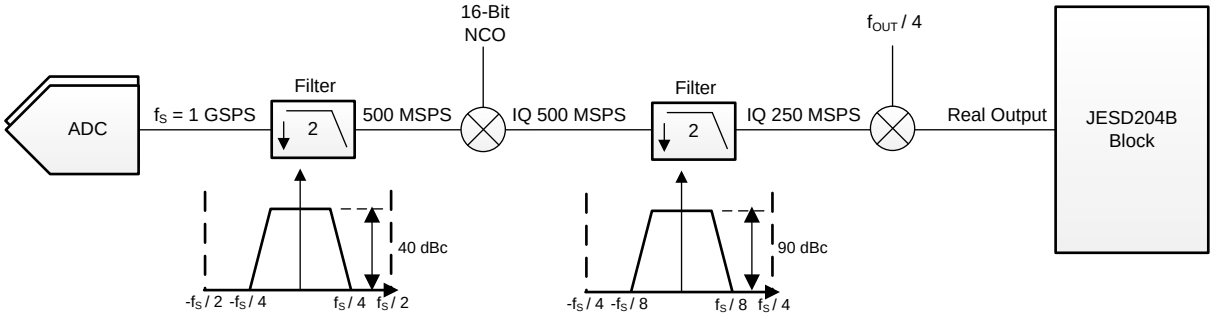



**图 58. Operating Mode 4**

### 7.4.1.8 Mode 6: Decimate-by-4 With IQ Outputs for Up to 110 MHz of IQ Bandwidth

In mode 6, the DDC block shown in 图 59 includes a 16-bit complex NCO digital mixer preceding a second-stage filter with a decimate-by-4 complex, generating a complex output at $f_S$ / 8.

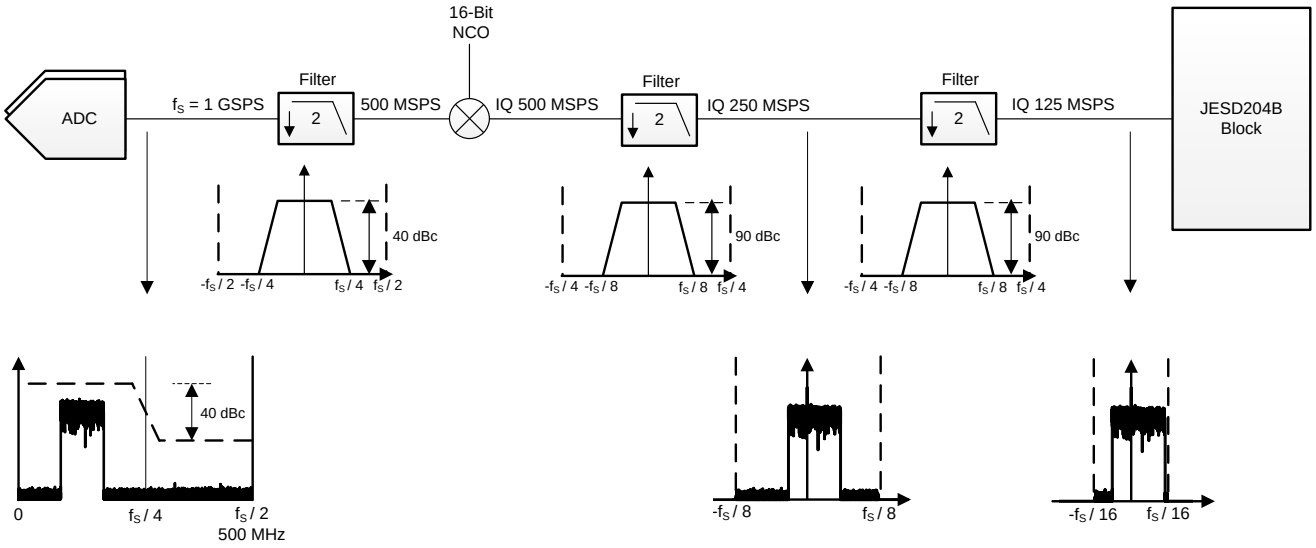



**图 59. Operating Mode 6**

### 7.4.1.9 Mode 7: Decimate-by-4 With Real Output and Zero Stuffing

In mode 7, the DDC block includes a 16-bit complex NCO digital mixer preceding the second-stage decimation filter. The signal is then mixed with $f_{OUT}$ / 4, as shown in 图 60, to generate a real output that is then doubled in sample rate by zero-stuffing every other sample. The bandwidth available in this mode is 100 MHz.

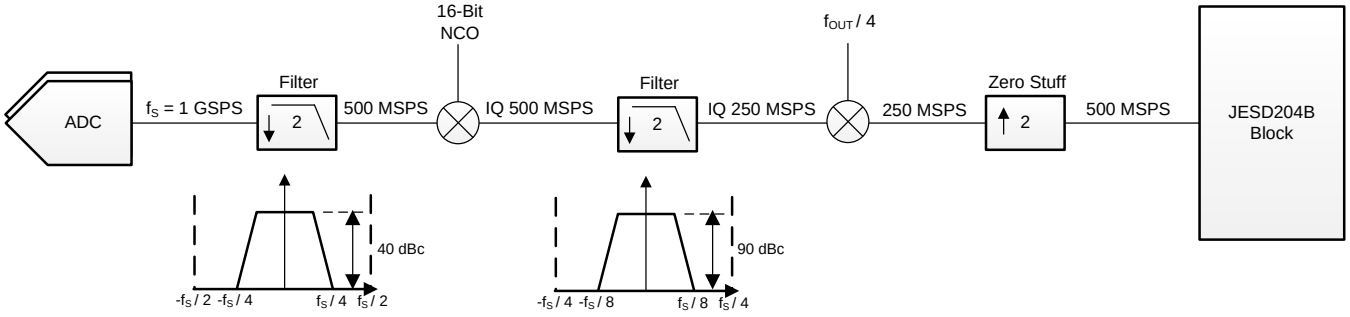
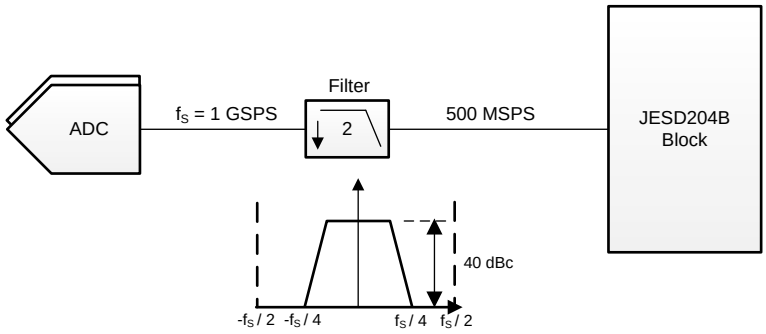



**图 60. Operating Mode 7**


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### 7.4.1.10 Mode 8: DDC Bypass Mode

In mode 8, the DDC block is bypassed as shown in 图 61 and the 2x decimated data are available on the JESD output. The decimation filter can be configured to be high pass or low pass using an SPI register bit. The stop-band attenuation is approximately 40 dB and the available bandwidth is 225 MHz. The decimation filter response is illustrated in 图 50 and 图 51.

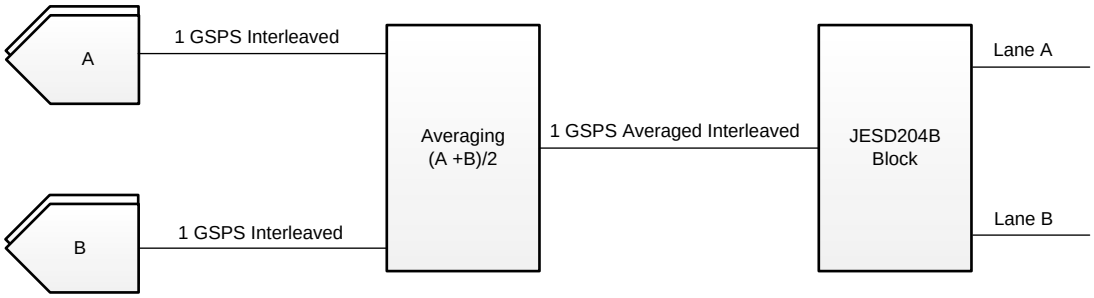



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**图 61. Operating Mode 8**

### 7.4.1.11 Averaging Mode

In dual ADC mode, two channels (channels A, B and C, D) are averaged and given out as a single output. As a result, the device operates in a dual-channel mode with 2x interleaved sample rate. For a 1-GSPS input clock, the averaged output at 1 GSPS is available on two JESD lanes, each operating at 10 Gbps. 图 62 shows the device supporting an averaging of channels A and B. An identical averaging path is available for channels C and D. Configure the device in mode 8 before enabling dual ADC mode through SPI register writes.




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**图 62. Averaging Mode for Channels A and B (C and D Averaging is Identical)**

### 7.4.1.12 Overrange Indication

The ADS54J64 provides a fast overrange indication that can be presented in the digital output data stream via SPI configuration. When the FOVR indication is embedded in the output data stream as shown in 图 63, this indication replaces the LSB (D0) of the 16 bits going to the 8b, 10b encode.

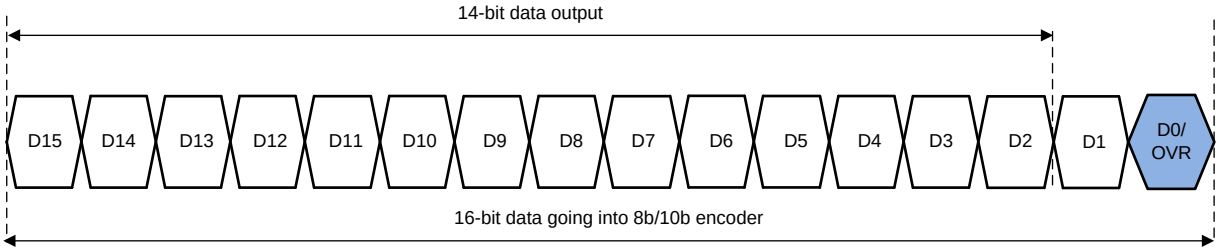



**图 63. FOVR Timing Diagram**

The fast overrange feature of the ADS54J64 is configured using an upper (FOVR Hi) and a lower (FOVR Lo) 8-bit threshold that are compared against the partial ADC output of the initial pipeline stages. 图 64 shows the FOVR high and FOVR low thresholds.

The two thresholds are configured via the SPI register where a setting of 136 maps to the maximum ADC code for a high FOVR, and a setting of 8 maps to the minimum ADC code for a low FOVR.

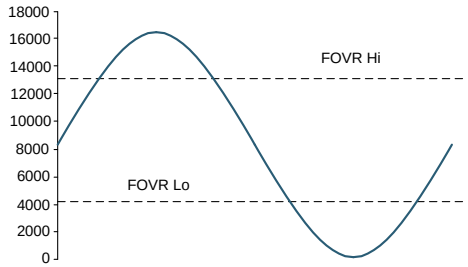



**图 64. FOVR High and FOVR Low Thresholds**

公式 2 calculates the FOVR threshold from a full-scale input based on the ADC code:

$$\text{FOVR (dBFS)} = 20\log\left|\frac{\text{FOVR High or FOVR Low} - 72}{64}\right| \quad (2)$$

Therefore, a threshold of –0.5 dBFS from full-scale can be set with:

- FOVR high = 132 (27h, 84h)
- FOVR low = 12 (28h, 0Ch)


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## 7.5 Programming

### 7.5.1 JESD204B Interface

The ADS54J64 supports device subclass 1 with a maximum output data rate of 10 Gbps for each serial transmitter.

图 65 shows that an external SYSREF signal is used to align all internal clock phases and the local multi-frame clock to a specific sampling clock edge. A common SYSREF signal allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty. The ADS54J64 supports single (for all four JESD links) or dual (for channels A, B and C, D) SYNCb inputs and can be configured via the SPI.

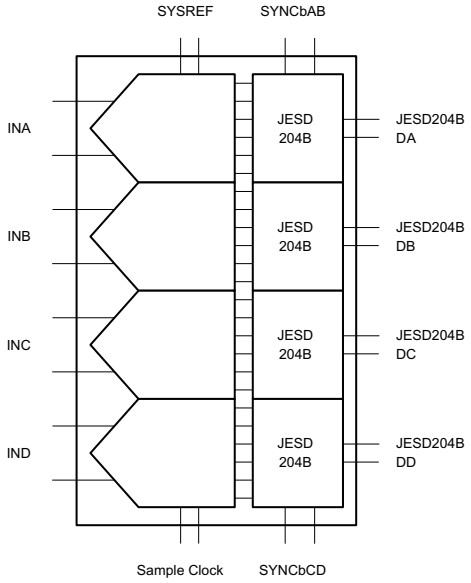



**图 65. JESD204B Transmitter Block**

Depending on the ADC sampling rate, the JESD204B output interface can be operated with one lane per channel. The JESD204B setup and configuration of the frame assembly parameters is handled via the SPI interface.

The JESD204B transmitter block shown in 图 66 consists of the transport layer, the data scrambler, and the link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format and manages if the ADC output data or test patterns are being transmitted. The link layer performs the 8b, 10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer can be scrambled.

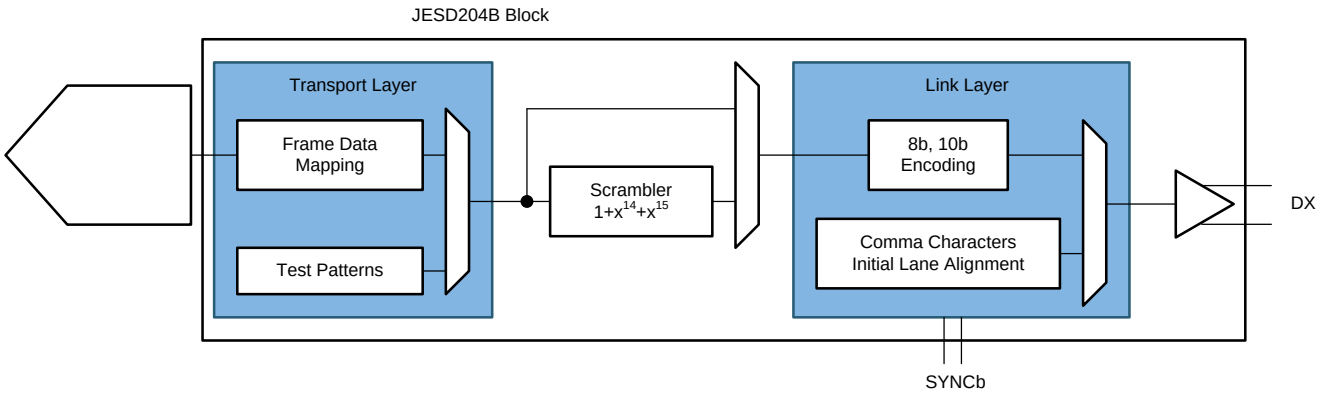



**图 66. JESD Interface Block Diagram**

## Programming (接下页)

### 7.5.2 JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started by the receiving device by deasserting the SYNCb signal. When a logic low is detected on the SYNC input pins, as shown in 图 67, the ADS54J64 starts transmitting comma (K28.5) characters to establish code group synchronization.

When synchronization is complete, the receiving device reasserts the SYNCb signal and the ADS54J64 starts the initial lane alignment sequence with the next local multi-frame clock boundary. The ADS54J64 transmits four multi-frames, each containing K frames (K is SPI programmable). Each of the multi-frames contains the frame start and end symbols and the second multi-frame also contains the JESD204 link configuration data.

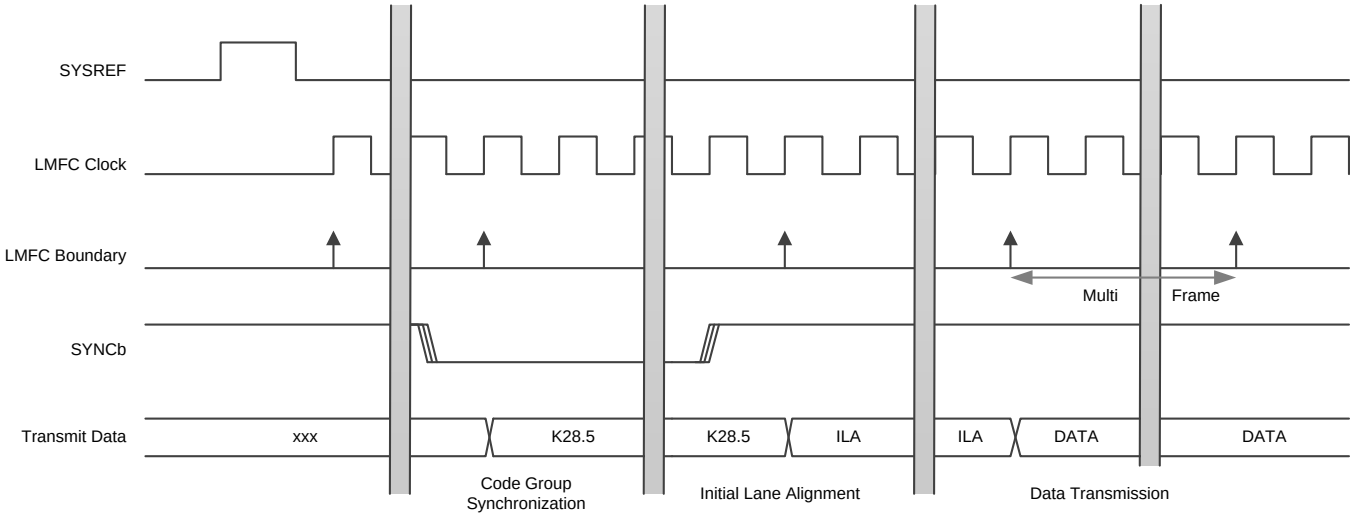



**图 67. ILA Sequence**


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## Programming (接下页)

### 7.5.3 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per link
- M is the number of converters per device
- F is the number of octets per frame clock period
- S is the number of samples per frame

表 3 lists the available JESD204B formats and valid ranges for the ADS54J64. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency.

**表 3. Available JESD204B Formats and Valid Ranges for the ADS54J64**

| L | M | F | S | OPERATING MODE | DIGITAL MODE | OUTPUT FORMAT | MAX ADC OUTPUT RATE (MSPS) | MAX $f_{SerDes}$ (Gbps) | JESD PLL REGISTER CONFIGURATION |
|---|---|---|---|---|---|---|---|---|---|
| 4 | 8 | 4 | 1 | 0, 1 | 2x decimation | Complex | 250 | 10.0 | — |
| 4 | 4 | 2 | 1 | 2, 4 | 2x decimation | Real | 250 | 5.0 | CTRL_SER_MODE = 1, SerDes_MODE = 1 |
| 2 | 4 | 4 | 1 | 2, 4 | 2x decimation | Real | 250 | 10.0 | — |
| 4 | 8 | 4 | 1 | 6 | 4x decimation | Complex | 125 | 5.0 | — |
| 2 | 8 | 8 | 1 | 6 | 4x decimation | Complex | 125 | 10.0 | CTRL_SER_MODE = 1, SerDes_MODE = 3 |
| 4 | 4 | 2 | 1 | 7 | 2x decimation with 0-pad | Real | 500 | 10.0 | — |
| 4 | 4 | 2 | 1 | 3, 8 | DDC bypass | Real | 500 | 10.0 | — |
| 4 | 2 | 1 | 1 | 8 | DDC bypass dual ADC | Real | 1000 | 10.0 | — |

表 4, 表 5, and 表 6 show the detailed frame assembly for various LMFS settings.

**表 4. Detailed Frame Assembly for Four-Lane Modes (Modes 0, 1, 3, 6, 7, and 8)**

| OUTPUT LANE | LMFS = 4841 | | | | LMFS = 4421 | | | | LMFS = 4421 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DA | $AI_0$[15:8] | $AI_0$[7:0] | $AQ_0$[15:8] | AQ0[7:0] | $A_0$[15:8] | $A_0$[7:0] | $A_1$[15:8] | $A_1$[7:0] | $A_0$[15:8] | $A_0$[7:0] | 0000 0000 | 0000 0000 |
| DB | $BI_0$[15:8] | $BI_0$[7:0] | $BQ_0$[15:8] | $BQ_0$[7:0] | $B_0$[15:8] | $B_0$[7:0] | $B_1$[15:8] | $B_1$[7:0] | $B_0$[15:8] | $B_0$[7:0] | 0000 0000 | 0000 0000 |
| DC | $CI_0$[15:8] | $CI_0$[7:0] | $CQ_0$[15:8] | $CQ_0$[7:0] | $C_0$[15:8] | $C_0$[7:0] | $C_1$[15:8] | $C_1$[7:0] | $C_0$[15:8] | $C_0$[7:0] | 0000 0000 | 0000 0000 |
| DD | $DI_0$[15:8] | $DI_0$[7:0] | $DQ_0$[15:8] | $DQ_0$[7:0] | $D_0$[15:8] | $D_0$[7:0] | $D_1$[15:8] | $D_1$[7:0] | $D_0$[15:8] | $D_0$[7:0] | 0000 0000 | 0000 0000 |

**表 5. Detailed Frame Assembly for Two-Lane Modes (Modes 2 and 4)**

| OUTPUT LANE | LMFS = 2441 | | | | LMFS = 2881 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB | $A_0$[15:8] | $A_0$[7:0] | $B_0$[15:8] | $B_0$[7:0] | $AI_0$[15:8] | $AI_0$[7:0] | $AQ_0$[15:8] | $AQ_0$7:0] | $BI_0$[15:8] | $BI_0$[7:0] | $BQ_0$[15:8] | $BQ_0$[7:0] |
| DC | $C_0$[15:8] | $C_0$[7:0] | $D_0$[15:8] | $D_0$[7:0] | $CI_0$[15:8] | $CI_0$[7:0] | $CQ_0$[15:8] | $CQ_0$[7:0] | $DI_0$[15:8] | $DI_0$[7:0] | $DQ_0$[15:8] | $DQ_0$[7:0] |

**表 6. Detailed Frame Assembly for Four-Lane Mode (2x Interleaved Dual ADC)**

| OUTPUT LANE | LMFS = 4211 | | | |
|---|---|---|---|---|
| DA | $AB^{(1)}_0$[15:8] | $AB_1$[15:8] | $AB_2$[15:8] | $AB_3$[15:8] |
| DB | $AB_0$[7:0] | $AB_1$[7:0] | $AB_2$[7:0] | $AB_3$[7:0] |
| DC | $CD^{(2)}_0$[15:8] | $CD_1$[15:8] | $CD_2$[15:8] | $CD_3$[15:8] |
| DD | $CD_0$[7:0] | $CD_1$[7:0] | $CD_2$[7:0] | $CD_3$[7:0] |

(1) AB corresponds to the average output of channel A and channel B.
(2) CD corresponds to the average output of channel C and channel D.

### 7.5.4 JESD Output Switch

To ease layout constraints, the ADS54J64 provides a digital cross-point switch in the JESD204B block (as shown in 图 68) that allows internal routing of any output of the two ADCs within one channel pair to any of the two JESD204B serial transmitters. The cross-point switch routing is configured via the SPI (address 41h in the SERDES_XX digital page).

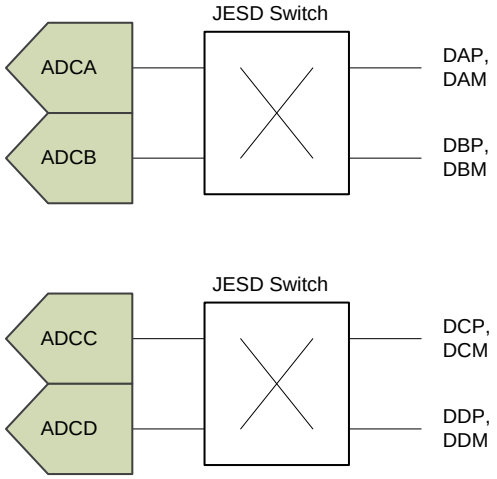



**图 68. Switching the Output Lanes**

#### *7.5.4.1 SerDes Transmitter Interface*

As shown in 图 69, each 10-Gbps SerDes transmitter output requires ac-coupling between the transmitter and receiver. Terminate the differential pair with 100 Ω as close to the receiving device as possible to avoid unwanted reflections and signal degradation.

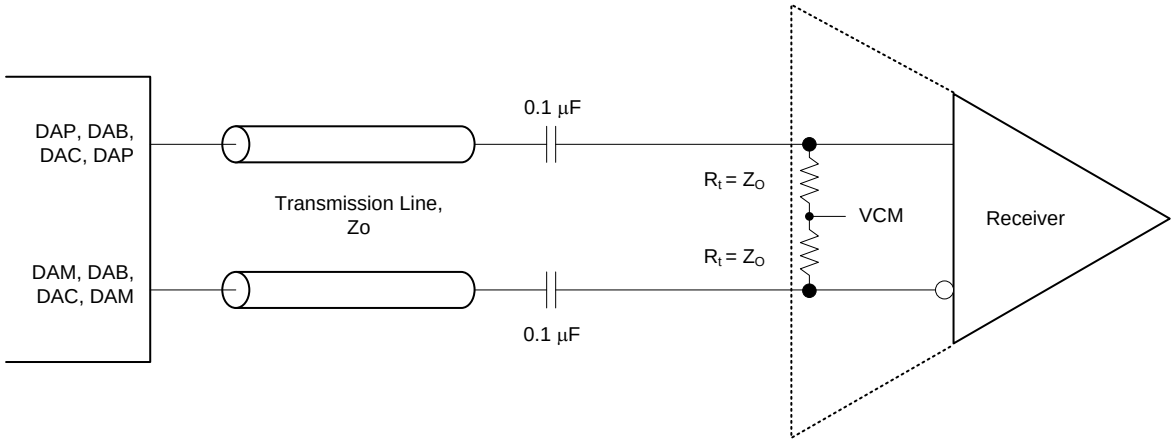



**图 69. SerDes Transmitter Connection to Receiver**

#### *7.5.4.2 SYNCb Interface*

The ADS54J64 supports single SYNCb control (where the SYNCb input controls all four JESD204B links) or dual SYNCb control (where one SYNCb input controls two JESD204B lanes: DA, DB and DC, DD). When using the single SYNCb control, connect the unused input to a differential logic high (SYNCbxxP = DVDD, SYNCbxxM = 0 V).


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#### 7.5.4.3 Eye Diagram

图 70 to 图 73 show the serial output eye diagrams of the ADS54J64 at 7.5 Gbps and 10 Gbps with default and increased output voltage swing against the JESD204B mask.

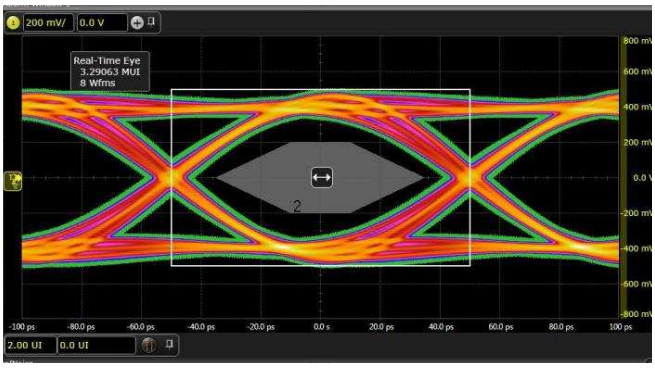



图 70. Eye at 10-Gbps Bit Rate With Default Output Swing

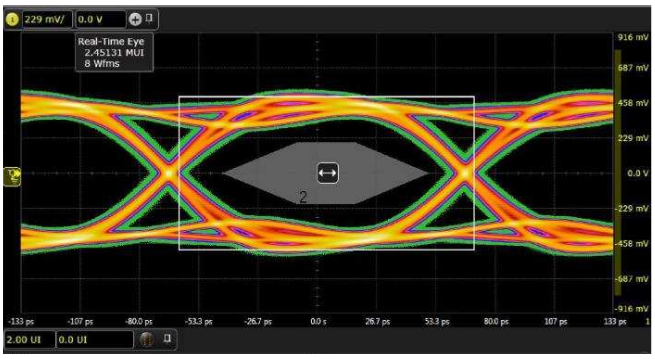



图 71. Eye at 7.5-Gbps Bit Rate With Default Output Swing

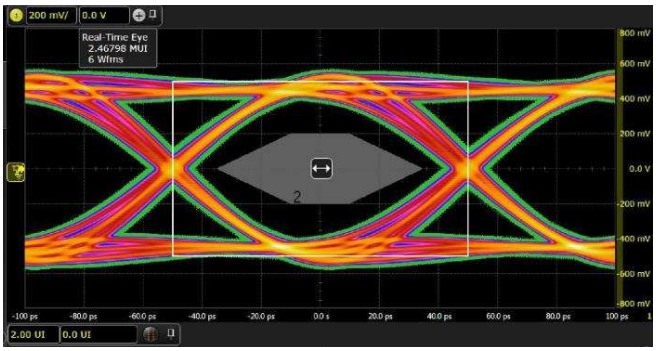



图 72. Eye at 10-Gbps Bit Rate With Increased Output Swing

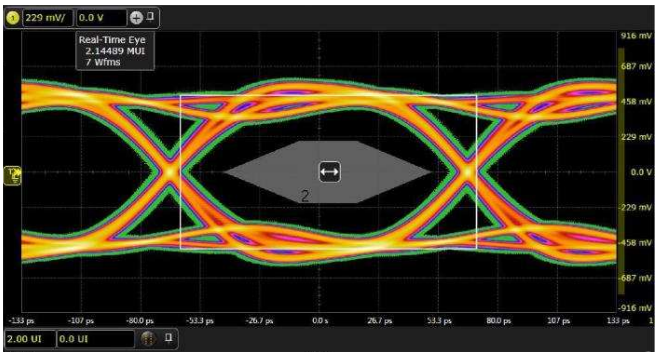



图 73. Eye at 7.5-Gbps Bit Rate With Increased Output Swing

### 7.5.5 Device Configuration

The ADS54J64 can be configured using a serial programming interface, as described in the *Register Maps* section. In addition, the device has one dedicated parallel pin (PDN) for controlling the power-down modes. The ADS54J64 supports a 24-bit (16-bit address, 8-bit data) SPI operation and uses paging to access all register bits.

#### 7.5.5.1 Details of the Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDIN (serial data input data), and SDOUT (serial data output) pins. Serially shifting bits into the device is enabled when SEN is low. SDIN serial data are latched at every SCLK rising edge when SEN is active (low). Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The first 16 bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 10 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

##### 7.5.5.1.1 Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one hardware reset by applying a high pulse on the RESET pin.

### 7.5.5.2 Serial Register Write

The internal registers of the ADS54J64 can be programmed (as shown in 图 74) by:

1. Driving the SEN pin low
2. Setting the R/W bit = 0
3. Initiating a serial interface cycle specifying the address of the register (A[14:0]) whose content must be written
4. Writing the 8-bit data that is latched in on the SCLK rising edge

The ADS54J64 has several different register pages (page selection in address 11h, 12h). Specify the register page before writing to the desired address. The register page only must be set one time for continuous writes to the same page.

During the write operation, the SDOUT pin is in a high-impedance mode and must float.

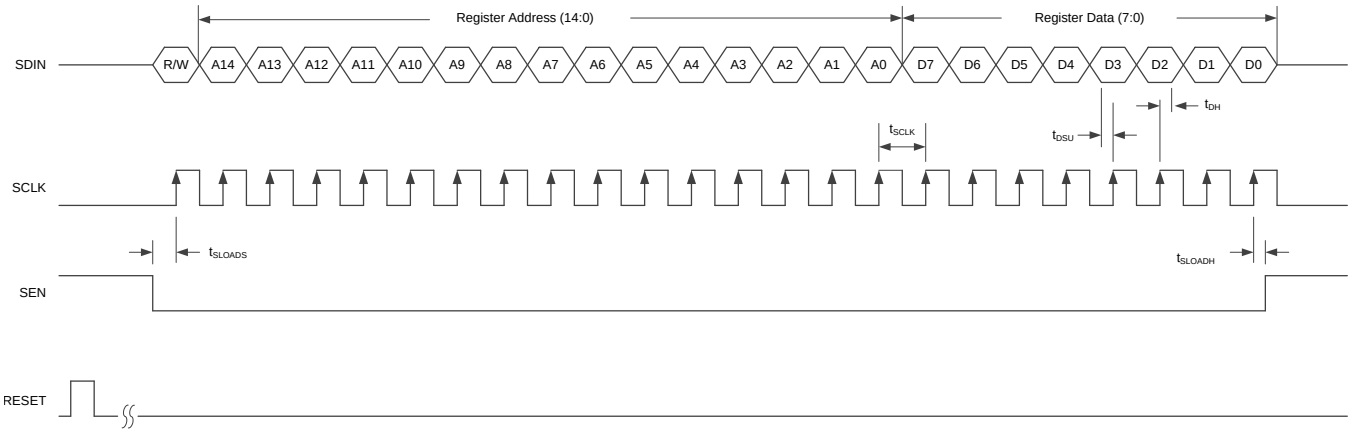



**图 74. Serial Interface Write Timing Diagram**


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### 7.5.5.3 Serial Read

图 75 shows a typical 4-wire serial register readout. In the default 4-pin configuration, the SDIN pin is the data output from the ADS54J64 during the data transfer cycle when SDOUT is in a high-impedance state. The internal registers of the ADS54J64 can be read out by:

1. Driving the SEN pin low
2. Setting the R/W bit to 1 to enable read back
3. Specifying the address of the register (A[14:0]) whose content must be read back
4. The device outputs the contents (D[7:0]) of the selected register on the SDOUT pin (pin 51)
5. The external controller can latch the contents at the SCLK rising edge

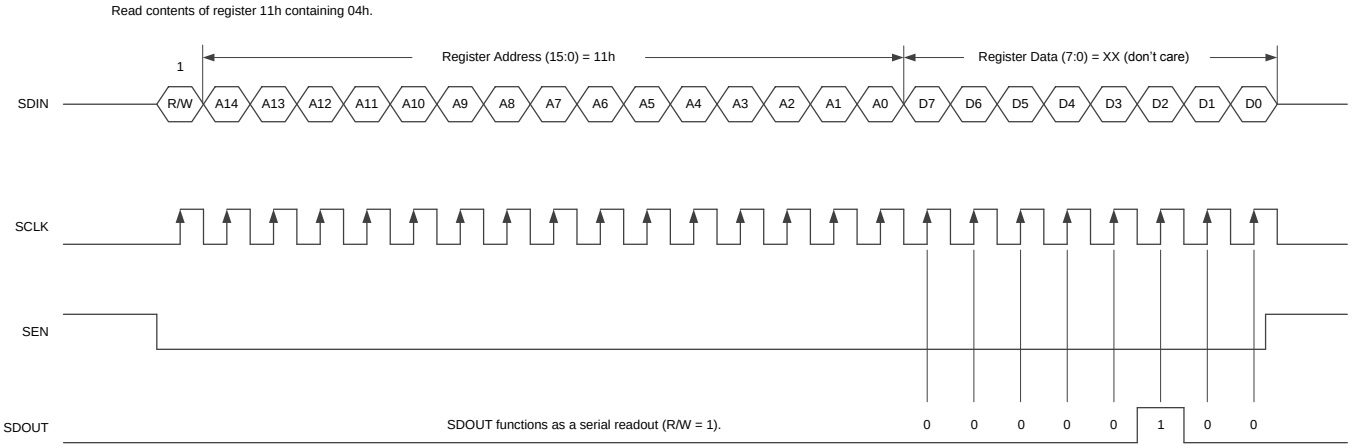



**图 75. Serial Interface 4-Wire Read Timing Diagram**

## 7.6 Register Maps

### 7.6.1 Register Map

The ADS54J64 registers are organized on different pages depending on their internal functions. The pages are accessed by selecting the page in the master pages 11h–13h. The page selection must only be written one time for a continuous update of registers for that page.

There are six different SPI banks (see 图 76 and 表 7) that group together different functions:

- GLOBAL: contains controls for accessing other SPI banks
- DIGTOP: top-level digital functions
- ANALOG: registers controlling power-down and analog functions
- SERDES_XX: registers controlling JESD204B functions
- CHX: registers controlling channel-specific functions, including DDC
- ADCXX: register page for one of the eight interleaved ADCs

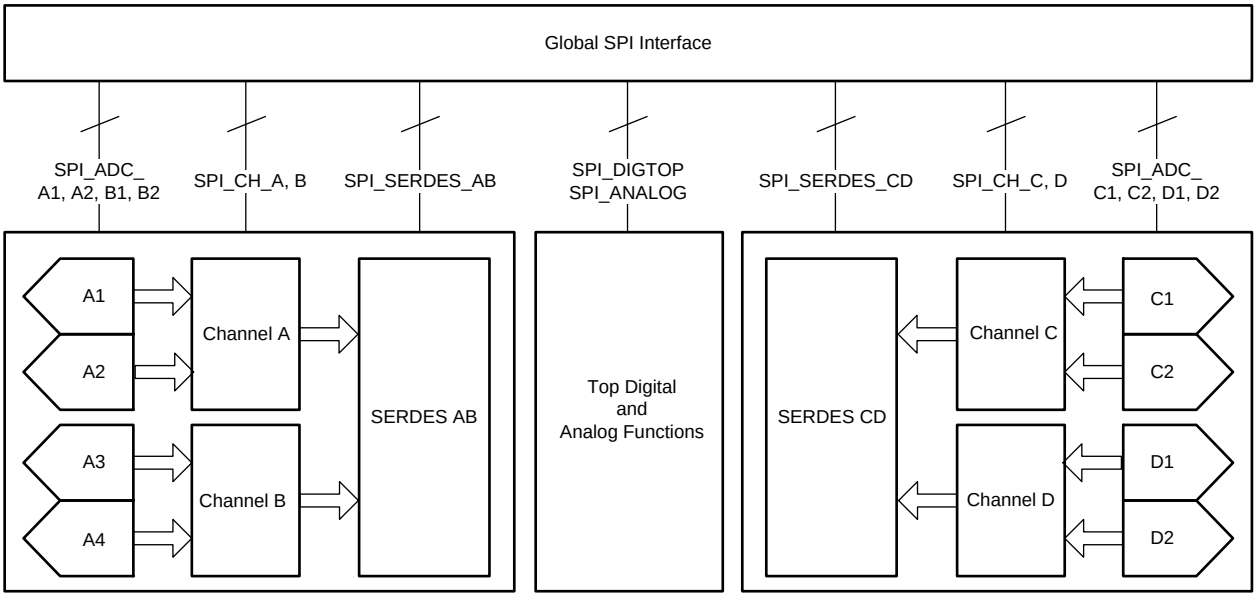



**图 76. SPI Register Block Diagram**


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## 表 7. Serial Interface Register Map

| ADDRESS (Hex) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **GLOBAL PAGE** | | | | | | | | |
| 00h | WRITE_1 | 0 | 0 | 0 | 0 | 0 | 0 | SW_RESET |
| 04h | VERSION_ID | | | | | | | |
| 11h | SPI_D2 | SPI_D1 | SPI_C2 | SPI_C1 | SPI_B2 | SPI_B1 | SPI_A2 | SPI_A1 |
| 12h | 0 | SPI_SERDES_CD | SPI_SERDES_AB | SPI_CHD | SPI_CHC | SPI_CHB | SPI_CHA | SPI_DIGTOP |
| 13h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SPI_ANALOG |
| **DIGTOP PAGE** | | | | | | | | |
| 64h | 0 | 0 | 0 | 0 | 0 | 0 | FS_375_500 | 0 |
| 8Dh | CUSTOMPATTERN1[7:0] | | | | | | | |
| 8Eh | CUSTOMPATTERN1[15:8] | | | | | | | |
| 8Fh | CUSTOMPATTERN2[7:0] | | | | | | | |
| 90h | CUSTOMPATTERN2[15:8] | | | | | | | |
| 91h | TESTPATTERNSELECT | | | | TESTPATTERNENCHD | TESTPATTERNENCHC | TESTPATTERNENCHB | TESTPATTERNENCHA |
| A5h | 0 | 0 | 0 | 0 | 0 | 0 | CH_CD_AVG_EN | CH_AB_AVG_EN |
| A6h | 0 | 0 | AVG_ENABLE | OVR_ON_LSB | GAIN_WORD_ENABLE | 0 | 0 | 0 |
| ABh | 0 | 0 | 0 | 0 | 0 | 0 | INTERLEAVE_A | SPECIALMODE0 |
| ACh | 0 | 0 | 0 | 0 | 0 | 0 | INTERLEAVE_C | SPECIALMODE1 |
| ADh | 0 | 0 | 0 | 0 | DDCMODEAB | | | |
| AEh | 0 | 0 | 0 | 0 | DDCMODECD | | | |
| B7h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LOAD_TRIMS |
| 8Ch | 0 | 0 | 0 | 0 | 0 | 0 | ENABLE_LOAD_TRIMS | 0 |
| **ANALOG PAGE** | | | | | | | | |
| 6Ah | 0 | 0 | 0 | 0 | 0 | 0 | DIS_SYSREF | 0 |
| 6Fh | 0 | JESD_SWING | | | 0 | 0 | 0 | 0 |
| 71h | EMP_LANE_B[5:4] | | EMP_LANE_A | | | | | |
| 72h | 0 | 0 | 0 | 0 | EMP_LANE_B[3:0] | | | |
| 93h | EMP_LANE_D[5:4] | | EMP_LANE_C | | | | | |
| 94h | 0 | 0 | 0 | 0 | EMP_LANE_D[3:0] | | | |
| 9Bh | 0 | 0 | 0 | SYSREF_PDN | 0 | 0 | 0 | 0 |
| 9Dh | PDN_CHA | PDN_CHB | 0 | 0 | PDN_CHD | PDN_CHC | 0 | 0 |
| 9Eh | 0 | 0 | 0 | PDN_SYNCAB | 0 | 0 | 0 | PDN_GLOBAL |
| 9Fh | 0 | 0 | 0 | 0 | 0 | 0 | PIN_PDN_MODE | FAST_PDN |
| AFh | 0 | 0 | 0 | 0 | 0 | 0 | PDN_SYNCCD | 0 |
| **SERDES_XX PAGE** | | | | | | | | |
| 20h | CTRL_K | CTRL_SER_MODE | 0 | TRANS_TEST_EN | 0 | LANE_ALIGN | FRAME_ALIGN | TX_ILA_DIS |
| 21h | SYNC_REQ | OPT_SYNC_REQ | SYNCB_SEL_AB_CD | 0 | 0 | 0 | SERDES_MODE | |
| 22h | LINK_LAYER_TESTMODE_SEL | | | RPAT_SET_DISP | LMFC_MASK_RESET | 0 | 0 | 0 |
| 23h | FORCE_LMFC_COUNT | LMFC_CNT_INIT | | | | | RELEASE_ILANE_REQ | |
| 25h | SCR_EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 26h | 0 | 0 | 0 | K_NO_OF_FRAMES_PER_MULTIFRAME | | | | |

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## 表 7. Serial Interface Register Map (接下页)

| ADDRESS (Hex) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 28h | 0 | 0 | 0 | 0 | CTRL_LID | 0 | 0 | 0 |
| 2Dh | LID1 | | | | LID2 | | | |
| 36h | PRBS_MODE | | 0 | 0 | 0 | 0 | 0 | 0 |
| 41h | LANE_BONA | | | | LANE_AONB | | | |
| 42h | 0 | 0 | 0 | 0 | INVERT_AC | | INVERT_BD | |
| **CHX PAGE** | | | | | | | | |
| 26h | 0 | 0 | 0 | 0 | 0 | 0 | GAINWORD | |
| 27h | OVR_ENABLE | OVR_FAST_SEL | 0 | 0 | OVR_LSB1 | 0 | OVR_LSB0 | 0 |
| 2Dh | 0 | 0 | 0 | 0 | 0 | 0 | NYQUIST_SELECT | 0 |
| 78h | 0 | 0 | 0 | 0 | 0 | FS4_SIGN | NYQ_SEL_MODE02 | NYQ_SEL |
| 7Ah | NCO_WORD[15:8] | | | | | | | |
| 7Bh | NCO_WORD[7:0] | | | | | | | |
| 7Eh | 0 | 0 | 0 | 0 | 0 | MODE467_GAIN | MODE0_GAIN | MODE13_GAIN |
| **ADCXX PAGE** | | | | | | | | |
| 07h | FAST_OVR_THRESHOLD_HIGH | | | | | | | |
| 08h | FAST_OVR_THRESHOLD_LOW | | | | | | | |
| D5h | 0 | 0 | 0 | 0 | CAL_EN | 0 | 0 | 0 |
| 2Ah | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ADC_TRIM1 |
| CFh | ADC_TRIM2 | | | | 0 | 0 | 0 | 0 |


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#### 7.6.1.1 Register Description

表 8 lists the access codes for the ADS54J64 registers.

**表 8. ADS54J64 Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| R | R | Read |
| R/W | R-W | Read or Write |
| W | W | Write |
| *-n* | | Value after reset or the default value |

##### 7.6.1.1.1 GLOBAL Page Register Description

###### 7.6.1.1.1.1 Register 00h (address = 00h) [reset = 0h], GLOBAL Page

**图 77. Register 0h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| WRITE_1 | 0 | 0 | 0 | 0 | 0 | 0 | SW_RESET |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 9. Register 00h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | WRITE_1 | R/W | 0h | Always write 1 |
| 6-1 | 0 | R/W | 0h | Must read or write 0 |
| 0 | SW_RESET | R/W | 0h | This bit rests the device. |

###### 7.6.1.1.1.2 Register 04h (address = 04h) [reset = 0h], GLOBAL Page

**图 78. Register 4h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VERSION_ID | | | | | | | |
| R-0h | | | | | | | |

**表 10. Register 04h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | VERSION_ID | R | 0h | These bits set the version ID of the device.<br>16 : PG 1.0<br>32 : PG 2.0<br>48 : PG 3.0 |

#### *7.6.1.1.1.3 Register 11h (address = 11h) [reset = 0h], GLOBAL Page*

**图 79. Register 11h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SPI_D2 | SPI_D1 | SPI_C2 | SPI_C1 | SPI_B2 | SPI_B1 | SPI_A2 | SPI_A1 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 11. Register 11h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SPI_D2 | R/W | 0h | This bit selects the ADC D2 SPI.<br>0 : ADC D2 SPI is disabled<br>1 : ADC D2 SPI is enabled |
| 6 | SPI_D1 | R/W | 0h | This bit selects the ADC D1 SPI.<br>0 : ADC D1 SPI is disabled<br>1 : ADC D1 SPI is enabled |
| 5 | SPI_C2 | R/W | 0h | This bit selects the ADC C2 SPI<br>0 : ADC C2 SPI is disabled<br>1 : ADC C2 SPI is enabled |
| 4 | SPI_C1 | R/W | 0h | This bit selects the ADC C1 SPI.<br>0 : ADC C1 SPI is disabled<br>1 : ADC C1 SPI is enabled |
| 3 | SPI_B2 | R/W | 0h | This bit selects the ADC B2 SPI.<br>0 : ADC B2 SPI is disabled<br>1 : ADC B2 SPI is enabled |
| 2 | SPI_B1 | R/W | 0h | This bit selects the ADC B1 SPI.<br>0 : ADC B1 SPI is disabled<br>1 : ADC B1 SPI is enabled |
| 1 | SPI_A2 | R/W | 0h | This bit selects the ADC A2 SPI.<br>0 : ADC A2 SPI is disabled<br>1 : ADC A2 SPI is enabled |
| 0 | SPI_A1 | R/W | 0h | This bit selects the ADC A1 SPI.<br>0 : ADC A1 SPI is disabled<br>1 : ADC A1 SPI is enabled |


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#### 7.6.1.1.1.4 Register 12h (address = 12h) [reset = 0h], GLOBAL Page

**图 80. Register 12h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SPI_SERDES_CD | SPI_SERDES_AB | SPI_CHD | SPI_CHC | SPI_CHB | SPI_CHA | SPI_DIGTOP |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 12. Register 12h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0h | Must read or write 0 |
| 6 | SPI_SERDES_CD | R/W | 0h | This bit selects the channel CD SerDes SPI.<br>0 : Channel CD SerDes SPI is disabled<br>1 : Channel CD SerDes SPI is enabled |
| 5 | SPI_SERDES_AB | R/W | 0h | This bit selects the channel AB SerDes SPI.<br>0 : Channel AB SerDes is disabled<br>1 : Channel AB SerDes is enabled |
| 4 | SPI_CHD | R/W | 0h | This bit selects the channel D SPI.<br>0 : Channel D SPI is disabled<br>1 : Channel D SPI is enabled |
| 3 | SPI_CHC | R/W | 0h | This bit selects the channel C SPI.<br>0 : Channel C SPI is disabled<br>1 : Channel C SPI is enabled |
| 2 | SPI_CHB | R/W | 0h | This bit selects the channel B SPI.<br>0 : Channel B SPI is disabled<br>1 : Channel B SPI is enabled |
| 1 | SPI_CHA | R/W | 0h | This bit selects the channel A SPI.<br>0 : Channel A SPI is disabled<br>1 : Channel A SPI is enabled |
| 0 | SPI_DIGTOP | R/W | 0h | This bit selects the DIGTOP SPI.<br>0 : DIGTOP SPI is disabled<br>1 : DIGTOP SPI is enabled |

#### 7.6.1.1.1.5 Register 13h (address = 13h) [reset = 0h], GLOBAL Page

**图 81. Register 13h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SPI_ANALOG |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 13. Register 13h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R/W | 0h | Must read or write 0 |
| 0 | SPI_ANALOG | R/W | 0h | This bit selects the analog SPI.<br>0 : Analog SPI is disabled<br>1 : Analog SPI is enabled |

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#### 7.6.1.1.2 DIGTOP Page Register Description

##### *7.6.1.1.2.1 Register 64h (address = 64h) [reset = 0h], DIGTOP Page*

**图 82. Register 64h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | FS_375_500 | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 14. Register 64h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0h | Must read or write 0 |
| 1 | FS_375_500 | R/W | 0h | This bit selects the clock rate for loading trims.<br>0 : 375 MSPS<br>1 : 500 MSPS |
| 0 | 0 | R/W | 0h | Must read or write 0 |

##### *7.6.1.1.2.2 Register 8Dh (address = 8Dh) [reset = 0h], DIGTOP Page*

**图 83. Register 8Dh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUSTOMPATTERN1[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**表 15. Register 8Dh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CUSTOMPATTERN1[7:0] | R/W | 0h | These bits set the custom pattern 1 that is used when the test pattern is enabled and set to a single or dual test pattern. |

##### *7.6.1.1.2.3 Register 8Eh (address = 8Eh) [reset = 0h], DIGTOP Page*

**图 84. Register 8Eh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUSTOMPATTERN1[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**表 16. Register 8Eh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CUSTOMPATTERN1[15:8] | R/W | 0h | These bits set the custom pattern 1 that is used when the test pattern is enabled and set to a single or dual test pattern. |


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#### 7.6.1.1.2.4 Register 8Fh (address = 8Fh) [reset = 0h], DIGTOP Page

**图 85. Register 8Fh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUSTOMPATTERN2[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**表 17. Register 8Fh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CUSTOMPATTERN2[7:0] | R/W | 0h | These bits set the custom pattern 2 that is used when the test pattern select is set to dual pattern mode. |

#### 7.6.1.1.2.5 Register 90h (address = 90h) [reset = 0h], DIGTOP Page

**图 86. Register 90h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUSTOMPATTERN2[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**表 18. Register 90h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CUSTOMPATTERN2[15:8] | R/W | 0h | These bits set the custom pattern 2 that is used when the test pattern select is set to dual pattern mode. |

#### 7.6.1.1.2.6 Register 91h (address = 91h) [reset = 0h], DIGTOP Page

**图 87. Register 91h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TESTPATTERNSELECT | | | | TESTPATTERNENCHD | TESTPATTERNENCHC | TESTPATTERNENCHB | TESTPATTERNENCHA |
| R/W-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 19. Register 91h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | TESTPATTERNSELECT | R/W | 0h | These bits select the test pattern on the output when the test pattern is enabled for a suitable channel.<br>0 : Default<br>1 : All zeros<br>2 : All ones<br>3 : Toggle pattern<br>4 : Ramp pattern<br>6 : Custom pattern 1<br>7 : Toggle between custom pattern 1 and custom pattern 2<br>8 : Deskew pattern (0xAAAA) |
| 3 | TESTPATTERNENCHD | R/W | 0h | This bit enables the channel D test pattern.<br>0 : Default data on channel D<br>1 : Enable test pattern on channel D |
| 2 | TESTPATTERNENCHC | R/W | 0h | This bit enables the channel C test pattern.<br>0 : Default data on channel C<br>1 : Enable test pattern on channel C |
| 1 | TESTPATTERNENCHB | R/W | 0h | This bit enables the channel B test pattern.<br>0 : Default data on channel B<br>1 : Enable test pattern on channel B |
| 0 | TESTPATTERNENCHA | R/W | 0h | This bit enables the channel A test pattern.<br>0 : Default data on channel A<br>1 : Enable test pattern on channel A |

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#### 7.6.1.1.2.7 Register A5h (address = A5h) [reset = 0h], DIGTOP Page

**图 88. Register A5h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | CH_CD_AVG_EN | CH_AB_AVG_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 20. Register A5h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0h | Must read or write 0 |
| 1 | CH_CD_AVG_EN | R/W | 0h | 0: Averaging is disabled for channels C, D<br>1: Averaging is enabled for channels C, D; set AVG_ENABLE in Register A6h (address = A6h) [reset = 0h], DIGTOP Page to 1 if using this option |
| 0 | CH_AB_AVG_EN | R/W | 0h | 0: Averaging is disabled for channels A, B<br>1: Averaging is enabled for channels A, B; set AVG_ENABLE in Register A6h (address = A6h) [reset = 0h], DIGTOP Page to 1 if using this option |

#### 7.6.1.1.2.8 Register A6h (address = A6h) [reset = 0h], DIGTOP Page

**图 89. Register A6h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | AVG_ENABLE | OVR_ON_LSB | GAIN_WORD_ENABLE | 0 | 0 | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 21. Register A6h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | R/W | 0h | Must read or write 0 |
| 5 | AVG_ENABLE | R/W | 0h | 0: Default operation<br>1: Enable averaging option for the AB and CD channel pairs |
| 4 | OVR_ON_LSB | R/W | 0h | This bit enables the overrange indicator (OVR) on the LSB1 and LSB0 bits. OVR_LSB1 and OVR_LSB0 must be configured in register 27h of the CHX page.<br>0 : Default data<br>1 : OVR on LSB1 and LSB0 bits |
| 3 | GAIN_WORD_ENABLE | R/W | 0h | This bit enables the digital gain. Gain can be programmed using the GAINWORD bits in register 26h of the CHX page.<br>0 : Disable digital gain<br>1 : Enable digital gain |
| 2-0 | 0 | R/W | 0h | Must read or write 0 |


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#### 7.6.1.1.2.9 Register ABh (address = ABh) [reset = 0h], DIGTOP Page

图 90. Register ABh

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | INTERLEAVE_A | SPECIALMODE0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

表 22. Register ABh Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0h | Must read or write 0 |
| 1 | INTERLEAVE_A | R/W | 0h | 0: Default operation<br>1: 2x interleaved data enable; this bit is used in dual ADC mode to bring the average data of channels A and B on the JESD outputs; averaging mode is enabled by setting CH_AB_AVG_EN to 1 (see register A5h) |
| 0 | SPECIALMODE0 | R/W | 0h | Always write 1 |

#### 7.6.1.1.2.10 Register ACh (address = ACh) [reset = 0h], DIGTOP Page

图 91. Register ACh

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | INTERLEAVE_C | SPECIALMODE1 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

表 23. Register ACh Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0h | Must read or write 0 |
| 1 | INTERLEAVE_C | R/W | 0h | 0: Default operation<br>1: 2x interleaved data enable; this bit is used in dual ADC mode to bring the average data of channels C and D on the JESD outputs; averaging mode is enabled by setting CH_CD_AVG_EN to 1 (see register A5h) |
| 0 | SPECIALMODE1 | R/W | 0h | Always write 1 |

#### 7.6.1.1.2.11 Register ADh (address = ADh) [reset = 0h], DIGTOP Page

图 92. Register ADh

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DDCMODEAB | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | |

表 24. Register ADh Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R/W | 0h | Must read or write 0 |
| 3-0 | DDCMODEAB | R/W | 0h | These bits select the DDC mode for the AB channel pair.<br>0 : Mode 0<br>1 : Mode 1<br>2 : Mode 2<br>3 : Mode 3<br>4 : Mode 4<br>6 : Mode 6<br>7 : Mode 7<br>8 : Mode 8 |

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#### 7.6.1.1.2.12 Register AEh (address = AEh) [reset = 0h], DIGTOP Page

**图 93. Register AEh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DDCMODECD | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | |

**表 25. Register AEh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R/W | 0h | Must read or write 0 |
| 3-0 | DDCMODECD | R/W | 0h | These bits select the DDC mode for the CD channel pair.<br>0 : Mode 0<br>1 : Mode 1<br>2 : Mode 2<br>3 : Mode 3<br>4 : Mode 4<br>6 : Mode 6<br>7 : Mode 7<br>8 : Mode 8 |

#### 7.6.1.1.2.13 Register B7h (address = B7h) [reset = 0h], DIGTOP Page

**图 94. Register B7h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | LOAD_TRIMS |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 26. Register B7h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R/W | 0h | Must read or write 0 |
| 0 | LOAD_TRIMS | R/W | 0h | This bit load trims the device. |

#### 7.6.1.1.2.14 Register 8Ch (address = 8Ch) [reset = 0h], DIGTOP Page

**图 95. Register 8Ch**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | ENABLE_LOAD_TRIMS | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 27. Register 8Ch Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0h | Must read or write 0 |
| 1 | ENABLE_LOAD_TRIMS | R/W | 0h | 0: Trim loading is disabled<br>1: Trim loading is enabled (recommended) |
| 0 | 0 | R/W | 0h | Must read or write 0 |


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#### 7.6.1.1.3 ANALOG Page Register Description

##### *7.6.1.1.3.1 Register 6Ah (address = 6Ah) [reset = 0h], ANALOG Page*

**图 96. Register 6Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | DIS_SYSREF | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 28. Register 6Ah Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0h | Must read or write 0 |
| 1 | DIS_SYSREF | R/W | 0h | This bit masks the SYSREF input.<br>0 : SYSREF input is not masked<br>1 : SYSREF input is masked |
| 0 | 0 | R/W | 0h | Must read or write 0 |

##### *7.6.1.1.3.2 Register 6Fh (address = 6Fh) [reset = 0h], ANALOG Page*

**图 97. Register 6Fh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | JESD_SWING | | | 0 | 0 | 0 | 0 |
| R/W-0h | R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 29. Register 6Fh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0h | Must read or write 0 |
| 6-4 | JESD_SWING | R/W | 0h | These bits control the JESD swing.<br>0 : 860 $mV_{PP}$<br>1 : 810 $mV_{PP}$<br>2 : 770 $mV_{PP}$<br>3 : 745 $mV_{PP}$<br>4 : 960 $mV_{PP}$<br>5 : 930 $mV_{PP}$<br>6 : 905 $mV_{PP}$<br>7 : 880 $mV_{PP}$ |
| 3-0 | 0 | R/W | 0h | Must read or write 0 |

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#### 7.6.1.1.3.3 Register 71h (address = 71h) [reset = 0h], ANALOG Page

**图 98. Register 71h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EMP_LANE_B[5:4] | | EMP_LANE_A | | | | | |
| R/W-0h | | R/W-0h | | | | | |

**表 30. Register 71h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | EMP_LANE_B[5:4] | R/W | 0h | These bits along with bits 3-0 of register 72h set the de-emphasis for lane B.<br>These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in decibels (dB) is measured as the ratio between the peak value after the signal transitions to the settled value of the voltage in one bit period.<br>0 : 0 dB<br>1 : –1 dB<br>3 : –2 dB<br>7 : –4.1 dB<br>15 : –6.2 dB<br>31 : –8.2 dB<br>63 : –11.5 dB<br>Others: Do not use |
| 5-0 | EMP_LANE_A | R/W | 0h | These bits set the de-emphasis for lane A.<br>These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transitions to the settled value of the voltage in one bit period.<br>0 : 0 dB<br>1 : –1 dB<br>3 : –2 dB<br>7 : –4.1 dB<br>15 : –6.2 dB<br>31 : –8.2 dB<br>63 : –11.5 dB<br>Others: Do not use |

#### 7.6.1.1.3.4 Register 72h (address = 72h) [reset = 0h], ANALOG Page

**图 99. Register 72h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | EMP_LANE_B[3:0] | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | |

**表 31. Register 72h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R/W | 0h | Must read or write 0 |
| 3-0 | EMP_LANE_B[3:0] | R/W | 0h | These bits along with bits 7-6 of register 71h set the de-emphasis for lane B.<br>These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transitions to the settled value of the voltage in one bit period.<br>0 : 0 dB<br>1 : –1 dB<br>3 : –2 dB<br>7 : –4.1 dB<br>15 : –6.2 dB<br>31 : –8.2 dB<br>63 : –11.5 dB<br>Others: Do not use |


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#### 7.6.1.1.3.5 Register 93h (address = 93h) [reset = 0h], ANALOG Page

**图 100. Register 93h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EMP_LANE_D[5:4] | | EMP_LANE_C | | | | | |
| R/W-0h | | R/W-0h | | | | | |

**表 32. Register 93h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | EMP_LANE_D[5:4] | R/W | 0h | These bits along with bits 3-0 of register 94h set the de-emphasis for lane D.<br>These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transitions to the settled value of the voltage in one bit period.<br>0 : 0 dB<br>1 : –1 dB<br>3 : –2 dB<br>7 : –4.1 dB<br>15 : –6.2 dB<br>31 : –8.2 dB<br>63 : –11.5 dB<br>Others: Do not use |
| 5-0 | EMP_LANE_C | R/W | 0h | These bits set the de-emphasis for lane C.<br>These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transitions to the settled value of the voltage in one bit period.<br>0 : 0 dB<br>1 : –1 dB<br>3 : –2 dB<br>7 : –4.1 dB<br>15 : –6.2 dB<br>31 : –8.2 dB<br>63 : –11.5 dB<br>Others: Do not use |

#### 7.6.1.1.3.6 Register 94h (address = 94h) [reset = 0h], ANALOG Page

**图 101. Register 94h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | EMP_LANE_D[3:0] | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | |

**表 33. Register 94h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R/W | 0h | Must read or write 0 |
| 3-0 | EMP_LANE_D[3:0] | R/W | 0h | These bits along with bits 7-4 of register 93h set the de-emphasis for lane D.<br>These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transitions to the settled value of the voltage in one bit period.<br>0 : 0 dB<br>1 : –1 dB<br>3 : –2 dB<br>7 : –4.1 dB<br>15 : –6.2 dB<br>31 : –8.2 dB<br>63 : –11.5 dB<br>Others: Do not use |

#### 7.6.1.1.3.7 Register 9Bh (address = 9Bh) [reset = 0h], ANALOG Page

**图 102. Register 9Bh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | SYSREF_PDN | 0 | 0 | 0 | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 34. Register 9Bh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | R/W | 0h | Must read or write 0 |
| 4 | SYSREF_PDN | R/W | 0h | This bit powers down the SYSREF buffer.<br>0 : SYSREF buffer is powered up<br>1 : SYSREF buffer is powered down |
| 3-0 | 0 | R/W | 0h | Must read or write 0 |

#### 7.6.1.1.3.8 Register 9Dh (address = 9Dh) [reset = 0h], ANALOG Page

**图 103. Register 9Dh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PDN_CHA | PDN_CHB | 0 | 0 | PDN_CHD | PDN_CHC | 0 | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 35. Register 9Dh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PDN_CHA | R/W | 0h | This bit powers down channel A.<br>0 : Normal operation<br>1 : Channel A is powered down |
| 6 | PDN_CHB | R/W | 0h | This bit powers down channel B.<br>0 : Normal operation<br>1 : Channel B is powered down |
| 5-4 | 0 | R/W | 0h | Must read or write 0 |
| 3 | PDN_CHD | R/W | 0h | This bit powers down channel D.<br>0 : Normal operation<br>1 : Channel D is powered down |
| 2 | PDN_CHC | R/W | 0h | This bit powers down channel C.<br>0 : Normal operation<br>1 : Channel C is powered down |
| 1-0 | 0 | R/W | 0h | Must read or write 0 |


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#### 7.6.1.1.3.9 Register 9Eh (address = 9Eh) [reset = 0h], ANALOG Page

**图 104. Register 9Eh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | PDN_SYNCAB | 0 | 0 | 0 | PDN_GLOBAL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 36. Register 9Eh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | R/W | 0h | Must read or write 0 |
| 4 | PDN_SYNCAB | R/W | 0h | This bit controls the STNCAB buffer power-down.<br>0 : SYNCAB buffer is powered up<br>1 : SYNCAB buffer is powered down |
| 3-1 | 0 | R/W | 0h | Must read or write 0 |
| 0 | PDN_GLOBAL | R/W | 0h | This bit controls the global power-down.<br>0 : Global power-up<br>1 : Global power-down |

#### 7.6.1.1.3.10 Register 9Fh (address = 9Fh) [reset = 0h], ANALOG Page

**图 105. Register 9Fh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | PIN_PDN_MODE | FAST_PDN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 37. Register 9Fh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0h | Must read or write 0 |
| 1 | PIN_PDN_MODE | R/W | 0h | This bit selects the pin power-down mode.<br>0 : PDN pin is configured to fast power-down<br>1 : PDN pin is configured to global power-down |
| 0 | FAST_PDN | R/W | 0h | This bit controls the fast power-down.<br>0 : Device powered up<br>1 : Fast power down |

#### 7.6.1.1.3.11 Register AFh (address = AFh) [reset = 0h], ANALOG Page

**图 106. Register AFh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | PDN_SYNCCD | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 38. Register AFh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0h | Must read or write 0 |
| 1 | PDN_SYNCCD | R/W | 0h | This bit controls the SYNCCD buffer power-down.<br>0 : SYNCCD buffer is powered up<br>1 : SYNCCD buffer is powered down |
| 0 | 0 | R/W | 0h | Must read or write 0 |

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#### 7.6.1.1.4 SERDES_XX Page Register Description

##### *7.6.1.1.4.1 Register 20h (address = 20h) [reset = 0h], SERDES_XX Page*

**图 107. Register 20h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CTRL_K | CTRL_SER_MODE | 0 | TRANS_TEST_EN | 0 | LANE_ALIGN | FRAME_ALIGN | TX_ILA_DIS |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 39. Register 20h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CTRL_K | R/W | 0h | This bit is the enable bit for programming the number of frames per multi-frame.<br>0 : Five frames per multi-frame (default)<br>1 : Frames per multi-frame can be programmed using register 26h |
| 6 | CTRL_SER_MODE | R/W | 0h | This bit allows the SERDES_MODE setting in register 21h (bits 1-0) to be changed.<br>0 : Disabled<br>1 : Enables SERDES_MODE setting |
| 5 | 0 | R/W | 0h | Must read or write 0 |
| 4 | TRANS_TEST_EN | R/W | 0h | This bit generates the long transport layer test pattern mode, as per section 5.1.6.3 of the JESD204B specification.<br>0 : Test mode is disabled<br>1 : Test mode is enabled |
| 3 | 0 | R/W | 0h | Must read or write 0 |
| 2 | LANE_ALIGN | R/W | 0h | This bit inserts the lane-alignment character (K28.3) for the receiver to align to the lane boundary, as per section 5.3.3.5 of the JESD204B specification.<br>0 : Normal operation<br>1 : Inserts lane-alignment characters |
| 1 | FRAME_ALIGN | R/W | 0h | This bit inserts the frame-alignment character (K28.7) for the receiver to align to the lane boundary, as per section 5.3.3.5 of the JESD204B specification.<br>0 : Normal operation<br>1 : Inserts frame-alignment characters |
| 0 | TX_ILA_DIS | R/W | 0h | This bit disables sending the initial link alignment (ILA) sequence when SYNC is deasserted.<br>0 = Normal operation<br>1 = Disables ILA |


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#### 7.6.1.1.4.2 Register 21h (address = 21h) [reset = 0h], SERDES_XX Page

**图 108. Register 21h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SYNC_REQ | OPT_SYNC_REQ | SYNCB_SEL_AB_CD | 0 | 0 | 0 | SERDES_MODE | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |

**表 40. Register 21h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SYNC_REQ | R/W | 0h | This bit controls the SYNC register (bit 6 must be enabled).<br>0 : Normal operation<br>1 : ADC output data are replaced with K28.5 characters |
| 6 | OPT_SYNC_REQ | R/W | 0h | This bit enables SYNC operation.<br>0 : Normal operation<br>1 : Enables SYNC from the SYNC_REQ register bit |
| 5 | SYNCB_SEL_AB_CD | R/W | 0h | This bit selects which SYNCb input controls the JESD interface.<br>0 : Use the SYNCbAB, SYNCbCD pins<br>1 : When set in the SerDes AB SPI, SYNCbCD is used for the SerDes AB and CD; when set in the SerDes CD SPI, SYNCbAB is used for the SerDes AB and CD |
| 4-2 | 0 | R/W | 0h | Must read or write 0 |
| 1-0 | SerDes_MODE | R/W | 0h | These bits set the JESD output parameters. The CTRL_SER_MODE bit (register 20h, bit 6) must also be set to control these bits. These bits are auto configured for modes 0, 1, 3, and 7, but must be configured for modes 2, 4, and 6. |

#### 7.6.1.1.4.3 Register 22h (address = 22h) [reset = 0h], SERDES_XX Page

**图 109. Register 22h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LINK_LAYER_TESTMODE_SEL | | | RPAT_SET_DISP | LMFC_MASK_RESET | 0 | 0 | 0 |
| R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 41. Register 22h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | LINK_LAYER_TESTMODE_SEL | R/W | 0h | These bits generate a pattern as per section 5.3.3.8.2 of the JESD204B document.<br>0 : Normal ADC data<br>1 : D21.5 (high-frequency jitter pattern)<br>2 : K28.5 (mixed-frequency jitter pattern)<br>3 : Repeat the initial lane alignment (generates a K28.5 character and continuously repeats lane alignment sequences)<br>4 : 12-octet RPAT jitter pattern<br>6 : PRBS pattern (PRBS7, 15, 23, 31); use PRBS_MODE (register 36h, bits 7-6) to select the PRBS pattern |
| 4 | RPAT_SET_DISP | R/W | 0h | This bit changes the running disparity in the modified RPAT pattern test mode (only when the link layer test mode = 100).<br>0 : Normal operation<br>1 : Changes disparity |
| 3 | LMFC_MASK_RESET | R/W | 0h | 0 : Default<br>1 : Resets the LMFC mask |
| 2-0 | 0 | R/W | 0h | Must read or write 0 |

#### 7.6.1.1.4.4 Register 23h (address = 23h) [reset = 0h], SERDES_XX Page

**图 110. Register 23h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FORCE_LMFC_COUNT | LMFC_CNT_INIT | | | | | RELEASE_ILANE_REQ | |
| R/W-0h | R/W-0h | | | | | R/W-0h | |

**表 42. Register 23h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | FORCE_LMFC_COUNT | R/W | 0h | This bit forces an LMFC count.<br>0 : Normal operation<br>1 : Enables using a different starting value for the LMFC counter |
| 6-2 | LMFC_CNT_INIT | R/W | 0h | These bits set the initial value to which the LMFC count resets. The FORCE_LMFC_COUNT register bit must be enabled. |
| 1-0 | RELEASE_ILANE_REQ | R/W | 0h | These bits delay the generation of the lane alignment sequence by 0, 1, 2, or 3 multi-frames after the code group synchronization.<br>0 : 0 multi-frames<br>1 : 1 multi-frame<br>2 : 2 multi-frames<br>3 : 3 multi-frames |

#### 7.6.1.1.4.5 Register 25h (address = 25h) [reset = 0h], SERDES_XX Page

**图 111. Register 25h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCR_EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 43. Register 25h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SCR_EN | R/W | 0h | This bit is the scramble enable bit in the JESD204B interface.<br>0 : Scrambling is disabled<br>1 : Scrambling is enabled |
| 6-0 | 0 | R/W | 0h | Must read or write 0 |

#### 7.6.1.1.4.6 Register 26h (address = 26h) [reset = 0h], SERDES_XX Page

**图 112. Register 26h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | K_NO_OF_FRAMES_PER_MULTIFRAME | | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | | |

**表 44. Register 26h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | R/W | 0h | Must read or write 0 |
| 4-0 | K_NO_OF_FRAMES_PER_MULTIFRAME | R/W | 0h | These bits set the number of frames per multi-frame. The K value used is set value + 1 (for example, if the set value is 0xF, then K = 16). |


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#### 7.6.1.1.4.7 Register 28h (address = 28h) [reset = 0h], SERDES_XX Page

**图 113. Register 28h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | CTRL_LID | 0 | 0 | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 45. Register 28h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R/W | 0h | Must read or write 0 |
| 3 | CTRL_LID | R/W | 0h | This bit is the enable bit to program the lane ID (LID).<br>0 : Default LID<br>1 : Enable LID programming |
| 2-0 | 0 | R/W | 0h | Must read or write 0 |

#### 7.6.1.1.4.8 Register 2Dh (address = 2Dh) [reset = 0h], SERDES_XX Page

**图 114. Register 2Dh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LID1 | | | | LID2 | | | |
| R/W-0h | | | | R/W-0h | | | |

**表 46. Register 2Dh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | LID1 | R/W | 0h | Lane ID for channels A, C. Select SerDes AB for channel A and SerDes CD for channel C.<br>Valid only when CTRL_LID = 1. |
| 3-0 | LID2 | R/W | 0h | Lane ID for channels B, D. Select SerDes AB for channel B and SerDes CD for channel D. |

#### 7.6.1.1.4.9 Register 36h (address = 36h) [reset = 0h], SERDES_XX Page

**图 115. Register 36h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PRBS_MODE | | 0 | 0 | 0 | 0 | 0 | 0 |
| R-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 47. Register 36h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | PRBS_MODE | R | 0h | These bits select the PRBS polynomial in the PRBS pattern mode.<br>0 : PRBS7<br>1 : PRBS15<br>2 : PRBS23<br>3 : PRBS31 |
| 5-0 | 0 | R/W | 0h | Must read or write 0 |

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#### 7.6.1.1.4.10 Register 41h (address = 41h) [reset = 0h], SERDES_XX Page

**图 116. Register 41h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LANE_BONA | | | | LANE_AONB | | | |
| R/W-0h | | | | R/W-0h | | | |

**表 48. Register 41h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | LANE_BONA | R/W | 0h | These bits enable lane swap.<br>0 : Default<br>10 : For SerDes AB, channel B on lane A; for SerDes CD, channel D on lane C<br>Others: Do not use |
| 3-0 | LANE_AONB | R/W | 0h | These bits enable lane swap.<br>0 : Default<br>10 : For SerDes AB, channel A on lane B; for SerDes CD, channel C on lane D<br>Others: Do not use |

#### 7.6.1.1.4.11 Register 42h (address = 42h) [reset = 0h], SERDES_XX Page

**图 117. Register 42h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | INVERT_AC | | INVERT_BD | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | R/W-0h | |

**表 49. Register 42h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R/W | 0h | Must read or write 0 |
| 3-2 | INVERT_AC | R/W | 0h | These bits invert lanes A and C.<br>0 : No inversion<br>3 : Data inversion on lane A, C<br>Others: Do not use |
| 1-0 | INVERT_BD | R/W | 0h | These bits invert lanes B and D.<br>0 : No inversion<br>3 : Data inversion on lane B, D<br>Others: Do not use |


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#### 7.6.1.1.5 CHX Page Register Description

##### *7.6.1.1.5.1 Register 26h (address = 26h) [reset = 0h], CHX Page*

**图 118. Register 26h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | GAINWORD | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |

**表 50. Register 26h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0h | Must read or write 0 |
| 1-0 | GAINWORD | R/W | 0h | These bits control the channel A gain word.<br>0 : 0 dB<br>1 : 1 dB<br>2 : 2 dB<br>3 : 3 dB |

##### *7.6.1.1.5.2 Register 27h (address = 27h) [reset = 0h], CHX Page*

**图 119. Register 27h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OVR_ENABLE | OVR_FAST_SEL | 0 | 0 | OVR_LSB1 | 0 | OVR_LSB0 | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 51. Register 27h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | OVR_ENABLE | R/W | 0h | This bit enables or disables the OVR on the JESD lanes.<br>0 : Disables OVR<br>1 : Enables OVR |
| 6 | OVR_FAST_SEL | R/W | 0h | This bit selects the fast or delay-matched OVR.<br>0 : Delay-matched OVR<br>1 : Fast OVR |
| 5-4 | 0 | R/W | 0h | Must read or write 0 |
| 3 | OVR_LSB1 | R/W | 0h | This bit selects either data or OVR on LSB1.<br>0 : Data selected<br>1 : OVR or FOVR selected |
| 2 | 0 | R/W | 0h | Must read or write 0 |
| 1 | OVR_LSB0 | R/W | 0h | This bit selects either data or OVR on LSB0.<br>0 : Data selected<br>1 : OVR or FOVR selected |
| 0 | 0 | R/W | 0h | Must read or write 0 |

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#### *7.6.1.1.5.3 Register 2Dh (address = 2Dh) [reset = 0h], CHX Page*

**图 120. Register 2Dh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | NYQUIST_SELECT | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 52. Register 2Dh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0h | Must read or write 0 |
| 1 | NYQUIST_SELECT | R/W | 0h | This bit selects the Nyquist zone of operation for trim loading.<br>0 : Nyquist 1<br>1 : Nyquist 2 |
| 0 | 0 | R/W | 0h | Must read or write 0 |

#### *7.6.1.1.5.4 Register 78h (address = 78h) [reset = 0h], CHX Page*

**图 121. Register 78h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | FS4_SIGN | NYQ_SEL_MODE02 | NYQ_SEL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 53. Register 78h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | R/W | 0h | Must read or write 0 |
| 2 | FS4_SIGN | R/W | 0h | This bit controls the sign of mixing in mode 0.<br>0 : Centered at $-f_S / 4$<br>1 : Centered at $f_S / 4$ |
| 1 | NYQ_SEL_MODE02 | R/W | 0h | This bit selects the pass band of the decimation filter in mode 2.<br>0 : Low pass<br>1 : High pass |
| 0 | NYQ_SEL | R/W | 0h | This bit selects the pass band of the filter before the DDC.<br>0 : LPF ($0 – f_S / 2$)<br>1 : HPF ($0 – f_S / 2$) |


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#### 7.6.1.1.5.5 Register 7Ah (address = 7Ah) [reset = 0h], CHX Page

**图 122. Register 7Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NCO_WORD[15:8] | | | | | | | |
| R/W-0h | | | | | | | |

**表 54. Register 7Ah Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | NCO_WORD[15:8] | R/W | 0h | These bits set the NCO frequency word.<br>0 : 0 × $f_S$ / $2^{16}$<br>1 : 1 × $f_S$ / $2^{16}$<br>2 : 2 × $f_S$ / $2^{16}$<br>3 : 3 × $f_S$ / $2^{16}$<br>5 : 5 × $f_S$ / $2^{16}$<br>6 : 6 × $f_S$ / $2^{16}$<br>…<br>65535 : 65535 × $f_S$ / $2^{16}$ |

#### 7.6.1.1.5.6 Register 7Bh (address = 7Bh) [reset = 0h], CHX Page

**图 123. Register 7Bh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NCO_WORD[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**表 55. Register 7Bh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | NCO_WORD[7:0] | R/W | 0h | These bits set the NCO frequency word.<br>0 : 0 × $f_S$ / $2^{16}$<br>1 : 1 × $f_S$ / $2^{16}$<br>2 : 2 × $f_S$ / $2^{16}$<br>3 : 3 × $f_S$ / $2^{16}$<br>5 : 5 × $f_S$ / $2^{16}$<br>6 : 6 × $f_S$ / $2^{16}$<br>…<br>65535 : 65535 × $f_S$ / $2^{16}$ |

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#### 7.6.1.1.5.7 Register 7Eh (address = 7Eh) [reset = 3h], CHX Page

图 124. Register 7Eh

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | MODE467_GAIN | MODE0_GAIN | MODE13_GAIN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-1h | R/W-1h |

表 56. Register 7Eh Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | R/W | 0h | Must read or write 0 |
| 2 | MODE467_GAIN | R/W | 0h | This bit sets the mixer loss compensation for modes 4, 6, and 7.<br>0 : No gain<br>1 : 6-dB gain |
| 1 | MODE0_GAIN | R/W | 1h | This bit sets the mixer loss compensation for mode 0.<br>0 : No gain<br>1 : 6-dB gain |
| 0 | MODE13_GAIN | R/W | 1h | This bit sets the mixer loss compensation for modes 1 and 3.<br>0 : No gain<br>1 : 6-dB gain |

### 7.6.1.1.6 ADCXX Page Register Description

#### 7.6.1.1.6.1 Register 07h (address = 07h) [reset = FFh], ADCXX Page

图 125. Register 7h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FAST_OVR_THRESHOLD_HIGH | | | | | | | |
| R/W-FFh | | | | | | | |

表 57. Register 07h Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | FAST_OVR_THRESHOLD_HIGH | R/W | FFh | Fast OVR threshold high; see the *Overrange Indication* section for programming. |

#### 7.6.1.1.6.2 Register 08h (address = 08h) [reset = 0h], ADCXX Page

图 126. Register 8h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FAST_OVR_THRESHOLD_LOW | | | | | | | |
| R/W-0h | | | | | | | |

表 58. Register 08h Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | FAST_OVR_THRESHOLD_LOW | R/W | 0h | Fast OVR threshold low; see the *Overrange Indication* section for programming. |


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#### *7.6.1.1.6.3 Register D5h (address = D5h) [reset = 0h], ADCXX Page*

**图 127. Register D5h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | CAL_EN | 0 | 0 | 0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 59. Register D5h Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R/W | 0h | Must read or write 0 |
| 3 | CAL_EN | R/W | 0h | This bit is the enable calibration bit. This bit must be toggled during the startup sequence.<br>0 : Disables calibration<br>1 : Enables calibration |
| 2-0 | 0 | R/W | 0h | Must read or write 0 |

#### *7.6.1.1.6.4 Register 2Ah (address = 2Ah) [reset = 0h], ADCXX Page*

**图 128. Register 2Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | ADC_TRIM1 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 60. Register 2Ah Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R/W | 0h | Must read or write 0 |
| 0 | ADC Trim1 | R/W | 1h | Always write 0 |

#### *7.6.1.1.6.5 Register CFh (address = CFh) [reset = 0h], ADCXX Page*

**图 129. Register CFh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADC_TRIM2 | | | | 0 | 0 | 0 | 0 |
| R/W-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

**表 61. Register CFh Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | ADC_TRIM2 | R/W | 0h | Always write 5 |
| 3-0 | 0 | R/W | 0h | Must read or write 0 |

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# 8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 Start-Up Sequence

表 62 lists the recommended start-up sequence for a 500-MSPS, Nyquist 2 operation with DDC mode 8 enabled.

**表 62. Recommended Start-Up Sequence for 500-MSPS, Nyquist 2, DDC Bypass Mode (Mode 8) Operation**

| STEP | DESCRIPTION | REGISTER ADDRESS | REGISTER DATA | COMMENT |
|---|---|---|---|---|
| 1 | Provide a 1.15-V power supply (AVDD, DVDD) | — | — | — |
| 2 | Provide a 1.9-V power supply (AVDD19) | — | — | A 1.15-V supply must be supplied first for proper operation. |
| 3 | Provide a clock to CLKINM, CLKINP and a SYSREF signal to SYSREFM, SYSREFP | — | — | SYSREF must be established before SPI programming. |
| 4 | Pulse a reset (low to high to low) via a hardware reset (pin 48), wait 100 µs | — | — | Hardware reset loads all trim register settings. |
| 5 | Issue a software reset to initialize the registers | 00h | 81h | — |
| 6 | Set the high SNR mode for channel pairs AB and CD, select trims for 500-MSPS operation | 11h | 00h | Select the DIGTOP page. |
| | | 12h | 01h | |
| | | 13h | 00h | |
| | | ABh | 01h | Set the high SNR mode for channels A and B. |
| | | ACh | 01h | Set the high SNR mode for channels C and D. |
| | | ADh | 08h | Select DDC bypass mode (mode 8) for channels A and B. |
| | | AEh | 08h | Select DDC bypass mode (mode 8) for channels C and D. |
| | | 64h | 02h | Select trims for 500-MSPS operation. |
| 7 | Set up the SerDes configuration | 11h | 00h | Select the SerDes_AB and SerDes_CD pages. |
| | | 12h | 60h | |
| | | 13h | 00h | |
| | | 26h | 0Fh | Set the K value to 16 frames per multi-frame. |
| | | 20h | 80h | Enable the K value from register 26h. |
| 8 | ADC calibration | 11h | FFh | Select the ADC_A1, ADC_A2, ADC_B1, ADC_B2, ADC_C1, ADC_C2, ADC_D1, and ADC_D2 pages. |
| | | 12h | 00h | |
| | | 13h | 00h | |
| | | D5h | 08h | Enable ADC calibration. |
| | | Wait 2 ms | | ADC calibration time. |
| | | D5h | 00h | Disable ADC calibration. |
| | | 2Ah | 00h | Internal trims. |
| | | CFh | 50h | |
| 9 | Select trims for the second Nyquist | 11h | 00h | Select the channel A, channel B, channel C, and channel D pages. |
| | | 12h | 1Eh | |
| | | 13h | 00h | |
| | | 2Dh | 02h | Select trims for the second Nyquist. |


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## Application Information (接下页)

### 表 62. Recommended Start-Up Sequence for 500-MSPS, Nyquist 2, DDC Bypass Mode (Mode 8) Operation (接下页)

| STEP | DESCRIPTION | REGISTER ADDRESS | REGISTER DATA | COMMENT |
|---|---|---|---|---|
| 10 | Load linearity trims | 11h | 00h | Select the DIGTOP page. |
| | | 12h | 01h | |
| | | 13h | 00h | |
| | | 8Ch | 02h | Load linearity trims. |
| | | B7h | 01h | |
| | | B7h | 00h | |
| 11 | Disable SYSREF | 11h | 00h | Select the ANALOG page. |
| | | 12h | 00h | |
| | | 13h | 01h | |
| | | 6Ah | 02h | Disable SYSREF. |

表 63 lists the recommended start-up sequence for a 500-MSPS, Nyquist 2, 2x interleaved dual ADC operation.

### 表 63. Recommended Start-Up Sequence for 500-MSPS, Nyquist 2, 2x Interleaved Dual ADC Operation

| STEP | DESCRIPTION | REGISTER ADDRESS | REGISTER DATA | COMMENT |
|---|---|---|---|---|
| 1 | Provide a 1.15-V power supply (AVDD, DVDD) | — | — | — |
| 2 | Provide a 1.9-V power supply (AVDD19) | — | — | A 1.15-V supply must be supplied first for proper operation. |
| 3 | Provide a clock to CLKINM, CLKINP and a SYSREF signal to SYSREFM, SYSREFP | — | — | SYSREF must be established before SPI programming. |
| 4 | Pulse a reset (low to high to low) via a hardware reset (pin 48), wait 100 µs | — | — | Hardware reset loads all trim register settings. |
| 5 | Issue a software reset to initialize the registers | 00h | 81h | — |
| 6 | Set the high SNR mode for channel pairs AB and CD, select trims for 500-MSPS operation | 11h | 00h | Select the DIGTOP page. |
| | | 12h | 01h | |
| | | 13h | 00h | |
| | | A5h | 03h | Enable averaging on the AB and CD channel pair. |
| | | A6h | 20h | Enable the averaging option. |
| | | ABh | 03h | Set the high SNR and interleave mode for channels A and B. |
| | | ACh | 03h | Set the high SNR and interleave mode for channels C and D. |
| | | ADh | 08h | Select DDC bypass mode (mode 8) for channels A and B. |
| | | AEh | 08h | Select DDC bypass mode (mode 8) for channels C and D. |
| | | 64h | 02h | Select trims for 500-MSPS operation. |
| 7 | Set up the SerDes configuration | 11h | 00h | Select the SERDES_AB and SERDES_CD pages. |
| | | 12h | 60h | |
| | | 13h | 00h | |
| | | 26h | 0Fh | Set the K value to 16 frames per multi-frame. |
| | | 20h | 80h | Enable the K value from register 26h. |

**表 63. Recommended Start-Up Sequence for 500-MSPS, Nyquist 2, 2x Interleaved Dual ADC Operation (接下页)**

| STEP | DESCRIPTION | REGISTER ADDRESS | REGISTER DATA | COMMENT |
|---|---|---|---|---|
| 8 | ADC calibration | 11h | FFh | Select the ADC_A1, ADC_A2, ADC_B1, ADC_B2, ADC_C1, ADC_C2, ADC_D1, and ADC_D2 pages. |
| | | 12h | 00h | |
| | | 13h | 00h | |
| | | D5h | 08h | Enable ADC calibration. |
| | | Wait 2 ms | | ADC calibration time. |
| | | D5h | 00h | Disable ADC calibration. |
| | | 2Ah | 00h | Internal trims. |
| | | CFh | 50h | |
| 9 | Select trims for the second Nyquist | 11h | 00h | Select the channel A, channel B, channel C, and channel D pages. |
| | | 12h | 1Eh | |
| | | 13h | 00h | |
| | | 2Dh | 02h | Select trims for the second Nyquist. |
| 10 | Load linearity trims | 11h | 00h | Select the DIGTOP page. |
| | | 12h | 01h | |
| | | 13h | 00h | |
| | | 8Ch | 02h | Load linearity trims. |
| | | B7h | 01h | |
| | | B7h | 00h | |
| 11 | Disable SYSREF | 11h | 00h | Select the ANALOG page. |
| | | 12h | 00h | |
| | | 13h | 01h | |
| | | 6Ah | 02h | Disable SYSREF. |


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### 8.1.2 Hardware Reset

图 130 shows the timing information for the hardware reset.

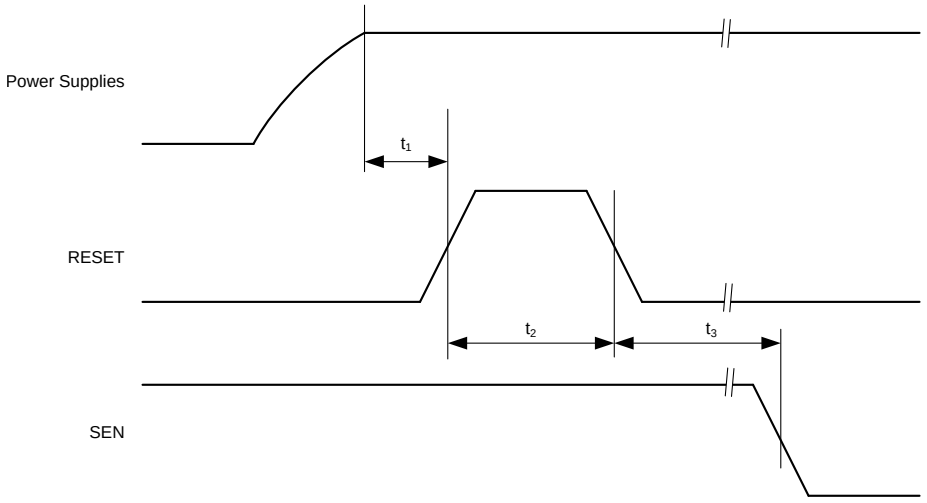



**图 130. Hardware Reset Timing Diagram**

**表 64. Timing Requirements for 图 130**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_1$ | Power-on delay from power-up to an active high RESET pulse | 1 | | | ms |
| $t_2$ | Reset pulse duration: active high RESET pulse duration | 10 | | | ns |
| $t_3$ | Register write delay from RESET disable to SEN active | 100 | | | µs |

### 8.1.3 Frequency Planning

The ADS54J64 uses an architecture where the ADCs are 2x interleaved followed by a digital decimation by 2. The 2x interleaved and decimation architecture comes with a unique advantage of improved linearity resulting from frequency planning. Frequency planning refers to choosing the clock frequency and signal band appropriately such that the harmonic distortion components, resulting from the analog front-end (LNA, PGA), can be made to fall outside the decimation filter pass band. In absence of the 2x interleave and decimation architecture, these components alias back in band and limit the performance of the signal chain. For example, for $f_{CLK}$ = 983.04 MHz and $f_{IN}$ = 184.32 MHz:

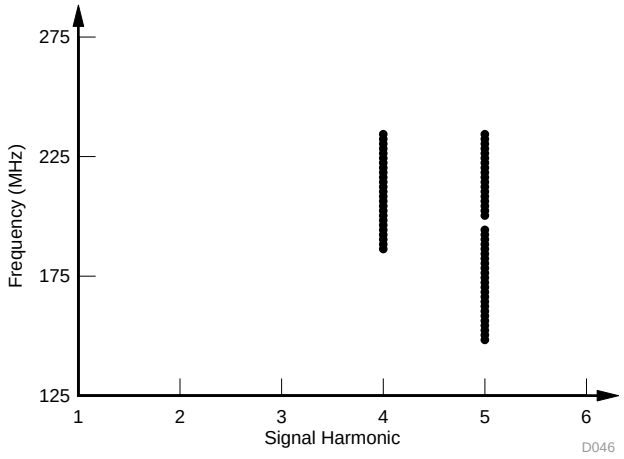
Second-order harmonic distortion (HD2) = 2 × 184.32 = 368.64 MHz

Pass band of the 2x decimation filter = 0 MHz to 245.76 MHz (0 to $f_{CLK}$ / 4)

The second-order harmonic performance improves by the stop-band attenuation of the filter (approximately 40 dBc) because the second-order harmonic frequency is outside the pass band of the decimation filter.

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图 131 shows the harmonic components (HD2–HD5) that fall in the decimation pass band for the input clock rate ($f_{CLK}$) of the 983.04-MHz and 100-MHz signal band around the center frequency of 184.32 MHz.




NOTE: $f_{CLK}$ = 983.04 MHz, signal band = 134.32 MHz to 234.32 MHz.

**图 131. In-Band Harmonics for a Frequency Planned System**

As shown in 图 131, both HD2 and HD3 are completely out of band. HD4 and HD5 fall in the decimation pass band for some frequencies of the input signal band.

Through proper frequency planning, the specifications of the ADC antialias filter can be relaxed.

### 8.1.4 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors (as shown in 公式 3): the quantization noise is typically not noticeable in pipeline converters and is 84 dB for a 14-bit ADC. The thermal noise limits the SNR at low input frequencies and the clock jitter sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20log\sqrt{\left(10^{-\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (3)$$

公式 4 calculates the SNR limitation resulting from sample clock jitter:

$$SNR_{Jitter}[dBc] = -20log\left(2\pi \times f_{in} \times T_{Jitter}\right) \quad (4)$$

The total clock jitter ($T_{Jitter}$) has two components: the internal aperture jitter (100 $f_S$ for the ADS54J64) that is set by the noise of the clock input buffer and the external clock jitter. 公式 5 calculates $T_{Jitter}$:

$$T_{Jitter} = \sqrt{\left(T_{Jitter,\ Ext_Clock_Input}\right)^2 + \left(T_{Aperture_ADC}\right)^2} \quad (5)$$

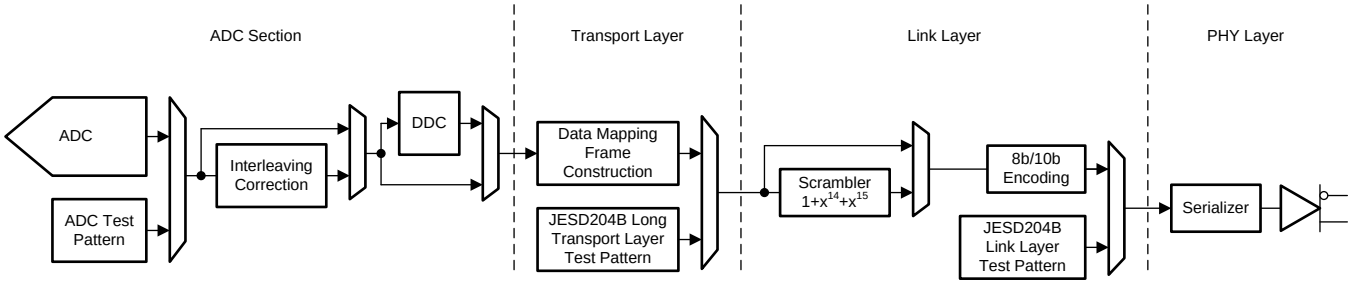
External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input; a faster clock slew rate also improves the ADC aperture jitter.

The ADS54J64 has a thermal noise of approximately 70 dBFS and an internal aperture jitter of 100 $f_S$.


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### 8.1.5 ADC Test Pattern

The ADS54J64 provides several different options to output test patterns instead of the actual output data of the ADC in order to simplify debugging of the JESD204B digital interface link. 图 132 shows the output data path.




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**图 132. ADC Test Pattern**

#### *8.1.5.1 ADC Section*

The ADC test pattern replaces the actual output data of the ADC. These test patterns can be programmed using register 91h of the DIGTOP page. 表 65 lists the supported test patterns.

**表 65. ADC Test Pattern Settings**

| BIT | NAME | DEFAULT | DESCRIPTION |
|---|---|---|---|
| 7-4 | TESTPATTERNSELECT | 0000 | These bits select the test pattern on the output when the test pattern is enabled for a suitable channel.<br>0 : Default<br>1 : All zeros<br>2 : All ones<br>3 : Toggle pattern<br>4 : Ramp pattern<br>6 : Custom pattern 1<br>7 : Toggles between custom pattern 1 and custom pattern 2<br>8 : Deskew pattern (AAAAh) |

#### *8.1.5.2 Transport Layer Pattern*

The transport layer maps the ADC output data into 8-bit octets and constructs the JESD204B frames using the LMFS parameters. Tail bits or 0s are added when needed. Alternatively, as shown in 表 66, the JESD204B long transport layer test pattern can be substituted by programming register 20h.

**表 66. Transport Layer Test Mode**

| BIT | NAME | DEFAULT | DESCRIPTION |
|---|---|---|---|
| 4 | TRANS_TEST_EN | 0 | This bit generates the long transport layer test pattern mode according to clause 5.1.6.3 of the JESD204B specification.<br>0 = Test mode disabled<br>1 = Test mode enabled |

### 8.1.5.3 Link Layer Pattern

The link layer contains the scrambler and the 8b, 10b encoding of any data passed on from the transport layer. Additionally, the link layer also handles the initial lane alignment sequence that can be manually restarted. The link layer test patterns are intended for testing the quality of the link (jitter testing and so forth). The test patterns do not pass through the 8b, 10b encoder. These test patterns can be used by programming register 22h of the SERDES_XX page. 表 67 shows the supported programming options.

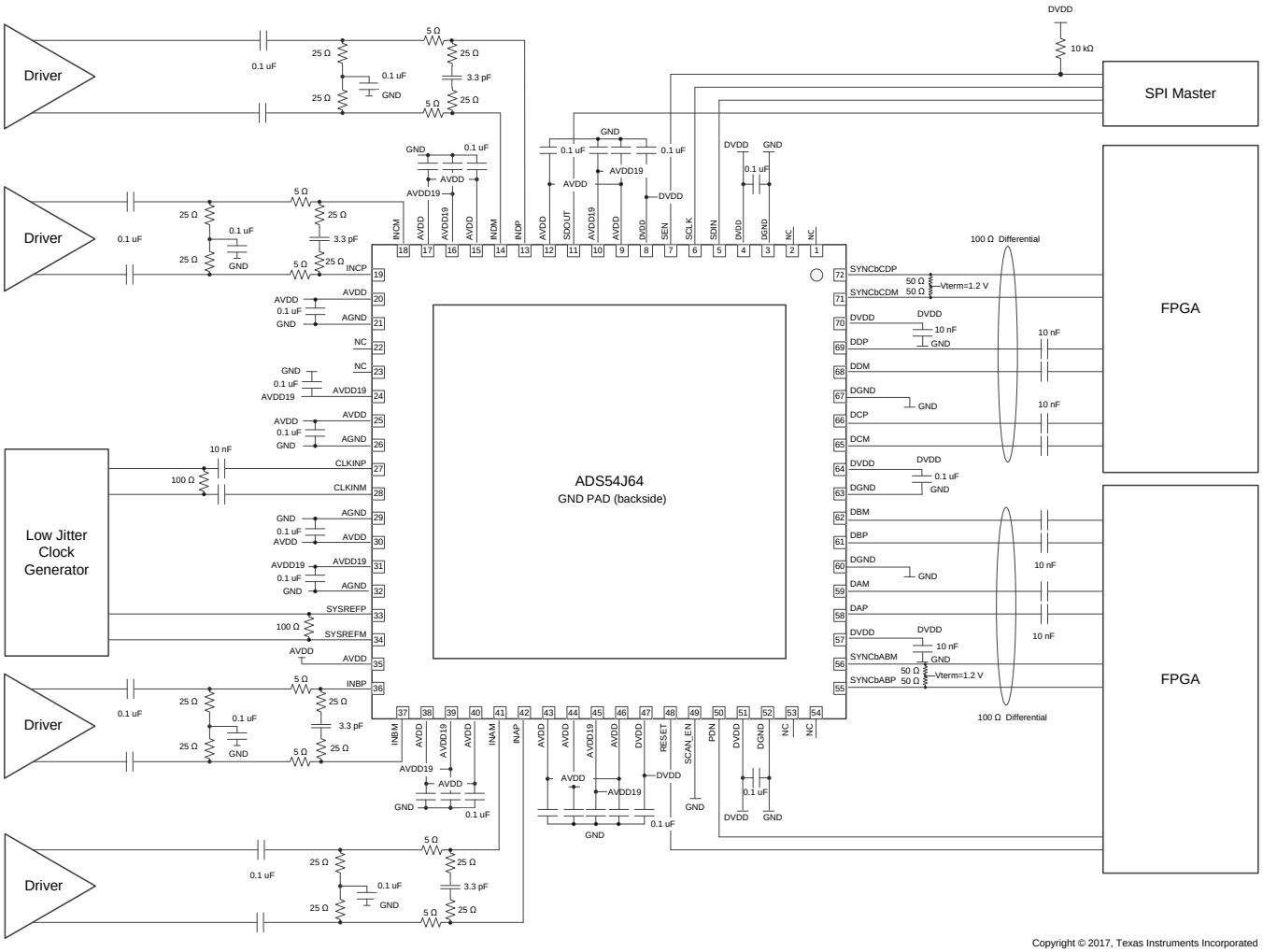
**表 67. Link Layer Test Mode**

| BIT | NAME | DEFAULT | DESCRIPTION |
|---|---|---|---|
| 7-5 | LINK_LAYER_TESTMODE_SEL | 000 | These bits generate a pattern according to clause 5.3.3.8.2 of the JESD204B document.<br>0 : Normal ADC data<br>1 : D21.5 (high-frequency jitter pattern)<br>2 : K28.5 (mixed-frequency jitter pattern)<br>3 : Repeats initial lane alignment (generates a K28.5 character and continuously repeats lane alignment sequences)<br>4 : 12-octet RPAT jitter pattern<br>6 : PRBS pattern (PRBS7,15,23,31); use PRBS mode (register 36h) to select the PRBS pattern |


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## 8.2 Typical Application

The ADS54J64 is designed for wideband receiver applications demanding excellent dynamic range over a large input frequency range. 图 133 shows a typical schematic for an ac-coupled dual receiver [dual field-programmable gate array (FPGA) with a dual SYNC].




NOTE: GND = AGND and DGND are connected in the PCB layout.

**图 133. Application Diagram for the ADS54J64**

### 8.2.1 Design Requirements

By using the simple drive circuit of 图 133 (when the amplifier drives the ADC) or 图 46 (when transformers drive the ADC), uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

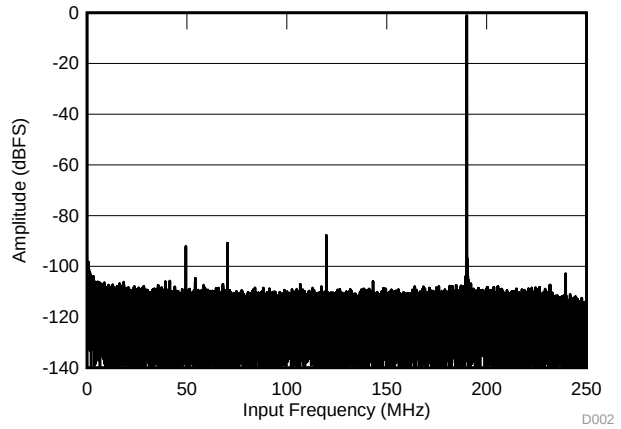
### 8.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin, as shown in 图 133, is recommended to damp out ringing caused by package parasitics.

## Typical Application (接下页)

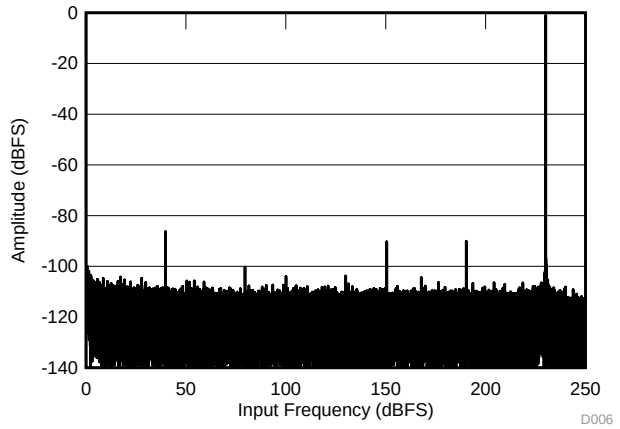
### 8.2.3 Application Curves

图 134 and 图 135 show the typical performance at 190 MHz and 230 MHz, respectively.




$f_{IN}$ = 190 MHz, $A_{IN}$ = –1 dBFS,
SNR = 69.4 dBFS, SFDR = 88 dBc, SFDR = 96 dBc (non 23)

**图 134. FFT for 190-MHz Input Signal**




$f_{IN}$ = 230 MHz, $A_{IN}$ = –1 dBFS,
SNR = 69.4 dBFS, SFDR = 85 dBc, SFDR = 96 dBc (non 23)

**图 135. FFT for 230-MHz Input Signal**

## 9 Power Supply Recommendations

The device requires a 1.15-V nominal supply for DVDD, a 1.15-V nominal supply for AVDD, and a 1.9-V nominal supply for AVDD19. AVDD and DVDD are recommended to be powered up the before the AVDD19 supply for reliable loading of factory trims.


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# 10 Layout

## 10.1 Layout Guidelines

The device evaluation module (EVM) layout can be used as a reference layout to obtain the best performance. 图 136 shows a layout diagram of the EVM top layer. A complete layout of the EVM is available at the ADS54J64 EVM folder. Some important points to remember during board layout are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pinout in opposite directions, as shown in the reference layout of 图 136 as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of 图 136 as much as possible.
- Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as an FPGA or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD, DVDD, or AVDD19), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

## 10.2 Layout Example

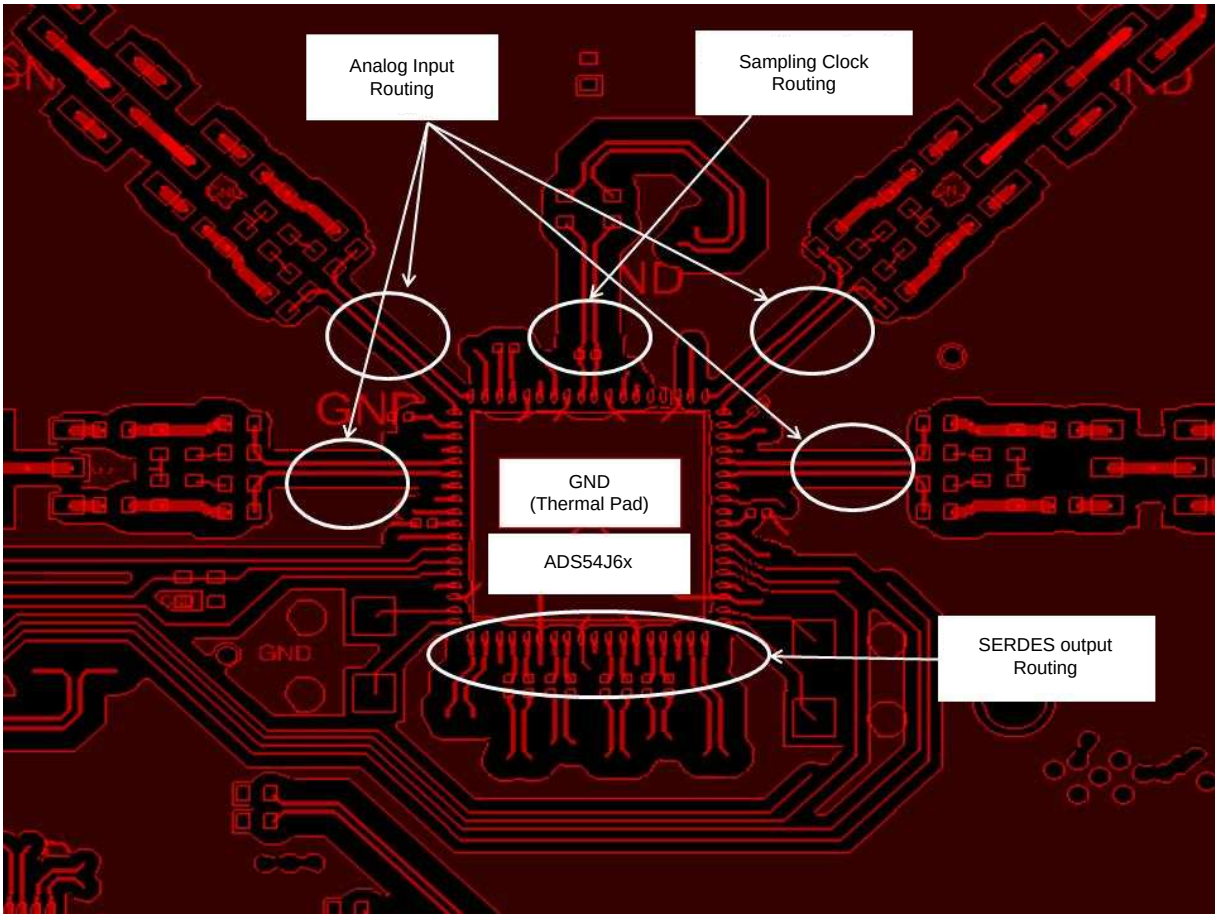



**图 136. ADS54J64EVM Layout**

# 11 器件和文档支持

## 11.1 接收文档更新通知

要接收文档更新通知，请转至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 11.2 社区资源

**下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。**

**TI E2E™ 在线社区** ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

**设计支持** ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

## 11.3 商标

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## 11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ADS54J64IRMP | Active | Production | VQFN (RMP) \| 72 | 168 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ54J64 |
| ADS54J64IRMP.A | Active | Production | VQFN (RMP) \| 72 | 168 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ54J64 |
| ADS54J64IRMPG4 | Active | Production | VQFN (RMP) \| 72 | 168 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ54J64 |
| ADS54J64IRMPG4.A | Active | Production | VQFN (RMP) \| 72 | 168 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ54J64 |
| ADS54J64IRMPT | Active | Production | VQFN (RMP) \| 72 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ54J64 |
| ADS54J64IRMPT.A | Active | Production | VQFN (RMP) \| 72 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ54J64 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

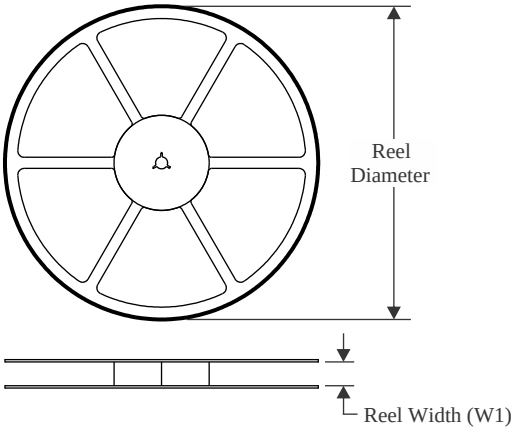
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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

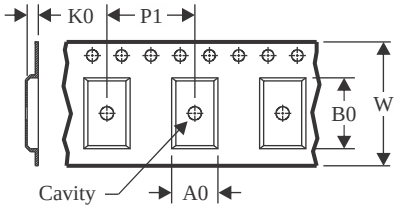
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

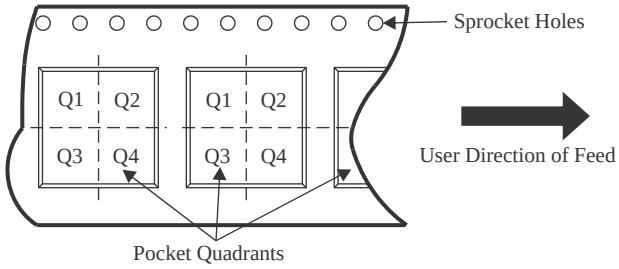



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

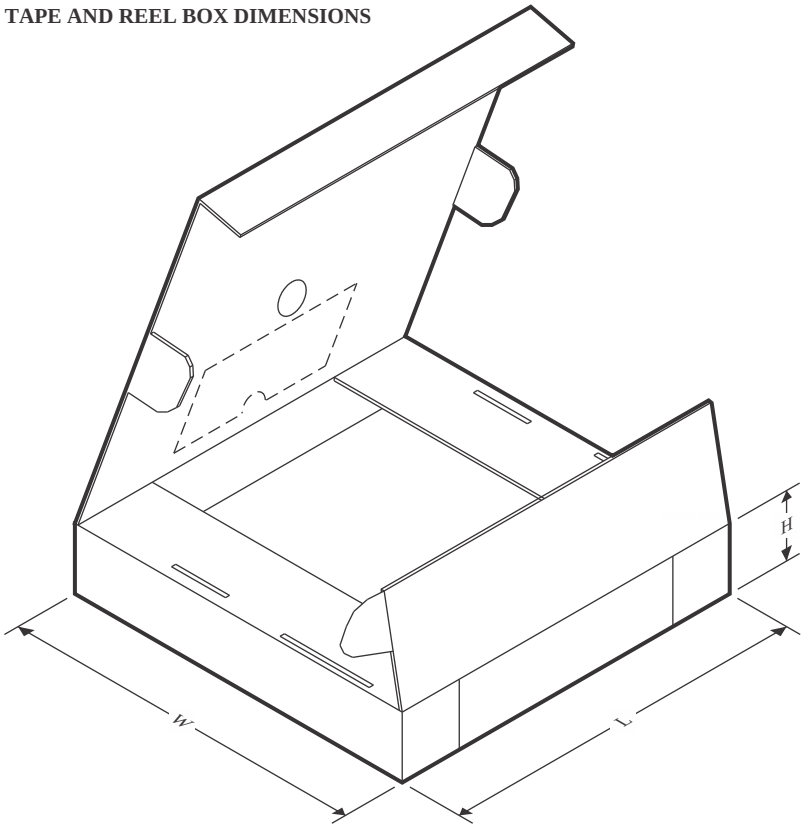
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS54J64IRMPT | VQFN | RMP | 72 | 250 | 180.0 | 24.4 | 10.25 | 10.25 | 2.25 | 16.0 | 24.0 | Q2 |

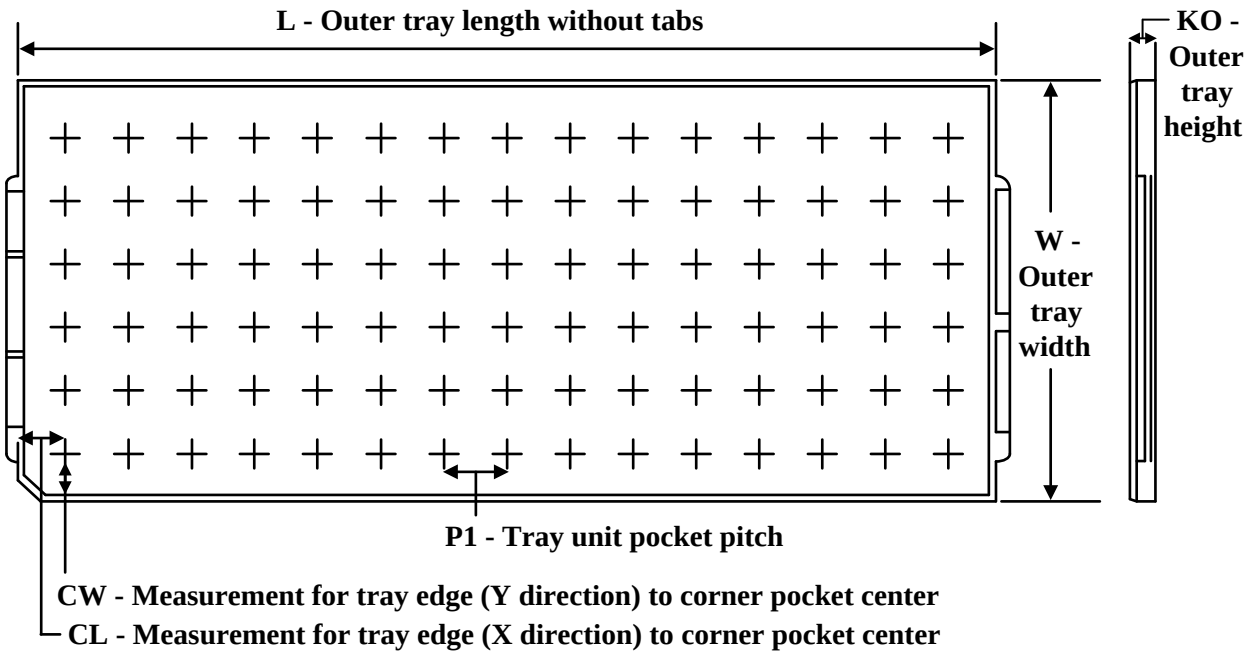
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS54J64IRMPT | VQFN | RMP | 72 | 250 | 213.0 | 191.0 | 55.0 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

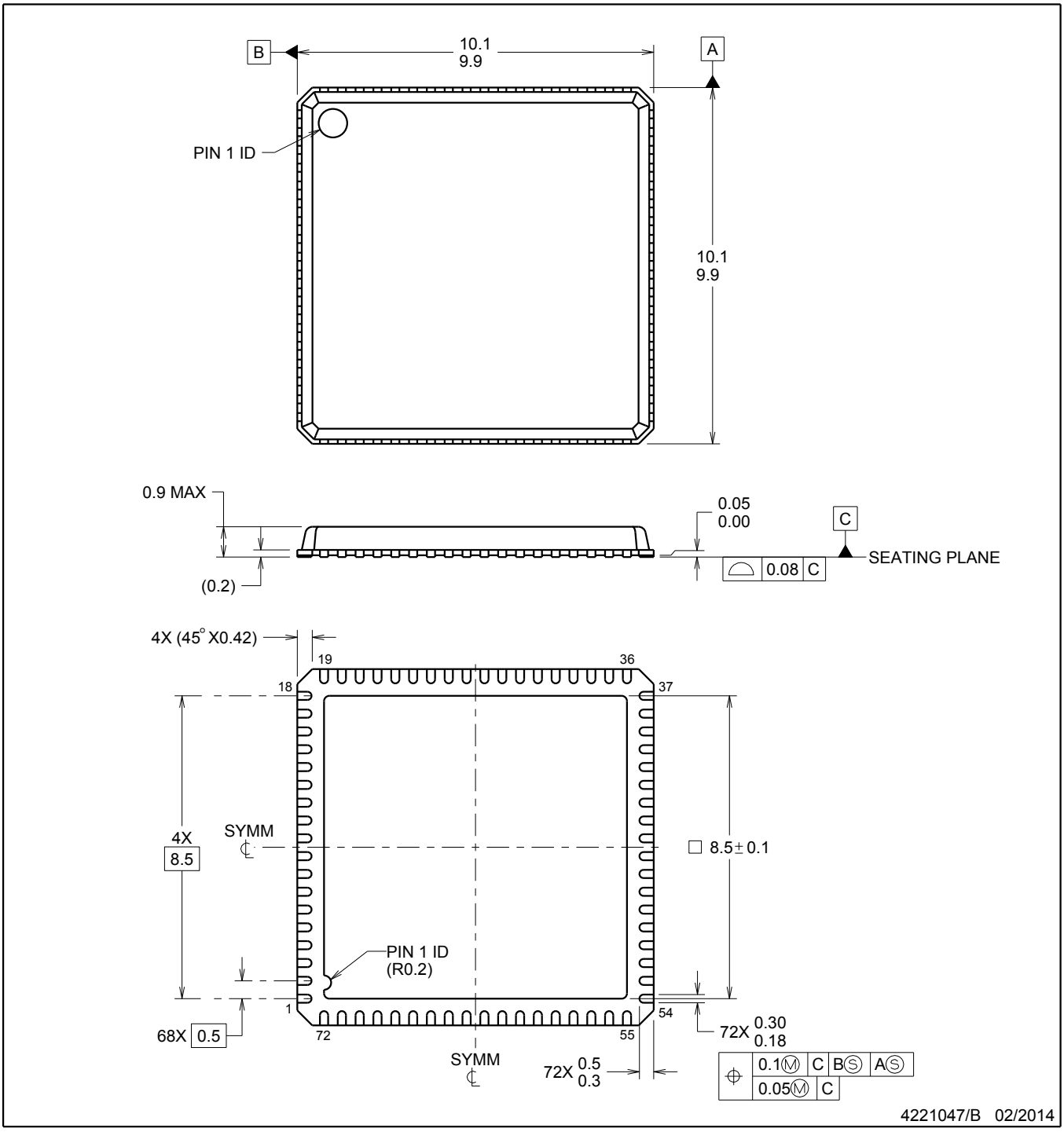
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS54J64IRMP | RMP | VQFNP | 72 | 168 | 8 X 21 | 150 | 315 | 135.9 | 7620 | 14.65 | 11 | 11.95 |
| ADS54J64IRMP.A | RMP | VQFNP | 72 | 168 | 8 X 21 | 150 | 315 | 135.9 | 7620 | 14.65 | 11 | 11.95 |
| ADS54J64IRMPG4 | RMP | VQFNP | 72 | 168 | 8 X 21 | 150 | 315 | 135.9 | 7620 | 14.65 | 11 | 11.95 |
| ADS54J64IRMPG4.A | RMP | VQFNP | 72 | 168 | 8 X 21 | 150 | 315 | 135.9 | 7620 | 14.65 | 11 | 11.95 |

# PACKAGE OUTLINE

## RMP0072A

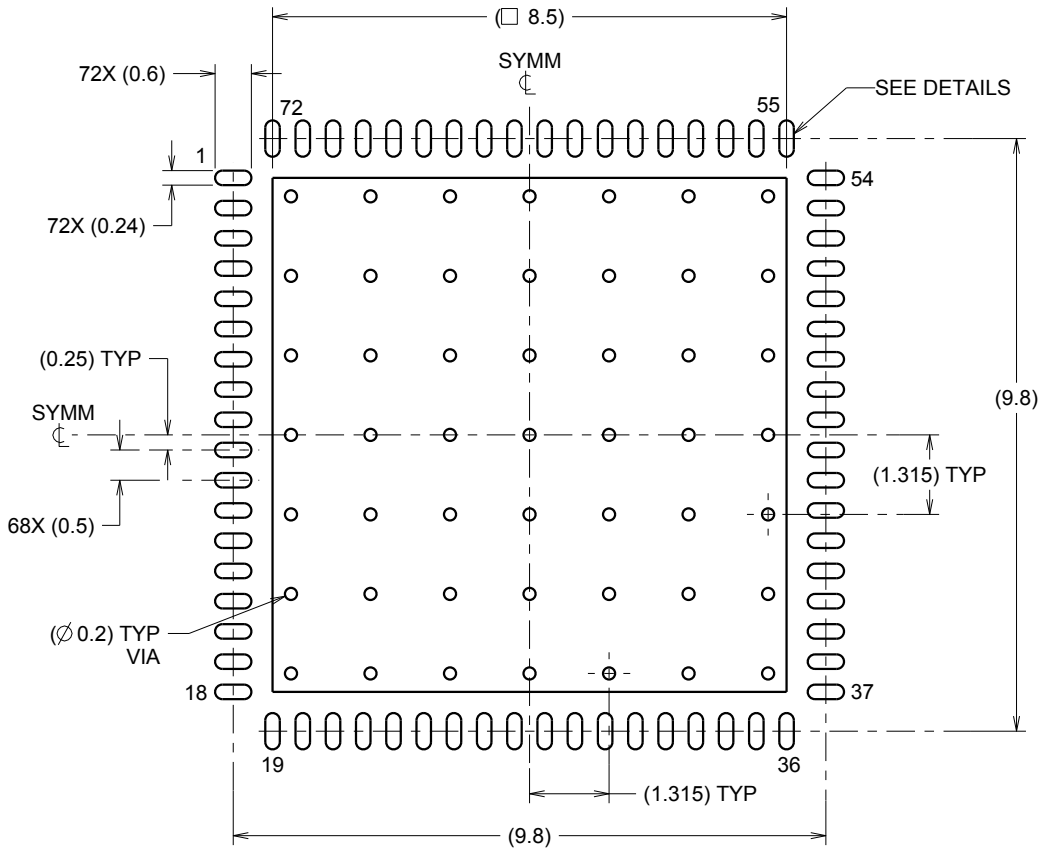
## VQFN - 0.9 mm max height

VQFN

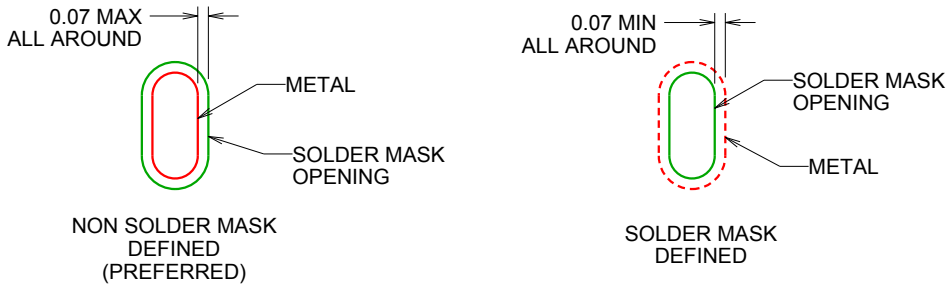



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:8X

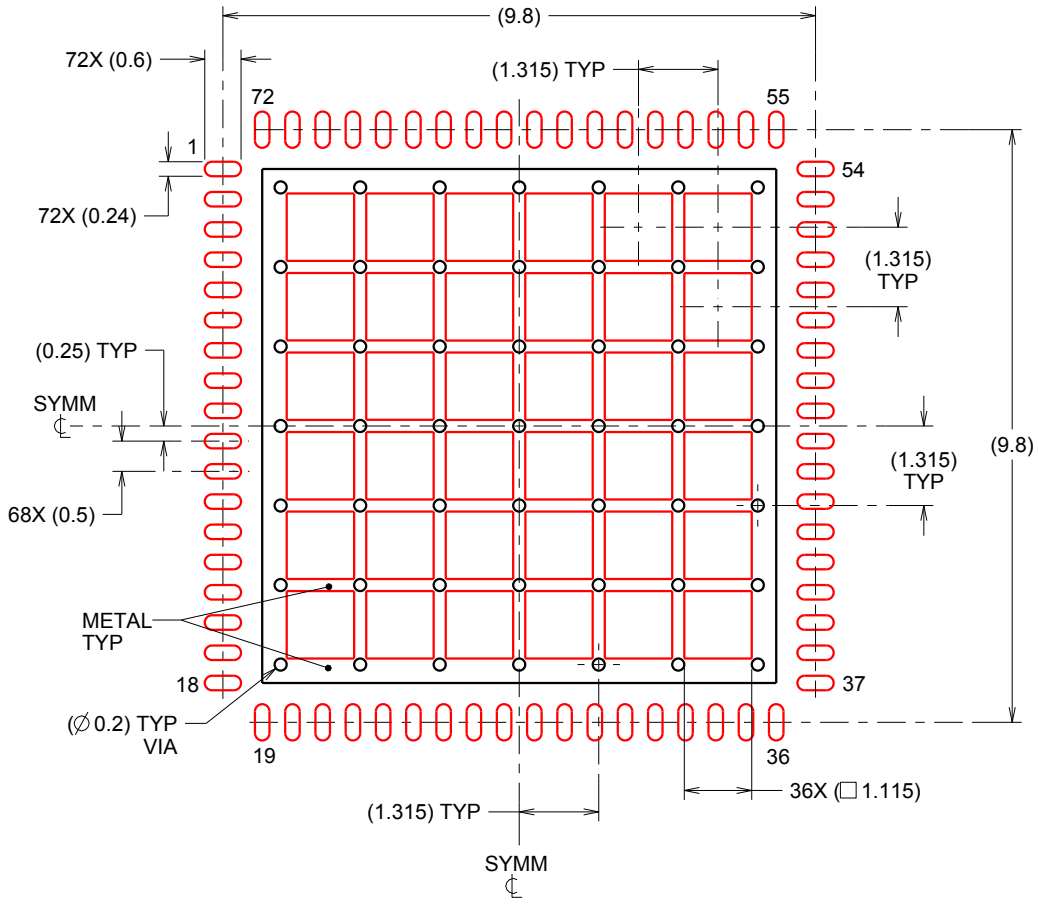



SOLDER MASK DETAILS

4221047/B 02/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4221047/B 02/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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